

# COMPOUND FIELD EFFECT POWER TRANSISTOR $\mu$ PA 1640

## **MONOLITHIC POWER MOS FET ARRAY**

#### **DESCRIPTION**

The  $\mu$ PA1640 is Monolithic N-channel Power MOS FET Array that built in 8 circuits with 2 AND GATE.

In groups of 4 circuits and they each have ENABLE terminal.

## **FEATURES**

- Wired Connection is possible. (Output Step is Open Drain)
- Output Voltage: Vo = 30 V MAX.
   Output Current: Io = 100 mA MAX.
- Wide Operation Temperature: -40 to +85 °C

## **ORDERING INFORMATION**

Part Number	Package	Quality Grade
μPA1640GS	20-Pin SOP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

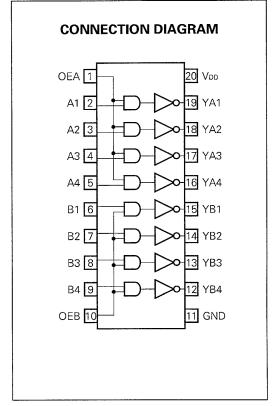
## ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Supply Voltage	VDD	-0.5 to +7.0	V
Output Voltage	Vo	-0.5 to +30	V
Input Voltage	Vı	$-0.5$ to $V_{DD} + 0.5$	V
Output Current	lo	±100	mA
Input Current	lı	-10 to +0.1	mA/unit
Total Power Dissipation	PD	1.0	W/PKG
Operating Temperature	$T_{\text{opt}}$	-40 to +85	°C
Storage Temperature	Tstg	-55 to +150	°C

## **TRUTH TABLE**

INPUT		OUTPUT	INPUT		OUTPUT
OUTPUT			OUTPUT		
ENABLE	Α	YA	ENABLE	В	YB
Α			В		
Н	L	Z	Н	L	Z
Н	Н	L	Н	Н	L
L	Х	Z	L	Х	Z

- H: High-Level
- L: Low-Level
- Z: High-Impedance





# RECOMMENDED OPERATING CONDITIONS ( $T_a = -40 \text{ to } +85 \text{ }^{\circ}\text{C}$ )

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	4.5	5.0	5.5	V
Output Voltage	Vo			24	V
Input Voltage	Vı	0		V <sub>DD</sub>	V
Low-Level Input Voltage	VıL	0		0.3 V <sub>DD</sub>	V
High-Level Input Voltage	Vih	0.7 V <sub>DD</sub>		VDD	V
Low-Level Output Current	loL		48		mA
Operation Temperature	Topt	-10		60	°C

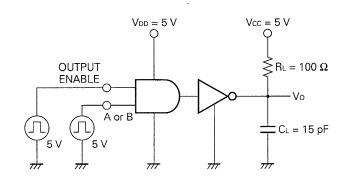
# **ELECTRICAL CHARACTERISTICS (Ta = 25 °C)**

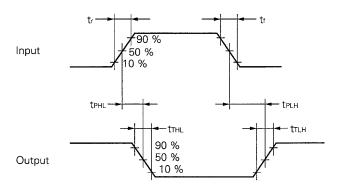
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
	V <sub>OL1</sub>			0.2	V	V <sub>DD</sub> = 4.5 V, V <sub>I</sub> = 2 V, I <sub>O</sub> = 24 mA
Low Level Output Voltage	V <sub>OL2</sub>			0.4	V	V <sub>DD</sub> = 4.5 V, V <sub>I</sub> = 2 V, I <sub>O</sub> = 48 mA
	Vol3			0.8	V	V <sub>DD</sub> = 4.5 V, V <sub>I</sub> = 2 V, I <sub>O</sub> = 100 mA
Output Leakage Current	lπL			5	μΑ	V <sub>DD</sub> = 5.5 V, V <sub>O</sub> = 30 V, V <sub>I</sub> = 0
Low-Level Input Voltage	Vil			1.5	V	$V_{DD} = 5 \text{ V, } V_0 = 30 \text{ V, } lo \le 20 \ \mu\text{A}$
High-Level Input Voltage	ViH	3.5			V	$V_{DD} = 5 \text{ V, } V_0 = 0.4 \text{ V, } lo \ge 48 \text{ mA}$
Input Current	lı .			±1	μΑ	VDD = 5.5 V, VI = 0 or VDD
Quiescent Supply Current	loo			10	μΑ	VDD = 5.5 V, Vi = 0 or VDD, lo = 0
Input Capacitance	Cı		7	15	pF	
Body Equivalent Capacitance	C <sub>pd</sub>		30		рF	

# ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C, V<sub>DD</sub> = V<sub>CC</sub> = 5 V, C<sub>L</sub> = 15 pF, R<sub>L</sub> = 100 $\Omega$ , t<sub>r</sub> = t<sub>f</sub> = 5 ns)

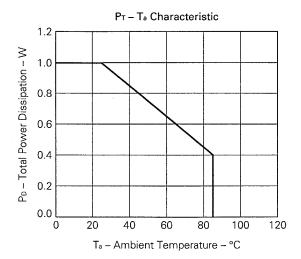
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Delay Time	tpzL tpLz		20	30	ns	A,B → Y, OEA, OEB=H
	tpzL tpLz		20	30	ns	OUTPUT ENABLE → Y, A,B = H
Rise Time	tтьн		20	30	ns	
Fall Time	tтнь		20	30	ns	

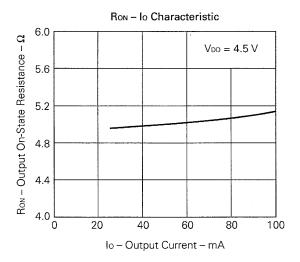
# **SWITCHING WAVE FORMS AND TEST CIRCUITS**

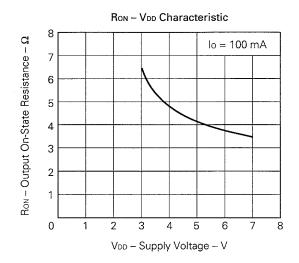


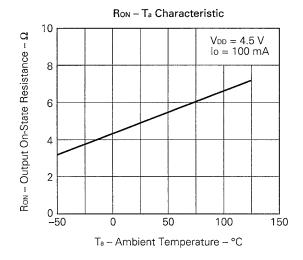


# TYPICAL CHARACTERISTICS (Ta = 25 °C)



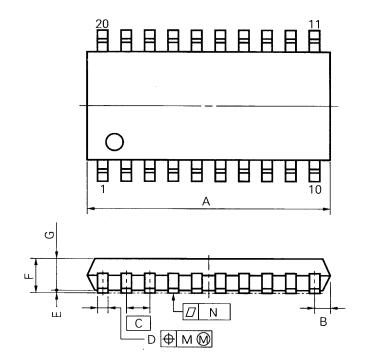


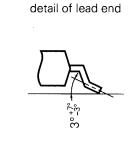


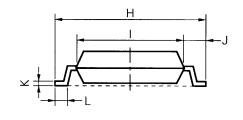


# **PACKAGE DIMENSIONS**

# 20 PIN PLASTIC SOP (300 mil)







P20GM-50-300B,C-3

## NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
А	13.00 MAX.	0.512 MAX.
В	0.78 MAX.	0.031 MAX.
С	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	0.016+0.004
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
Н	7.7±0.3	0.303±0.012
ı	5.6	0.220
J	1.1	0.043
K	0.20+0.10	0.008+0.004
L	0.6±0.2	0.024+0.008
М	0.12	0.005
N	0.10	0.004



## **RECOMMENDED SOLDERING CONDITIONS**

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

## TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SEMICONDUCTOR DEVICES TECHNOLOGY MANUAL" (IEI-1207).  $\mu$ PA1640GS

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 2 or below, Exposure limit*: None	IR35-00-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2 or below, Exposure limit*: None	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: None	WS60-00-1

<sup>\*:</sup> Exposure limit before soldering after dry-pack package is opened. Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

## Reference

Document name	Document No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Semiconductor device package manual	IEI-1213
SMD surface mount technology manual	IEI-1207

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Application examples recommended by NEC Corporation.

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

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