MOS DIGITAL CLOCK

Features

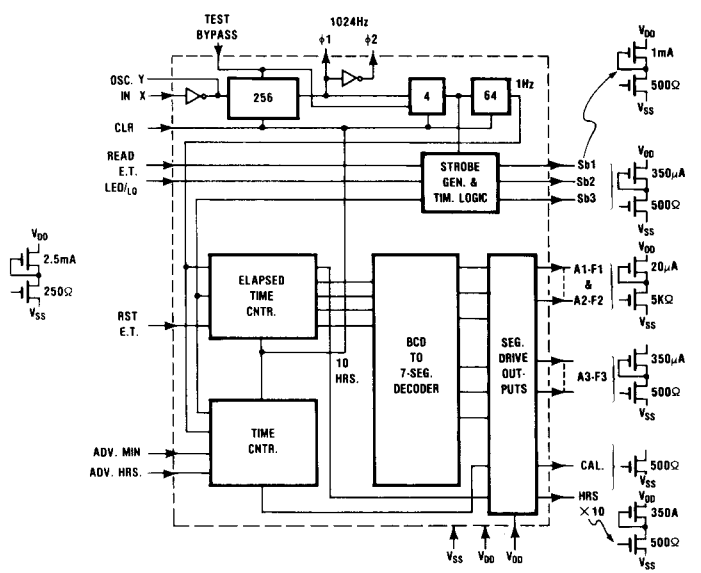
- 262,144 External Quartz Crystal
- Has 20 Hr. Resettable Elapsed Time Counter
- Direct LCD or Tung-sol DT1704 Tube Interface
- Electrically Selectable Multiplexed LED Output
- Minute and Hour SET Controls
- Separate Display Supply Allows Display Turn Off for Reduced Battery Current Drain
- 1024Hz Outputs for Voltage Doubler
- Calendar Advancing or AM/PM Output

General Description

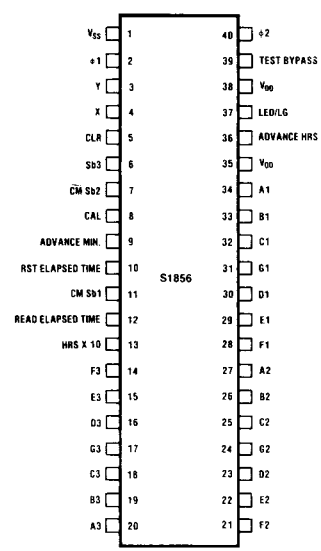
The S1856 Digital Clock provides the circuitry to implement a 4-digit time keeper with separate elapsed time counter. It is an MOS/LSI circuit consisting of down counters, combinational logic, BCD to 7-segment decoder and output buffer transistors in a 40-pin DIP. The circuit has a separate output pin to drive each segment of a Liquid Crystal Display directly. However if the LED mode of operation is selected, only the HRS×10 and F3 through A3 outputs are used to provide segment drive current. In this mode of operation segment drivers F3 through A3 are multiplexed at 25% duty cycle to provide MINUTES, 10's of MINUTES and HOURS information.

The ELAPSED TIME COUNTER can be reset and displayed separately without affecting the state of the time keeper. The ELAPSED TIME COUNTER has the added feature of displaying SECONDS, 10's of SECONDS and MINUTES automatically during the first 10 minutes after a reset has occurred. The counter will then display MINUTES, 10's of MINUTES, HOURS and 10's of HOURS for the remainder for its 20 hours capacity.

Block Diagram



Pin Configuration



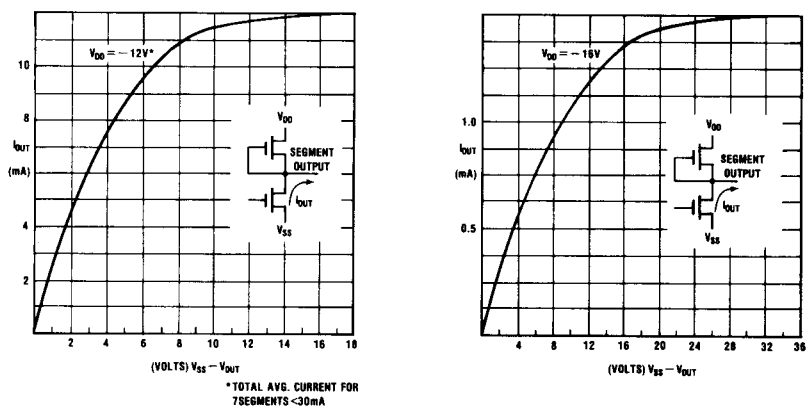
Absolute Maximum Ratings

Positive Voltage on any Pin	$V_{SS}+0.3V$
Negative Voltage on any Pin	$V_{SS}-28V$
Storage Temperature	$-65°C$ to $+150°C$
Operating Temperature	$-40°C$ to $+100°C$

Dynamic Characteristics: $T_A=-40°C$ to $+70°C$, $V_{SS}=0V$, $V_{DD}-6V$ to $-16V$, $V_{OD}-5V$ to $-28V$

Symbol	Min.	Typ.	Max.	Units	Conditions
V_{IL}(OSC X) V_{IH} V_{IH}(Control) V_{IL}	V_{DD} $V_{SS}-1$ $V_{SS}-0.5$ V_{DD}		$V_{SS}-6$ $V_{SS}+0.3$ $V_{SS}+0.3$ $V_{SS}-6$	V V V V	An Internal resistor of 700KΩ (typical) to V_{DD} is provided for all control inputs.
V_{OH}(Outputs)	$V_{SS}-1$			V	Open circuit
V_{OL}			V_{DD}	V	Open circuit
I_{DD}		10	15	mA	$V_{DD}-14V$
I_{DD}		10		mA	$V_{DD}-6V$

Figure 1. Typical Performance Characteristics



Typical Applications

- ☐ Automotive Clock
- ☐ Household Clock With Auxiliary Battery for Accurate Time Keeping During Power Interruptions
- ☐ Appliance Timers
- ☐ Industrial Timers
- ☐ Photographic Timers
- ☐ Avionics Timers
- ☐ Portable Clock

Operational Description

The Clock circuit block diagram is shown on the previous page. The input transistor of the circuit forms an oscillator circuit with an external quartz crystal and a few other components (see application drawings). The resultant 262.144kHz signal is amplified and clipped in the input stage. A chain of binary down counters divides the square wave frequency by 256 to supply two complemen-

tary outputs, $\phi 1$ and $\phi 2$ at 1024Hz. These low impedance outputs can drive an external voltage doubler as well as allow an accurate frequency tuning on the oscillator.

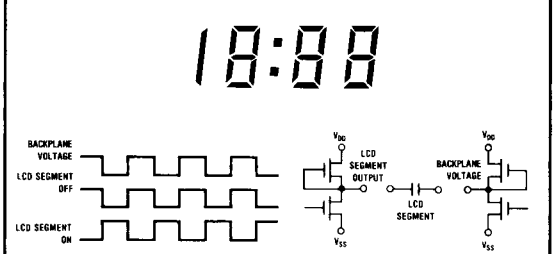
Next a divide by four stage produces a 64Hz signal from which the three strobes Sb1, Sb2, and Sb3 are generated. The strobe generator also contains logic to synchronize the display outputs with the external strobes as well as control the segments for Liquid Crystal Display operation. The 64Hz signal also inputs to a divide by 64-stage to produce a 1 Hz signal which inputs to both the TIME COUNTER and the ELAPSED TIME COUNTER.

The TIME COUNTER contains the binary stages and the decoding logic to generate the BCD code for MINUTES, HOURS and HRS $\times 10$. This data is strobed into the BCD to 7-segment DECODER and loaded into the output buffers in synchronization with the appropriate strobe, Sb1, Sb2 or Sb3.

The ELAPSED TIME COUNTER functions similarly to the TIME COUNTER with the additional decoding of SECONDS and 10's of SECONDS to the display instead of HRS and HRS $\times 10$ during the first 10 minutes after reset.

An internal connection to V_{DD} supply at pin 37 holds the clock in the liquid crystal mode and the outputs are interfaced directly with the LCD as shown in Figure 2.

Figure 2. LCD Output Drive



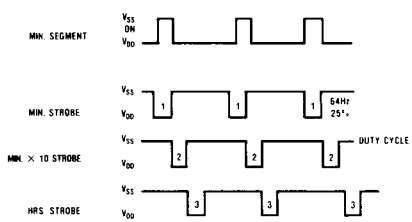
To assure longevity of the LCD display, a 64Hz signal is applied to the individual segments. When the applied segment signal is in-phase with the 64Hz backplane (LCD common terminal) voltage, no visibility occurs. When the applied signal is 180° out of phase with the backplane voltage, visibility occurs. The waveforms shown in Figure 2 represent these conditions.

The backplane voltage is generated by buffering the signal which drives the timing counters. This assures that visibility of the display will not occur through synchronizing problems or rise and fall time differences.

The phase of the segment outputs is generated from the contents of data latches and buffer circuits. This provides an active pull-up or pull-down to both terminals of the segments at all times, thus eliminating the effect of capacitive coupling across the LCD segment. (See Figure 2.)

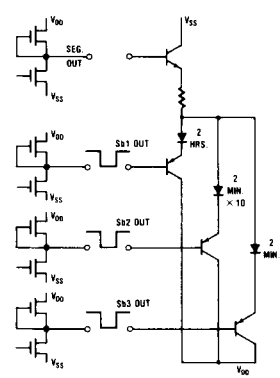
When pin 37 is connected to V_{SS} the multiplexed mode of operation is selected. An ON segment in this mode is driven by a pull-down to V_{SS} which is true during its appropriate strobe time as shown in Figure 3 below.

Figure 3. Strobe Time



A typical LED interface circuit is shown below in Figure 4. In this mode the HRS $\times 10$-digit is a steady state DC output and can be used at any of the 3 strobe times.

Figure 4. MOS/LED Interface



Functional Description of Inputs

V_{SS}	Positive voltage supply return line for circuit.
Y	Oscillator pull-up resistor connection. A 10KΩ resistor to V_{CC} from this pin serves as the 262.144kHz oscillator load.
X	Oscillator input pin. Provides amplification at oscillation frequency of the output from the external crystal and RC network.
CLR	Master Clear. Resets all counters to zero when connected to V_{SS}.
ADV. MIN.	Sets MINUTES with carry to MINUTES ×10 at a one per second rate when connected to V_{SS}.
RST ET	Displays contents of ELAPSED TIME COUNTER when connected to V_{SS}, otherwise time of day displayed.
V_{OD}	Negative power supply input for output buffers only. Allows display to be turned off while internal clock counters continue to operate.
ADV. HRS.	Sets HRS, with carry to HRS ×10, at a one per second rate connected to V_{SS}.
LED/LQ	Mode select pin. When connected to V_{SS} the LED mode is selected. In this mode the three strobe outputs are used to multiplex outputs A3 through F3 to drive MINUTES, MINUTES ×10 and HRS ×10 digits. This occurs at 64Hz 25% duty rate. In this mode outputs A1 through F1 and A2 through F2 remain off at negative supply level, V_{OD}.
V_{DD}	Negative power supply input for internal logic can be connected to V_{OD} for single supply operation.
TEST BYPASS	When connected to V_{SS} time counters advance at 1024 × normal rate. Used for automatic testing of the clock circuitry.

Functional Description of Outputs

$\phi 1$	Voltage doubler and frequency check output. This supplies a 1024Hz square wave signal which swings between the V_{SS} and V_{DD} voltage levels.
$\phi 2$	Same as $\phi 1$ but 180° out of phase.
Sb3	Strobe signal for HRS digit. 64Hz 25% duty cycle with voltage swing from V_{SS} to V_{OD}. Used only in LED mode.
$\overline{CM}$ Sb2	Drives colon in Liquid Crystal mode and serves as MIN ×10 digit strobe in LED mode. Voltage swing V_{SS} to V_{OD}.
CAL OUT	Calendar advance output. This pin has internal pull-down to V_{SS} only for stepping motor interface. An external 30kΩ resistor may be connected to V_{OD} to drive an external latch for AM-PM display.
CM Sb1	Drives display backplane in LIQUID CRYSTAL mode and serves as MINUTES digit strobe in LED mode. Voltage swing V_{SS} to V_{OD}.

Figure 5. 7-Segment Call Out

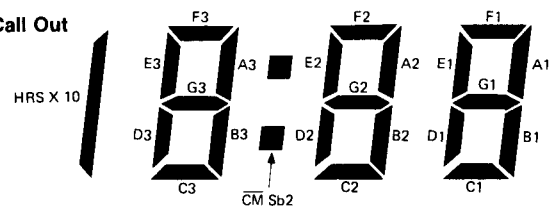
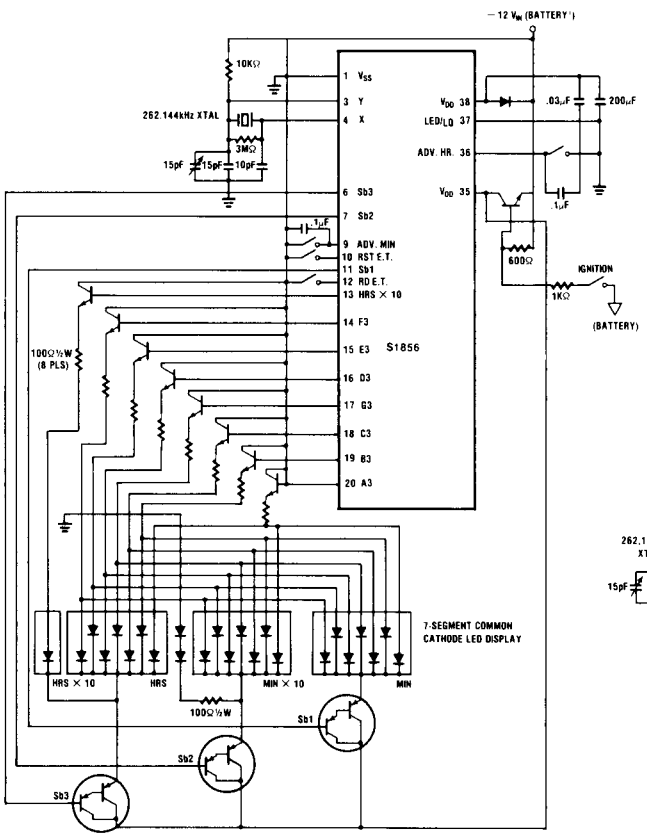
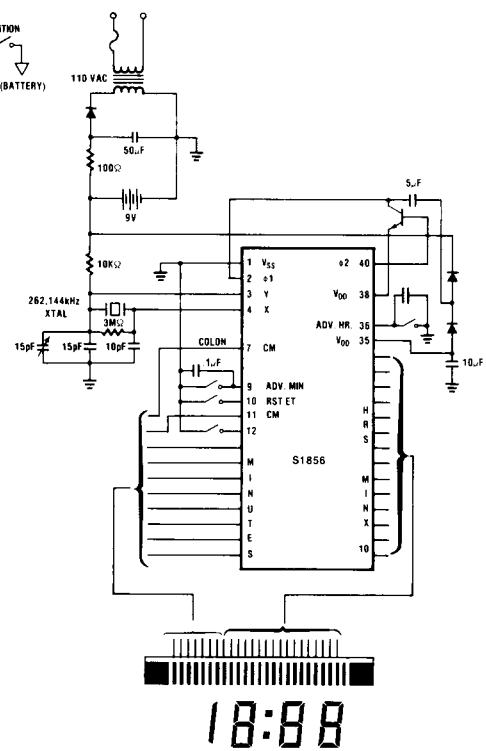


Figure 6. Application Data



AUTOMOBILE CLOCK
WITH LED DISPLAY



HOUSEHOLD CLOCK
WITH AUXILIARY BATTERY