mosaic
semiconductor, inc.

128K x 32 FLASH MODULE

PUMA 68F4001-15/17/20

Issue 4.1 : August 1997

Description

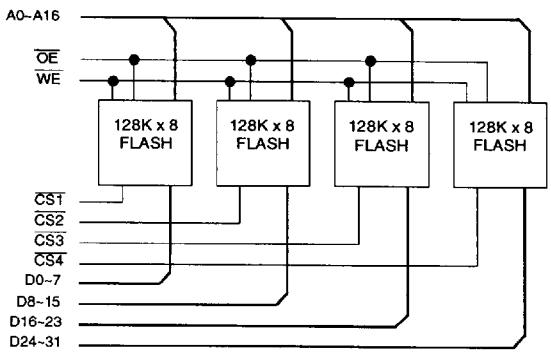
The PUMA 68F4001 is a 4Mbit CMOS FLASH memory module organised as 128K x 32 in a JEDEC 68 pin surface mount PLCC, available with access times of 150, 170 and 200ns. The output width is user configurable as 8 , 16 or 32 bits using four Chip Selects ($\overline{CS1}$~4). The plastic device is screened to ensure high reliability.

Page write (128 Bytes) is performed in 10ms with Toggle bit and $\overline{DATA}$ polling indication of cycle completion. The device features both hardware and software data protection and a low power standby of 6.6mW. Write cycle endurance is 10,000 Erase/Write cycles with a data retention time of 10 years.

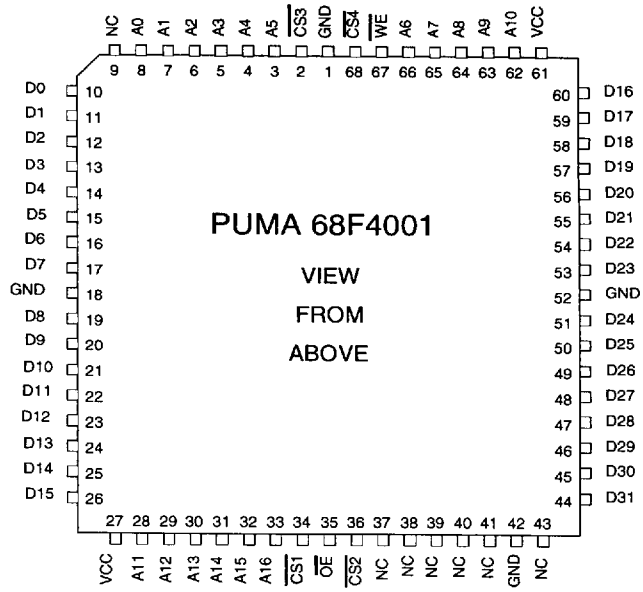
Features

- Access Times of 150,170 and 200ns.
- JEDEC 68 'J' leaded plastic Surface Mount Substrate.
- Industrial, Military or Military(High Rel) Grade.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power : 1320 mW (max)
- Standby Power : -L Part (CMOS) 6.6 mW (max)
- Page Write (128 Bytes) in 10ms typ.
- $\overline{DATA}$ Polling and Toggle bit indication of end of write.
- Hardware and Software Data Protection.
- Endurance of 10^4 Erase/write Cycles and Data Retention Time of 10 years.

Block Diagram



Pin Definition



Pin Functions

A0~16	Address Inputs	**D0~31**	Data Inputs/Outputs
$\overline{CS1}$~4	Chip Select	**OE**	Output Enable
$\overline{WE}$	Write Enable	**NC**	No Connect
V_{cc}	Power (+5V)	**GND**	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Operating Temperature	T_{OPR}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Input voltages (including N.C. pins) with Respect to GND	V_{IN}	-0.5 to +7.0	V
Output voltages with respect to GND	V_{OUT}	-0.5 to +7.0	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
DC Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3	0.8	V	
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3	V
Operating Temp Range	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (**I** Suffix)
	T_{AM}	-55	-	125	°C (**M**, **MB** Suffix)

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current		I_{LI1}	V_{IN} = GND to V_{CC}	-	40	µA
Output Leakage Current	32 bit	I_{LO}	V_{IN} = GND to V_{CC}, $\overline{CS}^{(1)}$=V_{IH}	-	40	µA
Operating Supply Current	32 bit	I_{CC32}	$\overline{CS}^{(1)}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, I_{OUT}=0mA, f=5MHz	-	240	mA
	16 bit	I_{CC16}	As above	-	126	mA
	8 bit	I_{CC8}	As above	-	69	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}^{(1)}$= V_{IH}, $I_{I/O}$= 0mA, Other Inputs = V_{IH}	-	12	mA
	CMOS levels	I_{SB2}	$\overline{CS}^{(1)}$= V_{CC}-0.3V, $I_{I/O}$ = 0mA, Other Inputs = V_{CC}	-	1.2	mA
Output Low Voltage		V_{OL}	I_{OL} = 2.1mA.	-	0.4	V
Output High Voltage		V_{OH}	I_{OH} = -400µA.	2.4	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

Capacitance (T_A=25°C, f=1MHz) Note: These parameters are calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	$\overline{CS1\text{-}4}$	C_{IN1}	V_{IN}=0V	-	16	pF
	Other Inputs	C_{IN2}	V_{IN}=0V	-	34	pF
Output Capacitance		C_{OUT}	V_{OUT}=0V	-	22	pF

AC OPERATING CONDITIONS

Read Cycle

Parameter	Symnbol	-15 min	-15 max	-17 min	-17 max	-20 min	-20 max	Unit	Notes
Read Cycle Time	t_{RC}	150	-	170	-	200	-	ns	
Address Access Time	t_{AA}	-	150	-	170	-	200	ns	
Chip Select Access Time	t_{CS}	-	150	-	170	-	200	ns	
Output Enable Access Time	t_{OE}	0	70	0	80	0	80	ns	
Chip Select High to High Z Output	t_{HZ}	0	50	0	50	0	50	ns	(1)
Output Enable High to High Z Output	t_{OHZ}	0	50	0	55	0	60	ns	(1)
Output Hold from Address Change	t_{OH}	0	-	0	-	0	-	ns	

Notes:(1) t_{HZ} is specified from $\overline{OE}$ or $\overline{CS\ 1\text{-}4}$ whichever occurs first (Cl=5 pf).

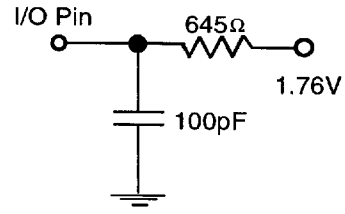
Write Cycle

Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	80	-	-	ns
Output Enable Set-up Time	t_{OES}	0	-	-	ns
Output Enable Hold Time	t_{OEH}	0	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Write Enable High Recovery	t_{WPH}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Delay to Next Write	t_{DW}	10	-	-	µs
Byte Load Cycle	t_{BLC}	-	-	150	µs

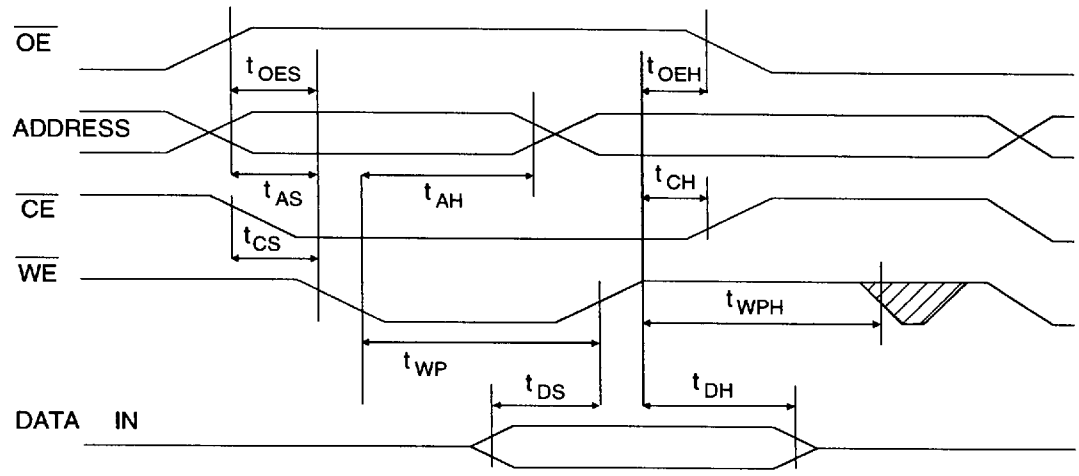
AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 10ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

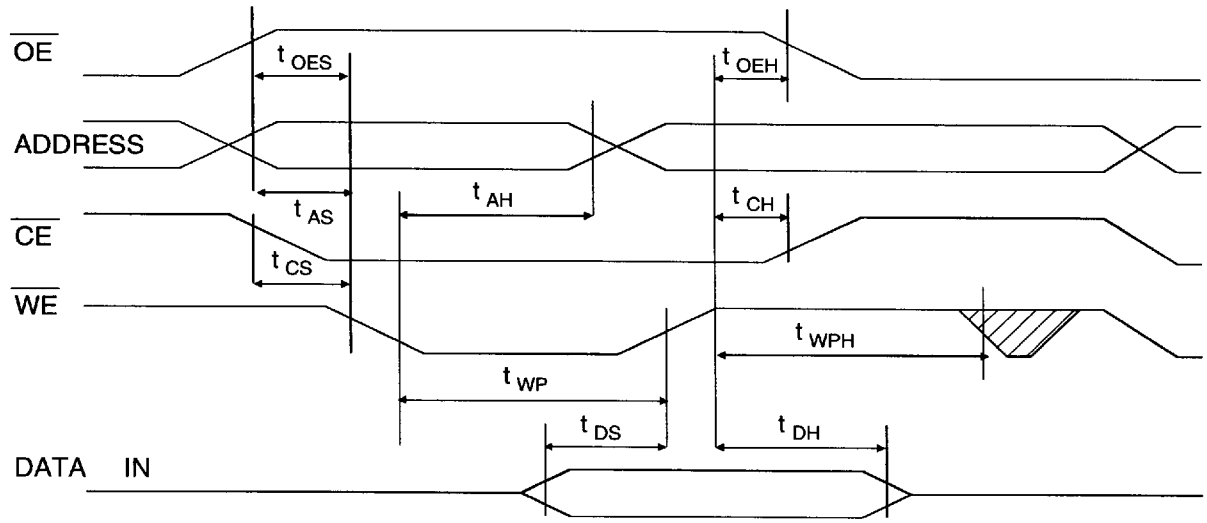
Output Test Load



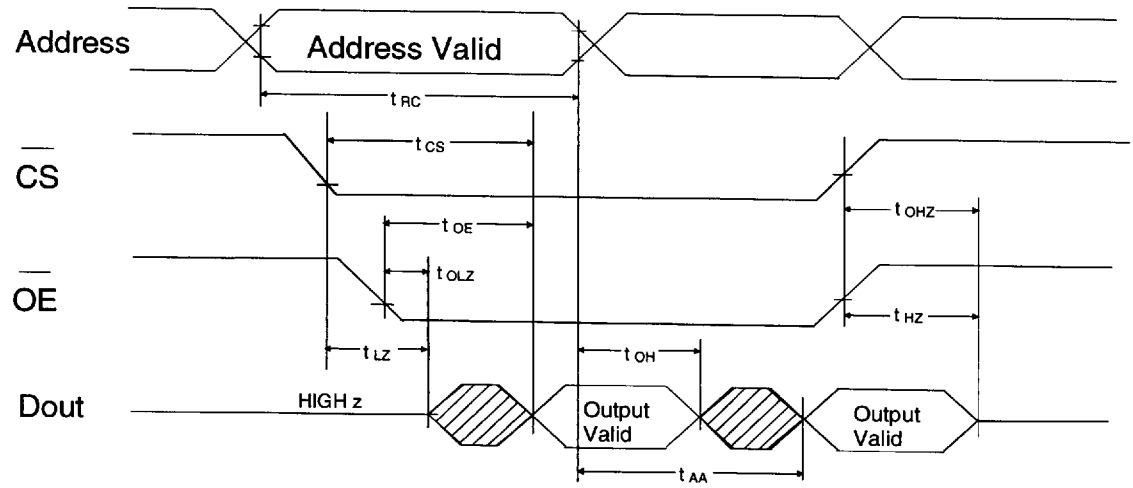
AC Write Waveform - $\overline{WE}$ Controlled



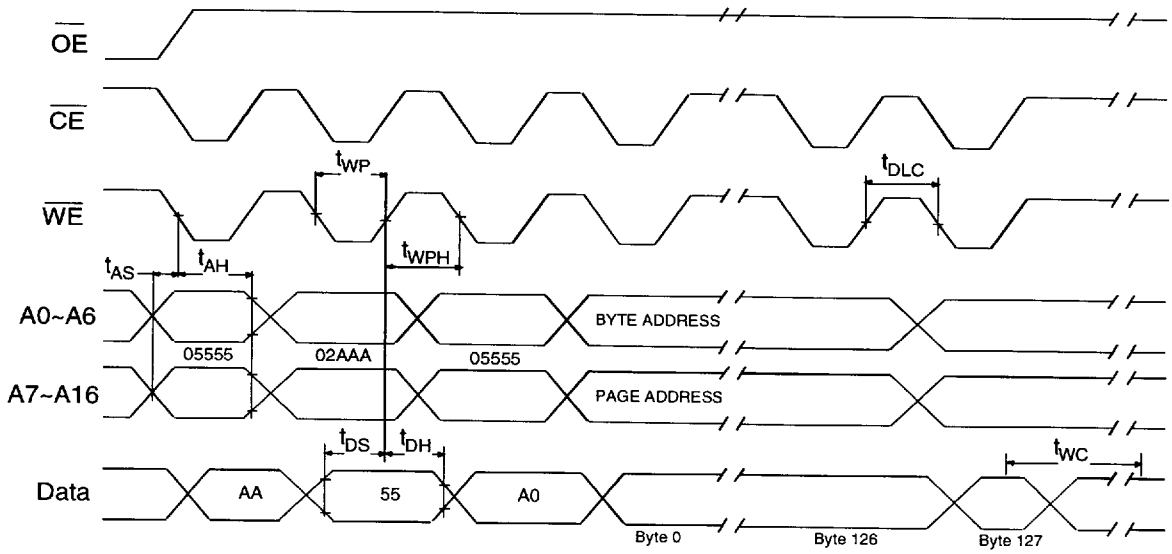
AC Write Waveform - $\overline{CS}$ Controlled



Read Cycle Timing Waveform

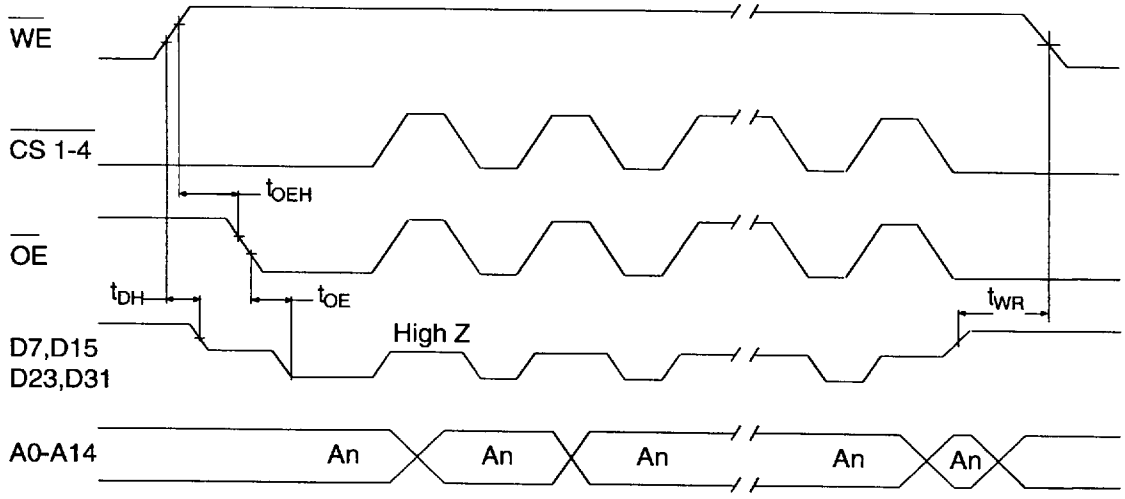


Software Protected Write Waveform

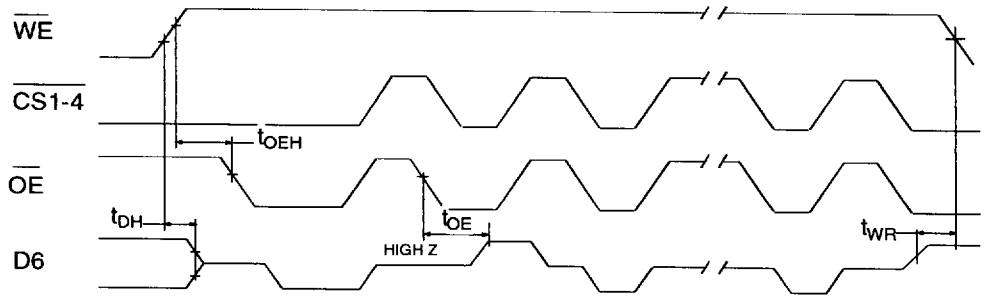


Note: (1) A7 through A16 must specify the page address during each high to low transition of Write Enable (or Chip select).
(2) Output Enable must be high only when Write Enable and Chip Select are both low.
(3) All bytes that are not loaded within the sector being programmed will be erased to FF.

DATA Polling Waveform



Toggle Bit Waveform

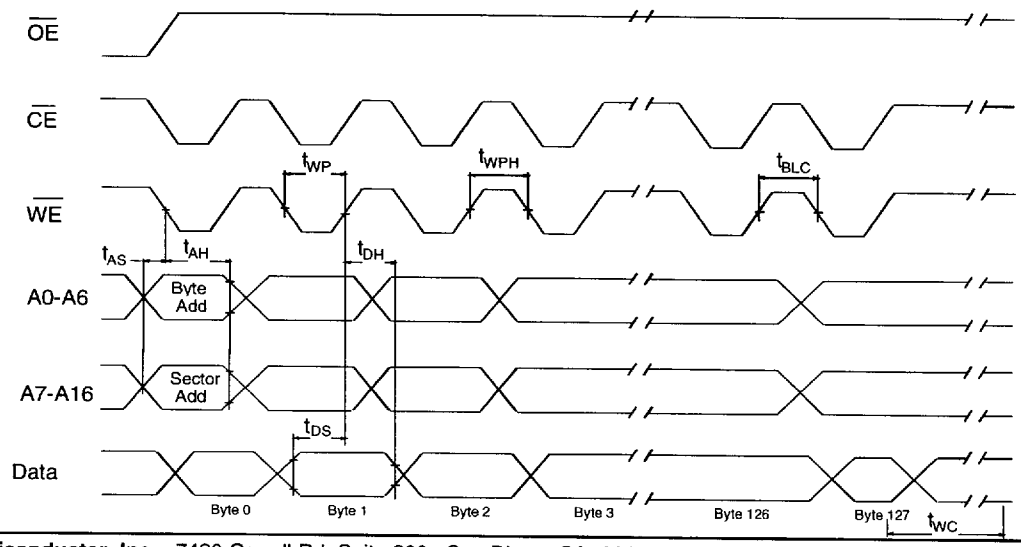


(1) Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.

(2) Beginning and adding state of D7, D15, D23, D31 may vary.

(3) Any address location may be used but the address should not vary.

Page Mode Write Waveform



Device Operation

Read

The PUMA 68F4001 read operations are initiated when Write Enable is high and both Output Enable and Chip Select are LOW. The read operation is terminated by either Chip Select or Output Enable returning HIGH. This 2-line control architecture eliminates bus connection in a system environment. The data bus will be in a high impedance state when either Output Enable or Chip Select is HIGH.

Write

The device is reprogrammed on a sector basis. Byte loads are used to enter the 128 bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be erased to read FFh.

During a reprogram cycle, the address locations and 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling on D7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the high to low transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the sector address. The sector address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

DATA Polling

In order to detect the end of a write cycle, two methods are provided. During a write operation (Byte or Page) an attempt to read the last byte written will result in the compliment of the written data appearing on D7 (or D15, D23 or D31, depending on the device selected). Once the write cycle is completed, true data appears on the outputs and the next write cycle may begin. Using this method of indicating the end of a write can effectively reduce the total write time by 50%.

TOGGLE bit

In addition to DATA polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 (or D14, D22 or D30, depending on the device selected). toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read as normal, allowing the next write cycle to be performed. This can eliminate the software housekeeping chore of saving and fetching the last address and data written in order to implement DATA polling. This can be especially helpful in an array composed of multiple PUMA 68F4001 modules that are frequently updated.

Hardware Data Protection

Both hardware and software protection is provided as described below.

Four types of hardware protection give high security against accidental writes:

- If V_{cc} - 3.8V, Write is inhibited.
- $\overline{OE}$ low, $\overline{CS}$ or $\overline{WE}$ high inhibits inadvertant Write Cycles during power-on and power-off. Write Cycle timing specifications must be observed concurrently.
- Pulses are less than 20ns on $\overline{WE}$ do not initiate a Write Cycle.

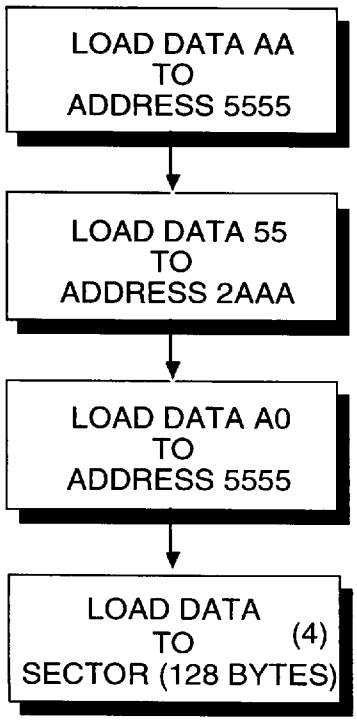
Software controlled data protection, once enabled by the user, means that a software algorithm must be used before any write can be performed. To enable this feature the algorithm opposite is followed, and must be reused for each subsequent write operation. Once set the data protection remains operational until it is disabled by using the second algorithm overleaf: power transitions will not reset this feature.

Software Algorithms

Selecting the software data protection mode requires the host system to precede datawrite operations by a series of three write operations to three specfic addresses. The three byte sequence opens the page write window enabling the host to write 128 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state

Software Data Protection Algorithm (1)

Regardless of whether the device has been protected or not, once the software data protected algorithm is used and the data is written, the PUMA 68F4001 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the PUMA 68F4001 will be write protected during power-down and any subsequent power-up.



WRITES ENABLED (2)

ENTER DATA PROTECT STATE

Notes:

(1) Data Format I/O7-I/O0 (Hex);
Once initiated, this sequence of write operations should not be interrupted.

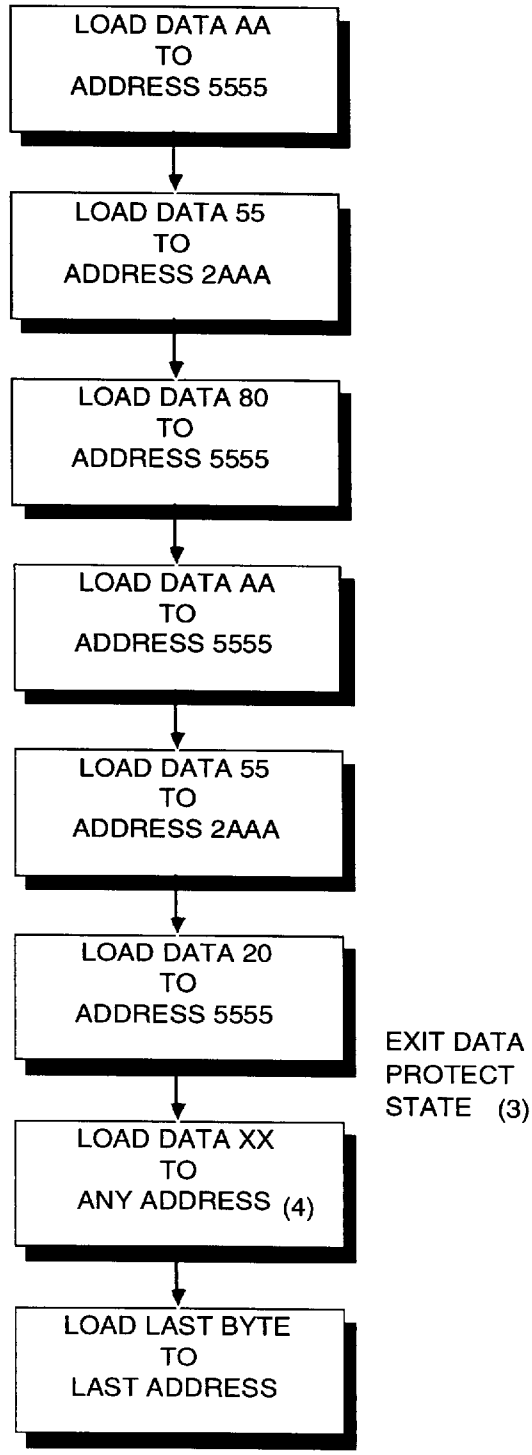
(2) Enable Write Protect state will be initiated at end of write even if no other data is loaded.

(3) Disable Write Protect state will be initiated at end of write period even if no other data is loaded.

(4) 128 bytes of data must be loaded.

Software Data Protect Disable

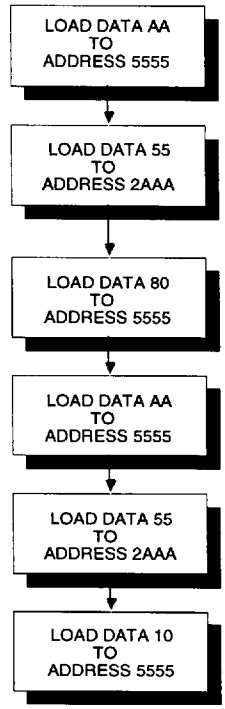
In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer. The following six step algorithm will reset the internal protection circuit. After t_{WC}, the PUMA 68F4001 will be in standard operating mode.



Chip Erase Algorithm

The Puma 68F4001 offers a chip erase function in which the entire device can be erased by a six byte algorithm. Once this code has been entered, the device will set each byte to a high state, (FFh) erasing any stored data. The device will also internally time this operation so that no external clocks are needed.

The Puma 68F4001 can also be completely erased by setting the entire device to a high state. This is accomplished by first placing $\overline{OE}$ at 12 volts with $\overline{CE}$ low and $\overline{WE}$ high: when $\overline{WE}$ is pulsed low for a minimum of 20 ms, the contents of the entire device will be erased.



Notes :

(1) Data format: I/O_7 ~I/O_0 (Hex.)

(2) Data polling may be used to determine the erase cycle by checking any address for data equal to FFh.

(3) After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within t_{WC}.

Operating Modes

The table below shows the logic inputs required to control the operating modes of each device on the PUMA 68F4001.

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUTS
Read	0	0	1	Data Out
Write	0	I	0	Data in
Standby	1	X	X	High Z
Write Inhibit	X	X	1	
Write Inhibit	X	0	X	
Output Disable	X	1	X	High Z
Chip Erase	0	I	0	

$1 = V_{IH}$ $0 = V_{IL}$ X = Don't care

Note : (1) Refer to AC Programming Waveforms

SCREENING

Military Screening Procedure

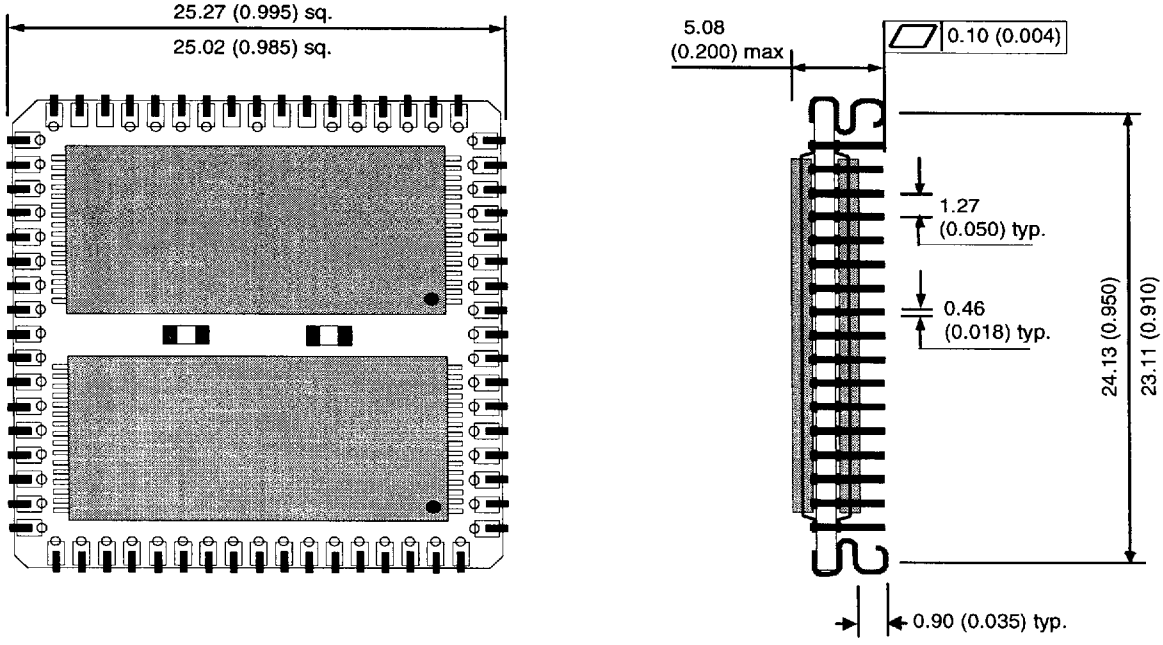
Screening Flow for high reliability product is in accordance with Mil-883 method 5004 .

MB MODULE SCREENING FLOW

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Temperature cycle	1010 Condition B (10 Cycles,-55°C to +125°C)	100%
Burn-In		
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	T_A=+125°C,160hrs minimum.	100%
Final Electrical Tests	Per applicable Device Specification	
Static (DC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (AC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
External Visual	2009 Per vendor or customer specification	100%

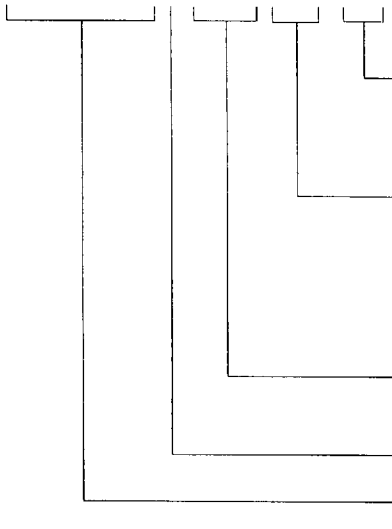
Package Information Dimensions in mm(inches)

Plastic 68 Pin JEDEC Surface mount PLCC



Ordering Information

PUMA 68F4001MB-15



Speed	15	= 150 ns
	17	= 170 ns
	20	= 200 ns
Temp. range/screening	Blank	= Commercial Temperature
	I	= Industrial Temperature
	M	= Military Temperature
	MB	= Screened in accordance with MIL-STD-883
Organisation	4001	= 128K x 32, user configurable as 256K x 16 and 512K x 8
Memory Type	F	= FLASH
Package	PUMA 68	= 68 pin "J" Leaded PLCC