LXT380/4 Octal T1/E1 LIUs — Interfacing with the Transwitch Octal Framers

Application Note

January 2001

Order Number: 249136-001

As of January 15, 2001, this document replaces the Level One document known as *AN120*.

Application Note

Contents

Figures

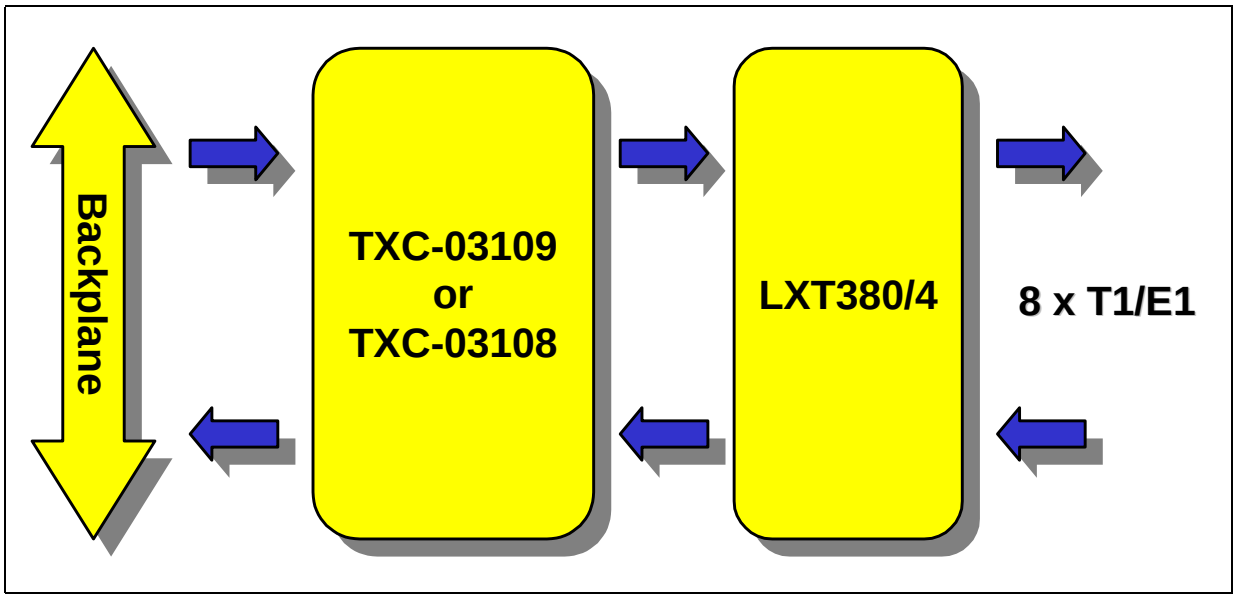
Tables

1.0 General Description

The LXT380/4 series of octal Line Interface Units (LIUs) are the highest density T1/E1 solutions currently available on the market. The LXT380 is an octal E1 (only) LIU with clock and data recovery. The LXT384 is a full featured T1/E1 LIU with crystal-less jitter attenuator.

In many applications, these LIUs will interface with multi-port framers. The Transwitch TXC-03108 octal T1 framer and the TXC-03109 octal E1 framer are a natural choice given their rich feature set and high density packages.

This application note shows that the Transwitch octal T1/E1 framers can easily interface with the LXT380/4 series of LIUs. The following sections provide some guidelines regarding the connection of these devices in a typical T1/E1 application.



2.0 Digital Interface

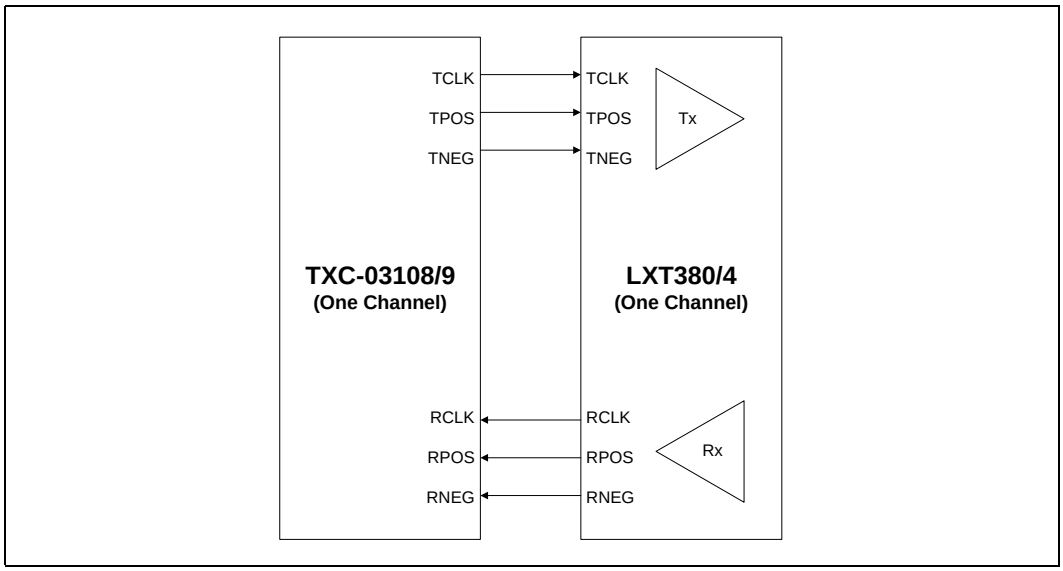
2.1 Unipolar/Bipolar Interface

The LXT380/4 and the TXC-03108/9 interface at the digital level through independent sets of data and clock signals for the receive and transmit paths. This interface can be either unipolar or bipolar. Given the bipolar interface's simplicity, it is recommended for most applications.

2.1.1 Bipolar Interface

In Bipolar mode, the LIU and the framer communicate using three signals in each direction: positive pulse (POS), negative pulse (NEG) and clock (CLK). See Figure 1.

Figure 1. Bipolar Interface



At the receive side, RPOS and RNEG indicate the LIU receiver has detected either a positive or negative pulse. RCLK is the clock extracted from the incoming signal, and is used to latch the RPOS/RNEG data into the framer. Bipolar mode is sometimes called "dual rail mode", or "transparent mode" as the LIU simply reports the reception of negative or positive pulses to the framer. Note that the T1/E1 input signal is a three level signal with 0 V, positive or negative pulses. Therefore, in Bipolar mode the framer must decode the sequence of positive and negative pulses into a data stream of 0's and 1's. As a result, the framer's HDB3 or AMI/B8ZS decoders must be enabled.

At the transmit side, the LIU outputs either positive or negative pulses according to the TPOS/TNEG data. When TPOS is High, a positive pulse is transmitted. When TNEG is High, a negative pulse is transmitted. When both TPOS and TNEG are Low, no pulse is transmitted onto the line. TCLK is used to latch the TPOS/TNEG data into the LIU. Note that since the sequence of positive and negative pulses (encoding) is not determined by the LIU, the HDB3 or B8ZS/AMI encoder must be enabled in the framer. Table 1 summarizes the settings in both the LXT380/4 and the TXC-03108/9 for Bipolar interface mode.

Table 1. Bipolar Interface Settings

LXT380/4	TXC-03109/8
CLKE = High: RPOS/RNEG valid on falling edge of RCLK. TPOS/TNEG valid on falling edge of TCLK.	RXCP = 0: bit 5 in register X+00H. RPOS/RNEG valid on falling edge of RCLK.
	TXCP = 0: bit 3 in register X+05H. TPOS/TNEG valid on falling edge of TCLK.
	RAIL = 1: bit 7 in register X+00H. Sets dual rail interface.[1]
	B8ZS: bit 6 in register X+00H.[2] B8ZS = 1 sets B8ZS codec B8ZS = 0 sets AMI codec

1. Note that Transwitch refers to this interface as being "Unipolar". This is the reverse of Intel's notation.
2. TXC-03108 with LXT384 only.

2.1.2 Unipolar Interface

In Unipolar mode, the LIU and the framer exchange data using only two signals in each direction: one for data (DATA) and another for clock (CLK). See Figure 2. Unipolar mode is sometimes referred to as "single rail" or "NRZ" mode.

At the receive side, RDATA indicates the data content in the receive signal. RCLK is used to latch the RDATA information into the framer. Unipolar mode assumes that the data content of the LIU receive signal has already been decoded into a stream of 1's and 0's. Therefore, the HDB3 or B8ZS/AMI codecs should enabled in the LIU.

At the transmit side, the TNRZ/TCLK outputs from the framer connect directly to the TDATA/TCLK inputs of the LIU. The LIU is responsible for encoding the data stream into HDB3 or B8ZS/AMI line code.

Table 2 summarizes the settings in both the LXT380/4 and the TXC-03108/9 for Unipolar interface mode.

Figure 2. Unipolar Interface

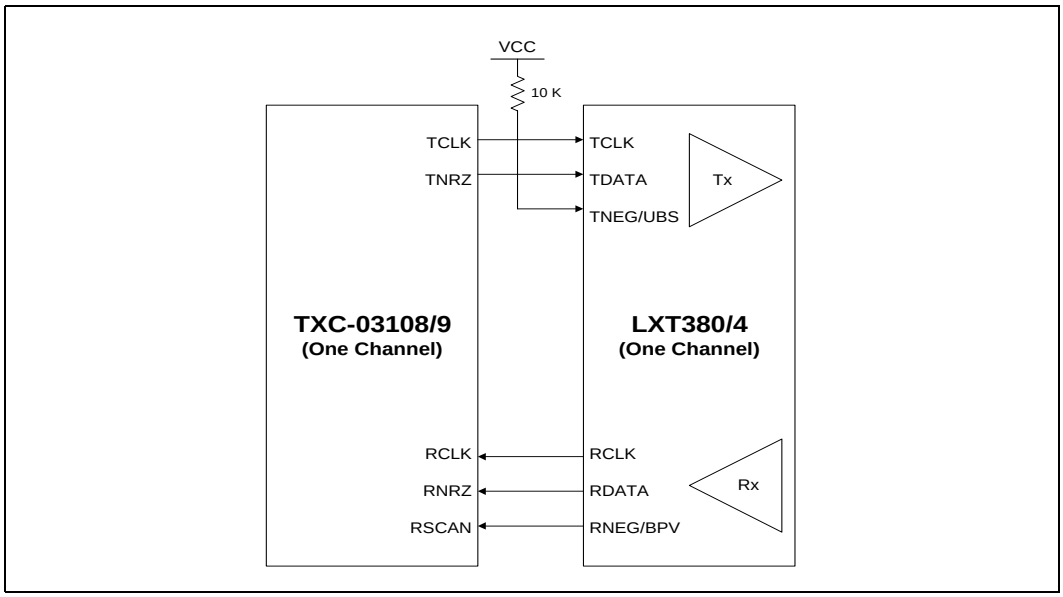


Table 2. Unipolar Interface Settings

LXT380/4	TXC-03109/8
CLKE = High: RDATA valid on falling edge of RCLK. TDATA valid on falling edge of TCLK (Default).	**RXCP = 0**: bit 5 in register X+00H. RNRZ valid on falling edge of RCLK.
TNEG/UBS = High: Sets Unipolar Mode.	**TXCP = 0**: bit 3 in register X+05H. TNRZ valid on falling edge of TCLK.
CODEN pin in Hardware mode [2]: CODEN=High for AMI CODEN=Low for B8ZS **CODEN** bit in Software mode [2], bit 4 in register GCR: CODEN=1 for AMI CODEN=0 for B8ZS Note: In Unipolar mode, the LXT380 enables HDB3 codecs by default.	**RAIL = 0**: bit 7 in register X+00H. Sets single rail interface.[1]

3. Note that Transwitch refers to this interface as a “NRZ interface”.
1. TXC-03108 with LXT384 only.

2.2 Timing Considerations

The timing characteristics of the LXT380/4 and the TXC-03108/9 are compatible. There is sufficient setup and hold time margin at both the receive and transmit interfaces.

2.3 Loss of Signal Detection

2.3.1 Bipolar Mode

Loss Of Signal (LOS) can be detected at either the framer or at the LIU. The TXC-03108/9 LOS detection is based on the content of the RPOS/RNEG outputs. The LOS status is reported in the corresponding Line Status Registers.

Alternatively, the LXT380/4 can be used to detect LOS. In Software mode, the LOS register will indicate a LOS condition in any of the eight channels. In Hardware mode, the individual LOS pins will go High when a LOS condition is detected in the corresponding channel.

2.3.2 Unipolar Mode

In Unipolar mode, the LIU is responsible for LOS detection. In Software mode, LOS status is reported in the LXT380/4 LOS register. LOS status can also be communicated to the framer via the LOS pins.

If the LOS condition is to be reported to the framer, then the LOS output pin for each channel should be connected to the corresponding RSCAN input pin of the TXC-03108/9. In addition, the RXFS bit (address X+1FF) and the EXLOS and ELOSN bits (address X+00) should be set as follows:

- RXFS = 0; RSCAN is not used as frame sync.
- EXLOS = 1; RSCAN is used as external LOS detect.
- ELOSN = 0; RSCAN LOS detect is active High.

With the above configuration, the LOS status will be reflected in the framer Line Status Registers.

2.4 BPV Detection

2.4.1 Bipolar Mode

In Bipolar mode, code violations are detected by the framer and reported in the corresponding Performance Counters.

2.4.2 Unipolar Mode

In Unipolar mode, code violations are detected by the LIU and reported at the RNEG/BPV output pins. If the code violations need to be monitored, the RNEG/BPV pin should be connected to the corresponding RSCAN inputs of the TXC-03108/9. See Figure 2. In addition, the RXFS bit (address X+1FF) and EXLOS bit (address X+00) should be set as follows:

- RXFS = 0; RSCAN is not used as frame sync.
- EXLOS = 0; RSCAN used as code violation detect.

With the above configuration, code violations will be detected by the framer and reported in the corresponding Performance Counters. Note that since the RSCAN inputs are being used for BPV detection, LOS detection can only be done at the LIU level. Therefore, either LOS or BPV can be communicated to the framer, but not both. See “Loss of Signal Detection” on page 9.

2.5 AIS Detection

An Alarm Indication Signal (AIS) can be detected by the framer. The AIS alarm is reported in the corresponding status register.

The LXT384 can also detect AIS in Software mode. This feature is not available in the LXT380.

3.0 Jitter Attenuator

For E1 only applications the TXC-3109 offers a digital jitter attenuator that will remove jitter in the receive path.

For T1 only or T1/E1 applications, the LXT384 offers an advanced CTR12 compliant jitter attenuator that can be placed in either the receive or the transmit path.

4.0 5V I/O Tolerance

Both the TXC-03108/9 and the LXT380/4 are 3.3V devices. When either of them interface with a 5V I/O device (a microprocessor for example), it is crucial to have 5V tolerant inputs.

All these devices can interface directly with 5V ICs. The TXC-03108/9 and the LXT384 accomplish this by offering 5V tolerant inputs. The LXT380 on the other hand, includes separate output ring power pins (VCCIO) that should be connected to the 5V supply when interfacing with 5V devices. Please refer to the LXT380 FAQ, section 4.6 for details.

5.0 Design Guidelines

Here's a list of general design guidelines:

- ***Avoid routing digital signals near analog signals.*** This is especially important near the receiver inputs as the cross- talk may induce bit errors.
- ***Provide ample power and ground planes.*** This practice will reduce emissions and assure signal integrity across the board.
- ***Reduce trace lengths connecting the devices, especially the clock signals.*** Although the T1/E1 clock frequencies are relatively low, the rise and fall times in modern sub-micron CMOS technologies can be extremely fast. The LXT380/4 have controlled slew rate output buffers that help minimize problems associated with fast transitions. However, the rise/fall time from the framers, or other digital devices, may be considerably faster. This can create signal integrity problems when long traces connect the devices. As a rule of thumb, terminate clock signals between devices when the distance exceeds 6 inches.
- ***Use decoupling capacitors near the power supply pins.*** Decoupling capacitors will help reduce switching noise in the power supply. Follow the recommendations in the corresponding datasheets.