

Device Data Library

*WIRELESS RF PRODUCT
DEVICE DATA*

DL110/D
Rev. 14
2/2003



wireless

**For More Information On This Product,
Go to: www.freescale.com**

Contents at a Glance

Wireless RF Product Device Data

Data Sheet Device Index (Alphanumeric)	ix
End of Life Product Index	xii
After Market Support	xiv
Chapter One	
Selector Guide	1–1
Chapter Two	
RF Front End ICs Data Sheets	2–1
Chapter Three	
RF/IF Subsystem ICs Data Sheets	3–1
Chapter Four	
Frequency Synthesis Data Sheets	4–1
Chapter Five	
RF Transistors Data Sheets	5–1
Chapter Six	
RF Amplifier ICs and Modules Data Sheets	6–1
Chapter Seven	
RF CATV Distribution Amplifier Modules Data Sheets	7–1
Chapter Eight	
Tape and Reel Specifications	8–1
Chapter Nine	
Packaging Information	9–1
Chapter Ten	
Applications and Product Literature	10–1



Wireless RF Product Device Data

Table of Contents

	Page		Page
Foreword	v	Chapter Three	
About This Revision	vi	RF/IF Subsystem ICs	
Data Classification	vi	Data Sheets	3-1
On-Line Access to Wireless RF Information ...	vii	Chapter Four	
Data Sheet Device Index (Alphanumeric)	ix	Frequency Synthesis	
End of Life Product Index	xii	Data Sheets	4-1
After Market Support	xiv	Chapter Five	
Chapter One		RF Transistors Data Sheets	5-1
Selector Guide	1-1	Chapter Six	
RF Front End ICs	1-3	RF Amplifier ICs and Modules	
RF/IF Subsystems	1-7	Data Sheets	6-1
Frequency Synthesis	1-11	Chapter Seven	
RF Transistors	1-13	RF CATV Distribution Amplifier	
RF Amplifier ICs and Modules	1-29	Modules Data Sheets	7-1
RF General Purpose Linear Amplifier		Chapter Eight	
Modules	1-33	Tape and Reel Specifications ...	8-1
CATV Distribution Amplifier Modules	1-35	Chapter Nine	
Chapter Two		Packaging Information	9-1
RF Front End ICs		Chapter Ten	
Data Sheets	2-1	Applications and Product	
		Literature	10-1



Wireless RF Product Device Data

FOREWORD

This publication includes technical information for the several product families that comprise the Motorola portfolio of Wireless RF products. The product families include bipolar, RF BiCMOS, SiGe:C BiCMOS, LDMOS, MOSFET RF Power, and gallium arsenide chip technologies in a variety of ceramic and plastic surface mount packages. Discrete components, hybrid modules, and integrated circuits provide different levels of complexity in an effort to provide solutions for our customers' needs.

All devices are in alphanumeric order in the *Data Sheet Device Index* of this book. Just turn to the appropriate page for technical details of the known device. Complete device specifications are provided in the form of *Data Sheets* which are categorized by product type into six chapters for easy reference. A *Selector Guide* by product family is provided at the beginning of the book to enable quick comparisons of performance characteristics and to aid you in identifying devices that meet your

functional performance requirements of frequency, output power, gain, or other parameters.

Chapters on Tape and Reel Options, Packaging Information, Applications and Product Literature include additional information to aid you in the design process.

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274. Please refer to our section on *On-line Access to Wireless Semiconductor Data* so that you will always have easy access to the most current information available on Motorola's Wireless RF product portfolio.

Refer to the *End of Life Product Index* section for information on products that are Not Recommended for New Design, End of Life or available through After Market Support.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

MOTOROLA and the Stylized M Logo are registered in the US Patent and Trademark Office. All other product or service names are the property of their respective owners.

Freescale Semiconductor, Inc.

ABOUT THIS REVISION

This edition of the *Wireless RF Product Device Data Library* encompasses a considerable number of changes that have occurred since our last printing. Some devices have been removed from this book due to package changes or new technology replacements and many new devices have been added.

Application Notes, Engineering Bulletins and Article Reprints of special interest to designers of RF and IF equipment are available on the Motorola Semiconductor Product Sector Web site or are available through the Motorola Literature Distribution Center. Phone and fax numbers for ordering literature are listed on the back cover of this book and in our Accessing Data On-line section. See Chapter Ten for a complete listing of Application Literature.

For information on products that are Not Recommended for New Design, End of Life or available through After Market Support, see the End of Life Product Index section in this data book.

For Cross Reference information on Motorola replacement devices, please consult your local Distributor or Motorola Sales Office.

DATA CLASSIFICATION

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

This heading on a data sheet indicates that the device is in sampling, pre-production, or first production stages. The disclaimer at the bottom of the first page reads: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your local Motorola Semiconductor Sales Office.

ACCESS MOTOROLA SEMICONDUCTOR TECHNICAL INFORMATION**Access Data On-Line! – Use Motorola's SPS Internet Server**

Motorola Semiconductors has provided a World Wide Web Server to deliver Motorola SPS technical data to the global Internet community. Available online are the Product Library, Documentation Library, Tools Library, Industry Focus sites, Design Resource sites, Technical Helpline, Technical Training and Where to Buy at the following URL: <http://www.motorola.com/semiconductors>.

See the RF and IF Design Resource site at <http://www.motorola.com/rf> for specific Wireless RF Product support information for:

- Data sheets
- Applications notes
- Selector guides
- Packaging information
- Application information
- Models
- Reference designs
- Reference design simulations
- Circuit board artwork
- Roadmaps
- Press releases
- Events

RF Reference Designs

RF Power Reference Designs provide:

- RF Performance Tuned for Specific Standard Broadcast Formats
- Low Cost Component Selection
- Complete BOM, Layout, PCB and All Design Information Available
- Integral Temperature Compensated Bias Circuits Included
- Extensive RF Characterizations

Motorola is pleased to offer application-specific reference designs. These application-specific reference designs show some of the many possible uses of our high power RF transistors. They provide the customer's design engineers with a fast and accurate tool to both evaluate the performance envelope and fully characterize the devices under a variety of different operating conditions.

Low-cost component selection was chosen so that the end users could transition the design and its entire Bill of Materials into a high volume base station manufacturing process and still be cost competitive with other competing technologies.

The circuit board is made of a recently developed ceramic loaded thermoset plastic woven glass material that offers very low material costs, low PCB fabrication cost, and yet still has an exceptionally low dissipation factor giving low RF loss. The dielectric constant of this material is high enough to allow for compact, distributed element matching structures, yet of a reasonable value to make it relatively insensitive to fabrication and etching variations.

The circuit's matching and decoupling capacitors utilize a low-cost silicon dioxide dielectric process rather than the traditional porcelain multi-layered assemblies, and they offer low ESRs, very high Q's and tight capacitance value tolerances.

The reference design data sheet contains a wealth of information that customers can use to better understand the range and capabilities of the Motorola devices. Included on the data sheet are such basics as the intended end use application (GSM, W-CDMA, etc.), the typical performance level expected (2% EVM, -40 dBc ACP, etc.) and some device features such as ESD protection and good thermal stability. For more information, go to <http://www.motorola.com/rf> and select Tools/Hardware Tools/Reference Designs and Systems.

RF LDMOS Models

Motorola continues to populate its LDMOS Model Library with the LDMOS MET (Motorola's Electro Thermal) models and with the LDMOS Root models. All product models available in the RF LDMOS Model Library (Root and MET) include package, bond wire and internal matching network effects.

The Motorola Electro Thermal (MET) model for RF LDMOS transistors is a nonlinear model that examines both electrical and thermal phenomena and can account for dynamic self-heating effects of device performance. It is specifically tailored to model high power RF LDMOS transistors used in wireless base station applications.

Implemented in the Agilent® EEsof® EDA Advanced Design System, APLAC® Analog Design Tool, Applied Wave Research Microwave Office™, Ansoft® Serenade Design Environment and Eagleware™ GENESYS™ Microwave and RF Design Suite, the MET LDMOS model is capable of performing small-signal, large-signal, harmonic-balance, noise and transient simulations. Because of its ability to simulate self-heating effects, the MET model is more

Freescale Semiconductor, Inc.

accurate than existing models, enabling circuit designers to predict prototype performance more accurately and reduce design cycle time.

The current release of the MET LDMOS model is available for these tools:

- Agilent EEsof ADS® (UNIX and PC) nonlinear circuit simulator
- APLAC Analog Design Tool
- Applied Wave Research Microwave™ Office
- Ansoft Serenade Design Environment
- Eagleware GENESYS Microwave and RF Design Suite

The LDMOS Model Library is available for all major computer platforms supported by these simulators.

For more information and latest releases supported, go to

<http://www.motorola.com/rf/models>.

RF Power Reference Design Simulations

- Provides a link between Reference Designs and MET models
- Example designs exist for a wide selection of Motorola RF devices
- Demonstrates how to design an amplifier using microwave stripline techniques in the Agilent® ADS® environment
- Provides “real-world” tutorial on how to use nonlinear models
- Example designs for all major applications: GSM, CDMA, W-CDMA, TDMA
- Models provide examples of CW and 2-tone signal simulation
- Simulation files are provided royalty-free to allow for reuse and adaptation
- The device selection and applications are being continually updated
- Provides feedback path from customers to improve usability and accuracy of models

Reference Design Simulations

In the past, Motorola has provided application-specific reference designs that are targeted to provide a pre-designed circuit suitable for a specific application. Additionally, Motorola has also provided modeling tools, specifically MET models, to facilitate design using Computer Aided Engineering (CAE) techniques. These two pieces of the puzzle are excellent design tools; however, they are never linked to each other, leaving the customer to figure out the

best way to blend the two tools to their advantage. Reference Design Simulations are designed to provide the link between these two tools.

Tools Provided

Reference Design Simulations provide an example application of MET models in a pre-designed application circuit. Motorola has taken the time to characterize specific reference design circuits in “software form.” The simulations have been chosen to represent a wide selection of RF devices under many of the major communication standards, including GSM, CDMA, W-CDMA and TDMA.

Learning Tools

Reference Design Simulations provide examples of how to use nonlinear models of RF transistors. Specifically, the user will also learn how to design an amplifier using microwave stripline matching techniques. To provide the most accurate modeling results, each simulation provides examples for CW, 2-tone and modulated signals, as applicable.

Reference Design Simulation Availability

The Reference Design Simulation circuits are available as downloadable Agilent ADS projects from the Motorola SPS web site. These simulation files are provided royalty-free to allow for reuse and adaptation to other application requirements.

Go to <http://www.motorola.com/rf> and select Tools/Software Tools/Reference Design Simulations.

Literature Centers

Printed literature can be obtained from the Literature Centers upon request. For those items that incur a cost, the U.S. Literature Center will accept Master Card and Visa.

USA/EUROPE/Locations Not Listed:

Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
Phone: 1-800-521-6274 or 1-480-768-2130

JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-8573 Japan
Phone: 81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre
2 Dai King Street, Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
Phone: 852-26668334

Freescale Semiconductor, Inc.

DATA SHEET DEVICE INDEX

Device Number	Page Number	Device Number	Page Number
MBC13720	2-3	MHW7185CL	7-28
MBC13900	5-3	MHW7205C	7-30
MBC13916	2-17	MHW7205CL	7-32
MC13190	3-3	MHW7222B	7-34
MC13751	2-27	MHW7242A	7-36
MC13770	2-31	MHW7272A	7-38
MC144110	3-22	MHW7292A	7-39
MC144111	3-22	MHW8182B	7-40
MC145026	3-23	MHW8185	7-42
MC145027	3-23	MHW8185L	7-44
MC145028	3-23	MHW8202B	7-46
MC145151-2	4-3	MHW8205	7-48
MC145152-2	4-3	MHW8205L	7-50
MC145157-2	4-3	MHW8222B	7-52
MC145158-2	4-3	MHW8242A	7-54
MC145170-2	4-4	MHW8272A	7-55
MHL9236	6-3	MHW9146	7-56
MHL9236M	6-3	MHW9182B	7-58
MHL9318	6-6	MHW9186	7-59
MHL9838	6-9	MHW9187	7-61
MHL18336	6-12	MHW9188	7-63
MHL18926	6-13	MHW9189	7-65
MHL19338	6-14	MHW9206	7-67
MHL19926	6-15	MHW9227	7-69
MHL19936	6-16	MHW9236	7-71
MHL21336	6-19	MHW9242A	7-73
MHPA19010	6-22	MHW9247	7-75
MHPA21010	6-25	MHW9267	7-77
MHVIC910HR2	6-28	MHW9276	7-79
MHVIC915R2	6-35	MMG1001R2	7-81
MHW1223LA	7-3	MMG2001R2	7-86
MHW1224LA	7-5	MMM5047	2-36
MHW1244	7-7	MMM5062	2-56
MHW1253LA	7-9	MMM5063	2-75
MHW1254L	7-11	MRF281SR1	5-26
MHW1254LA	7-12	MRF281ZR1	5-26
MHW1303LA	7-14	MRF282SR1	5-30
MHW1304LA	7-16	MRF282ZR1	5-30
MHW1345	6-61	MRF284R1	5-37
MHW1353LA	7-18	MRF284LSR1	5-37
MHW1354LA	7-20	MRF372	5-46
MHW6342T	7-22	MRF373AR1	5-57
MHW7182B	7-24	MRF373ALSR1	5-57
MHW7185C	7-26	MRF374A	5-62

Freescale Semiconductor, Inc.

DATA SHEET DEVICE INDEX — continued

Device Number	Page Number	Device Number	Page Number
MRF1511T1	5-72	MRF9180	5-255
MRF1513T1	5-82	MRF9180S	5-255
MRF1517T1	5-94	MRF18030AR3	5-263
MRF1518T1	5-106	MRF18030ASR3	5-263
MRF1535T1	5-118	MRF18030BR3	5-268
MRF1535FT1	5-118	MRF18030BSR3	5-268
MRF1550T1	5-128	MRF18060A	5-273
MRF1550FT1	5-128	MRF18060AR3	5-273
MRF1570T1	5-137	MRF18060ALSR3	5-273
MRF1570FT1	5-137	MRF18060ASR3	5-273
MRF6522-70	5-151	MRF18060B	5-279
MRF6522-70R3	5-151	MRF18060BR3	5-279
MRF9002R2	5-158	MRF18060BLSR3	5-279
MRF9030R1	5-165	MRF18060BSR3	5-279
MRF9030LSR1	5-165	MRF18085A	5-285
MRF9030MR1	5-172	MRF18085AR3	5-285
MRF9030MBR1	5-172	MRF18085ALSR3	5-285
MRF9045R1	5-180	MRF18085B	5-290
MRF9045LSR1	5-180	MRF18085BR3	5-290
MRF9045MR1	5-186	MRF18085BLSR3	5-290
MRF9045MBR1	5-186	MRF18090A	5-297
MRF9060R1	5-194	MRF18090AS	5-297
MRF9060LSR1	5-194	MRF18090B	5-303
MRF9060MR1	5-202	MRF18090BS	5-303
MRF9060MBR1	5-202	MRF19030R3	5-309
MRF9080	5-210	MRF19030SR3	5-309
MRF9080R3	5-210	MRF19045R3	5-314
MRF9080SR3	5-210	MRF19045SR3	5-314
MRF9080LSR3	5-210	MRF19060	5-321
MRF9085	5-218	MRF19060R3	5-321
MRF9085R3	5-218	MRF19060SR3	5-321
MRF9085SR3	5-218	MRF19085	5-327
MRF9085LSR3	5-218	MRF19085R3	5-327
MRF9100	5-224	MRF19085SR3	5-327
MRF9100R3	5-224	MRF19085LSR3	5-327
MRF9100SR3	5-224	MRF19090	5-335
MRF9120	5-233	MRF19090S	5-335
MRF9120S	5-233	MRF19090SR3	5-335
MRF9130L	5-241	MRF19120	5-341
MRF9130LR3	5-241	MRF19120S	5-341
MRF9130LSR3	5-241	MRF19125	5-348
MRF9135L	5-248	MRF19125S	5-348
MRF9135LR3	5-248	MRF19125SR3	5-348
MRF9135LSR3	5-248	MRF21010R1	5-356

Freescale Semiconductor, Inc. **DATA SHEET DEVICE INDEX — continued**

Device Number	Page Number	Device Number	Page Number
MRF21010LSR1	5-356	MRF21125SR3	5-408
MRF21030R3	5-362	MRF5S21130	5-415
MRF21030SR3	5-362	MRF5S21130R3	5-415
MRF21045R3	5-367	MRF5S21130S	5-415
MRF21045SR3	5-367	MRF5S21130SR3	5-415
MRF21060	5-375	MRF5S21150	5-422
MRF21060R3	5-375	MRF5S21150R3	5-422
MRF21060SR3	5-375	MRF5S21150S	5-422
MRF21085	5-381	MRF5S21150SR3	5-422
MRF21085R3	5-381	MRF5P21180	5-429
MRF21085SR3	5-381	MRF21180	5-436
MRF21085LSR3	5-381	MRF21180S	5-436
MRF5S21090L	5-389	MRFG35003M6T1	5-444
MRF5S21090LR3	5-389	MRFG35010	5-451
MRF5S21090LSR3	5-389	MRFG35010MT1	5-459
MRF21090	5-396	MRFIC0970	2-92
MRF21090S	5-396	MRFIC1870	2-98
MRF21120	5-401	MW4IC915MBR1	6-43
MRF21125	5-408	MW4IC915GMBR1	6-43
MRF21125S	5-408	MWIC930R1	6-53
		MWIC930GR1	6-53

Freescale Semiconductor, Inc.

END OF LIFE PRODUCT INDEX

Motorola SPS follows the industry standard “EIA-724 Product Life Cycle Data Model” to track the life cycle of its product. This model tracks the product’s life cycle from “Product Newly Introduced” to “Product Phase Out.” Products can be phased for a variety of reasons: improved product performance, change in technology roadmap, process obsolescence, market decline, etc. When products are discontinued, a suggested possible replacement device or an alternative source of supply for discontinued devices are made available when possible.

For a list of discontinued devices with possible alternative suppliers, please contact your local Motorola sales office or authorized distributor, or visit the following URL:

<http://www.motorola.com/rf>

Wireless Infrastructure RF Products

Product	Last Order Date	Last Ship Date	Possible Replacement
---------	-----------------	----------------	----------------------

Not Recommended for New Design

MHW1224	—	—	MHW1224LA
MHW1304L	—	—	MHW1304LA

End of Life

CA2810C	Past	Past	MHW6342T
CA2830C	Past	Past	MHW6342T
CA2832C	Past	Past	None
CA901	Past	Past	MHW8182B
CA901A	Past	Past	MHW8182B
CA922	Past	Past	MHW8185
CA922A	Past	Past	MHW8185
MHL8018	Past	Past	None
MHL8115	Past	Past	None
MHL8118	Past	Past	None
MHW1810-001	9/1/03	3/1/04	MW4IC2020MBR1
MHW1910-001	9/1/03	3/1/04	MW4IC2020MBR1
MHW5182A	Past	Past	MHW7182B
MHW5222A	Past	Past	None
MHW6181	Past	Past	MHW7182B
MHW6182	Past	Past	MHW7182B
MHW6272	Past	Past	MHW7272A
MHW7222A	Past	Past	MHW7222B
MHW7292	Past	Past	None
MHW8185LR	Past	Past	None
MHW8185R	Past	Past	None
MHW8205R	Past	Past	None
MHW8292	Past	Past	None
MHW910	Past	6/30/03	MHVIC910HR2
MHW916	Past	6/30/03	None
MRF1507T1	Past	Past	MRF1511T1 or MRF1517T1
MRF182	Past	Past	MRF9030R1
MRF182SR1	Past	Past	MRF9030LSR1
MRF183	Past	Past	MRF9045R1
MRF183S	Past	Past	MRF9045MR1 or MRF9045LSR1

END OF LIFE PRODUCT INDEX — continued

Product	Last Order Date	Last Ship Date	Possible Replacement
End of Life – continued			
MRF183SR1	Past	Past	MRF9045MR1 or MRF9045LSR1
MRF183LSR1	7/31/04	1/31/05	MRF9045MR1 or MRF9045LSR1
MRF184	Past	Past	MRF9060R1
MRF184SR1	Past	Past	MRF9060LSR1 or MRF9060MR1
MRF184R1	7/31/04	1/31/05	MRF9060
MRF184LSR1	7/31/04	1/31/05	MRF9060LSR1 or MRF9060MR1
MRF185	7/31/04	1/31/05	MRF9080
MRF186	7/31/04	1/31/05	MRF9120
MRF187	7/31/04	1/31/05	MRF9085
MRF187S	7/31/04	1/31/05	MRF9085SR3
MRF1946	Past	Past	MRF1535T1
MRF1946A	Past	Past	MRF1535T1
MRF20030R	Past	Past	MRF19030R3
MRF20060R	Past	Past	MRF19060
MRF20060RS	Past	Past	MRF19060
MRF21120S	Past	Past	MRF21120
MRF247	Past	Past	MRF1550T1
MRF2628	Past	Past	None
MRF373	7/31/04	1/31/05	MRF373AR1
MRF373S	Past	Past	MRF373ALSR1
MRF373LSR1	7/31/04	1/31/05	MRF373ALSR1
MRF374	7/31/04	1/31/05	MRF374A
MRF492	Past	Past	MRF1550T1
MRF5015	Past	Past	None
MRF6401	Past	Past	None
MRF6404	Past	Past	MRF9030R1
MRF646	Past	Past	MRF1550T1
MRF648	Past	Past	MRF1550T1
MRF650	Past	Past	MRF1550T1
MRF652	Past	Past	MRF1518T1
MRF6522-060	7/31/04	1/31/05	MRF9060R1
MRF6522-10R1	7/31/04	1/31/05	MRF282SR1
MRF6522-5R1	7/31/04	1/31/05	MRF282ZR1 or MRF9002R2
MRF652S	Past	Past	MRF1518T1
MRF847	Past	Past	MRF9045R1
MRF857S	Past	Past	MRF9002R2
MRF897	Past	Past	MRF9045LSR1
MRF897R	Past	Past	MRF9045R1
MRF898	Past	Past	MRF9060R1
MRF899	Past	Past	MRF9180
TPV8100B	Past	Past	None

For information on Wireless RF and IF handset products, see After Market Support at the following URL:

<http://www.motorola.com/rf>

Freescal Semiconductor, Inc.

AFTER MARKET SUPPORT

For a list of discontinued devices with possible alternative suppliers, please contact your local Motorola sales office or authorized distributor, or visit the following URL:

<http://www.motorola.com/rf>

For Wireless Infrastructure products transferred to another manufacturer, see the list of Wireless Infrastructure RF products below. After market support on these parts is available through M/A–COM. For additional information, contact M/A–COM Customer Service at (310) 320–6160 x 354 (voice), clarkj@tycoelectronics.com (email) or (310) 618–9191 (FAX).

2N6439	MRF137	MRF171A	MRF317
MRF10005	MRF140	MRF173	MRF321
MRF1000MB	MRF141	MRF173CQ	MRF323
MRF10031	MRF141G	MRF174	MRF327
MRF1004MB	MRF148A	MRF175GU	MRF392
MRF10120	MRF150	MRF175GV	MRF393
MRF10150	MRF151	MRF175LU	MRF421
MRF10350	MRF151G	MRF176GU	MRF422
MRF10502	MRF154	MRF176GV	MRF426
MRF1090MA	MRF157	MRF177	MRF428
MRF1090MB	MRF158	MRF275G	MRF429
MRF1150MA	MRF160	MRF275L	MRF448
MRF1150MB	MRF16006	MRF3104	MRF454
MRF134	MRF16030	MRF313	MRF455
MRF136	MRF166C	MRF314	MRF587
MRF136Y	MRF166W	MRF316	

Chapter One

Wireless RF Product Selector Guide

Offering a broad portfolio of RF products, Motorola serves both the wireless infrastructure and subscriber markets. Motorola RF Solutions is the leader in RF technology—today AND tomorrow—and is the answer for developers who are creating innovative new products to meet their customers' need for wireless connections. Motorola pioneered RF technology and continues to drive future innovations, delivering significantly higher measurable performance over our competitors—in most cases, 15 to 30 percent. Motorola RF Solutions supports developers through unequaled integration, high terminal impedance, the most comprehensive RF toolkit in the industry, and access to our global support team. Motorola is committed to the development of new products and expansion of our product offerings to meet the increasing global demands of ISM band and personal communications systems, including cellular phone, broadband data, TV broadcast, land mobile and CATV systems.

How to Use This Selector Guide

The RF Monolithic Integrated Circuits and the RF/IF Integrated Circuits products in this guide are divided into three major functional categories: RF Front End ICs, RF/IF Subsystem ICs and Frequency Synthesis. Each of these categories is further subdivided based on circuit functionality. This structure differentiates highly integrated subsystem ICs from fundamental circuit building blocks and discrete transistors.

The Power LDMOS Transistors, Power GaAs Transistors, Power Amplifier ICs and Modules and CATV Distribution Amplifier Modules are FIRST divided into major categories by frequency band. SECOND, within each category, parts are listed by power level. THIRD, within a frequency band, transistors are further grouped by operating voltage and, finally, output power.

Applications Assistance

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274.

Access Data On-Line!

Use the Motorola SPS Internet to access Motorola Semiconductor Product data at <http://www.motorola.com/semiconductors> or <http://www.motorola.com/rf>. The SPS Internet provides you with instant access to product summary pages, data sheets, selector guide information, application information, design tools, package outlines, on-line technical support and much more.

Table of Contents

	Page
RF Front End ICs	1-3
RFICs	1-4
Upconverters/Exciters	1-4
Downconverters	1-4
Power Amplifiers	1-4
RF Building Blocks	1-5
Amplifiers	1-5
Packages	1-6
RF/IF Subsystems	1-7
Tranceivers	1-8
Miscellaneous Functions	1-8
ADCs/DACs	1-8
Encoders/Decoders	1-8
Packages	1-9
Frequency Synthesis	1-11
Single PLL Synthesizers	1-12
Packages	1-12
RF Transistors	1-13
RF High Power LDMOS Transistors	1-14
Mobile – To 520 MHz	1-14
TV Broadcast – To 1.0 GHz	1-14
Cellular – To 1.0 GHz	1-15
PCS and 3G – To 2.1 GHz	1-16
RF Power GaAs Transistors	1-19
3.5 GHz – Linear Transistors	1-19
RF Low Power Transistors	1-20
RF High Power Amplifier Line-ups	1-21
Packages	1-27
RF Amplifier ICs and Modules	1-29
Base Stations	1-30
Packages	1-32
RF General Purpose Linear Amplifier Modules	1-33
RF General Purpose Linear Amplifier Modules	1-34
Packages	1-34
CATV Distribution Amplifier Modules	1-35
Forward Amplifier Modules	1-36
Reverse Amplifier Modules	1-39
Packages	1-41

RF Front End ICs

Motorola's RF Front End integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SOT-343, SOT-363, TSSOP-16, TSSOP-20EP, QFN-20, QFN-24, or QFN-32 packages.

Evaluation Boards

Evaluation boards are available for RF Front End Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

Table of Contents

	Page
RF Front End ICs	1-3
RFICs	1-4
Upconverters/Exciters	1-4
Downconverters	1-4
Power Amplifiers	1-4
RF Building Blocks	1-5
Amplifiers	1-5
Packages	1-6

RF Front End ICs

RFICs

Upconverters/Exciters

Product	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Conv. Gain dB (Typ)	Output IP3 dBm (Typ)	Packaging	System Applicability
MC13751FC ^(18b)	800 to 900 1900 to 1950	2.7 to 2.9	53	0.025	21.5 23	24	1307/ QFN-24	TDMA, PCS

Downconverters

Product	Input Freq. MHz	LO Freq. Vdc	IF Freq. (MHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply Current	Packaging	System Applicability
MC13770 ^(42,46a) (LNA)	2100 to 2170	n/a	n/a	15 -5.0	1.5 5.0	0 20	3.0 mA 10 μ A	1345/ QFN-12	W-CDMA, PCS, PDC
MC13770 ^(43,46a) (Mixer)	2110 to 2170	2300 to 2360 2490 to 2550	190 380	10.0	8.0	-3.0	5.0 mA	1345/ QFN-12	W-CDMA, PCS, PDC

Power Amplifiers

Product	Freq. Range MHz	Supply Volt. Range Vdc	Saturated P _{out} dBm (Typ)	PAE % (Typ)	Gain P _{out} /P _{in} dB (Typ)	Packaging	System Applicability
MRFIC0970 ^(18b)	800 to 1000	2.8 to 5.5	35.2	53	30.2	1308/ QFN-20	GSM, ISM
MRFIC1870 ^(18b)	1700 to 2000	2.8 to 5.5	33	45	28	1308/ QFN-20	DCS1800, PCS
MMM5047 ^(46a)	824 to 849	3.0 to 4.5	28 30 32	27.9 37.1 44.8	31.3 30.8 31.1	1440/ 9x12 mm Module	AMPS, TDMA, GSM850
	1850 to 1910		30 32	32.3 39.9	31.6 31.5		TDMA, PCS1900
MMM5062 ^(18m)	800 to 1000 1700 to 2000	2.7 to 5.5	33.4 34.0	54 43	36.2 31.0	1383/ 7x7 mm Module	GSM850, GSM900, DCS1800, PCS1900
MMM5063★	800 to 2000	2.7 to 5.5	34.0 35.2 33.8	44 43 53	— — —	1383/ 7x7 mm Module	GSM900, DCS1800, PCS1900

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units;

f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽⁴²⁾In LNA section, specifications are represented in High Gain Mode first and Bypass Mode second.

⁽⁴³⁾In Mixer section, LO frequency ranges are specified for 190 MHz and 380 MHz IF.

⁽⁴⁶⁾To be introduced: a) 1Q03

★New Product

Freescale Semiconductor, Inc.

RF Building Blocks

Amplifiers

Product	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μ A (Typ)	Small Signal Gain dB (Typ)	Output IP3 dBm (Typ)	NF dB (Typ)	Packaging	System Applicability
MBC13720 ^(18c)	400 to 2500	2.5 to 3.0	9.0	<20	14.5 @ 1900 MHz	24.5 @ 1900 MHz	1.38 @ 1900 MHz	419B/ SOT-363	ISM900, 2400, PCS, CDMA
MBC13916 ^(18c)	100 to 2500	2.7 to 5.0	4.7	–	19 @ 900 MHz	16.5 @ 900 MHz	0.9 @ 900 MHz	SOT-343R	General Purpose Cascode Amp for VCOs, Buffers, & LNAs

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

Freescale Semiconductor, Inc. **RF Front End Integrated Circuit Packages**



CASE 419B
(SOT-363)



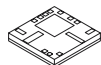
CASE 1307
(QFN-24)



CASE 1308
(QFN-20)



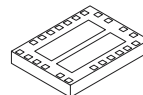
CASE 1345
(QFN-12)



CASE 1383
(7x7 Module)



CASE 1404
(SOT-343R)



CASE 1440
(9x12 Module)

SCALE 1:1

RF/IF Subsystems

Table of Contents

	Page
Tranceivers	1-8
Miscellaneous Functions	1-8
ADCs/DACs	1-8
Encoders/Decoders	1-8
Packages	1-9

RF/IF Subsystems

Tranceivers

Product	V _{CC}	I _{CC}	Max Input Freq.	Sensitivity	PLLS	Baseband BW	System Applicability	Packaging
MC13190FC ^(18b)	2.5–3.0 V	12 mA Rx 64 mA Tx 78 mA SB	2.5 GHz	–68 dBm @ 15 dBm S/N	1	5 MHz	2.4 GHz ISM	1311/ QFN–32

Miscellaneous Functions

ADCs/DACs

Product	Function	I/O Format	Resolution	Number of Analog Channels	Other Features	Suffix/ Packaging
MC144110 ^(25b)	DAC	Serial	6 Bits	6	Emitter–Follower Outputs	DW/751D
MC144111 ^(25b)				4		DW/751G

Encoders/Decoders

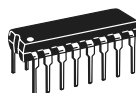
Product	Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Suffix/ Packaging
MC145026 ^(25b)	Encoder	Depends on Decoder	Depends on Decoder	Depends on Decoder	Simplex	P/648, D/751B
MC145027 ^(25b)	Decoder	5	243	4	Simplex	P/648, DW/751G
MC145028 ^(25b)		9	19,683	0	Simplex	

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽²⁵⁾Device available only from Lansdale Semiconductor **after**: a) 3Q03; b) 3Q04.

Freescale Semiconductor, Inc.

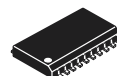
RF/IF Subsystems Packages



CASE 648
P SUFFIX
(DIP-16)



CASE 751B
D SUFFIX
(SO-16)



CASE 751D
DW SUFFIX
(SO-20L)



CASE 751G
DW SUFFIX
(SO-16W)



CASE 1311
(QFN-32)

Frequency Synthesis

Table of Contents

	Page
Single PLL Synthesizers	1-12
Packages	1-12

Freescale Semiconductor, Inc.

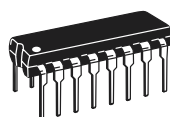
Frequency Synthesis

Single PLL Synthesizers

Product	Maximum Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Features	Packaging
MC145151-2 ^(25b)	20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface	DW/751F
MC145152-2 ^(25b)	20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface, Uses External Dual-Modulus Prescaler	DW/751F
MC145157-2 ^(25a)	20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface	DW/751G
MC145158-2 ^(25a)	20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface, Uses External Dual-Modulus Prescaler	DW/751G
MC145170-2	100 @ 3.0 V 185 @ 4.5 V	2.7 to 5.5	2 @ 3 V 6 @ 5 V	Serial Interface, Auxiliary Reference Divider, Evaluation Kit – MC145170EVK	P/648, D/751B, DT/948C

⁽²⁵⁾Device available only from Lansdale Semiconductor after: a) 3Q03; b) 3Q04.

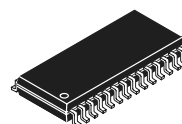
Frequency Synthesis Packages



CASE 648
P SUFFIX
(DIP-16)



CASE 751B
D SUFFIX
(SO-16)



CASE 751F
DW SUFFIX
(SO-28L)



CASE 751G
DW SUFFIX
(SO-16W)



CASE 948C
DT SUFFIX
(TSSOP-16)

Motorola RF Transistors

Motorola continues to be the industry leader in RF transistor technology. Our current portfolio ranges from high gain and low noise devices at microwave frequencies to high power devices for fixed RF and microwave applications. Technical innovation combined with world-class manufacturing capability allows Motorola to offer world class product, service and support to its customers.

From our LDMOS and GaAs portfolio, the user can choose from a variety of packages. They include plastic and ceramic that are microstrip circuit compatible or surface mountable. Many are designed for automated assembly equipment.

Table of Contents

	Page
RF High Power LDMOS Transistors	1-14
Mobile – To 520 MHz	1-14
TV Broadcast – To 1.0 GHz	1-14
Cellular – To 1.0 GHz	1-15
PCS and 3G – To 2.1 GHz	1-16
RF Power GaAs Transistors	1-19
3.5 GHz Linear Transistors	1-19
RF Low Power Transistors	1-20
RF High Power Amplifier Line-ups	1-21
Packages	1-27

Motorola RF Transistors

RF High Power LDMOS Transistors

Motorola LDMOS technology is ideally suited for RF power amplifier applications. Several families of products have been targeted for specific markets including VHF and UHF portable/land mobile, 900 MHz linear cellular, GSM, TDMA and CDMA, digital television, GSM EDGE, PCS, UMTS, and W-CDMA.

With the unique LDMOS characteristics, these parts offer superior thermal performance. This is due to the simplified package design, which offers excellent Class AB intermodulation performance under medium peak-to-average ratios providing a superior device choice for advanced digital modulations formats or high gain applications.

Table 1. Mobile – To 520 MHz

Designed for broadband VHF and UHF commercial and industrial applications. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 12.5/7.5 volt mobile, portable and base station operation.

Product	Frequency Band ⁽³⁷⁾	P _{out} Watts	Test Signal	V _{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ _{JC} °C/W	Pkg/Style
---------	--------------------------------	------------------------	-------------	-----------------------	-------------------------	----------------	----------------------	-----------

VHF & UHF, Land Mobile Radio, Class AB

MRF1513T1 ^(18f)	U	400–520	3 CW	1–Tone	7.5/12.5	11/520	55	4.0	466/1
MRF1511T1 ^(18f)	U	135–175	8 CW	1–Tone	7.5	11.5/175	55	2.0	466/1
MRF1517T1 ^(18f)	U	430–520	8 CW	1–Tone	7.5	11/520	55	2.0	466/1
MRF1518T1 ^(18f)	U	400–520	8 CW	1–Tone	12.5	11/520	55	2.0	466/1
MRF1535T1 ^(18j)	U	400–520	35 CW	1–Tone	12.5	10(Min)/520	50(Min)	0.90	1264/1
MRF1535FT1 ^(18j)	U	400–520	35 CW	1–Tone	12.5	10(Min)/520	50(Min)	0.90	1264A/1
MRF1550T1 ^(18j)	U	135–175	50 CW	1–Tone	12.5	10(Min)/175	50(Min)	0.75	1264/1
MRF1550FT1 ^(18j)	U	135–175	50 CW	1–Tone	12.5	10(Min)/175	50(Min)	0.75	1264A/1
MRF1570T1 ^{(18j)★}	U	400–470	70 CW	1–Tone	12.5	10(Min)/470	50(Min)	0.75	1366/1
MRF1570FT1 ^{(18j)★}	U	400–470	70 CW	1–Tone	12.5	10(Min)/470	50(Min)	0.75	1366A/1

Table 2. TV Broadcast – To 1.0 GHz

Product	Frequency Band ⁽³⁷⁾	P _{out} Watts	Test Signal	V _{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ _{JC} °C/W	Pkg/Style
---------	--------------------------------	------------------------	-------------	-----------------------	-------------------------	----------------	----------------------	-----------

470 – 1000 MHz, Class AB

MRF373AR1 ^(18a)	U	470–860	75 CW	1–Tone	32	18.2/860	60	0.89	360B/1
MRF373ALSR1 ^(18a)	U	470–860	75 CW	1–Tone	32	18.2/860	60	0.63	360C/1
MRF374A	U	470–860	130 PEP	2–Tone	32	17.3/860	41.2	0.58	375F/1
MRF372	I	470–860	180 PEP	2–Tone	32	17/860	36	0.5	375G/1
MRF377 ^(46b)	I/O	470–860	50 AVG	OFDM	32	17/860	24	0.37	375G/1

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units;

f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽³⁷⁾U = Unmatched; I = Input; I/O = Input/Output.

⁽⁴⁶⁾To be introduced: a) 1Q03; b) 2Q03; c) 3Q03

★New Product

RF High Power LDMOS Transistors (continued)

Table 3. Cellular – To 1.0 GHz

Product	Frequency Band ⁽³⁷⁾	P _{out} (Typ) Watts	Test Signal	V _{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ _{JC} °C/W	Pkg/ Style
800 – 1.0 GHz, Class AB								
MRF9002R2 ^(18e)	U	960	(3x) 2 PEP ⁽⁴¹⁾	26	18/960	50	12	978/–
MRF9030MBR1 ^{(18a)★}	U	945	30 PEP	26	20/945	41	1.08	1337/1
MRF9030MR1 ^(18a)	U	945	30 PEP	26	20/945	41	1.08	1265/1
MRF9030R1 ^(18a)	U	945	30 PEP	26	19/945	41.5	1.9	360B/1
MRF9030LSR1 ^{(18a)★}	U	945	30 PEP	26	19/945	41.5	1.5	360C/1
MRF9045MBR1 ^(18a)	U	945	45 PEP	28	19/945	41	0.85	1337/1
MRF9045MR1 ^(18a)	U	945	45 PEP	28	19/945	41	0.85	1265/1
MRF9045R1 ^(18a)	U	945	45 PEP	28	18.8/945	42	1.4	360B/1
MRF9045LSR1 ^(18a)	U	945	45 PEP	28	18.8/945	42	1.0	360C/1
MRF9060MBR1 ^(18a)	U	945	60 PEP	26	18/945	40	0.56	1337/1
MRF9060MR1 ^{(18a)★}	U	945	60 PEP	26	18/945	40	0.56	1265/1
MRF9060R1 ^(18a)	U	945	60 PEP	26	17/945	40	1.1	360B/1
MRF9060LSR1 ^(18a)	U	945	60 PEP	26	17/945	40	0.8	360C/1
MRF6522–70	I	921–960	70 CW	26	16/921,960	58	1.1	465D/1
MRF6522–70R3 ⁽¹⁸ⁱ⁾	I	921–960	70 CW	26	16/921,960	58	1.1	465D/1
MRF9080	I	921–960	70 CW	26	18.5/921,960	52	0.7	465/1
MRF9080R3 ⁽¹⁸ⁱ⁾	I	921–960	70 CW	26	18.5/921,960	52	0.7	465/1
MRF9080SR3 ⁽¹⁸ⁱ⁾	I	921–960	70 CW	26	18.5/921,960	52	0.7	465A/1
MRF9080LSR3 ^{(18i)★}	I	921–960	70 CW	26	18.5/921,960	52	0.7	465A/1
MRF9085	I	880	90 PEP	26	17.9/880	40	0.7	465/1
MRF9085R3 ⁽¹⁸ⁱ⁾	I	880	90 PEP	26	17.9/880	40	0.7	465/1
MRF9085SR3 ⁽¹⁸ⁱ⁾	I	880	90 PEP	26	17.9/880	40	0.7	465A/1
MRF9085LSR3 ⁽¹⁸ⁱ⁾	I	880	90 PEP	26	17.9/880	40	0.7	465A/1
MRF9100★	I/O	921–960	100 CW	26	17/960	51	1.0	465/1
MRF9100R3 ^{(18i)★}	I/O	921–960	100 CW	26	17/960	51	1.0	465/1
MRF9100SR3 ^{(18i)★}	I/O	921–960	100 CW	26	17/960	51	1.0	465A/1
MRF9120	I	880	120 PEP	26	16.5/880	39	0.45	375B/1
MRF9120S	I	880	120 PEP	26	16.5/880	39	0.45	375H/1
MRF9130L★	I	921–960	130 CW	28	16.5/921,960	48	0.6	465/1
MRF9130LR3 ^{(18i)★}	I	921–960	130 CW	28	16.5/921,960	48	0.6	465/1
MRF9130LSR3 ^{(18i)★}	I	921–960	130 CW	28	16.5/921,960	48	0.6	465A/1
MRF9135L★	I	880	25 AVG	26	17.8/880	25	0.6	465/1
MRF9135LR3 ^{(18i)★}	I	880	25 AVG	26	17.8/880	25	0.6	465/1
MRF9135LSR3 ^{(18i)★}	I	880	25 AVG	26	17.8/880	25	0.6	465A/1
MRF9180	I	880	170 PEP	26	17.5/880	39	0.45	375D/1
MRF9180S	I	880	170 PEP	26	17.5/880	39	0.45	375E/1
MRF9200L ^(46b)	I/O	880	45 AVG	26	17/880	26	0.37	465B/1
MRF9200LS ^(46b)	I/O	880	45 AVG	26	17/880	26	0.37	465C/1
MRF9200LSR3 ^(18i,46b)	I/O	880	45 AVG	26	17/880	26	0.37	465C/1
MRF9210 ^(46b)	I/O	880	40 AVG	26	16.5/880	25.5	0.4	375G/1

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units;

f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽³⁷⁾U = Unmatched; I = Input; I/O = Input/Output.

⁽⁴¹⁾Three individual transistors in a single package.

⁽⁴⁶⁾To be introduced: a) 1Q03; b) 2Q03; c) 3Q03

★New Product

RF High Power LDMOS Transistors (continued)

Table 4. PCS and 3G – To 2.1 GHz

Product	Frequency Band ⁽³⁷⁾		P _{out} (Typ) Watts	Test Signal	V _{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ _{JC} °C/W	Pkg/ Style
1805 – 1990 MHz, Class AB (GSM1800, GSM1900, GSM EDGE and PCS TDMA)									
MRF18030AR3 ⁽¹⁸ⁱ⁾	I/O	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465E/1
MRF18030ASR3 ⁽¹⁸ⁱ⁾	I/O	1805–1880	30 CW	1–Tone	26	14/1805,1880	50	2.1	465F/1
MRF18030BR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465E/1
MRF18030BSR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	30 CW	1–Tone	26	14/1930,1990	50	2.1	465F/1
MRF18060A	I/O	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465/1
MRF18060AR3 ⁽¹⁸ⁱ⁾	I/O	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465/1
MRF18060ASR3 ⁽¹⁸ⁱ⁾	I/O	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465A/1
MRF18060ALSR3 ⁽¹⁸ⁱ⁾	I/O	1805–1880	60 CW	1–Tone	26	13/1805,1880	45	0.97	465A/1
MRF18060B	I/O	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465/1
MRF18060BR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465/1
MRF18060BSR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465A/1
MRF18060BLSR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	60 CW	1–Tone	26	13/1930,1990	45	0.97	465A/1
MRF18085A★	I/O	1805–1880	85 CW	1–Tone	26	15/1805,1880	52	0.64	465/1
MRF18085AR3 ⁽¹⁸ⁱ⁾ ★	I/O	1805–1880	85 CW	1–Tone	26	15/1805,1880	52	0.64	465/1
MRF18085ALSR3 ⁽¹⁸ⁱ⁾ ★	I/O	1805–1880	85 CW	1–Tone	26	15/1805,1880	52	0.64	465A/1
MRF18085B★	I/O	1930–1990	85 CW	1–Tone	26	12.5/1930,1990	50	0.64	465/1
MRF18085BR3 ⁽¹⁸ⁱ⁾ ★	I/O	1930–1990	85 CW	1–Tone	26	12.5/1930,1990	50	0.64	465/1
MRF18085BLSR3 ⁽¹⁸ⁱ⁾ ★	I/O	1930–1990	85 CW	1–Tone	26	12.5/1930,1990	50	0.64	465A/1
MRF18090A	I/O	1805–1880	90 CW	1–Tone	26	13.5/1805,1880	52	0.7	465B/1
MRF18090AS	I/O	1805–1880	90 CW	1–Tone	26	13.5/1805,1880	52	0.7	465C/1
MRF18090B	I/O	1930–1990	90 CW	1–Tone	26	13.5/1930,1990	45	0.7	465B/1
MRF18090BS	I/O	1930–1990	90 CW	1–Tone	26	13.5/1930,1990	45	0.7	465C/1

1.9 GHz, Class AB (2–CH N–CDMA and W–CDMA)

MRF19030R3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465E/1
MRF19030SR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	30 PEP	2–Tone	26	13/1990	36	2.1	465F/1
MRF19045R3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	1.65	465E/1
MRF19045SR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	9.5 AVG	N–CDMA	26	14.5/1990	23.5	1.65	465F/1
MRF5S19060M ^(46b)	I/O	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	—	—
MRF19060	I/O	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465/1
MRF19060R3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465/1
MRF19060SR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	60 PEP	2–Tone	26	12.5/1990	36	0.97	465A/1
MRF19085	I/O	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465/1
MRF19085R3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465/1
MRF19085SR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF19085LSR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	18 AVG	N–CDMA	26	13/1990	23	0.64	465A/1
MRF5S19090L ^(46b)	I/O	1930–1990	18 AVG	N–CDMA	28	14.5/1990	26	—	465/1
MRF5S19090LR3 ^(18i,46b)	I/O	1930–1990	18 AVG	N–CDMA	28	14.5/1990	26	—	465/1
MRF5S19090LSR3 ^(18i,46b)	I/O	1930–1990	18 AVG	N–CDMA	28	14.5/1990	26	—	465A/1
MRF19090	I/O	1930–1990	90 PEP	2–Tone	26	11.5/1990	35	0.65	465B/1
MRF19090S	I/O	1930–1990	90 PEP	2–Tone	26	11.5/1990	35	0.65	465C/1
MRF19090SR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	90 PEP	2–Tone	26	11.5/1990	35	0.65	465C/1

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units;

f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽³⁷⁾U = Unmatched; I = Input; I/O = Input/Output.

⁽⁴⁶⁾To be introduced: a) 1Q03; b) 2Q03; c) 3Q03

★New Product

RF High Power LDMOS Transistors (continued)

Table 4. PCS and 3G – To 2.1 GHz (continued)

Product		Frequency Band ⁽³⁷⁾	P _{out} (Typ) Watts	Test Signal	V _{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ _{JC} °C/W	Pkg/ Style
1.9 GHz, Class AB (2-CH N-CDMA and W-CDMA) (continued)									
MRF5S19100 ^(46b)	I/O	1930–1990	22 AVG	N-CDMA	28	14/1990	26	—	46S/1
MRF5S19100R3 ^(18i,46b)	I/O	1930–1990	22 AVG	N-CDMA	28	14/1990	26	—	46S/1
MRF5S19100SR3 ^(18i,46b)	I/O	1930–1990	22 AVG	N-CDMA	28	14/1990	26	—	46SA/1
MRF19120 ⁽³⁾	I/O	1930–1990	120 PEP	2-Tone	26	11.7/1990	34	0.45	375D/1
MRF19120S ⁽³⁾	I/O	1930–1990	120 PEP	2-Tone	26	11.7/1990	34	0.45	375E/1
MRF19125	I/O	1930–1990	24 AVG	N-CDMA	26	13.5/1990	22	0.53	465B/1
MRF19125S	I/O	1930–1990	24 AVG	N-CDMA	26	13.5/1990	22	0.53	465C/1
MRF19125SR3 ⁽¹⁸ⁱ⁾	I/O	1930–1990	24 AVG	N-CDMA	26	13.5/1990	22	0.53	465C/1
MRF5S19130 ^(46b)	I/O	1930–1990	26 AVG	N-CDMA	28	13.5/1990	26	—	465B/1
MRF5S19130S ^(46b)	I/O	1930–1990	26 AVG	N-CDMA	28	13.5/1990	26	—	465C/1
MRF5S19150 ^(46b)	I/O	1930–1990	34 AVG	N-CDMA	28	13.5/1990	26	—	465B/1
MRF5S19150S ^(46b)	I/O	1930–1990	34 AVG	N-CDMA	28	13.5/1990	26	—	465C/1
MRF5P20180 ^(46b)	I/O	1930–1990	38 AVG	W-CDMA	28	14/1990	25.5	—	375D/1
2.0 GHz, Class A, AB									
MRF281SR1 ^(18a)	U	1930–2000	4 PEP	2-Tone	26	12.5/2000	33	5.74	458B/1
MRF281ZR1 ^(18a)	U	1930–2000	4 PEP	2-Tone	26	12.5/2000	33	5.74	458C/1
MRF282SR1 ^(18a)	U	1930–2000	10 PEP	2-Tone	26	11.5/2000	28(min)	4.2	458B/1
MRF282ZR1 ^(18a)	U	1930–2000	10 PEP	2-Tone	26	11.5/2000	28(min)	4.2	458C/1
MRF284R1 ^(18a)	U	1930–2000	30 PEP	2-Tone	26	10.5/2000	35	2.0	360B/1
MRF284LSR1 ^(18a)	U	1930–2000	30 PEP	2-Tone	26	10.5/2000	35	2.0	360C/1
2.1 GHz, Class AB (2-CH W-CDMA, UMTS)									
MRF21010R1 ^(18a)	U	2110–2170	10 PEP	2-Tone	28	13.5/2170	35	5.5	360B/1
MRF21010LSR1 ^(18a)	U	2110–2170	10 PEP	2-Tone	28	13.5/2170	35	5.5	360C/1
MRF21030R3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	30 PEP	2-Tone	28	13/2170	33	2.1	465E/1
MRF21030SR3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	30 PEP	2-Tone	28	13/2170	33	2.1	465F/1
MRF21045R3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	10 AVG	W-CDMA	28	15/2170	23.5	1.65	465E/1
MRF21045SR3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	10 AVG	W-CDMA	28	15/2170	23.5	1.65	465F/1
MRF21060	I/O	2110–2170	60 PEP	2-Tone	28	12.5/2170	34	1.02	465/1
MRF21060R3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	60 PEP	2-Tone	28	12.5/2170	34	1.02	465/1
MRF21060SR3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	60 PEP	2-Tone	28	12.5/2170	34	1.02	465A/1
MRF21085	I/O	2110–2170	19 AVG	W-CDMA	28	13.6/2170	23	0.78	465/1
MRF21085R3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	19 AVG	W-CDMA	28	13.6/2170	23	0.78	465A/1
MRF21085LSR3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	19 AVG	W-CDMA	28	13.6/2170	23	0.78	465A/1
MRF21085SR3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	19 AVG	W-CDMA	28	13.6/2170	23	0.78	465A/1
MRF21090	I/O	2110–2170	90 PEP	2-Tone	28	11.7/2170	33	0.65	465B/1
MRF21090S	I/O	2110–2170	90 PEP	2-Tone	28	11.7/2170	33	0.65	465C/1
MRF5S21090L★	I/O	2110–2170	19 AVG	W-CDMA	28	14.5/2170	26	0.78	465/1
MRF5S21090LR3 ⁽¹⁸ⁱ⁾ ★	I/O	2110–2170	19 AVG	W-CDMA	28	14.5/2170	26	0.78	465A/1
MRF5S21090LSR3 ⁽¹⁸ⁱ⁾ ★	I/O	2110–2170	19 AVG	W-CDMA	28	14.5/2170	26	0.78	465/1
MRF5S21100L ^(46b)	I/O	2110–2170	23 AVG	W-CDMA	28	13.5/2170	26	0.7	465/1
MRF5S21100LR3 ^(18i,46b)	I/O	2110–2170	23 AVG	W-CDMA	28	13.5/2170	26	0.7	465/1
MRF5S21100LSR3 ^(18i,46b)	I/O	2110–2170	23 AVG	W-CDMA	28	13.5/2170	26	0.7	465A/1
MRF21120 ⁽³⁾	I/O	2110–2170	120 PEP	2-Tone	28	11.4/2170	34.5	0.45	375D/1
MRF21125	I/O	2110–2170	20 AVG	W-CDMA	28	13/2170	18	0.53	465B/1
MRF21125S	I/O	2110–2170	20 AVG	W-CDMA	28	13/2170	18	0.53	465C/1
MRF21125SR3 ⁽¹⁸ⁱ⁾	I/O	2110–2170	20 AVG	W-CDMA	28	13/2170	18	0.53	465C/1

⁽³⁾Internal Impedance Matched Push-Pull Transistors

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units;

f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽³⁷⁾U = Unmatched; I = Input; I/O = Input/Output.

⁽⁴⁶⁾To be introduced: a) 1Q03; b) 2Q03; c) 3Q03

★New Product

Freescale Semiconductor, Inc.

RF High Power LDMOS Transistors (continued)

Table 4. PCS and 3G – To 2.1 GHz (continued)

Product	Frequency Band ⁽³⁷⁾	P _{out} (Typ) Watts	Test Signal	V _{DD} Volts	Gain (Typ)/Freq. dB/MHz	η Eff. (Typ) %	θ _{JC} °C/W	Pkg/ Style
---------	--------------------------------	------------------------------	-------------	-----------------------	-------------------------	----------------	----------------------	------------

2.1 GHz, Class AB (2-CH W-CDMA, UMTS) (continued)

MRF5S21130★	I/O	2110–2170	28 AVG	W-CDMA	28	13.5/2170	26	0.54	465B/1
MRF5S21130R3 ⁽¹⁸ⁱ⁾ ★	I/O	2110–2170	28 AVG	W-CDMA	28	13.5/2170	26	0.54	465B/1
MRF5S21130S★	I/O	2110–2170	28 AVG	W-CDMA	28	13.5/2170	26	0.54	465C/1
MRF5S21130SR3 ⁽¹⁸ⁱ⁾ ★	I/O	2110–2170	28 AVG	W-CDMA	28	13.5/2170	26	0.54	465C/1
MRF5S21150★	I/O	2110–2170	33 AVG	W-CDMA	28	12.5/2170	25	0.47	465B/1
MRF5S21150R3 ⁽¹⁸ⁱ⁾ ★	I/O	2110–2170	33 AVG	W-CDMA	28	12.5/2170	25	0.47	465B/1
MRF5S21150S★	I/O	2110–2170	33 AVG	W-CDMA	28	12.5/2170	25	0.47	465C/1
MRF5S21150SR3 ⁽¹⁸ⁱ⁾ ★	I/O	2110–2170	33 AVG	W-CDMA	28	12.5/2170	25	0.47	465C/1
MRF5P21180★	I/O	2110–2170	38 AVG	W-CDMA	28	14/2170	25.5	0.40	375D/1
MRF21180 ⁽³⁾	I/O	2110–2170	38 AVG	W-CDMA	28	12.1/2170	22	0.46	375D/1
MRF21180S ⁽³⁾	I/O	2110–2170	38 AVG	W-CDMA	28	12.1/2170	22	0.46	375E/1
MRF5P21240 ^(46c)	I/O	2110–2170	52 AVG	W-CDMA	28	13/2170	24.5	—	375D/1

⁽³⁾Internal Impedance Matched Push-Pull Transistors

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units;

f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽³⁷⁾U = Unmatched; I = Input; I/O = Input/Output.

⁽⁴⁶⁾To be introduced: a) 1Q03; b) 2Q03; c) 3Q03

Freescale Semiconductor, Inc.

RF Power GaAs Transistors

Motorola power GaAs transistors are made using an InGaAs PHEMT epitaxial structure for superior RF efficiency and linearity. The FETs listed in this section are designed for operation in base station infrastructure RF power amplifiers and are grouped according to frequency range and type of application. Parts are listed first by order of operating voltage, then by increasing output power.

Table 1. 3.5 GHz – Linear Transistors

Product	Frequency Band ⁽³⁷⁾		P _{out} (Typ) Watts	Test Signal	V _{DD} Volts	Gain (Typ)/Freq. dB/GHz	η Eff. (Typ) %	θ _{JC} °C/W	Pkg/ Style
3.5 GHz, Class AB (WLL, BWA, W-CDMA)									
MRFG35002MT1 ^(18f,46b)	U	3.5 G	0.2 AVG	W-CDMA ⁽⁴⁴⁾	12	10/3.5	30	—	466/1
MRFG35003MT1 ^(18f,46b)	U	3.5 G	0.3 AVG	W-CDMA ⁽⁴⁴⁾	12	12.5/3.5	26	—	466/1
MRFG35003M6T1 ^(18f) ★	U	3.5 G	0.45 AVG	W-CDMA ⁽⁴⁴⁾	6	9/3.5	24	—	466/1
MRFG35005MT1 ^(18f,46b)	U	3.5 G	0.45 AVG	W-CDMA ⁽⁴⁴⁾	12	11.5/3.5	25	—	466/1
MRFG35010	U	3.5 G	1 AVG	W-CDMA ⁽⁴⁴⁾	12	10/3.5	30	4.8 ⁽¹⁵⁾	360D/1
MRFG35010MT1 ^(18f) ★	U	3.5 G	0.9 AVG	W-CDMA ⁽⁴⁴⁾	12	10/3.5	28		466/1
MRFG35030 ⁽⁹⁾	I/O	3.5 G	4 AVG	W-CDMA ⁽⁴⁴⁾	12	10/3.5	26		—

⁽⁹⁾In development.

⁽¹⁵⁾Class A = 5.3

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units;

f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽³⁷⁾U = Unmatched; I = Input; I/O = Input/Output.

⁽⁴⁴⁾Peak-to-Average Power Ratio = 10 dB

⁽⁴⁶⁾To be introduced: a) 1Q03; b) 2Q03; c) 3Q03

★New Product

Freescale Semiconductor, Inc.

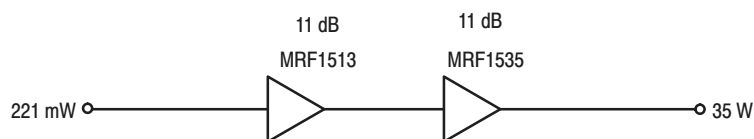
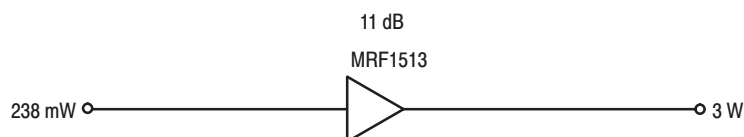
RF Low Power Transistors

Product	Gain – Bandwidth		NFmin @ f		Gain @ f		Maximum Ratings		Packaging
	f _T Typ GHz	I _C mA	Typ dB	GHz	Typ dB	GHz	V(BR) CEO Volts	I _C mA	
MBC13900 ^(18c)	15	20	1.0	1.0	17	1.0	7.0	20	318M/ SOT-343
			1.3	2.0	14	2.0			

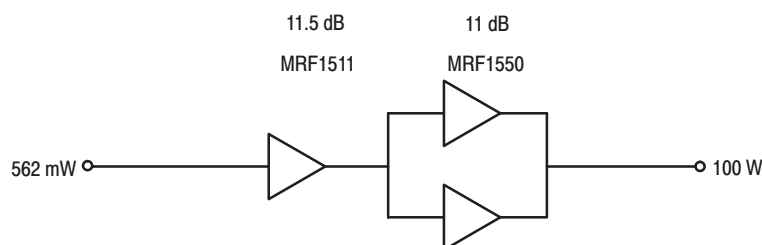
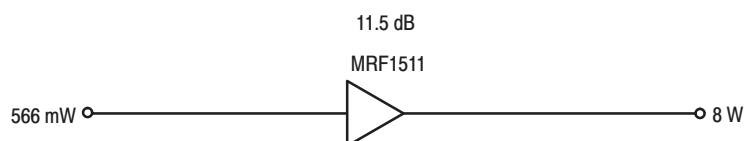
⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

Freescale Semiconductor, Inc.

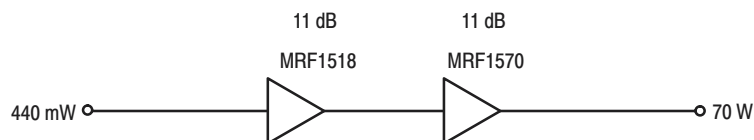
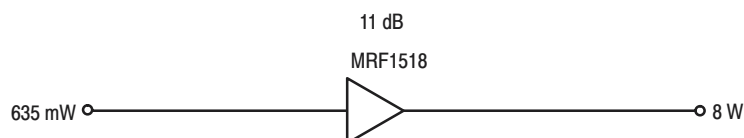
RF High Power Amplifier Line-ups



Mobile – UHF 400 – 520 MHz



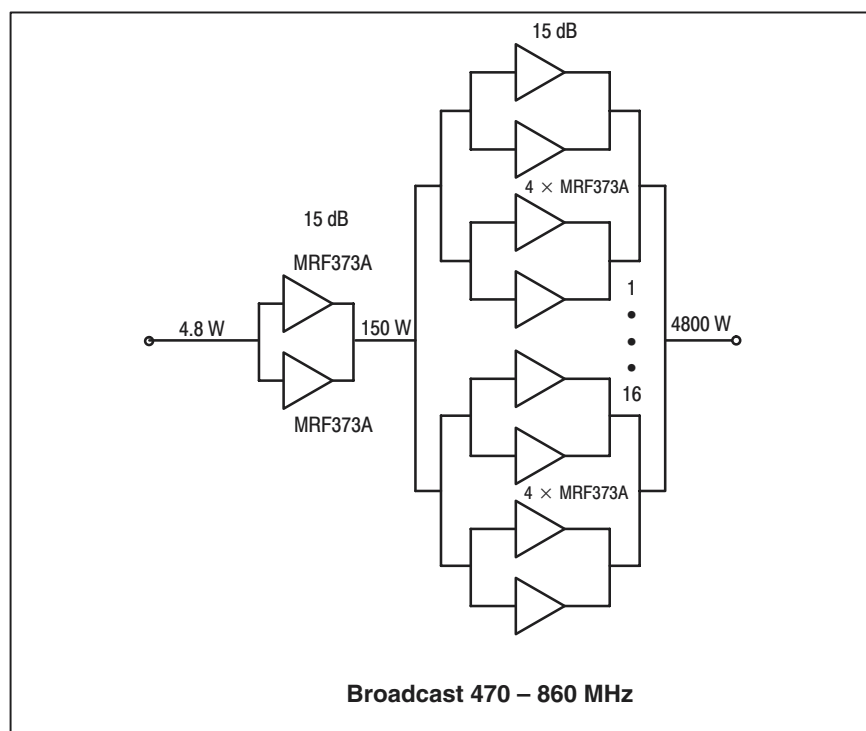
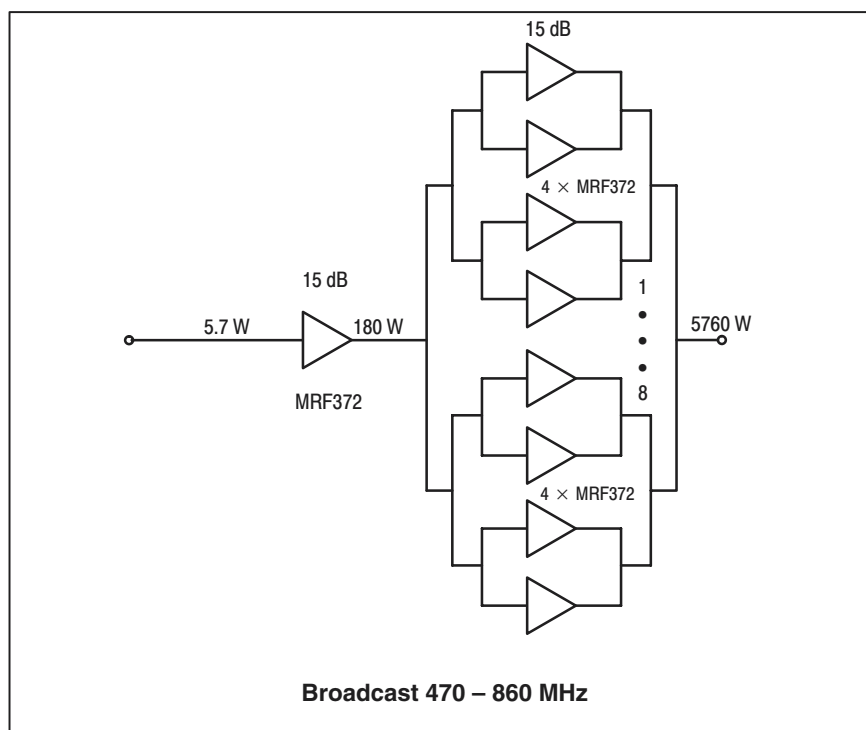
Mobile – VHF 135 – 175 MHz



Mobile – UHF 400 – 470 MHz

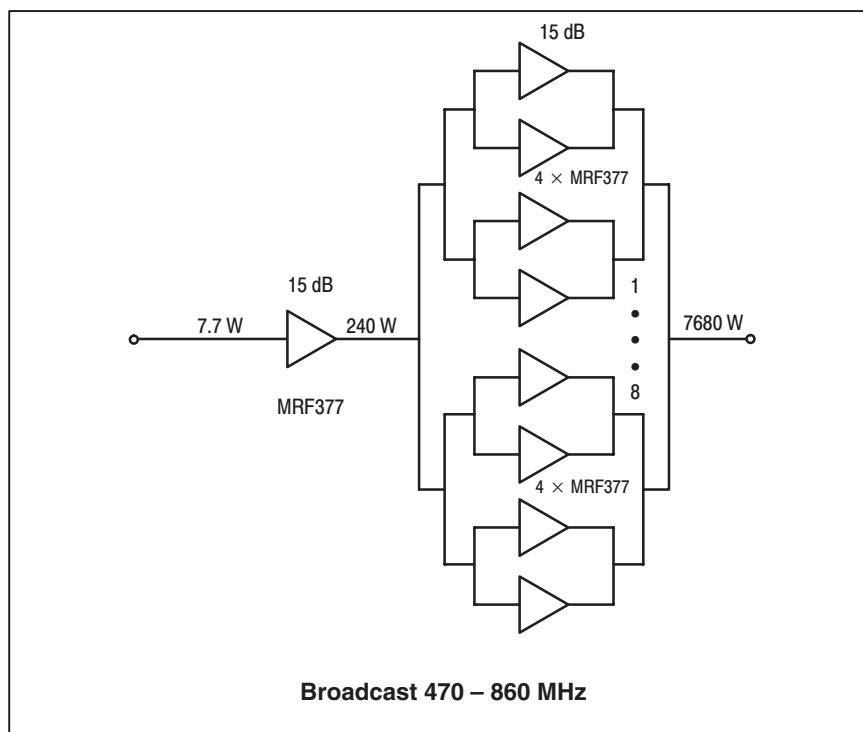
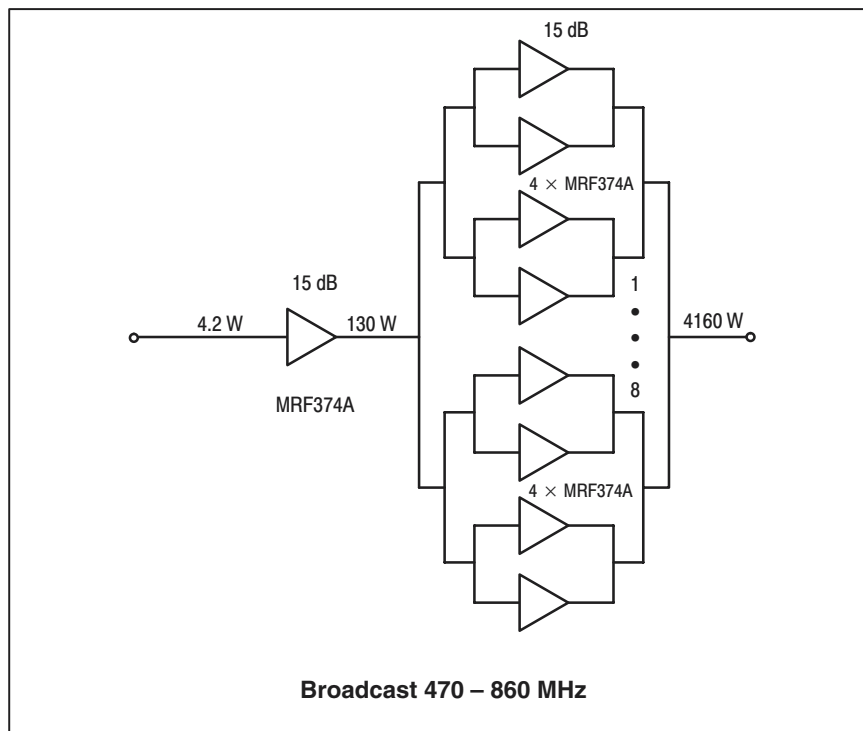
Freescale Semiconductor, Inc.

RF High Power Amplifier Line-ups (continued)



Freescale Semiconductor, Inc.

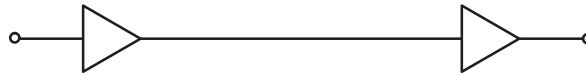
RF High Power Amplifier Line-ups (continued)



Freescale Semiconductor, Inc.

RF High Power Amplifier Line-ups (continued)

GSM and EDGE – 900 MHz



Ceramic	MRF9030	MRF9045	MRF9100
		MRF9060	MRF9120
		MRF6522-70	MRF9130L
		MRF9080	MRF9135L
		MRF9085	MRF9180
			MRF9200L
			MRF9210

Hybrid	MHL9838
	MHL9236
	MHL9318

Plastic	MRF9002R2	MRF9030M
	MHVIC910HR2	MRF9045M
	MHVIC915	MRF9060M
	MW4IC915	
	MWIC930	

GSM and EDGE – 1800 MHz



Ceramic	MRF18030A	MRF18060A
		MRF18085A
		MRF18090A

Hybrid	MHL18336
	MHL18926
	MHPA18010

Plastic	MHVIC2115
	MW4IC2020

Freescal Semiconductor, Inc.

RF High Power Amplifier Line-ups (continued)

GSM and EDGE – 1900 MHz



Ceramic

MRF18030B

MRF18060B

MRF18085B

MRF18090B

Hybrid

MHPA19010

MHL19338

MHL19926

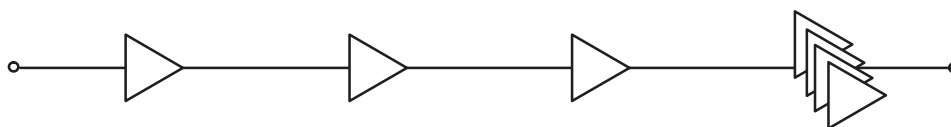
MHL19936

Plastic

MHVIC2115

MW4IC2020

N-CDMA – 1900 MHz



Ceramic

MRF21010

MRF19030

MRF19045

MRF19060

MRF19085

MRF19090

MRF5S19090L

MRF5S19100

MRF19120

MRF19125

MRF5S19130

MRF5S19150

MRF5P20180

Hybrid

MHL19338

MHL19926

MHL19936

MHPA19010

Plastic

MHVIC2115

MW4IC2020

Freescal Semiconductor, Inc.

RF High Power Amplifier Line-ups (continued)

W-CDMA – 2200 MHz

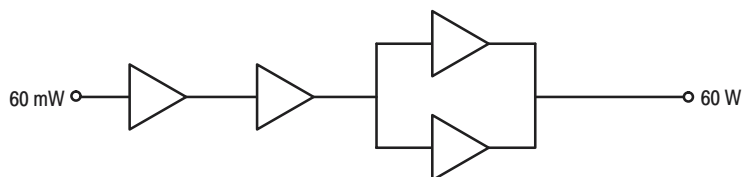


Ceramic	MRF21010	MRF21030	MRF21060	MRF21120	MRF5S21090L
		MRF21045	MRF21085	MRF21125	MRF5S21100L
			MRF21090	MRF21180	MRF5S21130
					MRF5P21150
					MRF5P21180
					MRF5P21240

Hybrid	MHL21336	MHPA21010
---------------	----------	-----------

Plastic	MHVIC2115	MW4IC2230
----------------	-----------	-----------

WLL – 3500 MHz



Ceramic	MRFG35010	MRFG35030
----------------	-----------	-----------

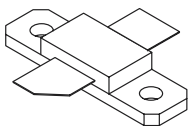
Plastic	MRFG35002M	MRFG35010M
----------------	------------	------------

Freescale Semiconductor, Inc.

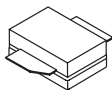
RF Transistor Packages



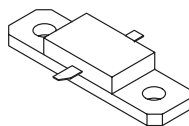
CASE 318M
STYLE 1
(SOT-343)



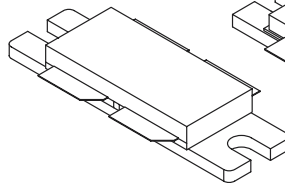
CASE 360B
STYLE 1
(NI-360)



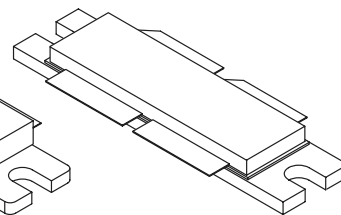
CASE 360C
STYLE 1
(NI-360S)



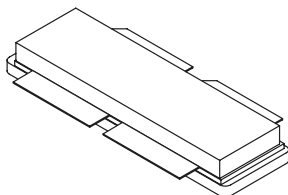
CASE 360D
STYLE 1
(NI-360HF)



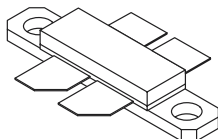
CASE 375B
STYLE 1
(NI-860)



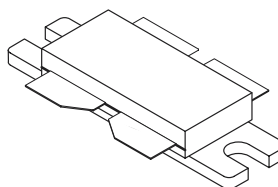
CASE 375D
STYLE 1
(NI-1230)



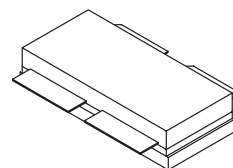
CASE 375E
STYLE 1
(NI-1230S)



CASE 375F
STYLE 1
(NI-650)



CASE 375G
STYLE 1
(NI-860C3)



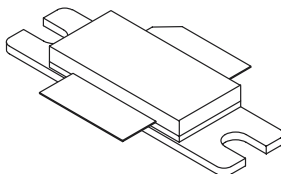
CASE 375H
STYLE 1
(NI-860S)



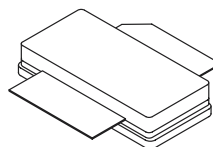
CASE 458B
STYLE 1
(NI-200S)



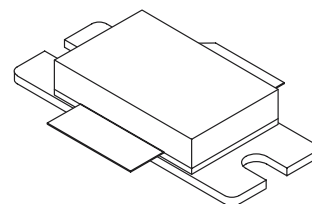
CASE 458C
STYLE 1
(NI-200Z)



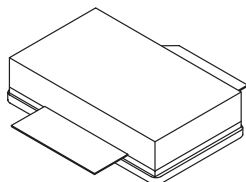
CASE 465
STYLE 1
(NI-780)



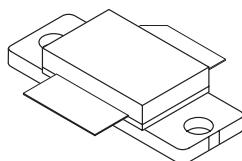
CASE 465A
STYLE 1
(NI-780S)



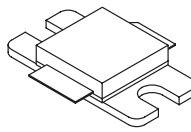
CASE 465B
STYLE 1
(NI-880)



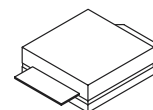
CASE 465C
STYLE 1
(NI-880S)



CASE 465D
STYLE 1
(NI-600)



CASE 465E
STYLE 1
(NI-400)



CASE 465F
STYLE 1
(NI-400S)

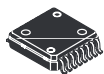


CASE 466
STYLE 1
PLASTIC
(PLD 1.5)

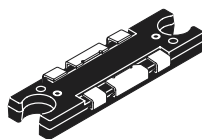
SCALE 1:1

Freescale Semiconductor, Inc.

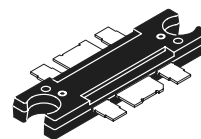
RF Transistor Packages (continued)



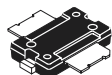
CASE 978
PLASTIC
(PFP-16)



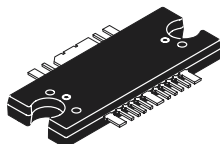
CASE 1264
STYLE 1
PLASTIC
(TO-272)



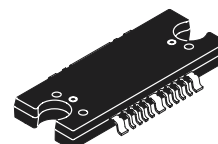
CASE 1264A
STYLE 1
PLASTIC
(TO-272 Straight Lead)



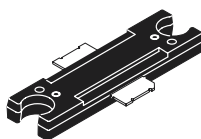
CASE 1265
STYLE 1
PLASTIC
(TO-270)



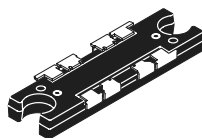
CASE 1329
STYLE 1
PLASTIC
(TO-272 Wide Body Multi Lead)



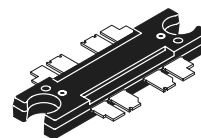
CASE 1329A
STYLE 1
PLASTIC
(TO-272 Wide Body Multi Lead Gull Wing)



CASE 1337
STYLE 1
PLASTIC
(TO-272 Dual Lead)



CASE 1366
STYLE 1
PLASTIC
(TO-272 Split Lead)



CASE 1366A
STYLE 1
PLASTIC
(TO-272 Split Lead-Straight Lead Version)

SCALE 1:1

Motorola RF Amplifier ICs and Modules

Motorola's RF portfolio includes many hybrid designs optimized to perform in narrowband base station transmitter applications and IC designs optimized for wideband applications. Motorola modules feature two or more active transistors (LDMOS or GaAs die technology) and their associated 50 ohm matching networks. Circuit substrate and metallization have been selected for optimum performance and reliability. For PA designers, IC driver devices offer the benefits of multiple gain stages in one package with most of the decoupling and matching circuitry incorporated into a single low-cost plastic device.

Table of Contents

	Page
RF Amplifier ICs and Modules	1-29
Base Stations	1-30
Packages	1-32

Motorola RF Amplifier ICs and Modules

Complete amplifiers with 50 ohm input impedances are available for all popular base station transmitter systems, including GSM and CDMA, covering frequencies from 800 MHz up to 2.2 GHz.

Base Stations

Designed for applications such as macrocell drivers and microcell output stage, these Class AB amplifiers are ideal for base station systems with power requirements up to 30 watts.

Table 1. Base Station IC Drivers

Product	Frequency MHz	P1dB Watts	Gain (Typ) dB	Supply Voltage Volts	Class	System Application	Die Technology	Pkg/Style
MHVIC910HR2 ^(18e)	921–960	10	39	26	AB	GSM900	LDMOS	978/–
MHVIC915R2 ^(18e,46a)	746–960	15	30	26	AB	N–CDMA, GSM/GSM EDGE	LDMOS	978/–
MW4IC915MBR1 ^{(18a)★}	860–960	15	30	26	AB	N–CDMA, GSM/GSM EDGE	LDMOS	1329/1
MW4IC915GMBR1 ^{(18a)★}	860–960	15	30	26	AB	N–CDMA, GSM/GSM EDGE	LDMOS	1329A/1
MWIC930R1 ^{(18a)★}	746–960	30	30	27	AB	N–CDMA, GSM/GSM EDGE	LDMOS	1329/1
MWIC930GR1 ^{(18a)★}	746–960	30	30	27	AB	N–CDMA, GSM/GSM EDGE	LDMOS	1329A/1
MW4IC2020MBR1 ^(18a,46a)	1805–1990	20	29	26	AB	N–CDMA, GSM/GSM EDGE	LDMOS	1329/1
MW4IC2020GMBR1 ^(18a,46a)	1805–1990	20	29	26	AB	N–CDMA, GSM/GSM EDGE	LDMOS	1329A/1
MHVIC2115R2 ^{(18e)★}	2110–2170	15	30	26	AB	W–CDMA	LDMOS	978/–
MW4IC2230MBR1 ^(18a,46b)	2110–2170	30	32	28	AB	W–CDMA	LDMOS	1329/1
MW4IC2230GMBR1 ^(18a,46b)	2110–2170	30	32	28	AB	W–CDMA	LDMOS	1329A/1

Table 2. Base Station Module Drivers

Designed for applications such as macrocell drivers and microcell output stage, these Class AB amplifiers are ideal for base station systems with power requirements up to 10 watts.

Product	Frequency MHz	P1dB Watts	Gain (Min) dB	Supply Voltage Volts	Class	System Application	Die Technology	Pkg/Style
MHPA18010 ^(46a)	1805–1880	10	24.5	28	AB	N–CDMA	LDMOS	301AP/3
MHPA19010★	1930–1990	10	24.5	28	AB	PCS1900	LDMOS	301AP/3
MHPA21010★	2110–2170	10	23.7	28	AB	W–CDMA	LDMOS	301AP/3

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽⁴⁶⁾To be introduced: a) 1Q03; b) 2Q03

★New Product

Freescale Semiconductor, Inc.

RF Amplifier ICs and Modules: Base Stations (continued)

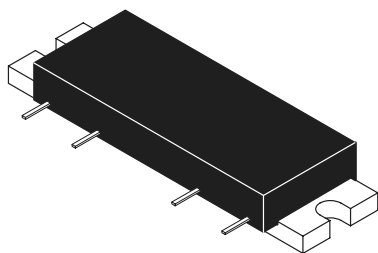
Table 3. Base Station Module Pre-Drivers

These 50 ohm amplifiers are recommended for modern multi-tone CDMA, TDMA and UMTS base station pre-driver applications. Their high third-order intercept point, tight phase and gain control, and excellent group delay characteristics make these devices ideal for use in high-power feedforward loops.

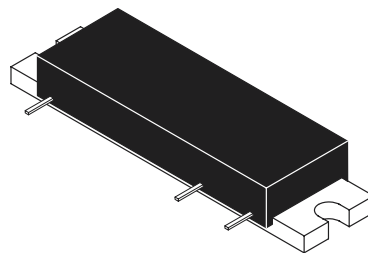
Ultra-Linear (for CDMA, W-CDMA, TDMA, Analog) – Class A (LDMOS Die) – Lateral MOSFETs

Product	Frequency Band MHz	V _{DD} (Nom.) Volts	I _{DD} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) dB	P _{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm	NF (Typ) dB	Pkg/ Style
MHL9838	800–925	28	770	31	.1	39	50	3.7	301AP/1
MHL9236	800–960	26	550	30.5	.1	34	47	3.5	301AP/1
MHL9236M	800–960	26	550	30.5	.1	34	47	3.5	301AP/2
MHL9318	860–900	28	500	17.5	.1	35.5	49	3.0	301AS/1
MHL18336	1800–1900	26	500	30	.2	36	46	4.2	301AP/1
MHL18926	1805–1880	26	1100	28.6	.3	40	50	4.2	301AY/1
MHL19338	1900–2000	28	500	30	.1	36	46	4.2	301AP/1
MHL19926	1930–1990	26	1000	29.4	.3	40	50	4.2	301AY/1
MHL19936	1900–2000	26	1400	29	.2	41	49.5	4.2	301AY/1
MHL21336	2110–2170	26	500	31	.15	35	45	4.5	301AP/1

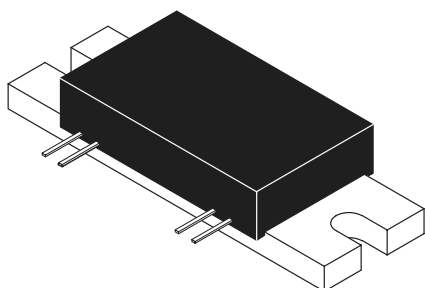
Freescale Semiconductor, Inc. **RF Amplifier ICs and Modules Packages**



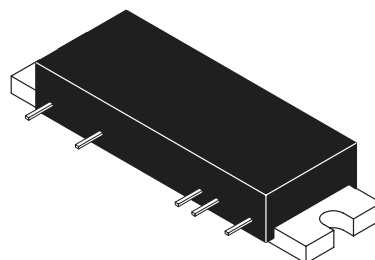
CASE 301AP
STYLE 1, 2, 3



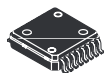
CASE 301AS
STYLE 1



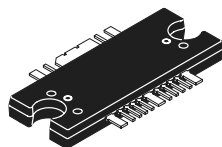
CASE 301AW
STYLE 1



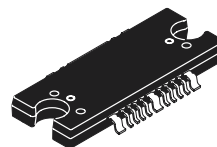
CASE 301AY
STYLE 1



CASE 978
PLASTIC
(PFP-16)



CASE 1329
STYLE 1
PLASTIC
(TO-272 Wide Body Multi Lead)



CASE 1329A
STYLE 1
PLASTIC
(TO-272 Wide Body Multi Lead Gull Wing)

SCALE 1:1

Motorola RF General Purpose Linear Amplifier Modules

Motorola general purpose linear amplifier modules are designed and specified for 50 ohm applications where linearity and dynamic range are essential.

Table of Contents

	Page
RF General Purpose Linear Amplifier Modules	1-34
Packages	1-34

Freescale Semiconductor, Inc.

Motorola RF General Purpose Linear Amplifier Modules

This device has been optimized for 50 ohm applications. It was designed for multi-purpose applications where linearity and dynamic range are of primary concern.

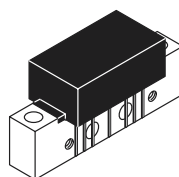
General Purpose Linear Amplifier Modules — Class A – Silicon Bipolar

Product	Frequency Band MHz	V _{CC} (Nom) Volts	I _{CC} (Nom) mA	Gain (Nom) @ 100 MHz dB	Gain Flatness (Typ) dB	P _{1dB} (Typ) @ 200 MHz dBm	3rd Order Intercept (Typ) dBm	NF (Typ) @ 200 MHz dB	Pkg/Style
MHW1345★	10–200	24	310	34.5	1.0	28	44	3.8	1302/1

Note: Possible replacement for CA2830C.

★New Product

RF General Purpose Linear Amplifier Module Package



CASE 1302
STYLE 1

SCALE 1:2

Motorola CATV Distribution Amplifier Modules

Motorola Hybrids are manufactured using the latest CATV generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels. Additions to our CATV product family include 40–870 MHz high output gallium arsenide (GaAs) power doublers as well as low distortion, low power consumption reverse amplifiers.

Table of Contents

	Page
CATV Distribution Amplifier Modules	1–35
Forward Amplifier Modules	1–36
Reverse Amplifier Modules	1–39
Packages	1–41

Motorola CATV Distribution Amplifier Modules

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Forward Amplifier Modules

40–1000 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				DC Current mA Typ	Noise Figure @ 1000 MHz dB Max	Pkg/ Style
			Output Level dBmV/CH	2nd Order Test dBc	Composite Triple Beat	Cross Modulation			
					dBc 152 CH	dBc 152 CH			

Preamplifiers

MHW9182B	18.5	152	+38	−63 ⁽⁴⁰⁾	−61	−61	210	7.5	714Y/1
MHW9242A	23.2	152	+38	−61 ⁽⁴⁰⁾	−58	−59	318	8.0	1302/1

40–870 MHz High Output Hybrids, $V_{CC} = 24$ Vdc, Class A — GaAs

Product	Hybrid Gain (Nom) @ 870 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				DC Current mA Typ	Noise Figure @ 870 MHz dB Max	Pkg/ Style
			Output Level dBmV/CH	2nd Order Test dBc	Composite Triple Beat	Cross Modulation			
					dBc 132 CH	dBc 132 CH			

Preamplifiers

MHW9146★	14.3	132	+44	−60 ⁽³⁶⁾	−60	−55	245	5.5	1302/1
MHW9186★	18.5	132	+44	−60 ⁽³⁶⁾	−58	−52	250	5.0	1302/1
MHW9206★	20.2	132	+44	−59 ⁽³⁶⁾	−57	−51	245	4.5	1302/1
MHW9236 ^(46a)	23.6	132	+44	−60 ⁽³⁶⁾	−60	−53	255	6.0	1302/1
MHW9276★	27.9	132	+44	−60 ⁽³⁶⁾	−60	−53	250	6.5	1302/1

Power Doublers

MHW9187	20	132	+48	−62 ⁽³⁴⁾	−56	−55	425	4.5	1302/1
MHW9188★	20.3	132	+48	−62 ⁽³⁴⁾	−56	−55	425	4.5	1302/1
MHW9189 ⁽³⁵⁾ ★	20.3	132	+48	−62 ⁽³⁴⁾	−56	−55	425	4.5	1302/2
MHW9227★	22.1	132	+48	−62 ⁽³⁴⁾	−56	−55	425	4.5	1302/1
MHW9247★	24.9	132	+48	−62 ⁽³⁴⁾	−56	−54	440	7.0	1302/1
MHW9267★	27.6	132	+48	−60 ⁽³⁴⁾	−56	−54	440	7.0	1302/1

⁽³⁴⁾Composite 2nd order; $V_{out} = +48$ dBmV/ch

⁽³⁵⁾Mirror image of MHW9188

⁽³⁶⁾Composite 2nd order; $V_{out} = +44$ dBmV/ch

⁽⁴⁰⁾Composite 2nd Order; $V_{out} = +38$ dBmV/ch

⁽⁴⁶⁾To be introduced: a) 1Q03; b) 2Q03

★New Product

Freescale Semiconductor, Inc.

CATV Distribution: Forward Amplifier Modules (continued)

40–870 MHz High Output MMIC, $V_{CC} = 24$ Vdc, Class A — GaAs

Product	Hybrid Gain (Nom) @ 870 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				DC Current mA Typ	Noise Figure @ 870 MHz dB Max	Pkg/ Style
			Output Level dBmV/CH	2nd Order Test dBc	Composite Triple Beat	Cross Modulation			
					dBc 132 CH	dBc 132 CH			

Preamplifiers

MMG1001R2 ^(18e) ★	18.5	132	+44	−58	−56	−52	250	5.0	978–03
------------------------------	------	-----	-----	-----	-----	-----	-----	-----	--------

Power Doublers

MMG2001R2 ^(18e) ★	19.5	132	+48	−60	−54	−53	425	4.5	978–03
------------------------------	------	-----	-----	-----	-----	-----	-----	-----	--------

40–870 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 870 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				DC Current mA Typ	Noise Figure @ 870 MHz dB Max	Pkg/ Style
			Output Level dBmV/CH	2nd Order Test dBc	Composite Triple Beat	Cross Modulation			
					dBc 128 CH	dBc 128 CH			

Preamplifiers

MHW8202B★	20.9	128	+38	−66 ⁽⁴⁰⁾	−63	−62	220	7.0	1302/1
-----------	------	-----	-----	---------------------	-----	-----	-----	-----	--------

40–860 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				DC Current mA Typ	Noise Figure @ 860 MHz dB Max	Pkg/ Style
			Output Level dBmV/CH	2nd Order Test dBc	Composite Triple Beat	Cross Modulation FM = 55 MHz			
					dBc 128 CH	dBc 128 CH			

Preamplifiers

MHW8182B	18.5	128	+38	−64 ⁽⁴⁰⁾	−66	−65	220	7.5	714Y/1
MHW8222B	21.9	128	+38	−60 ⁽⁴⁰⁾	−64	−63	220	7.0	1302/1
MHW8242A	24	128	+38	−62 ⁽⁴⁰⁾	−64	−62	318	7.5	1302/1
MHW8272A	27.2	128	+38	−64 ⁽⁴⁰⁾	−64	−62	310	7.0	1302/1

Power Doublers

MHW8185L ⁽²¹⁾	18.5	128	+40	−62 ⁽³⁹⁾	−63	−64	365	8.5*	714Y/1
MHW8185	18.8	128	+40	−62 ⁽³⁹⁾	−64	−64	400	8.0	714Y/1
MHW8205L ⁽²²⁾	19.5	128	+40	−60 ⁽³⁹⁾	−63	−64	365	8.5*	714Y/1
MHW8205	19.8	128	+40	−60 ⁽³⁹⁾	−63	−64	400	8.0	714Y/1

*@ 870 MHz

⁽¹⁸⁾Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units;

f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units; j) T1 = 500 units; k) R2 = 450 units; l) T1 = 5,000 units; m) R2 = 2,000 units.

⁽²¹⁾Low DC Current Version of MHW8185; Typical I_{CC} @ Vdc = 24 V is 365 mA.

⁽²²⁾Low DC Current Version of MHW8205; Typical I_{CC} @ Vdc = 24 V is 365 mA.

⁽³⁹⁾Composite 2nd order; $V_{out} = +40$ dBmV/ch

⁽⁴⁰⁾Composite 2nd Order; $V_{out} = +38$ dBmV/ch

★New Product

Freescale Semiconductor, Inc.

CATV Distribution: Forward Amplifier Modules (continued)

40–750 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				DC Current mA Typ	Noise Figure @ 750 MHz dB Max	Pkg/ Style
			Output Level dBmV/CH	2nd Order Test dBc	Composite Triple Beat	Cross Modulation FM = 55 MHz			
					dBc 110 CH	dBc 110 CH			

Preamplifiers

MHW7182B	18.5	110	+40	−63 ⁽³⁹⁾	−66	−64	220	6.5	714Y/1
MHW7222B	21.9	110	+40	−60 ⁽³⁹⁾	−61	−60	220	6.5	1302/1
MHW7242A	24	110	+40	−62 ⁽³⁹⁾	−63	−61	318	7.0	1302/1
MHW7272A	27.2	110	+40	−64 ⁽³⁹⁾	−64	−60	310	6.5	1302/1
MHW7292A ★	29	110	+40	−60 ⁽³⁹⁾	−60	−60	310	6.5*	1302/1

*@ 770 MHz

40–750 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar (continued)

Product	Hybrid Gain (Nom) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				DC Current mA Typ	Noise Figure @ 750 MHz dB Max	Pkg/ Style
			Output Level dBmV/CH	2nd Order Test dBc	Composite Triple Beat	Cross Modulation FM = 55 MHz			
					dBc 110 CH	dBc 110 CH			

Power Doublers

MHW7185CL	18.5	110	+44	−64 ⁽³⁶⁾	−61	−63	370	7.5	714Y/1
MHW7185C	18.8	110	+44	−64 ⁽³⁶⁾	−62	−63	400	7.5	714Y/1
MHW7205CL	19.5	110	+44	−63 ⁽³⁶⁾	−61	−62	365	7.5	714Y/1
MHW7205C	19.8	110	+44	−63 ⁽³⁶⁾	−61	−62	400	7.5	714Y/1

40–550 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				DC Current mA Typ	Noise Figure @ 550 MHz dB Max	Pkg/ Style
			Output Level dBmV/CH	2nd Order Test dBc	Composite Triple Beat	Cross Modulation			
					dBc 77 CH	dBc 77 CH			

Forward Amplifiers

MHW6342T	34.5	77	+44	−57 ⁽³⁶⁾	−57	−57	310	6.5	1302/1
----------	------	----	-----	---------------------	-----	-----	-----	-----	--------

⁽³⁶⁾Composite 2nd order; $V_{out} = +44$ dBmV/ch

⁽³⁹⁾Composite 2nd order; $V_{out} = +40$ dBmV/ch

★New Product

Freescale Semiconductor, Inc.

Reverse Amplifier Modules

5–200 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 10 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications						DC Current mA Typ	Noise Figure @ 175 MHz dB Max	Pkg/ Style
			Output Level dBmV/ CH	2nd Order Test ⁽³⁰⁾ dBc	Composite Triple Beat dBc		Cross Modulation dBc				
					22 CH	26 CH	22 CH	26 CH			
MHW1244	24	22, 26	+50	−72	−68	−67.5 ⁽¹⁹⁾	−61	−61 ⁽¹⁹⁾	210	5.0	1302/1

Low Current Amplifiers — 5–200 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 5 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications								DC Current mA Typ	Noise Figure @ 200 MHz dB Max	Pkg/ Style
			Output Level dBmV/ CH	2nd Order Test		Composite Triple Beat		Cross Modulation					
				dBc		dBc		dBc					
				6 CH	10 CH	6 CH	10 CH	6 CH	10 CH				
MHW1223LA	22.7	6,10	+50	−68	−65	−75	−66	−65	−60	95	7.0	1302/1	
MHW1253LA	25.5	6,10	+50	−68	−66	−75	−66	−65	−61	95	6.5	1302/1	
MHW1303LA	30.8	6,10	+50	−68	−65	−74	−64	−64	−58	95	5.7	1302/1	

Low Current Amplifiers — 5–150 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 5 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications							DC Current mA Typ	Noise Figure @ 150 MHz dB Max	Pkg/ Style
			Output Level dBmV/ CH	2nd Order Test		Composite Triple Beat		Cross Modulation				
				dBc		dBc		dBc				
				6 CH	10 CH	6 CH	10 CH	6 CH	10 CH			
MHW1353LA	35.2	6, 10	+50	−68	−65	−73	−62	−63	−57	95	5.4	1302/1

Low Current Amplifiers — 5–65 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 5 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications								DC Current mA Typ	Noise Figure @ 65 MHz dB Max	Pkg/Style
			Output Level dBmV/CH	2nd Order Test		Composite Triple Beat		Cross Modulation					
				dBc		dBc		dBc					
				6 CH	10 CH	6 CH	10 CH	6 CH	10 CH				
MHW1224LA	22.7	6,10	+50	−68	−65	−75	−66	−65	−60	95	7.0	1302/1	
MHW1254LA	25.5	6,10	+50	−68	−66	−75	−66	−65	−61	95	6.5	1302/1	
MHW1304LA	30.8	6,10	+50	−68	−65	−74	−64	−64	−58	95	5.7	1302/1	
MHW1354LA	35.2	6,10	+50	−68	−65	−73	−62	−63	−57	95	5.4	1302/1	

⁽¹⁹⁾Typical⁽³⁰⁾Channels 2 and A @ 7

Freescale Semiconductor, Inc.

CATV Distribution: Reverse Amplifier Modules (continued)

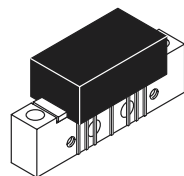
Low Current Amplifiers — 5–50 MHz Hybrids, $V_{CC} = 24$ Vdc, Class A — Silicon Bipolar

Product	Hybrid Gain (Nom) @ 5 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				DC Current mA Typ	Noise Figure @ 50 MHz dB Max	Pkg/ Style
			Output Level dBmV/CH	2nd Order Test ⁽³⁰⁾ dBc	Composite Triple Beat	Cross Modulation			
					dBc 3 CH	dBc 4 CH			
MHW1254L	25	4	+50	−70	−70	−62	115	4.5	1302/1

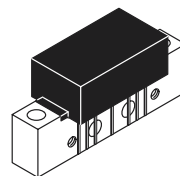
⁽³⁰⁾Channels 2 and A @ 7

Freescale Semiconductor, Inc.

CATV Distribution Amplifier Module Packages



CASE 714Y
STYLE 1



CASE 1302
STYLE 1, 2

SCALE 1:2

Chapter Two

RF Front End ICs – Data Sheets

Device Number	Page Number
RFICs	
Upconverter/Exciter	
MC13751	2-27
Downconverter	
MC13770	2-31
Power Amplifiers	
MRFIC0970	2-92
MRFIC1870	2-98
MMM5047	2-36
MMM5062	2-56
MMM5063	2-75
RF Building Blocks	
Amplifiers	
MBC13720	2-3
MBC13916	2-17

Technical Data Sheet

MBC13720/D
Rev. 1, 01/2002

SiGe:C Low Noise
Amplifier with Bypass
Switch



MOTOROLA
intelligence everywhere™

digital dna™

MBC13720



(Scale 2:1)

Package Information

Plastic Package
Case 419B
(SOT-363)

Ordering Information

Device	Device Marking	Package
MBC13720T1	20	SOT-363

The MBC13720 is a high IP3, low noise amplifier designed for 400 MHz to 2.4 GHz multistandard wireless applications. The input and output match is external to allow maximum design flexibility. The LNA has two selectable current settings as well as standby mode. The LNA will operate from a 2.5 to 3.0 V supply. The MBC13720 is fabricated using Motorola's Advanced RF BiCMOS process with the SiGe:C option and housed in an ultra small SOT-363 surface mount package.

- Selectable Current, 5.0 mA or 11 mA
- Standby Mode to Turn Off Device Completely
- High Input IP3:
10 dBm @ 1.9 GHz
13 dBm @ 2.4 GHz
- Low Noise Figure:
1.38 dB @ 1.9 GHz
1.55 dB @ 2.4 GHz
- Gain @ 9.0 mA, 2.75 V:
14.5 dB @ 1.9 GHz
12 dB @ 2.4 GHz
- Suitable for use from 400 MHz to 2.4 GHz
- Bias Stabilized for Device and Temperature Variations
- Ultra Small SOT-363 Surface Mount Package
- Available Only in Tape and Reel Packaging

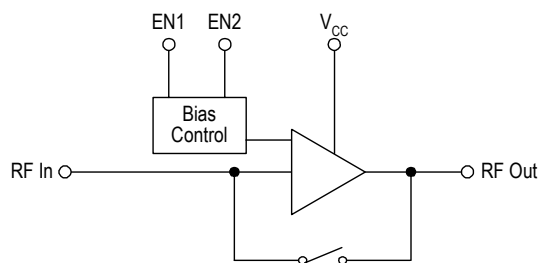


Figure 1. Simplified Block Diagram

1 Specifications

Table 1. Maximum Ratings

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	3.3	V
Storage Temperature Range	T_{stg}	-65 to 150	°C
Operating Ambient Temperature Range	T_A	-30 to 85	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables.
 2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤ 550 V and Machine Model (MM) ≤ 50 V. Additional EST data available upon request.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{CC}	2.5	2.7	3.0	V
Frequency Range	f_{RF}	400	-	2400	MHz

Table 3. Electrical Characteristics ($V_{CC} = 2.75$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Consumption	I_{CC}				
Low IP3		-	5.0	-	mA
High IP3		-	11	-	mA
Bypass		-	0	-	μA
Input/Output Return Loss	RL				dB
Low IP3		-	10	-	
High IP3		-	10	-	
Bypass		-	12	-	

Table 3. Electrical Characteristics (Continued) ($V_{CC} = 2.75$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Min	Typ	Max	Unit
RF Gain (900 MHz)	G				dB
Low IP3		-	20	-	
High IP3		-	21	-	
Bypass		-	-2.9	-	
RF Gain (1.9 GHz)	G				dB
Low IP3		-	13	-	
High IP3		-	14.5	-	
Bypass		-	-2.5	-	
RF Gain (2.4 GHz)	G				dB
Low IP3		-	11.5	-	
High IP3		-	12	-	
Bypass		-	-2.8	-	
Noise Figure	NF				dB
900 MHz		-	1.2	-	
1.9 GHz		-	1.38	-	
2.4 GHz		-	1.55	-	
Input IP3 (900 MHz)	IIP3				dBm
Low IP3		-	-3.5	-	
High IP3		-	10	-	
Bypass		-	27	-	
Input IP3 (1.9 GHz)	IIP3				dBm
Low IP3		-	4.0	-	
High IP3		-	10	-	
Bypass		-	29	-	
Input IP3 (2.4 GHz)	IIP3				dBm
Low IP3		-	6.0	-	
High IP3		-	13	-	
Bypass		-	25	-	
Output 1dB Compression (900 MHz)	P_{1dB}				dBm
Low IP3		-	12	-	
High IP3		-	11.5	-	
Bypass		-	5.0	-	
Output 1db Compression (1.9 GHz)	P_{1dB}				dBm
Low IP3		-	11	-	
High IP3		-	11.5	-	
Bypass		-	5.0	-	
Output 1dB Compression (2.4 GHz)	P_{1dB}				dBm
Low IP3		-	14	-	
High IP3		-	14	-	
Bypass		-	5.0	-	
Reverse Isolation	IS_{12}				dB
Low IP3		-	25	-	
High IP3		-	20	-	

Table 4. Truth Table

EN1	EN2	State	Current Consumption
0	0	Standby	< 20 μ A
0	1	Bypass	0 μ A
1	0	High IP3	11 mA (approx.)
1	1	Low IP3	5.0 mA (approx.)

NOTE: Logic state of "1" equals V_{CC} voltage. Logic state of "0" equals ground potential.

Table 5. Low IP3 Mode Scattering Parameters ($V_{CC} = 2.7\text{ V}$, EN1 = High, EN2 = High)

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₁₁	∠φ	S ₁₁	∠φ	S ₁₁	∠φ
100	0.811	-7	11.939	168	0.010	39	0.890	-5
200	0.787	-14	11.375	157	0.015	55	0.875	-9
300	0.756	-20	10.789	148	0.021	61	0.853	-12
400	0.706	-24	9.892	138	0.026	65	0.819	-15
500	0.673	-28	8.949	131	0.031	68	0.796	-17
600	0.636	-31	8.293	125	0.036	69	0.772	-19
700	0.602	-34	7.590	119	0.040	70	0.750	-21
800	0.575	-36	6.987	114	0.045	72	0.732	-22
900	0.553	-38	6.457	109	0.050	73	0.716	-24
1000	0.531	-39	5.972	105	0.055	74	0.702	-25
1100	0.514	-40	5.566	101	0.060	75	0.690	-26
1200	0.500	-42	5.218	98	0.065	76	0.680	-27
1300	0.488	-43	4.884	95	0.070	77	0.671	-28
1400	0.477	-44	4.629	92	0.075	77	0.664	-29
1500	0.469	-45	4.373	89	0.081	78	0.657	-30
1600	0.458	-46	4.136	87	0.087	79	0.651	-31
1700	0.455	-47	3.938	84	0.093	79	0.645	-32
1800	0.450	-48	3.762	82	0.099	80	0.641	-33
1900	0.445	-49	3.614	80	0.105	80	0.636	-34
2000	0.442	-50	3.479	78	0.112	81	0.631	-35
2100	0.440	-51	3.352	76	0.119	81	0.625	-37
2200	0.438	-52	3.223	74	0.126	82	0.621	-38
2300	0.440	-53	3.127	72	0.135	82	0.619	-39
2400	0.440	-55	3.044	70	0.144	82	0.615	-41
2500	0.443	-57	2.966	68	0.154	82	0.610	-43
2600	0.446	-59	2.886	66	0.165	83	0.603	-45
2800	0.447	-64	2.778	62	0.189	83	0.589	-50
3000	0.458	-71	2.691	58	0.221	82	0.570	-56

Table 6. High IP3 Mode Scattering Parameters ($V_{CC} = 2.7$ V, EN1 = High, EN2 = Low)

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₁₁	∠φ	S ₁₁	∠φ	S ₁₁	∠φ
100	0.661	-8	21.189	161	0.010	36	0.829	-6
200	0.629	-14	18.913	146	0.014	54	0.801	-10
300	0.583	-20	16.730	134	0.019	61	0.764	-14
400	0.544	-21	14.168	123	0.024	67	0.726	-15
500	0.526	-23	12.141	116	0.029	71	0.709	-16
600	0.502	-25	10.757	111	0.034	73	0.690	-17
700	0.486	-26	9.523	106	0.039	75	0.676	-18
800	0.473	-27	8.531	101	0.044	76	0.665	-19
900	0.464	-28	7.725	98	0.050	77	0.656	-20
1000	0.457	-29	7.028	94	0.056	78	0.650	-21
1100	0.450	-30	6.461	92	0.061	79	0.643	-22
1200	0.446	-31	5.990	89	0.067	79	0.639	-23
1300	0.445	-32	5.551	86	0.073	80	0.634	-24
1400	0.443	-33	5.226	84	0.079	80	0.632	-25
1500	0.440	-35	4.903	82	0.085	80	0.628	-26
1600	0.437	-35	4.611	80	0.091	80	0.626	-27
1700	0.439	-37	4.370	78	0.097	80	0.623	-28
1800	0.439	-38	4.160	76	0.103	81	0.622	-29
1900	0.437	-40	3.981	74	0.111	81	0.618	-31
2000	0.440	-41	3.822	73	0.117	81	0.617	-32
2100	0.439	-42	3.675	71	0.124	81	0.613	-34
2200	0.443	-44	3.530	69	0.132	81	0.612	-35
2300	0.444	-45	3.416	68	0.140	82	0.611	-37
2400	0.448	-48	3.322	66	0.149	82	0.608	-38
2500	0.452	-50	3.236	64	0.159	81	0.605	-41
2600	0.456	-52	3.151	63	0.169	82	0.600	-43
2800	0.460	-57	3.032	59	0.193	81	0.589	-48
3000	0.472	-65	2.943	55	0.223	80	0.573	-54

Table 7. Bypass Mode Scattering Parameters ($V_{CC} = 2.7$ V, EN1 = Low, EN2 = High)

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₁₁	∠φ	S ₁₁	∠φ	S ₁₁	∠φ
100	0.958	-11	0.115	79	0.116	80	0.950	-8
200	0.921	-21	0.222	70	0.224	70	0.925	-16
300	0.881	-30	0.318	61	0.319	61	0.889	-23
400	0.832	-38	0.399	53	0.396	53	0.849	-29
500	0.786	-45	0.457	45	0.462	46	0.806	-35
600	0.737	-52	0.515	39	0.513	39	0.764	-41
700	0.693	-57	0.552	33	0.553	33	0.724	-45
800	0.654	-63	0.585	28	0.584	28	0.689	-49
900	0.618	-67	0.610	23	0.609	23	0.655	-53
1000	0.587	-72	0.626	19	0.627	19	0.626	-57
1100	0.561	-76	0.642	16	0.643	15	0.598	-61
1200	0.533	-80	0.655	12	0.654	12	0.573	-64
1300	0.514	-83	0.660	9.0	0.663	8	0.549	-67
1400	0.493	-87	0.673	6.0	0.669	5	0.527	-71
1500	0.478	-90	0.672	2.0	0.673	2	0.506	-74
1600	0.461	-93	0.674	-1.0	0.676	-1	0.486	-78
1700	0.449	-96	0.675	-4.0	0.677	-4	0.468	-82
1800	0.435	-99	0.673	-7.0	0.675	-6	0.448	-85
1900	0.427	-102	0.671	-9.0	0.673	-9	0.431	-89
2000	0.421	-104	0.668	-11	0.670	-11	0.413	-93
2100	0.412	-107	0.663	-14	0.664	-14	0.397	-98
2200	0.407	-110	0.655	-16	0.658	-16	0.380	-103
2300	0.401	-114	0.647	-19	0.648	-19	0.364	-109
2400	0.396	-117	0.634	-21	0.638	-21	0.347	-115
2500	0.396	-121	0.622	-23	0.623	-23	0.335	-122
2600	0.396	-124	0.608	-25	0.609	-26	0.319	-130
2800	0.393	-132	0.569	-29	0.571	-29	0.294	-147
3000	0.397	-142	0.527	-32	0.528	-32	0.276	-167

Table 8. Standby Mode Scattering Parameters ($V_{CC} = 2.7\text{ V}$, EN1 = Low, EN2 = Low)

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₁₁	∠φ	S ₁₁	∠φ	S ₁₁	∠φ
100	0.963	-4	0.010	35	0.010	43	0.951	-3
200	0.953	-7	0.014	61	0.016	61	0.948	-4
300	0.949	-10	0.022	71	0.022	68	0.947	-6
400	0.945	-13	0.029	76	0.029	72	0.945	-8
500	0.943	-16	0.036	75	0.036	74	0.944	-10
600	0.937	-19	0.043	70	0.043	74	0.941	-12
700	0.932	-21	0.050	76	0.049	74	0.938	-15
800	0.926	-24	0.054	74	0.056	74	0.935	-16
900	0.920	-27	0.062	75	0.063	73	0.932	-19
1000	0.914	-30	0.069	72	0.069	73	0.928	-21
1100	0.911	-33	0.075	72	0.075	72	0.923	-23
1200	0.903	-36	0.082	71	0.081	71	0.919	-25
1300	0.897	-38	0.086	72	0.087	70	0.913	-27
1400	0.892	-41	0.094	69	0.092	70	0.908	-29
1500	0.885	-44	0.097	69	0.097	69	0.902	-31
1600	0.877	-47	0.101	68	0.102	69	0.894	-33
1700	0.874	-50	0.104	68	0.106	69	0.887	-35
1800	0.861	-52	0.109	69	0.110	69	0.878	-37
1900	0.855	-55	0.115	69	0.115	69	0.868	-39
2000	0.850	-58	0.120	69	0.118	69	0.857	-42
2100	0.841	-61	0.120	70	0.122	70	0.845	-44
2200	0.831	-64	0.127	71	0.126	71	0.832	-46
2300	0.821	-67	0.132	72	0.132	73	0.816	-49
2400	0.808	-70	0.138	74	0.138	74	0.798	-52
2500	0.797	-73	0.146	75	0.146	76	0.776	-55
2600	0.784	-76	0.155	79	0.156	78	0.751	-58
2800	0.751	-82	0.183	80	0.184	81	0.688	-64
3000	0.720	-89	0.222	82	0.225	81	0.609	-70

2 Application Information

The MBC13720 SiGe:C LNA is designed for applications in the 400 MHz to 2.4 GHz range. It has four different modes; Low IP3, High IP3, Bypass, and Standby. The IC is programmable through the Enable 1 and 2 pins. In Low IP3 mode, the current consumption is optimized. Current consumption is higher in High IP3 mode to boost the intercept point performance. The gain difference between Low IP3 and High IP3 modes is typically 1.0 dB and typically the Low IP3 mode has a slightly better noise figure performance.

The internal bypass switch is designed for broadband applications. One of the advantages of the MBC13720 is the simplification of matching network in both bypass and amplifier modes. The bypass switch is designed such that the changes of input and output return losses between bypass mode and amplifier mode is minimized. As a result, the mismatch at the LNA input and output is minimized and therefore, the matching network design is simplified as well.

In the design of the external matching network, conjugate match condition does not necessarily provide the best noise figure performance. Balancing between noise figure, gain, and intercept point is the major design consideration. Typical circuits are provided in Figures 2 and 3 for 1.9 GHz, 2.4 GHz and 900 MHz applications.

In Figure 2, it shows the typical application circuit at 1.9 and 2.4 GHz. The noise figure, input intercept point, gain, and return losses are optimized. L2 and C2 act as a low frequency trap to improve the input intercept point. The noise figure measured on this board is 1.4 dB (in Low IP3 mode) at 1.9 GHz, including the external components, connectors, and PC board. The input third order intercept point is 10 dBm (in High IP3 mode).

In Figure 3, the typical application circuit at 900 MHz is shown. The input low frequency trap again is used to maximize the input intercept point. It has moderate IP3 performance and high gain. For higher IP3, Figure 4 shows the application circuit with feedback network. Capacitive feedback method is used to reduce the gain and therefore increase the 3rd order input intercept point. The feedback circuit is designed to provide unconditional stability.

The corresponding PCBs are shown in Figures 5 through 10. Typical characteristics of the application boards are shown in Table 9.

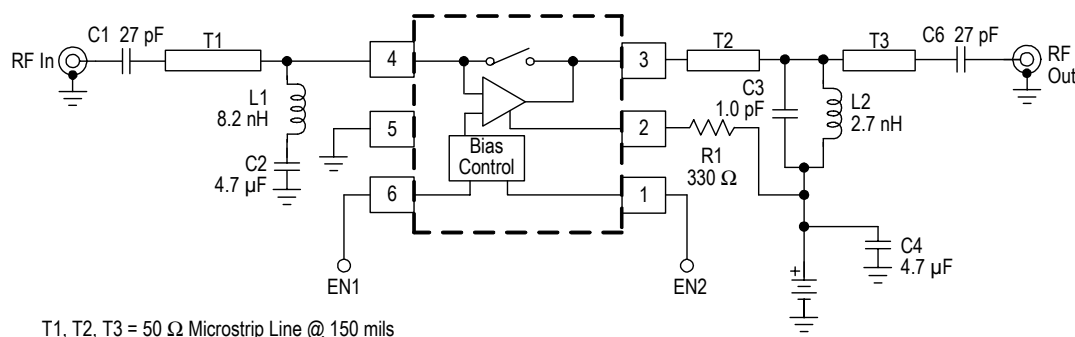


Figure 2. Typical 1.9 and 2.4 GHz LNA Application Schematic

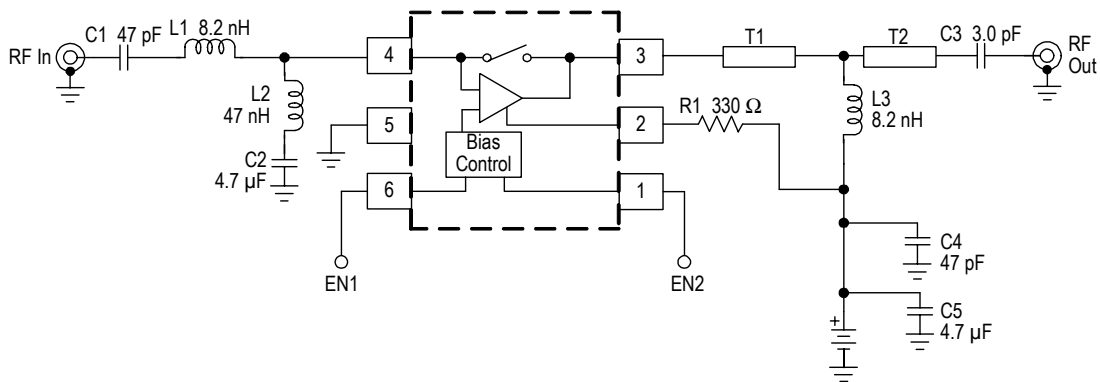


Figure 3. Typical 900 MHz LNA Application Schematic

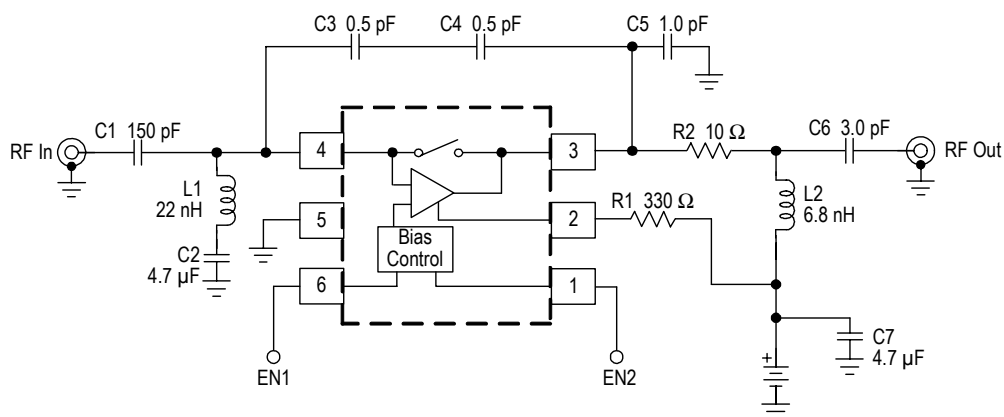


Figure 4. High IP3 900 MHz LNA Application Schematic

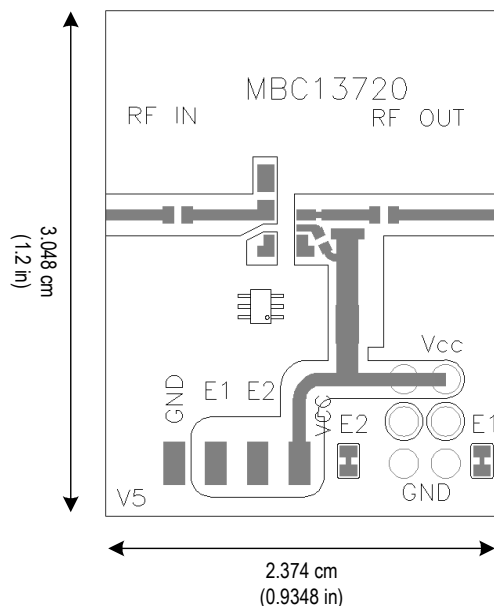


Figure 5. 1.9/2.4 GHz PCB

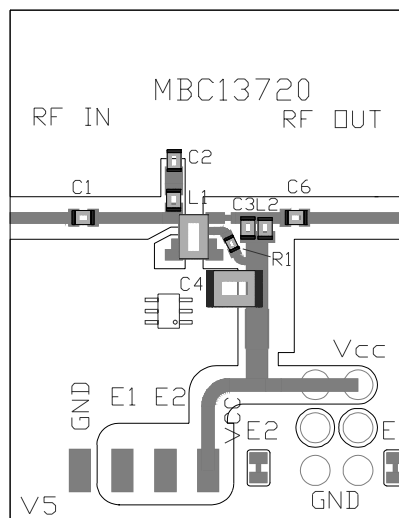


Figure 6. 1.9/2.4 GHz Assembly Diagram

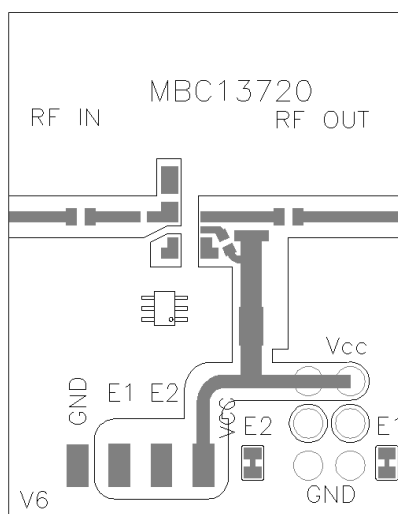


Figure 7. 900 MHz PCB

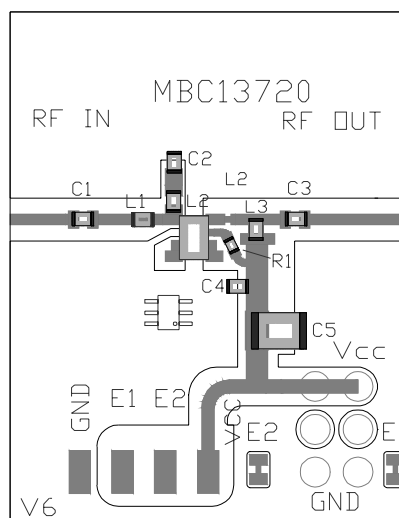


Figure 8. 900 MHz Assembly Diagram

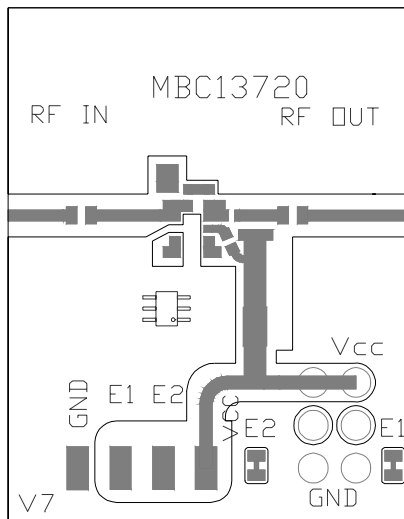


Figure 9. 900 MHz Capacitive Feedback PCB

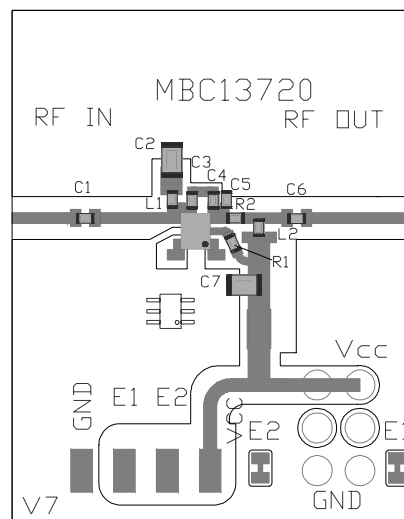


Figure 10. 900 MHz Capacitive Feedback Assembly Diagram

Table 9. Typical Electrical Characteristics of the Application Schematic

Mode	Symbol	High IP3	Low IP3	Bypass	Standby	Unit
------	--------	----------	---------	--------	---------	------

900 MHz TYPICAL (See Figure 3)

Gain	G	21	20	-2.9	-22	dB
Noise Figure	NF	1.3	1.2	2.9	-	dB
Input Intermodulation Intercept Point	IIP3	2.0	-3.0	29	-	dBm
Output Intermodulation Intercept Point	OIP3	23	17	26	-	dBm
Output 1dB Compression Point	P _{1dB}	11.5	10.5	5.0	-	dBm
Input Return Loss	IS ₁₁ ²	11	10	12	-	dB
Output Return Loss	IS ₂₂ ²	11	10	15	-	dB
Reverse Isolation	IS ₁₂ ²	25	24	2.9	22	dB

900 MHz HIGH IP3 (See Figure 4)

Gain	G	16	15	-4.0	-14.5	dB
Noise Figure	NF	1.4	1.3	4.0	-	dB
Input Intermodulation Intercept Point	IIP3	10	3.5	27	-	dBm
Output Intermodulation Intercept Point	OIP3	26	18.5	23	-	dBm
Output 1dB Compression Point	P _{1dB}	11.5	12	7.0	-	dBm
Input Return Loss	IS ₁₁ ²	12	11	8.0	-	dB
Output Return Loss	IS ₂₂ ²	12	12	14	-	dB
Reverse Isolation	IS ₁₂ ²	22	20	4.0	14.5	dB

1.9 GHz (See Figure 2)

Gain	G	14	13	-2.5	-16	dB
Noise Figure	NF	1.5	1.4	2.5	-	dB
Input Intermodulation Intercept Point	IIP3	10	4.0	29	-	dBm
Output Intermodulation Intercept Point	OIP3	24.4	17	26.5	-	dBm
Output 1dB Compression Point	P _{1dB}	11.5	11	5.0	-	dBm
Input Return Loss	IS ₁₁ ²	10	8.0	20	-	dB
Output Return Loss	IS ₂₂ ²	8.0	7.0	30	-	dB
Reverse Isolation	IS ₁₂ ²	19	19	2.5	16	dB

Table 9. Typical Electrical Characteristics of the Application Schematic (Continued)

Mode	Symbol	High IP3	Low IP3	Bypass	Standby	Unit
2.4 GHz (See Figure 2)						
Gain	G	12	11	-2.8	-15	dB
Noise Figure	NF	1.7	1.65	2.8	-	dB
Input Intermodulation Intercept Point	IIP3	13	6.0	25	-	dBm
Output Intermodulation Intercept Point	OIP3	25	17.5	22	-	dBm
Output 1dB Compression Point	P _{1dB}	14	14	5.0	-	dBm
Input Return Loss	S ₁₁ ²	12	10	12	-	dB
Output Return Loss	S ₂₂ ²	8.0	7.0	14	-	dB
Reverse Isolation	S ₁₂ ²	17	17	2.8	15	dB

Technical Data

MBC13916/D
Rev. 0, mm/2002

General Purpose
SiGe:C RF Cascode
Amplifier



MOTOROLA
intelligence everywhere™

digital dna™

MBC13916



(Scale 2:1)

Package Information

Plastic Package

Case 1404

(SOT-343R)

Ordering Information

Device	Device Marking	Package
MBC13916T1	916	SOT-343R

The MBC13916 is a cost-effective, high isolation amplifier fabricated with Motorola's Advanced RF BiCMOS process using the SiGe:C module. It is intended to be a similar replacement for the MRFIC0916 and is housed in the smaller SOT-343R surface mount package. As with the MRFIC0916, the device is designed for general purpose RF applications, but has improved high frequency gain and noise figure. On-chip bias circuitry sets the bias point, while matching is accomplished off-chip, affording the maximum in application flexibility.

- Usable Frequency Range = 100 to 2500 MHz
- 19 dB typical gain at 900 MHz, $V_{CC} = 2.7$ V
- NF_{min} (Device Level) = 0.9 dB @ 900 MHz
- NF_{min} (Device Level) = 1.9 dB @ 1.9 GHz
- 2.5 dBm typical Output Power at 1.0 dB Gain Compression at 900 MHz, $V_{CC} = 2.7$ V
- 45 dB Typical Reverse Isolation (Device Level) at 900 MHz, $V_{CC} = 2.7$ V
- 4.7 mA Typ Bias Current at $V_{CC} = 2.7$ V
- 2.7 to 5.0 V Supply
- Industry Standard SOT-343R Package
- Available Only in Tape and Reel Packaging
- Device Weight = 0.00642 g (Typ)

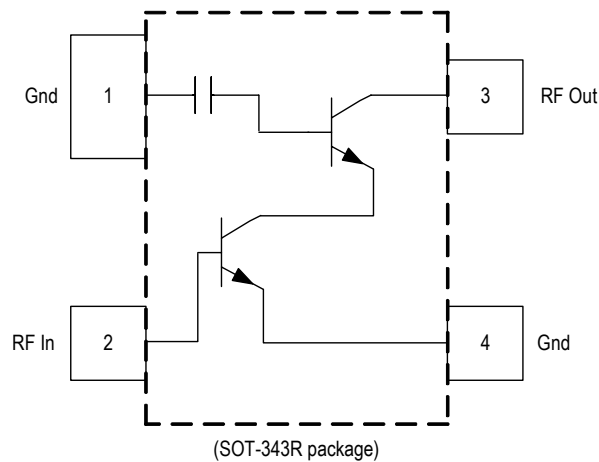


Figure 1. Functional Block Diagram

Table 1. Maximum Ratings

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	Vdc
RF Input Power	P_{RF}	10	dBm
Power Dissipation	P_{DIS}	100	mW
Supply Current	I_{CC}	20	mA
Thermal Resistance, Junction to Case	$R_{\theta JC}$	400	C/W
Storage Temperature Range	T_{stg}	-65 to 150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Conditions and Electrical Characteristics tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤ 550 V and Machine Model (MM) ≤ 50 V. Additional ESD data available upon request.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
RF Frequency	f_{RF}	100	-	2500	MHz
Supply Voltage	V_{CC}	2.7	-	5.0	Vdc

Table 3. Device Level Characteristics

($V_{CC} = 2.7$ V, $T_A = 25^\circ\text{C}$, measured in S-parameter test fixture, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Insertion Gain $f = 900$ MHz $f = 1900$ MHz	$ S_{21} ^2$	- -	16.5 10	- -	dB
Maximum Stable Gain and/or Minimum Available Gain [Note 1] $f = 900$ MHz $f = 1900$ MHz	MSG, MAG	- -	24.5 14.3	- -	dB

Freescale Semiconductor, Inc.

Table 3. Device Level Characteristics (Continued)

($V_{CC} = 2.7$ V, $T_A = 25^\circ\text{C}$, measured in S-parameter test fixture, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Minimum Noise Figure [Note 2] f = 900 MHz f = 1900 MHz	NF_{min}	- -	0.9 1.9	- -	dB
Output Third Order Intercept Point [Note 3] f = 900 MHz f = 1900 MHz	OIP3	- -	16.5 17	- -	dBm
Reverse Isolation f = 900 MHz f = 1900 MHz	$ S_{12} ^2$	- -	-45 -31	- -	dB

NOTES: 1. Maximum Available Gain and Maximum Stable Gain are defined by the K factor as follows:

$$MAG = \left| \frac{S_{21}}{S_{12}} (K \pm \sqrt{K^2 - 1}) \right|, \text{ if } K > 1, \text{ MSG} = \left| \frac{S_{21}}{S_{12}} \right|, \text{ if } K < 1$$

2. Device matched for best noise figure.
3. Z_{out} matched for optimum IP3.

($V_{CC} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$, $f_{RF} = 900\text{ MHz}$, Tested in Circuit Shown in Figure 2, unless otherwise noted.)

3.05 cm
(1.2 in)

Gnd V_{cc} Gnd

MOTOROLA

RF IN

1 2 3 4

RF OUT

MBC13916 SOT343

RF CASCODE AMPLIFIER

V₂

1.9 cm
(0.75 in)

NOTE:
PCB material FR4
 $\epsilon_r = 4.5$
 $h = 25$ mils
 $t = 1.75$

MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

Table 5. Electrical Characteristics

($V_{CC} = 2.7$ V, $T_A = 25^\circ\text{C}$, $f_{RF} = 1.9$ GHz, Tested in Circuit Shown in Figure 4, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Small Signal Gain	S_{21}	9.5	11.5	13.5	dB
Noise Figure	NF	-	2.1	-	dB
Power Output at 1.0 dB Gain Compression	P_{1dB}	-	-4.0	-	dBm
Output 3rd Order Intercept Point	OIP3	-	5.5	-	dBm
Reverse Isolation	S_{12}	-	-28	-	dB
Supply Current	I_{CC}	3.8	4.7	5.6	mA

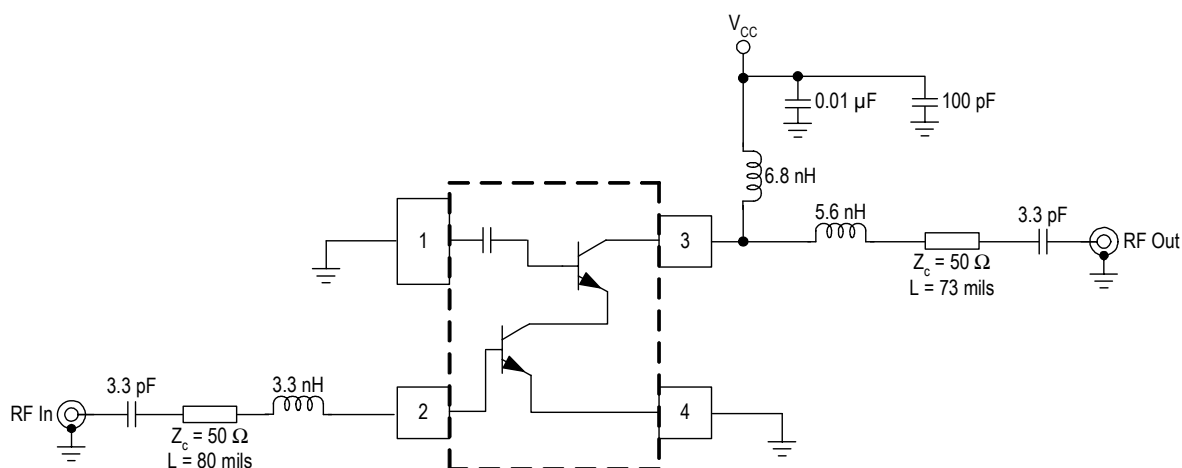


Figure 4. 1.9 GHz Application Configuration Circuit

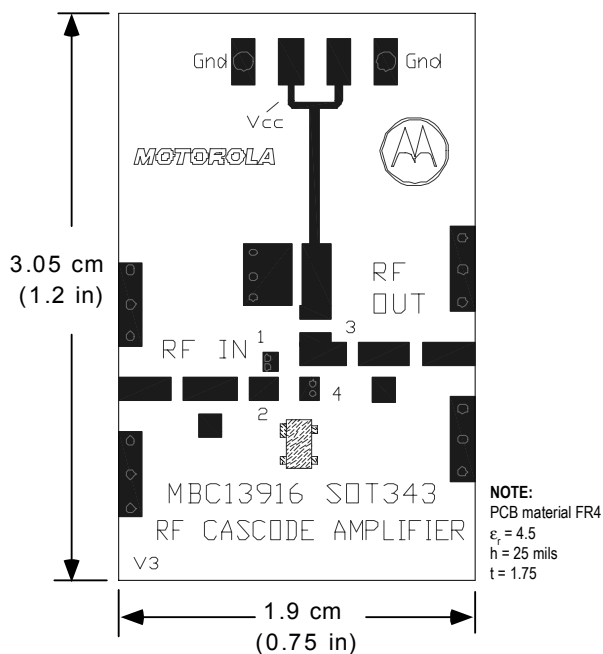


Figure 5. 1.9 GHz Printed Circuit Board

Freescale Semiconductor, Inc.

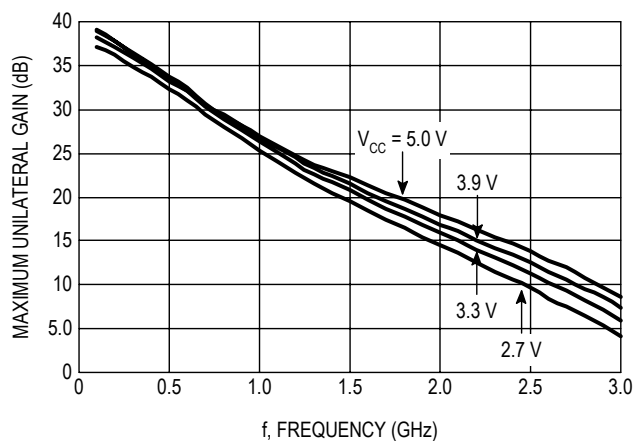


Figure 6. Gmax versus Frequency

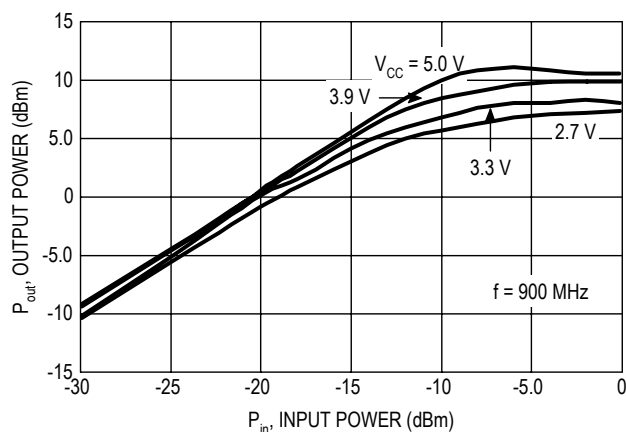


Figure 7. Output Power versus Input Power

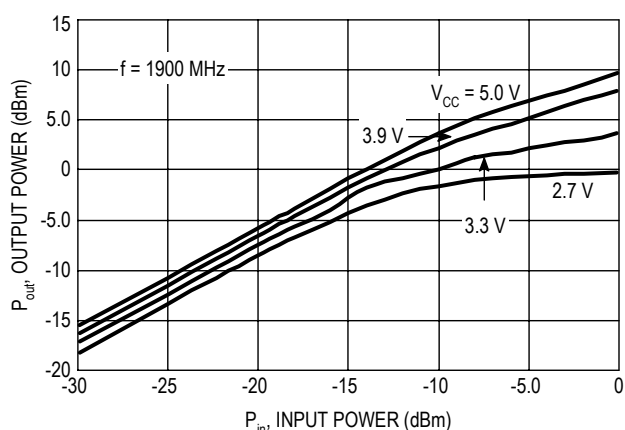


Figure 8. Output Power versus Input Power

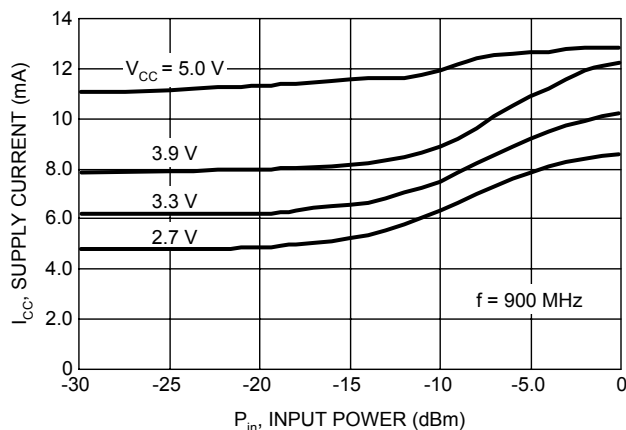


Figure 9. Supply Current versus Input Power

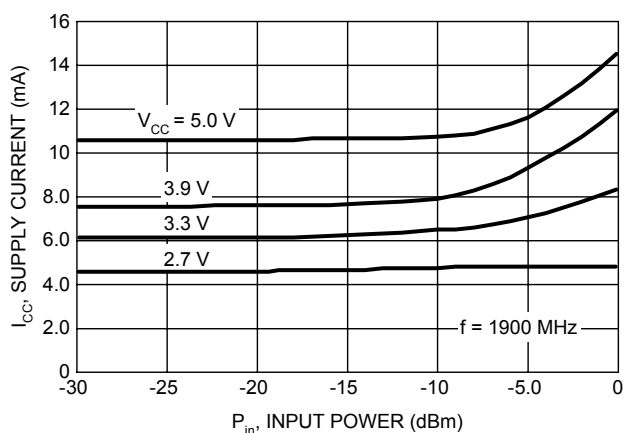


Figure 10. Supply Current versus Input Power

Table 6. Scattering Parameters

($V_{CC} = 2.7\text{ V}$, $50\ \Omega$ System)

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	$\angle \phi$	S ₂₁	$\angle \phi$	S ₁₂	$\angle \phi$	S ₂₂	$\angle \phi$
100	0.829	-11	11.98	165	0.001	17	0.955	-4
200	0.798	-21	11.43	152	0.002	47	0.957	-7
300	0.753	-31	10.69	139	0.002	55	0.956	-11
400	0.701	-39	10.12	128	0.003	56	0.955	-14
500	0.648	-46	9.28	118	0.003	51	0.955	-18
600	0.599	-53	8.66	108	0.004	49	0.954	-22
700	0.554	-58	7.95	98	0.004	41	0.947	-26
800	0.518	-61	7.33	90	0.004	24	0.941	-30
900	0.485	-65	6.83	82	0.004	15	0.933	-34
1000	0.458	-67	6.23	74	0.004	-4	0.926	-38
1100	0.438	-69	5.78	67	0.004	-28	0.915	-43
1200	0.426	-71	5.39	60	0.005	-50	0.902	-46
1300	0.417	-72	4.97	52	0.006	-74	0.893	-51
1400	0.414	-73	4.59	46	0.008	-93	0.879	-54
1500	0.415	-74	4.31	39	0.011	-106	0.868	-58
1600	0.421	-75	3.99	32	0.014	-115	0.851	-62
1700	0.430	-76	3.66	25	0.018	-125	0.835	-66
1800	0.441	-78	3.43	19	0.022	-131	0.818	-70
1900	0.455	-80	3.16	12	0.027	-139	0.803	-73
2000	0.474	-82	2.93	5	0.033	-146	0.777	-77
2100	0.490	-85	2.70	-1	0.039	-152	0.761	-81
2200	0.504	-88	2.48	-8	0.045	-159	0.735	-85
2300	0.524	-92	2.27	-14	0.052	-163	0.707	-89
2400	0.542	-95	2.09	-21	0.059	-169	0.683	-93
2500	0.559	-98	1.90	-28	0.067	-175	0.651	-98
2600	0.572	-103	1.70	-34	0.075	180	0.624	-102
2700	0.587	-106	1.56	-40	0.083	174	0.593	-107
2800	0.603	-110	1.40	-48	0.091	169	0.562	-111
2900	0.610	-114	1.26	-55	0.098	163	0.533	-116
3000	0.613	-118	1.11	-60	0.105	160	0.501	-120

Table 7. Scattering Parameters

(V_{CC} = 3.0 V, 50 Ω System)

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
100	0.812	-11	13.42	165	0.001	11	0.954	-3
200	0.778	-21	12.73	151	0.001	50	0.955	-7
300	0.731	-30	11.82	138	0.002	58	0.956	-11
400	0.677	-38	11.10	127	0.003	50	0.954	-14
500	0.623	-44	10.12	116	0.003	51	0.954	-18
600	0.575	-50	9.37	107	0.003	43	0.952	-22
700	0.533	-54	8.56	98	0.003	30	0.945	-26
800	0.499	-57	7.85	90	0.004	24	0.937	-30
900	0.470	-59	7.29	82	0.004	8	0.930	-34
1000	0.448	-61	6.63	74	0.003	-11	0.923	-38
1100	0.433	-63	6.14	67	0.004	-38	0.911	-42
1200	0.423	-64	5.72	60	0.005	-58	0.900	-46
1300	0.418	-65	5.27	53	0.006	-77	0.891	-50
1400	0.421	-66	4.87	47	0.008	-96	0.878	-54
1500	0.425	-67	4.56	40	0.011	-108	0.868	-58
1600	0.432	-68	4.23	34	0.014	-120	0.852	-61
1700	0.444	-70	3.89	27	0.018	-126	0.838	-65
1800	0.459	-72	3.63	21	0.022	-133	0.822	-69
1900	0.473	-74	3.35	15	0.027	-140	0.809	-73
2000	0.490	-77	3.12	8	0.033	-147	0.784	-77
2100	0.509	-80	2.87	2	0.039	-152	0.769	-80
2200	0.527	-83	2.64	-5	0.045	-159	0.744	-84
2300	0.545	-86	2.42	-11	0.051	-163	0.717	-88
2400	0.560	-90	2.23	-17	0.059	-170	0.694	-92
2500	0.579	-94	2.03	-24	0.067	-175	0.663	-97
2600	0.594	-98	1.82	-30	0.075	-180	0.637	-101
2700	0.606	-101	1.68	-36	0.083	175	0.607	-105
2800	0.620	-105	1.50	-43	0.090	169	0.576	-110
2900	0.630	-110	1.35	-50	0.097	164	0.548	-114
3000	0.636	-113	1.19	-55	0.105	160	0.516	-119

Table 8. Scattering Parameters

($V_{CC} = 3.9\text{ V}$, $50\ \Omega$ System)

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₂₁	∠φ	S ₁₂	∠φ	S ₂₂	∠φ
100	0.796	-11	14.82	164	0.001	25	0.954	-3
200	0.760	-20	13.98	150	0.001	50	0.955	-7
300	0.711	-29	12.90	137	0.002	46	0.955	-11
400	0.655	-36	12.03	126	0.002	55	0.955	-14
500	0.602	-42	10.90	115	0.003	50	0.954	-18
600	0.556	-46	10.04	106	0.003	45	0.954	-22
700	0.517	-50	9.12	97	0.003	34	0.947	-26
800	0.487	-52	8.34	89	0.003	22	0.940	-30
900	0.463	-54	7.72	82	0.003	11	0.933	-34
1000	0.444	-56	7.02	74	0.003	-6	0.927	-38
1100	0.432	-57	6.49	67	0.003	-40	0.917	-42
1200	0.428	-58	6.03	61	0.005	-69	0.905	-46
1300	0.427	-59	5.55	53	0.006	-88	0.896	-50
1400	0.430	-60	5.13	48	0.008	-99	0.883	-53
1500	0.437	-61	4.81	41	0.011	-111	0.874	-57
1600	0.449	-62	4.45	35	0.014	-118	0.858	-61
1700	0.462	-64	4.09	29	0.018	-128	0.843	-64
1800	0.475	-66	3.83	23	0.022	-134	0.829	-68
1900	0.493	-69	3.53	17	0.027	-140	0.815	-72
2000	0.512	-72	3.28	10	0.032	-148	0.790	-76
2100	0.529	-75	3.03	4	0.038	-152	0.776	-79
2200	0.544	-78	2.79	-2	0.045	-159	0.752	-83
2300	0.565	-82	2.56	-8	0.051	-164	0.726	-87
2400	0.583	-85	2.37	-14	0.058	-169	0.704	-91
2500	0.599	-89	2.16	-21	0.067	-175	0.674	-96
2600	0.613	-93	1.94	-27	0.075	-179	0.648	-100
2700	0.629	-97	1.79	-32	0.083	175	0.621	-105
2800	0.643	-101	1.60	-39	0.091	170	0.589	-109
2900	0.650	-105	1.44	-46	0.098	164	0.562	-114
3000	0.653	-109	1.28	-51	0.105	160	0.531	-118

Table 9. Scattering Parameters

(V_{CC} = 5.0 V, 50 Ω System)

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
100	0.719	-9	21.47	161	0.001	5	0.939	-3
200	0.678	-17	19.60	145	0.001	18	0.939	-7
300	0.628	-23	17.43	132	0.001	38	0.940	-10
400	0.579	-27	15.66	120	0.002	47	0.937	-14
500	0.540	-30	13.78	110	0.002	38	0.936	-18
600	0.512	-32	12.40	101	0.003	37	0.934	-22
700	0.492	-34	11.05	93	0.002	32	0.927	-26
800	0.480	-34	9.97	86	0.002	9	0.920	-30
900	0.472	-35	9.12	79	0.002	-14	0.914	-34
1000	0.470	-37	8.21	73	0.002	-54	0.908	-38
1100	0.473	-37	7.54	67	0.003	-75	0.899	-42
1200	0.478	-39	6.97	61	0.004	-90	0.890	-46
1300	0.484	-40	6.37	54	0.006	-101	0.884	-50
1400	0.496	-42	5.86	50	0.008	-114	0.875	-54
1500	0.509	-44	5.49	44	0.010	-120	0.871	-57
1600	0.521	-46	5.08	39	0.013	-128	0.858	-60
1700	0.535	-49	4.67	34	0.017	-133	0.848	-63
1800	0.552	-51	4.38	29	0.021	-139	0.838	-67
1900	0.570	-54	4.06	23	0.025	-144	0.829	-70
2000	0.587	-56	3.80	18	0.030	-150	0.807	-73
2100	0.604	-60	3.54	13	0.036	-154	0.795	-76
2200	0.621	-63	3.28	7	0.042	-160	0.772	-79
2300	0.643	-67	3.04	2	0.048	-164	0.746	-83
2400	0.658	-70	2.84	-4	0.056	-169	0.722	-87
2500	0.673	-74	2.61	-10	0.063	-175	0.687	-91
2600	0.690	-78	2.36	-16	0.071	-179	0.657	-96
2700	0.705	-82	2.19	-21	0.079	176	0.623	-101
2800	0.715	-86	1.97	-27	0.088	170	0.588	-107
2900	0.720	-91	1.78	-33	0.094	164	0.556	-113
3000	0.723	-94	1.57	-38	0.101	161	0.523	-119

Technical Data Sheet

MC13751/D
Rev. 1, 10/2002

Dual-Band Upmixer and
Driver Amplifier



MOTOROLA
intelligence everywhere™

digital dna™

MC13751



Package Information

Plastic Package
Case 1307
(QFN-24)

Ordering Information

Device	Device Marking	Package
MC13751FC	MC751	QFN-24

The MC13751 is an integrated transmit upmixer and driver amplifier designed for use in cellular phones. It includes two mixers and two RF step attenuators. The device is fabricated using Motorola's Advanced RF BiCMOS process with the SiGe:C option and is housed in a leadless QFN-24 package.

- Total Gain:
22 dB for Low Band
19.5 dB for High Band
- Total Current Consumption = 53 mA (Typ)
- Available in Tape and Reel, 2500 Units per 12 mm, 7 inch Reel

Freescale Semiconductor, Inc.

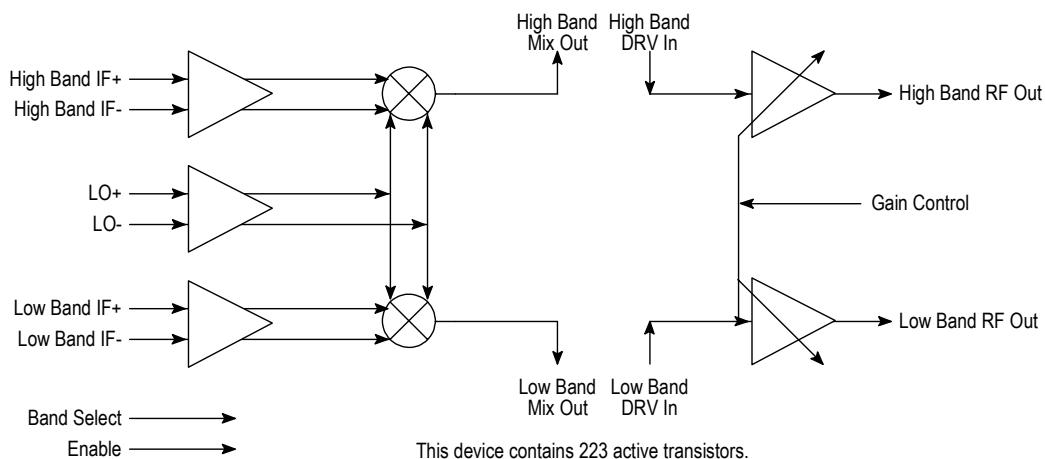


Figure 1. Simplified Block Diagram

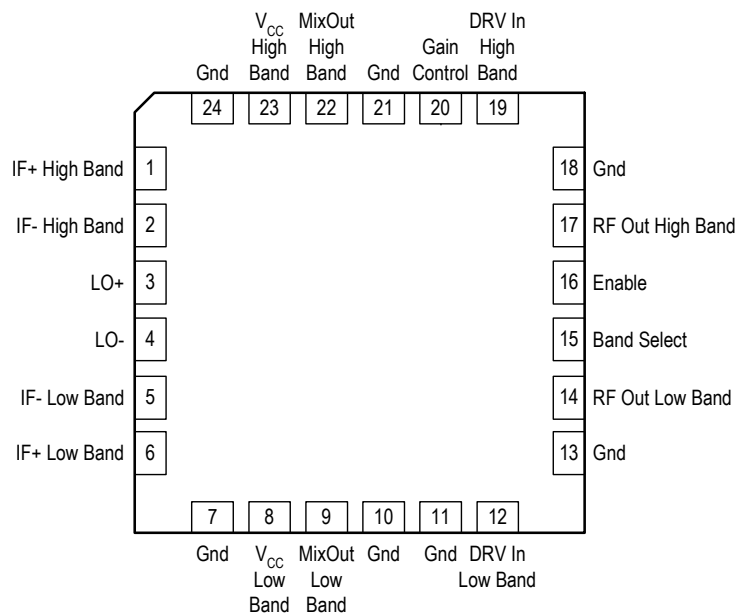


Figure 2. Contact Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	3.6	V
LO Input Power		0	dBm
IF Input Level		0	dBm
Operating Temperature Range	T_A	-30 to 85	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.
 2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤ 250 V and Machine Model (MM) ≤ 25 V. Additional ESD data available upon request.

Table 2. DC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage		2.7	2.78	2.86	V
Power Supply Current		-	53	64	mA
Enable Inactive State Active State		- 1.6	- -	0.6 -	V
Band 800 MHz Enabled 1900 MHz Enabled		- 1.6	- -	0.6 -	V
Power Down State Leakage Current (0.2 V Logic Levels)		-	-	25	μA
Gain Select Voltage Gain High = 1 Gain Low = 0		1.6 -	- -	- 0.6	V
Gain Select (enable and band signals current)		-	-	10	μA

Table 3. Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
IF Frequency Low Band High Band		150 150	178 213	250 250	MHz
LO Frequency Range Low Band High Band		1002 2028	- -	1029 2125	MHz
RF Frequency Range Low Band High Band		824 1850	- -	849 1910	MHz
IF Input Level, Both Bands (differential, typ -7.0 dBm)		-60	-	0	dBm
LO Input Level, Both Bands (differential)		-12	-10	-8.0	dBm
RF GMSK Output Level Both Bands Both Bands, Low Gain		10 6.0	- -	- -	dBm
RF Linear Output Level, TDMA Both Bands Both Bands, Low Gain		6.0 2.0	- -	- -	dBm
ACP @ f ±30 kHz, TDMA @ f ±60 kHz, TDMA @ f ±200 kHz, GSM @ f ±400 kHz, GSM		-32 -51 -36 -66	- - - -	- - - -	dBc

Table 3. Electrical Characteristics (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Conversion Gain Mixer					dBc
Low Band		6.3	8.3	10.3	
High Band		6.5	8.5	10.5	
Gain, Driver, High Gain					dBc
Low Band		11.7	13.7	15.7	
High Band		9.0	11	13	
Gain, Drivers, Low Gain					dBc
Low Band		7.7	9.7	11.7	
High Band		5.0	7.0	9.0	
Noise Figure					dB
Mixer (SSB)		-	11	14	
Drivers		-	5.0	8.0	
IF Impedance (differential)		-	200	-	W
LO Impedance (differential)		-	100	-	W
RF Impedance (Both Bands @ Mixer (rf out, driver rf in and driver rf out))		-	50	-	W

Table 4. Spurious (measured with interstage filter)

Characteristic	Symbol	Min	Typ	Max	Unit
LO Leakage to RF Port (Both bands, $P_{out} = 6.0$ dBm)		-	-	-20	dBc
IF Leakage to RF Port (Both bands)		-	-	-50	dBc
Image Supression (Both bands)		-	-	-20	dBc
2x Image Supression (Both bands)		-	-	-40	dBc
LO - 2x IF (Both bands)		-	-	-30	dBc
2x LO - 7x IF (Low band)		-	-	-40	dBc
5 * IF (Low band)		-	-	-80	dBc
11 * IF (Low band)		-	-	-80	dBc

Product Preview

Order this document
from WBSG Marketing
Rev. 1, 11/2002

W-CDMA LNA and
Downconverter



MOTOROLA
intelligence everywhere™

digital dna™

MC13770



(Scale 2:1)

Package Information

Plastic Package

Case 1345

(QFN-12)

Ordering Information

Device	Device Marking	Package
PC13770FC	PC70	QFN-12

The MC13770 is a LNA Downconverter designed specifically for WCDMA handsets. The LNA is integrated with a bypass switch to preserve input intercept performance. The device is fabricated using Motorola's Advanced RF BiCMOS process using the SiGe:C option and is packaged in a 12 pin Quad Flat Non-leaded package.

- RF Input Frequency: 2110 to 2170 MHz
- LNA Gain = 15 dB (Typ)
- LNA Input 3rd Order Intercept Point (IIP3) = 0 dBm (Typ)
- LNA Noise Figure (NF) = 1.5 dB (Typ)
- Bypass Mode Included for Improved Intercept Point Performance
- Double Balanced Mixer
- Mixer Conversion Gain = 10 dB (Typ)
- Mixer Noise Figure (NF) = 8.0 dB (Typ)
- Mixer Input 3rd Order Intercept Point (IIP3) = -3.0 dBm (Typ)
- Total Supply Current = 8.0 mA
 - LNA = 3.0 mA
 - Mixer = 5.0 mA

Freescale Semiconductor, Inc.

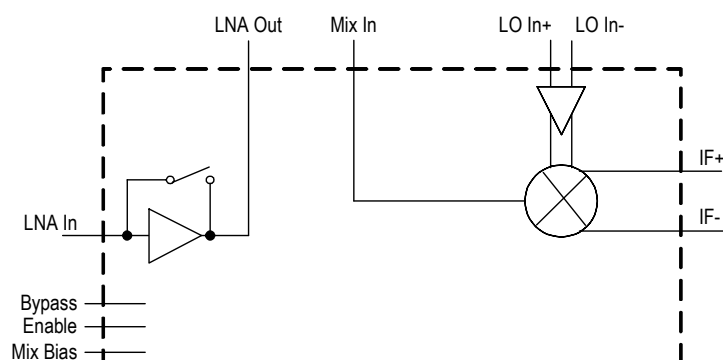


Figure 1. Simplified Block Diagram

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	3.6	V
Storage Temperature Range	T_{stg}	-65 to 150	°C
Operating Temperature Range	T_A	-40 to 85	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage		2.7	2.75	3.0	Vdc
Logic Voltage (Enable and Bypass Pins)					V
Input High Voltage		0.85 V_{CC}	-	V_{CC}	
Input Low Voltage		0	-	0.15 V_{CC}	

Table 3. Target Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Turn-on Time		-	100	-	ns

LNA High Gain Mode ($V_{CC} = 2.75$ V, Bypass = 2.75 V, Enable = 2.75 V)

LNA Gain		-	15	-	dB
LNA Noise Figure		-	1.5	-	dB
LNA Input IP3		-	0	-	dBm

NOTE: Tone spacing for IIP3 measurement is 5.0 MHz.

Freescale Semiconductor, Inc.

Table 3. Target Specifications (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
LNA Supply Current	I_{DD}	-	3.0	-	mA

LNA Low Gain Mode ($V_{CC} = 2.75$ V, Bypass = 0 V, Enable = 2.75 V)

LNA Gain		-	-5.0	-	dB
LNA Noise Figure		-	5.0	-	dB
LNA Input IP3		-	20	-	dBm
LNA Supply Current	I_{DD}	-	10	-	μ A

Mixer Mode ($V_{CC} = 2.75$ Vdc, Enable = 2.75 V)

Conversion Gain		-	10	-	dB
SSB Noise Figure		-	8.0	-	dB
Input IP3		-	-3.0	-	dBm
Supply Current		-	5.0	-	mA
LO Drive Level		-	-10	-	dBm

NOTE: Tone spacing for IIP3 measurement is 5.0 MHz.

Table 4. Truth Table

(1 = 2.75 V, 0 = 0 V)

Enable	Bypass	Mode
0	0	Sleep
0	1	Undefined - do not use
1	0	Low Gain
1	1	High Gain

Table 5. Pin Function Description

Pin	Symbol	Description
1	LNA Out	LNA Output
2	Bypass	LNA Bypass Control
3	Mix In	Mixer Input
4	Enable	Chip Enable
5	LO+	Local Oscillator Input +
6	LO-	Local Oscillator Input -

Freescale Semiconductor, Inc.

Table 5. Pin Function Description (Continued)

Pin	Symbol	Description
7	IF+	Differential IF Output +
8	IF-	Differential IF Output -
9	V _{CC}	Supply
10	LNA In	LNA Input
11	Gnd	Ground
12	Mix Bias	Mixer Bias Adjustment

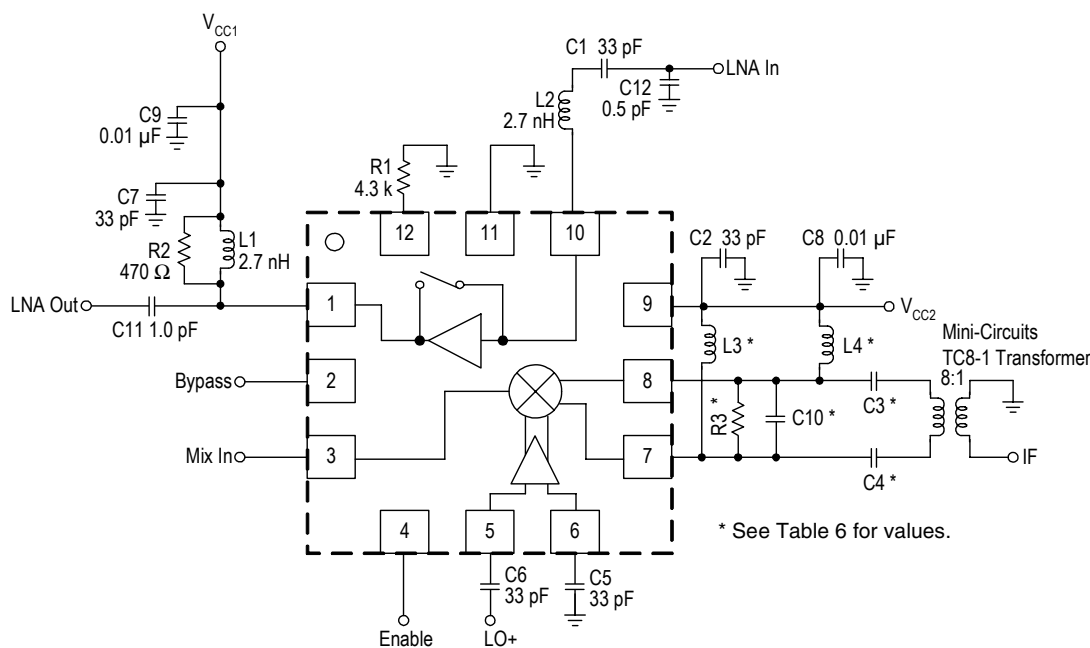


Figure 2. Application Schematic

Table 6. Bill of Material for Application Schematic

Component	190 MHz IF	380 MHz IF
C3	1.2 pF	2.2 pF
C4	1.2 pF	2.2 pF
C10	1.2 pF	1.2 pF
L3	150 nH	39 nH
L4	150 nH	39 nH
R3	5.0 kΩ	20 kΩ

NOTE: All other components are the same for both configurations.

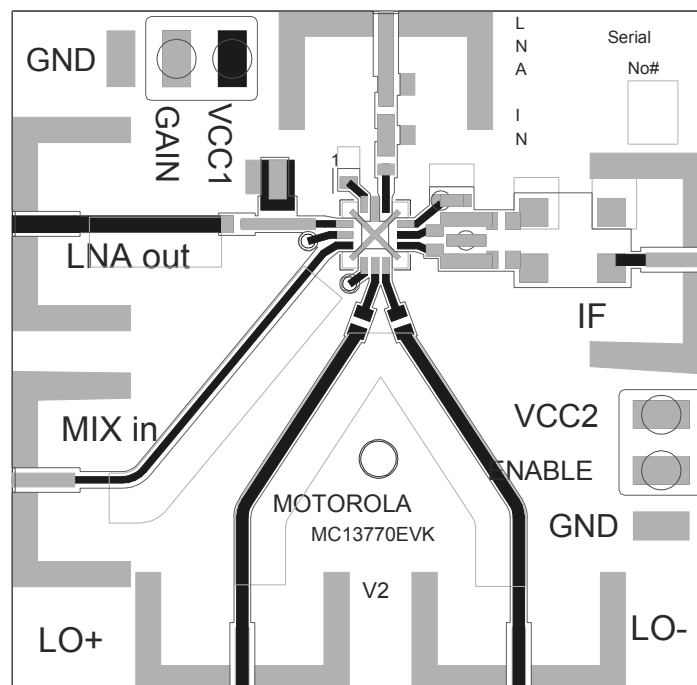


Figure 3. Application PCB (Not to Scale)

Product Preview

Order this document
from WBSG Marketing
Rev. 2, 12/2002

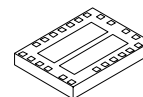
$\pi/4$ -DQPSK/GMSK
800/1900 MHz
3.5 V Power Amplifier



MOTOROLA
intelligence everywhere™

digital dna™

MMM5047



Package Information

Plastic Package
Case 1440
(Module, 9x12mm)

Ordering Information

Device	Device Marking	Package
MMM5047	Figure 42	Module

The MMM5047 is a 3.5 V dual-band, tri-mode (AMPS 800 MHz, $\pi/4$ -DQPSK/GMSK 800/1900 MHz) single supply RF power amplifier module for the 800/1900 MHz bands. This is an integrated Power Amplifier with input and output matching. This device is manufactured in advanced InGaP HBT.

- Multi-Mode and Dual-Band
824 to 849 MHz AMPS/ $\pi/4$ -DQPSK/GMSK
1850 to 1910 MHz $\pi/4$ -DQPSK/GMSK
- Single Supply InGaP HBT Technology
- Internal Input and Output Matching
- Low Leakage Current (<10 μ A)
- High Linearity
- Typical 3.5 V Characteristics:
AMPS: PAE = 27.6% @ P_{out} = 28 dBm
 $\pi/4$ -DQPSK Low Band: PAE = 36.7% ACP1 = -31.7 dBc,
ACP2 = -58 dBc @ P_{out} = 30 dBm
GMSK Low Band: PAE = 44.3% @ P_{out} = 32 dBm
 $\pi/4$ -DQPSK High Band: PAE = 32.2% ACP1 = -33.4 dBc,
ACP2 = -51 dBc @ P_{out} = 30 dBm
GMSK High Band: PAE = 39.8% @ P_{out} = 32 dBm
- SMT Module Package
- Small Footprint (9 x 12 mm)
- Low Profile (<1.8 mm)

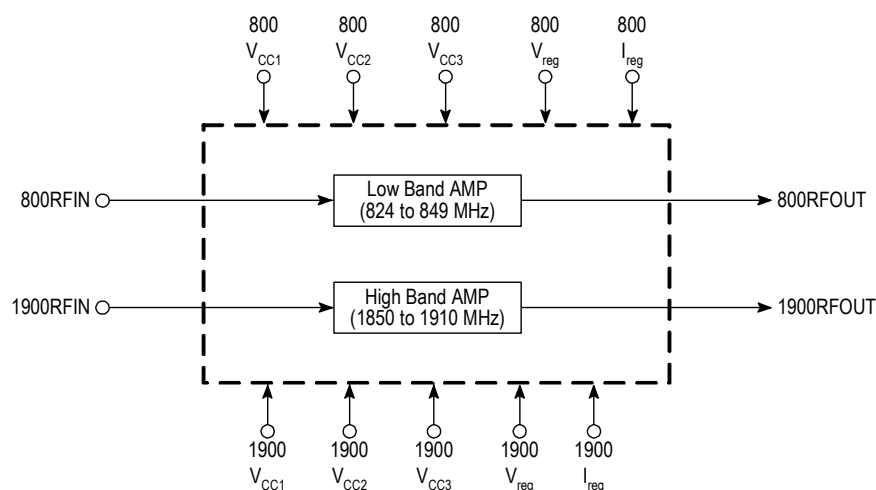


Figure 1. Simplified Block Diagram

1 Electrical Characteristics

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage (DC only)	800V _{CC1,2,3} , 1900V _{CC1,2,3}	6.0	V
Leakage Current (800V _{reg} = 1900V _{reg} = 800I _{reg} = 1900I _{reg} = 0 V) V _{CC} = 3.5 V and T _A = 25°C V _{CC} = 3.5 V and T _A = 85°C V _{CC} = 4.5 V and T _A = 60°C		<10 <20 <20	μA
Maximum Input Power (V _{CC} ≤ 4.5 V into 50 Ω load)		10	dBm
Operating Ambient Temperature Range	T _A	-30 to 85	°C
Operating Case Temperature Range	T _C	-30 to 90	°C
Storage Temperature Range	T _{stg}	-35 to 100	°C
Maximum Die Temperature		150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.
 2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤60 V and Machine Model (MM) ≤50 V. Additional ESD data available upon request.
 3. Meets Moisture Sensitivity Level (MSL) 3. See Figure 42 on page 56 for additional details.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Collector Voltage	800V _{CC1,2,3} , 1900V _{CC1,2,3}	3.0	-	4.5	V
Regulated Voltage	800V _{reg} , 1900V _{reg}	2.7	-	2.86	V
Bias Supply Voltage	800I _{reg} , 1900I _{reg}	0	-	2.7	V
Bias Supply Current	800I _{reg} , 1900I _{reg}	0	-	5.0	mA
Input Power					dBm
Low Band AMPS Mode	800RFIN	-40	-	2.0	
Low Band $\pi/4$ -DQPSK Mode		-40	-	5.0	
Low Band GMSK Mode		-30	-	7.0	
High Band $\pi/4$ -DQPSK Mode	1900RFIN	-35	-	3.0	
High Band GMSK Mode		-30	-	6.0	

Table 3. Electrical Characteristics

(Specifications guaranteed for T_A = -30 to 85°C, V_{CC} = 3.0 to 4.5 V, with I_{reg} adjusted for Band and Temperature, unless otherwise noted. Typical values are for T_A = 25°C, V_{CC} = 3.5 V, V_{reg} = 2.75 V.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

All Modes

Input VSWR (Impedance 50 Ω)					
Low Band		-	1.3:1	2:1	
High Band		-	1.9:1	2.8:1	
Output VSWR (Impedance 50 Ω)					
Low Band		-	1.8:1	2.5:1	
High Band		-	1.8:1	2.5:1	
Load Mismatch Stress: Survival @ P _{out} = 32 dBm, V _{CC} = 4.5 V		-	-	10:1	VSWR
Stability: Spurious Output Level @ VSWR = 8:1 (output power under 50 Ω load should not exceed 32 dBm)		-	-	-36	dBm

Low Band Section (800 MHz)

AMPS (100% Duty Cycle)

Operating Frequency	f	824	-	849	MHz
Recommended Bias Control Current	800I _{reg}				mA
T _A = -30°C		-	0.8	-	
T _A = 25°C		-	1.2	-	
T _A = 85°C		-	1.6	-	
Output Power	P _{out}				dBm
V _{CC} $\geq$ 3.5 V		28	-	-	
3.0 V $\leq$ V _{CC} < 3.5 V		27	-	-	

Table 3. Electrical Characteristics (Continued)

(Specifications guaranteed for $T_A = -30$ to 85°C , $V_{CC} = 3.0$ to 4.5 V, with I_{reg} adjusted for Band and Temperature, unless otherwise noted. Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 3.5$ V, $V_{reg} = 2.75$ V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Power (adjusted to achieve minimum output power)	P_{in}	-40	-	2.0	dBm
Gain (minimum output Power)	G	25	30.3	36.8	dB
Power Added Efficiency @ $3.0\text{ V} \leq V_{CC} \leq 3.5\text{ V}$ @ $V_{CC} > 3.5\text{ V}$	PAE	19 16	27.6 -	- -	%
Intermodulation due to signals at Input (Desired input signal adjusted for minimum P_{out} @ 849 MHz, Interfering input signal @ 829 MHz adjusted for -40 dBc relative to desired output signal)	$P_{im\text{dout}}$	-	-60.3	-46	dBc
Intermodulation due to signals at Output (Desired input signal adjusted for minimum P_{out} @ 849 MHz, Interfering signal injected at device output @ 829 MHz, -40 dBc relative to desired output signal)	$P_{im\text{dout}}$	-	-71.8	-50	dBc
Harmonics $2f_o$ $3f_o$		- -	-33 -69	-27 -59	dBc
RX Band Noise Power (30 kHz resolution bandwidth)		-	-87.6	-78	dBm

$\pi/4$ -DQPSK (33% Duty Cycle, 20 msec period)

Operating Frequency	f	824	-	849	MHz
Recommended Bias Control Current $T_A = -30^\circ\text{C}$ $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$800I_{reg}$	- - -	0.6 0.8 1.2	- - -	mA
Output Power $V_{CC} \geq 3.5\text{ V}$ $3.0\text{ V} \leq V_{CC} < 3.5\text{ V}$	P_{out}	30 28.5	- -	- -	dBm
Input Power (adjusted to achieve minimum output power)	P_{in}	-40	-	5.0	dBm
Gain (minimum output Power)	G	24	29.6	36.5	dB
Power Added Efficiency @ $3.0\text{ V} \leq V_{CC} \leq 3.5\text{ V}$ @ $V_{CC} > 3.5\text{ V}$	PAE	24 21	36.7 -	- -	%
ACP1 @ $\pm 30\text{ kHz}$ @ $V_{CC} \geq 3.5\text{ V}$ @ $3.0\text{ V} \leq V_{CC} < 3.5\text{ V}$		- -	-31.7 -	-29 -28.5	dBc
ACP2 @ $\pm 60\text{ kHz}$		-	-58	-48	dBc
ACP3 @ $\pm 90\text{ kHz}$		-	-	-48	dBc

Table 3. Electrical Characteristics (Continued)

(Specifications guaranteed for $T_A = -30$ to 85°C , $V_{CC} = 3.0$ to 4.5 V, with I_{reg} adjusted for Band and Temperature, unless otherwise noted. Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 3.5$ V, $V_{reg} = 2.75$ V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Intermodulation due to signals at Input (Desired input signal adjusted for minimum P_{out} @ 849 MHz, Interfering input signal @ 829 MHz adjusted for -40 dBc relative to desired output signal)	P_{imdout}	-	-57.5	-50	dBc
Intermodulation due to signals at Output (Desired input signal adjusted for minimum P_{out} @ 849 MHz, Interfering signal injected at device output @ 829 MHz, -40 dBc relative to desired output signal)	P_{imdout}	-	-67.5	-50	dBc
Harmonics $2f_o$ $3f_o$		- -	-32.4 -67.3	-27 -59	dBc
Error Vector Magnitude @ $3.0\text{ V} \leq V_{CC} \leq 3.5\text{ V}$ @ $V_{CC} > 3.5\text{ V}$	EVM	- -	2.1 -	4.5 4.0	%
RX Band Noise Power (30 kHz resolution bandwidth)		-	-85.7	-76	dBm

GMSK (25% Duty Cycle, 4.615 msec period)

Operating Frequency	f	824	-	849	MHz
Recommended Bias Control Current $T_A = -30^\circ\text{C}$ $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$800I_{reg}$	- - -	2.0 2.0 2.0	- - -	mA
Output Power $V_{CC} \geq 3.5\text{ V}$ $3.0\text{ V} \leq V_{CC} < 3.5\text{ V}$	P_{out}	32 30.5	- -	- -	dBm
Input Power (adjusted to achieve minimum output power)	P_{in}	-30	-	7.0	dBm
Gain (minimum output Power)	G	24	29.9	37	dB
Power Added Efficiency @ $3.0\text{ V} \leq V_{CC} \leq 3.5\text{ V}$ @ $V_{CC} > 3.5\text{ V}$	PAE	33 28.5	44.3 -	- -	%
AM/PM Conversion @ $3.0\text{ V} \leq V_{CC} \leq 3.5\text{ V}$ @ $V_{CC} > 3.5\text{ V}$		- -	1.1 -	3.0 2.0	°/dB
Intermodulation due to signals at Input (Desired input signal adjusted for minimum P_{out} @ 849 MHz, Interfering input signal @ 829 MHz adjusted for -40 dBc relative to desired output signal)	P_{imdout}	-	-50.7	-44	dBc
Intermodulation due to signals at Output (Desired input signal adjusted for minimum P_{out} @ 849 MHz, Interfering signal injected at device output @ 829 MHz, -40 dBc relative to desired output signal)	P_{imdout}	-	-62.3	-50	dBc

Table 3. Electrical Characteristics (Continued)

(Specifications guaranteed for $T_A = -30$ to 85°C , $V_{CC} = 3.0$ to 4.5 V, with I_{reg} adjusted for Band and Temperature, unless otherwise noted. Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 3.5$ V, $V_{reg} = 2.75$ V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Harmonics					dBc
$2f_o$		-	-33.2	-29	
$3f_o$		-	-64.5	-59	
RX Band Noise Power (30 kHz resolution bandwidth)		-	-86.5	-77	dBm
Low Band Harmonics @ High Band Output (low band @ minimum output power, high band off)					dBc
$2f_o$		-	-64.1	-60	
$3f_o$ (25 and 85°C)		-	-66.2	-60	
$3f_o$ (-30°C)		-	-	-58	

High Band Section (1900 MHz)

$\pi/4$ -DQPSK (33% Duty Cycle, 20 msec period)

Operating Frequency	f	1850	-	1910	MHz
Recommended Bias Control Current	$1900I_{reg}$				mA
$T_A = -30^\circ\text{C}$		-	1.8	-	
$T_A = 25^\circ\text{C}$		-	2.0	-	
$T_A = 85^\circ\text{C}$		-	2.0	-	
Output Power	P_{out}				dBm
$V_{CC} \geq 3.5$ V		30	-	-	
$3.0 \text{ V} \leq V_{CC} < 3.5$ V		28.5	-	-	
Input Power (adjusted to achieve minimum output power)	P_{in}	-35	-	3.0	dBm
Gain (minimum output Power)	G	26	31.1	36.3	dB
Relative Image Band Gain (Freq = 2275 to 2340 MHz, relative to in-band gain at minimum P_{out})		-	-5.0	-1.4	dBc
Power Added Efficiency	PAE				%
@ $3.0 \text{ V} \leq V_{CC} \leq 3.5$ V		22	32.2	-	
@ $V_{CC} > 3.5$ V		19	-	-	
ACP1 @ ± 30 kHz		-	-33.4	-29	dBc
ACP2 @ ± 60 kHz		-	-51	-47	dBc
ACP3 @ ± 90 kHz		-	-	-48	dBc
Intermodulation due to signals at Input (Desired input signal adjusted for minimum P_{out} @ 1910 MHz, Interfering input signal @ 1890 MHz adjusted for -40 dBc relative to desired output signal)	P_{imdout}	-	-69.5	-50	dBc
Intermodulation due to signals at Output (Desired input signal adjusted for minimum P_{out} @ 1910 MHz, Interfering signal injected at device output @ 1890 MHz, -40 dBc relative to desired output signal)	P_{imdout}	-	-64.5	-50	dBc

Table 3. Electrical Characteristics (Continued)

(Specifications guaranteed for $T_A = -30$ to 85°C , $V_{CC} = 3.0$ to 4.5 V, with I_{reg} adjusted for Band and Temperature, unless otherwise noted. Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 3.5$ V, $V_{reg} = 2.75$ V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Harmonics $2f_o$ $3f_o$		- -	-41.2 -53.7	-34 -46	dBc
Error Vector Magnitude @ $3.0\text{ V} \leq V_{CC} \leq 3.5\text{ V}$ @ $V_{CC} > 3.5\text{ V}$	EVM	- -	1.6 -	4.5 4.0	%
RX Band Noise Power (30 kHz resolution bandwidth)		-	-85.3	-75	dBm

GMSK (25% Duty Cycle, 4.615 msec period)

Operating Frequency	f	1850	-	1910	MHz
Recommended Bias Control Current $T_A = -30^\circ\text{C}$ $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$1900I_{reg}$	- - -	1.1 2.0 2.0	- - -	mA
Output Power $V_{CC} \geq 3.5\text{ V}$ $3.0\text{ V} \leq V_{CC} < 3.5\text{ V}$	P_{out}	32 30.5	- -	- -	dBm
Input Power (adjusted to achieve minimum output power)	P_{in}	-30	-	6.0	dBm
Gain (minimum output Power)	G	25	30.9	36.1	dB
Relative Image Band Gain (Freq = 2275 to 2340 MHz, relative to in-band gain at minimum P_{out})		-	-5.7	-2.0	dBc
Power Added Efficiency @ $3.0\text{ V} \leq V_{CC} \leq 3.5\text{ V}$ @ $V_{CC} > 3.5\text{ V}$	PAE	28 22	39.8 -	- -	%
AM/PM Conversion @ $3.0\text{ V} \leq V_{CC} \leq 3.5\text{ V}$ @ $V_{CC} > 3.5\text{ V}$		- -	1.1 -	2.5 2.0	°/dB
Intermodulation due to signals at Input (Desired input signal adjusted for minimum P_{out} @ 1910 MHz, Interfering input signal @ 1890 MHz adjusted for -40 dBc relative to desired output signal)	P_{imdout}	-	-54.2	-45	dBc
Intermodulation due to signals at Output (Desired input signal adjusted for minimum P_{out} @ 1910 MHz, Interfering signal injected at device output @ 1890 MHz, -40 dBc relative to desired output signal)	P_{imdout}	-	-54.9	-48	dBc
Harmonics $2f_o$ $3f_o$		- -	-41.9 -53.1	-35 -44	dBc
RX Band Noise Power (30 kHz resolution bandwidth)		-	-86.2	-77	dBm

Table 3. Electrical Characteristics (Continued)

(Specifications guaranteed for $T_A = -30$ to 85°C , $V_{CC} = 3.0$ to 4.5 V, with I_{reg} adjusted for Band and Temperature, unless otherwise noted. Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 3.5$ V, $V_{reg} = 2.75$ V.)

Characteristic	Symbol	Min	Typ	Max	Unit
High Band Harmonics @ Low Band Output (high band @ minimum output power, low band off)					dBc
$2f_o$		-	-68.7	-63	
$3f_o$		-	-62.3	-53	

2 Typical Performance Characteristics

2.1 Low Band ($\text{AMPS}/\pi/4$ -DQPSK/GMSK Modes)

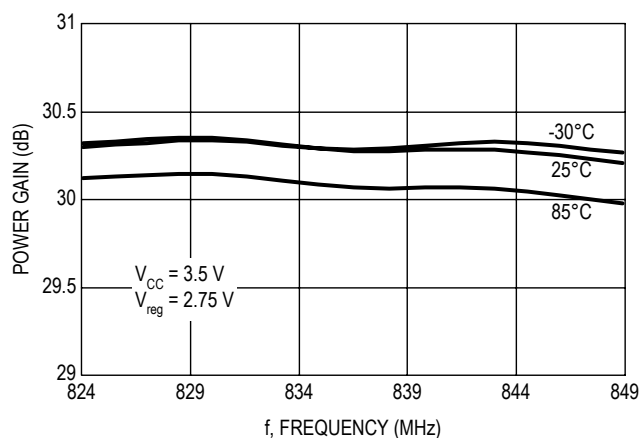


Figure 2. Power Gain in AMPS Mode versus Frequency

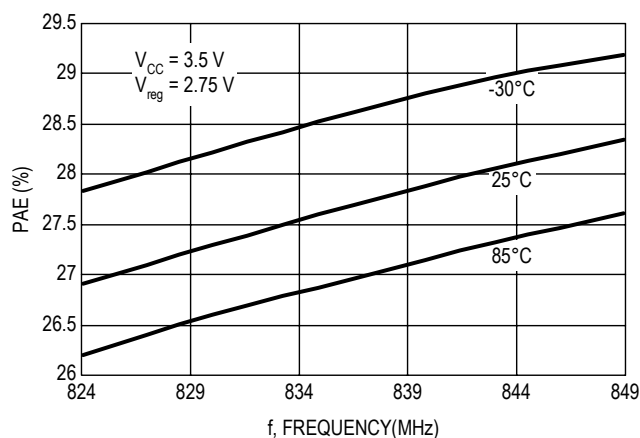


Figure 3. Power Added Efficiency in AMPS Mode versus Frequency

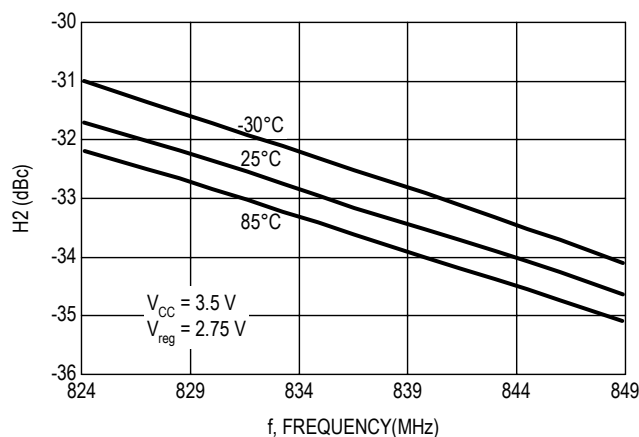


Figure 4. Second Harmonic Output in AMPS Mode versus Frequency

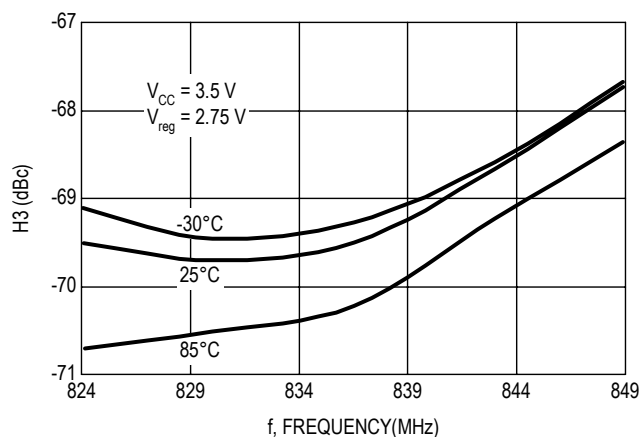


Figure 5. Third Harmonic Output in AMPS Mode versus Frequency

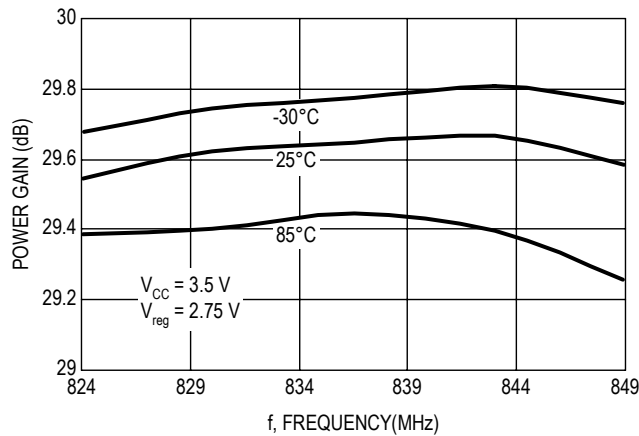


Figure 6. Power Gain in $\pi/4$ -DQPSK Mode versus Frequency

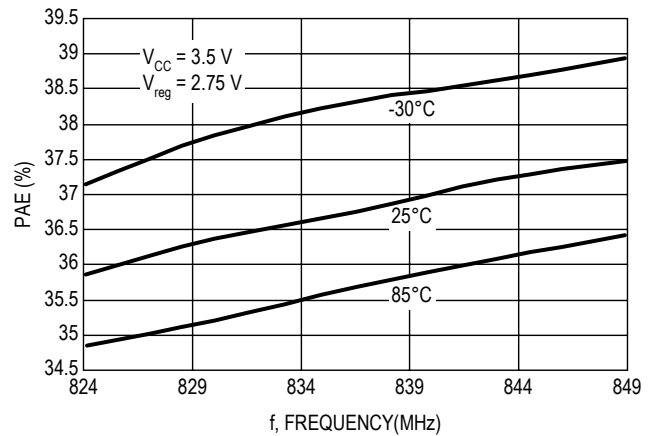


Figure 7. Power Added Efficiency in $\pi/4$ -DQPSK Mode versus Frequency

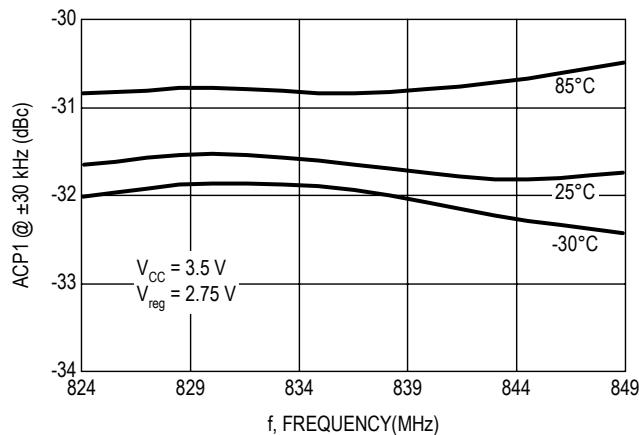


Figure 8. Adjacent Channel Power in $\pi/4$ -DQPSK Mode versus Frequency

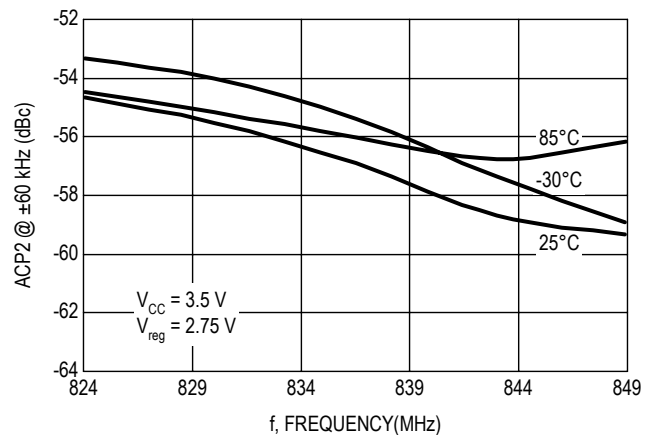


Figure 9. Adjacent Channel Power in $\pi/4$ -DQPSK Mode versus Frequency

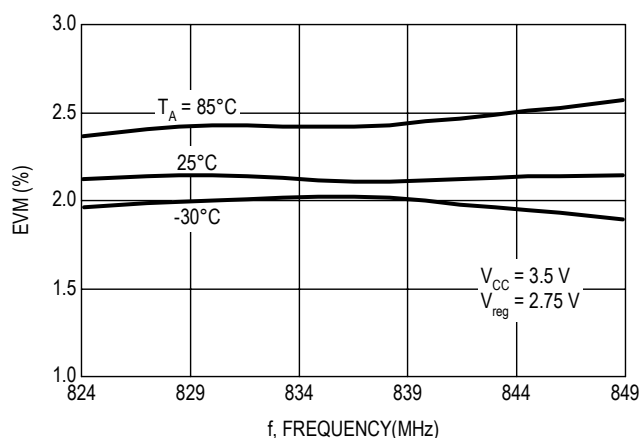


Figure 10. Error Vector Magnitude in $\pi/4$ -DQPSK versus Frequency

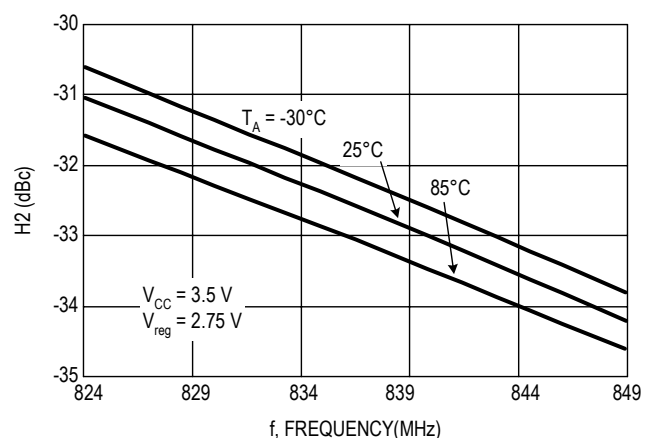


Figure 11. Second Harmonic Output in $\pi/4$ -DQPSK versus Frequency

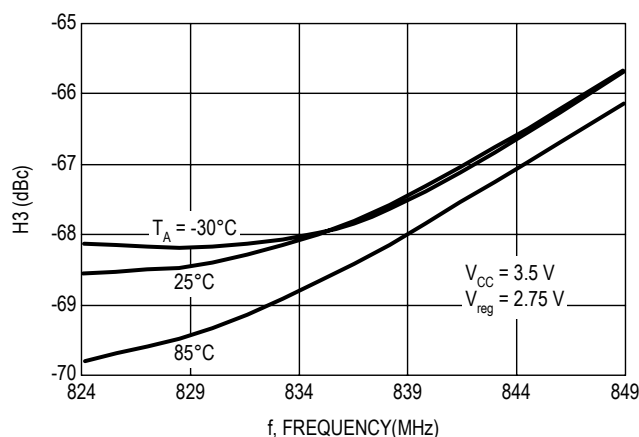


Figure 12. Third Harmonic Output in $\pi/4$ -DQPSK versus Frequency

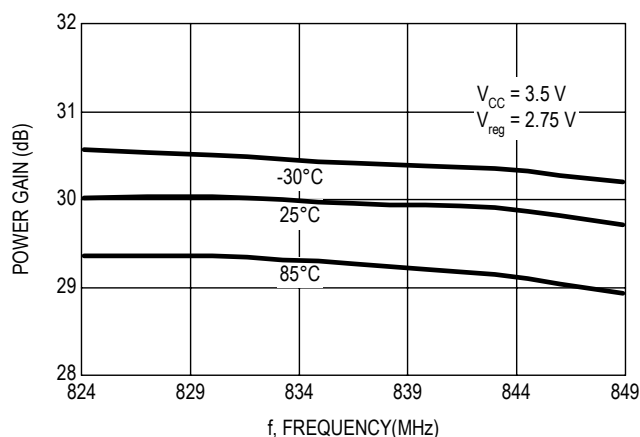


Figure 13. Power Gain in GMSK Mode versus Frequency

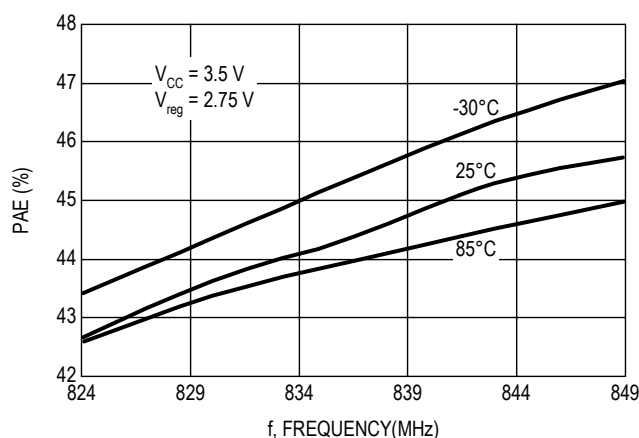


Figure 14. Power Added Efficiency in GMSK Mode versus Frequency

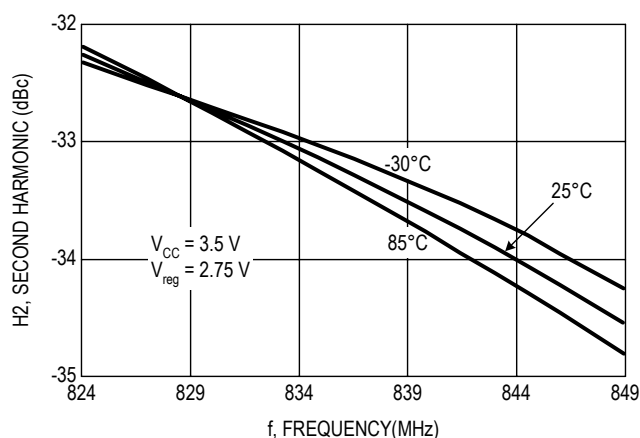


Figure 15. Second Harmonic Output in GMSK Mode versus Frequency

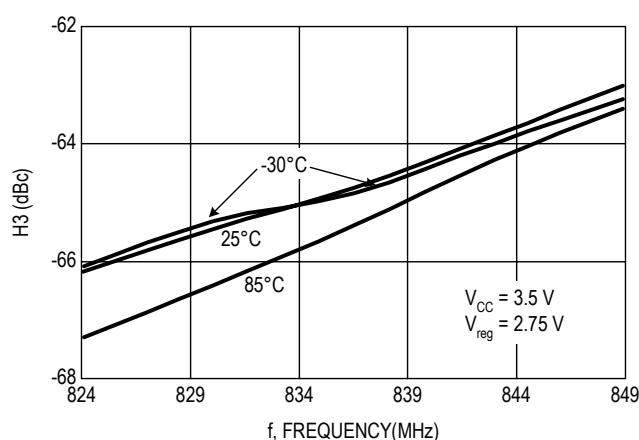


Figure 16. Third Harmonic Output in GMSK Mode versus Frequency

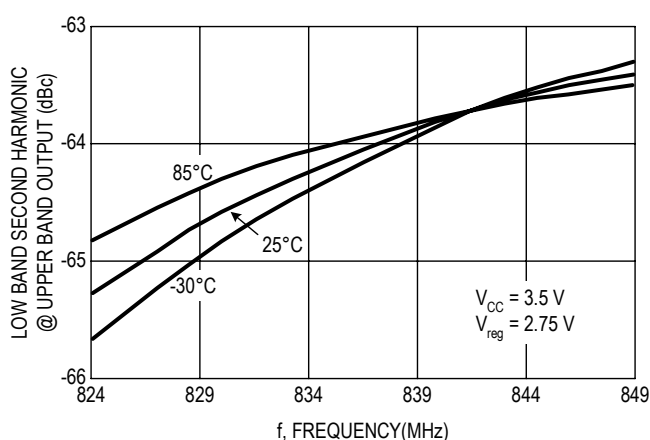


Figure 17. Low Band Second Harmonic at Upper Band Output in GMSK Mode versus Frequency

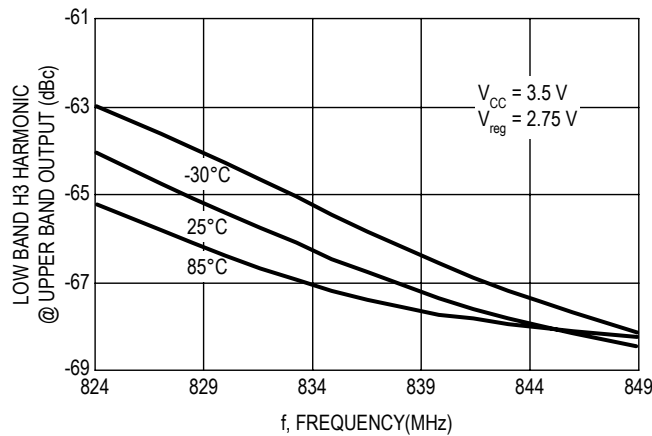


Figure 18. Low Band Third Harmonic at High Band Output in GMSK Mode versus Frequency

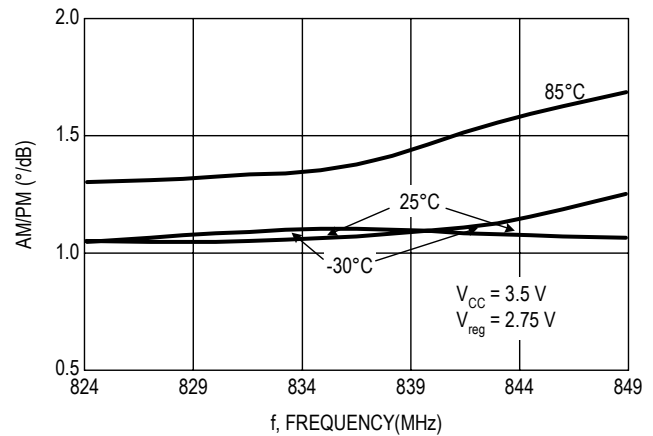


Figure 19. AM/PM in GMSK Mode versus Frequency

2.2 High Band ($\pi/4$ -DQPSK/GMSK Modes)

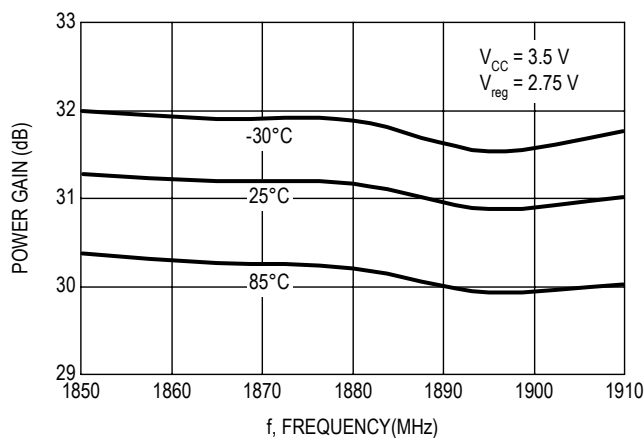


Figure 20. Power Gain in $\pi/4$ -DQPSK Mode versus Frequency

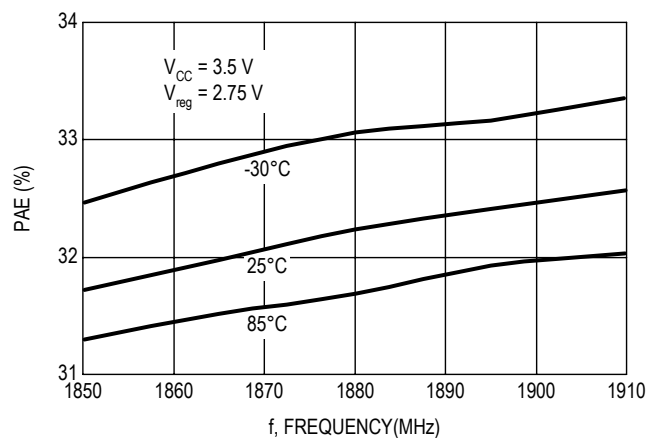


Figure 21. Power Added Efficiency in $\pi/4$ -DQPSK Mode versus Frequency

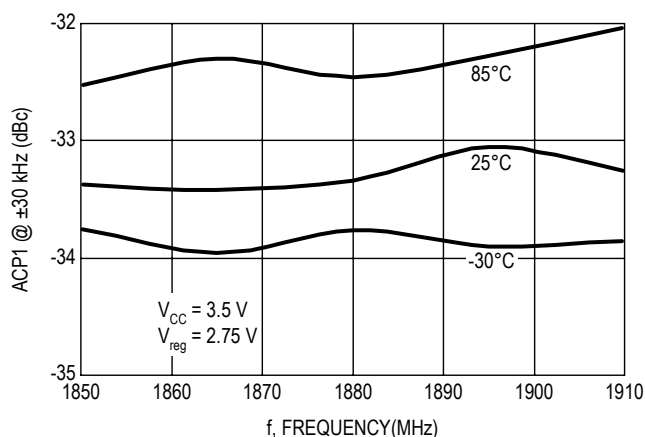


Figure 22. Adjacent Channel Power in $\pi/4$ -DQPSK Mode versus Frequency

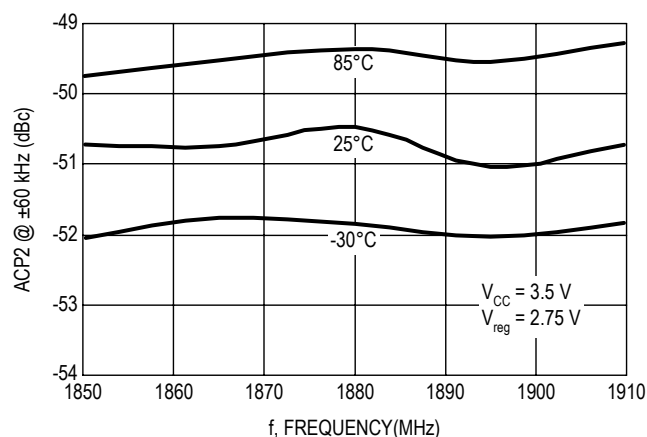


Figure 23. Adjacent Channel Power in $\pi/4$ -DQPSK Mode versus Frequency

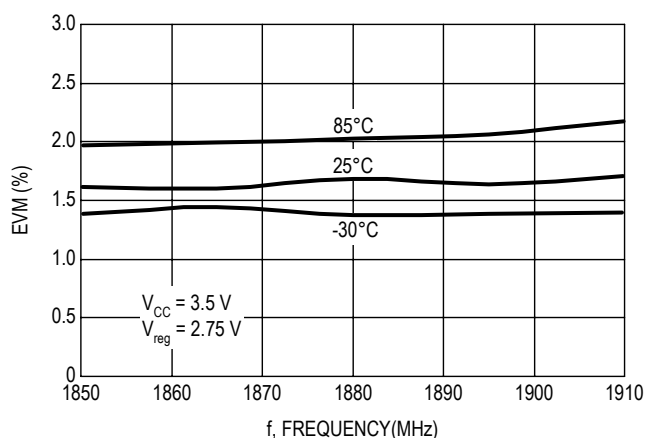


Figure 24. Error Vector Magnitude versus in $\pi/4$ -DQPSK Mode Frequency

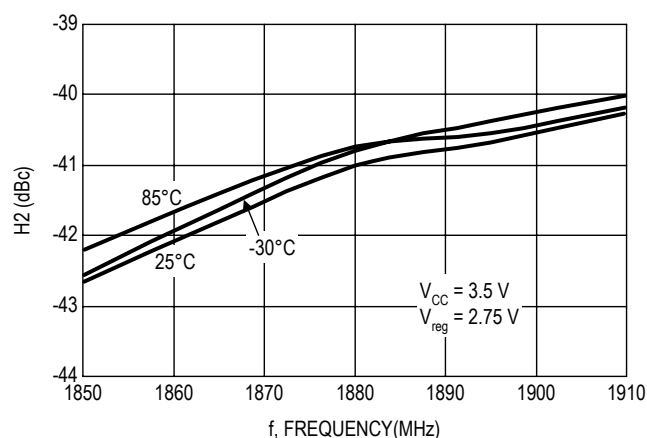


Figure 25. Second Harmonic Output in $\pi/4$ -DQPSK Mode versus Frequency

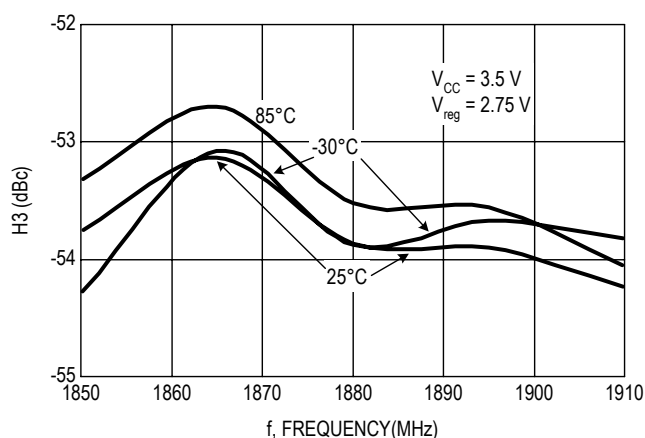


Figure 26. Third Harmonic Output in $\pi/4$ -DQPSK Mode versus Frequency

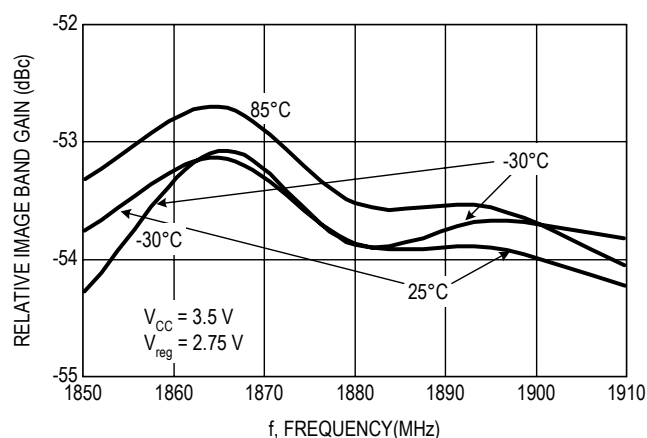


Figure 27. Relative Image Band Gain in $\pi/4$ -DQPSK Mode versus Frequency

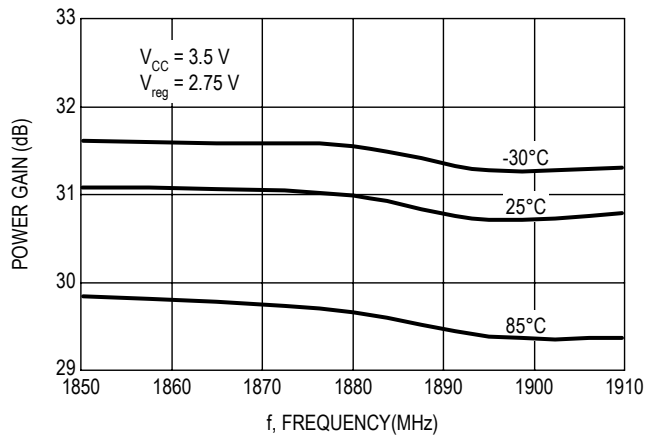


Figure 28. Power Gain in GMSK Mode versus Frequency

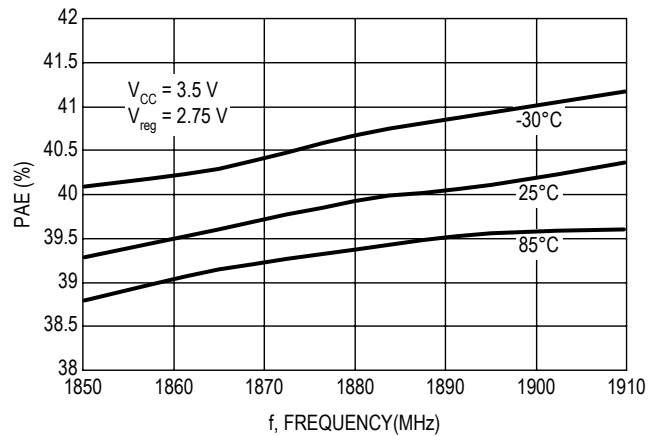


Figure 29. Power Added Efficiency in GMSK Mode versus Frequency

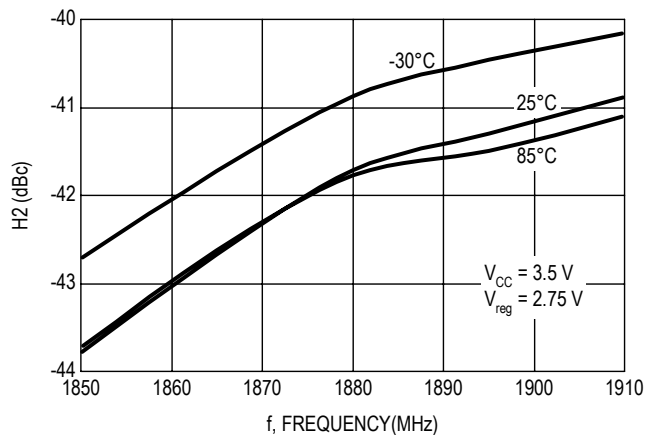


Figure 30. Second Harmonic Output in GMSK Mode versus Frequency

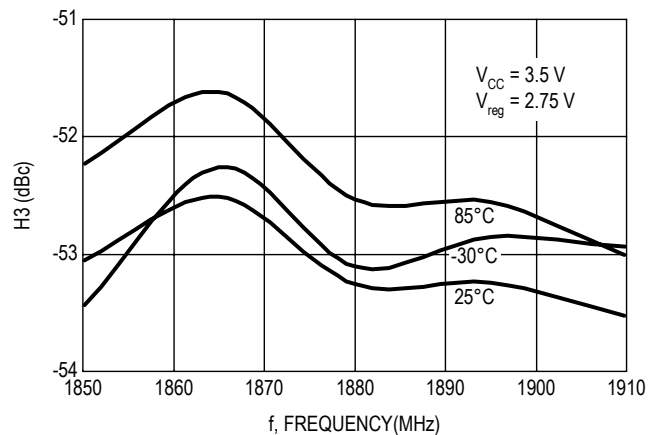


Figure 31. Third Harmonic Output in GMSK Mode versus Frequency

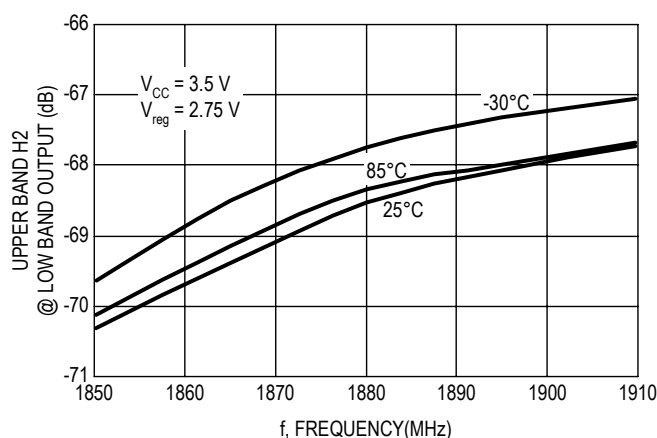


Figure 32. Upper Band Second Harmonic at Low Band Output in GMSK Mode versus Frequency

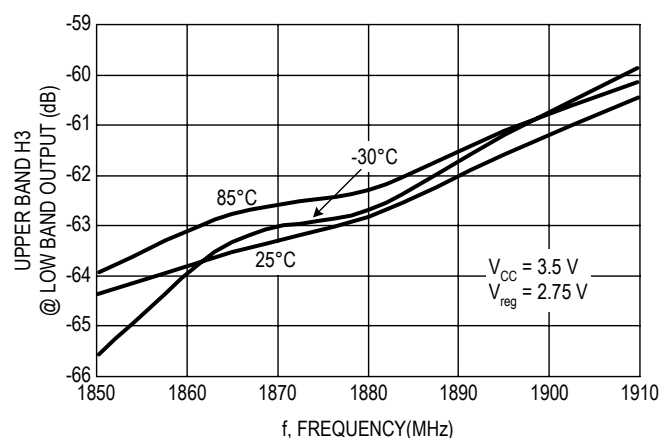


Figure 33. Upper Band Third Harmonic at Low Band Output in GMSK Mode versus Frequency

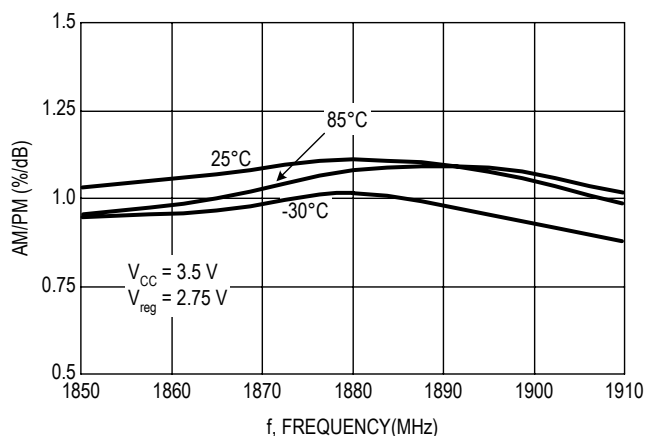


Figure 34. AM/PM in GMSK Mode versus Frequency

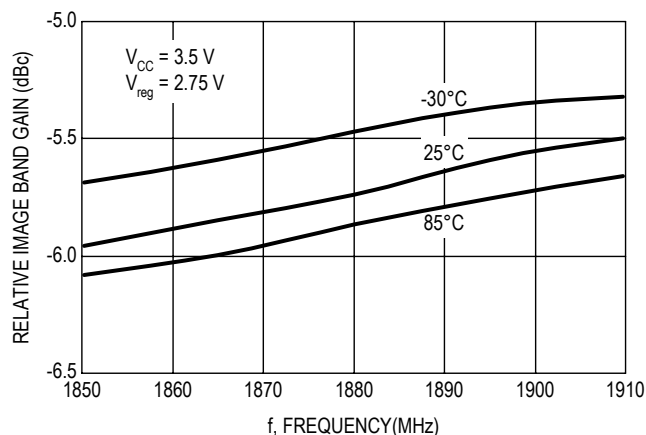


Figure 35. Relative Image Band Gain in GMSK Mode versus Frequency

2.3 All Modes

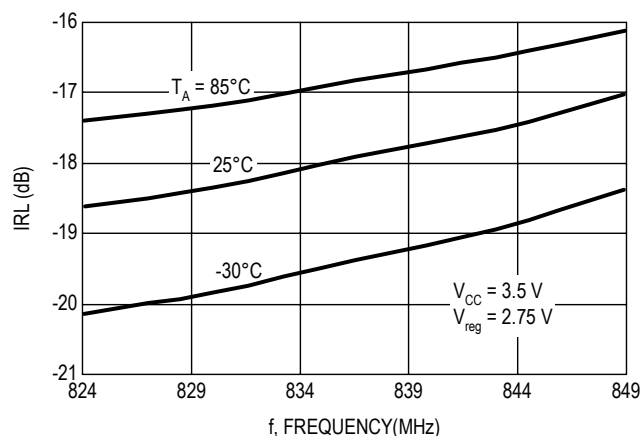


Figure 36. Input Return Loss in Low Band versus Frequency

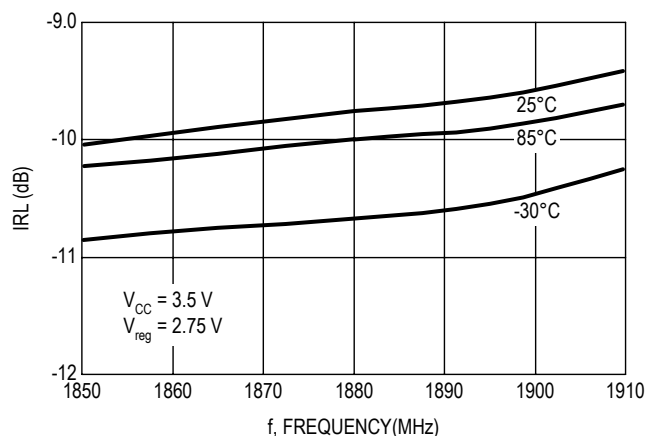


Figure 37. Input Return Loss in High Band versus Frequency

3 Contact Connections

Table 4. Contact Function Description

Contact	Symbol	Description
1	1900 RFIN	1900 MHz RF input
2	GND	Ground
3	1900 V_{reg}	1900 MHz regulated DC voltage supply for 1st and 2nd stages bias circuits
4	1900 V_{CC2}	1900 MHz DC voltage supply for 2nd stage
5	1900 I_{reg}	1900 MHz bias adjust current supply for 3rd stage
6	GND	Ground
7	N.C.	Not connected
8	1900 V_{CC3}	1900 MHz DC voltage supply for 3rd stage
9	N.C.	Not connected
10	1900 RFOUT	1900 MHz RF output
11	800 RFOUT	800 MHz RF output
12	N.C.	Not connected
13	800 V_{CC3}	800 MHz DC voltage supply for 3rd stage
14	N.C.	Not connected
15	N.C.	Not connected
16	800 I_{reg}	800 MHz bias adjust current supply for 3rd stage
17	800 V_{CC2}	800 MHz DC voltage supply for 2nd stage
18	800 V_{CC1}	800 MHz DC voltage supply for 1st stage
19	800 RFIN	800 MHz RF input
20	GND	Ground
21	800 V_{reg}	800 MHz regulated DC voltage supply for 1st and 2nd stages bias circuits
22	N.C.	Not connected
23	1900 V_{CC1}	1900 MHz DC voltage supply for 1st stage

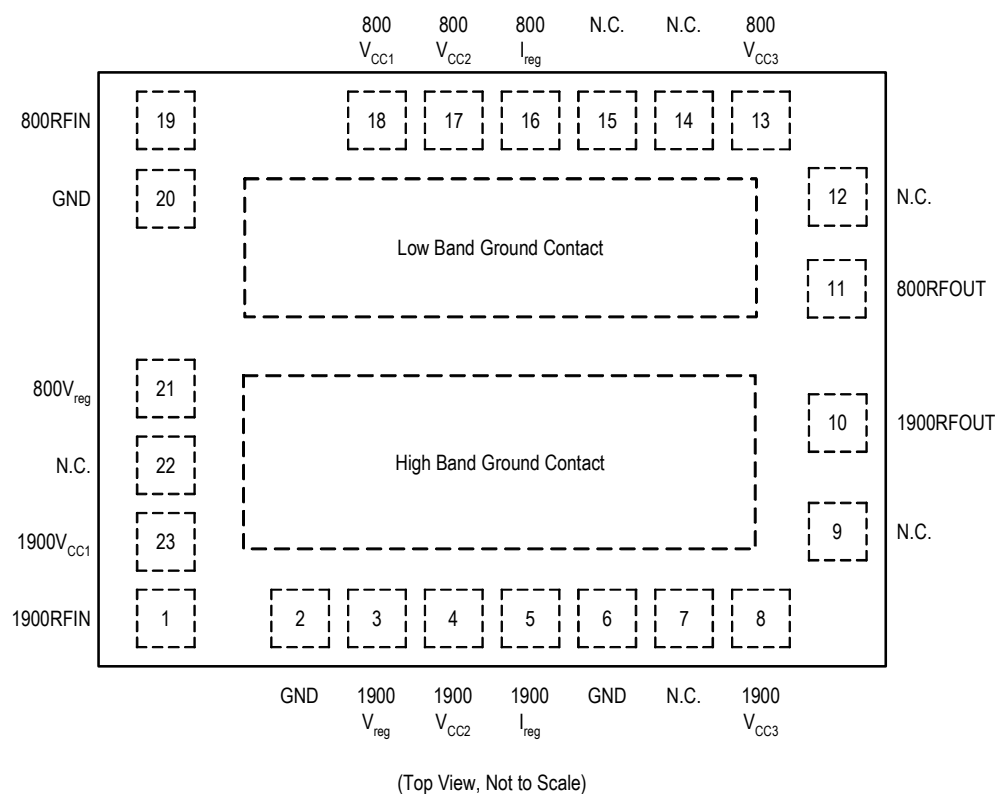


Figure 38. Contact Connections

4 Application Information

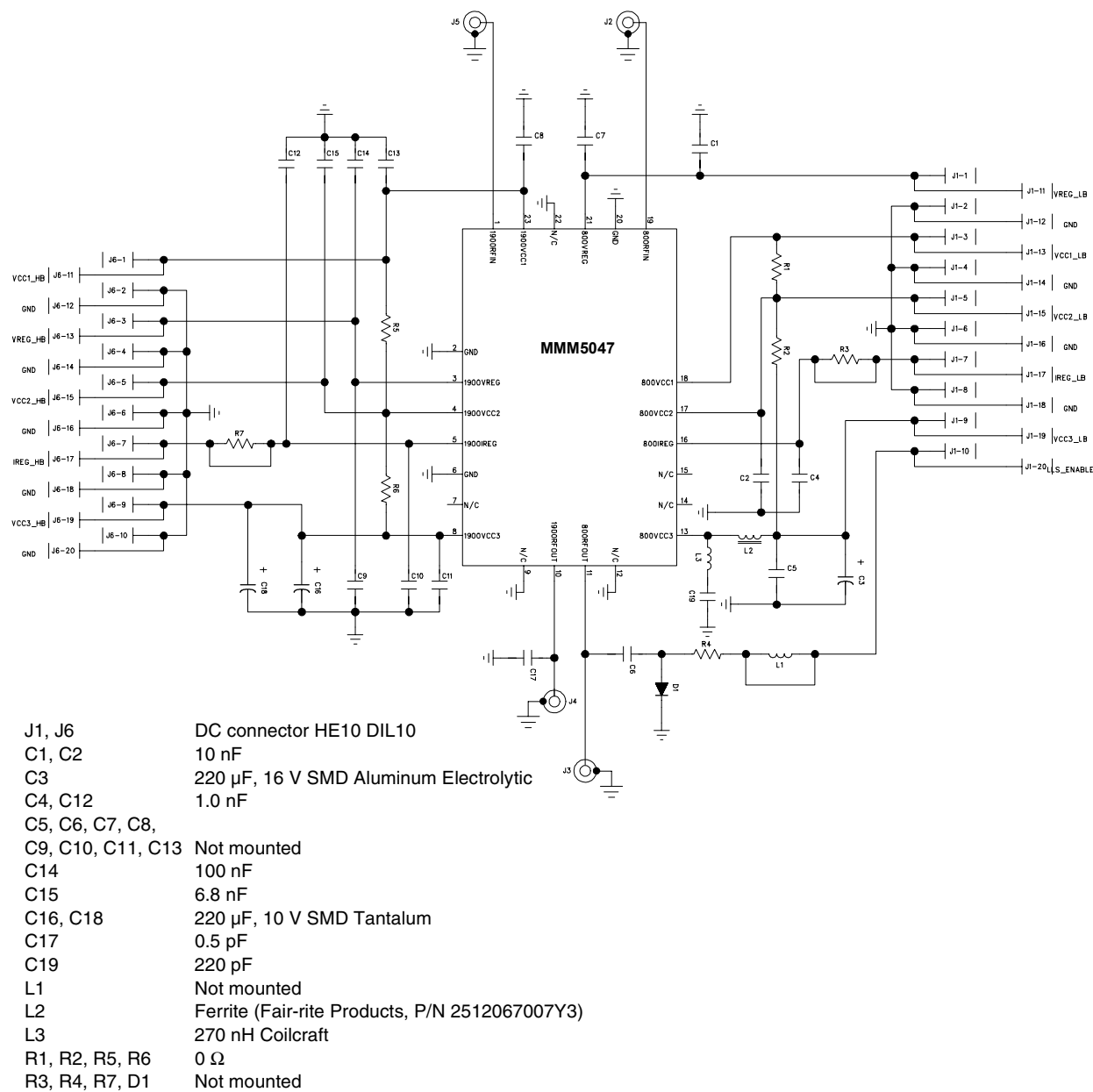
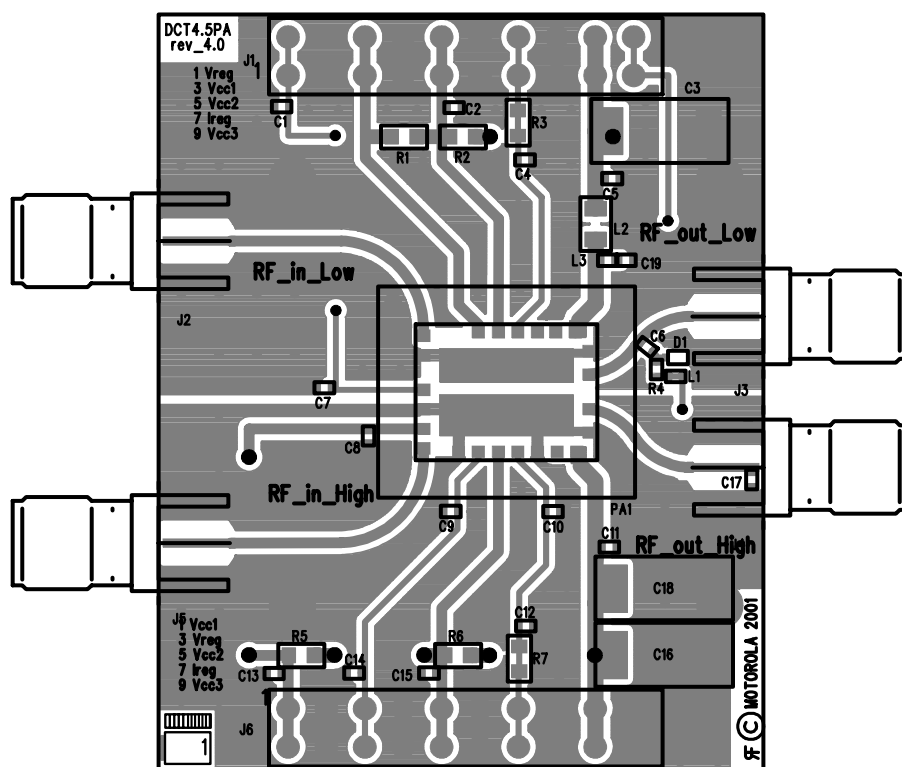


Figure 39. Application Schematic



NOTES: ALL VIA HOLES .015 DIA (0,38 mm DIAM)
 MATERIAL FR4 [NELCO]
 COPPER THICKNESS 35 μ m
 TOTAL THICKNESS .063 (1,6 mm)

STACKING INFOS.

TOP	
INNER 2	FR4 DIELEC t = .018 (0,46mm)
INNER 3	FR4 DIELEC t = .020 (0,50mm)
BOTTOM	FR4 DIELEC t = .018 (0,46mm)

Figure 40. Application PCB

Table 5. Recommended I_{reg} versus Mode and Temperature

Temperature	Low Band (824 to 849 MHz)			High Band (1850 to 1910 MHz)	
	AMPS (mA)	$\pi/4$ -DQPSK (mA)	GMSK (mA)	$\pi/4$ -DQPSK (mA)	GMSK (mA)
-30°C	0.8	0.6	2.0	1.8	1.1
25°C	1.2	0.8	2.0	2.0	2.0
85°C	1.6	1.2	2.0	2.0	2.0

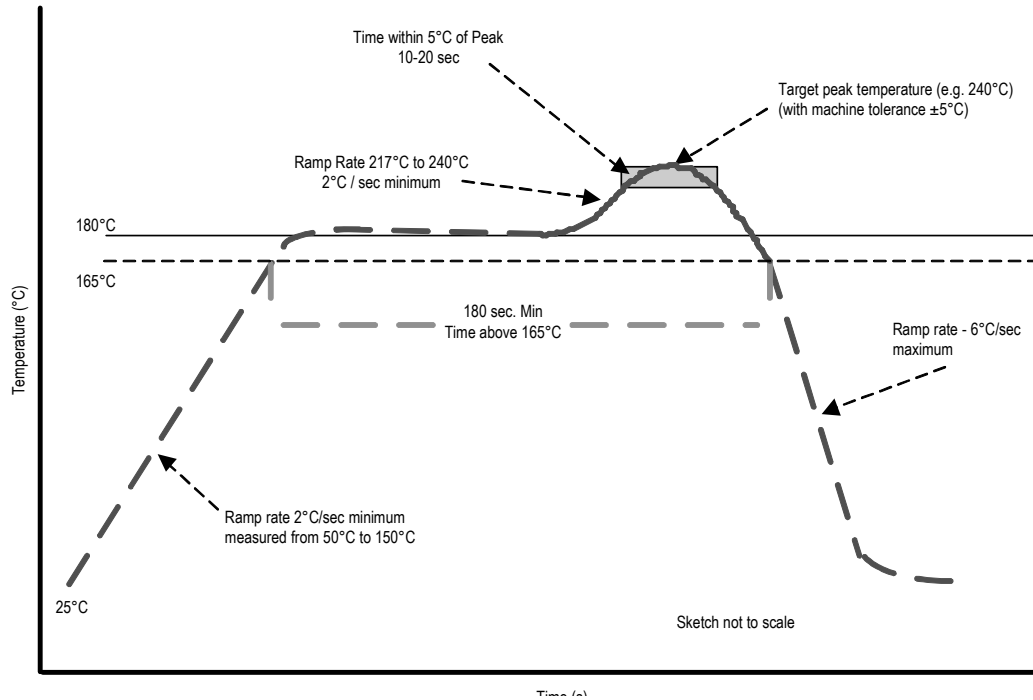


Figure 41. Solder Reflow Diagram

5 Packaging Information

Shipping, Packaging and Marking Information

Tape Width: 24.0 mm

Tape Pitch 12 mm (part to part)

Reel Diameter: 330 mm (13 in)

Component Orientation: Parts are to be orientated with pin 1 side closest to the tape's round sprocket holes on the tape's trailing edge.

Dry Pack: This device meets Moisture Sensitivity Level (MSL) 3. Parts will be shipped in Dry Pack. Parts must be stored at 30°C and 60% relative humidity with time out of dry pack not to exceed 168 hours.

In the event that parts are not handled or stored within these limits, one of the following dry out procedures must be completed prior to reflow:

1) 40°C Dry Out: Bake devices at $40^{\circ}\text{C} \leq T_A \leq 45^{\circ}\text{C}$, 5% Relative Humidity for at least 192 hours.

2) Room Temperature Dry Out: Store devices at less than 20% Relative Humidity for at least 500 hours.

Marking:

1st line: Motorola Logo

2nd Line: 7-digit Alphanumeric Part Number (MMM5047)

3rd Line: 5-digit X1 LOT ID (2-digit WAFER ID)/5-digit X4 LOT ID (2-digit WAFER ID)

4th Line: ASSEMBLY LOT # XXXXXXXXXX (10-digit Max.)

5th Line: DATE CODE - YYWW

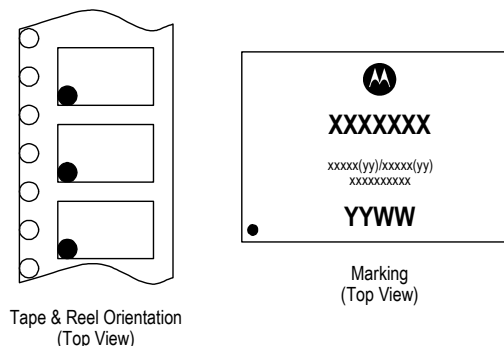


Figure 42. Shipping, Packing, and Marking Information

Technical Data

MMM5062/D
Rev. 3, 9/2002

Quad-Band GSM GPRS
3.5 V Power Amplifier



MOTOROLA
intelligence everywhere™

digital dna™

MMM5062



(Scale 1:1)

Package Information

Plastic Package

Case 1383

(Module, 7x7 mm)

Ordering Information

Device	Device Marking	Package
MMM5062	See Figure 30	Module

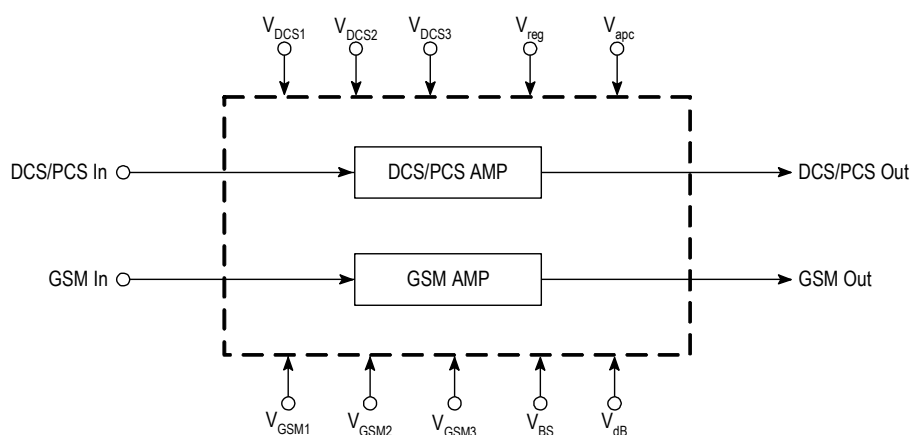
The MMM5062 is a quad-band single supply RF Power Amplifier for GSM850/GSM900/DCS1800/PCS1900 GPRS handheld radios. This fully integrated Power Amplifier uses a patented concept to realize the 50 Ω matching on-chip through integration of passives on the GaAs die. This allows module functionality in a very small 7 x 7 mm package and achieves best-in-class Power Amplifier performance and multi-band capability.

Applications:

- Quad-Band GSM850/900 DCS1800 and PCS1900
- Guaranteed for Class 10 GPRS

Features:

- Single Supply Enhancement Mode GaAs MESFET Technology
- Internal 50 Ω Input/Output Matching
- High Gain Three Stage Amplifier Design
- Typical 3.5 V Characteristics:
 - $P_{out} = 35.5$ dBm, PAE = 50% for GSM850
 - $P_{out} = 35.2$ dBm, PAE = 53% for GSM900
 - $P_{out} = 33.8$ dBm, PAE = 44% for DCS
 - $P_{out} = 34$ dBm, PAE = 43% for PCS
- Optimized and Guaranteed for Open-Loop Power Control Applications
- Small 7 x 7 mm Package



This device contains 26 active transistors.

Figure 1. Simplified Block Diagram

1 Electrical Specifications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	$V_{GSM1,2,3}, V_{DCS1,2,3}, V_{dB}$	6.0	V
RF Input Power	GSM IN, DCS/PCS IN	10	dBm
RF Output Power GSM Section DCS/PCS Section	GSM OUT DCS/PCS OUT	38 36	dBm
Operating Case Temperature Range	T_C	-35 to 100	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C
Die Temperature	T_J	150	°C

- NOTES:** 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤ 150 V and Machine Model (MM) ≤ 50 V. Additional ESD data available upon request.
3. Meets Moisture Sensitivity Level (MSL) 3. See Figure 30 on page 75 for additional details.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	$V_{GSM1,2,3}$, $V_{DCS1,2,3}$	2.7	-	5.5	V
Bias Supply Voltage	V_{dB}	2.7	-	5.5	V
Regulated Voltage	V_{REG}	2.5	2.8	3.0	V
Power Control Voltage	V_{apc}	0	1.8	2.8	V
Band Select	V_{BS}	0	2.8	3.0	V
Input Power GSM850/900	GSM IN	-1.0	-	8.0	dBm
Input Power DCS/PCS	DCS/PCS IN	2.0	-	10	dBm

Table 3. Control Requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Current for V_{reg} @ 2.8 V	I_{reg}	-	7.7	10	mA
Band Select Low Band Enable Voltage High Band Enable Voltage	V_{BS}	2.2 0	2.8 -	- 0.3	V
Current for $V_{BS} = 2.8$ V	I_{BS}	-	0.76	1.0	mA

Table 4. Electrical Characteristics

(Peak measurement at 25% duty cycle, 4.6 ms period, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
GSM 850 Section ($P_{in} = -1.0$ dBm, $V_{GSM1,2,3} = 3.5$ V pulsed, $V_{dB} = 3.5$ V, $V_{REG} = V_{BS} = 2.8$ V, $V_{ramp} = 1.8$ V pulsed)					
Frequency Range	BW	824	-	849	MHz
Output Power	P_{out}	34.5	35.5	-	dBm
Power Added Efficiency	PAE	42	50	-	%
Output Power @ Low Voltage ($V_{GSM1,2,3} = 2.8$ V pulsed, $V_{dB} = 2.8$ V)	P_{out}	33	33.8	-	dBm
Power Added Efficiency @ Low Voltage ($V_{GSM1,2,3} = 2.8$ V pulsed, $V_{dB} = 2.8$ V)	PAE	43	51	-	%
Harmonic Output $2f_o$ $\geq 3f_o$		- -	-35 -60	-30 -45	dBc
Second Harmonic Leakage at DCS Output		-	-25	-15	dBm

Table 4. Electrical Characteristics (Continued)

(Peak measurement at 25% duty cycle, 4.6 ms period, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Return Loss	$ S_{11} $	-	13	-	dB
Output Power Isolation ($V_{\text{ramp}} = 0\text{ V}$, $V_{\text{GSM1,2,3}} = 0\text{ V}$)	P_{off}	-	-45	-40	dBm
Noise Power in Rx Band @ $P_{\text{in}} = -1.0\text{ dBm}$ (100 kHz measurement bandwidth) @ $f_o + 20\text{ MHz}$ $f_o = 849\text{ MHz}$	NP	-	-83	-	dBm
Noise Power in Rx Band @ $P_{\text{in}} = 6.0\text{ dBm}$ (100 kHz measurement bandwidth) @ $f_o + 20\text{ MHz}$ $f_o = 849\text{ MHz}$	NP	-	-86	-82	dBm
Stability-Spurious Output ($P_{\text{out}} = 5.0\text{ to }35\text{ dBm}$, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress ($P_{\text{out}} = 5.0\text{ to }35\text{ dBm}$, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			

GSM 900 Section($P_{\text{in}} = -1.0\text{ dBm}$, $V_{\text{GSM1,2,3}} = 3.5\text{ V}$ pulsed, $V_{\text{dB}} = 3.5\text{ V}$, $V_{\text{REG}} = V_{\text{BS}} = 2.8\text{ V}$, $V_{\text{ramp}} = 1.8\text{ V}$ pulsed)

Frequency Range	BW	880	-	915	MHz
Output Power	P_{out}	34.2	35.2	-	dBm
Power Added Efficiency	PAE	48	53	-	%
Output Power @ Low Voltage ($V_{\text{GSM1,2,3}} = 2.8\text{ V}$ pulsed, $V_{\text{dB}} = 2.8\text{ V}$)	P_{out}	32.5	33.4	-	dBm
Power Added Efficiency @ Low Voltage ($V_{\text{GSM1,2,3}} = 2.8\text{ V}$ pulsed, $V_{\text{dB}} = 2.8\text{ V}$)	PAE	48	54	-	%
Harmonic Output $2f_o$ $\geq 3f_o$		- -	-37 -60	-33 -45	dBc
Second Harmonic Leakage at DCS Output (Crosstalk isolation)		-	-28	-15	dBm
Input Return Loss	$ S_{11} $	-	10	-	dB
Output Power Isolation ($V_{\text{ramp}} = 0\text{ V}$, $V_{\text{GSM1,2,3}} = 0\text{ V}$)	P_{off}	-	-45	-40	dBm
Noise Power in Rx Band @ $P_{\text{in}} = -1.0\text{ dBm}$ (100 kHz measurement bandwidth) @ $f_o + 10\text{ MHz}$ ($f_o = 915\text{ MHz}$) @ $f_o + 20\text{ MHz}$ ($f_o = 915\text{ MHz}$)	NP	- -	-80 -81	- -	dBm
Noise Power in Rx Band @ $P_{\text{in}} = 6.0\text{ dBm}$ (100 kHz measurement bandwidth) @ $f_o + 10\text{ MHz}$ ($f_o = 915\text{ MHz}$) @ $f_o + 20\text{ MHz}$ ($f_o = 915\text{ MHz}$)	NP	- -	-84 -86	-77 -81	dBm

Table 4. Electrical Characteristics (Continued)

(Peak measurement at 25% duty cycle, 4.6 ms period, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Stability-Spurious Output ($P_{\text{out}} = 5.0$ to 35 dBm, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress ($P_{\text{out}} = 5.0$ to 35 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			

DCS Section($P_{\text{in}} = 2.0$ dBm, $V_{\text{DCS1,2,3}} = 3.5$ V pulsed, $V_{\text{dB}} = 3.5$ V, $V_{\text{REG}} = 2.8$ V, $V_{\text{ramp}} = 1.8$ V pulsed, $V_{\text{BS}} = 0$ V)

Frequency Range	BW	1710	-	1785	MHz
Output Power	P_{out}	32.5	33.8	-	dBm
Power Added Efficiency	PAE	38	44	-	%
Output Power @ Low Voltage ($V_{\text{DCS1,2,3}} = 2.8$ V pulsed, $V_{\text{dB}} = 2.8$ V)	P_{out}	31	32	-	dBm
Power Added Efficiency @ Low Voltage ($V_{\text{DCS1,2,3}} = 2.8$ V pulsed, $V_{\text{dB}} = 2.8$ V)	PAE	38	45	-	%
Harmonic Output $2f_o$ $\geq 3f_o$		- -	-65 -50	-45 -45	dBc
Input Return Loss	$ S_{11} $	-	9.0	-	dB
Output Power Isolation ($V_{\text{ramp}} = 0$ V, $V_{\text{DCS1,2,3}} = 0$ V)	P_{off}	-	-40	-35	dBm
Noise Power in Rx Band @ $P_{\text{in}} = 2.0$ dBm @ $f_o + 20$ MHz ($f_o = 1785$ MHz) (100 kHz measurement bandwidth)	NP	-	-78	-75	dBm
Stability-Spurious Output ($P_{\text{out}} = 0$ to 33 dBm, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress ($P_{\text{out}} = 0$ to 33 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			

PCS Section($P_{\text{in}} = 3.0$ dBm, $V_{\text{DCS1,2,3}} = 3.5$ V pulsed, $V_{\text{dB}} = 3.5$ V, $V_{\text{REG}} = 2.8$ V, $V_{\text{ramp}} = 1.8$ V pulsed, $V_{\text{BS}} = 0$ V)

Frequency Range	BW	1850	-	1910	MHz
Output Power	P_{out}	32.5	34	-	dBm
Power Added Efficiency	PAE	37	43	-	%
Output Power @ Low Voltage ($V_{\text{DCS1,2,3}} = 2.8$ V pulsed, $V_{\text{dB}} = 2.8$ V)	P_{out}	31	32	-	dBm
Power Added Efficiency @ Low Voltage ($V_{\text{DCS1,2,3}} = 2.8$ V pulsed, $V_{\text{dB}} = 2.8$ V)	PAE	37	43	-	%

Table 4. Electrical Characteristics (Continued)

(Peak measurement at 25% duty cycle, 4.6 ms period, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Harmonic Output $2f_o$ $\geq 3f_o$		- -	-65 -50	-45 -45	dBc
Input Return Loss	$ S_{11} $	-	5.0	-	dB
Output Power Isolation ($V_{\text{ramp}} = 0\text{ V}$, $V_{\text{DCS1,2,3}} = 0\text{ V}$)	P_{off}	-	-35	-32	dBm
Noise Power in Rx Band @ $P_{\text{in}} = 3.0\text{ dBm}$ @ $f_o + 20\text{ MHz}$ ($f_o = 1910\text{ MHz}$) (100 kHz measurement bandwidth)	NP	-	-78	-75	dBm
Stability-Spurious Output ($P_{\text{out}} = 0\text{ to }33\text{ dBm}$, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress ($P_{\text{out}} = 0\text{ to }33\text{ dBm}$, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			

2 Typical Performance Characteristics

2.1 GSM850

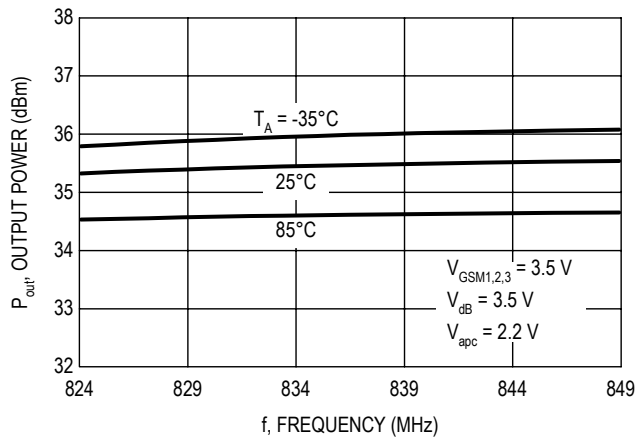


Figure 2. Output Power versus Frequency

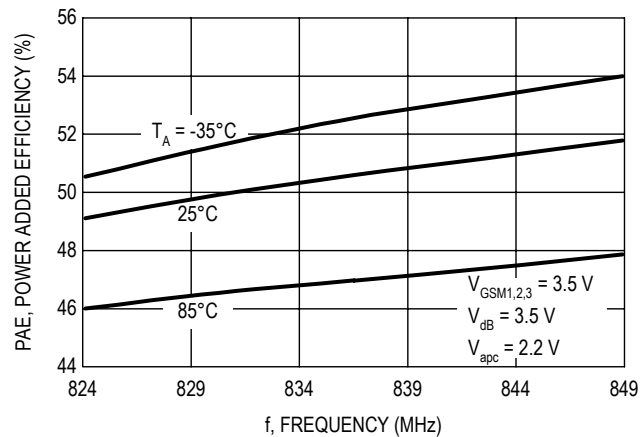


Figure 3. Power Added Efficiency versus Frequency

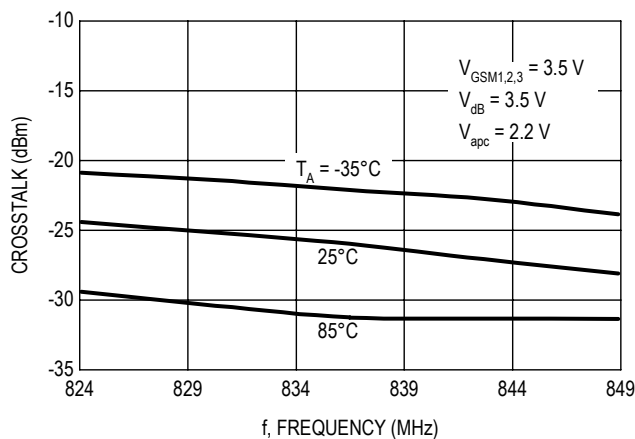


Figure 4. Crosstalk versus Frequency

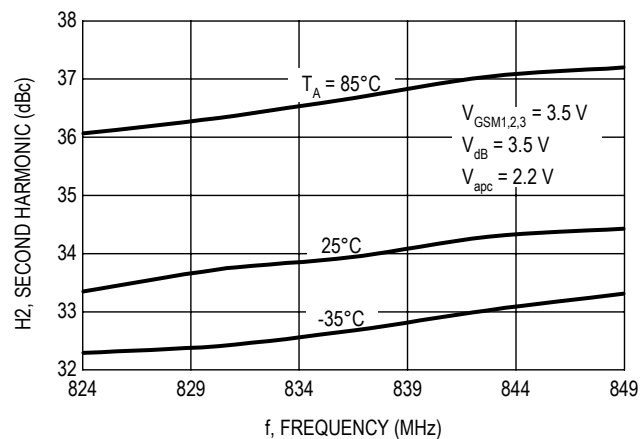


Figure 5. Second Harmonic Output versus Frequency

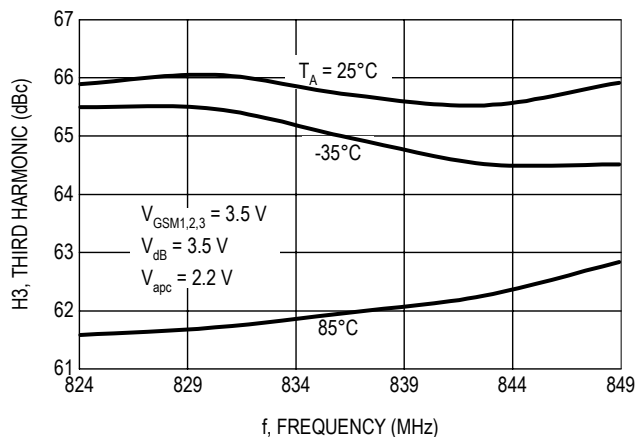


Figure 6. Third Harmonic Output versus Frequency

2.2 GSM900

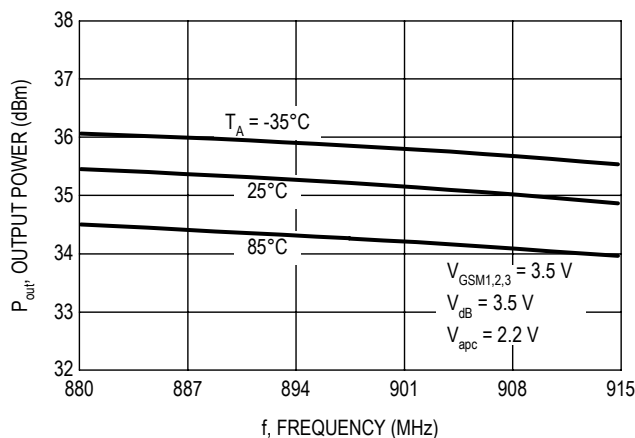


Figure 7. Output Power versus Frequency

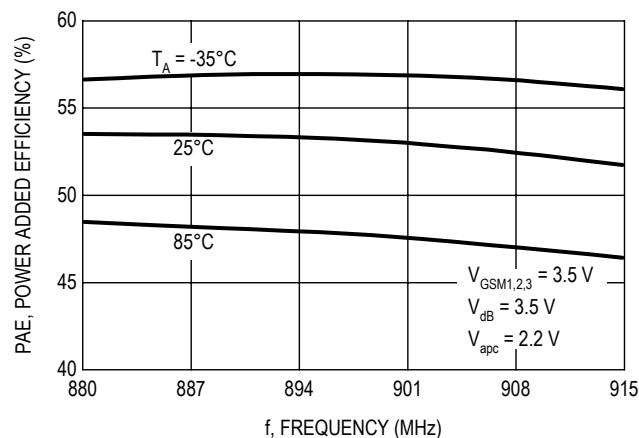


Figure 8. Power Added Efficiency versus Frequency

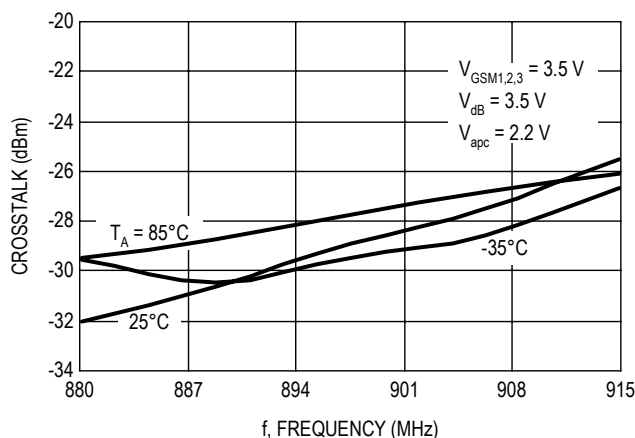


Figure 9. Crosstalk versus Frequency

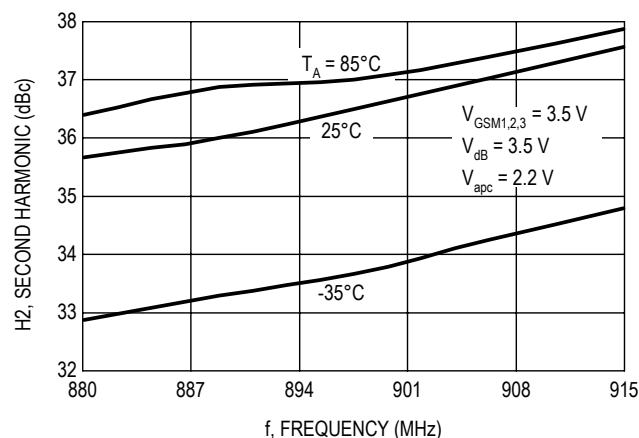


Figure 10. Second Harmonic Output versus Frequency

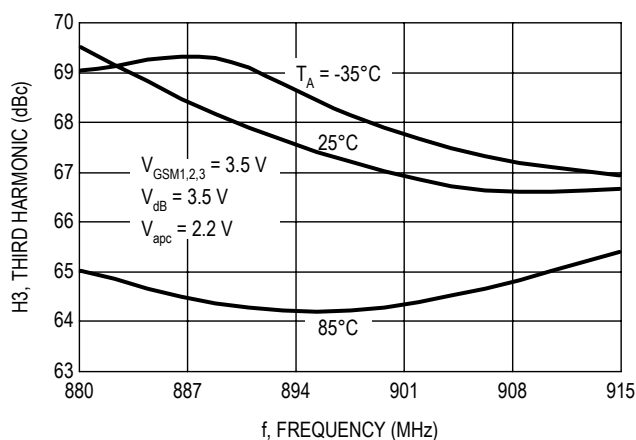


Figure 11. Third Harmonic Output versus Frequency

2.3 DCS

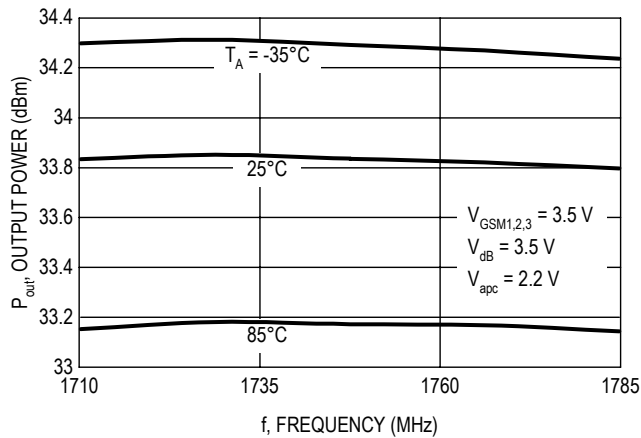


Figure 12. Output Power versus Frequency

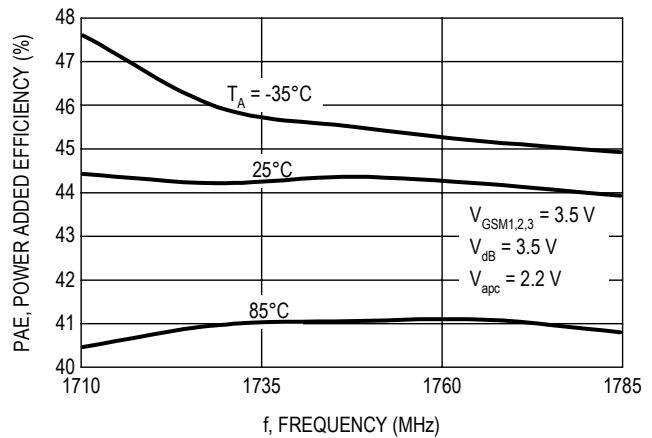


Figure 13. Power Added Efficiency versus Frequency

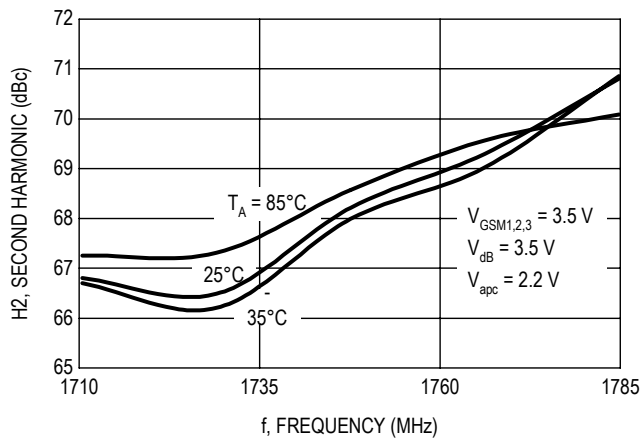


Figure 14. Second Harmonic Output versus Frequency

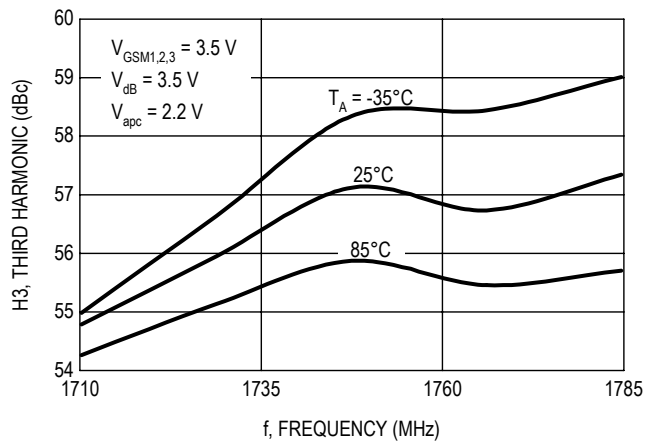


Figure 15. Third Harmonic Output versus Frequency

2.4 PCS

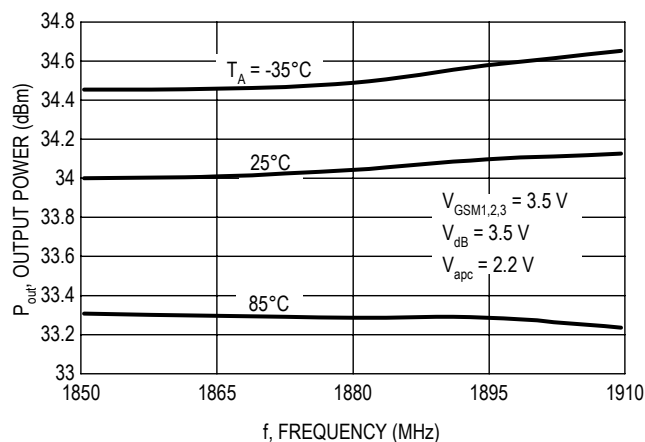


Figure 16. Output Power versus Frequency

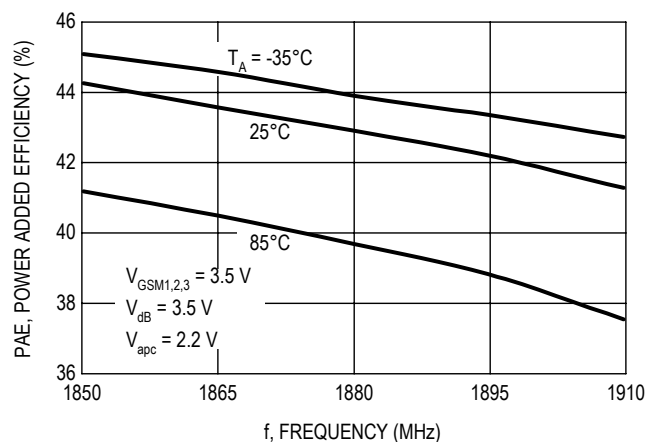


Figure 17. Power Added Efficiency versus Frequency

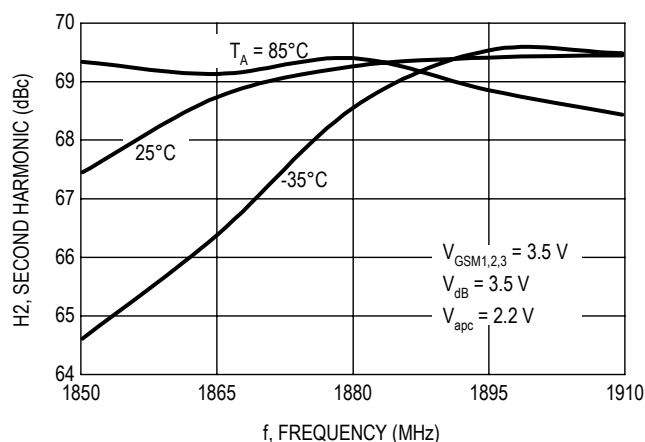


Figure 18. Second Harmonic Output versus Frequency

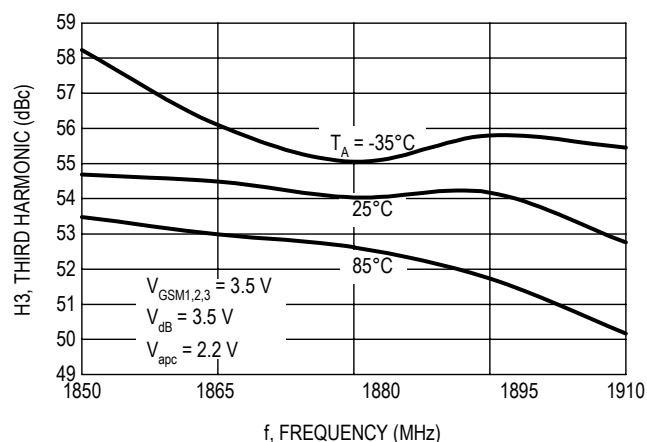
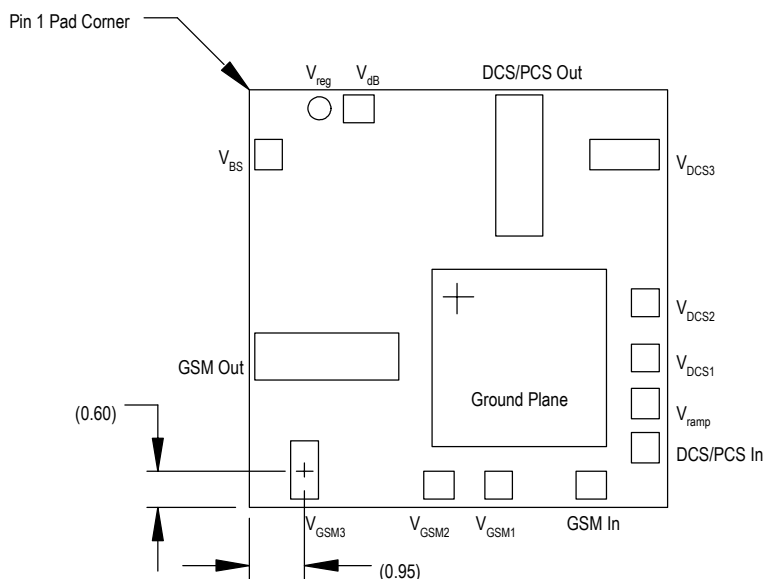


Figure 19. Third Harmonic Output versus Frequency

3 Pin Descriptions and Connections

Table 5. Pin Function Description

Pin	Symbol	Description
1	V_{reg}	Regulated dc voltage for bias circuit
2	V_{dB}	DC supply voltage for active bias circuits connected to the battery
3	DCS/PCS Out	DCS/PCS RF output
4	V_{DCS3}	DCS/PCS DC supply voltage for 3rd stage
5	V_{DCS2}	DCS/PCS DC supply voltage for 2nd stage
6	V_{DCS1}	DCS/PCS DC supply voltage for 1st stage
7	V_{apc}	Power control for both line-ups ($V_{apc} = 0\text{ V}$, $P_{out} = P_{off}$, $V_{apc} = 1.8\text{ V}$, $P_{out} = P_{max}$)
8	DCS/PCS In	DCS/PCS RF input
9	GSM In	GSM850/GSM900 RF input
10	V_{GSM1}	GSM850/GSM900 DC supply voltage for 1st stage
11	V_{GSM2}	GSM850/GSM900 DC supply voltage for 2nd stage
12	V_{GSM3}	GSM850/GSM900 DC supply voltage for 3rd stage
13	GSM Out	GSM850/GSM900 RF output
14	V_{BS}	Band selection between GSM850/GSM900 and DCS/PCS



NOTE: For optimum performance V_{GSM1} and V_{GSM2} , as well as V_{DCS1} and V_{DCS2} , must be strapped together on the application demobard.

Figure 20. Pin Connections
(Bottom View)

4 Application Information

4.1 Power Control Considerations

The MMM5062 is designed for open loop (drain control) applications. A PMOS FET is used to switch the MMM5062 drain and vary the supply voltage from 0 to the battery voltage setting (V_{bat}). The simplified concept schematic (see Figure 27) describes the application circuit used to control the device through the drain voltage.

A drain control provides a linear transfer function which is repeatable versus control voltage (see Figure 21).

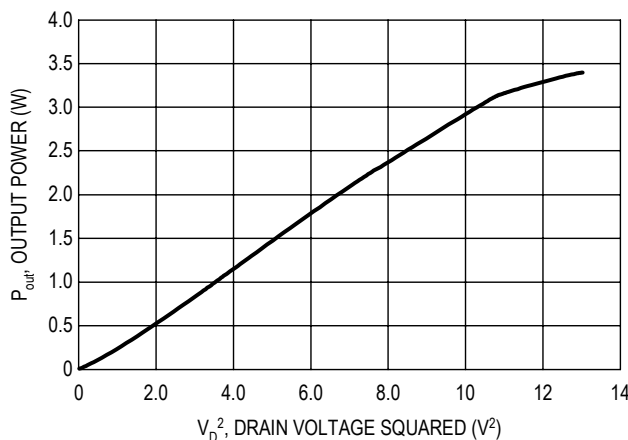


Figure 21. Output Power versus Drain Voltage

4.2 GSM Second Harmonic (H2) Trap Circuitry

When transmitting in GSM saturated mode, the second harmonic is naturally present at the RF output of the PA and reaches the antenna after additional filtering in the front-end. ETSI specifies that harmonic level cannot exceed -36 dBm. In order to improve H2 rejection in low Band (GSM850/GSM900), an H2 trap has been developed. The topology is based on a Low Pass π Cell Filter (see Figure 22) where the first shunt capacitor is actually part of the PA output match.

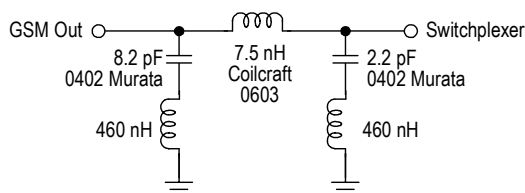
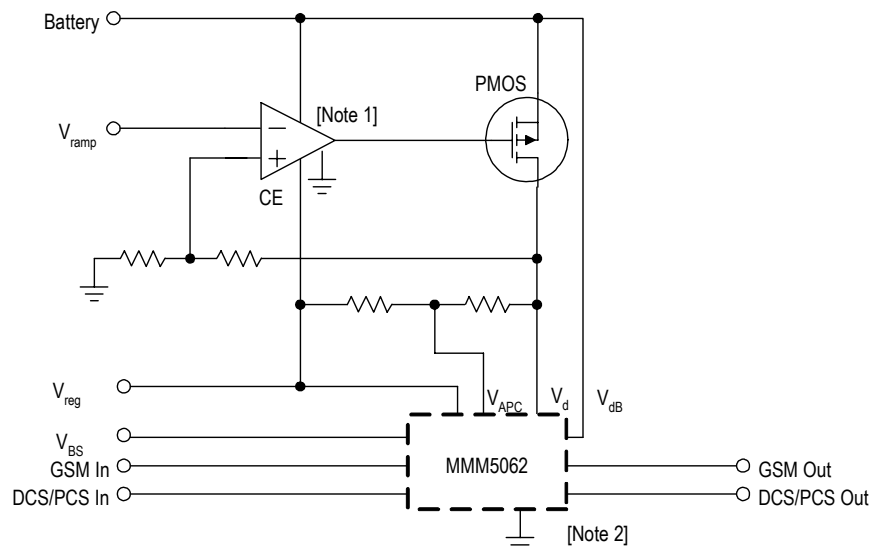


Figure 22. Low Pass Filter

This circuit reduces H2 level by 7 to 8 dB with low in-band insertion losses (mainly due to the series inductor). Moreover, this structure can be used to match Power amplifier module output to the switchplexer.

4.3 Application Schematics and Printed Circuit Boards



- NOTES:**
1. Op/Amp is either external (with an enable pin CE) or in an ASIC.
 2. The MMM5062 requires 4 to 6 RF/LF decoupling capacitors (not shown).

Figure 23. Open Loop Control Application Schematic

Figure 23 represents the complete Power Amplifier implementation including the MMM5062 Amplifier Module and the Control Circuitry. This functionality is realized with two separate printed circuit boards; the PA Evaluation Circuit with schematic shown in Figure 26 and PCB Layout shown in Figure 28, and the Power Amplifier Control Loop with schematic shown in Figure 27 and PCB Layout shown in Figure 29.

The PA Evaluation Circuit is straightforward and, due to the MMM5062's high level of integration, requires only a few passive components around the package. These components are mainly de-coupling capacitors.

The Power Amplifier Control Loop is based on an operational amplifier driving a PMOS transistor. The PMOS device functions as a linear drain voltage regulator controlled by V_{ramp} with a typical gain of 2 which is set through the resistive divider R4 and R5 as shown in Figure 27. To control output power through the drain, V_{apc} must be indexed to the drain voltage to prevent the PA Section from drawing excessive current especially at low output power. Nevertheless, V_{apc} should stay above 0.8 V to provide sufficient gain for the line-up. Figure 24 describes the application circuit used to control V_{apc} through the drain voltage. It uses V_{reg} to pre-position V_{apc} at 0.9 V and add a voltage which is dependent on the drain Voltage.

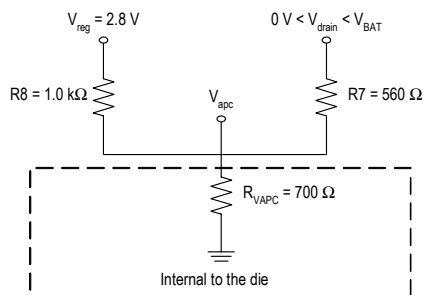


Figure 24.

R8 and $R_{V_{apc}}$ set V_{apc} at 0.9 V while R7 sets the V_{apc} slope. V_{apc} versus V_{drain} is shown in the Figure 25.

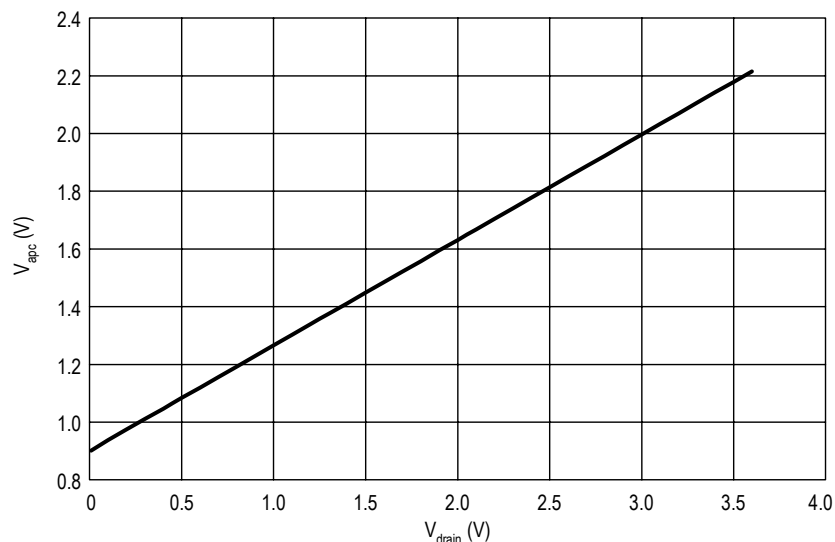


Figure 25. V_{apc} versus V_{drain}

It is possible that the Power Control DAC output voltage can be in the 200 mV to 2.0 V range. This raises a concern for the MMM5062 ramp control voltage (V_{ramp}) which must start at 0 V to get enough output power dynamic range. To overcome this limitation, a resistor (R6 in Figure 27) is used to set an additional offset (200 mV with $R6 = 39 \text{ k}\Omega$). This residual voltage is then subtracted the DAC output voltage through the differential Operational Amplifier.

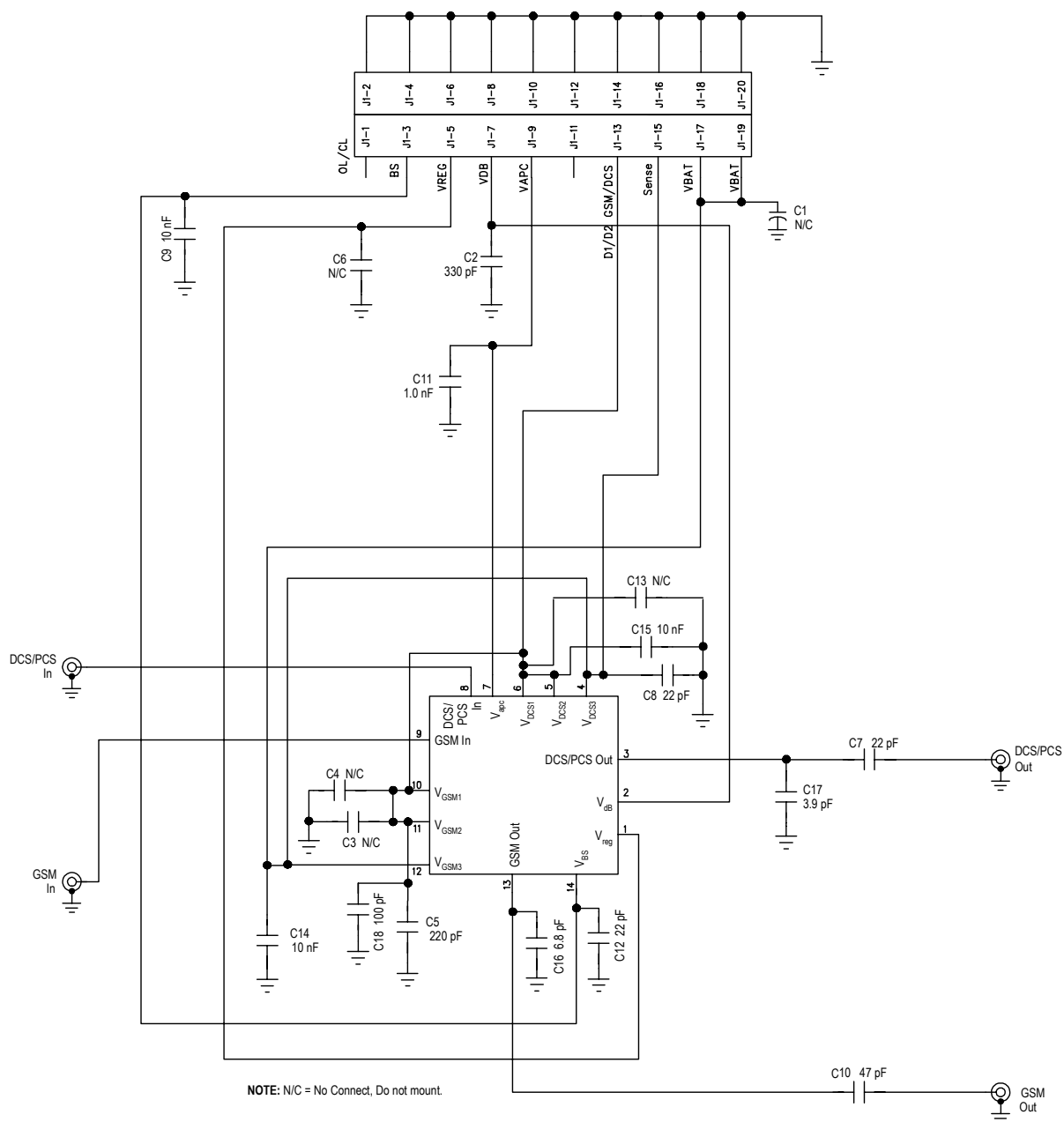


Figure 26. PA Evaluation Circuit

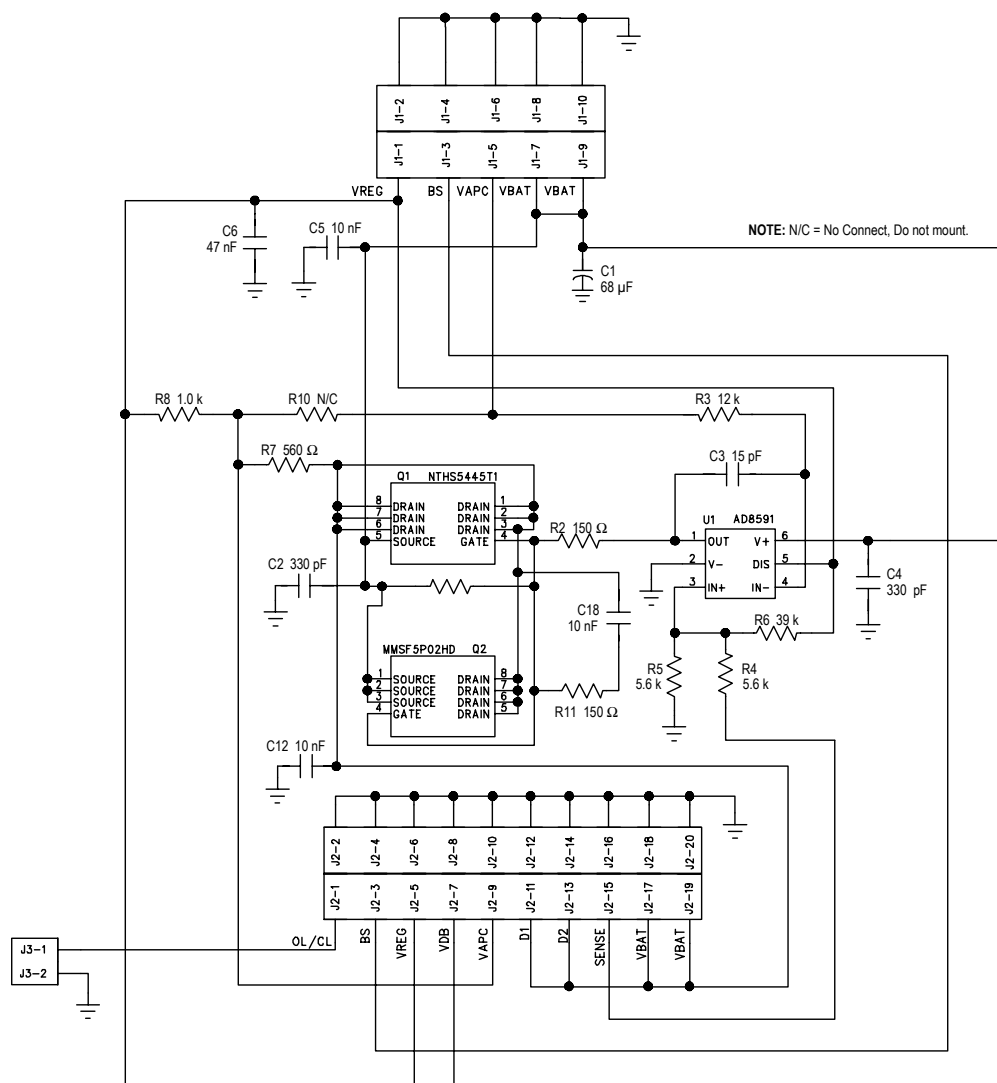


Figure 27. Power Amplifier Control Loop

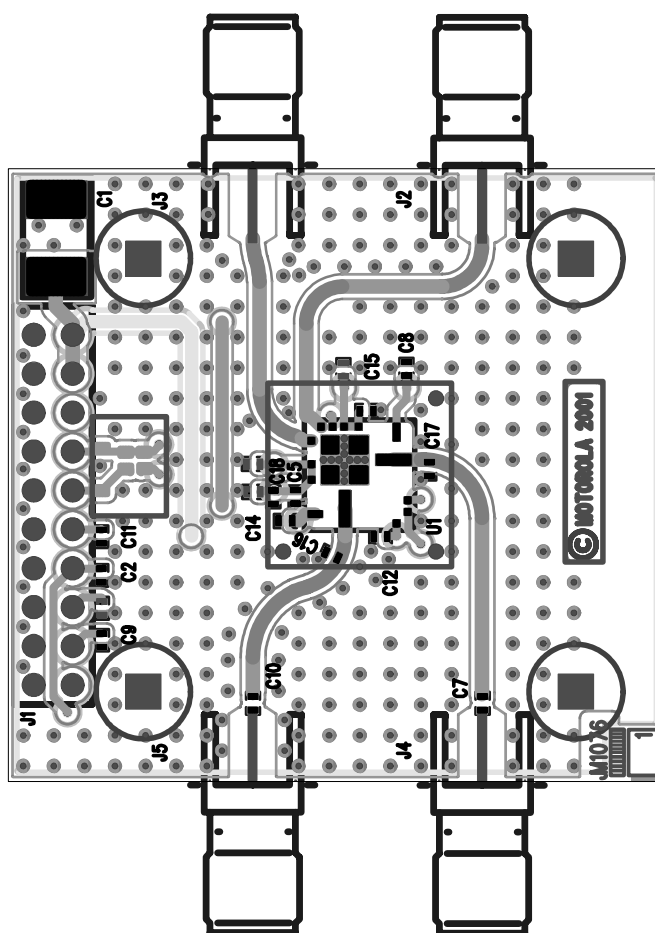


Figure 28. PA Evaluation Circuit PCB

Table 6. PA Evaluation Circuit PCB Bill of Materials

Reference	Value	Part Number	Manufacturer
C1, C3, C4, C6, C13	N/C - Do not mount		
C2	330 pF	GRM36COG330J50	Murata
C5	220 pF	GRM36X7R221K50	Murata
C7, C8, C12	22 pF	GRM36COG220J50	Murata
C9, C14, C15	10 nF	GRM36X7R103K25	Murata
C10	47 pF	GRM36COG470J50	Murata
C11	1.0 nF	GRM36X7R102K25	Murata
C16	6.8 pF	GRM36COG6R8J50	Murata
C17	3.9 pF	GRM36COG3R9J50	Murata
C18	100 nF	GRM36X7R104K25	Murata
J2, J3, J4, J5	50 Ω	142-0711-821	Johnson

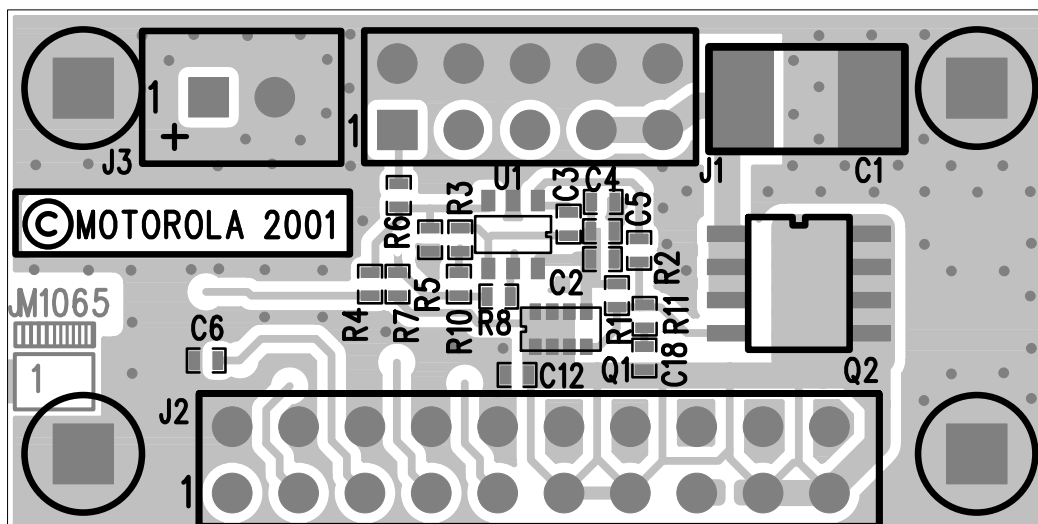


Figure 29. Power Amplifier Control Loop PCB

Table 7. Power Amplifier Control Loop PCB Bill of Materials

Reference	Value	Part Number	Manufacturer
C1	68 μ F	293D685X9020C	Sprague
C2	330 pF	GRM36COG330J50	Murata
C3	15 pF	GRM36COG150J50	Murata
C4	330 pF	GRM36x7R331K50	Murata
C5, C12, C18	10 nF	GRM36X7R103K25	Murata
C6	47 nF	GRM36X7R473K10	Murata
J1, J2, J3	DC connector		
Q1	Power MOSFET	NTHS5445T	ON Semiconductor
Q2	N/C - Do not mount		
R1, R8	1.0 k	CRG0402 5% 1 kO	NEOHM
R2	150 Ω	CRG0402 5% 150 O	NEOHM
R3	12 k	CRG0402 5% 12 kO	NEOHM
R4, R5	5.6 k	CRG0402 5% 5.6 kO	NEOHM
R6, R10	N/C - Do not mount		
R7	560 Ω	CRG0402 5% 560 O	NEOHM
R11	100 Ω	CRG0402 5% 100 O	NEOHM
U1	CMOS Op Amp	AD8591	Analog Devices

5 Packaging Information

Shipping, Packaging and Marking Information

Tape Width: 16.0 mm

Tape Pitch 12 mm (part to part)

Reel Diameter: 330 mm (13 in)

Component Orientation: Parts are to be orientated with pin 1 side closest to the tape's round sprocket holes on the tape's trailing edge.

Dry Pack: This device meets Moisture Sensitivity Level (MSL) 3. Parts will be shipped in Dry Pack. Parts must be stored at 30°C and 60% relative humidity with time out of dry pack not to exceed 168 hours.

In the event that parts are not handled or stored within these limits, one of the following dry out procedures must be completed prior to reflow:

1) 40°C Dry Out: Bake devices at $40^{\circ}\text{C} \leq T_A \leq 45^{\circ}\text{C}$, 5% Relative Humidity for at least 192 hours.

2) Room Temperature Dry Out: Store devices at less than 20% Relative Humidity for at least 500 hours.

Marking:

1st line: Motorola Logo

2nd Line: Partnumber coded on 7 characters

3rd Line: Wafer lot number (coded on 6 characters) followed by wafer number (coded on 3 digits)

4th Line: Assy site code (on 1 or 2 characters), followed by Wafer Lot Number (coded on 1 or 2 characters), followed by Year (on 2 digits) and Workweek (on 2 digits).

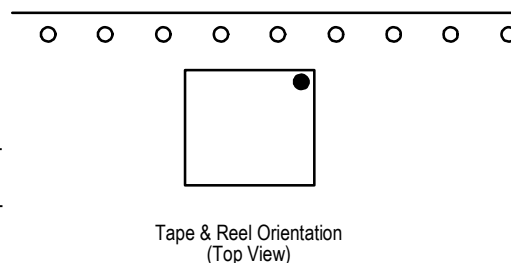
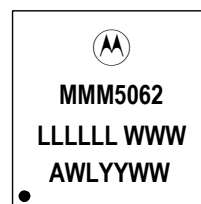


Figure 30. Packaging Information

Advance Information

MMM5063/D
Rev. 0, 12/2002

Tri-Band GSM GPRS
3.5 V Power Amplifier



MOTOROLA
intelligence everywhere™

digital dna™

MMM5063



(Scale 1:1)

Package Information

Plastic Package

Case 1383

(Module, 7x7 mm)

Ordering Information

Device	Device Marking	Package
MMM5063	See Figure 25	Module

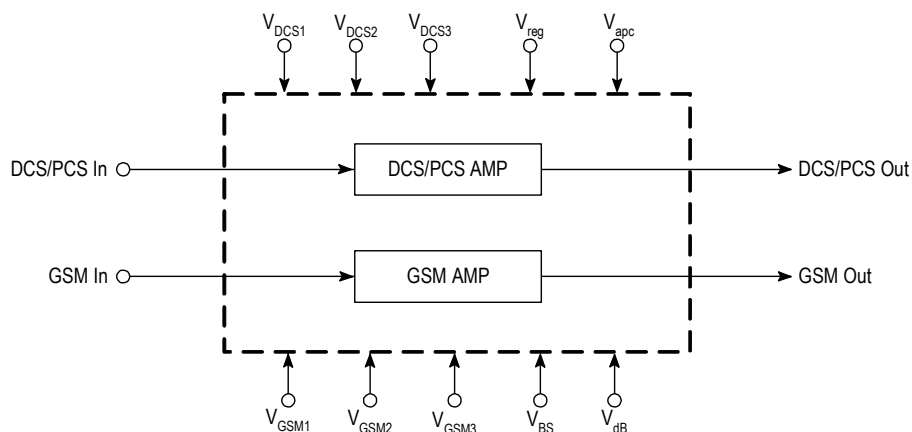
The MMM5063 is a tri-band single supply RF Power Amplifier for GSM900/DCS1800/PCS1900 GPRS handheld radios. This fully integrated Power Amplifier uses a patented concept to realize the 50 Ω matching on-chip through integration of passives on the GaAs die. This allows module functionality in a very small 7 x 7 mm package and achieves best-in-class Power Amplifier performance and multi-band capability.

Applications:

- Tri-Band GSM900 DCS1800 and PCS1900
- Guaranteed for Class 10 GPRS

Features:

- Single Supply Enhancement Mode GaAs MESFET Technology
- Internal 50 Ω Input/Output Matching
- High Gain Three Stage Amplifier Design
- Typical 3.5 V Characteristics:
 - $P_{out} = 35.2$ dBm, PAE = 53% for GSM
 - $P_{out} = 33.8$ dBm, PAE = 44% for DCS
 - $P_{out} = 34$ dBm, PAE = 43% for PCS
- Optimized and Guaranteed for Open-Loop Power Control Applications
- Small 7 x 7 mm Package



This device contains 26 active transistors.

Figure 1. Simplified Block Diagram

1 Electrical Specifications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	$V_{GSM1,2,3}, V_{DCS1,2,3}, V_{dB}$	6.0	V
RF Input Power	GSM IN, DCS/PCS IN	11	dBm
RF Output Power GSM Section DCS/PCS Section	GSM OUT DCS/PCS OUT	38 36	dBm
Operating Case Temperature Range	T_C	-35 to 100	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C
Die Temperature	T_J	150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤ 150 V and Machine Model (MM) ≤ 50 V. Additional ESD data available upon request.
3. Meets Moisture Sensitivity Level (MSL) 3. See Figure 25 on page 93 for additional details.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	$V_{GSM1,2,3}$, $V_{DCS1,2,3}$	2.7	-	5.5	V
Bias Supply Voltage	V_{dB}	2.7	-	5.5	V
Regulated Voltage	V_{REG}	2.5	2.8	3.0	V
Power Control Voltage	V_{apc}	0	1.8	2.8	V
Band Select	V_{BS}	0	2.8	3.0	V
Input Power GSM	GSM IN	-1.0	-	8.0	dBm
Input Power DCS/PCS	DCS/PCS IN	2.0	-	10	dBm

Table 3. Control Requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Current for V_{reg} @ 2.8 V	I_{reg}	-	7.7	10	mA
Band Select Low Band Enable Voltage High Band Enable Voltage	V_{BS}	2.2 0	2.8 -	- 0.3	V
Current for $V_{BS} = 2.8$ V	I_{BS}	-	0.76	1.0	mA

Table 4. Electrical Characteristics

(Peak measurement at 25% duty cycle, 4.6 ms period, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
GSM 900 Section ($P_{in} = -1.0$ dBm, $V_{GSM1,2,3} = 3.5$ V pulsed, $V_{dB} = 3.5$ V, $V_{REG} = V_{BS} = 2.8$ V, $V_{ramp} = 1.8$ V pulsed)					
Frequency Range	BW	880	-	915	MHz
Output Power	P_{out}	34.2	35.2	-	dBm
Power Added Efficiency	PAE	48	53	-	%
Output Power @ Low Voltage ($V_{GSM1,2,3} = 2.8$ V pulsed, $V_{dB} = 2.8$ V)	P_{out}	32.5	33.4	-	dBm
Power Added Efficiency @ Low Voltage ($V_{GSM1,2,3} = 2.8$ V pulsed, $V_{dB} = 2.8$ V)	PAE	48	54	-	%
Harmonic Output $2f_o$ $\geq 3f_o$		- -	-37 -60	-33 -45	dBc

Table 4. Electrical Characteristics (Continued)

(Peak measurement at 25% duty cycle, 4.6 ms period, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Second Harmonic Leakage at DCS Output (Crosstalk isolation)		-	-28	-15	dBm
Input Return Loss	$ S_{11} $	-	10	-	dB
Output Power Isolation ($V_{\text{ramp}} = 0\text{ V}$, $V_{\text{GSM1,2,3}} = 0\text{ V}$)	P_{off}	-	-45	-40	dBm
Noise Power in Rx Band @ $P_{\text{in}} = -1.0\text{ dBm}$ (100 kHz measurement bandwidth) @ $f_o + 10\text{ MHz}$ ($f_o = 915\text{ MHz}$) @ $f_o + 20\text{ MHz}$ ($f_o = 915\text{ MHz}$)	NP	- -	-80 -81	- -	dBm
Noise Power in Rx Band @ $P_{\text{in}} = 6.0\text{ dBm}$ (100 kHz measurement bandwidth) @ $f_o + 10\text{ MHz}$ ($f_o = 915\text{ MHz}$) @ $f_o + 20\text{ MHz}$ ($f_o = 915\text{ MHz}$)	NP	- -	-84 -86	-77 -81	dBm
Stability-Spurious Output ($P_{\text{out}} = 5.0\text{ to }35\text{ dBm}$, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress ($P_{\text{out}} = 5.0\text{ to }35\text{ dBm}$, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			

DCS Section ($P_{\text{in}} = 2.0\text{ dBm}$, $V_{\text{DCS1,2,3}} = 3.5\text{ V}$ pulsed, $V_{\text{dB}} = 3.5\text{ V}$, $V_{\text{REG}} = 2.8\text{ V}$, $V_{\text{ramp}} = 1.8\text{ V}$ pulsed, $V_{\text{BS}} = 0\text{ V}$)

Frequency Range	BW	1710	-	1785	MHz
Output Power	P_{out}	32.5	33.8	-	dBm
Power Added Efficiency	PAE	38	44	-	%
Output Power @ Low Voltage ($V_{\text{DCS1,2,3}} = 2.8\text{ V}$ pulsed, $V_{\text{dB}} = 2.8\text{ V}$)	P_{out}	31	32	-	dBm
Power Added Efficiency @ Low Voltage ($V_{\text{DCS1,2,3}} = 2.8\text{ V}$ pulsed, $V_{\text{dB}} = 2.8\text{ V}$)	PAE	38	45	-	%
Harmonic Output $2f_o$ $\geq 3f_o$		- -	-65 -50	-45 -45	dBc
Input Return Loss	$ S_{11} $	-	9.0	-	dB
Output Power Isolation ($V_{\text{ramp}} = 0\text{ V}$, $V_{\text{DCS1,2,3}} = 0\text{ V}$)	P_{off}	-	-40	-35	dBm
Noise Power in Rx Band @ $P_{\text{in}} = 2.0\text{ dBm}$ @ $f_o + 20\text{ MHz}$ ($f_o = 1785\text{ MHz}$) (100 kHz measurement bandwidth)	NP	-	-78	-75	dBm
Stability-Spurious Output ($P_{\text{out}} = 0\text{ to }33\text{ dBm}$, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc

Table 4. Electrical Characteristics (Continued)

(Peak measurement at 25% duty cycle, 4.6 ms period, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Load Mismatch Stress ($P_{\text{out}} = 0$ to 33 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			

PCS Section ($P_{\text{in}} = 3.0$ dBm, $V_{\text{DCS1,2,3}} = 3.5$ V pulsed, $V_{\text{dB}} = 3.5$ V, $V_{\text{REG}} = 2.8$ V, $V_{\text{ramp}} = 1.8$ V pulsed, $V_{\text{BS}} = 0$ V)

Frequency Range	BW	1850	-	1910	MHz
Output Power	P_{out}	32.5	34	-	dBm
Power Added Efficiency	PAE	37	43	-	%
Output Power @ Low Voltage ($V_{\text{DCS1,2,3}} = 2.8$ V pulsed, $V_{\text{dB}} = 2.8$ V)	P_{out}	31	32	-	dBm
Power Added Efficiency @ Low Voltage ($V_{\text{DCS1,2,3}} = 2.8$ V pulsed, $V_{\text{dB}} = 2.8$ V)	PAE	37	43	-	%
Harmonic Output $2f_o$ $\geq 3f_o$		- -	-65 -50	-45 -45	dBc
Input Return Loss	$ S_{11} $	-	5.0	-	dB
Output Power Isolation ($V_{\text{ramp}} = 0$ V, $V_{\text{DCS1,2,3}} = 0$ V)	P_{off}	-	-35	-32	dBm
Noise Power in Rx Band @ $P_{\text{in}} = 3.0$ dBm @ $f_o + 20$ MHz ($f_o = 1910$ MHz) (100 kHz measurement bandwidth)	NP	-	-78	-75	dBm
Stability-Spurious Output ($P_{\text{out}} = 0$ to 33 dBm, Load VSWR = 6:1 all Phase Angles, Adjust V_{ramp} for specified power)	P_{spur}	-	-	-60	dBc
Load Mismatch Stress ($P_{\text{out}} = 0$ to 33 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust V_{ramp} for specified power)		No Degradation in Output Power Before and After Test			

2 Typical Performance Characteristics

2.1 GSM

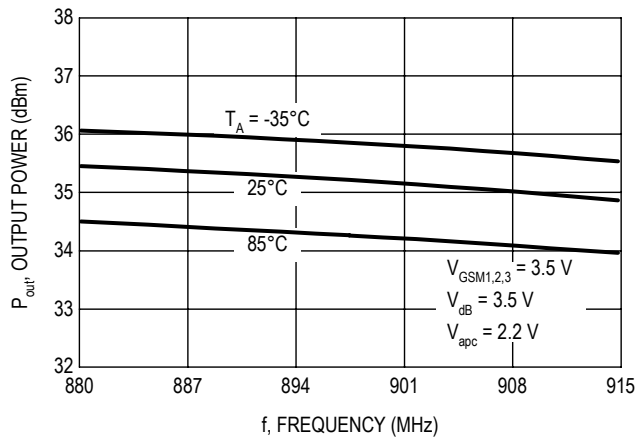


Figure 2. Output Power versus Frequency

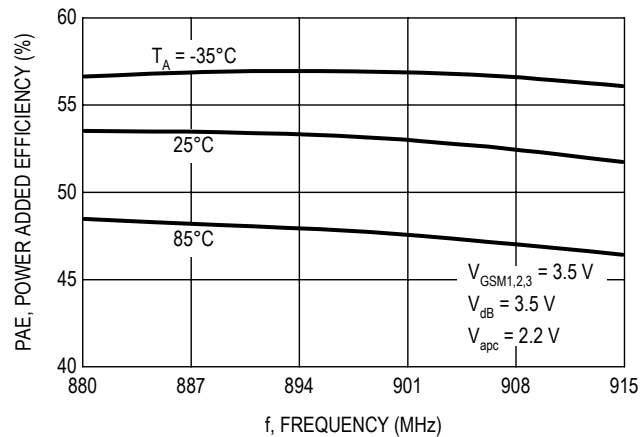


Figure 3. Power Added Efficiency versus Frequency

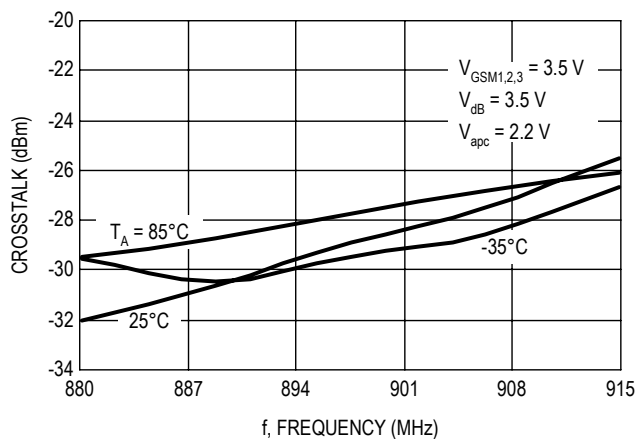


Figure 4. Crosstalk versus Frequency

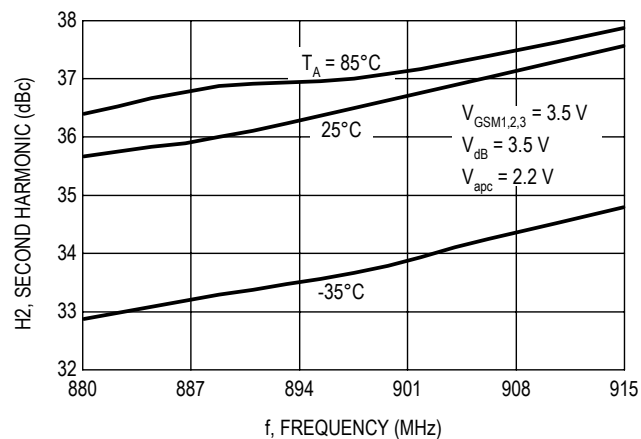


Figure 5. Second Harmonic Output versus Frequency

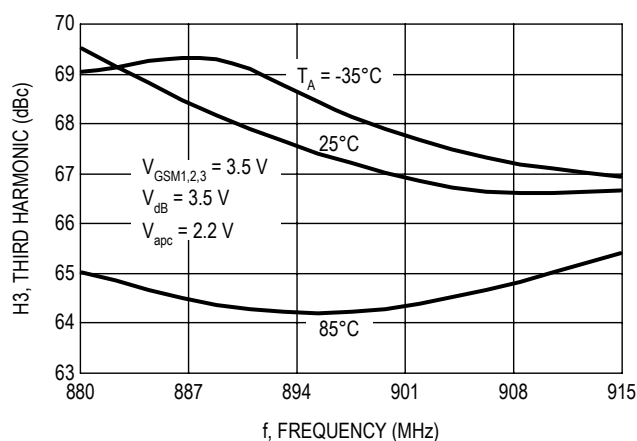


Figure 6. Third Harmonic Output versus Frequency

2.2 DCS

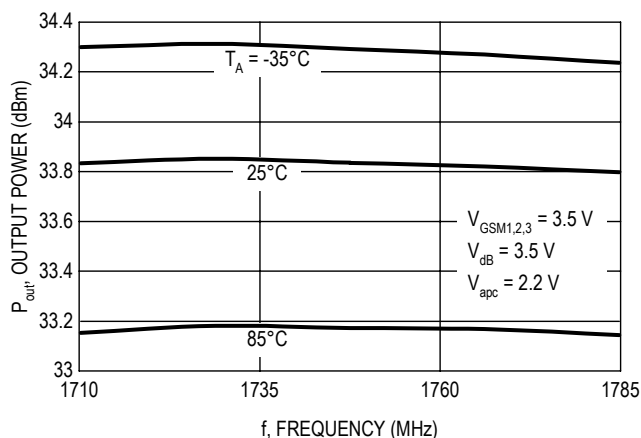


Figure 7. Output Power versus Frequency

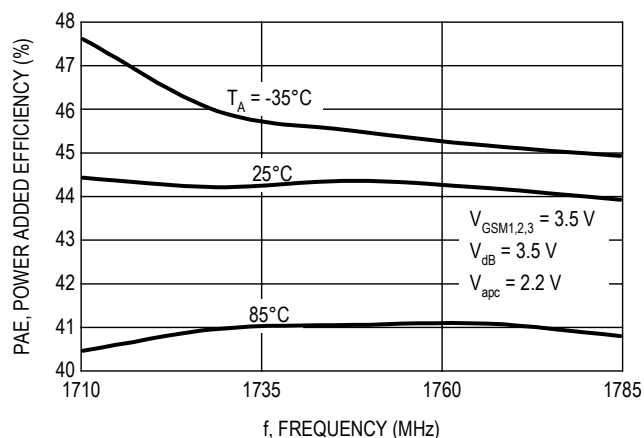


Figure 8. Power Added Efficiency versus Frequency

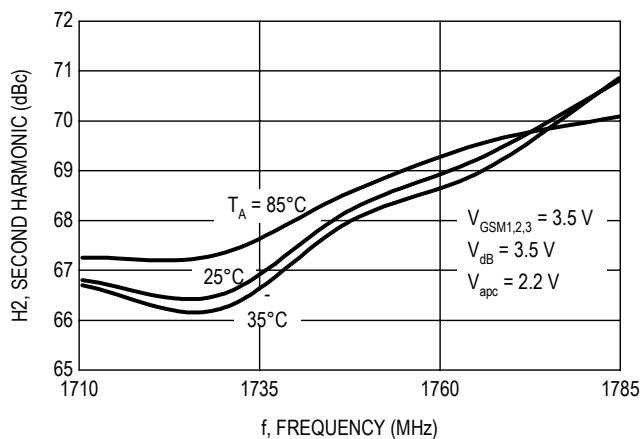


Figure 9. Second Harmonic Output versus Frequency

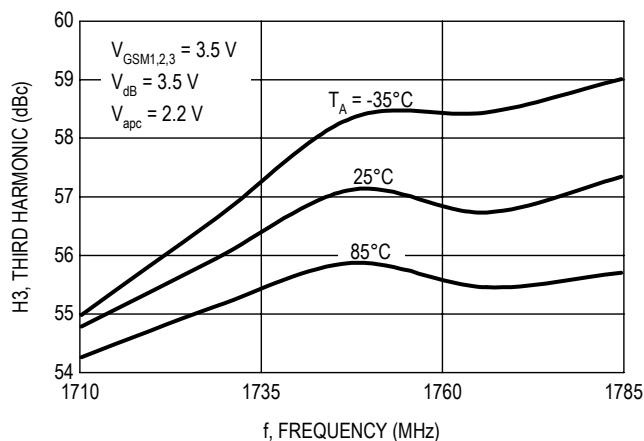


Figure 10. Third Harmonic Output versus Frequency

2.3 PCS

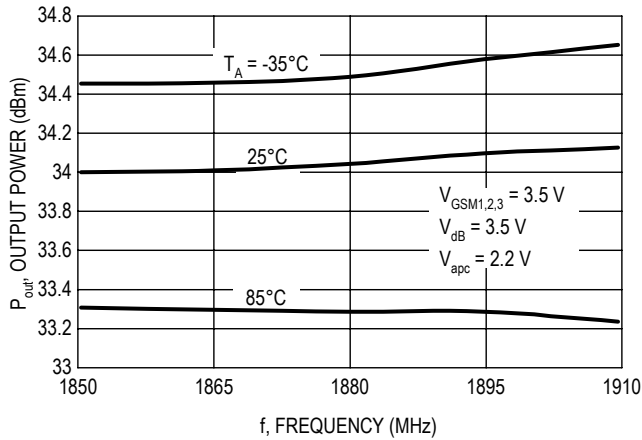


Figure 11. Output Power versus Frequency

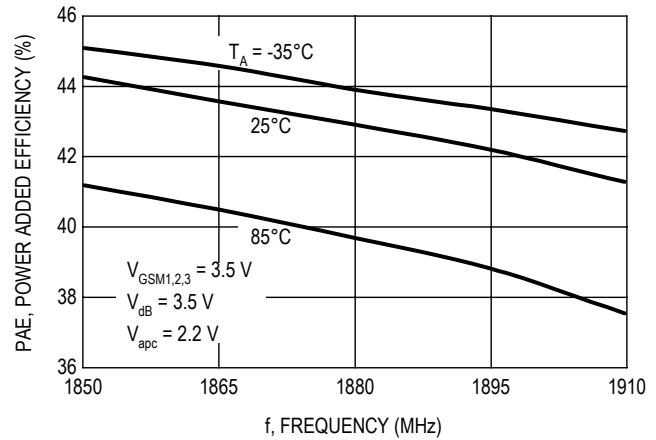


Figure 12. Power Added Efficiency versus Frequency

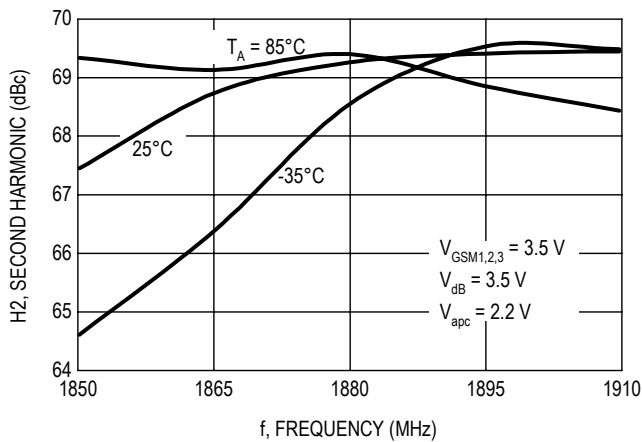


Figure 13. Second Harmonic Output versus Frequency

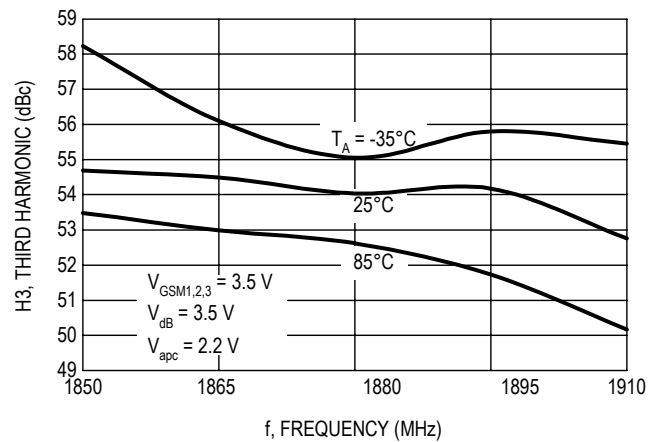
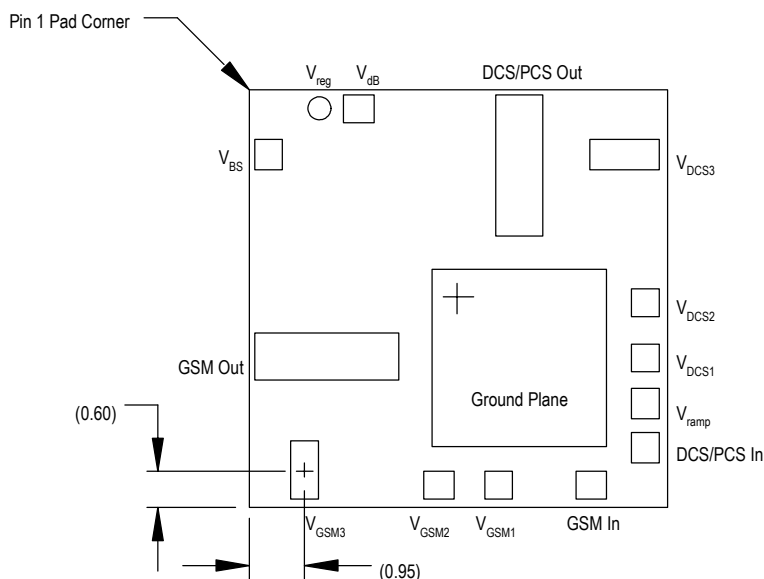


Figure 14. Third Harmonic Output versus Frequency

3 Contact Descriptions and Connections

Table 5. Contact Function Description

Pin	Symbol	Description
1	V_{reg}	Regulated dc voltage for bias circuit
2	V_{dB}	DC supply voltage for active bias circuits connected to the battery
3	DCS/PCS Out	DCS/PCS RF output
4	V_{DCS3}	DCS/PCS DC supply voltage for 3rd stage
5	V_{DCS2}	DCS/PCS DC supply voltage for 2nd stage
6	V_{DCS1}	DCS/PCS DC supply voltage for 1st stage
7	V_{apc}	Power control for both line-ups ($V_{apc} = 0\text{ V}$, $P_{out} = P_{off}$, $V_{apc} = 1.8\text{ V}$, $P_{out} = P_{max}$)
8	DCS/PCS In	DCS/PCS RF input
9	GSM In	GSM RF input
10	V_{GSM1}	GSM DC supply voltage for 1st stage
11	V_{GSM2}	GSM DC supply voltage for 2nd stage
12	V_{GSM3}	GSM DC supply voltage for 3rd stage
13	GSM Out	GSM RF output
14	V_{BS}	Band selection between GSM and DCS/PCS



NOTE: For optimum performance V_{GSM1} and V_{GSM2} , as well as V_{DCS1} and V_{DCS2} , must be strapped together on the application demobard.

Figure 15. Contact Connections
(Bottom View)

4 Application Information

4.1 Power Control Considerations

The MMM5063 is designed for open loop (drain control) applications. A PMOS FET is used to switch the MMM5063 drain and vary the supply voltage from 0 to the battery voltage setting (V_{bat}). The simplified concept schematic (see Figure 22) describes the application circuit used to control the device through the drain voltage.

A drain control provides a linear transfer function which is repeatable versus control voltage (see Figure 16).

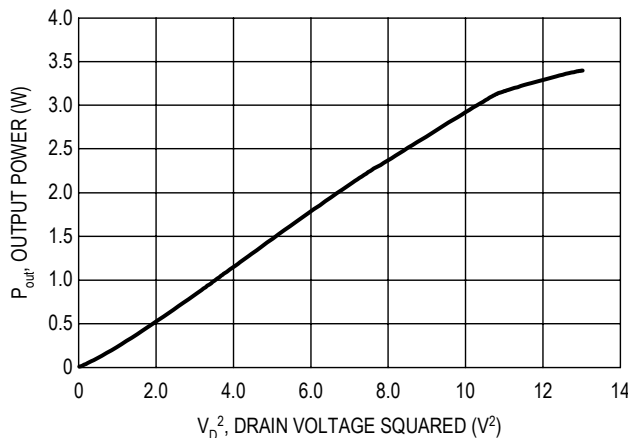


Figure 16. Output Power versus Drain Voltage

4.2 GSM Second Harmonic (H2) Trap Circuitry

When transmitting in GSM saturated mode, the second harmonic is naturally present at the RF output of the PA and reaches the antenna after additional filtering in the front-end. ETSI specifies that harmonic level cannot exceed -36 dBm. In order to improve H2 rejection in low Band (GSM), an H2 trap has been developed. The topology is based on a Low Pass π Cell Filter (see Figure 17) where the first shunt capacitor is actually part of the PA output match.

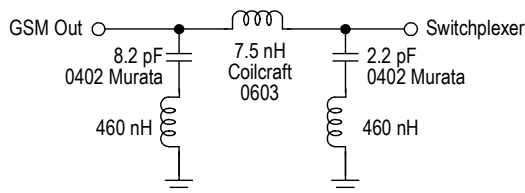


Figure 17. Low Pass Filter

This circuit reduces H2 level by 7 to 8 dB with low in-band insertion losses (mainly due to the series inductor). Moreover, this structure can be used to match Power amplifier module output to the switchplexer.

	PMOS	
--	------	--

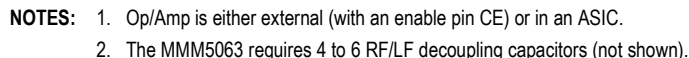


Figure 18 represents the complete Power Amplifier implementation including the MMM5063 Amplifier Module and the Control Circuitry. This functionality is realized with two separate printed circuit boards; the PA Evaluation Circuit with schematic shown in Figure 21 and PCB Layout shown in Figure 23, and the Power Amplifier Control Loop with schematic shown in Figure 22 and PCB Layout shown in Figure 24.

The Power Amplifier Control Loop is based on an operational amplifier driving a PMOS transistor. The PMOS device functions as a linear drain voltage regulator controlled by V_{ramp} with a typical gain of 2 which is set through the resistive divider R4 and R5 as shown in Figure 22. To control output power through the drain, V_{apc} must be indexed to the drain voltage to prevent the PA Section from drawing excessive current especially at low output power. Nevertheless, V_{apc} should stay above 0.8 V to provide sufficient gain for the line-up. Figure 19 describes the application circuit used to control V_{apc} through the drain voltage. It uses V_{reg} to pre-position V_{apc} at 0.9 V and add a voltage which is dependent on the drain Voltage.



R8 and $R_{V_{apc}}$ set V_{apc} at 0.9 V while R7 sets the V_{apc} slope. V_{apc} versus V_{drain} is shown in the Figure 20.

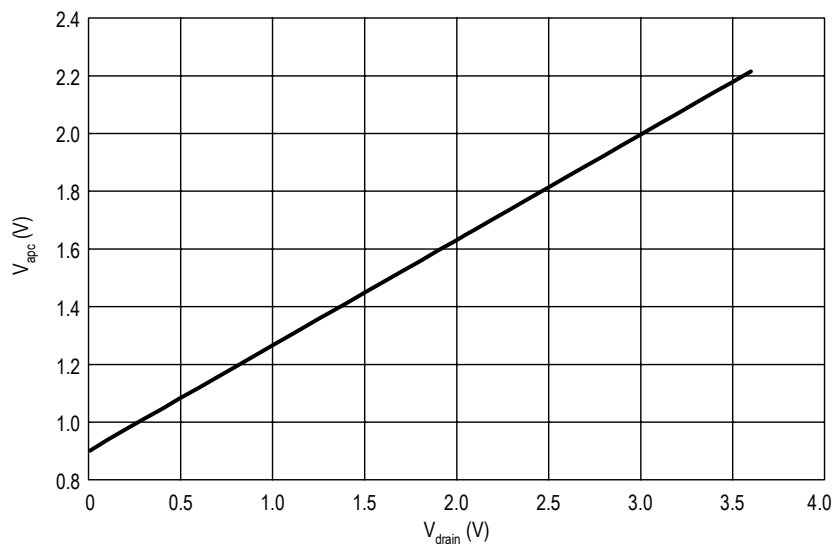


Figure 20. V_{apc} versus V_{drain}

It is possible that the Power Control DAC output voltage can be in the 200 mV to 2.0 V range. This raises a concern for the MMM5063 ramp control voltage (V_{ramp}) which must start at 0 V to get enough output power dynamic range. To overcome this limitation, a resistor (R6 in Figure 22) is used to set an additional offset (200 mV with $R6 = 39 \text{ k}\Omega$). This residual voltage is then subtracted the DAC output voltage through the differential Operational Amplifier.

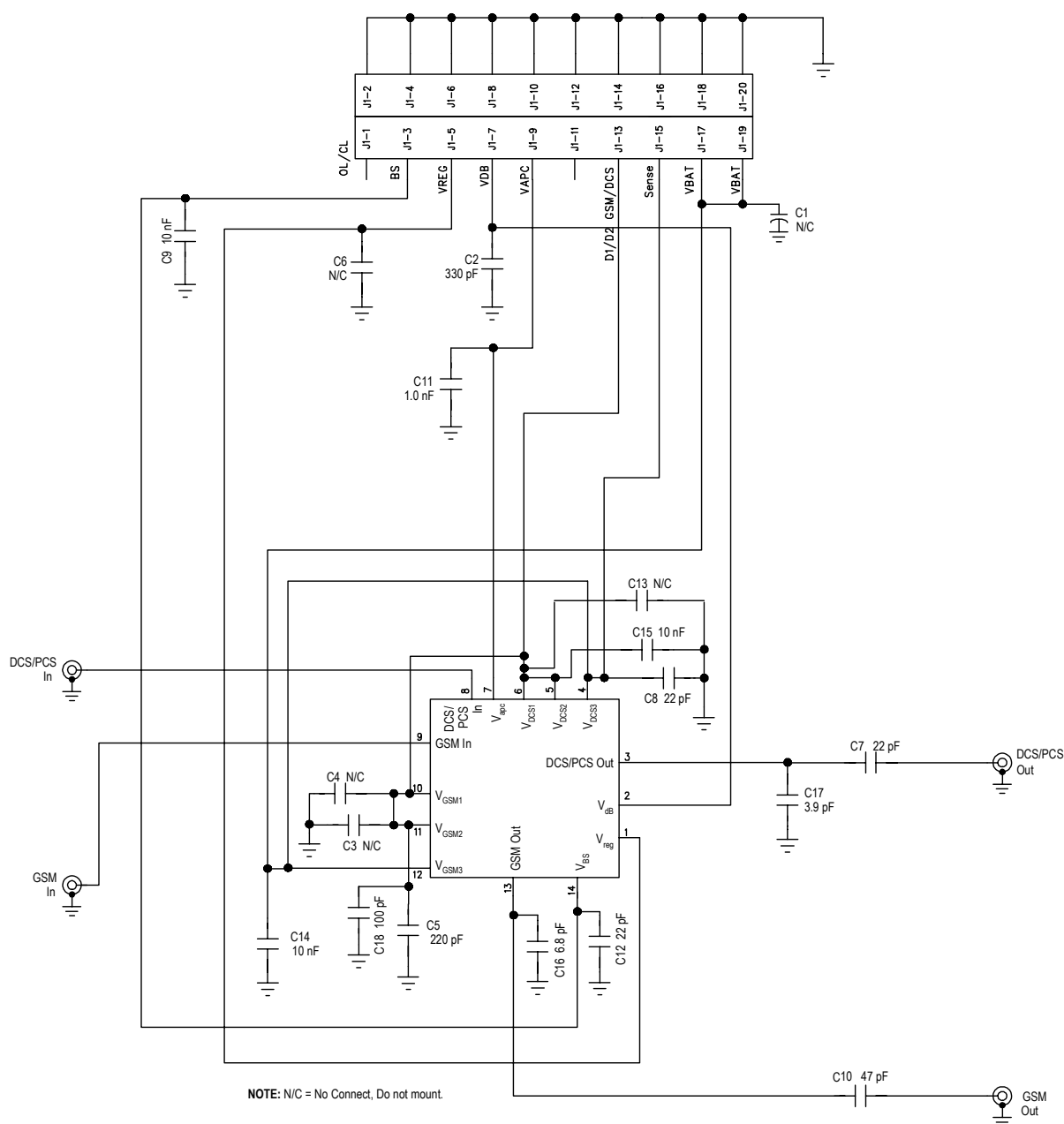


Figure 21. PA Evaluation Circuit

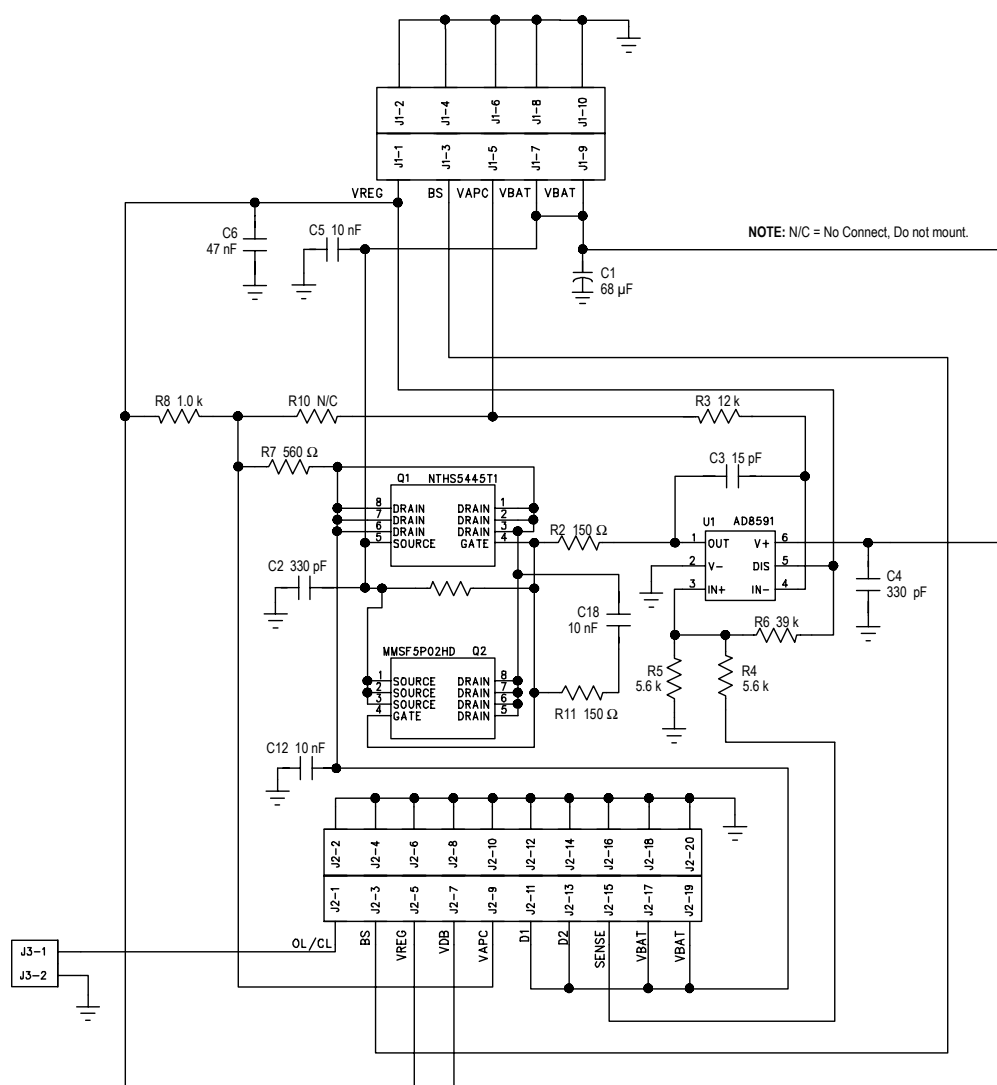


Figure 22. Power Amplifier Control Loop

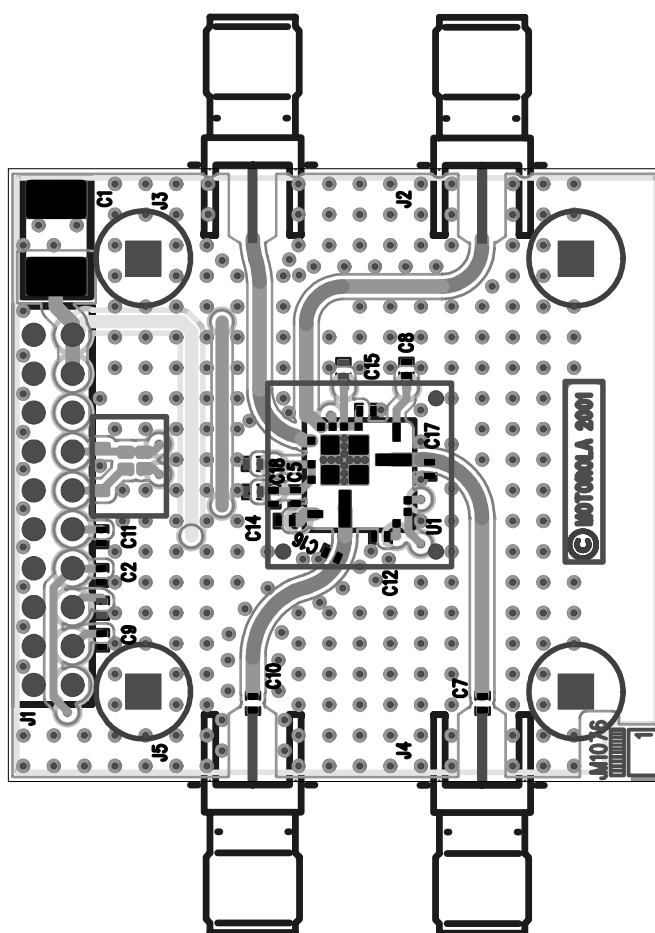


Figure 23. PA Evaluation Circuit PCB

Table 6. PA Evaluation Circuit PCB Bill of Materials

Reference	Value	Part Number	Manufacturer
C1, C3, C4, C6, C13	N/C - Do not mount		
C2	330 pF	GRM36COG330J50	Murata
C5	220 pF	GRM36X7R221K50	Murata
C7, C8, C12	22 pF	GRM36COG220J50	Murata
C9, C14, C15	10 nF	GRM36X7R103K25	Murata
C10	47 pF	GRM36COG470J50	Murata
C11	1.0 nF	GRM36X7R102K25	Murata
C16	6.8 pF	GRM36COG6R8J50	Murata
C17	3.9 pF	GRM36COG3R9J50	Murata
C18	100 nF	GRM36X7R104K25	Murata
J2, J3, J4, J5	50 Ω	142-0711-821	Johnson

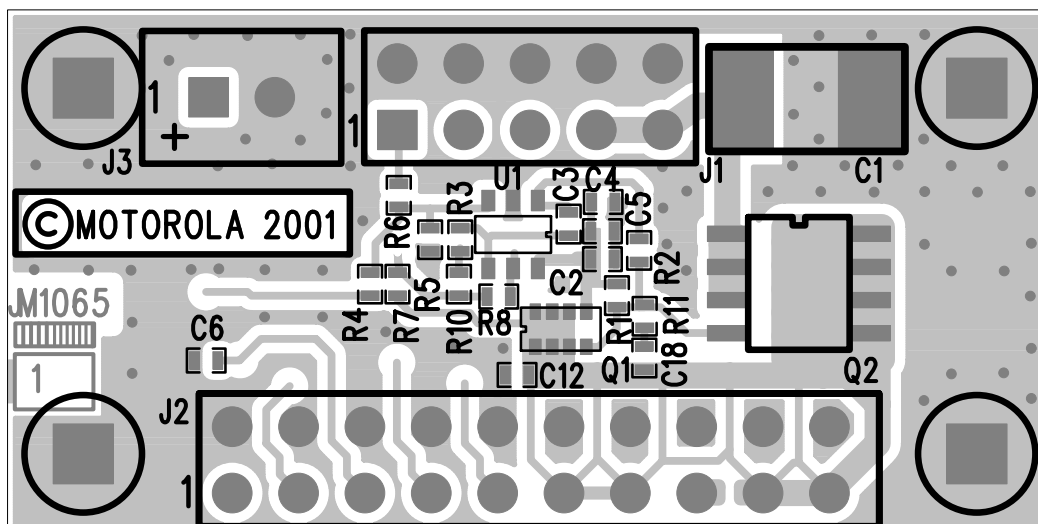


Figure 24. Power Amplifier Control Loop PCB

Table 7. Power Amplifier Control Loop PCB Bill of Materials

Reference	Value	Part Number	Manufacturer
C1	68 μ F	293D685X9020C	Sprague
C2	330 pF	GRM36COG330J50	Murata
C3	15 pF	GRM36COG150J50	Murata
C4	330 pF	GRM36x7R331K50	Murata
C5, C12, C18	10 nF	GRM36X7R103K25	Murata
C6	47 nF	GRM36X7R473K10	Murata
J1, J2, J3	DC connector		
Q1	Power MOSFET	NTHS5445T	ON Semiconductor
Q2	N/C - Do not mount		
R1, R8	1.0 k	CRG0402 5% 1 kO	NEOHM
R2	150 Ω	CRG0402 5% 150 O	NEOHM
R3	12 k	CRG0402 5% 12 kO	NEOHM
R4, R5	5.6 k	CRG0402 5% 5.6 kO	NEOHM
R6, R10	N/C - Do not mount		
R7	560 Ω	CRG0402 5% 560 O	NEOHM
R11	100 Ω	CRG0402 5% 100 O	NEOHM
U1	CMOS Op Amp	AD8591	Analog Devices

5 Packaging Information

Shipping, Packaging and Marking Information

Tape Width: 16.0 mm

Tape Pitch 12 mm (part to part)

Reel Diameter: 330 mm (13 in)

Component Orientation: Parts are to be orientated with pin 1 side closest to the tape's round sprocket holes on the tape's trailing edge.

Dry Pack: This device meets Moisture Sensitivity Level (MSL) 3. Parts will be shipped in Dry Pack. Parts must be stored at 30°C and 60% relative humidity with time out of dry pack not to exceed 168 hours.

In the event that parts are not handled or stored within these limits, one of the following dry out procedures must be completed prior to reflow:

1) 40°C Dry Out: Bake devices at $40^{\circ}\text{C} \leq T_A \leq 45^{\circ}\text{C}$, 5% Relative Humidity for at least 192 hours.

2) Room Temperature Dry Out: Store devices at less than 20% Relative Humidity for at least 500 hours.

Marking:

1st line: Motorola Logo

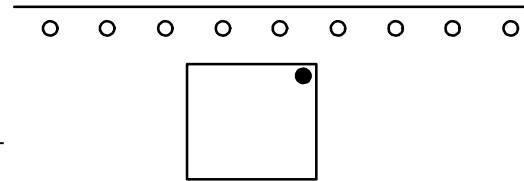
2nd Line: Partnumber coded on 7 characters

3rd Line: Wafer lot number (coded on 6 characters) followed by wafer number (coded on 3 digits)

4th Line: Assy site code (on 1 or 2 characters), followed by Wafer Lot Number (coded on 1 or 2 characters), followed by Year (on 2 digits) and Workweek (on 2 digits).



Marking
(Top View)



Tape & Reel Orientation
(Top View)

Figure 25. Packaging Information

Technical Data

MRFIC0970/D
Rev. 0, 07/2002

3.2 V GSM GaAs
Integrated Power
Amplifier



MOTOROLA
intelligence everywhere™

digital dna™

MRFIC0970



(Scale 2:1)

Package Information

Plastic Package

Case 1308

(QFN-20)

Ordering Information

Device	Marking	Package
MRFIC0970	0970	QFN-20

The MRFIC0970 is a single supply, RF power amplifier designed for the 2.0 W GSM900 handheld radios. The device is packaged in the QFN-20 package, with exposed backside pad, which allows excellent electrical and thermal performance through a solderable contact.

- Target 3.2 V Characteristics:
RF Output Power: 34.5 dBm Typical
Efficiency: 50% Typical
- Single Positive Supply Solution
- Available in Tape and Reel only. R2 Suffix = 2500 Units per 12 mm, 13 inch Reel

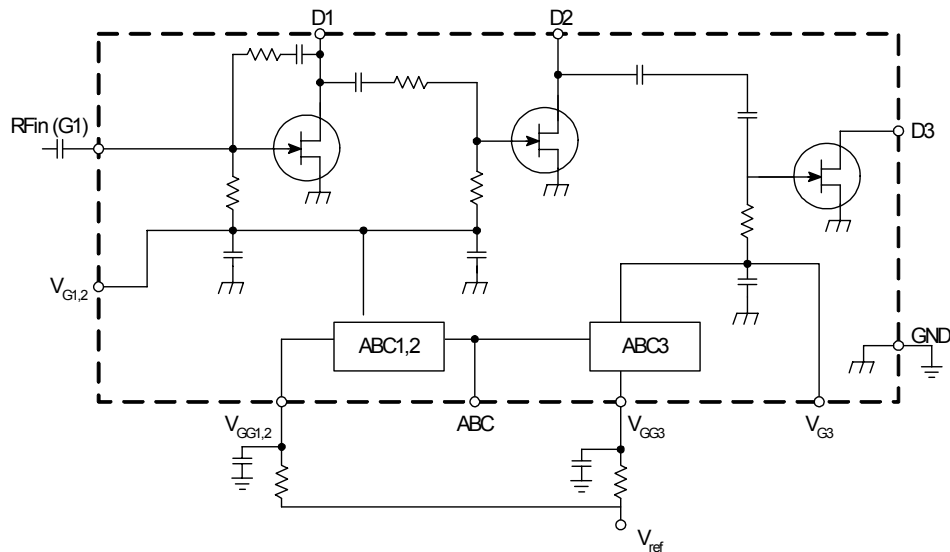


Figure 1. Functional Block Diagram

1 Electrical Characteristics

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	$V_{D1,2,3}, V_{abc}$ V_{ref}	8.0 5.0	V V
RF Input Power	P_{in}	15	dBm
RF Output Power	P_{out}	38	dBm
Operating Case Temperature Range	T_C	-40 to 85	°C
Storage Temperature Range	T_{stg}	-40 to 85	°C
Junction Temperature	T_J	150	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

2 ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤ 250 V and Machine Model (MM) ≤ 60 V. This device is rated Moisture Sensitivity Level (MSL) 1. Additional ESD data available upon request.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{D1,2,3}	2.8	-	5.5	Vdc
	V _{abc}	0	-	5.5	V
	V _{ref}	0.04	-	1.8	V
Input Power	P _{in}	5.0	-	10	dBm

Table 3. Electrical Specifications

($V_{D1,2,3} = 3.2$ V, $V_{abc} = 2.6$ V, $P_{in} = 5.0$ dBm, Peak measurement at 12.5% duty cycle, 4.6 ms period, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	880	-	915	MHz
Output Power	P_{out}	34.5	-	-	dBm
Power Added Efficiency	PAE	50	-	-	%
Minimum Output Power ($V_{ref} = 0.04$, $V_{abc} = 2.6$ V)		-	-	-17	dBm
Power Control Slope ($V_{ref} = 0.1$ to 1.8 V, $\Delta V_{ref} = 0.01$ V)		-	-	50:1	RFV _{rms} / V_{ref}
Bleed thru Power ($P_{in(f_o)} \leq -12$ dBm, $V_{ref} = 0.04$, $V_{abc} = 10$ k load)		-	-	-36	dBm
RF Leakage Current ($I_{DD1} + I_{DD2} + I_{DD3}$, $P_{in}(f_o) \leq 5.0$ dBm) ($V_{abc} = 10$ k load, $V_{ref} = 0.04$ V)		-	-	35	mA
Output Power Switching Speed ($\pm$ step input of V_{ref} RF Pout within 1.0 dB of final value)		-	-	1.0	μs
Input Return Loss	IS11I	-	-	6.0	dB
Noise Power in Rx band 925 to 935 MHz 935 to 960 MHz	NP	- -	- -	-73 -85	dBm
Stability-Spurious Output (Load VSWR 6:1 all phase angles, Adjust $V_{D1, 2\&3}$ for specified power)	P_{spur}	-	-	-30	dBc
Load Mismatch Stress (Load VSWR = 10:1 all phase angles, 5 seconds, Adjust $V_{D1, 2\&3}$ for specified power)	No Degradation in Output Power Before & After Test				

2 Pin Connections

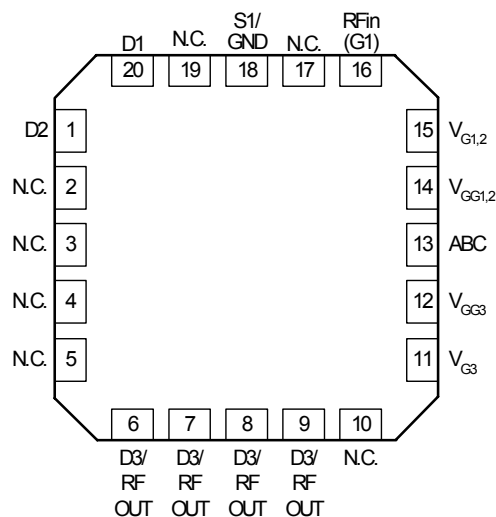


Figure 2. Pin Connections

3 Typical Performance Characteristics

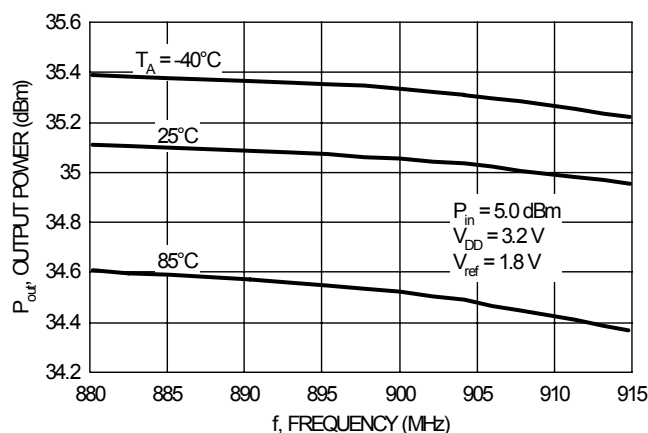


Figure 3. Output Power versus Frequency

Freescale Semiconductor, Inc. Typical Performance Characteristics

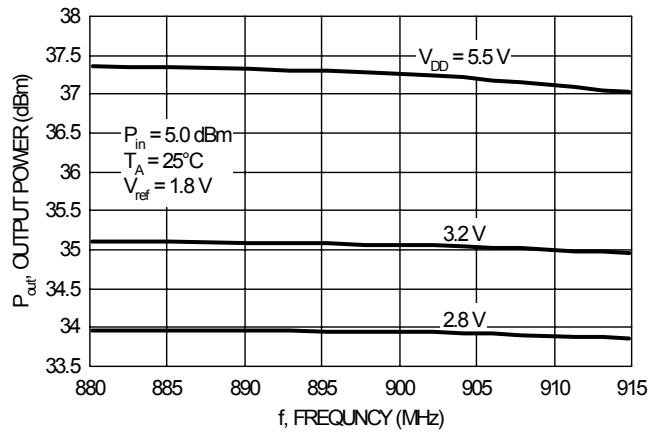


Figure 4. Output Power versus Frequency

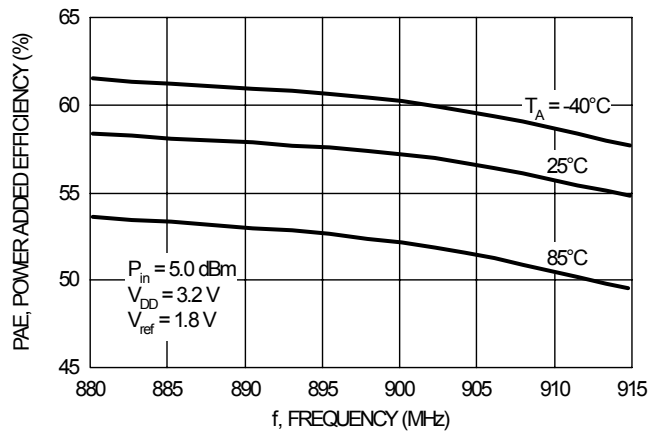


Figure 5. Power Added Efficiency versus Frequency

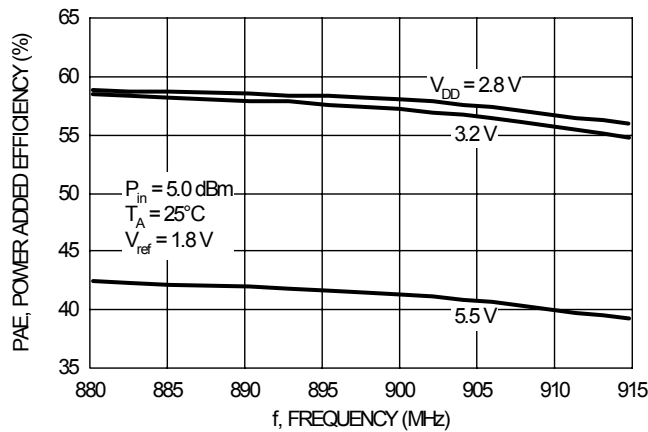


Figure 6. Power Added Efficiency versus Frequency

4 Application Schematic

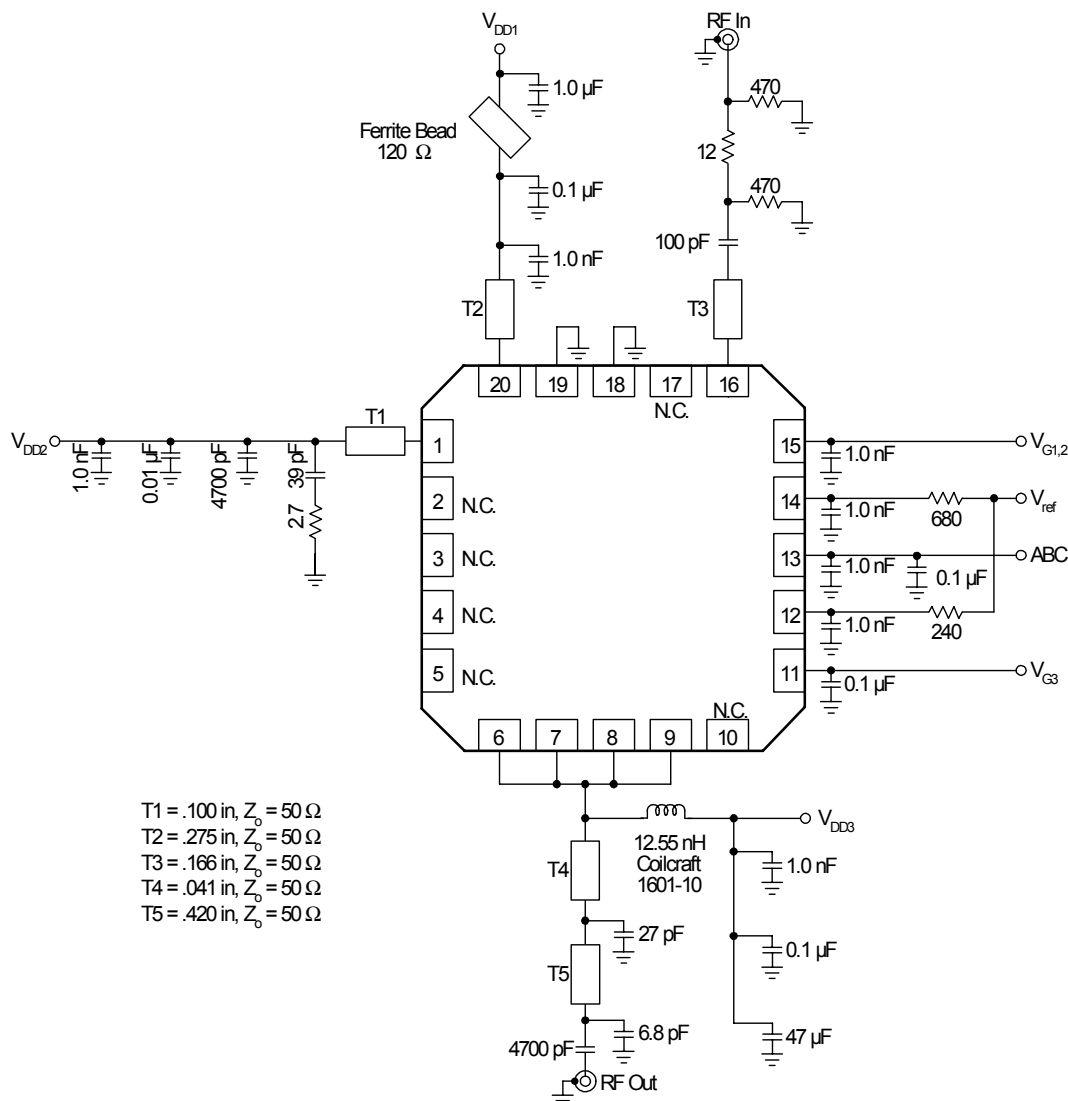


Figure 7. Application Schematic

Product Preview

MRFIC1870PP/D
Rev. 0, 02/2003

3.2 V DCS/PCS
GaAs Integrated
Power Amplifier



MRFIC1870



Package Information

Plastic Package
Case 1308
(QFN-20)

Ordering Information

Device	Device Marking	Package
MRFIC1870	1870	QFN-20

The MRFIC1870 is a single supply, RF power amplifier designed for the 2.0 W DCS/PCS handheld radios. The device is packaged in the QFN-20 package, with exposed backside pad, which allows excellent electrical and thermal performance through a solderable contact.

- Target 3.2 V Characteristics:
RF Output Power: 32 dBm Minimum
Efficiency: 42% Minimum
- Single Positive Supply Solution

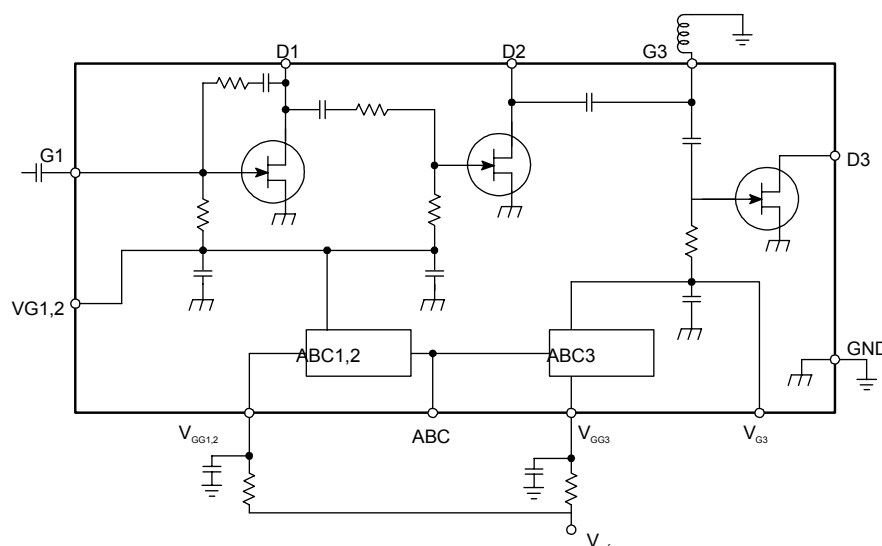


Figure 1. Functional Block Diagram

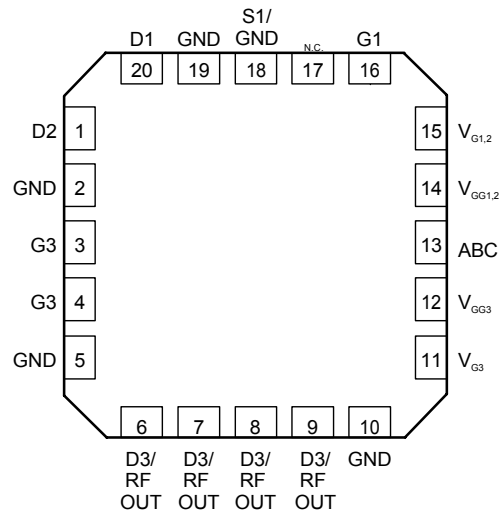


Figure 2. Contact Connections

Chapter Three

RF/IF Subsystems – Data Sheets

Device Number	Page Number
Transceivers	
MC13190	3-3
Miscellaneous Functions	
ADCs/DACs	
MC144110	3-22
MC144111	3-22
Encoders/Decoders	
MC145026	3-23
MC145027	3-23
MC145028	3-23

Advance Information

MC13190/D
Rev. 0, 10/2002

2.4 GHz Short-Range,
Low-Power Transceiver



MOTOROLA
intelligence everywhere™

digital dna™

MC13190



Package Information

Plastic Package
Case 1311
(QFN-32, 5x5 mm)

Ordering Information

Device	Device Marking	Package
MC13190FC	13190	QFN-32

The MC13190 is a Short-Range, Low-Power 2.4 GHz ISM band single chip radio. Together with an appropriate microprocessor or DSP for a Baseband Controller, it provides cost effective solutions for short-range (up to 10 meters), battery-powered data links. Applications include remote control, wire replacement, wireless streaming audio, and wireless game control. The receiver includes a low noise amplifier (LNA), AM demodulator, band pass filter and limiting IF. The transmitter includes modulation control, baseband filtering and AM modulator. An on-chip PLL/VCO derives the RF frequency from a fixed 256 multiplication of the reference frequency. The device is fabricated using Motorola's RF BiCMOS process and is housed in a 32 lead QFN package with backside ground.

- Typical Receiver Sensitivity: -71 dBm for 2×10^{-4} Bit Error Rate (BER)
- Typical Output Power = 4.8 dBm
- Fully Differential RF Input and Output



Table 1. Maximum Ratings

NOTES:

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.
2. Meets Human Body Model (HBM) ≤ 2.0 kV and Machine Model (MM) ≤ 200 V except RF and Limiter circuit contacts. Limiter circuit contacts (contacts 19 and 17) = 900 V HBM, 125 V MM. RF Contacts = 80 V HBM, 50V MM. RF contacts have no ESD protection. Additional ESD data available upon request.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.5	2.75	3.0	V
Digital Supply	V_{DD}	2.0	2.75	3.0	V
Signal and Control Pins		80% V_{DD}	-	V_{DD}	V
Demodulator Supply Voltage (no LNA input signal)		2.7	3.1	3.3	V
Input Operating Frequency		2.411	-	2.473	GHz
Maximum Input Power into LNA_IN		-	-	0	dBm
Differential Load Impedance for Transmitter (MOD_OUT)		-	50	-	Ω
Differential Source Impedance for Receiver (LNA_IN)		-	25	-	Ω
Transmit Data Rate (Manchester Encoded)		4	5	6	Mbits/s
Transmit Data Encoding		Manchester, 50% Duty Cycle			

Table 3. System Characteristics

($V_{CC} = 2.75$ V, $T_A = 25^\circ\text{C}$, RF Receiver Frequency = 2.442 GHz, 60% AM, Bit Rate = 5.0 Mbps Manchester coded, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Sensitivity for 2×10^{-4} Bit Error Rate		-65	-71	-	dBm
Baseband Filter Lower Corner Frequency		-	0.35	-	MHz
Baseband Filter Upper Corner Frequency		-	6.0	-	MHz
Receiver Recovery Time from a 7.0 dBm Burst		-	-	15	μs
AM Modulation Depth		50	60	88	%
Transmit Power (modulated)		1.9	4.8	-	dBm
Receive Supply Current ($P_{in} = -50$ dBm)	I_{CC}	-	11	-	mA
Transmit Supply Current	I_{CC}				mA
Logic 1		-	54	-	
Logic 0		-	27	-	
50% Duty Cycle		-	40.5	-	
Standby Supply Current		-	51	-	μA

Table 4. Receiver Section

($V_{CC} = 2.75\text{ V}$, $T_A = 25^\circ\text{C}$, RF Receiver Frequency = 2.442 GHz, 60% AM, Bit Rate = 5.0 Mbps Manchester coded, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Low Noise Amplifier and Am Demodulator

Current Consumption					
Active		-	11	-	mA
Disabled		-	7.0	-	μA
Recovered Signal Level at -65 dBm		-	5.0	-	mVpp

Limiter and Level Shifter

Current Consumption					μA
Active		-	240	-	
Disabled		-	3.0	-	
RX_DATA Drive Capability (5.0 MHz)		-	-	10	pF
Output High with respect to $V_{DD_RX_DATA}$ @ -100 μA		80% V_{DD}			V
Output Low with respect to GND @ -100 μA				0.2	V

Table 5. Transmit Section

($V_{CC} = 2.75\text{ V}$, $T_A = 25^\circ\text{C}$, RF Transmit Frequency = 2.442 GHz, 60% AM, Bit Rate = 5.0 Mbps Manchester coded, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Frequency Synthesizer ($V_{CC} = 2.75\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Total Current Consumption when active					
Active		-	10.2	-	mA
Disabled		-	1.1	-	μA
Frequency Range (FREF x 256)		2.4	-	2.484	GHz
Reference Input Frequency	f_{ref}	9.375	-	9.704	MHz
RF Frequency Divide Ratio	N	-	256	-	
Trim Time (using fixed clock derived from reference)		-	-	100	μs
Time required to turn on and lock after trim (250 kHz Loop Bandwidth)		-	25	-	μs
Reference Input Level					V
Ref Low		-	-	$V_{DD} \times 20\%$	
Ref High		$V_{DD} \times 80\%$	-	-	

Table 5. Transmit Section (Continued)

($V_{CC} = 2.75\text{ V}$, $T_A = 25^\circ\text{C}$, RF Transmit Frequency = 2.442 GHz, 60% AM, Bit Rate = 5.0 Mbps Manchester coded, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
AM Modulator					
Current Consumption					
Active		-	16.4	-	mA
Disabled		-	3.0	-	μA
AM Modulation Depth Range		50	60	88	%
Output Power		2.0	4.8	-	dBm
Occupied Bandwidth (99% Signal Energy)		-	22	-	MHz
Out of Band Spurious at Antenna Port					dBm
30 MHz to 1.0 GHz		-	-45	-	
1.0 to 1.275 GHz		-	-40	-	
1.8 to 1.9 GHz		-	-45	-	
5.15 to 5.3 GHz		-	-50	-	
Acceptable Duty Cycle for TX_DATA Signal (Manchester Encoded)		48	-	52	%

Table 6. Enable Logic Levels

($V_{CC} = 2.75\text{ V}$, $T_A = 25^\circ\text{C}$)

Symbol	Characteristic	Min	Max
V_{IH}	High Level Input Voltage	80% V_{DD}	-
V_{IL}	Low Level Input Voltage	-	20% V_{DD}
I_{IH}	High Level Input Current	-	1.0 μA
I_{IL}	Low Level Input Current	-	1.0 μA

2 Contact Connections

Table 7. Control Contact Definitions

Contact	Description
RX_EN	Enables LNA, Demod and Limiter
TX_EN	Enables TX Filter, Modulation Control, PA/Modulator
PLL_EN	Enables Frequency Synthesizer and VCO
TRIM_EN	Enables VCO Trimming
LNA_SW	Switches LNA Inputs to Ground in TX Mode

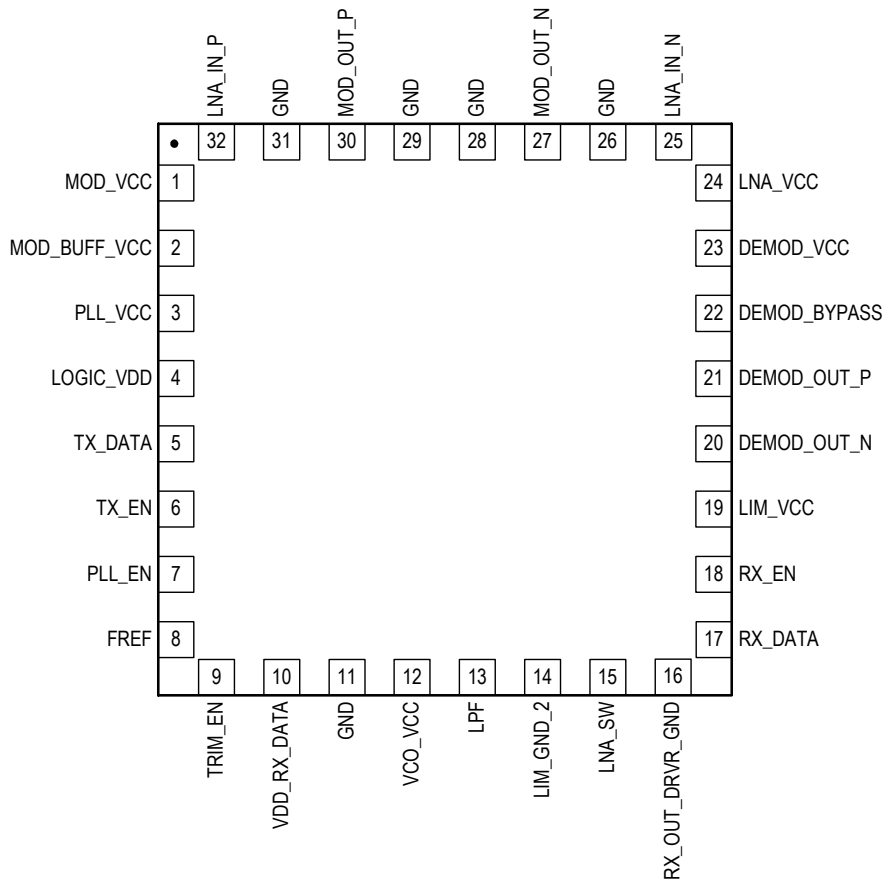


Figure 2. Contact Connections

3 Application Information

3.1 Introduction

The MC13190 is a 2.4 GHz transceiver that takes advantage of AM modulation to provide wide-band data capability with simple, low-cost circuitry. The transmit and receive baseband filters are designed for 5 Mbps Manchester encoded data. This high data rate capability is intended to provide low latency, avoid interference through short-burst protocol and allow for multiple retransmissions. The baseband interface is simple to allow maximum flexibility in applications. Depending on protocol choices and bit error rate requirements, the MC13190 is capable of supporting up to 1 Mbps data throughput.

3.2 Modes of Operation

The MC13190 has three modes of operation; Standby, Transmit and Receive. Refer to Figure 1, Simplified Block Diagram, for circuit functions.

3.2.1 Standby Mode

Standby mode is automatically initiated when all enable ($_EN$) IC Contacts are kept low. The current consumption during standby mode is typically 51 μA .

3.2.2 Transmit Mode

In the Transmit mode, the VCO frequency is set based on the reference by the PLL, the transmit chain is enabled, the transmit data is filtered and AM-modulates the transmit carrier. This sequence is shown in Figure 3. The switches to ground at the input of the LNA as well as the PLL are enabled ahead of the TX chain. Optionally, an external Transmit/Receive switch can be used and LNA_SW can be left low. This delay allows the PLL to settle prior to application of data. During power-up of the TX chain, TX_DATA should be kept low. This guarantees the modulator powers up at minimum output power which will prevent splatter.

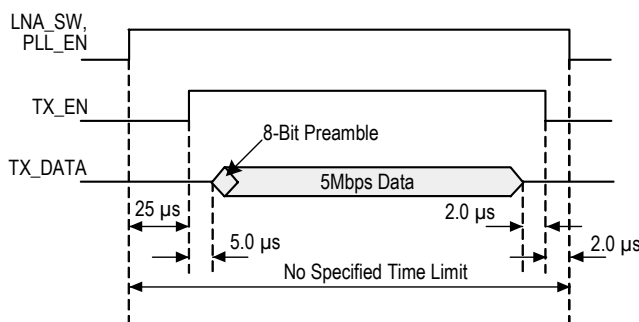


Figure 3. Recommended Timing During Transmit Mode

It should be noted that the transmit baseband filter is optimized for 5 Mbps Manchester encoded data. The MC13190 does not provide this encoding. See Section 3.6.1 for discussion of Manchester encoding.

The internal 2.4 GHz VCO includes circuitry to perform an automated trimming cycle. In the TRIM cycle, the VCO will trim itself to the required frequency keeping the control voltage within the specified range. After initial trimming, the VCO does not require trimming again until the supply voltage and/or the temperature changes. Trimming every one to 10 seconds is, however, recommended. The TRIM cycle timing is shown in Figure 4.

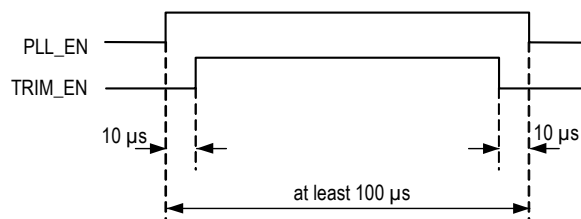


Figure 4. Recommended Timing During Trim Mode

The PLL is enabled, a delay of 10 µs is observed for the VCO and the PLL to settle, and then trimming is begun. Trimming continues until TRIM_EN is taken low and should continue for a minimum of 100 µs. After the TRIM_EN is taken low, the trim information is stored internally, a process that takes about 10 µs. PLL_EN must remain high while the trim information is stored.

The frequency synthesizer uses a fixed 256 divider and must be enabled in both TRIM and TX mode. The frequency synthesizer is not required in the receive mode and may be disabled. The frequency synthesizer requires an external reference signal (IC Contact 8), FREF, and an external loop filter connected to IC Contact 13.

3.2.3 Receive Mode

In Receive mode, the 2.4 GHz signals from the antenna are amplified by the LNA, peak detected in the demodulator and filtered and amplified to produce the RX_DATA output. The response time after the first time RX_EN is pulled high is set by the charging time of the demodulator bypass capacitor and is about 700 µs. Once the capacitor is charged, internal circuitry maintains the charge for at least one second and the response time is reduced to around 7 µs. An 8-bit preamble allows for receive circuitry setting. The receiver baseband filter is optimized for Manchester encoded 5 Mbps data. The Receive sequence is shown in Figure 5.

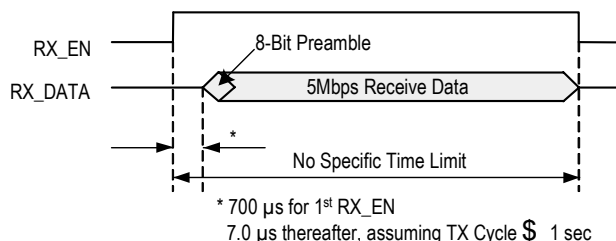


Figure 5. Recommended Timing During Receive Mode

3.3 Transmit and Receive Sequencing

Figure 6 shows the sequencing and timing for a typical Trim, Transmit, Receive and Re-transmit cycle. Note that the PLL and VCO (PLL_EN) are off during the Receive cycle. This sequence can be repeated as often as needed and is controlled by the applications software. The TRIM cycle should be repeated at regular intervals of 1 to 10 seconds or when the temperature and/or voltage have changed.

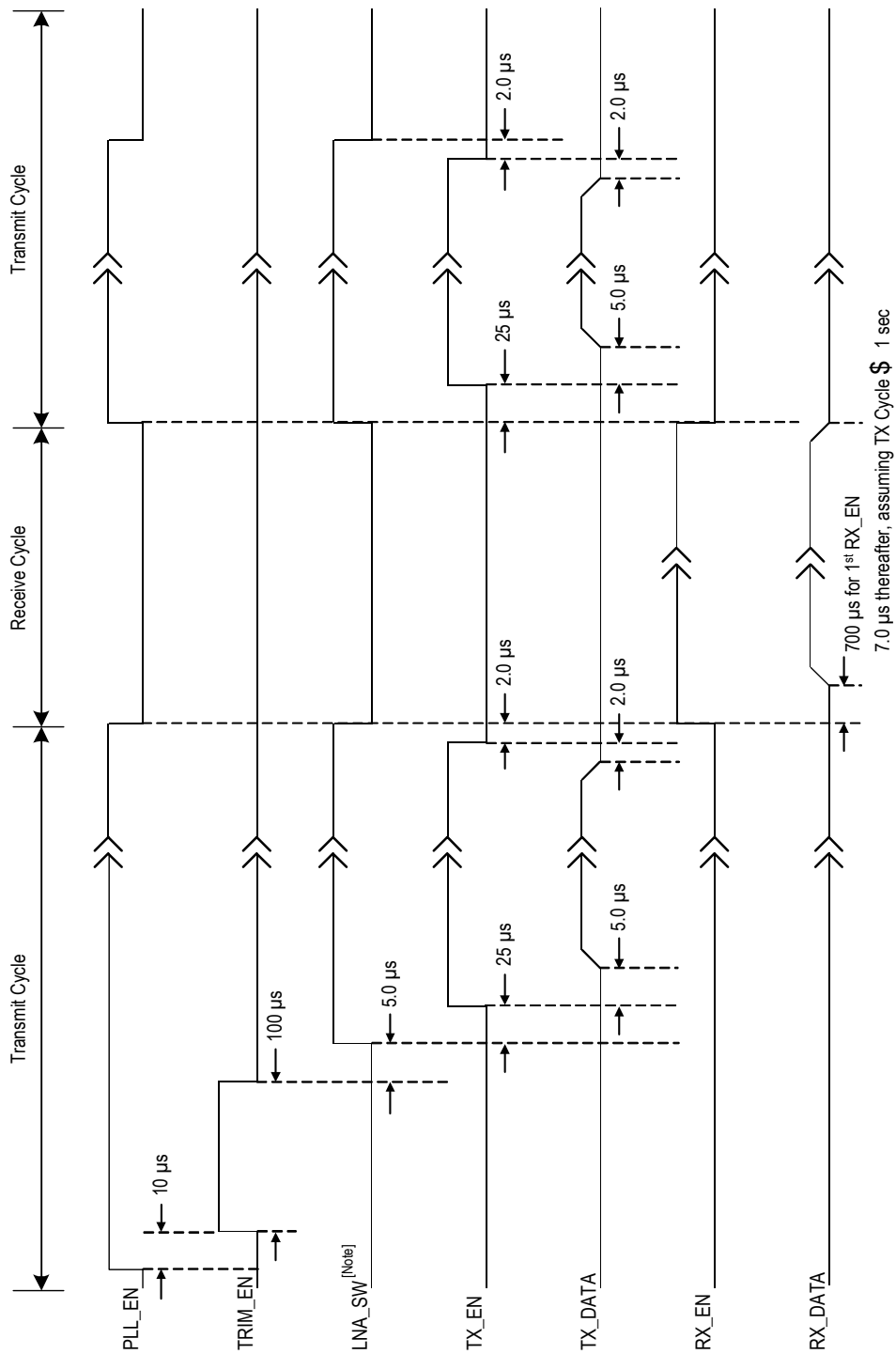


Figure 6. Transmit/Receive Timing Sequence

3.4 Basic Transceiver Circuit

Figure 7 shows the basic transceiver evaluation board circuit schematic with reference oscillator and Figure 8 shows the optional external LNAs. Figures 9 and 10 show the evaluation board printed circuit board layout details.

This realization is intended for device evaluation and has been designed with a 50 Ω interface. C19, C20, L10 and L12 form a lumped-element balun. In equipment applications a differential antenna can be interfaced through matching elements directly to the LNA and Modulator contacts. A PCB dipole antenna with balun and SMA connector is available for link evaluations. The RF circuit layout is critical and should be duplicated exactly. In normal applications, the entire transceiver should be shielded and control lines from the baseband should be as short as possible.

The optional external LNA circuits require an external differential switch that is implemented with PIN diodes D1, D2, D3 and D4. T1 and T2 are quarter wave lines for isolation. IC Contact 15, LNA_SW, is grounded since the internal switch is not used. If the LNA are used, C25 and C30 are not placed and “zero Ohm” resistors R5, R9, R13 and R14 insert the LNAs into the receive path.

Voltage supply Contacts 1, 2, 3, 12, 19, 23 and 24 require bypass capacitors as close as possible to the device. Logic supply Contact 4 can directly interface to the baseband supply in equipment applications. The DEMOD_BYPASS (Contact 22) bypasses the demodulator bias circuitry for both RF signals and low frequency signals. The differential demodulator output from contacts 20 and 21 is available at TP1 and TP2. The PLL loop filter is the standard R+C // C network and connects between contacts 12 and 13.

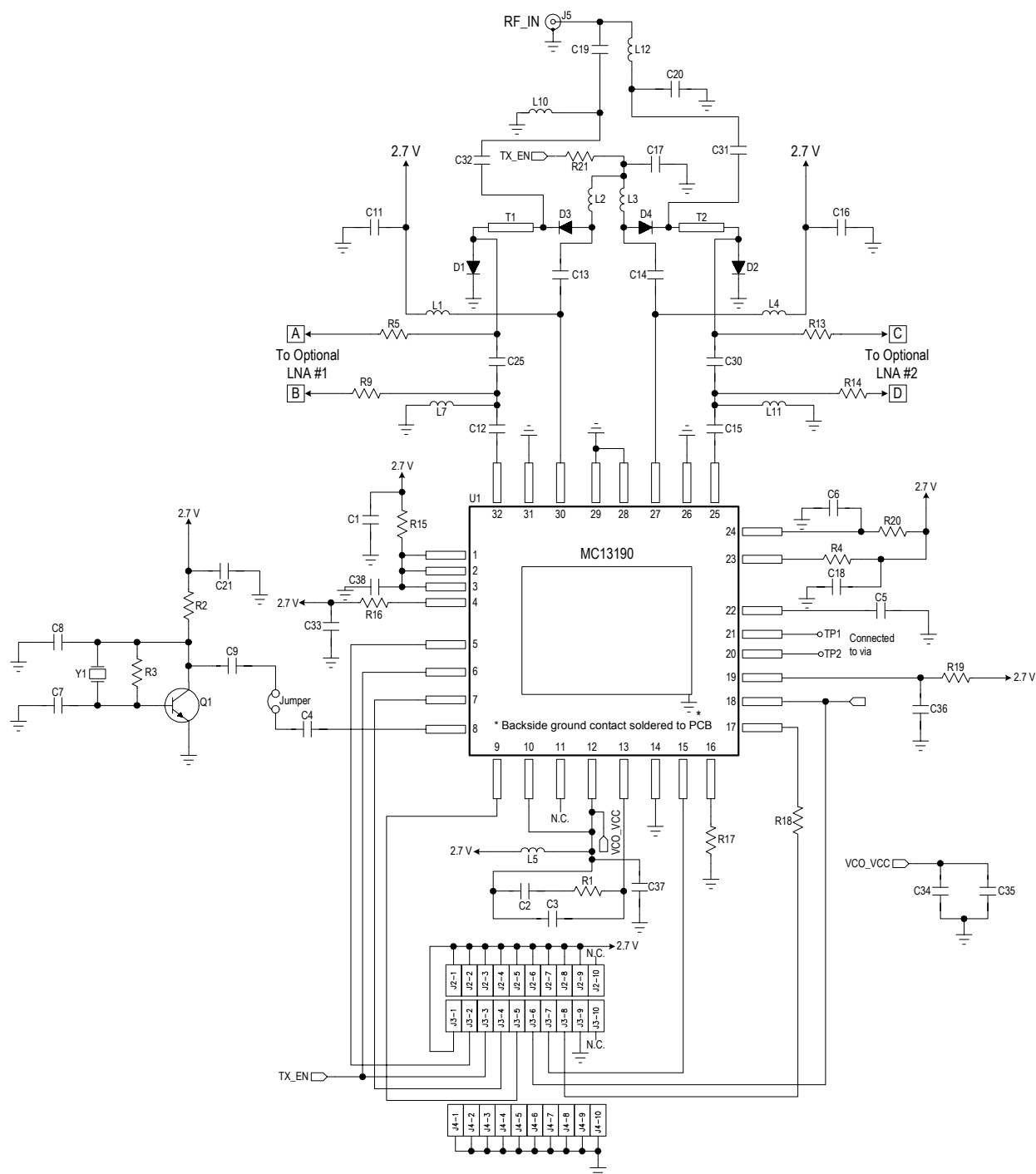


Figure 7. Transceiver Application Circuit Schematic

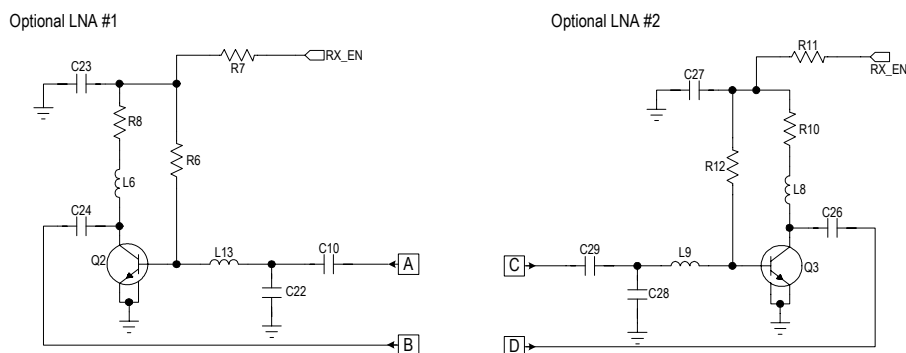


Figure 8. Optional LNA Circuits

Table 8. Bill of Materials

Reference	Value	Description
C1, C6, C11, C16, C18, C21, C33, C35, C36, C37	0.1 μ F	0402 Ceramic, Murata
C2	82 pF	0402 NPO Ceramic, Murata
C3	12 pF	0402 NPO Ceramic, Murata
C4, C23, C27	1000 pF	0402 Ceramic, Murata
C5	1.0 μ F	0603 Ceramic, Murata
C7, C8	27 pF	0402 NPO Ceramic, Murata
C9, C34	100 pF	0402 NPO Ceramic, Murata
C10, C13, C14, C29	6.0 pF	0402 NPO Ceramic, Murata
C12, C15	3.0 pF	0402 NPO Ceramic, Murata
C17	10 pF	0402 NPO Ceramic, Murata
C19, C20	1.5 pF	0402 NPO Ceramic, Murata
C22, C28	0.5 pF	0402 NPO Ceramic, Murata
C24, C26	2.0 pF	0402 NPO Ceramic, Murata
C25, C30, C31, C32, C38	33 pF	0402 NPO Ceramic, Murata
D1, D2, D3, D4	BAR63-03W	Pin Diode, Siemens
J2, J3, J4		1 x 10 Header Strip
J5		SMA Right Angle
L1, L4	2.2 nH	0402 Toko
L2, L3	15 nH	0402 Toko
L5	2.7 nH	0603 Toko
L6, L7, L8, L11	3.0 nH	0402 Toko
L9, L13	0.5 nH	0402 Toko

Table 8. Bill of Materials (Continued)

Reference	Value	Description
L10, L12	1.8 nH	0402 Toko
Q1		MMBT3904
Q2, Q3		MBC13900
R1	12 k Ω	0402 5%
R2	560 Ω	0402 5%
R3	68 k Ω	0402 5%
R4	51 Ω	0402 5%
R5, R9, R13, R14	0 Ω	0402
R6, R12	49 k Ω	0402 5%
R7, R11	130 Ω	0402 5%
R16, R17, R18	180 Ω	0402 5%
R8, R10, R15, R19, R20	10 Ω	0402 5%
R21	270 Ω	0402 5%
T1, T2	$Z_0 = 25 \Omega, l = 0.72$	Microstrip Transmission line, $\epsilon_r = 4.5$ mils, $t = 10$ mils
U1		MC13190
Y1	9.357 MHz	Temex

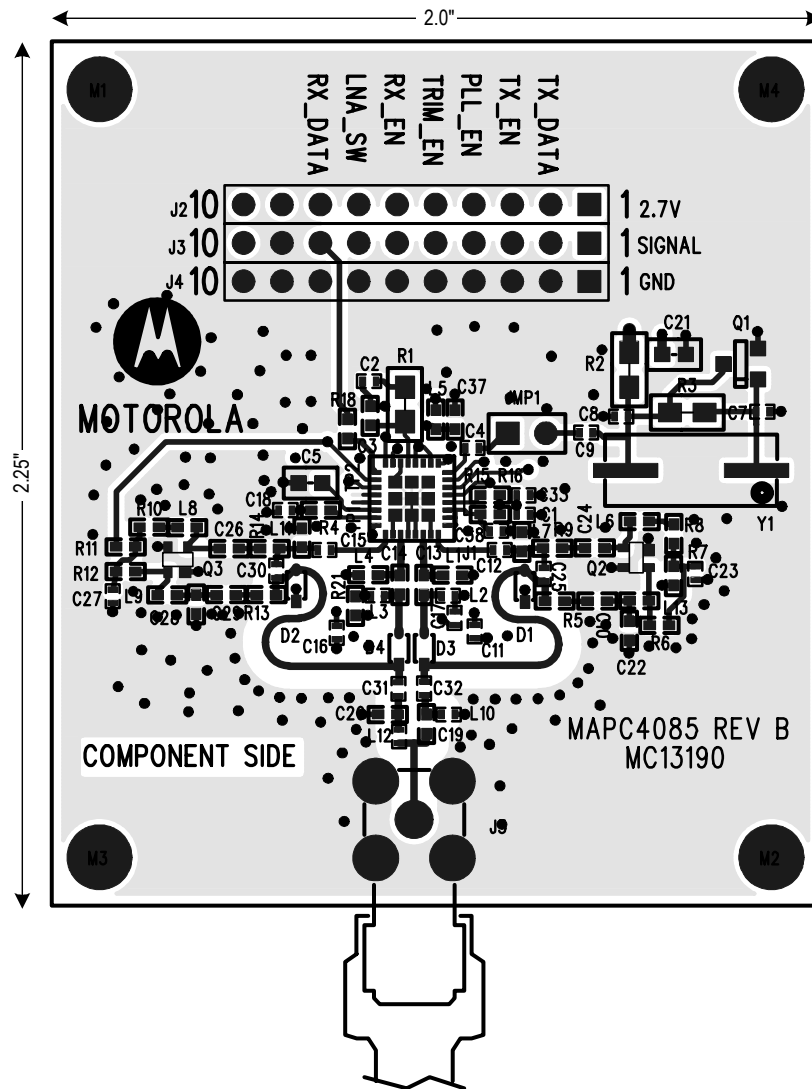


Figure 9. Transceiver Circuit PCB Topside
(Active Dielectric = 10 mil FR4, Total Board Thickness = 0.062")

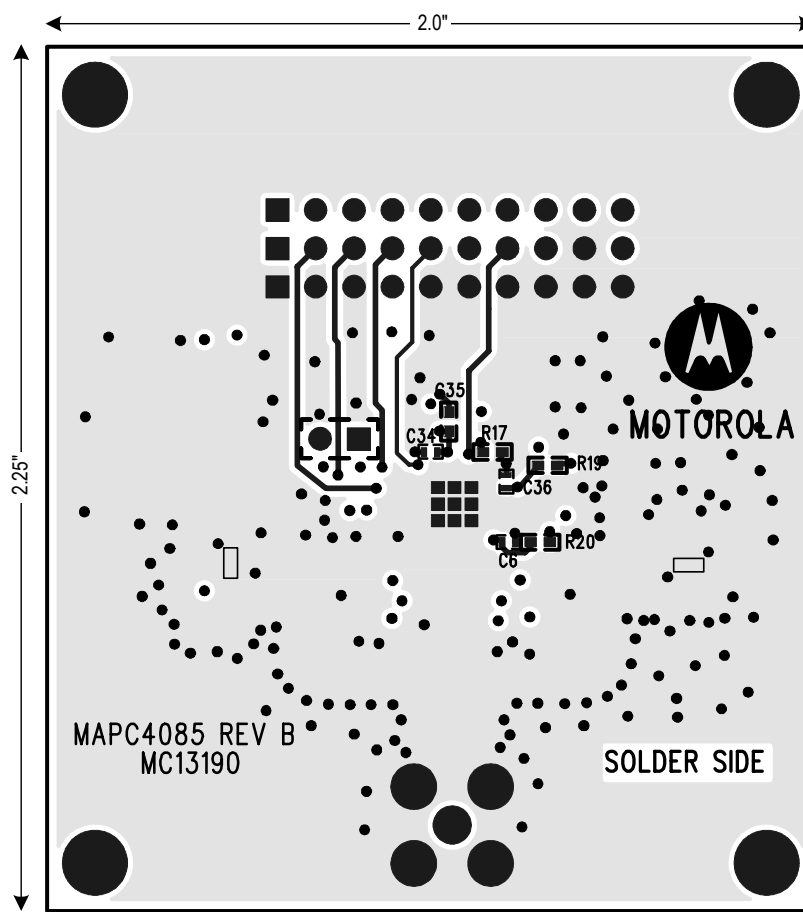


Figure 10. Transceiver Circuit PCB Bottom Side
(Active Dielectric = 10 mil FR4, Total Board Thickness = 0.062")

3.5 Baseband Interface

Referring again to Figure 1, the Simplified Block Diagram, the baseband interface is accomplished through the Logic Interface block. TX_DATA and RX_DATA provide the data interface. The MC13190 is designed to transmit and receive 5 Mbps Manchester encoded data. Data rates of between 4 and 6 Mbps are acceptable. The data pulses should be between 100 and 200 ns duration. The MC13190 does not provide encoding or decoding. The baseband device chosen must be capable of encoding and decoding a 5 Mbps data stream. FREF can be supplied by the baseband and can be "warped" or "dithered" to provide frequency variation.

The remaining five control lines are controlled through GPIO lines.

3.5.1 Low Data Rate Applications

For low data rate applications, an alternate approach can be used to employ a low-cost microcontroller. Figure 11 shows the basic principals. A Motorola MC68HC908GR8 is shown but the same approach can be used with any MCU that is capable of performing the required task. The system reference frequency is chosen to be the 9.537 MHz required for the MC13190's transmit synthesizer. The reference is also fed to a programmable divider which becomes an FSK generator controlled by the transmit data from the MCU. F1 will be 4.769 MHz while F2 will be 2.384 MHz. These frequencies AM modulate the 2.44 GHz carrier as though they were data. On the receive side, RX_DATA drives a peak detector tuned for F1. F1 therefore

produces a high output and F2 produces a low output. This recovered data stream is feed to the receive data input of the MCU. FSK, rather than ASK, was chosen to keep the baseband limiter compressed and reduce baseband noise. This technique has been shown to work up to 100 kb/s data rate. Details are given in Motorola Application Note AN1946/D.

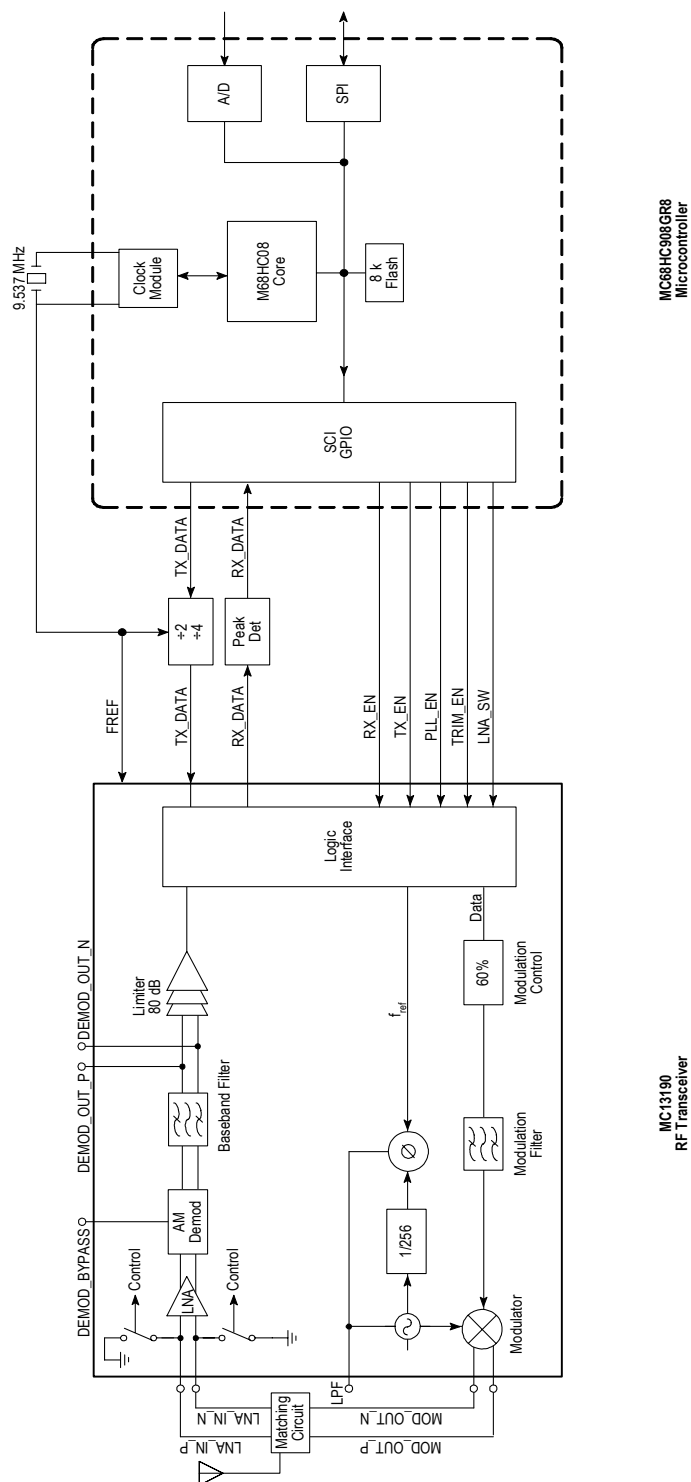


Figure 11. MC13190 Interface with HC08 Microcontroller for Low Data Rate Applications

3.6 Protocol Considerations

3.6.1 Manchester Encoding

As mentioned earlier, the MC13190 has been designed for use with protocols that employ Manchester encoding. The basic principle of this coding technique is that each data bit is encoded as a transition as opposed to a level. This results in two half-bits as shown in Figure 12. A data 1 bit is encoded as a high-low transition while a data 0 bit is encoded as a low-high transition. Each data bit then has a transition which facilitates data clock recovery. The half-bits are the transmitted and received symbols so each data bit results in two channel symbols.

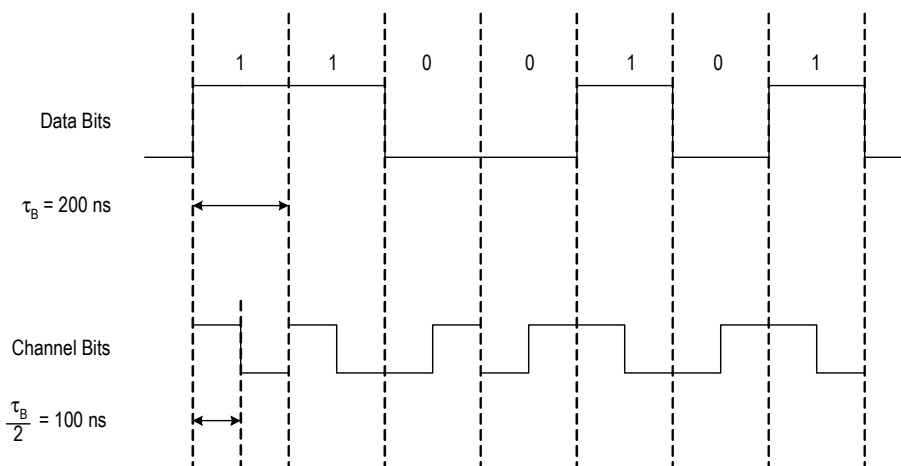


Figure 12. Manchester Encoding of 5 Mbit Data

At 5 Mbps a data bit is 200 ns long. The channel bits are then 100 ns each but because of the encoding algorithm there can be two half-bits in sequence when a data bit transition occurs. This is also the maximum number of half bits that can occur in sequence.

Although the active filters in the MC13190 transmitter are designed for a specific data rate and Manchester encoding, there is nothing to prevent the application from using other rates or encoding in just the transmitter.

The transmitter uses slope control and low-pass filtering to control the bandwidth of the baseband signal. These filters assume a 100 ns Manchester encoded half-bit with a tightly controlled duty cycle. TX_DATA is dc-coupled so there is no limit on the length of the data bit. A data 1 or 0 can be maintained indefinitely. If the pulse length at TX_DATA is much shorter than 100 ns, the slope control will not allow the modulator to peak and the modulation index will decrease.

The receive filters are hard-wired for 5 Mbps Manchester encoded data as shown in Figure 12 and cannot be changed by the user. These filters have bandpass response to maximize the performance of the receiver. The receiver is ac-coupled. Using Manchester encoded data rates outside the range of 4 to 6 Mbps will result in less than optimum performance. If the rate is too high or low, the data will fall out of the receiver passband and performance will degrade quickly.

3.6.2 Channel Considerations

The 2.4 GHz band is a noisy environment prone to multipath fading. Noise takes many forms but, at 2.4 GHz, microwave ovens and other users predominate. Multipath fading occurs when the same signal arrives at the receiver at different times. Not only can multipath impact the absolute signal level but it can also result in frequency selective fading and intersymbol interference. The AM modulation scheme used in the

MC13190 makes it susceptible to frequency selective fading through the “notching” of the carrier causing performance degradation in the envelope detector. These effects cannot be avoided so must be dealt with in protocol design. Sufficient margin must be built into the link and redundancy into the protocol to reduce bit error rate to an acceptable level.

3.6.3 Packet Structure

The 5 Mbps data rate that the MC13190 supports is high enough to allow multiple users to occupy the same frequency channel using time division multiple access (TDMA) techniques. The protocol for implementing the TDMA is left up to the system integrator and is heavily dependent on the number of users per unit area, the amount of data to be transmitted per user per unit time and the method used to detect the symbols.

The high level frame structure should allow for the total number of users required as well as the number of retransmissions allocated to each user with a guard band between each packet to allow for the timing uncertainty associated with each of the users clocks. The upper bound of the frame structure is determined by the desired data throughput for each user and the latency of the data. If low latency is the primary design goal, a short frame should be used.

The packets should be structured to provide for a robust synchronization between the transmitter and the receiver as well as a means to deliver the payload reliably with some level of error detection or correction. The packet should be designed with a preamble of at least 8 bits to allow for transceiver settling, a synchronization code, a header, the payload, and the error detection overhead. A suitable form of error detection could be an N-length CRC calculated and appended to the packet.

A common method of synchronization used in the industry is to transmit a length of a code that has been designed to provide for fast acquisition of the codeword yet low probability of false detection. The ideal code word has a very low autocorrelation side lobe. That is to say, when the codeword is shifted the correlation value is very low. A Barker or Neuman-Hofman code could be used and are well documented in most digital communication texts.

The MC13190 receiver outputs a waveform that has no timing associated with it. In other words, the baseband symbol detector will need to determine the waveform timing in order to make the correct bit decisions on the sampled waveform. Since the transmitted date is Manchester encoded, it is recommended that the input waveform be at least 8X oversampled so that there are at least 4 samples per half of the waveform. The correlation with the synchronization word should be performed on all samples of the waveform, but it is recommended that the bit decisions be based only on the second half of the Manchester encoded waveform since a transition is guaranteed at the middle of each transmitted bit. It should be noted that an artifact of the MC13190 baseband filtering is some corruption of the first half of the Manchester encode bit cycle as well. 8X oversampling should provide for adequate timing resolution of the bit edge transitions to insure correct bit decisions if the packet length is not too long. The packet length will be limited primarily by the accuracy of the reference clocks in the system. If the reference source has a guaranteed stability of 50 ppm, then a worst case timing shift will be 100 ppm or up to 20 ps per 200 ns bit. This would limit the packet length to 250 μ s before the accumulated timing drift will begin to affect the symbol detection. A method of coherent detection could be employed where a tracking loop is implemented if longer packers are desired.

3.7 Device Characterization Information

Table 9. Broadband Differential Scattering Parameters

f (GHz)	LNA RX Mode		LNA TX Mode	
	Mag	$\angle \phi$	Mag	$\angle \phi$
0.5	0.866	-17	0.946	-51.5
1.0	0.830	-40.2	0.807	-115.7
1.5	0.655	-69.3	0.736	173.4
2.0	0.440	-110.3	0.784	121.1
2.5	0.340	-176.5	0.845	89.7
3.0	0.478	120	0.889	69.8
3.5	0.640	86.6	0.917	56.1
4.0	0.756	66.4	0.936	46
4.5	0.831	52.5	0.950	38.2
5.0	0.879	42.3	0.959	31.8
5.5	0.910	34.4	0.966	26.5

Technical Data

Rev. 0, 02/2003

Digital-to-Analog
Converters with Serial
Interface



MOTOROLA
intelligence everywhere™

digitaldna™

MC144110

These devices are not recommended for
New Design. For the complete data sheet please
visit our website at
<http://www.motorola.com/semiconductors>

Ordering Information

Device	Package
MC144110P	Plastic DIP
MC144110DW	SOG Package
MC144111P	Plastic DIP
MC144111DW	SOG Package

The MC144110 and MC144111 are low-cost 6-bit D/A converters with serial interface ports to provide communication with CMOS microprocessors and microcomputers. The MC144110 contains six static D/A converters; the MC144111 contains four converters.

Due to a unique feature of these DACs, the user is permitted easy scaling of the analog outputs of a system. Over a 5 to 15 V supply range, these DACs may be directly interfaced to CMOS MPUs operating at 5 V.

- Direct R-2R Network Outputs
- Buffered Emitter-Follower Outputs
- Serial Data Input
- Digital Data Output Facilitates Cascading
- Direct Interface to CMOS μ P
- Wide Operating Voltage Range: 4.5 to 15 V
- Wide Operating Temperature Range: 0 to 85°C
- Software Information is Contained in Document M68HC11RM/AD

Technical Data

Rev. 0, 02/2003

Encoder and Decoder
Pairs**MOTOROLA**
intelligence everywhere™

digital dna™

MC145026

These devices are not recommended for
New Design. For the complete data sheet please
visit our website at
<http://www.motorola.com/semiconductors>

Ordering Information

Device	Package
MC145026P	Plastic DIP
MC145026D	SOG Package
MC145027P	Plastic DIP
MC145027DW	SOG Package
MC145028P	Plastic DIP
MC145028DW	SOG Package

These devices are designed to be used as encoder/decoder pairs in remote control applications.

The MC145026 encodes nine lines of information and serially sends this information upon receipt of a transmit enable (TE) signal. The nine lines may be encoded with trinary data (low, high, or open) or binary data (low or high). The words are transmitted twice per encoding sequence to increase security.

The MC145027 decoder receives the serial stream and interprets five of the trinary digits as an address code. Thus, 243 addresses are possible. If binary data is used at the encoder, 32 addresses are possible. The remaining serial information is interpreted as four bits of binary data. The valid transmission (VT) output goes high on the MC145027 when two conditions are met. First, two addresses must be consecutively received (in one encoding sequence) which both match the local address. Second, the 4 bits of data must match the last valid data received. The active VT indicates that the information at the Data output pins has been updated.

The MC145028 decoder treats all nine trinary digits as an address which allows 19,683 codes. If binary data is encoded, 512 codes are possible. The VT output goes high on the MC145028 when two addresses are consecutively received (in one encoding sequence) which both match the local address.

- Operating Temperature Range: - 40 to + 85°C
- Very-Low Standby Current for the Encoder: 300 nA Maximum @ 25°C
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- C Oscillator, No Crystal Required
- High External Component Tolerance; Can Use ±5% Components

Chapter Four

Frequency Synthesis – Data Sheets

Device Number	Page Number
PLL Synthesizers	
Single	
MC145151-2	4-3
MC145152-2	4-3
MC145157-2	4-3
MC145158-2	4-3
MC145170-2	4-4

Technical Data

Rev. 0, 02/2003

PLL Frequency
Synthesizer Family



MOTOROLA
intelligence everywhere™

digital dna™

MC145151-2

These devices are not recommended for
New Design. For the complete data sheet please
visit our website at
<http://www.motorola.com/semiconductors>

Ordering Information

Device	Package
MC145151P2	Plastic DIP
MC145151DW2	SOG Package
MC145152P2	Plastic DIP
MC145152DW2	SOG Package
MC145157P2	Plastic DIP
MC145157DW2	SOG Package
MC145158P2	Plastic DIP
MC145158DW2	SOG Package

The devices described in this document are typically used as low-power, phase-locked loop frequency synthesizers. When combined with an external low-pass filter and voltage-controlled oscillator, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a prescaler can be used between the VCO and the synthesizer IC.

These frequency synthesizer chips can be found in the following and other applications:

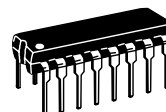
- CATV
- TV Tuning
- AM/FM Radios
- Scanning Receivers
- Two-Way Radios
- Amateur Radio

Technical Data

MC145170-2/D
Rev. 4, 02/2003PLL Frequency
Synthesizer with Serial
Interface**MOTOROLA**
intelligence everywhere™

digital dna™

MC145170-2

**D SUFFIX**
CASE 751B**P SUFFIX**
CASE 648**DT SUFFIX**
CASE 948C

Ordering Information

Device	Operating Temp Range	Package
MC145170P2	$T_A = -40$ to 85°C	Plastic DIP
MC145170D2		SOG-16
MC145170DT2		TSSOP-16

1 Introduction

The new MC145170-2 is pin-for-pin compatible with the MC145170-1. A comparison of the two parts is shown in the table below. The MC145170-2 is recommended for new designs and has a more robust power-on reset (POR) circuit that is more responsive to momentary power supply interruptions. The two devices are actually the same chip with mask options for the POR circuit. The more robust POR circuit draws approximately 20 μA additional supply current. Note that the maximum specification of 100 μA quiescent supply current has not changed.

The MC145170-2 is a single-chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL easy to program. Either a bit- or byte-oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2-byte serial transfer to the 16-bit N register.

The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on-chip support of an external crystal, a programmable reference output, and both single- and double-ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam-load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam-loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.7 to 5.5 V

- Maximum Operating Frequency:
185 MHz @ $V_{in} = 500$ mVpp, 4.5 V Minimum Supply
100 MHz @ $V_{in} = 500$ mVpp, 3.0 V Minimum Supply
- Operating Supply Current:
0.6 mA @ 3.0 V, 30 MHz
1.5 mA @ 3.0 V, 100 MHz
3.0 mA @ 5.0 V, 50 MHz
5.8 mA @ 5.0 V, 185 MHz
- Operating Temperature Range: -40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI Serial Data Port
- See Application Notes AN1207/D and AN1671/D
- Contact Motorola for MC145170 control software.

Table 1. Comparison of the PLL Frequency Synthesizers

Parameter	MC145170-2	MC145170-1
Minimum Supply Voltage	2.7 V	2.5 V
Maximum Input Current, f_{in}	150 μ A	120 μ A
Dynamic Characteristics, f_{in} (Figure 26)	Unchanged	-
Power-On Reset Circuit	Improved	-

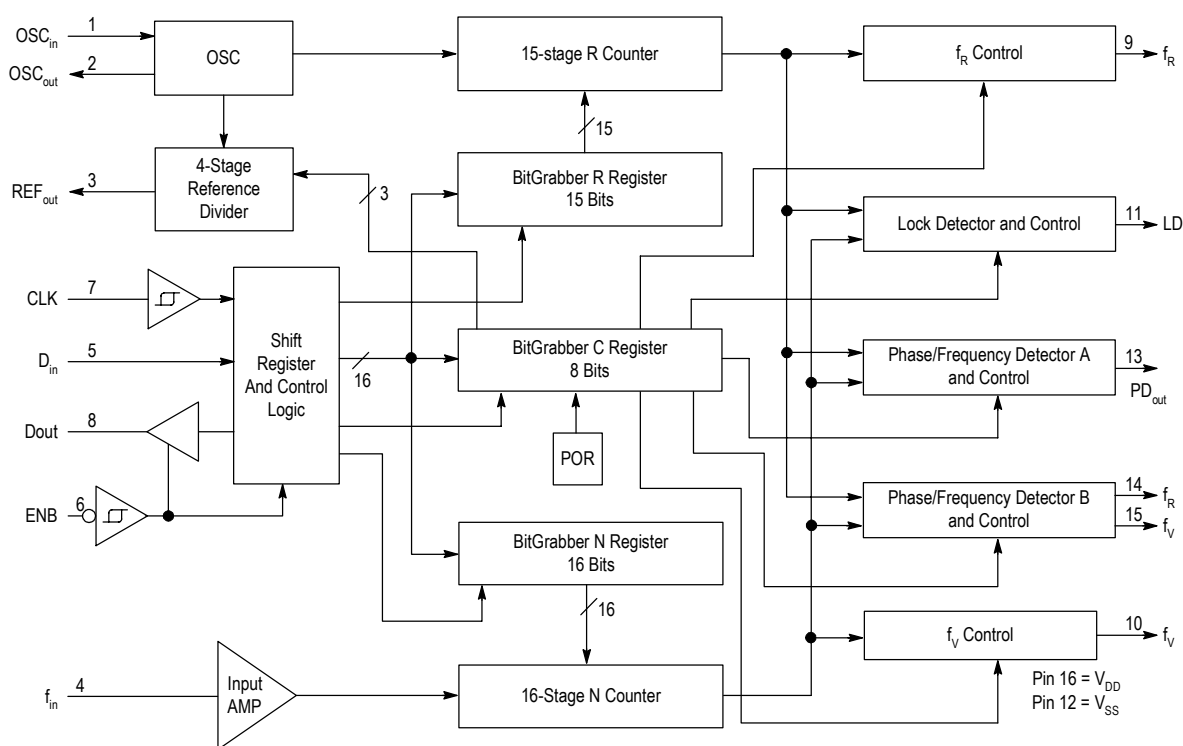


Figure 1. Block Diagram

2 Electrical Characteristics

Table 2. Maximum Ratings (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to 5.5	V
DC Input Voltage	V_{in}	-0.5 to $V_{DD} + 0.5$	V
DC Output Voltage	V_{out}	-0.5 to $V_{DD} + 0.5$	V
DC Input Current, per Pin	I_{in}	± 10	mA
DC Output Current, per Pin	I_{out}	± 20	mA
DC Supply Current, V_{DD} and V_{SS} Pins	I_{DD}	± 30	mA
Power Dissipation, per Package	P_D	300	mW
Storage Temperature	T_{stg}	-65 to 150	$^{\circ}\text{C}$
Lead Temperature, 1 mm from Case for 10 seconds	T_L	260	$^{\circ}\text{C}$

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD data available upon request.

Table 3. Electrical Characteristics (Voltages Referenced to V_{SS} , $T_A = -40$ to 85°C)

Parameter	Test Condition	Symbol	V_{DD} V	Guaranteed Limit	Unit
Power Supply Voltage Range		V_{DD}	-	2.7 to 5.5	V
Maximum Low-Level Input Voltage [Note 1] (D_{in} , CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IL}	2.7 4.5 5.5	0.54 1.35 1.65	V
Minimum High-Level Input Voltage [Note 1] (D_{in} , CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IH}	2.7 4.5 5.5	2.16 3.15 3.85	V
Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		V_{Hys}	2.7 5.5	0.15 0.20	V
Maximum Low-Level Output Voltage (Any Output)	$I_{out} = 20 \mu\text{A}$	V_{OL}	2.7 5.5	0.1 0.1	V
Minimum High-Level Output Voltage (Any Output)	$I_{out} = -20 \mu\text{A}$	V_{OH}	2.7 5.5	2.6 5.4	V
Minimum Low-Level Output Current (PD_{out} , REF_{out} , f_R , f_V , LD, ϕ_R , ϕ_V)	$V_{out} = 0.3 \text{ V}$ $V_{out} = 0.4 \text{ V}$ $V_{out} = 0.5 \text{ V}$	I_{OL}	2.7 4.5 5.5	0.12 0.36 0.36	mA
Minimum High-Level Output Current (PD_{out} , REF_{out} , f_R , f_V , LD, ϕ_R , ϕ_V)	$V_{out} = 2.4 \text{ V}$ $V_{out} = 4.1 \text{ V}$ $V_{out} = 5.0 \text{ V}$	I_{OH}	2.7 4.5 5.5	-0.12 -0.36 -0.36	mA
Minimum Low-Level Output Current (D_{out})	$V_{out} = 0.4 \text{ V}$	I_{OL}	4.5	1.6	mA
Minimum High-Level Output Current (D_{out})	$V_{out} = 4.1 \text{ V}$	I_{OH}	4.5	-1.6	mA
Maximum Input Leakage Current (D_{in} , CLK, $\overline{ENB}$, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	I_{in}	5.5	± 1.0	μA
Maximum Input Current (f_{in})	$V_{in} = V_{DD}$ or V_{SS}	I_{in}	5.5	± 150	μA
Maximum Output Leakage Current (PD_{out}) (D_{out})	$V_{in} = V_{DD}$ or V_{SS} , Output in High-Impedance State	I_{OZ}	5.5 5.5	± 100 ± 5.0	nA μA
Maximum Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS} ; Outputs Open; Excluding f_{in} Amp Input Current Component	I_{DD}	5.5	100	μA

NOTES: 1. When dc coupling to the OSC_{in} pin is used, the pin must be driven rail-to-rail. In this case, OSC_{out} should be floated.

2. The nominal values at 3.0 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5.0 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

Table 3. Electrical Characteristics (Continued) (Voltages Referenced to V_{SS} , $T_A = -40$ to 85°C)

Parameter	Test Condition	Symbol	V_{DD} V	Guaranteed Limit	Unit
Maximum Operating Supply Current	$f_{in} = 500$ mVpp; $OSC_{in} = 1.0$ MHz @ 1.0 Vpp; LD, f_R , f_V , REF_{out} = Inactive and No Connect; OSC_{out} , ϕ_V , ϕ_R , PD_{out} = No Connect; D_{in} , ENB, CLK = V_{DD} or V_{SS}	I_{dd}	-	[Note 2]	mA

NOTES: 1. When dc coupling to the OSC_{in} pin is used, the pin must be driven rail-to-rail. In this case, OSC_{out} should be floated.

2. The nominal values at 3.0 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5.0 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

Table 4. AC Interface Characteristics

($T_A = -40$ to 85°C , $C_L = 50$ pF, Input $t_r = t_f = 10$ ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	f_{clk}	2	2.7 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
Maximum Propagation Delay, CLK to D_{out}	t_{PLH} , t_{PHL}	2, 6	2.7 4.5 5.5	150 85 85	ns
Maximum Disable Time, D_{out} Active to High Impedance	t_{PLZ} , t_{PHZ}	3, 7	2.7 4.5 5.5	300 200 200	ns
Access Time, D_{out} High Impedance to Active	t_{PZL} , t_{PZH}	3, 7	2.7 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
Maximum Output Transition Time, D_{out} CL = 50 pF	t_{TLH} , t_{THL}	2, 6	2.7 4.5 5.5	150 50 50	ns
CL = 200 pF		2, 6	2.7 4.5 5.5	900 150 150	ns
Maximum Input Capacitance - D_{in} , $\overline{ENB}$, CLK	C_{in}		-	10	pF
Maximum Output Capacitance - D_{out}	C_{out}		-	10	pF

Table 5. Timing Requirements ($T_A = -40$ to 85°C , Input $t_r = t_f = 10$ ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Minimum Setup and Hold Times, D_{in} vs CLK	t_{su}, t_h	4	2.7 4.5 5.5	55 40 40	ns
Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	t_{su}, t_h, t_{rec}	5	2.7 4.5 5.5	135 100 100	ns
Minimum Inactive-High Pulse Width, $\overline{ENB}$	$t_{w(H)}$	5	2.7 4.5 5.5	400 300 300	ns
Minimum Pulse Width, CLK	t_w	2	2.7 4.5 5.5	166 125 125	ns
Maximum Input Rise and Fall Times, CLK	t_r, t_f	2	2.7 4.5 5.5	100 100 100	μs

2.1 Switching Waveforms

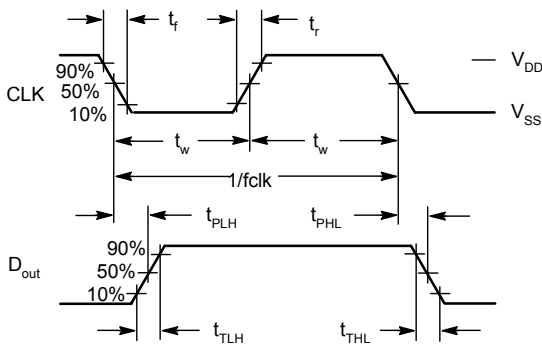


Figure 2.

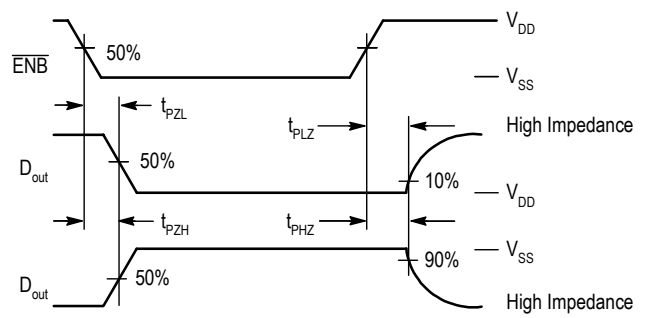


Figure 3.

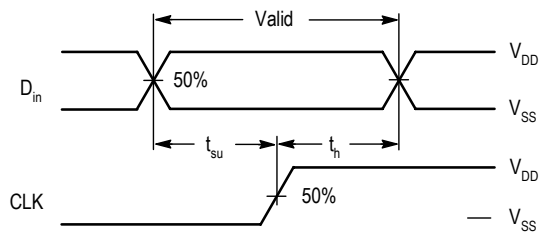


Figure 4.

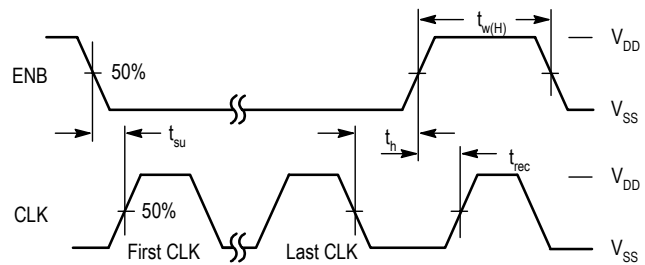


Figure 5.

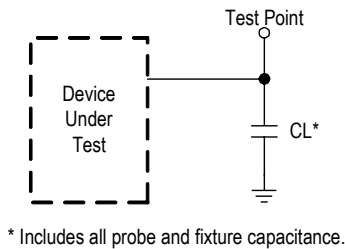


Figure 6. Test Circuit

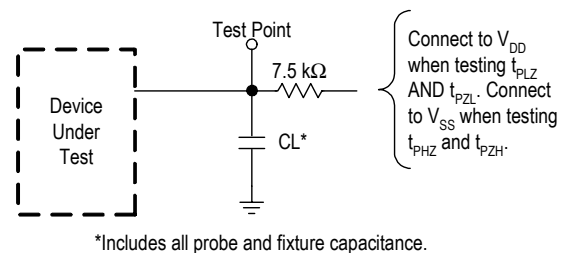
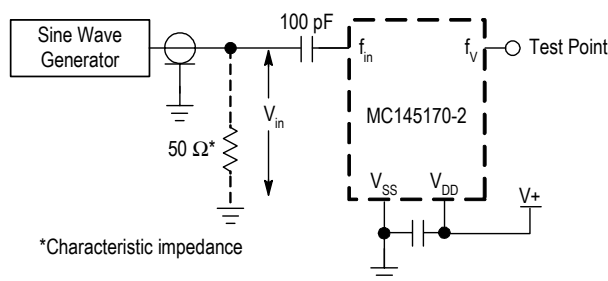


Figure 7. Test Circuit

Table 6. Loop Specifications ($T_A = -40$ to 85°C)

Parameter	Test Condition	Symbol	Figure No.	V_{DD} V	Guaranteed Range		Unit
					Min	Max	
Input Frequency, f_{in} [Note]	$V_{in} \geq 500$ mVpp Sine Wave, N Counter Set to Divide Ratio Such that $f_V \leq 2.0$ MHz	f	8	2.7 3.0 4.5 5.5	5.0 5.0 25 45	80 100 185 185	MHz
Input Frequency, OSC_{in} Externally Driven with ac-coupled Signal	$V_{in} \geq 1.0$ Vpp Sine Wave, $OSC_{out} =$ No Connect, R Counter Set to Divide Ratio Such that $f_R \leq 2$ MHz	f	9	2.7 3.0 4.5 5.5	1.0* 1.0* 1.0* 1.0*	22 25 30 35	MHz
Crystal Frequency, OSC_{in} and OSC_{out}	$C1 \leq 30$ pF $C2 \leq 30$ pF Includes Stray Capacitance	f_{XTAL}	11	2.7 3.0 4.5 5.5	2.0 2.0 2.0 2.0	12 12 15 15	MHz
Output Frequency, REF_{out}	$C_L = 30$ pF	f_{out}	12, 14	2.7 4.5 5.5	dc dc dc	- 10 10	MHz
Operating Frequency of the Phase Detectors		f		2.7 4.5 5.5	dc dc dc	- 2.0 2.0	MHz
Output Pulse Width, ϕ_R , ϕ_V , and LD	f_R in Phase with f_V $C_L = 50$ pF	t_w	13, 14	2.7 4.5 5.5	- 20 16	- 100 90	ns
Output Transition Times, ϕ_R , ϕ_V , LD, f_R , and f_V	$C_L = 50$ pF	t_{TLH} , t_{THL}	13, 14	2.7 4.5 5.5	- - -	- 65 60	ns
Input Capacitance f_{in} OSC_{in}		C_{in}	- -	- -	- -	7.0 7.0	pF

* IF lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac-coupled case. Also, see Figure 25 for dc coupling.

Figure 8. Test Circuit, f_{in}

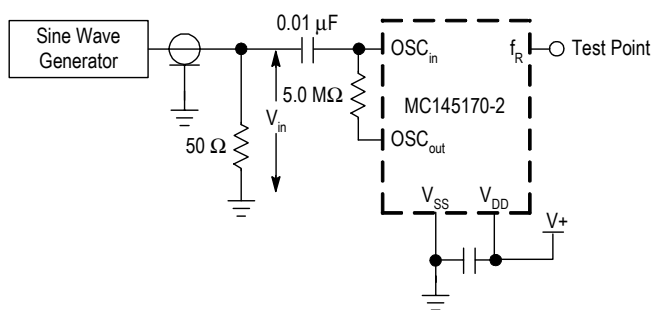


Figure 9. Test Circuit, OSC Circuitry Externally Driven [Note]

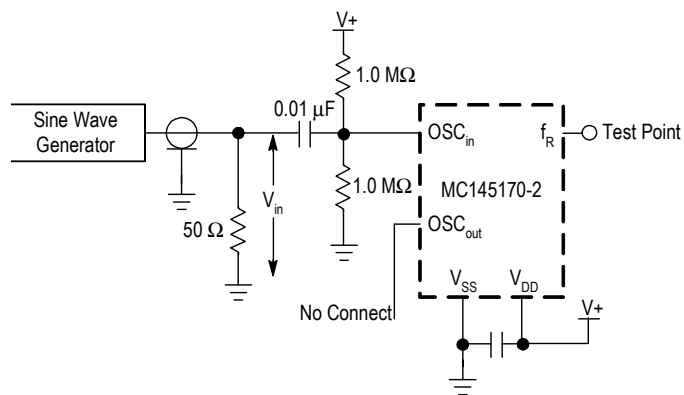


Figure 10. Circuit to Eliminate Self-Oscillation, OSC Circuitry Externally Driven [Note]

NOTE: Use the circuit of Figure 10 to eliminate self-oscillation of the OSCin pin when the MC145170-2 has power applied with no external signal applied at Vin. (Self-oscillation is not harmful to the MC145170-2 and does not damage the IC.)

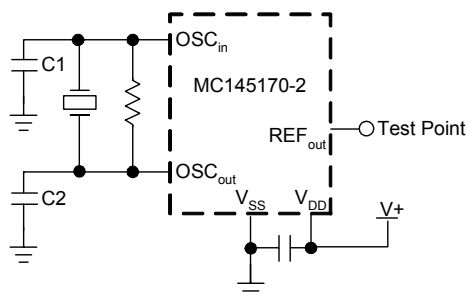


Figure 11. Test Circuit, OSC Circuit with Crystal

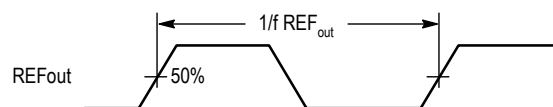


Figure 12. Test Circuit

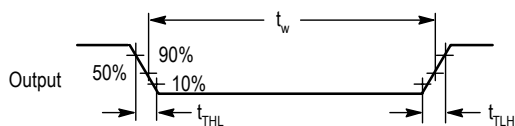
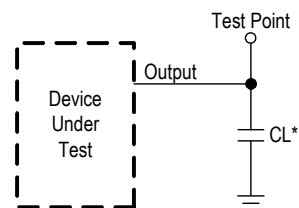


Figure 13. Switching Waveform



*Includes all probe and fixture capacitance.

Figure 14. Test Load Circuit

3 Pin Connections

3.1 Digital Interface Pins

D_{in} Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low-to-high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15-bit transfer (see Table 7). An optional pattern which resets the device is shown in Figure 15. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{\text{ENB}}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 15, 16, 17, and 18.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 7. Register Access
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
9 to 13	See Figure 15	(Reset)
8	C Register	C7, C6, C5, ..., C0
16	N Register	N15, N14, N13, ..., N0
15 or 24	R Register	R14, R13, R12, ..., R0
Other Values ≤ 32	None	
Values > 32	See Figures 27 to 34	

CLK

Serial Data Clock Input (Pin 7)

Low-to-high transitions on Clock shift bits available at D_{in}, while high-to-low transitions shift bits from D_{out}. The chip's 16-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four to eight clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 7 and Figures 15, 16, 17, and 18). For cascaded devices, see Figures 27 to 34.

CLK typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE: To guarantee proper operation of the power-on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 2.7 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 15 must be used.

ENB**Active-Low Enable Input (Pin 6)**

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{\text{ENB}}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high-impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{\text{ENB}}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and ENB is taken back high. The low-to-high transition on $\overline{\text{ENB}}$ transfers data to the C, N, or R register depending on the data stream length per Table 7.

NOTE: Transitions on $\overline{\text{ENB}}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{\text{ENB}}$ is high and CLK is low.

This input is also Schmitt-triggered and switches near 50% of V_{DD} , thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of D_{in} for more information.

 D_{out} **Three-State Serial Data Output (Pin 8)**

Data is transferred out of the 16-1/2-stage shift register through D_{out} on the high-to-low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D_{out} could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in-line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system and permits cascading devices.

3.2 Reference Pins

 $\text{OSC}_{\text{in}}/\text{OSC}_{\text{out}}$ **Reference Oscillator Input/Output (Pins 1, 2)**

These pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1.0 to 5.0 M Ω is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 11.

5 M Ω is required across the OSC_{in} and OSC_{out} pins in the ac-coupled case (see Figure 9 or alternate circuit Figure 10). *OSC_{out} is an internal node on the device and should not be used to drive any loads (i.e., OSC_{out} is unbuffered).* However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 Vpp; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings virtually rail-to-rail (V_{DD} to V_{SS}), then dc coupling can be used. In the dc-coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin. See Figure 25.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}**Reference Frequency Output (Pin 3)**

This output is the buffered output of the crystal-generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 16).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on-chip power-on-initialize circuit forces REF_{out} to the OSC_{in} divided-by-8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

3.3 Counter Output Pins

f_R**R Counter Output (Pin 9)**

This signal is the buffered output of the 15-stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 17). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz.

When activated, the f_R signal appears as normally low and pulses high. The pulse width is 4.5 cycles of the OSC_{in} pin signal, except when a divide ratio of 1 is selected. When 1 is selected, the OSC_{in} signal is buffered and appears at the f_R pin.

f_V**N Counter Output (Pin 10)**

This signal is the buffered output of the 16-stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz.

When activated, the f_V signal appears as normally low and pulses high.

3.4 Loop Pins

f_{in}**Frequency Input (Pin 4)**

This pin is a frequency input from the VCO. This pin feeds the on-chip amplifier which drives the N counter. This signal is normally sourced from an external voltage-controlled oscillator (VCO), and is ac-coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 25). The frequency capability of this input is dependent on the supply voltage as listed in Table 6, Loop Specifications. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin. See Figure 25.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}

Single-Ended Phase/Frequency Detector Output (Pin 13)

This is a three-state output for use as a loop error signal when combined with an external low-pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 16)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R : negative pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R : positive pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R : positive pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R : negative pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high-impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V

Double-Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 16)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R : ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R : ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R : ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R : ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD**Lock Detector Output (Pin 11)**

This output is essentially at a high level with narrow low-going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 19).

This output can be enabled and disabled via the C register (patented). Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false “lock” signal. If unused, LD should be disabled and left open.

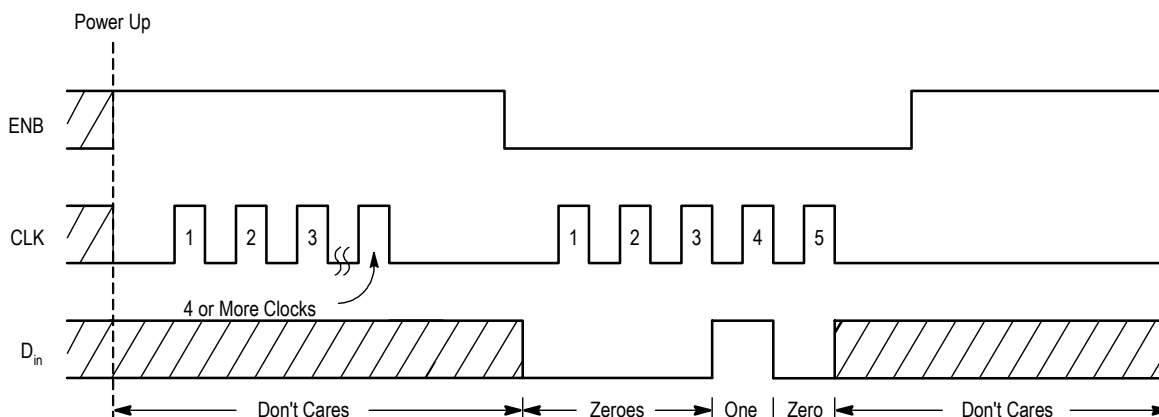
3.5 Power Supply **V_{DD}** **Most Positive Supply Potential (Pin 16)**

This pin may range from 2.7 to 5.5 V with respect to V_{SS} .

For optimum performance, V_{DD} should be bypassed to V_{SS} using low-inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

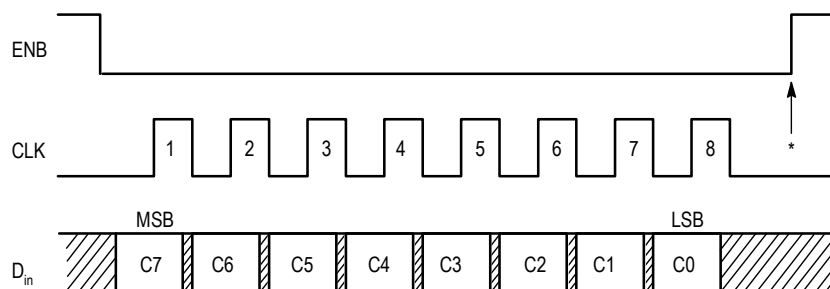
 V_{SS} **Most Negative Supply Potential (Pin 12)**

This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.



NOTE: This initialization sequence is usually not necessary because the on-chip power-on reset circuit performs the initialization function. However, this initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (Pin 7) toggles or floats upon power up, use the above sequence to reset the device. Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.7 V, but not down to at least 1 V (for example, the supply drops down to 2 V). This is necessary because the on-chip power-on reset is only activated when the supply ramps up from a voltage below approximately 1.0 V.

Figure 15. Reset Sequence



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 - POL:

Select the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 19. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 - PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high-impedance state. This bit is cleared low at power up.

C5 - LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 - C2, OSC2 - OSC0:

Reference output controls which determines the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$ (POR Default)
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

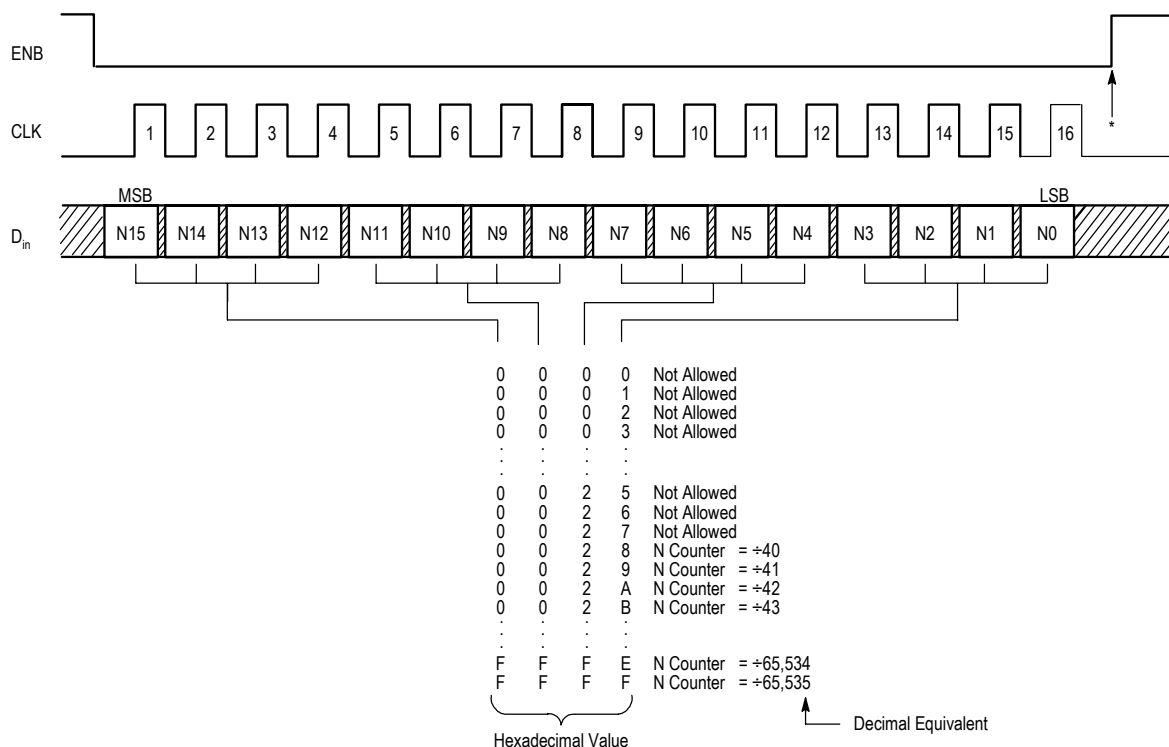
C1 - f_V E: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

C0 - f_R E: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 16. C Register Access and Format (8 Clock Cycles are Used)

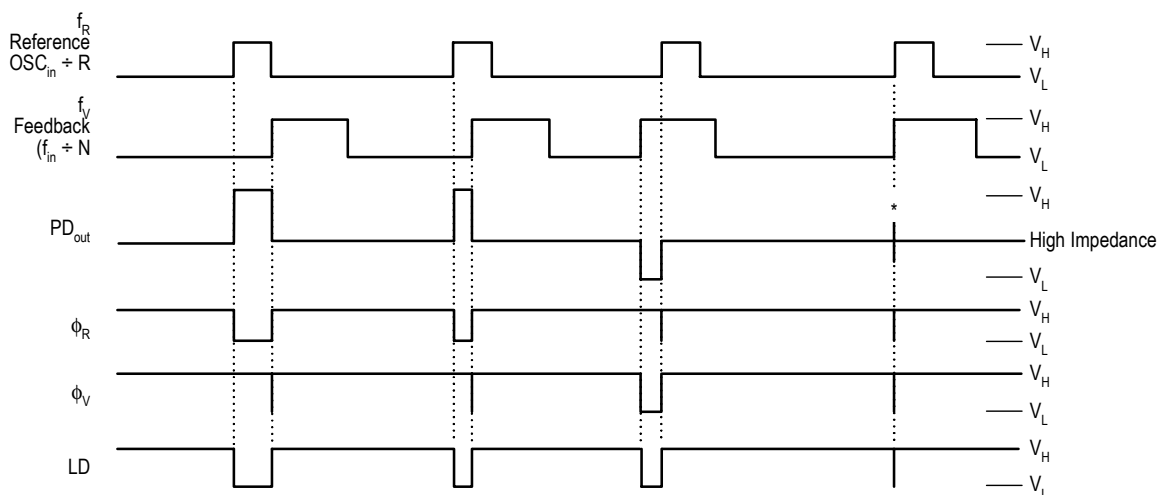


MC145170-2
4-19



*At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam-loaded and begin counting down together.

Figure 18. N Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level

V_L = Low voltage level

*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.

NOTE: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PD_{out} , ϕ_R and ϕ_V are shown with the polarity bit (POL) = low; see Figure 16 for POL.

Figure 19. Phase/Frequency Detector and Lock Detector Output Waveforms

4 Design Considerations

4.1 Crystal Oscillator Considerations

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

4.1.1 Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figures 9 and 10).

For additional information about TCXOs, visit *motorola.com* on the world wide web.

4.1.2 Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 20.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequencies listed in Table 6, **Loop Specifications**. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \times C2}{C1 + C2}$$

where

C_{in} = 5.0 pF (see Figure 21)

C_{out} = 6.0 pF (see Figure 21)

C_a = 1.0 pF (see Figure 21)

C1 and C2 = external capacitors (see Figure 21)

C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

A good design practice is to pick a small value for C1, such as 5 to 10 pF. Next, C2 is calculated. C1 < C2 results in a more robust circuit for start-up and is more tolerant of crystal parameter variations.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 22. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 20. limits the drive level. The use of R1 is not necessary in most cases.

Design Considerations **Freescale Semiconductor, Inc.**

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 8).

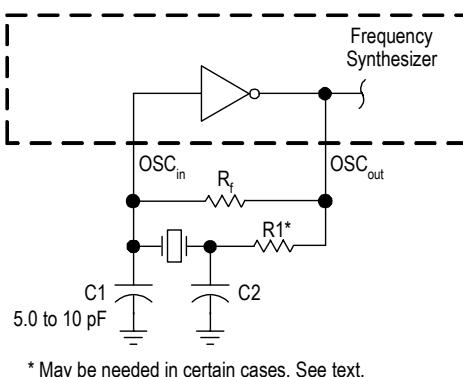


Figure 20. Pierce Crystal Oscillator Circuit

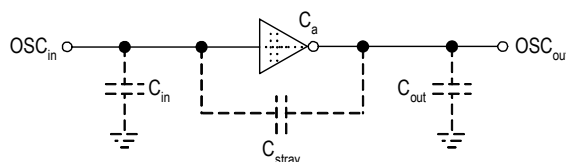
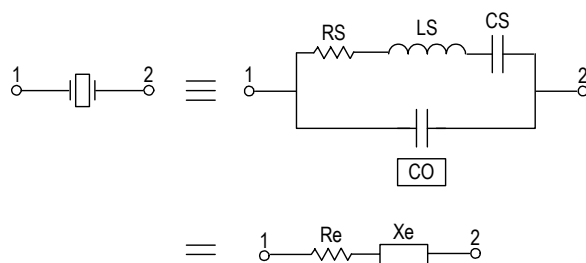


Figure 21. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 22. Equivalent Crystal Networks

Recommended Reading

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit-Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

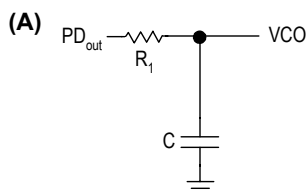
D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

Contact Motorola for MC145170-2 control software.

Table 8. Partial List of Crystal Manufacturers

CTS Corp.
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

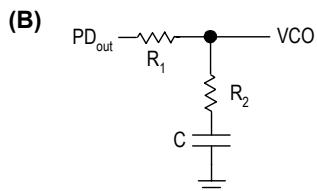
NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1 C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

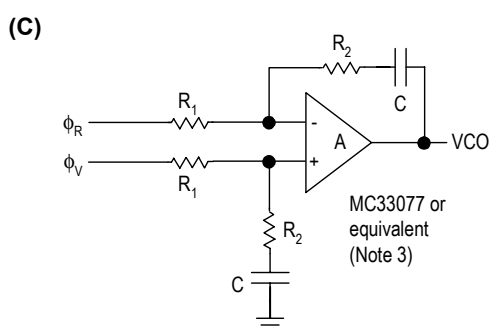
$$F(s) = \frac{1}{R_1 s C + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\omega_n \left(R_2 C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2 s C + 1}{(R_1 + R_2)s C + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

$$F(s) = \frac{R_2 s C + 1}{R_1 s C}$$

Notes:

1. For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n .
2. The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp.
3. For the latest information on MC33077 or equivalent, see the Motorola IC web site at <http://www.motorola.com/semiconductors>.

Denifitions:

N = Total Division Ratio in Feedback Loop

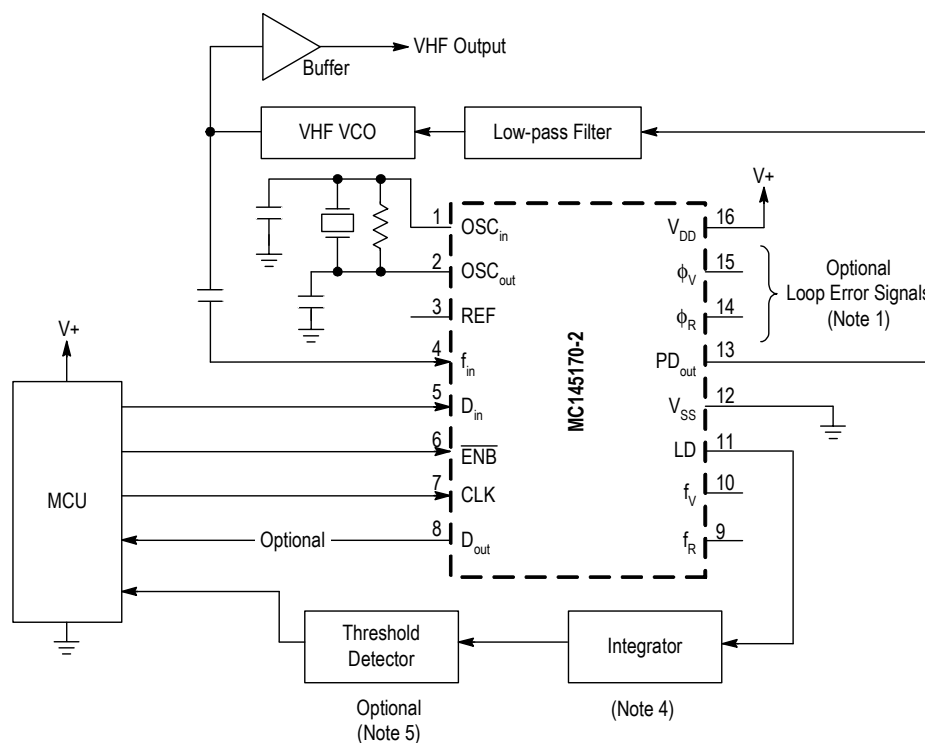
K_ϕ (Phase Detector Gain) = $VDD/4p$ volts per radian for PDout

K_ϕ (Phase Detector Gain) - $VDD/2p$ volts per radian for fV and fR

$$K_{VCO}(\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta = 0.7$ and a natural loop frequency $\omega_n = (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R -related VCO standards.

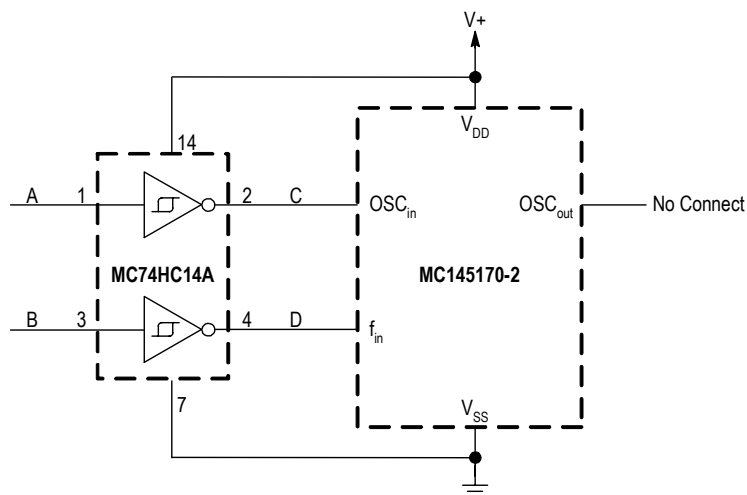
Figure 23. Phase-Locked Loop - Low Pass Filter Design



NOTES:

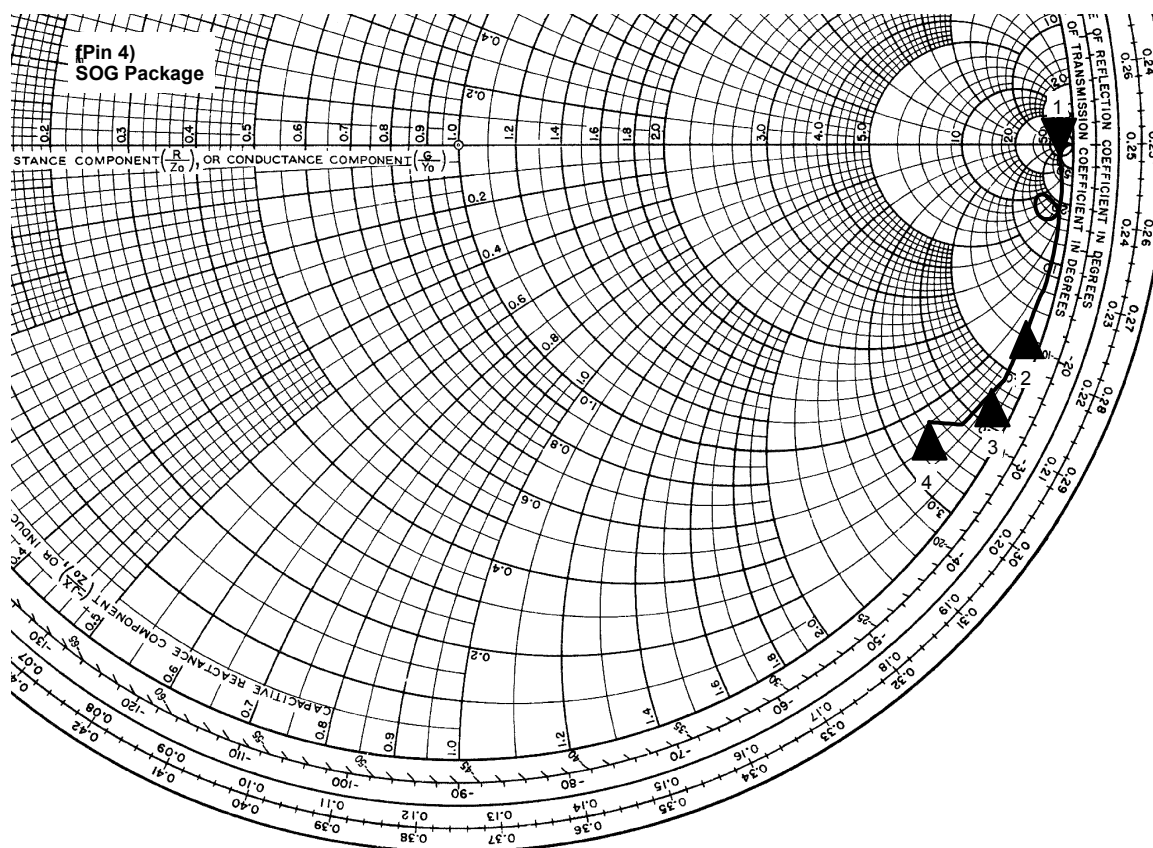
1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low-inductance capacitors.
3. The R counter is programmed for a divide value = OSC_{in}/f_R . Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N$, where N is the divide value of the N counter.
4. May be an R-C low-pass filter.
5. May be a bipolar transistor.

Figure 24. Example Application

**NOTE:**

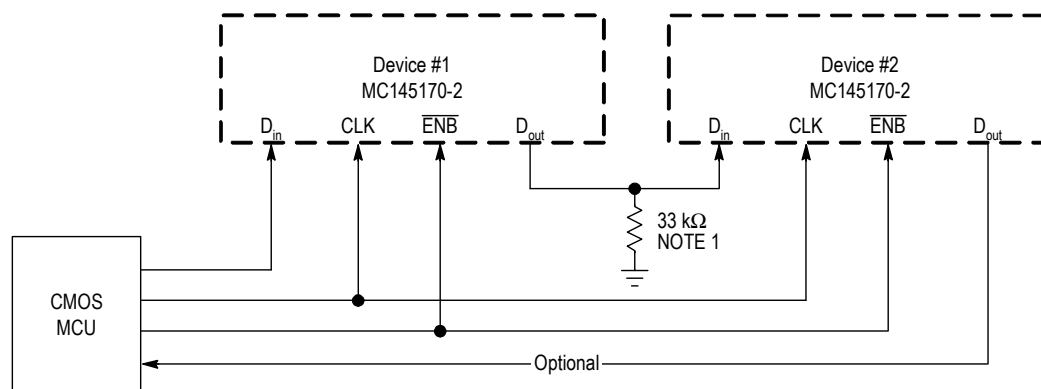
The signals at Points A and B may be low-frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail-to-rail signal swings. With signals as described at Points C and D, the MC145170-2 is guaranteed to operate down to a frequency as low as dc. Refer to the MC74HC14A data sheet for input switching levels and hysteresis voltage range.

Figure 25. Low Frequency Operation Using DC Coupling



Marker	Frequency (MHz)	Resistance (Ω)	Reactance (Ω)	Capacitance (pF)
1	5	2390	-5900	5.39
2	100	39.2	-347	4.58
3	150	25.8	-237	4.48
4	185	42.6	-180	4.79

Figure 26. Input Impedance at f_{in} - Series Format ($R + jX$) (5.0 MHz to 185 MHz)



NOTES:

1. The 33 k Ω resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three-state output.)
2. See related Figures 28, 29, and 30.

Figure 27. Cascading Two MC145170-2 Devices

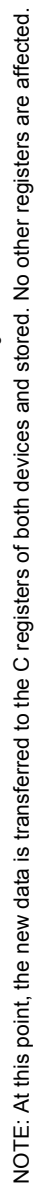


Figure 28. Accessing the C Registers of Two Cascaded MC145170-2 Devices

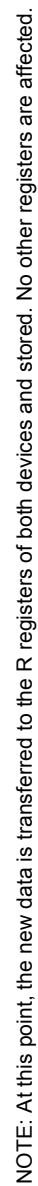
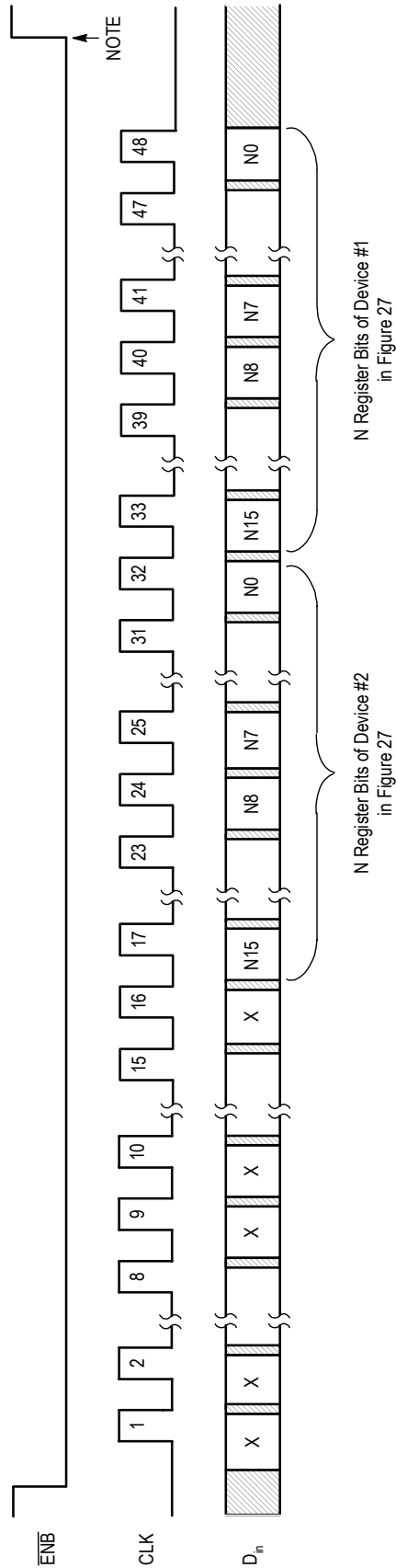
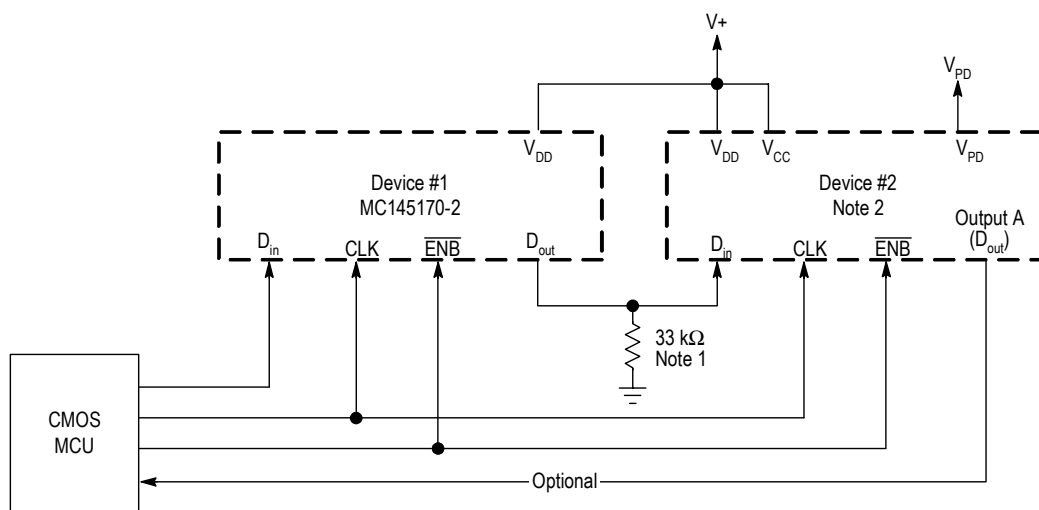


Figure 29. Accessing the R Registers of Two Cascaded MC145170-2 Devices



NOTE: At this point, the new data is transferred to the N registers of both devices and stored. No other registers are affected.

Figure 30. Accessing the N Registers of Two Cascaded MC145170-2 Devices



NOTES:

1. The $33\text{ k}\Omega$ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three-state output.)
2. This PLL Frequency Synthesizer may be a MC145190, MC145191, MC145192, MC145200, or MC145201.
3. See related Figures 32, 33, and 34.

Figure 31. Cascading Two Different Device Types

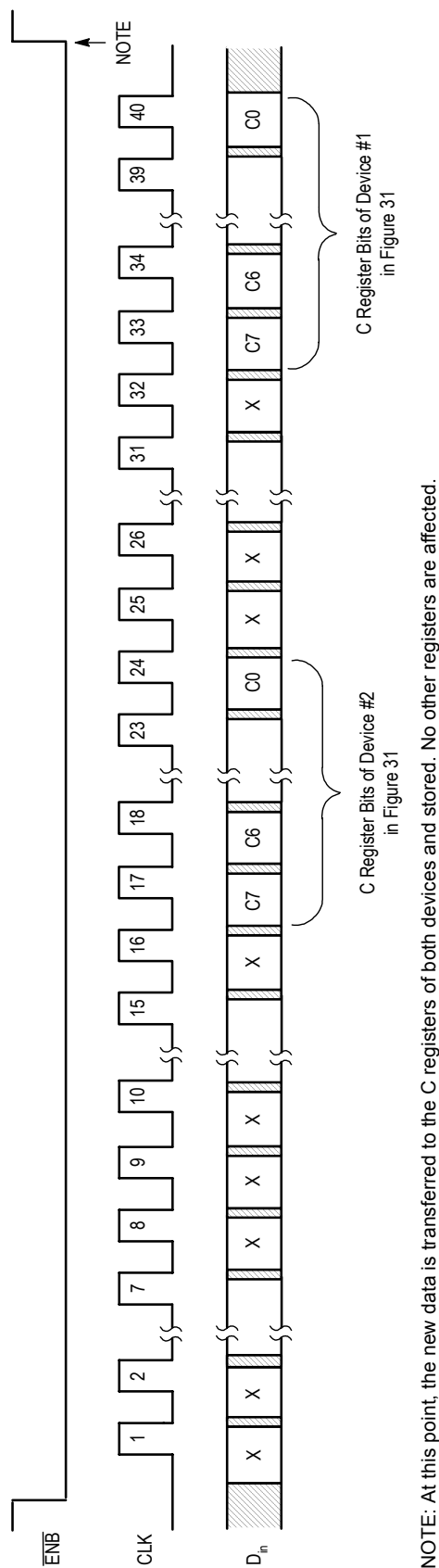


Figure 32. Accessing the C Registers of Two Different Device Types

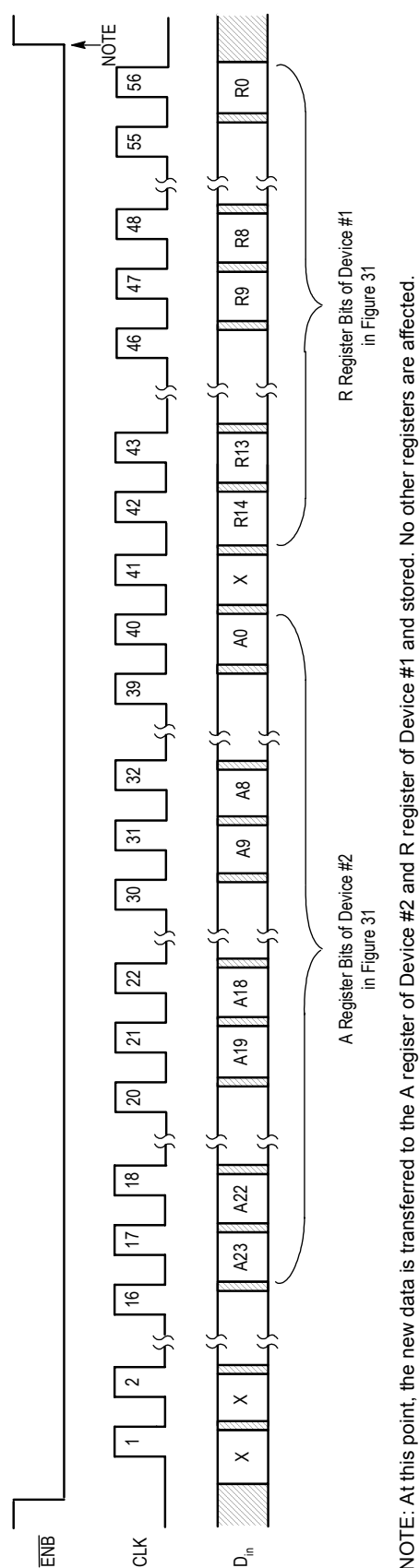


Figure 33. Accessing the A and R Registers of Two Different Device Types

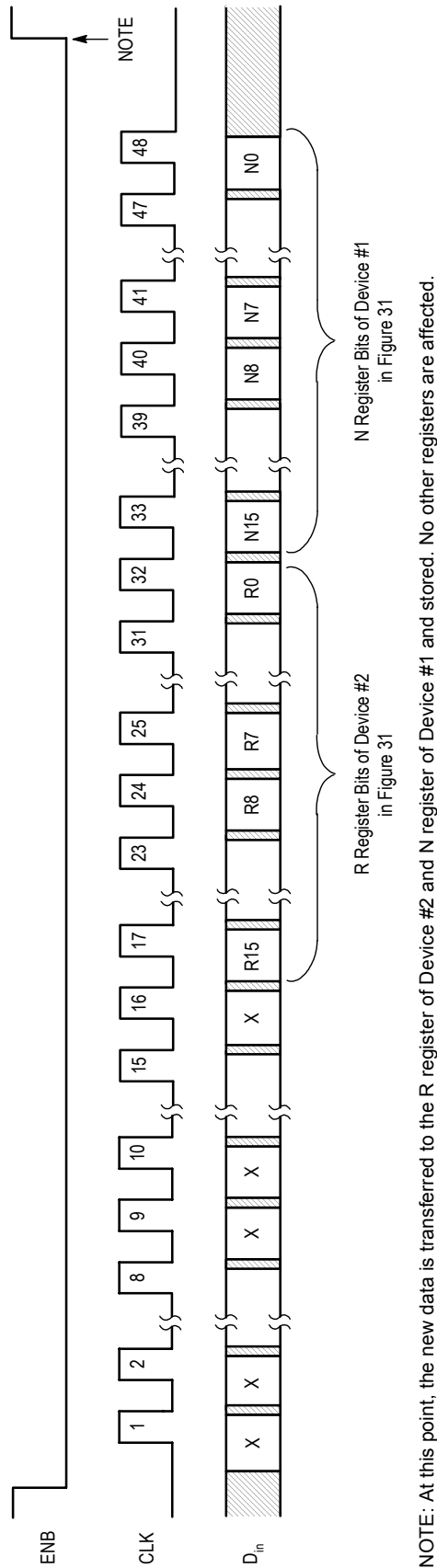


Figure 34. Accessing the R and N Registers of Two Different Device Types

Chapter Five

Motorola RF Transistors –
Data Sheets

Device Number	Page Number	Device Number	Page Number
MBC13900	5-3	MRF9080LSR3	5-210
MRF281SR1	5-26	MRF9085	5-218
MRF281ZR1	5-26	MRF9085R3	5-218
MRF282SR1	5-30	MRF9085SR3	5-218
MRF282ZR1	5-30	MRF9085LSR3	5-218
MRF284R1	5-37	MRF9100	5-224
MRF284LSR1	5-37	MRF9100R3	5-224
MRF372	5-46	MRF9100SR3	5-224
MRF373AR1	5-57	MRF9120	5-233
MRF373ALSR1	5-57	MRF9120S	5-233
MRF374A	5-62	MRF9130L	5-241
MRF1511T1	5-72	MRF9130LR3	5-241
MRF1513T1	5-82	MRF9130LSR3	5-241
MRF1517T1	5-94	MRF9135L	5-248
MRF1518T1	5-106	MRF9135LR3	5-248
MRF1535T1	5-118	MRF9135LSR3	5-248
MRF1535FT1	5-118	MRF9180	5-255
MRF1550T1	5-128	MRF9180S	5-255
MRF1550FT1	5-128	MRF18030AR3	5-263
MRF1570T1	5-137	MRF18030ASR3	5-263
MRF1570FT1	5-137	MRF18030BR3	5-268
MRF6522-70	5-151	MRF18030BSR3	5-268
MRF6522-70R3	5-151	MRF18060A	5-273
MRF9002R2	5-158	MRF18060AR3	5-273
MRF9030R1	5-165	MRF18060ALSR3	5-273
MRF9030LSR1	5-165	MRF18060ASR3	5-273
MRF9030MR1	5-172	MRF18060B	5-279
MRF9030MBR1	5-172	MRF18060BR3	5-279
MRF9045R1	5-180	MRF18060BLSR3	5-279
MRF9045LSR1	5-180	MRF18060BSR3	5-279
MRF9045MR1	5-186	MRF18085A	5-285
MRF9045MBR1	5-186	MRF18085AR3	5-285
MRF9060R1	5-194	MRF18085ALSR3	5-285
MRF9060LSR1	5-194	MRF18085B	5-290
MRF9060MR1	5-202	MRF18085BR3	5-290
MRF9060MBR1	5-202	MRF18085BLSR3	5-290
MRF9080	5-210	MRF18090A	5-297
MRF9080R3	5-210	MRF18090AS	5-297
MRF9080SR3	5-210	MRF18090B	5-303

Freescale Semiconductor, Inc.

Device Number	Page Number	Device Number	Page Number
MRF18090BS	5-303	MRF21060SR3	5-375
MRF19030R3	5-309	MRF21085	5-381
MRF19030SR3	5-309	MRF21085R3	5-381
MRF19045R3	5-314	MRF21085SR3	5-381
MRF19045SR3	5-314	MRF21085LSR3	5-381
MRF19060	5-321	MRF5S21090L	5-389
MRF19060R3	5-321	MRF5S21090LR3	5-389
MRF19060SR3	5-321	MRF5S21090LSR3	5-389
MRF19085	5-327	MRF21090	5-396
MRF19085R3	5-327	MRF21090S	5-396
MRF19085SR3	5-327	MRF21120	5-401
MRF19085LSR3	5-327	MRF21125	5-408
MRF19090	5-335	MRF21125S	5-408
MRF19090S	5-335	MRF21125SR3	5-408
MRF19090SR3	5-335	MRF5S21130	5-415
MRF19120	5-341	MRF5S21130R3	5-415
MRF19120S	5-341	MRF5S21130S	5-415
MRF19125	5-348	MRF5S21130SR3	5-415
MRF19125S	5-348	MRF5S21150	5-422
MRF19125SR3	5-348	MRF5S21150R3	5-422
MRF21010R1	5-356	MRF5S21150S	5-422
MRF21010LSR1	5-356	MRF5S21150SR3	5-422
MRF21030R3	5-362	MRF5P21180	5-429
MRF21030SR3	5-362	MRF21180	5-436
MRF21045R3	5-367	MRF21180S	5-436
MRF21045SR3	5-367	MRFG35003M6T1	5-444
MRF21060	5-375	MRFG35010	5-451
MRF21060R3	5-375	MRFG35010MT1	5-459

Technical Data

MBC13900/D
Rev. 0, 06/2002

NPN Silicon
Low Noise Transistor



MOTOROLA
intelligence everywhere™

digital dna™

MBC13900



(Scale 2:1)

Package Information

Plastic Package
Case 318M
(SOT-343)

Ordering Information

Device	Marking	Package
MBC13900T1	900	SOT-343

The MBC13900 is a high performance transistor fabricated using Motorola's 15 GHz f_T bipolar IC process. It is housed in the 4-lead SC-70 (SOT-343) surface mount plastic package resulting in a parasitic effect reduction and RF performance enhancements. The high performance at low power makes the MBC13900 suitable for front-end applications in portable wireless systems such as pagers, cellular and cordless phones.

- Low Noise Figure, $NF_{min} = 0.8$ dB (Typ) @ 0.9 GHz, 2.0 V and 5.0 mA
- Maximum Stable Gain, 22 dB @ 0.9 GHz, 2.0 V and 5.0 mA
- Output Third Order Intercept, $OIP3 = 18$ dBm (Typ) @ 2.0 V and 5.0 mA
- Ultra small SOT-343 Surface Mount Package
- Available Only in Tape and Reel Packaging

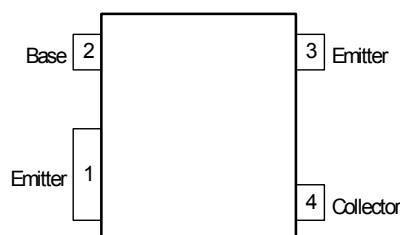


Figure 1. Pin Connections

1 Electrical Specifications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	6.5	Vdc
Collector-Base Voltage	V_{CBO}	8.0	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Power Dissipation @ $T_C = 75^\circ\text{C}$ Derate Linearity above $T_C = 75^\circ\text{C}$ at	$P_{D(max)}$	0.188 2.5	W mW/ $^\circ\text{C}$
Collector Current-Continuous	I_C	20	mA
Maximum Junction Temperature	$T_{J(max)}$	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 150	$^\circ\text{C}$

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤ 400 V and Machine Model (MM) ≤ 50 V. Additional ESD data available upon request.

Table 2. Thermal Characteristic

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	400	$^\circ\text{C/W}$

NOTES: To calculate the junction temperature use $T_J = (P_D \times R_{\theta JC}) + T_C$. The case temperature measured on collector lead adjacent to the package body.

Table 3. Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
OFF Characteristic [Note 1]					
Collector-Emitter Breakdown Voltage ($I_C = 0.1$ mA, $I_B = 0$)	$V_{(BR)CEO}$	6.5	7.5	-	Vdc
Collector-Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	8.0	12	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = 0.1$ mA, $I_C = 0$)	$V_{(BR)EBO}$	3.0	4.0	-	Vdc
Collector Cutoff Current ($V_{CB} = 7.0$ V, $I_E = 0$)	I_{CBO}	-	-	0.1	∞ A
Emitter Cutoff Current ($V_{EB} = 2.0$ V, $I_C = 0$)	I_{EBO}	-	-	0.1	∞ A
Base Cutoff Current ($V_{CE} = 5.0$ V, $I_B = 0$)	I_{CEO}	-	-	0.1	∞ A
ON Characteristic [Note 1]					
DC Current Gain ($V_{CE} = 2.0$ V, $I_C = 5.0$ mA)	h_{FE}	100	-	200	-

Table 3. Electrical Characteristics (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Current Gain Bandwidth Product ($V_{CE} = 2.0 \text{ V}$, $I_C = 15 \text{ mA}$, $f = 0.9 \text{ GHz}$)	f_t	-	15	-	GHz
Performance Characteristic					
Insertion Gain $V_{CE} = 2.0 \text{ V}$, $I_C = 5.0 \text{ mA}$, $f = 0.9 \text{ GHz}$ $V_{CE} = 2.0 \text{ V}$, $I_C = 5.0 \text{ mA}$, $f = 1.9 \text{ GHz}$ $V_{CE} = 3.0 \text{ V}$, $I_C = 3.0 \text{ mA}$, $f = 0.9 \text{ GHz}$ $V_{CE} = 3.0 \text{ V}$, $I_C = 3.0 \text{ mA}$, $f = 1.9 \text{ GHz}$	$ S_{21} ^2$	18.5 13.5 16.5 12.5	19.5 14.5 17.5 13.5	- - - -	dB
Maximum Stable Gain and/or Maximum Available Gain [Note 2] $V_{CE} = 2.0 \text{ V}$, $I_C = 5.0 \text{ mA}$, $f = 0.9 \text{ GHz}$ $V_{CE} = 2.0 \text{ V}$, $I_C = 5.0 \text{ mA}$, $f = 1.9 \text{ GHz}$ $V_{CE} = 3.0 \text{ V}$, $I_C = 3.0 \text{ mA}$, $f = 0.9 \text{ GHz}$ $V_{CE} = 3.0 \text{ V}$, $I_C = 3.0 \text{ mA}$, $f = 1.9 \text{ GHz}$	MSG, MAG	22 18 21 17.5	23 19 22 18.5	- - - -	dB
Minimum Noise Figure $V_{CE} = 2.0 \text{ V}$, $I_C = 5.0 \text{ mA}$, $f = 0.9 \text{ GHz}$ $V_{CE} = 2.0 \text{ V}$, $I_C = 5.0 \text{ mA}$, $f = 1.9 \text{ GHz}$ $V_{CE} = 3.0 \text{ V}$, $I_C = 3.0 \text{ mA}$, $f = 0.9 \text{ GHz}$ $V_{CE} = 3.0 \text{ V}$, $I_C = 3.0 \text{ mA}$, $f = 1.9 \text{ GHz}$	NF_{min}	- - - -	0.8 0.9 0.8 0.9	0.9 1.1 0.9 1.1	dB
Associated Gain at Minimum Noise Figure $V_{CE} = 2.0 \text{ V}$, $I_C = 5.0 \text{ mA}$, $f = 0.9 \text{ GHz}$ $V_{CE} = 2.0 \text{ V}$, $I_C = 5.0 \text{ mA}$, $f = 1.9 \text{ GHz}$ $V_{CE} = 3.0 \text{ V}$, $I_C = 3.0 \text{ mA}$, $f = 0.9 \text{ GHz}$ $V_{CE} = 3.0 \text{ V}$, $I_C = 3.0 \text{ mA}$, $f = 1.9 \text{ GHz}$	G_{NF}	- - - -	22 16 21 15	- - - -	dB
Output Third Order Intercept [Note 3] $(V_{CE} = 2.0 \text{ V}, I_C = 5.0 \text{ mA}, f = 0.9 \text{ GHz})$ $(V_{CE} = 2.0 \text{ V}, I_C = 5.0 \text{ mA}, f = 1.9 \text{ GHz})$ $(V_{CE} = 3.0 \text{ V}, I_C = 3.0 \text{ mA}, f = 0.9 \text{ GHz})$ $(V_{CE} = 3.0 \text{ V}, I_C = 3.0 \text{ mA}, f = 1.9 \text{ GHz})$	OIP3	- - - -	18 21 13.5 19	- - - -	dBm

NOTES: 1. Pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$ pulsed.

2. Maximum Available Gain and Maximum Stable Gain are defined by the K factor as follows:

$$MAG = \left| \frac{S_{21}}{S_{12}} (K \pm \sqrt{K^2 - 1}) \right|, \text{ if } K > 1, \text{ MSG} = \left| \frac{S_{21}}{S_{12}} \right|, \text{ if } K < 1$$

3. Z_{in} and Z_{out} matched for optimum IP3.

2 Typical Performance Characteristics

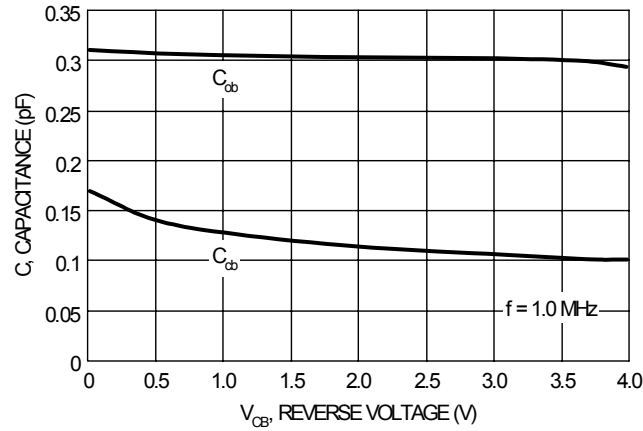


Figure 2. Capacitance versus Voltage

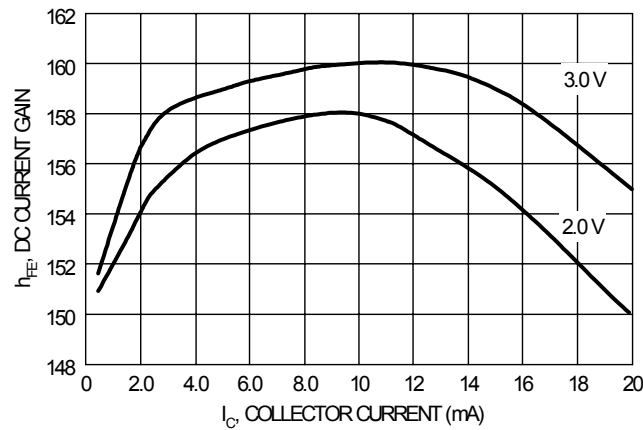


Figure 3. h_{FE} , DC Current Gain versus Collector Current

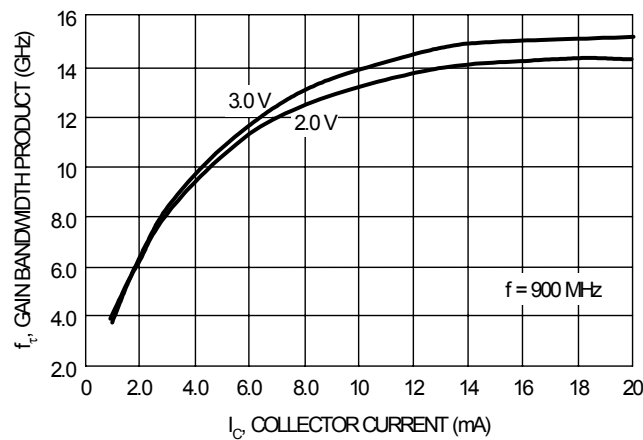


Figure 4. Gain-Bandwidth Product versus Collector Current

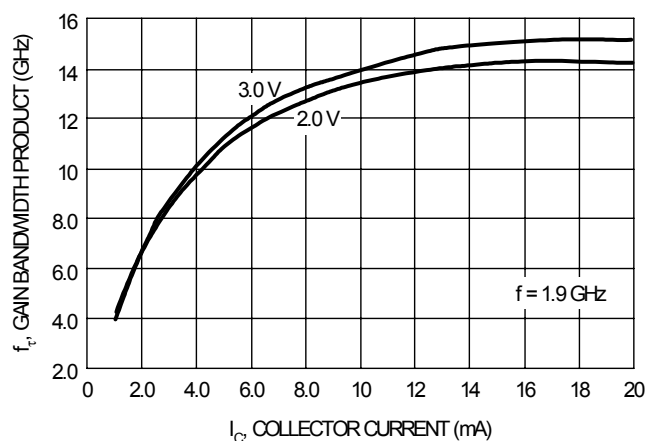


Figure 5. Gain-Bandwidth Product versus Collector Current

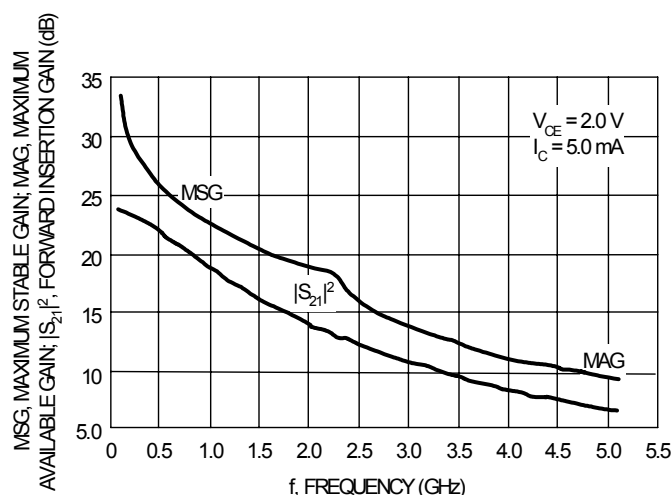


Figure 6. Maximum Stable/Available gain and Forward Insertion Gain versus Frequency

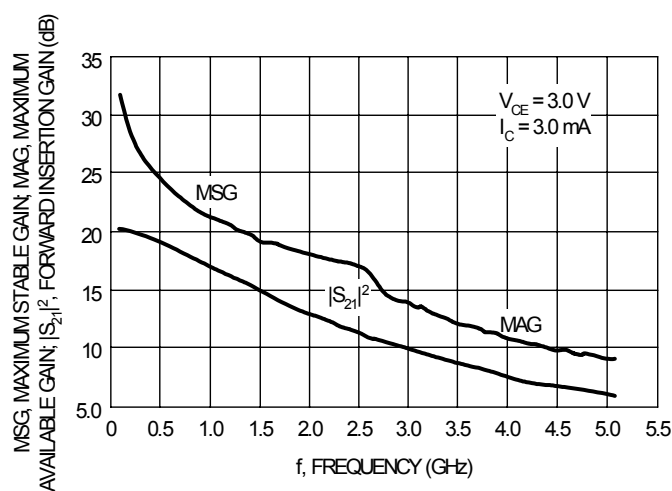


Figure 7. Maximum Stable/Available gain and Forward Insertion Gain versus Frequency

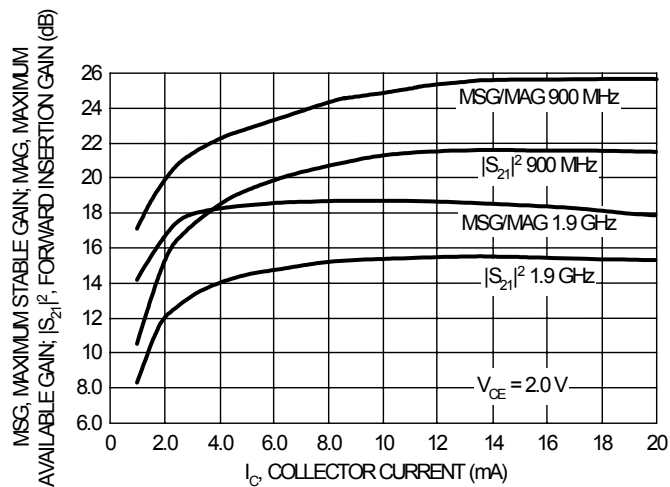


Figure 8. Maximum Stable/Available gain and Forward Insertion Gain versus Collector Current

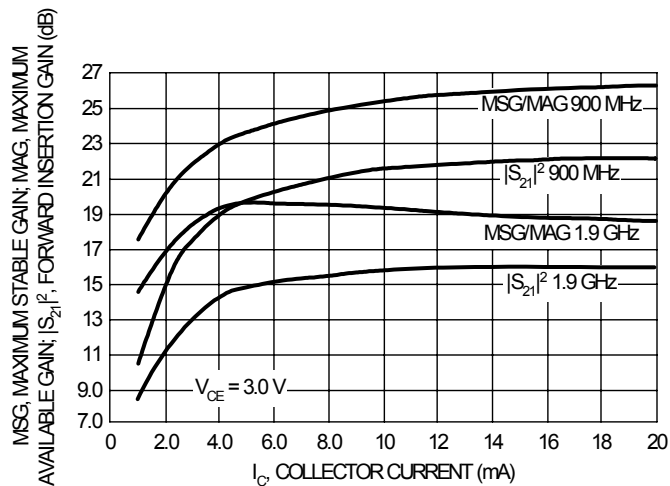


Figure 9. Maximum Stable/Available gain and Forward Insertion Gain versus Collector Current

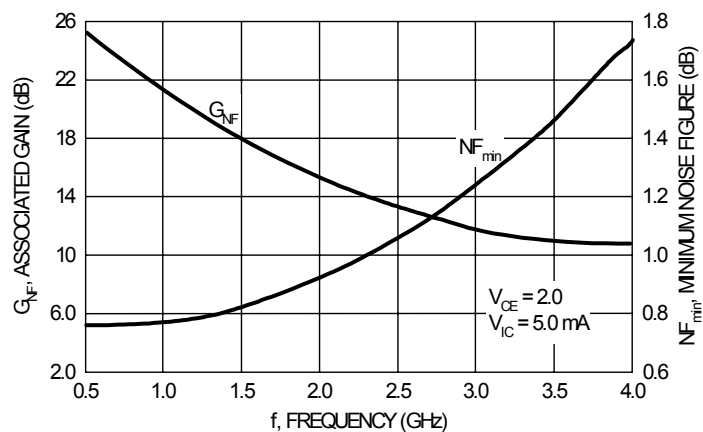


Figure 10. Minimum Noise Figure and Associated Gain versus Frequency

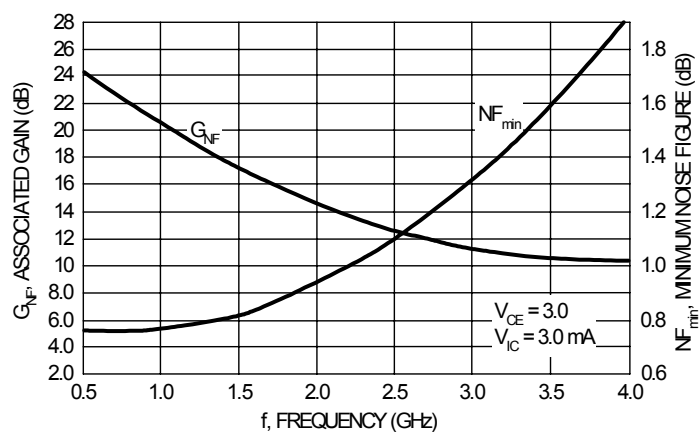


Figure 11. Minimum Noise Figure and Associated Gain versus Frequency

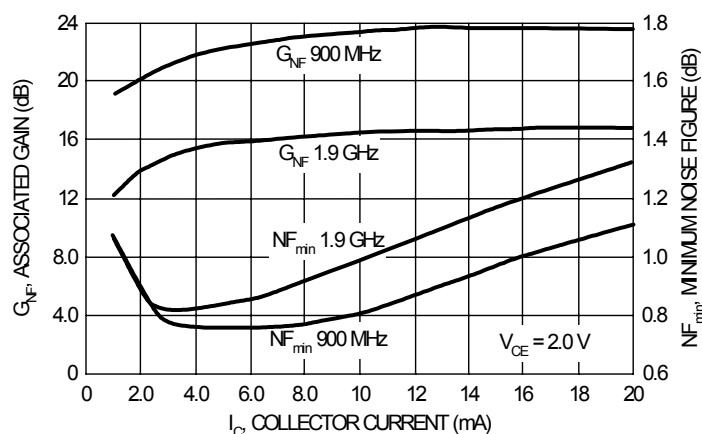


Figure 12. Minimum Noise Figure and Associated Gain versus Collector Current

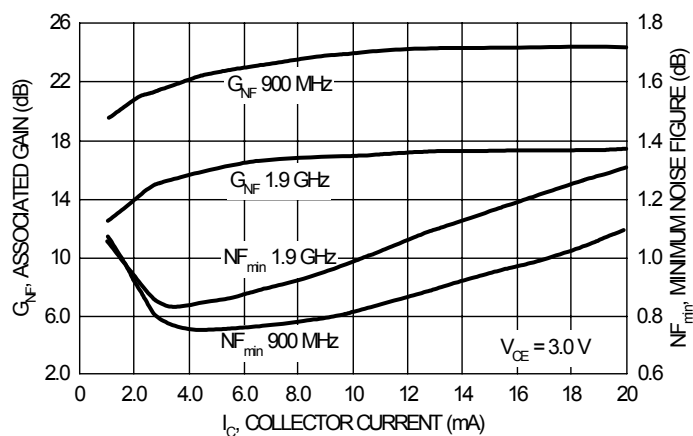


Figure 13. Minimum Noise Figure and Associated Gain versus Collector Current

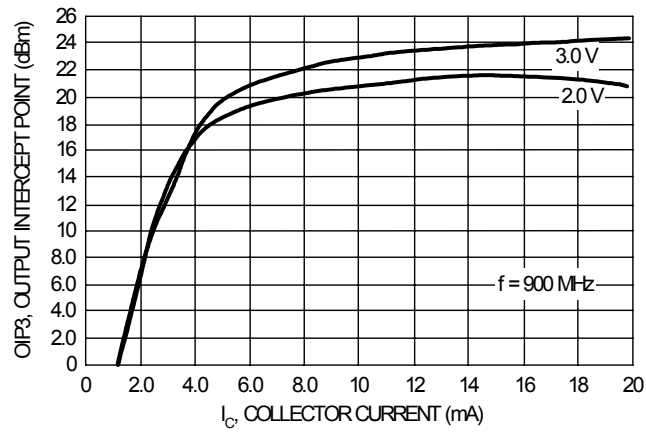


Figure 14. Output Third Order Intercept versus Collector Current

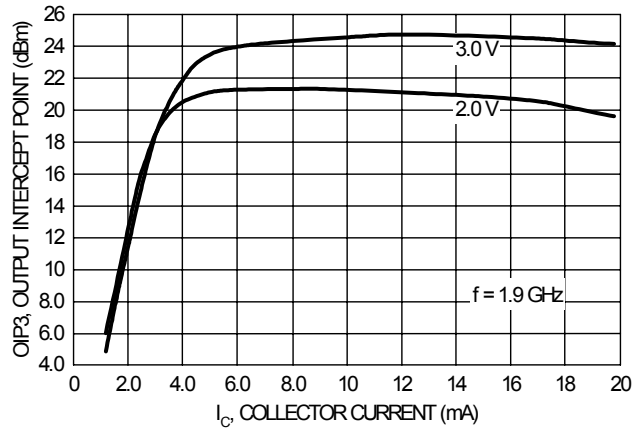


Figure 15. Output Third Order Intercept versus Collector Current

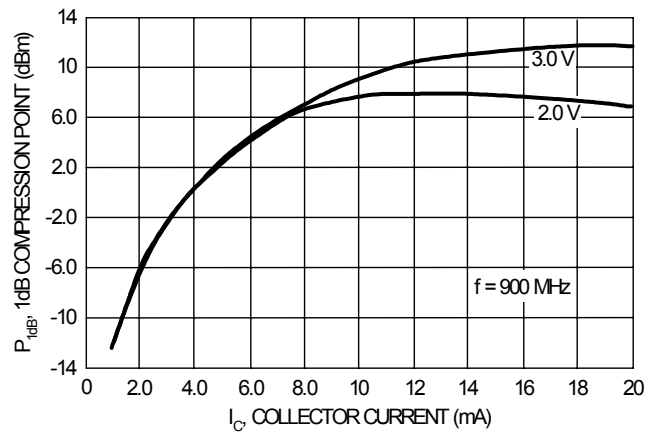


Figure 16. One dB Compression Point versus Collector Current

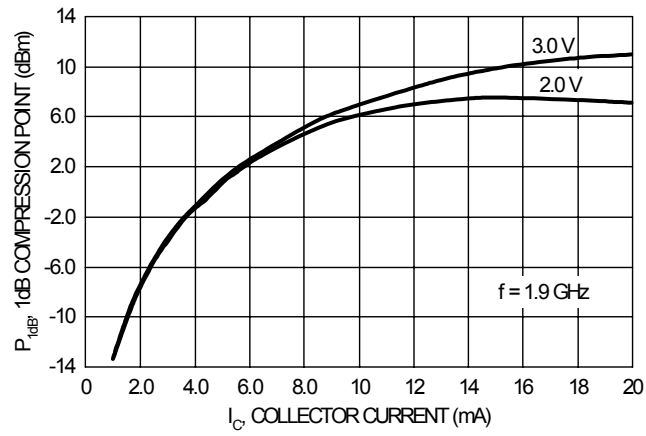


Figure 17. One dB Compression Point versus Collector Current

3 Applications Information

A flexible applications board topology has been developed to demonstrate the performance of the MBC13900 at 900 and 1900 MHz. The designs are a compromise of the competing performance requirements of gain, noise figure, input third-order intercept point (IIP3) and return losses. PCB, samples and assembly information are available from Motorola under part number KITMBC13900/D.

3.1 900 MHz LNA

Figure 18 shows the schematic and Figure 19 shows the component placement for a 900 MHz LNA. The design goals for the circuit are:

NF < 1.2 dB

Gain > 19 dB

Return Loss > 10 dB, input and output

Unconditional stability from 100 MHz to 6 GHz.

Typical performance that can be expected from this circuit at 3.0 and 3.5 V V_{CC} is listed in Table 4. The component values can be changed to enhance the performance of a particular parameter but usually at the expense of another. Gain can be improved by sacrificing stability (R3 and R5). Input return loss can be sacrificed to improve noise figure. IIP3 can be improved by increasing emitter degeneration (L3) and bias current (R2). Unused traces are available on the PCB to add emitter degeneration at leads 1 and 3 of the device.

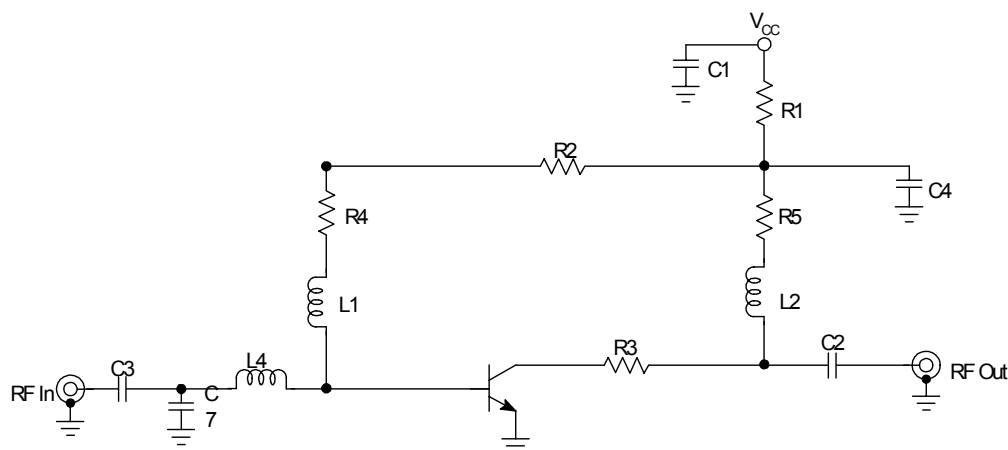


Figure 18. 900 MHz LNA Schematic

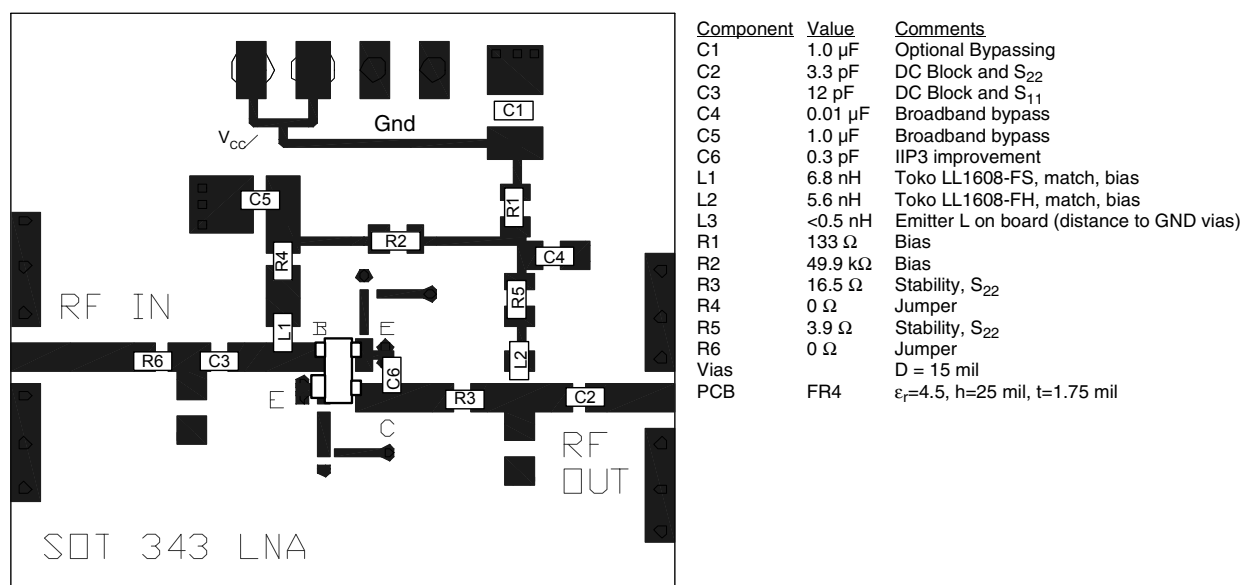


Figure 19. 900 MHz LNA Board Layout

Table 4. Typical 900 MHz LNA Performance

V_{CC}	I_C (mA)	NF (dB)	50 Ω Insertion Gain (dB)	Output IP3 (dBm)	Input Return Loss (dB)	Output Return Loss (dB)
3.0	5.0	1.2	19.7	15	10.1	10.2
3.5	6.1	1.21	20.2	17.6	10.8	10.8

3.2 1900 MHz LNA

Figure 20 shows the schematic and Figure 21 shows the component placement for a 1900 MHz LNA. The design goals for the circuit are:

NF < 1.35 dB

Gain > 14 dB

Return Loss > 10 dB, input and output

Unconditional stability from 100 MHz to 6 GHz.

Typical performance that can be expected from this circuit at 3.0 V V_{CC} and 5.0 mA is listed in Table 5. The component values can be changed to enhance the performance of a particular parameter but usually at the expense of another. Gain can be improved by sacrificing stability (R3 and R5). Input return loss can be sacrificed to improve noise figure. Input return loss can be improved at the expense of noise figure (C3, C7, L4). IIP3 can be improved by increasing emitter degeneration (L3) and bias current (R2). Unused traces are available on the PCB to add emitter degeneration at leads 1 and 3 of the device.

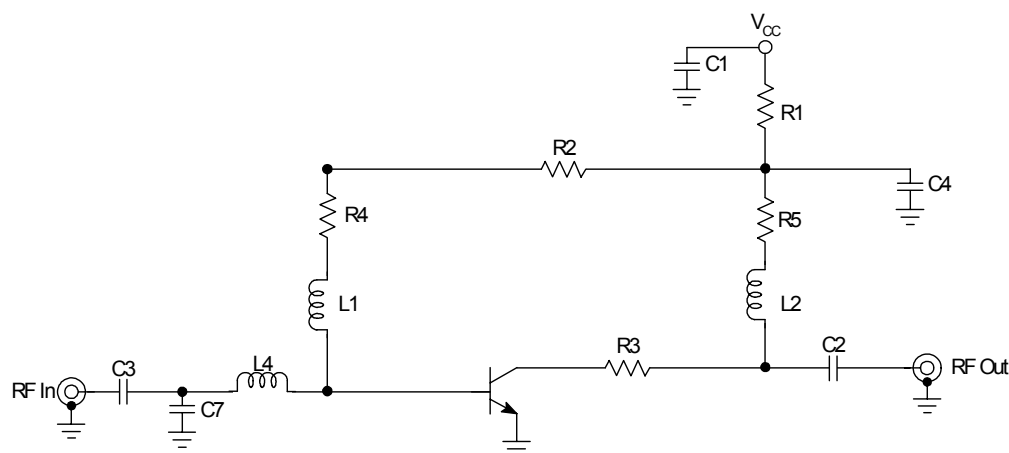
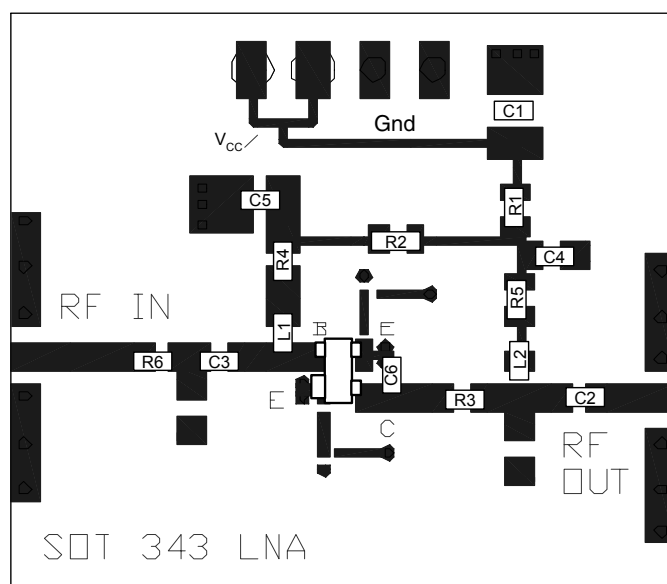


Figure 20. 1900 MHz LNA Schematic



Component	Value	Comments
C1	1.0 μ F	Optional Bypassing
C2	22 pF	DC Block and output match
C3	22 pF	DC Block and input match
C4	0.01 μ F	RF and IM subharmonic short to ground
C5	1.0 μ F	RF and IM subharmonic short to ground
C7	0.6 pF	Input match, RF / S_{11} compromise
L1	8.2 nH	Bias decoupling, input match
L2	3.3 nH	Output match, bias decoupling
L3	<0.5 nH	Emitter L on board (distance to GND vias)
L4	1.2 nH	S_{11}
R1	133 Ω	Bias
R2	49.9 k Ω	Bias
R3	8.2 Ω	Stability and S_{22} improvement
R4	0 Ω	Jumper
R5	4.7 Ω	Stability, Gain, S_{22}
Vias	D = 15 mil	
PCB	FR4	$\epsilon_r=4.5$, h=25 mil, t=1.75 mil

Figure 21. 1900 MHz LNA Board Layout

Table 5. Typical 1900 MHz LNA Performance

V_{CC}	I_C (mA)	NF (dB)	50 Ω Insertion Gain (dB)	Output IP3 (dBm)	Input Return Loss (dB)	Output Return Loss (dB)
3.0	5.0	1.28	14	19	10.4	10.7
3.5	6.1	1.29	14.4	20.2	10.8	11

Table 6. Common Emitter S-Parameters

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
2.0	1.0	0.1	0.973	-6	3.754	175	0.008	86	0.997	-3
		0.5	0.961	-33	3.366	153	0.038	71	0.968	-12
		0.9	0.895	-57	3.341	135	0.065	56	0.910	-22
		1.0	0.868	-63	3.256	131	0.070	53	0.915	-24
		1.5	0.766	-91	2.688	111	0.091	38	0.851	-33
		1.9	0.721	-114	2.610	94	0.100	26	0.788	-39
		2.0	0.706	-119	2.501	91	0.102	23	0.780	-41
		2.4	0.649	-140	2.280	77	0.104	15	0.731	-47
		3.0	0.628	-166	1.984	58	0.105	2	0.667	-56
		3.5	0.606	173	1.717	45	0.099	-3	0.650	-62
		4.0	0.606	155	1.478	33	0.094	-10	0.640	-68
		4.5	0.611	138	1.421	21	0.089	-12	0.604	-74
		5.0	0.610	122	1.309	9	0.085	-11	0.581	-81
	2.0	0.1	0.948	-8	7.181	173	0.008	86	0.993	-4
		0.5	0.907	-41	6.508	146	0.037	67	0.937	-15
		0.9	0.796	-70	5.770	126	0.059	52	0.843	-27
		1.0	0.763	-77	5.533	121	0.062	49	0.842	-29
		1.5	0.638	-107	4.304	101	0.076	36	0.753	-37
		1.9	0.585	-131	3.904	86	0.082	27	0.675	-42
		2.0	0.571	-136	3.716	83	0.083	25	0.667	-44
		2.4	0.532	-156	3.272	70	0.085	20	0.616	-48
		3.0	0.520	179	2.745	53	0.087	13	0.554	-57
		3.5	0.511	159	2.360	41	0.088	10	0.542	-62
		4.0	0.518	143	2.046	30	0.088	7	0.530	-67
		4.5	0.529	128	1.907	19	0.091	5	0.500	-72
		5.0	0.536	114	1.747	8	0.096	5	0.474	-78
	3.0	0.1	0.926	-10	10.121	172	0.008	84	0.990	-4
		0.5	0.853	-48	8.944	141	0.035	65	0.906	-18

Table 6. Common Emitter S-Parameters (Continued)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
		0.9	0.716	-80	7.393	120	0.053	49	0.786	-30
		1.0	0.680	-87	7.000	115	0.056	47	0.780	-31
		1.5	0.556	-118	5.248	95	0.068	36	0.685	-38
		1.9	0.507	-141	4.579	81	0.073	31	0.609	-43
		2.0	0.497	-147	4.359	78	0.074	29	0.601	-44
		2.4	0.472	-166	3.778	66	0.077	25	0.554	-48
		3.0	0.468	170	3.120	51	0.082	21	0.495	-56
		3.5	0.466	152	2.680	39	0.086	18	0.485	-61
		4.0	0.476	137	2.333	28	0.091	15	0.476	-66
		4.5	0.491	123	2.148	18	0.096	12	0.447	-70
		5.0	0.503	109	1.963	8	0.104	11	0.423	-75
	5.0	0.1	0.884	-13	15.377	170	0.007	83	0.982	-6
		0.5	0.753	-59	12.586	134	0.032	61	0.846	-22
		0.9	0.595	-94	9.434	111	0.046	49	0.699	-33
		1.0	0.561	-102	8.786	106	0.048	47	0.689	-34
		1.5	0.457	-134	6.309	88	0.058	39	0.596	-39
		1.9	0.421	-156	5.291	75	0.064	36	0.531	-42
		2.0	0.416	-161	5.033	72	0.065	36	0.525	-43
		2.4	0.408	-178	4.295	62	0.072	34	0.485	-47
		3.0	0.418	160	3.505	48	0.080	30	0.435	-54
		3.5	0.424	143	3.012	37	0.088	26	0.426	-58
		4.0	0.437	129	2.633	27	0.095	23	0.415	-63
		4.5	0.454	116	2.394	17	0.104	19	0.393	-67
		5.0	0.471	104	2.181	7	0.114	15	0.368	-72
	10	0.1	0.785	-19	25.691	165	0.007	78	0.961	-8
		0.5	0.575	-79	17.485	122	0.027	59	0.750	-28
		0.9	0.438	-118	11.534	99	0.037	51	0.595	-35
		1.0	0.421	-126	10.545	95	0.038	51	0.567	-35

Table 6. Common Emitter S-Parameters (Continued)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
		1.5	0.366	-156	7.311	80	0.050	48	0.500	-38
		1.9	0.356	-176	5.901	69	0.058	46	0.454	-39
		2.0	0.354	-180	5.625	67	0.060	46	0.449	-40
		2.4	0.362	166	4.737	57	0.069	44	0.417	-43
		3.0	0.392	148	3.842	45	0.082	38	0.372	-49
		3.5	0.399	134	3.307	35	0.092	34	0.357	-54
		4.0	0.414	120	2.907	25	0.103	29	0.345	-59
		4.5	0.434	109	2.613	16	0.113	25	0.328	-65
		5.0	0.453	98	2.374	6	0.124	18	0.307	-69
	15	0.1	0.708	-25	32.559	161	0.007	83	0.938	-10
		0.5	0.480	-94	19.200	115	0.024	58	0.679	-29
		0.9	0.381	-133	11.991	94	0.033	54	0.538	-34
		1.0	0.371	-141	10.889	90	0.035	54	0.515	-33
		1.5	0.344	-169	7.466	76	0.047	53	0.460	-36
		1.9	0.345	174	5.959	66	0.056	51	0.424	-37
		2.0	0.345	170	5.683	64	0.059	50	0.420	-38
		2.4	0.358	157	4.765	55	0.069	47	0.392	-41
		3.0	0.392	142	3.852	43	0.084	42	0.349	-47
		3.5	0.403	129	3.324	33	0.095	37	0.336	-52
		4.0	0.418	116	2.924	24	0.105	31	0.323	-57
		4.5	0.438	106	2.618	14	0.117	26	0.307	-63
		5.0	0.460	95	2.375	5	0.128	20	0.288	-67
	20	0.1	0.639	-31	37.220	158	0.007	75	0.919	-12
		0.5	0.430	-107	19.608	110	0.022	58	0.629	-30
		0.9	0.365	-146	11.885	91	0.032	58	0.504	-32
		1.0	0.360	-153	10.741	87	0.034	58	0.483	-32
		1.5	0.350	-178	7.337	73	0.047	55	0.438	-34
		1.9	0.357	167	5.815	64	0.056	54	0.408	-35

Table 6. Common Emitter S-Parameters (Continued)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
		2.0	0.357	164	5.555	62	0.060	52	0.403	-36
		2.4	0.371	152	4.641	53	0.069	49	0.378	-39
		3.0	0.408	138	3.746	42	0.084	44	0.338	-45
		3.5	0.419	126	3.239	32	0.096	39	0.323	-51
		4.0	0.435	113	2.849	23	0.109	32	0.312	-56
		4.5	0.453	104	2.545	13	0.119	27	0.295	-61
		5.0	0.475	94	2.306	4	0.131	20	0.276	-66
3.0	1.0	0.1	0.970	-7	3.745	175	0.007	86	0.999	-3
		0.5	0.949	-31	3.341	154	0.034	73	0.989	-12
		0.9	0.892	-55	3.339	136	0.059	59	0.939	-21
		1.0	0.878	-61	3.275	132	0.065	54	0.919	-23
		1.5	0.778	-89	2.724	112	0.084	39	0.869	-31
		1.9	0.730	-111	2.648	96	0.093	28	0.808	-37
		2.0	0.714	-116	2.543	93	0.095	26	0.801	-39
		2.4	0.652	-137	2.326	80	0.098	17	0.755	-44
		3.0	0.634	-164	2.040	61	0.098	5	0.689	-53
		3.5	0.604	175	1.765	48	0.093	-1	0.670	-60
		4.0	0.599	157	1.521	35	0.091	-8	0.660	-66
		4.5	0.604	140	1.466	23	0.084	-10	0.626	-73
		5.0	0.602	124	1.348	12	0.080	-9	0.606	-79
	2.0	0.1	0.951	-8	6.981	173	0.007	88	0.992	-3
		0.5	0.913	-39	6.335	147	0.033	69	0.944	-14
		0.9	0.807	-67	5.710	128	0.054	54	0.859	-25
		1.0	0.774	-74	5.488	123	0.057	51	0.860	-27
		1.5	0.647	-104	4.306	103	0.071	37	0.777	-35
		1.9	0.591	-127	3.935	87	0.077	28	0.704	-40
		2.0	0.576	-132	3.750	85	0.077	26	0.697	-42
		2.4	0.531	-152	3.316	72	0.080	22	0.647	-47

Table 6. Common Emitter S-Parameters (Continued)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
		3.0	0.516	-178	2.790	55	0.082	14	0.584	-55
		3.5	0.505	162	2.402	43	0.081	12	0.574	-60
		4.0	0.508	146	2.078	32	0.083	8	0.563	-65
		4.5	0.521	130	1.943	21	0.084	7	0.535	-70
		5.0	0.526	115	1.782	10	0.089	7	0.511	-76
	3.0	0.1	0.928	-9	10.077	172	0.007	84	0.991	-4
		0.5	0.859	-46	8.948	142	0.032	66	0.917	-17
		0.9	0.725	-77	7.487	121	0.049	51	0.806	-28
		1.0	0.687	-84	7.105	116	0.052	50	0.803	-30
		1.5	0.559	-115	5.356	97	0.063	38	0.711	-37
		1.9	0.505	-138	4.701	82	0.067	31	0.638	-41
		2.0	0.493	-143	4.473	79	0.068	31	0.631	-42
		2.4	0.462	-162	3.886	68	0.072	27	0.585	-47
		3.0	0.458	173	3.218	52	0.077	22	0.529	-54
		3.5	0.452	154	2.763	41	0.082	20	0.518	-59
		4.0	0.460	139	2.403	30	0.085	17	0.509	-64
		4.5	0.476	125	2.216	20	0.090	14	0.483	-69
		5.0	0.486	110	2.025	10	0.098	13	0.460	-74
	5.0	0.1	0.884	-12	15.441	170	0.007	82	0.985	-5
		0.5	0.756	-55	12.831	135	0.029	64	0.882	-22
		0.9	0.598	-90	9.722	112	0.042	50	0.743	-31
		1.0	0.570	-98	9.076	107	0.045	48	0.711	-32
		1.5	0.458	-129	6.576	89	0.054	42	0.629	-38
		1.9	0.415	-152	5.514	76	0.060	38	0.564	-40
		2.0	0.408	-157	5.251	74	0.061	37	0.557	-41
		2.4	0.395	-174	4.489	63	0.067	35	0.517	-45
		3.0	0.407	163	3.680	49	0.076	31	0.464	-51
		3.5	0.407	146	3.158	39	0.083	28	0.450	-56

Table 6. Common Emitter S-Parameters (Continued)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
		4.0	0.417	131	2.768	29	0.090	25	0.438	-61
		4.5	0.434	118	2.517	19	0.098	21	0.419	-67
		5.0	0.450	105	2.294	9	0.108	17	0.398	-72
	10	0.1	0.795	-18	25.574	165	0.007	79	0.970	-7
		0.5	0.587	-74	17.871	123	0.025	60	0.780	-26
		0.9	0.438	-112	11.957	101	0.034	54	0.631	-33
		1.0	0.417	-119	10.950	97	0.036	52	0.602	-33
		1.5	0.351	-150	7.620	81	0.047	50	0.536	-37
		1.9	0.334	-171	6.171	70	0.054	47	0.490	-38
		2.0	0.332	-175	5.878	68	0.056	47	0.485	-39
		2.4	0.336	169	4.960	59	0.065	45	0.454	-42
		3.0	0.363	151	4.029	46	0.076	40	0.408	-48
		3.5	0.371	136	3.465	36	0.087	36	0.393	-53
		4.0	0.385	122	3.048	27	0.097	31	0.383	-58
		4.5	0.405	110	2.743	17	0.107	26	0.368	-63
		5.0	0.425	99	2.493	8	0.117	20	0.348	-68
	15	0.1	0.723	-22	32.706	163	0.006	79	0.949	-9
		0.5	0.487	-88	19.861	116	0.021	60	0.695	-26
		0.9	0.373	-127	12.612	96	0.031	55	0.556	-32
		1.0	0.355	-134	11.492	92	0.033	55	0.555	-32
		1.5	0.317	-164	7.867	77	0.044	53	0.494	-34
		1.9	0.312	177	6.309	67	0.053	52	0.460	-37
		2.0	0.315	173	6.004	65	0.055	51	0.454	-37
		2.4	0.327	159	5.044	56	0.064	48	0.429	-41
		3.0	0.354	142	4.069	44	0.078	43	0.390	-47
		3.5	0.371	128	3.507	35	0.089	38	0.384	-52
		4.0	0.383	116	3.073	25	0.099	33	0.376	-57
		4.5	0.400	105	2.757	16	0.109	27	0.361	-61

Table 6. Common Emitter S-Parameters (Continued)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
	20	5.0	0.427	95	2.500	7	0.120	21	0.341	-65
		0.1	0.660	-27	37.408	160	0.006	79	0.933	-10
		0.5	0.430	-98	20.678	112	0.021	60	0.672	-27
		0.9	0.343	-137	12.691	93	0.030	59	0.548	-31
		1.0	0.335	-144	11.493	89	0.032	59	0.526	-31
		1.5	0.313	-172	7.854	75	0.044	57	0.479	-33
		1.9	0.317	171	6.249	66	0.052	55	0.450	-34
		2.0	0.318	168	5.963	64	0.055	54	0.446	-35
		2.4	0.332	155	4.996	55	0.065	51	0.421	-38
		3.0	0.365	140	4.042	43	0.080	45	0.381	-44
		3.5	0.379	127	3.486	34	0.090	40	0.366	-50
		4.0	0.393	115	3.068	25	0.102	34	0.356	-55
		4.5	0.411	105	2.747	16	0.112	29	0.342	-61
		5.0	0.434	94	2.492	6	0.123	23	0.324	-66

Table 7. Common Emitter Noise Parameters

V_{CE} (V)	I_C (mA)	freq (Ghz)	NFmin (dB)	Gamma Opt		R_n Ω	r_n Ω	G_{NF} (dB)	K
				Mag	Ang				
2.0	5.0	0.5	0.76	0.26	3	9.0	0.18	25.27	0.29
		0.7	0.76	0.25	14	8.5	0.17	23.60	0.37
		0.9	0.77	0.24	25	8.5	0.17	22.03	0.48
		1.0	0.77	0.24	31	8.0	0.16	21.29	0.51
		1.5	0.82	0.23	60	7.0	0.14	17.94	0.74
		1.9	0.90	0.22	85	6.5	0.13	15.73	0.90
		2.0	0.92	0.22	91	6.5	0.13	15.24	0.93
		2.4	1.03	0.22	116	5.5	0.11	13.54	1.03
		3.0	1.24	0.23	155	5.0	0.10	11.75	1.17
		3.5	1.47	0.25	-172	5.0	0.10	10.96	1.23
		4.0	1.74	0.27	137	6.5	0.13	10.81	1.29
3.0	3.0	0.5	0.76	0.38	8	12.0	0.24	24.32	0.22
		0.7	0.76	0.37	17	11.5	0.23	22.70	0.28
		0.9	0.76	0.37	26	11.0	0.22	21.19	0.36
		1.0	0.77	0.36	31	11.0	0.22	20.47	0.38
		1.5	0.82	0.35	56	9.5	0.19	17.24	0.59
		1.9	0.91	0.34	77	8.5	0.17	15.10	0.76
		2.0	0.94	0.34	83	8.0	0.16	14.63	0.79
		2.4	1.06	0.33	105	6.5	0.13	12.98	0.94
		3.0	1.32	0.31	141	5.0	0.10	11.27	1.12
		3.5	1.59	0.30	173	4.5	0.09	10.52	1.24
		4.0	1.92	0.29	-153	6.5	0.13	10.39	1.34

Table 8. SPICE Parameters (MBC13900 Die Parameters)

Name	Value	Name	Value	Name	Value
IS	2.77E-16	IRB	0.006	TF	6.34E-12
BF	181.6	RBM	0.047	XTF	3.051
NF	1.012	RE	4.431	VTF	1.336
VAF	40.66	RC	5.845	ITF	0.202
IKF	0.237	XTB	0.6	PTF	0
ISE	3.79E-14	EG	1.195	TR	1.02E-09
NE	2.00	XTI	0.8	FC	0.95
BR	4.547	CJE	4.52E-13		
NR	1.00	VJE	1.95		
VAR	2.722	MJE	0.58		
IKR	9.98E-04	CJC	1.56E-13		
ISC	3.78E-15	VJC	0.424		
NC	2.00	MJC	0.232		
RB	9.055	XCJC	0.187		

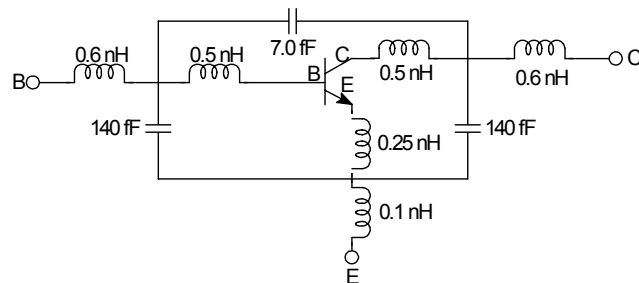
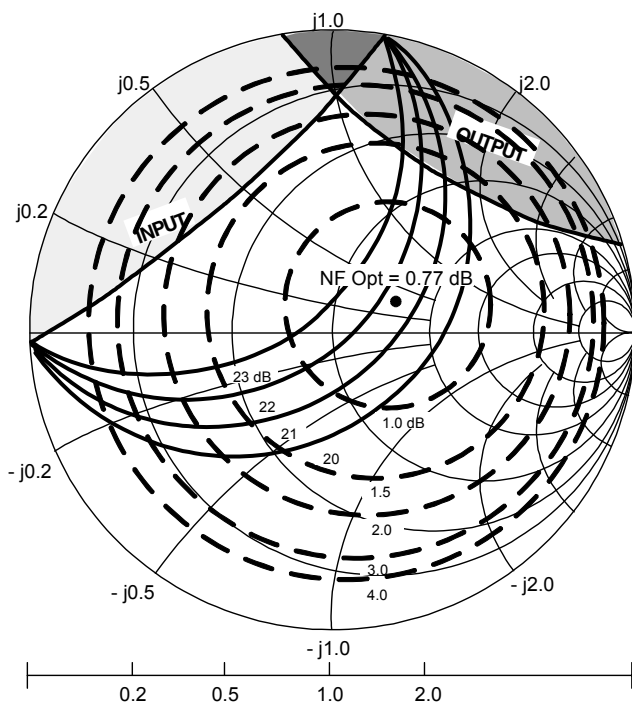


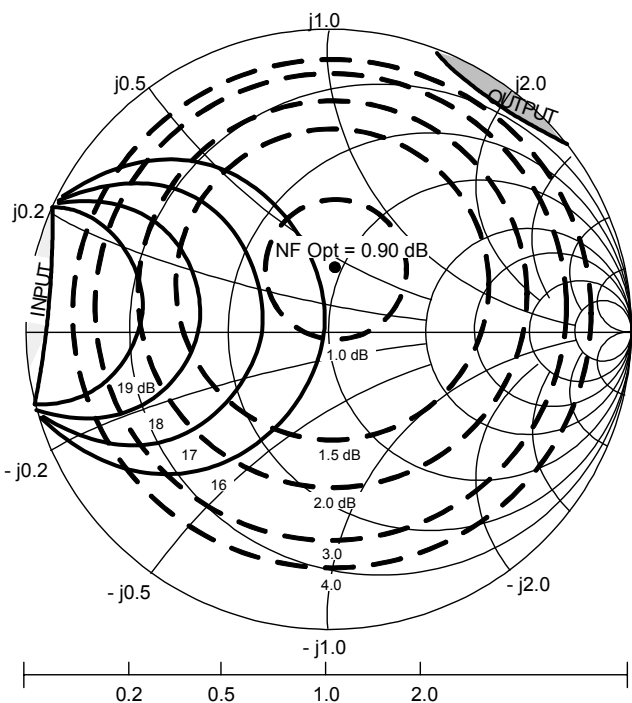
Figure 22. Simplified Package Model



$V_{CE} = 2.0 \text{ V}$
 $I_C = 5.0 \text{ mA}$
 — Potentially Unstable

f (GHz)	NF Opt (dB)	Γ_O	Rn	K
0.9	0.77	$0.24 \angle 25.2^\circ$	8.5	0.48

Figure 23. Constant Gain and Noise Figure Contours
(f = 900 MHz)



$V_{CE} = 2.0 \text{ V}$
 $I_C = 5.0 \text{ mA}$
 — Potentially Unstable

f (GHz)	NF Opt (dB)	Γ_O	Rn	K
1.9	0.9	$0.22 \angle 84.5^\circ$	6.5	0.90

Figure 24. Constant Gain and Noise Figure Contours
(f = 1.9 GHz)

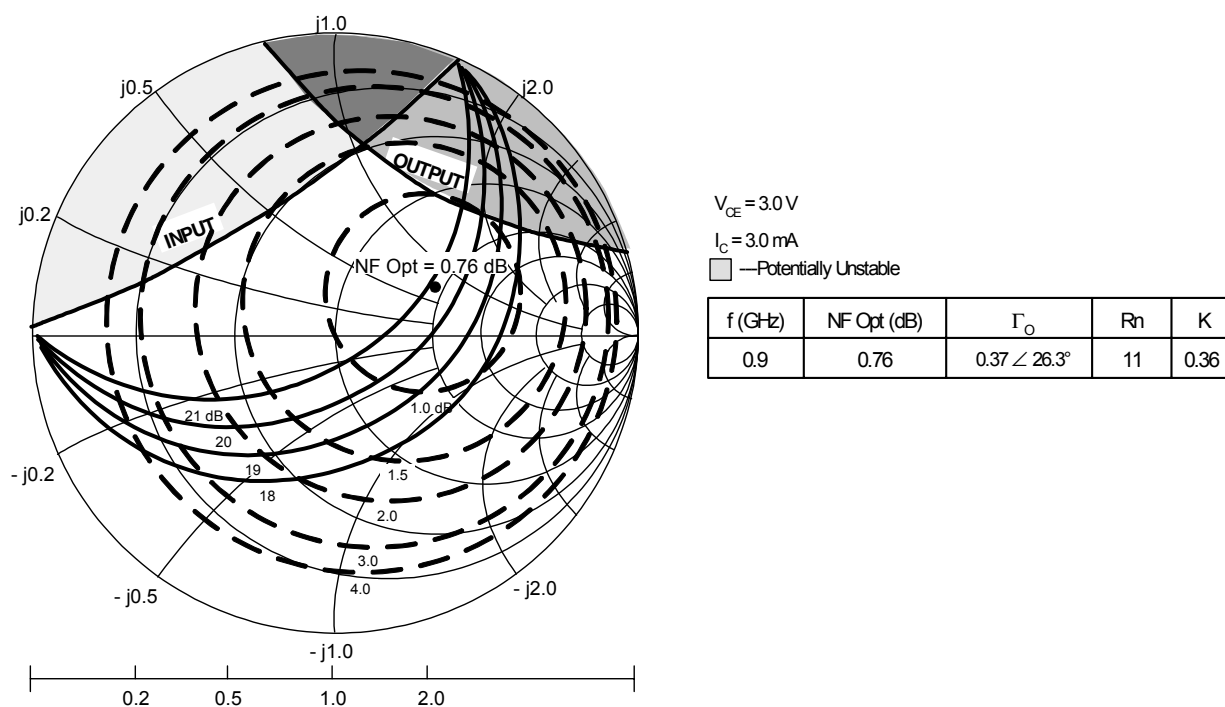


Figure 25. Constant Gain and Noise Figure Contours
(f = 900 MHz)

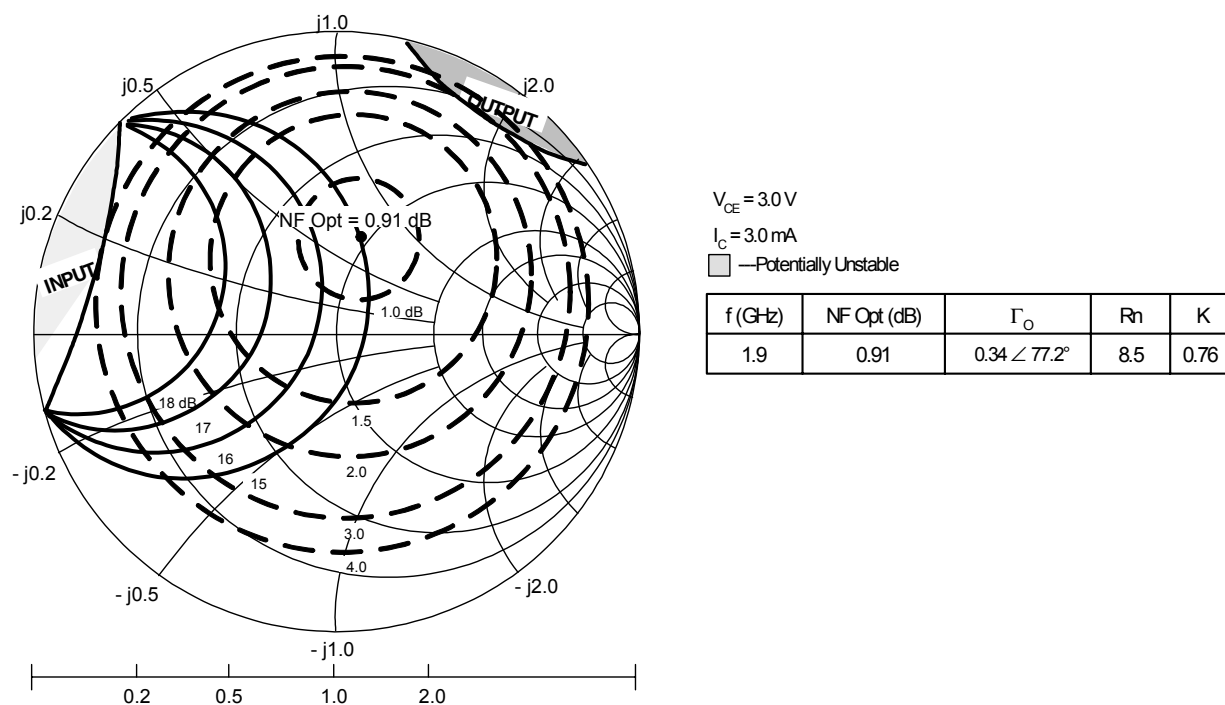


Figure 26. Constant Gain and Noise Figure Contours
(f = 1.9 GHz)

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for digital and analog cellular PCN and PCS base station applications with frequencies from 1000 to 2500 MHz. Characterized for operation Class A and Class AB at 26 volts in commercial and industrial applications.

- Specified Two-Tone Performance @ 1930 and 2000 MHz, 26 Volts
 - Output Power — 4 Watts PEP
 - Power Gain — 11 dB
 - Efficiency — 30%
 - Intermodulation Distortion — -29 dBc
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 4 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- S-Parameter Characterization at High Bias Levels
- Available in Tape and Reel. R1 Suffix = 500 Units per 12 mm, 7 inch Reel.

MRF281SR1

MRF281ZR1

2000 MHz, 4 W, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 458B-03, STYLE 1
(NI-200S)
(MRF281SR1)



CASE 458C-03, STYLE 1
(NI-200Z)
(MRF281ZR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	20 0.115	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.74	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

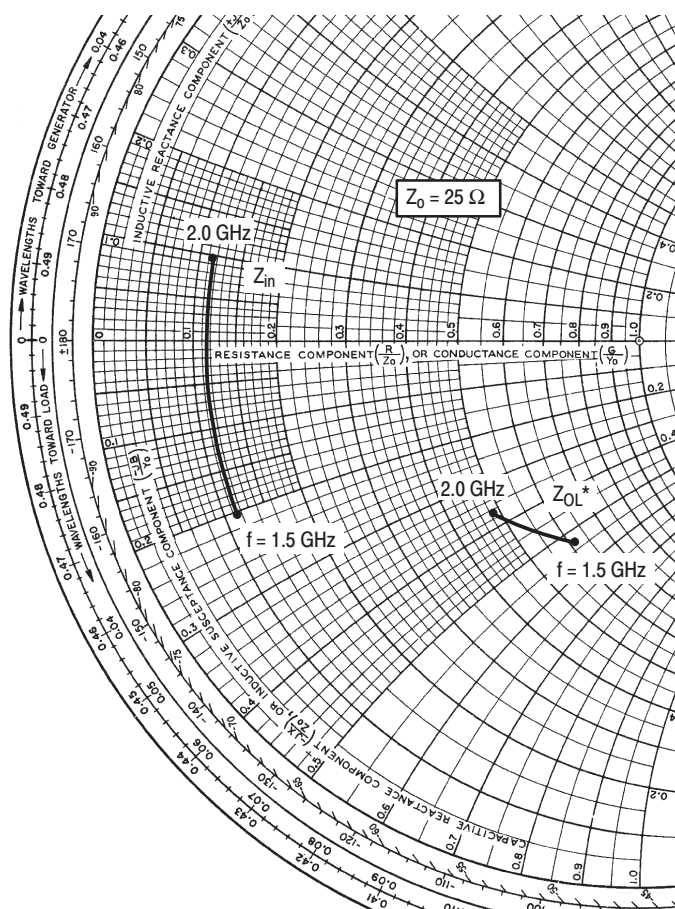
OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 10 \mu\text{Adc}$)	$V_{(BR)DSS}$	65	74	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28 \text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}	—	—	10	μAdc
Gate-Source Leakage Current ($V_{GS} = 20 \text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	—	1	μAdc

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 20\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	2.4	3.2	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 25\text{ mAdc}$)	$V_{GS(q)}$	3	4.1	5	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 0.1\text{ A}$)	$V_{DS(on)}$	0.18	0.24	0.30	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{iss}	—	5.5	—	pF
Output Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{oss}	—	3.3	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{rss}	—	0.17	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W PEP}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	G_{ps}	11	12.5	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W PEP}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	η	30	33	—	%
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W PEP}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	IRL	—	–16	–10	dB
Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W PEP}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	IMD	—	–31	–29	dBc
Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W PEP}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	G_{ps}	11	12.5	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	η	30	—	—	%
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W PEP}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	IRL	—	–16	–10	dB
Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W PEP}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	IMD	—	–31	—	dBc
Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W CW}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 2000.0\text{ MHz}$)	G_{ps}	10.5	12	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W CW}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 2000.0\text{ MHz}$)	η	40	44	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 4\text{ W CW}$, $I_{DQ} = 25\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $V_{SWR} = 10:1$, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power			



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 25 \text{ mA}$, $P_{out} = 4 \text{ W (PEP)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1500	$3.15 - j5.3$	$15.5 - j13.6$
1600	$3.1 - j3.8$	$14.7 - j12.5$
1700	$3.1 - j2.3$	$14.0 - j11.7$
1800	$3.1 - j0.7$	$13.4 - j11.0$
1900	$3.1 + j0.9$	$12.8 - j10.1$
2000	$3.1 + j2.4$	$12.2 - j9.2$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at given output power, voltage, IMD, bias current and frequency.

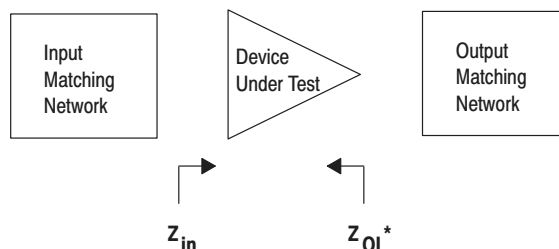


Figure 1. Series Equivalent Input and Output Impedance

Freescale Semiconductor, Inc.

Table 1. Common Source S-Parameters at $V_{DS} = 26$ Vdc, $I_D = 250$ mAdc

f GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	dB	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
0.1	.982	-28	18.9	160	.008	73	.851	-13
0.2	.947	-52	17.0	143	.015	58	.811	-25
0.3	.912	-73	15.0	129	.019	45	.770	-33
0.4	.886	-90	12.9	117	.022	36	.741	-42
0.5	.859	-103	11.1	108	.022	28	.719	-47
0.6	.854	-114	9.69	100	.023	23	.718	-51
0.7	.841	-123	8.54	93	.022	18	.709	-56
0.8	.837	-131	7.57	87	.021	15	.714	-59
0.9	.838	-138	6.69	81	.019	12	.719	-62
1.0	.841	-143	6.01	76	.018	11	.728	-64
1.1	.840	-149	5.41	72	.015	12	.742	-66
1.2	.849	-153	4.91	68	.013	13	.745	-68
1.3	.848	-158	4.51	64	.012	18	.758	-69
1.4	.856	-162	4.12	60	.010	26	.769	-70
1.5	.858	-167	3.78	57	.009	36	.786	-70
1.6	.871	-170	3.50	54	.008	54	.797	-72
1.7	.868	-173	3.22	51	.009	69	.808	-71
1.8	.870	-176	3.00	49	.009	82	.823	-72
1.9	.872	-180	2.80	46	.011	95	.828	-72
2.0	.877	178	2.63	44	.013	104	.845	-72
2.1	.876	174	2.47	41	.015	109	.843	-72
2.2	.880	171	2.36	39	.018	111	.859	-71
2.3	.882	168	2.21	36	.021	114	.858	-72
2.4	.886	165	2.12	34	.024	114	.872	-70
2.5	.896	162	1.97	32	.027	115	.863	-70
2.6	.897	158	1.89	29	.029	117	.873	-69

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for Class A and Class AB PCN and PCS base station applications with frequencies up to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications.

- Specified Two-Tone Performance @ 2000 MHz, 26 Volts
 - Output Power — 10 Watts PEP
 - Power Gain — 10.5 dB
 - Efficiency — 28%
 - Intermodulation Distortion — -31 dBc
- Specified Single-Tone Performance @ 2000 MHz, 26 Volts
 - Output Power — 10 Watts CW
 - Power Gain — 9.5 dB
 - Efficiency — 35%
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 10 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R1 Suffix = 500 Units per 12 mm, 7 inch Reel.

MRF282SR1
MRF282ZR1

2000 MHz, 10 W, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 458B-03, STYLE 1
(NI-200S)
(MRF282SR1)



CASE 458C-03, STYLE 1
(NI-200Z)
(MRF282ZR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	60 0.34	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.2	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 10 \mu\text{Adc}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28 \text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}	—	—	1.0	μAdc
Gate-Source Leakage Current ($V_{GS} = 20 \text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	—	1.0	μAdc

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 50 μAdc)	V _{GS(th)}	2.0	3.0	4.0	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 0.5 Adc)	V _{DS(on)}	—	0.4	0.6	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 75 mAdc)	V _{GS(q)}	3.0	4.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{iss}	—	15	—	pF
Output Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{oss}	—	8.0	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{rss}	—	0.45	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Power Gain (V _{DD} = 26 Vdc, P _{out} = 10 W PEP, I _{DQ} = 75 mA, f ₁ = 2000.0 MHz, f ₂ = 2000.1 MHz)	G _{ps}	10.5	11.5	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 10 W PEP, I _{DQ} = 75 mA, f ₁ = 2000.0 MHz, f ₂ = 2000.1 MHz)	η	28	—	—	%
Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 10 W PEP, I _{DQ} = 75 mA, f ₁ = 2000.0 MHz, f ₂ = 2000.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 10 W PEP, I _{DQ} = 75 mA, f ₁ = 2000.0 MHz, f ₂ = 2000.1 MHz)	IRL	—	–14	–9	dB
Common–Source Power Gain (V _{DD} = 26 Vdc, P _{out} = 10 W PEP, I _{DQ} = 75 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz)	G _{ps}	10.5	11.5	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 10 W PEP, I _{DQ} = 75 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz)	η	28	—	—	%
Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 10 W PEP, I _{DQ} = 75 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 10 W PEP, I _{DQ} = 75 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz)	IRL	—	–14	–9	dB
Common–Source Power Gain (V _{DD} = 26 Vdc, P _{out} = 10 W CW, I _{DQ} = 75 mA, f = 2000.0 MHz)	G _{ps}	9.5	11.5	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 10 W CW, I _{DQ} = 75 mA, f = 2000.0 MHz)	η	35	40	—	%
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 10 W CW, I _{DQ} = 75 mA, f ₁ = 2000.0 MHz, f ₂ = 2000.1 MHz, Load VSWR = 10:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power			

Freescale Semiconductor, Inc.

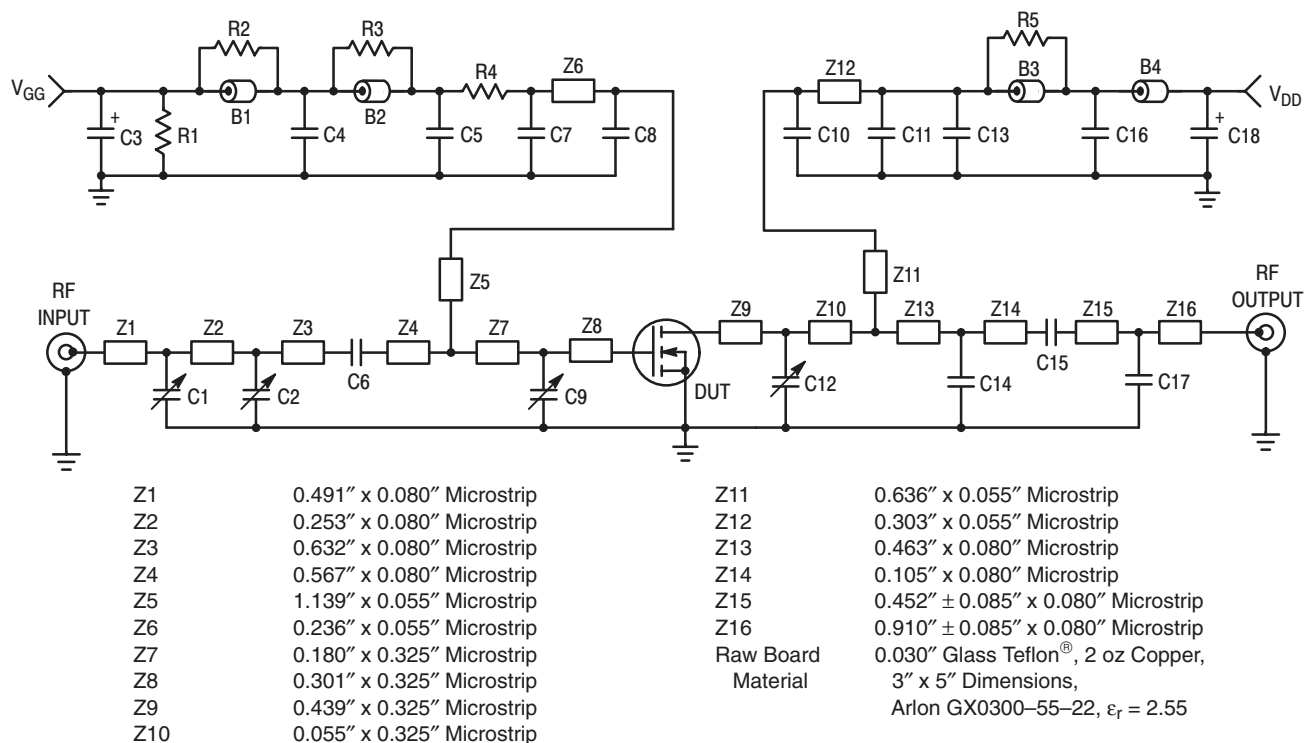


Figure 1. 1.93 – 2.0 GHz Broadband Test Circuit Schematic

Table 1. 1.93 – 2.0 GHz Broadband Test Circuit Component Designations and Values

Designators	Description
B1, B4	Surface Mount Ferrite Beads, 0.120" x 0.333" x 0.100", Fair Rite #2743019446
B2, B3	Surface Mount Ferrite Beads, 0.120" x 0.170" x 0.100", Fair Rite #2743029446
C1, C2, C9	0.8–8.0 pF Variable Capacitors, Johanson Gigatrim #27291SL
C3	10 μ F, 35 V Tantalum Surface Mount Chip Capacitor, Kemet #T495X106K035AS4394
C4, C5, C13, C16	0.1 μ F Chip Capacitors, Kemet #CDR33BX104AKWS
C6	200 pF Chip Capacitor, B Case, ATC #100B201JCA500X
C7	18 pF Chip Capacitor, B Case, ATC #100B180KP500X
C8	39 pF Chip Capacitor, B Case, ATC #100B390JCA500X
C10	27 pF Chip Capacitor, B Case, ATC #100B270JCA500X
C11	1.2 pF Chip Capacitor, B Case, ATC #100B1R2CCA500X
C12	0.6–4.5 pF Variable Capacitor, Johanson Gigatrim #27271SL
C14	0.5 pF Chip Capacitor, B Case, ATC #100B0R5BCA500X
C15	15 pF Chip Capacitor, B Case, ATC #100B150JCA500X
C17	0.1 pF Chip Capacitor, B Case, ATC #100B0R1BCA500X
C18	22 μ F, 35 V Tantalum Surface Mount Chip Capacitor, Kemet #T491X226K035AS4394
R1	560 k Ω , 1/4 W Chip Resistor, 0.08" x 0.13"
R2, R5	12 Ω , 1/4 W Chip Resistors, 0.08" x 0.13", Garrett Instruments #RM73B2B120JT
R3, R4	91 Ω , 1/4 W Chip Resistors, 0.08" x 0.13", Garrett Instruments #RM73B2B910JT
WS1, WS2	Beryllium Copper Wear Blocks 0.010" x 0.235" x 0.135" NOM
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type "N" Jack Connectors, Omni-Spectra # 3052–1648–10
	4–40 Ph Head Screws, 0.125" Long
	4–40 Ph Head Screws, 0.188" Long
	4–40 Ph Head Screws, 0.312" Long
	4–40 Ph Rec. Hd. Screws, 0.438" Long
RF Circuit Board	3" x 5" Copper Clad PCB, Glass Teflon®

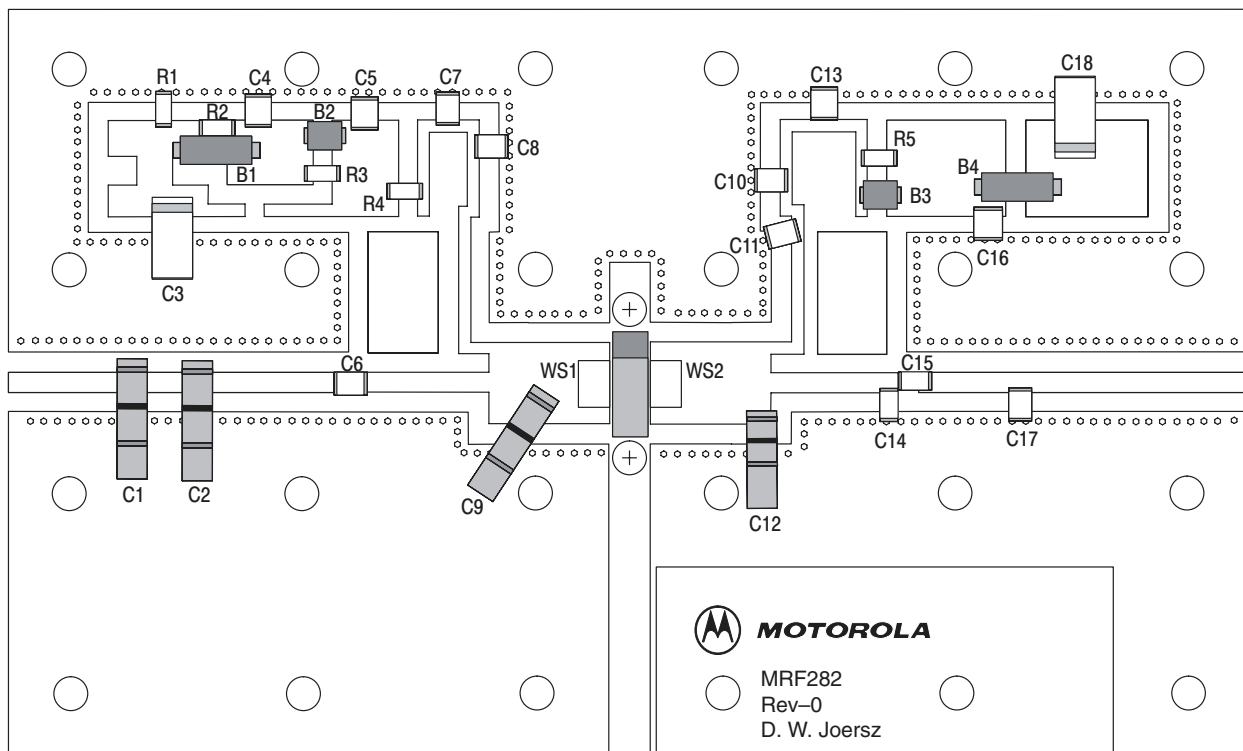
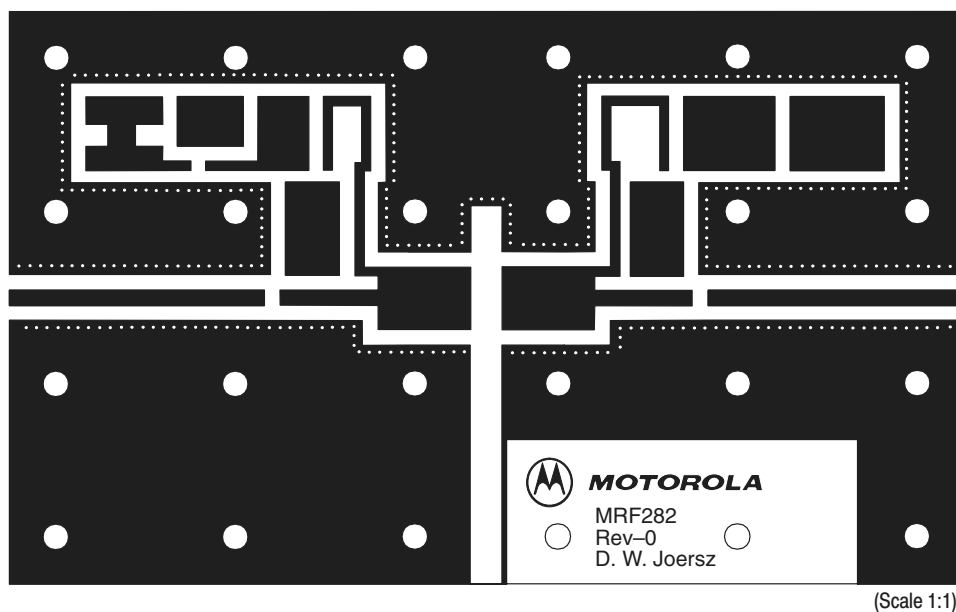


Figure 2. 1.93–2.0 GHz Broadband Test Circuit Component Layout



(Scale 1:1)

**Figure 3. MRF282 Test Circuit Photomaster
(Reduced 18% in printed data book, DL110/D)**

Freescale Semiconductor, Inc.

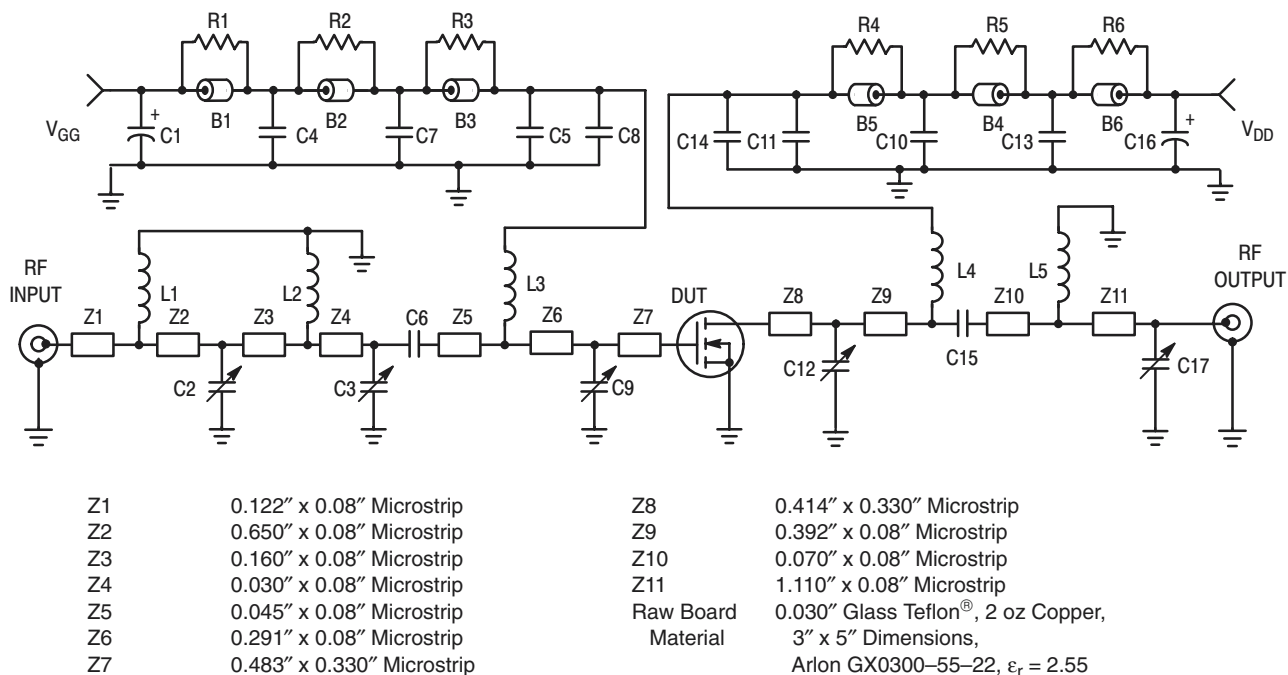


Figure 4. 1.81 – 1.88 GHz Broadband Test Circuit Schematic

Table 2. 1.81 – 1.88 GHz Broadband Test Circuit Component Designations and Values

Designators	Description
B1, B2, B3, B4, B5, B6	Surface Mount Ferrite Beads, 0.120" x 0.170" x 0.100", Fair Rite #2743029446
C1, C16	470 μ F, 63 V Electrolytic Capacitors, Mallory #SME63UB471M12X25L
C2, C9, C12, C17	0.6–4.5 pF Variable Capacitors, Johanson Gigatrim #27271SL
C3	0.8–8.0 pF Variable Capacitor, Johanson Gigatrim #27291SL
C4, C13	0.1 μ F Chip Capacitors, Kemet #CDR33BX104AKWS
C5, C14	100 pF Chip Capacitors, B Case, ATC #100B101JCA500X
C6, C8, C11, C15	12 pF Chip Capacitors, B Case, ATC #100B120JCA500X
C7, C10	1000 pF Chip Capacitors, B Case, ATC #100B102JCA50X
L1	3 Turns, 27 AWG, 0.087" OD, 0.050" ID, 0.053" Long, 6.0 nH
L2	5 Turns, 27 AWG, 0.087" OD, 0.050" ID, 0.091" Long, 15 nH
L3, L4	9 Turns, 26 AWG, 0.080" OD, 0.046" ID, 0.170" Long, 30.8 nH
L5	4 Turns, 27 AWG, 0.087" OD, 0.050" ID, 0.078" Long, 10 nH
R1, R2, R3	12 Ω , 1/8 W Fixed Film Chip Resistors, Garrett Instruments #RM73B2B120JT
R4, R5, R6	0.08" x 0.13" Resistors, Garrett Instruments #RM73B2B120JT
W1, W2	Beryllium Copper 0.010" x 0.110" x 0.210"

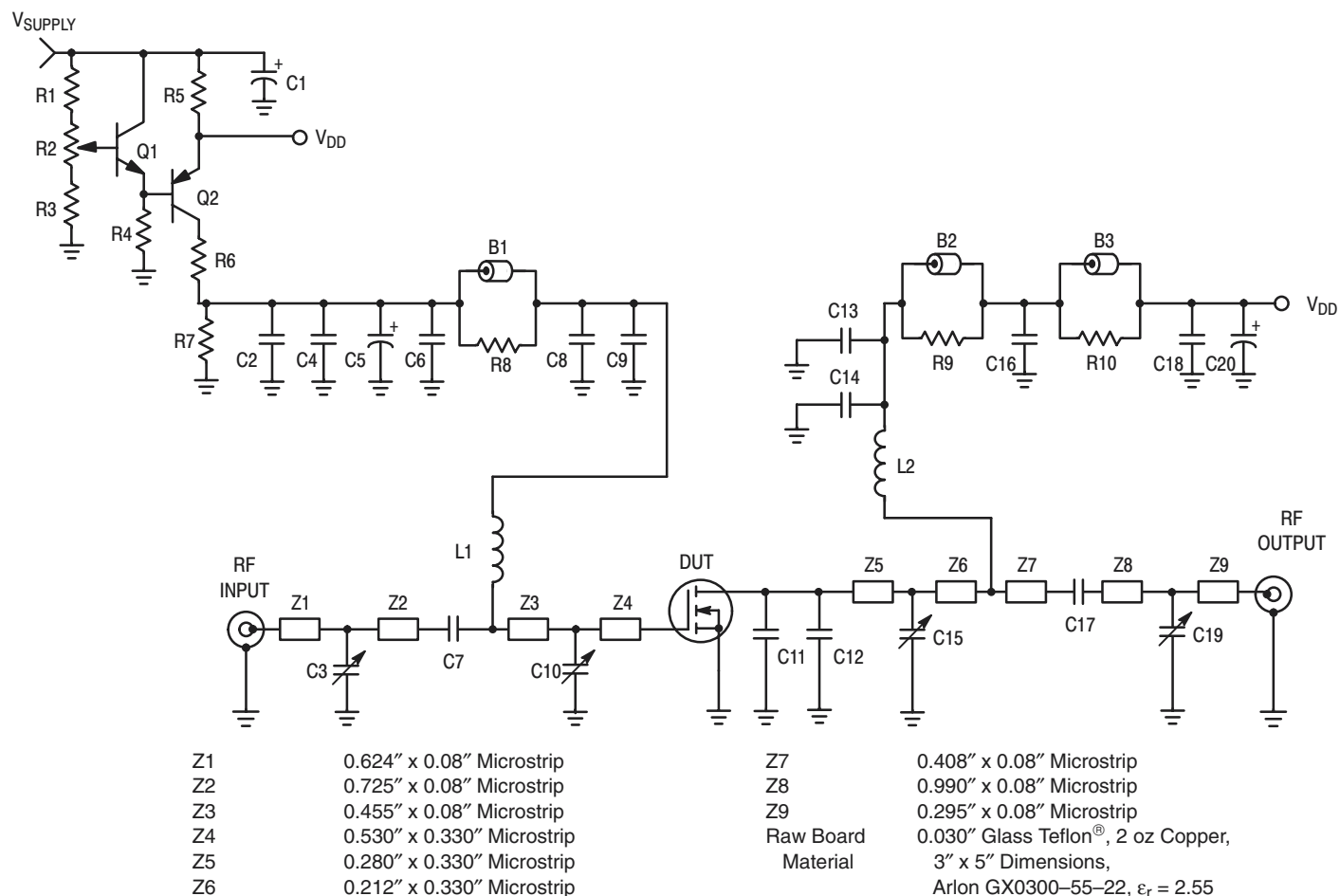
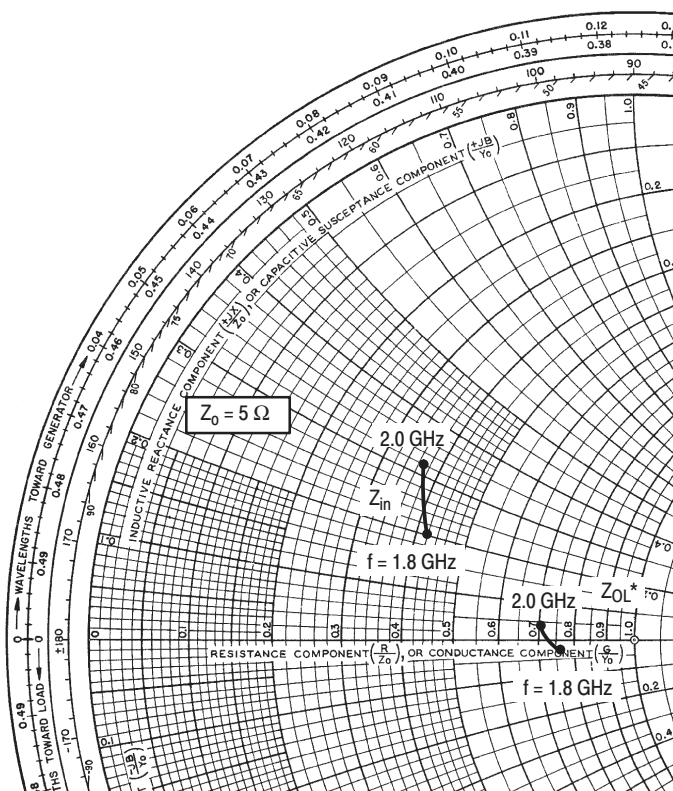


Figure 5. Class A Broadband Test Circuit Schematic

Table 3. Class A Broadband Test Circuit Component Designations and Values

Designators	Description
B1, B2, B3	Ferrite Beads, Ferroxcube #56-590-65-3B
C1, C20	470 μ F, 63 V Electrolytic Capacitors, Mallory #SME63V471M12X25L
C2	0.01 μ F Chip Capacitor, B Case, ATC #100B103JCA50X
C3, C10, C15	0.6-4.5 pF Variable Capacitors, Johanson #27271SL
C4, C16	0.02 μ F Chip Capacitors, B Case, ATC #100B203JCA50X
C5	100 μ F, 50 V Electrolytic Capacitor, Mallory #SME50VB101M12X256
C6, C7, C9, C14, C17	12 pF Chip Capacitors, B Case, ATC #100B120JCA500X
C8, C13	51 pF Chip Capacitors, B Case, ATC #100B510JCA500X
C11, C12	0.3 pF Chip Capacitors, B Case, ATC #100B0R3CCA500X
C18	0.1 μ F Chip Capacitor, Kemet #CDR33BX104AKWS
C19	0.4-2.5 pF Variable Capacitor, Johanson #27285
L1	8 Turns, 0.042" ID, 24 AWG, Enamel
L2	9 Turns, 0.046" ID, 26 AWG, Enamel
Q1	NPN, 15 W, Bipolar Transistor, MJD310
Q2	PNP, 15 W, Bipolar Transistor, MJD320
R1	200 Ω , 1/4 W Axial Resistor
R2	1.0 k Ω , 1/2 W Potentiometer, Bourns
R3	13 k Ω , 1/4 W Axial Resistor
R4, R6, R7	390 Ω , 1/8 W Chip Resistors, Garrett Instruments #RM73B2B391JT
R5	1.0 Ω , 10 W 1% Resistor, Dale #RE65G1R00
R8, R9, R10	12 Ω , 1/8 W Chip Resistors, Garrett Instruments #RM73B2B120JT
Input/Output	Type N Flange Mount RF55-22 Connectors, Omni-Spectra



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 75 \text{ mA}$, $P_{out} = 10 \text{ W (PEP)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1800	$2.1 + j1.0$	$3.8 - j0.15$
1860	$2.05 + j1.15$	$3.77 - j0.13$
1900	$2.0 + j1.2$	$3.75 - j0.1$
1960	$1.9 + j1.4$	$3.65 + j0.1$
2000	$1.85 + j1.6$	$3.55 + j0.2$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at given output power, voltage, IMD, bias current and frequency.

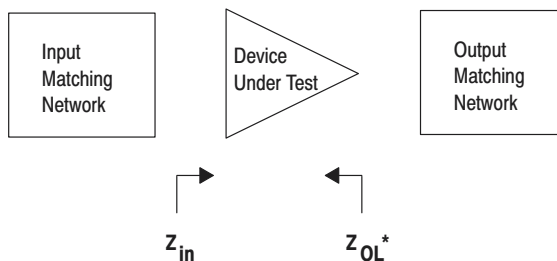


Figure 6. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

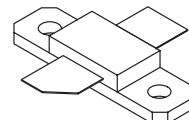
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1000 to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications. To be used in Class A and Class AB for PCN-PCS/cellular radio and wireless local loop.

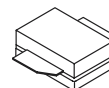
- Specified Two-Tone Performance @ 2000 MHz, 26 Volts
 - Output Power = 30 Watts PEP
 - Power Gain = 9 dB
 - Efficiency = 30%
 - Intermodulation Distortion = -29 dBc
- Typical Single-Tone Performance at 2000 MHz, 26 Volts
 - Output Power = 30 Watts CW
 - Power Gain = 9.5 dB
 - Efficiency = 45%
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

MRF284R1
MRF284LSR1

2000 MHz, 30 W, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B-05, STYLE 1
NI-360
MRF284R1



CASE 360C-05, STYLE 1
NI-360S
MRF284LSR1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	87.5 0.5	Watts $W/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 10 \mu\text{A}$)	$V_{(BR)DS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 20 \text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}	—	—	1.0	μA
Gate-Source Leakage Current ($V_{GS} = 20 \text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	—	10	μA

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 150\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 200\text{ mAdc}$)	$V_{GS(q)}$	3.0	4.0	5.0	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.0\text{ Adc}$)	$V_{DS(on)}$	—	0.3	0.6	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 1.0\text{ Adc}$)	g_{fs}	—	1.5	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{iss}	—	43	—	pF
Output Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{oss}	—	23	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{rss}	—	1.4	—	pF
FUNCTIONAL TESTS (in Motorola Test Fixture, 50 ohm system)					
Common–Source Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	G_{ps}	9	10.5	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	η	30	35	—	%
Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	IMD	—	–32	–29	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $f_2 = 2000.1\text{ MHz}$)	IRL	—	–15	–9	dB
Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	G_{ps}	9	10.4	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	η	—	35	—	%
Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	IMD	—	–34	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$)	IRL	—	–15	–9	dB
Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 2000.0\text{ MHz}$)	G_{ps}	8.5	9.5	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 2000.0\text{ MHz}$)	η	35	45	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 200\text{ mA}$, $f_1 = 2000.0\text{ MHz}$, $V_{SWR} = 10:1$, at All Phase Angles)	Ψ	No Degradation In Output Power			

Freescale Semiconductor, Inc.

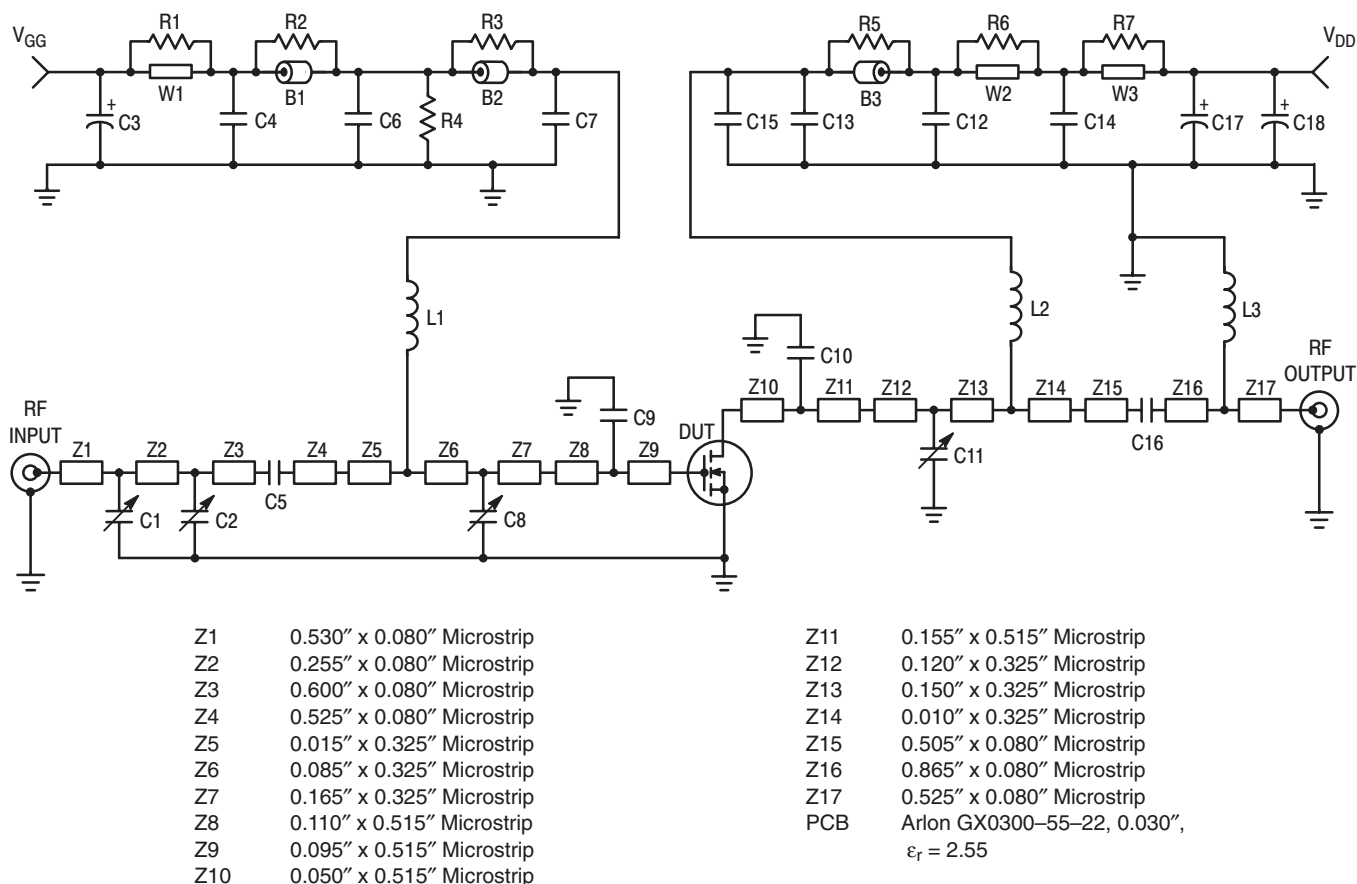


Figure 1. 1.93–2.0 GHz Broadband Test Circuit Schematic

Table 1. 1.93 – 2.0 GHz Broadband Test Circuit Component Designations and Values

Designators	Description
B1 – B3	Ferrite Beads, Round, Ferroxcube #56–590–65–3B
C1, C2, C8	0.8–8.0 pF Gigatrim Variable Capacitors, Johanson #27291SL
C3, C17	22 μ F, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T491X226K035AS4394
C4, C14	0.1 μ F Chip Capacitors, Kemet #CDR33BX104AKWS
C5	220 pF Chip Capacitor, B Case, ATC #100B221KP500X
C6, C12	1000 pF Chip Capacitors, B Case, ATC #100B102JCA50X
C7, C13	5.1 pF Chip Capacitors, B Case, ATC #100B5R1CCA500X
C9	1.2 pF Chip Capacitor, B Case, ATC #100B1R2CCA500X
C10	2.7 pF Chip Capacitor, B Case, ATC #100B2R7CCA500X
C11	0.6–4.5 pF Gigatrim Variable Capacitors, Johanson #27271SL
C15, C16	200 pF Chip Capacitors, B Case, ATC #100B201KP500X
C18	10 μ F, 35 V Tantalum Surface Mount Chip Capacitor, Kemet #T495X106K035AS4394
L1, L2	4 Turns, #24 AWG, 0.120" OD, 0.140" Long, (12.5 nH), Coilcraft #A04T–5
L3	2 Turns, #24 AWG, 0.120" OD, 0.140" Long, (5.0 nH), Coilcraft #A02T–5
R1, R2, R3, R5, R6, R7	12 Ω , 1/4 W Chip Resistors, 0.08" x 0.13", Garrett Instruments #RM73B2B120JT
R4	560 k Ω , 1/4 W Chip Resistor, 0.08" x 0.13"
W1, W2, W3	Solid Copper Buss Wire, 16 AWG
WS1, WS2	Beryllium Copper Wear Blocks 0.005" x 0.250" x 0.250"

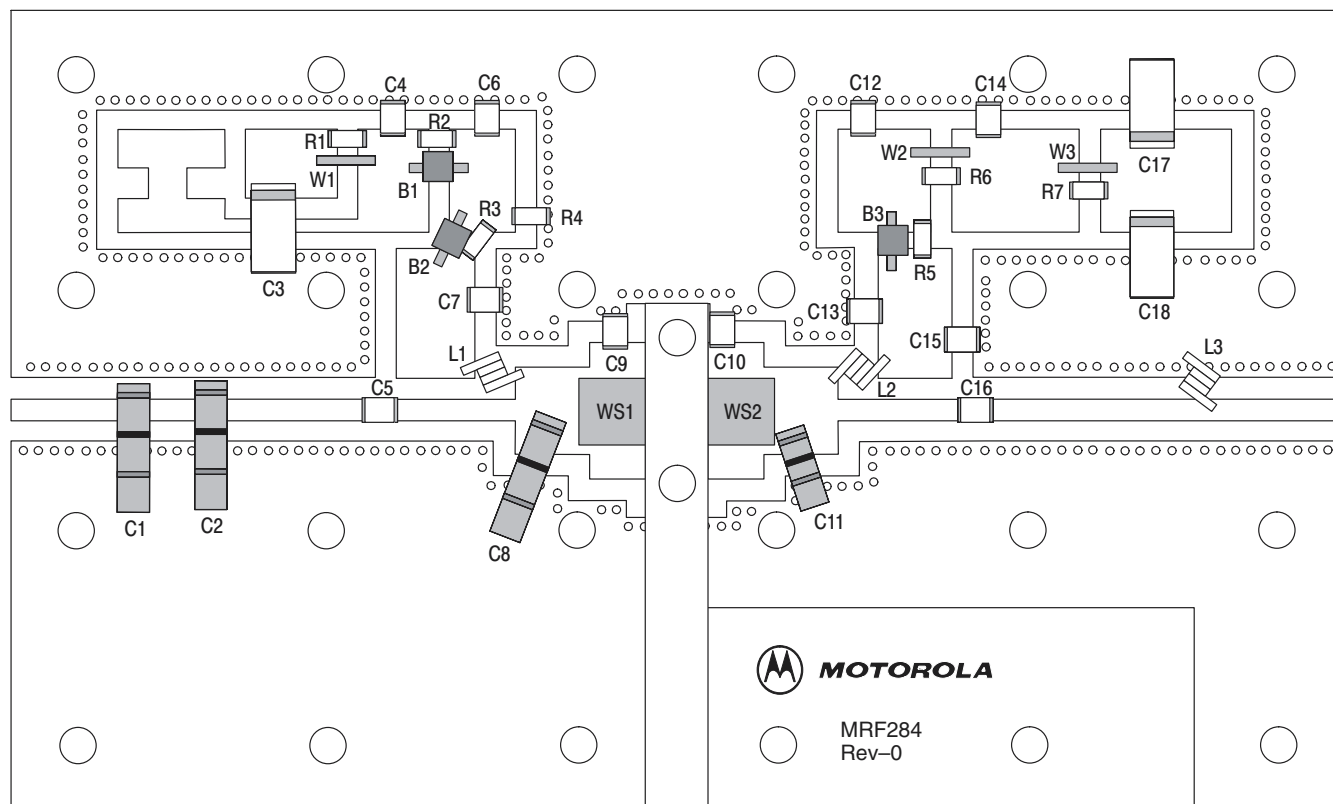


Figure 2. 1.93–2.0 GHz Broadband Test Circuit Component Layout

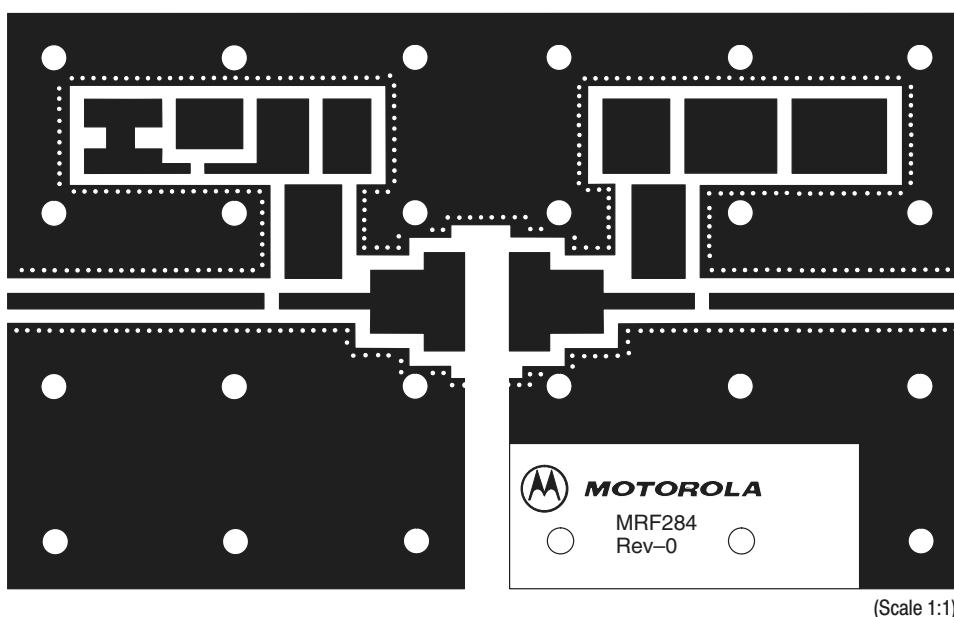


Figure 3. MRF284 Test Circuit Photomaster
(Reduced 18% in printed data book, DL110/D)

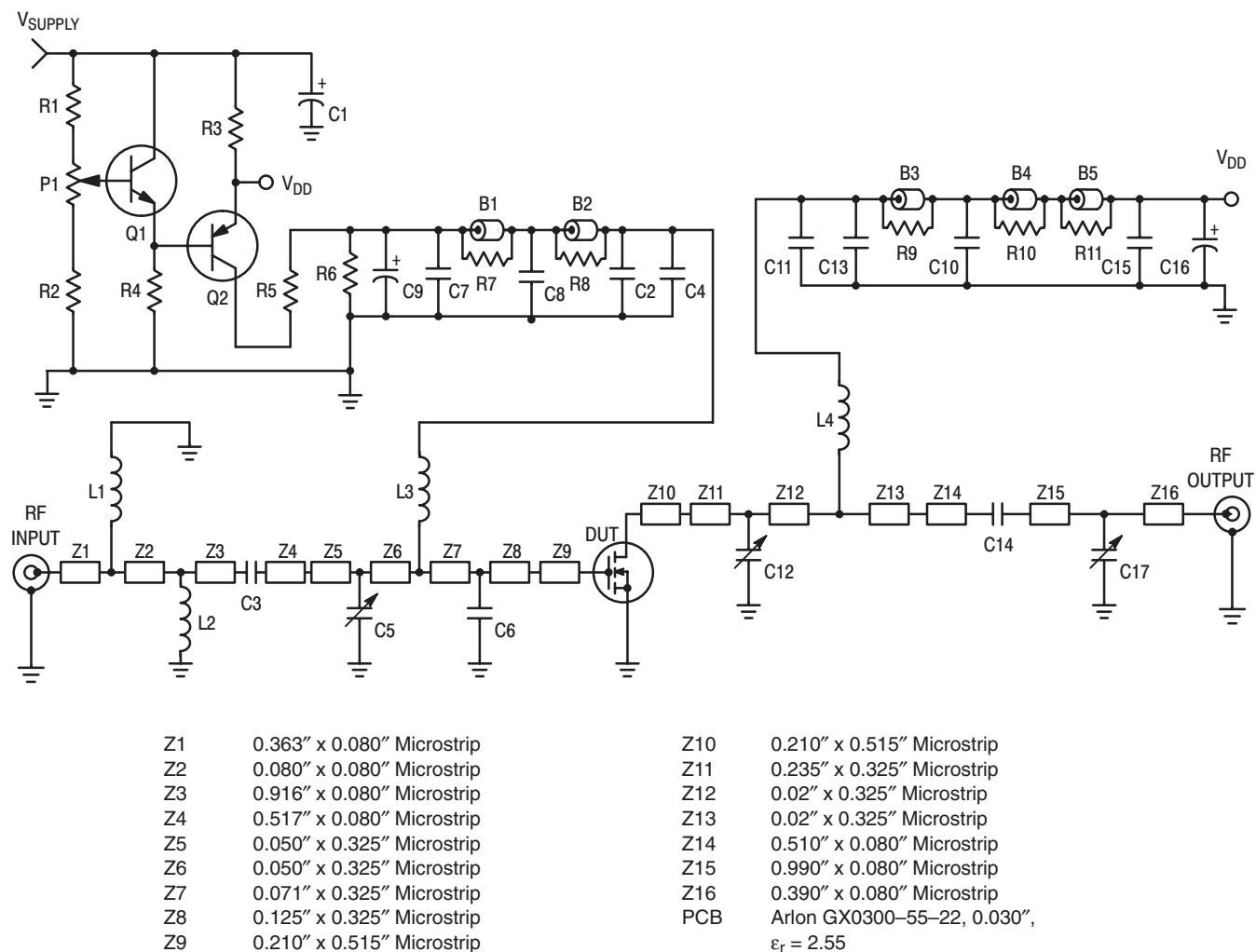


Figure 4. 2.0 GHz Class A Test Circuit Schematic

Freescale Semiconductor, Inc.

Table 2. 2.0 GHz Class A Test Circuit Component Designations and Values

Designators	Description
B1 – B5	Ferrite Beads, Round, Ferroxcube # 56–590–65–3B
C1, C9, C16	100 μ F, 50 V Electrolytic Capacitors, Mallory #SME50VB101M12X25L
C2, C13	51 pF Chip Capacitors, B Case, ATC #100B510JCA500x
C3, C14	10 pF Chip Capacitors, B Case, ATC #100B100JCA500X
C4, C11	12 pF Chip Capacitors, B Case, ATC #100B120JCA500X
C5	0.8 – 8.0 pF Variable Capacitor, Johansen Gigatrim #27291SL
C6	4.7 pF Chip Capacitor, B Case, ATC #100B4R7CCA500X
C7, C15	91 pF Chip Capacitors, B Case, ATC #100B910KP500X
C8	1000 pF Chip Capacitor, B Case, ATC #100B102JCA50X
C10	0.1 μ F Chip Capacitor, Kemet #CDR33BX104AKWS
C12, C17	0.6 – 4.5 pF Variable Capacitors, Johansen Gigatrim #27271SL
L1	4 Turns, #27 AWG, 0.087" OD, 0.050" ID, 0.069" Long, 10 nH
L2	5 Turns, #24 AWG, 0.083" OD, 0.040" ID, 0.128" Long, 12.5 nH
L3, L4	9 Turns, #26 AWG, 0.080" OD, 0.046" ID, 0.170" Long, 30.8 nH
P1	1000 Ω Potentiometer, 1/2 W, 10 Turns, Bourns
Q1	Transistor, NPN, Motorola P/N: MJD31, Case 369A–10
Q2	Transistor, PNP, Motorola P/N: MJD32, Case 369A–10
R1	360 Ω , Fixed Film Chip Resistor, 0.08" x 0.13", Garrett Instruments #RM73B2B361JT
R2	2 x 12 k Ω , Fixed Film Chip Resistor, 0.08" x 0.13", Garrett Instruments #RM73B2B122JT
R3	1 Ω , Wirewound, 5 W, 3% Resistor, Dale # RE60G1R00
R4	4 x 6.8 k Ω , Fixed Film Chip Resistor, 0.08" x 0.13", Garrett Instruments #RM73B2B682JT
R5	2 x 1500 Ω , Fixed Film Chip Resistor, 0.08" x 0.13", Garrett Instruments #RM73B2B152JT
R6	270 Ω , Fixed Film Chip Resistor, 0.08" x 0.13", Garrett Instruments #RM73B2B271JT
R7 – R11	12 Ω , Fixed Film Chip Resistors, 0.08" x 0.13", Garrett Instruments #RM73B2B120JT

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

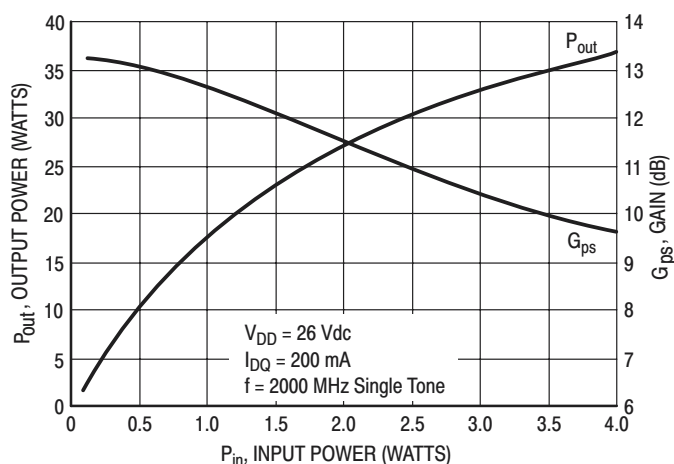


Figure 5. Output Power & Power Gain versus Input Power

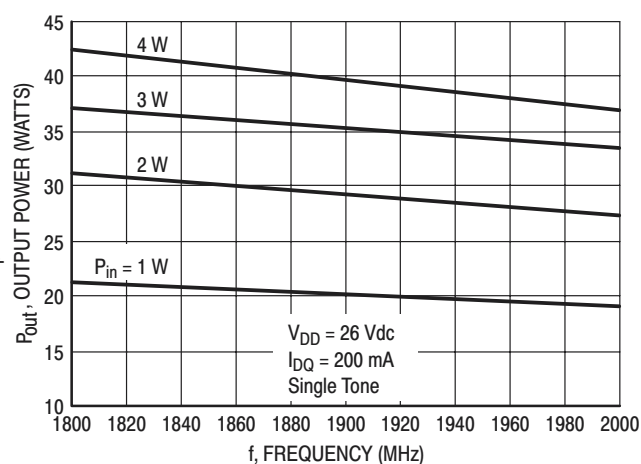


Figure 6. Output Power versus Frequency

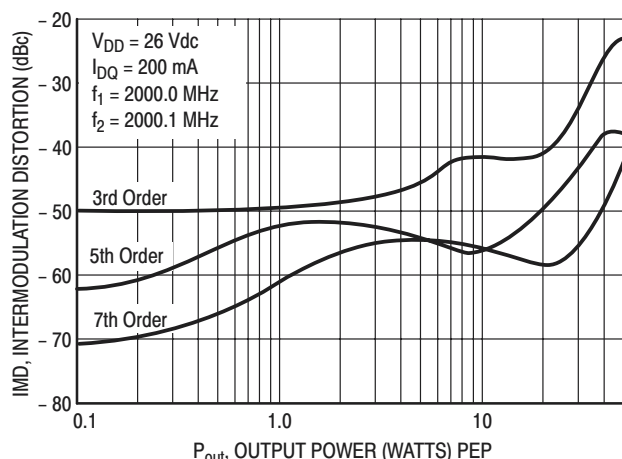


Figure 7. Intermodulation Distortion Products versus Output Power

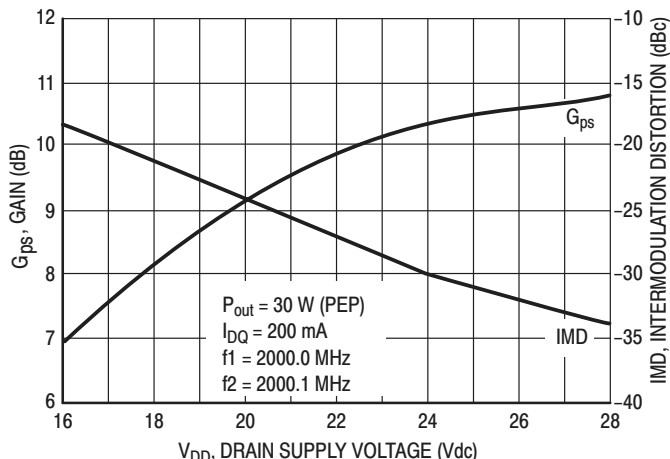


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage

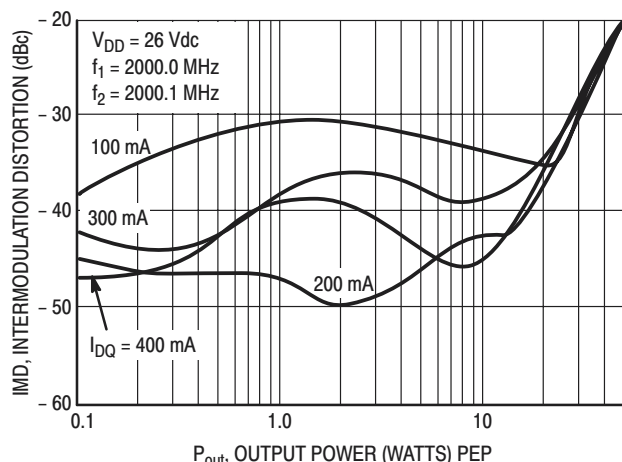


Figure 9. Intermodulation Distortion versus Output Power

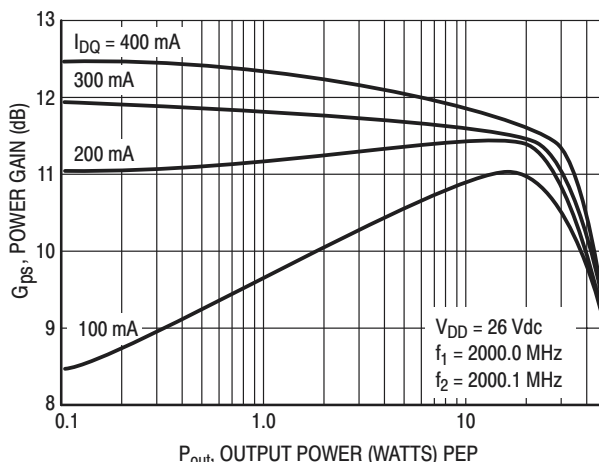


Figure 10. Power Gain versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

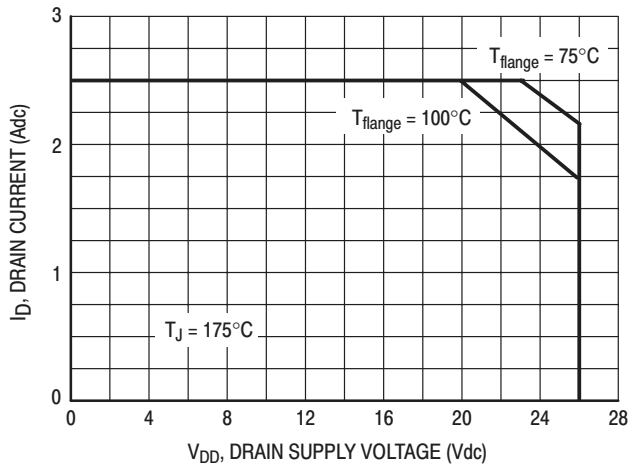


Figure 11. DC Safe Operating Area

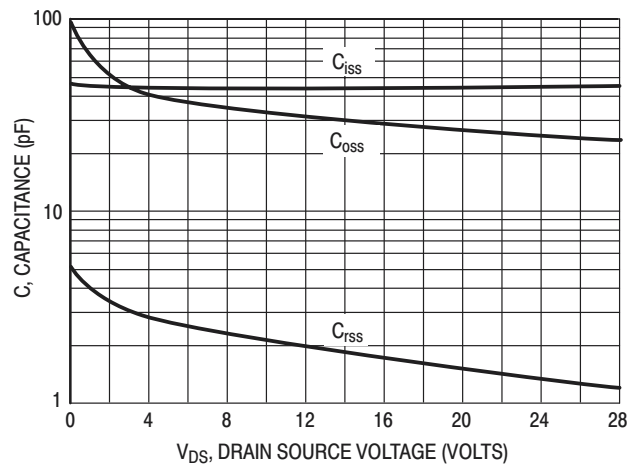


Figure 12. Capacitance versus Drain Source Voltage

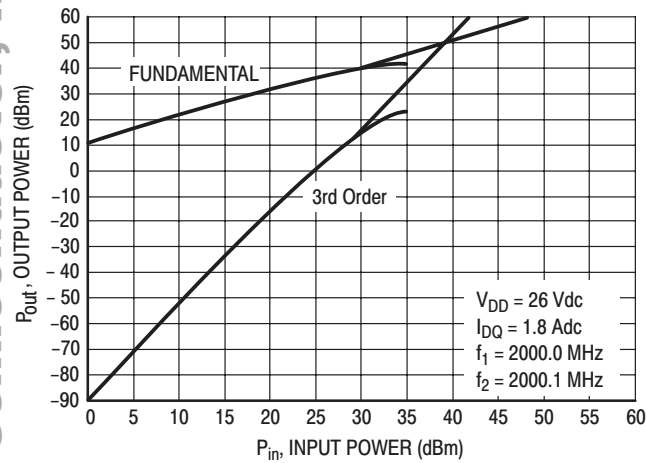


Figure 13. Class A Third Order Intercept Point

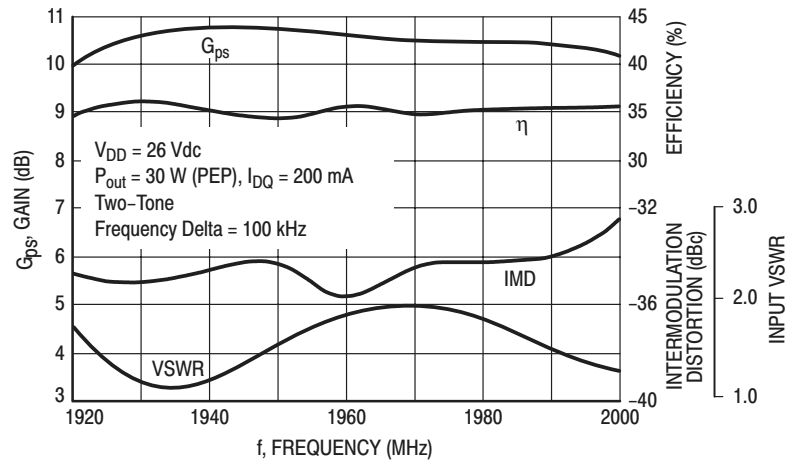
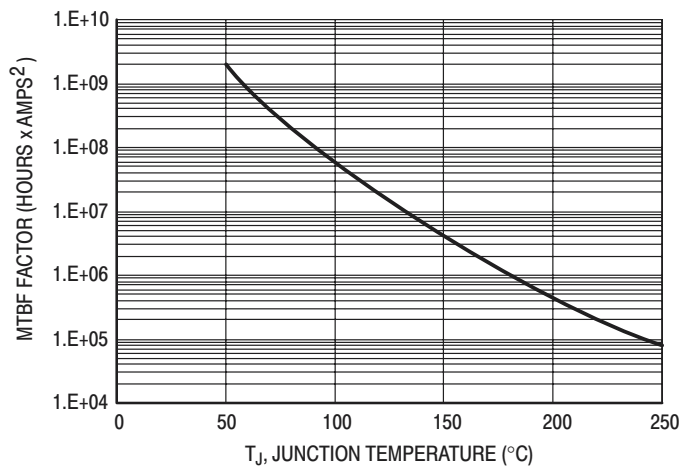


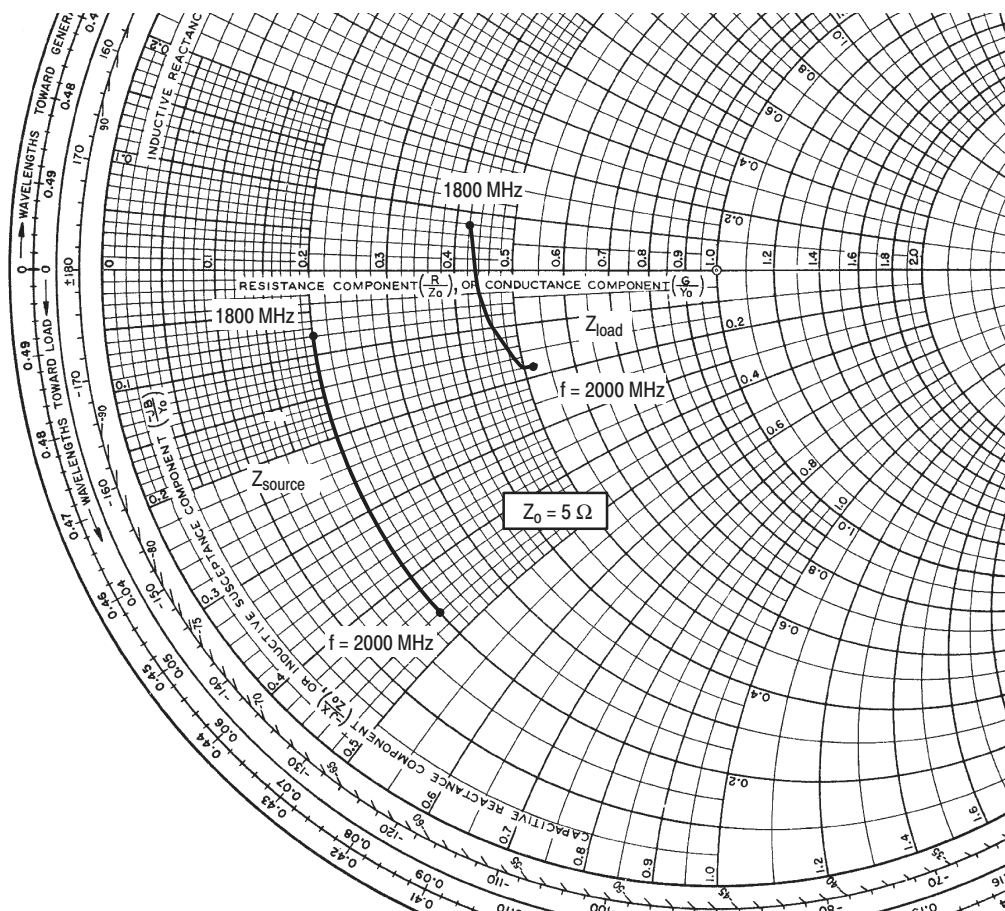
Figure 14. 1.92–2.0 GHz Broadband Circuit Performance



This graph displays calculated MTBF in hours x ampere² drain current. Life tests at elevated temperature have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 15. MTBF Factor versus Junction Temperature

Freescale Semiconductor, Inc.



$V_{CC} = 26 \text{ V}$, $I_{DQ} = 200 \text{ mA}$, $P_{out} = 15 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1800	$1.0 - j0.4$	$2.1 + j0.4$
1860	$1.0 - j0.8$	$2.2 - j0.2$
1900	$1.0 - j1.1$	$2.3 - j0.5$
1960	$1.0 - j1.4$	$2.5 - j0.9$
2000	$1.0 - j2.3$	$2.6 - j0.92$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

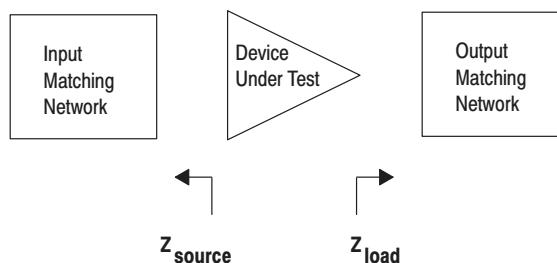


Figure 16. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field-Effect Transistor

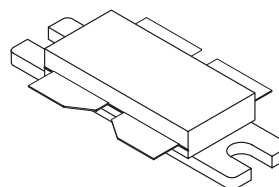
N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies from 470 to 860 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common source amplifier applications in 32 volt transmitter equipment.

- Typical Narrowband Two-Tone Performance @ $f_1 = 857$ MHz, $f_2 = 863$ MHz, 32 Volts
 Output Power — 180 Watts PEP
 Power Gain — 17 dB
 Efficiency — 36%
 IMD — -35 dBc
- Typical Broadband Two-Tone Performance @ $f_1 = 857$ MHz, $f_2 = 863$ MHz, 32 Volts
 Output Power — 180 Watts PEP
 Power Gain — 14.5 dB
 Efficiency — 37%
 IMD — -31 dBc
- Internally Matched, Controlled Q, for Ease of Use
- Integrated ESD Protection
- 100% Tested for Load Mismatch Stress at All Phase Angles with 3:1 VSWR @ 32 Vdc, $f_1 = 857$ MHz, $f_2 = 863$ MHz, 180 Watts PEP
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

MRF372

470 – 860 MHz, 180 W, 32 V
LATERAL N-CHANNEL
RF POWER MOSFET



CASE 375G-04, STYLE 1
NI-860C3

MAXIMUM RATINGS ⁽¹⁾

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	68	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Drain Current – Continuous	I_D	17	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	350 2.0	W W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.5	$^\circ\text{C/W}$

(1) Each side of device measured separately.

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

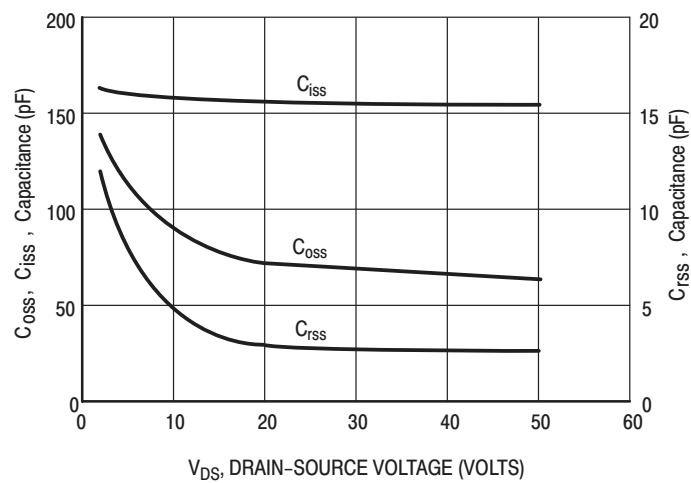
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS ⁽¹⁾					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D =10 μA)	V _{(BR)DSS}	68	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 32 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS ⁽¹⁾					
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 200 μA)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 32 V, I _D = 100 mA)	V _{GS(Q)}	2.5	3.5	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 V, I _D = 3 A)	V _{DS(on)}	—	0.28	0.45	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 3 A)	g _{fs}	—	2.6	—	S
DYNAMIC CHARACTERISTICS ⁽¹⁾					
Input Capacitance (Includes Input Matching Capacitance) (V _{DS} = 32 V, V _{GS} = 0 V, f = 1 MHz)	C _{iss}	—	260	—	pF
Output Capacitance (V _{DS} = 32 V, V _{GS} = 0 V, f = 1 MHz)	C _{oss}	—	69	—	pF
Reverse Transfer Capacitance (V _{DS} = 32 V, V _{GS} = 0 V, f = 1 MHz)	C _{rss}	—	2.5	—	pF
FUNCTIONAL CHARACTERISTICS, NARROWBAND OPERATION (In Motorola MRF372 Narrowband Circuit, 50 ohm system) ⁽²⁾					
Common Source Power Gain (V _{DD} = 32 V, P _{out} = 180 W PEP, I _{DQ} = 2 x 400 mA, f ₁ = 857 MHz, f ₂ = 863 MHz)	G _{ps}	16	17	—	dB
Drain Efficiency (V _{DD} = 32 V, P _{out} = 180 W PEP, I _{DQ} = 2 x 400 mA, f ₁ = 857 MHz, f ₂ = 863 MHz)	η	33	36	—	%
Intermodulation Distortion (V _{DD} = 32 Vdc, P _{out} = 180 W PEP, I _{DQ} = 2 x 400 mA, f ₁ = 857 MHz, f ₂ = 863 MHz)	IMD	—	–35	–31	dBc
Output Mismatch Stress (V _{DD} = 32 Vdc, P _{out} = 180 W PEP, I _{DQ} = 2 x 400 mA, f ₁ = 857 MHz, f ₂ = 863 MHz, V _{SWR} = 3:1 at all phase angles of test)	ψ	No Degradation in Output Power			
TYPICAL CHARACTERISTICS, BROADBAND OPERATION (In Motorola MRF372 Broadband Circuit, 50 ohm system) ⁽²⁾					
Common Source Power Gain (V _{DD} = 32 Vdc, P _{out} = 180 W PEP, I _{DQ} = 2 x 500 mA, f ₁ = 857 MHz, f ₂ = 863 MHz)	G _{ps}	—	14.5	—	dB
Drain Efficiency (V _{DD} = 32 Vdc, P _{out} = 180 W PEP, I _{DQ} = 2 x 500 mA, f ₁ = 857 MHz, f ₂ = 863 MHz)	η	—	37	—	%
Intermodulation Distortion (V _{DD} = 32 Vdc, P _{out} = 180 W PEP, I _{DQ} = 2 x 500 mA, f ₁ = 857 MHz, f ₂ = 863 MHz)	IMD	—	–31	—	dBc

(1) Each side of device measured separately.

(2) Measured in push–pull configuration.

Freescal Semiconductor, Inc.

TYPICAL CHARACTERISTICS



Note: C_{iss} does not include input matching capacitance.

Figure 1. Capacitance versus Voltage

Freescale Semiconductor, Inc.

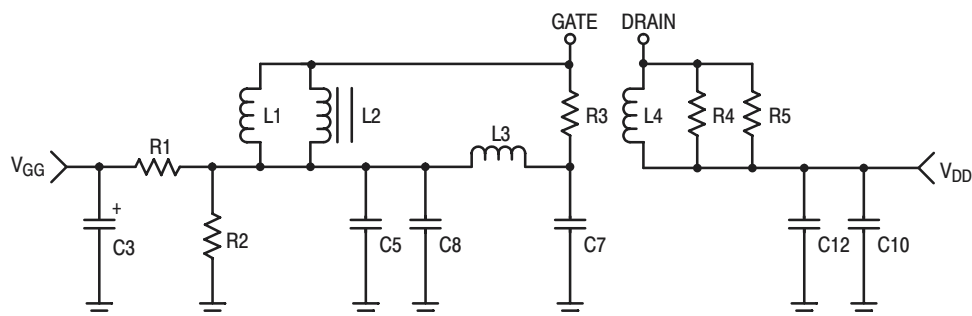
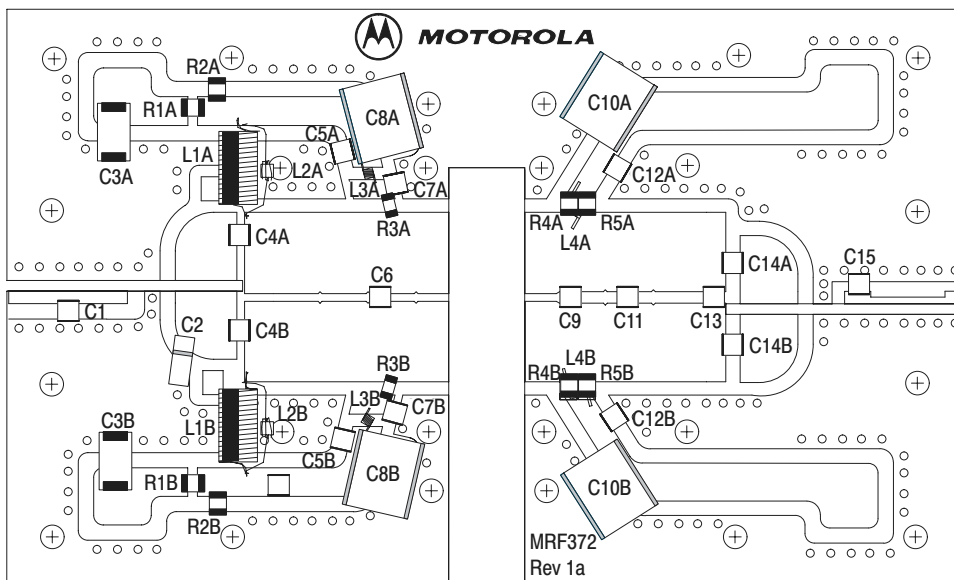


Figure 2. 860 MHz Narrowband DC Bias Networks

Table 1. 860 MHz Narrowband DC Bias Networks Component Designations and Values

Designation	Description
C1	2.2 pF Chip Capacitor, B Case, ATC
C2	0.5 — 5.0 pF Variable Capacitor, B Case, Johansen Gigatrim
C3A, B	22 μ F, 22 V Tantalum Chip Capacitors, Kemet #T491D226K22AS
C4A, B, C14A, B	47.0 pF Chip Capacitors, B Case, ATC
C5A, B	100 pF Chip Capacitors, B Case, ATC
C6	10.0 pF Chip Capacitor, B Case, ATC
C7A, B	2.7 pF Chip Capacitors, A Case, ATC
C8A, B	1.0 μ F, 100 V Chip Capacitors, Vitramon #VJ3640Y105KXBAT
C9	10.0 pF Chip Capacitor, B Case, ATC
C10A, B	2.2 μ F, 100 V Chip Capacitors, Vitramon #VJ3640Y225KXBAT
C11	5.1 pF Chip Capacitor, B Case, ATC
C12A, B	0.01 μ F, 100 V Chip Capacitors, Kemet #VJ1210Y103KXBAT
C13	3.9 pF Chip Capacitor, B Case, ATC
C15	1.2 pF Chip Capacitor, B Case, ATC
L1A, B	130 nH, Coilcraft #132–11SM
L2A, B	#24 AWG, 3 Turns Loose, Fair Rite #2643706001
L3A, B	3.85 nH, Coilcraft #0906–4
L4A, B	5.0 nH, Coilcraft #A02T
R1A, B, R2A, B R4A, B, R5A, B	180 Ω , 1/4 W Chip Resistors, Vishay Dale (1210)
R3A, B	12 Ω , 1/8 W Chip Resistors, Vishay Dale (1206)
PCB	MRF372 Printed Circuit Board Rev 1a, Rogers RO4350, Height 30 mils, $\epsilon_r = 3.48$
Balun A, B	Vertical 860 MHz Broadband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, $\epsilon_r = 10.2$



Vertical Balun Mounting Detail

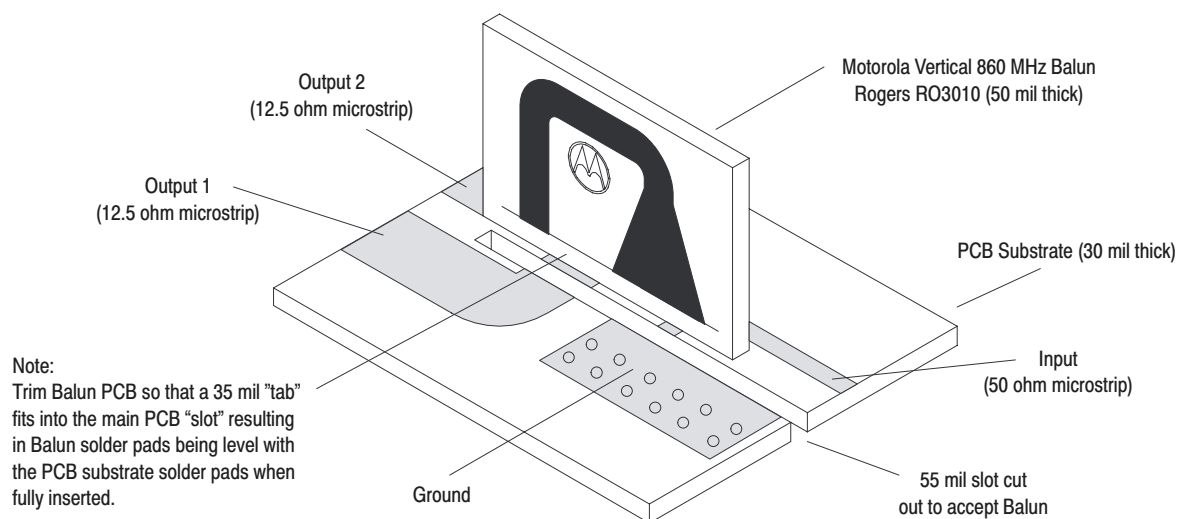
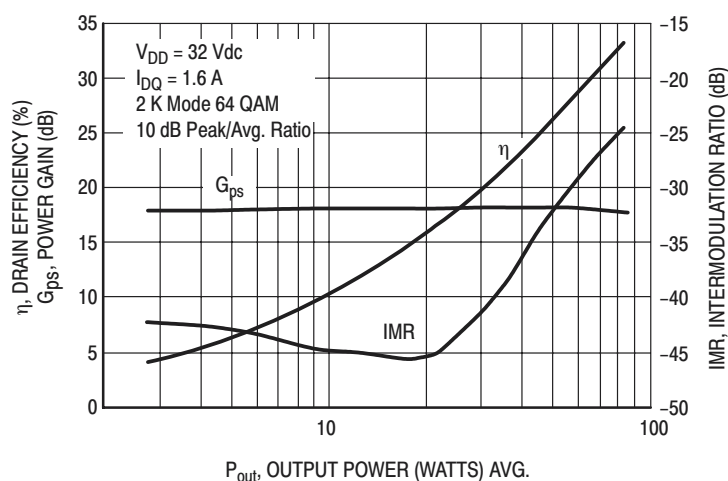


Figure 3. 860 MHz Narrowband Component Layout

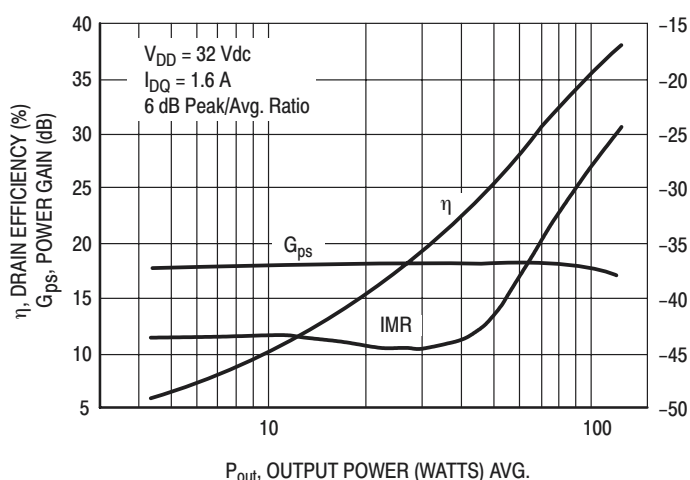
Freescale Semiconductor, Inc.

TYPICAL TWO-TONE NARROWBAND CHARACTERISTICS



Note: IMR measured using Delta Marker Method.

Figure 4. COFDM Performance (860 MHz)



Note: IMR measured using Delta Marker Method.

Figure 5. 8-VSB Performance (860 MHz)

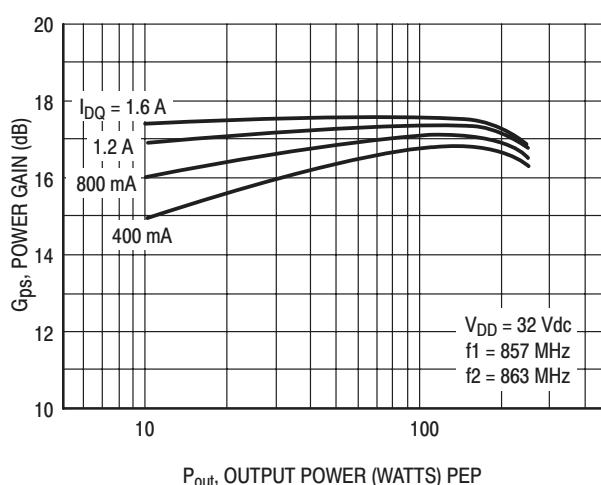


Figure 6. Power Gain versus Output Power

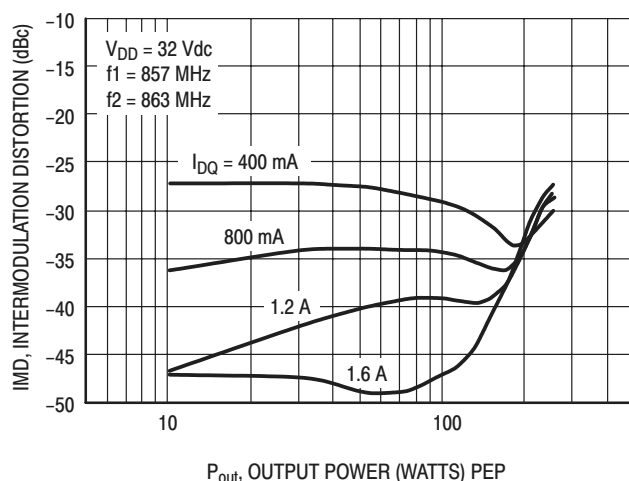


Figure 7. Intermodulation Distortion versus Output Power

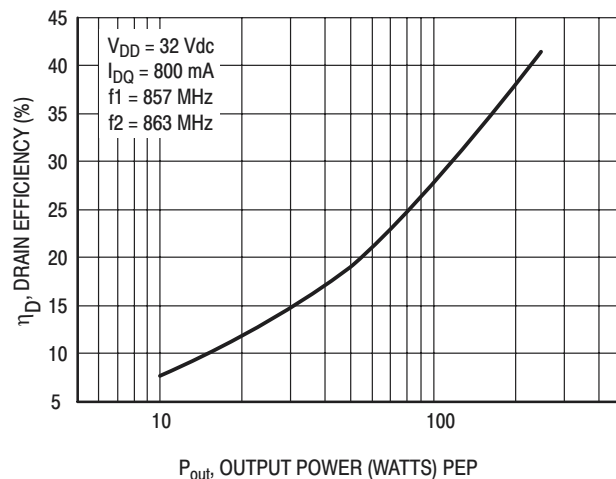
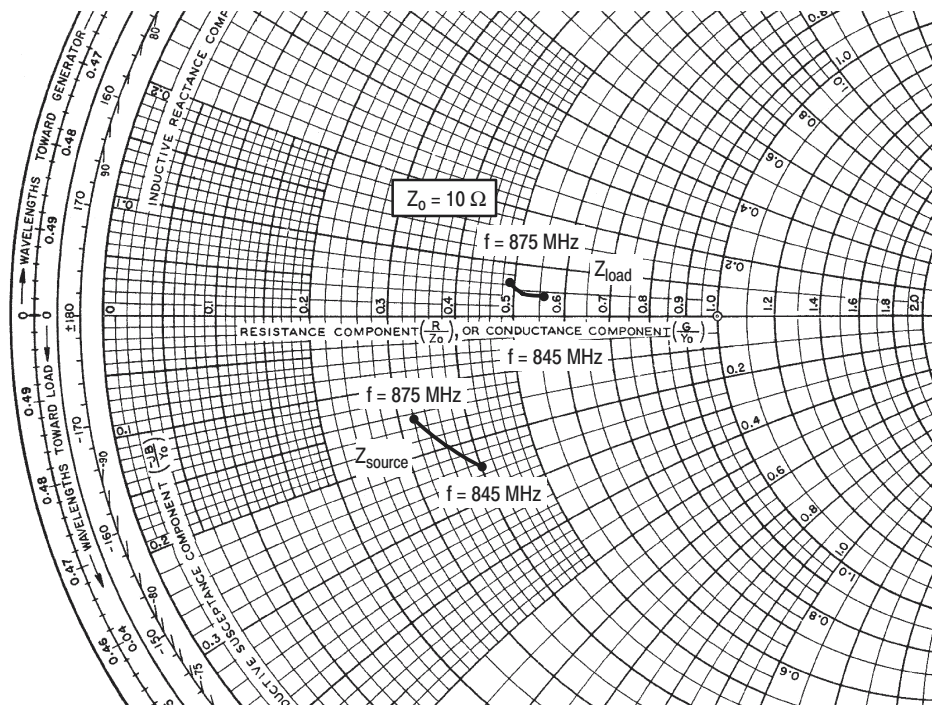


Figure 8. Drain Efficiency versus Output Power



$V_{DD} = 32 \text{ V}$, $I_{DQ} = 800 \text{ mA}$, $P_{\text{out}} = 180 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
845	$3.99 - j2.50$	$5.63 + j0.38$
860	$3.56 - j1.98$	$5.28 + j0.43$
875	$3.18 - j1.46$	$4.94 + j0.56$
Harmonics		
f GHz	Z_{source} Ω	Z_{load} Ω
1.69	$2.85 + j14.30$	$1.23 + j9.37$
1.72	$3.27 + j14.32$	$1.54 + j9.60$
1.75	$3.35 + j14.36$	$1.73 + j9.62$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

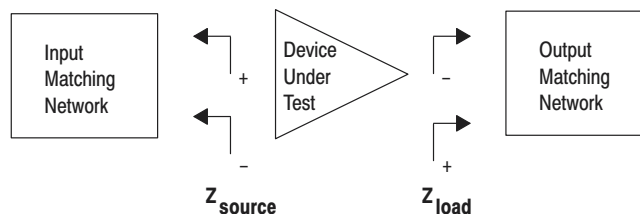


Figure 9. Narrowband Series Equivalent Input and Output Impedance

Freescale Semiconductor, Inc.

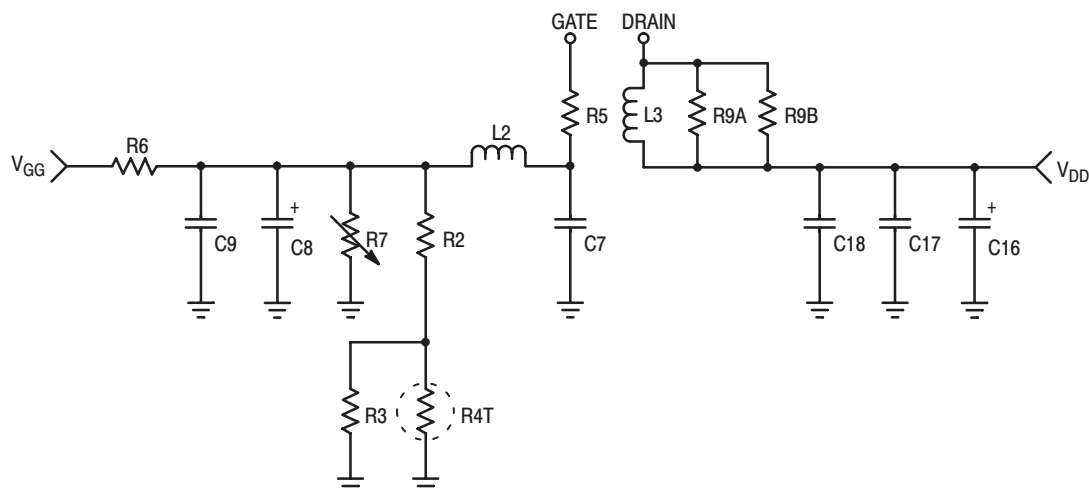
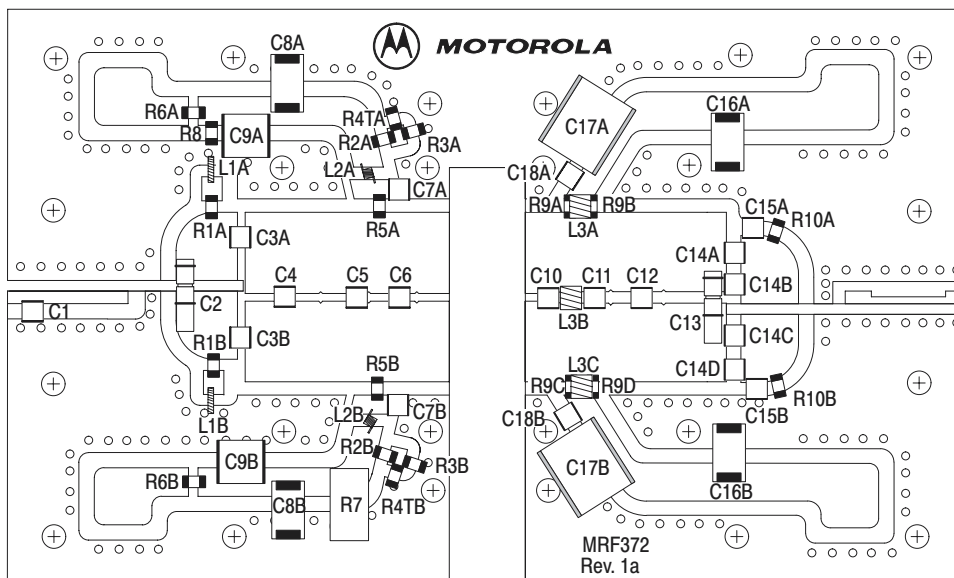


Figure 10. 470–860 MHz Broadband DC Bias Networks

Table 2. 470–860 MHz Broadband DC Bias Networks Component Designations and Values

Designation	Description
C1	0.7 pF Chip Capacitor, B Case, ATC
C2, C13	0.8 — 8.0 pF Variable Capacitors, Johansen Gigatrim
C3A, B, C14A, B, C, D	100 pF Chip Capacitors, B Case, ATC
C4	4.7 pF, Chip Capacitor, B Case, ATC
C5	7.5 pF Chip Capacitor, B Case, ATC
C6	10.0 pF Chip Capacitor, B Case, ATC
C7A, B	6.2 pF Chip Capacitors, A Case, ATC
C8A, B	22 μ F, 22 V Tantalum Chip Capacitors, Kemet #T491D226K22AS
C9A, B	0.1 μ F, 100 V Chip Capacitors, Vitramon #VJ3640Y104KXBAT
C10	13 pF Chip Capacitor, B Case, ATC
C11	6.8 pF Chip Capacitor, B Case, ATC
C12	3.9 pF Chip Capacitor, B Case, ATC
C15A, B	3.3 pF Chip Capacitors, B Case, ATC
C16A, B	10 μ F, 35 V Tantalum Chip Capacitors, Kemet #T491D106K35AS
C17A, B	3.3 μ F, 100 V Chip Capacitors, Vitramon #VJ3640Y335KXBAT
C18A, B	0.01 μ F Chip Capacitors, B Case, ATC
L1A, B	12.55 nH, Coilcraft #1606–10
L2A, B	5.45 nH, Coilcraft #0906–5
L3A, B, C	12.5 nH, Coilcraft #A04T
R1A, B	10 Ω , 1/4 W Chip Resistors, Vishay Dale (1210)
R2A, B	2.2 k Ω , 1/4 W Chip Resistors, Vishay Dale (1210)
R3A, B, R10A, B	390 Ω , 1/8 W Chip Resistors, Vishay Dale (1206)
R4TA, B	520 Ω , Thermistor, Vishay #NTHS—1206J14520R5%
R5A, B	6.2 Ω , 1/4 W Chip Resistors, Vishay Dale (1210)
R6A, B	6.8 k Ω , 1/4 W Chip Resistors, Vishay Dale (1210)
R7	100 k Ω Potentiometer, Bourns
R8	47.3 k Ω , 1/8 W Chip Resistor, Vishay Dale (1206)
R9A, B, C, D	180 Ω , 1/4 W Chip Resistors, Vishay Dale (1210)
PCB	MRF372 Printed Circuit Board Rev 1a, Rogers RO4350, Height 30 mils, $\epsilon_r = 3.48$
Balun A, B	Vertical 660 MHz Broadband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, $\epsilon_r = 10.2$

Freescale Semiconductor, Inc.



Vertical Balun Mounting Detail

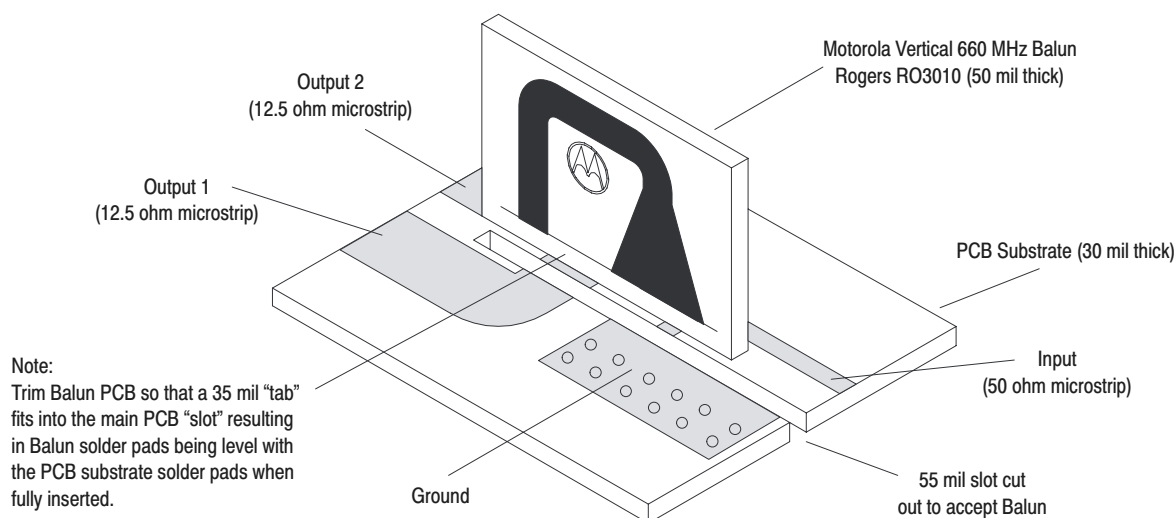


Figure 11. 470–860 MHz Broadband Component Layout

Freescale Semiconductor, Inc.

TYPICAL TWO-TONE BROADBAND CHARACTERISTICS

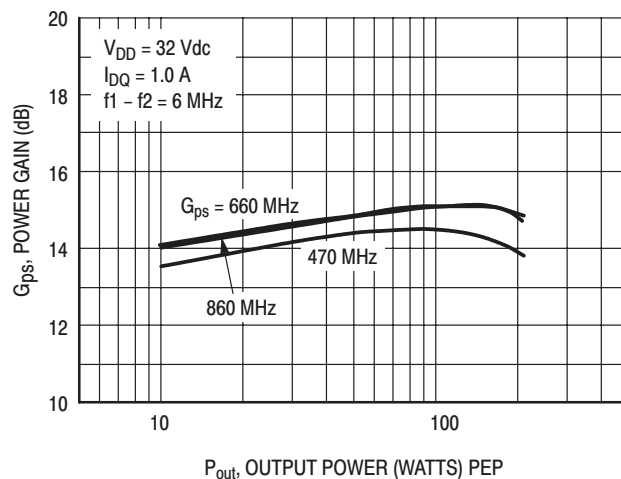


Figure 12. Power Gain versus Output Power

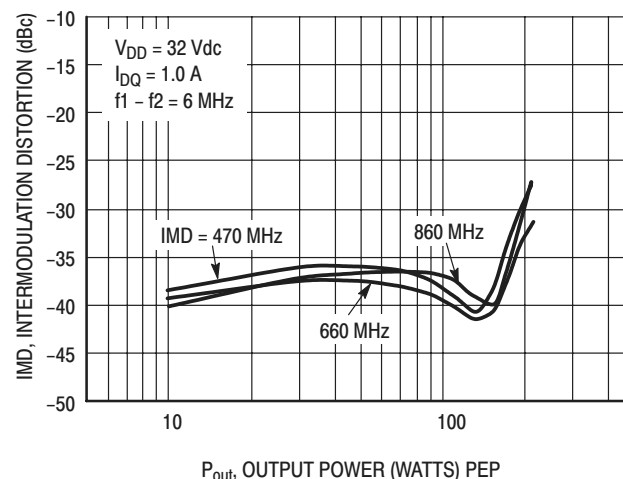


Figure 13. Intermodulation Distortion versus Output Power

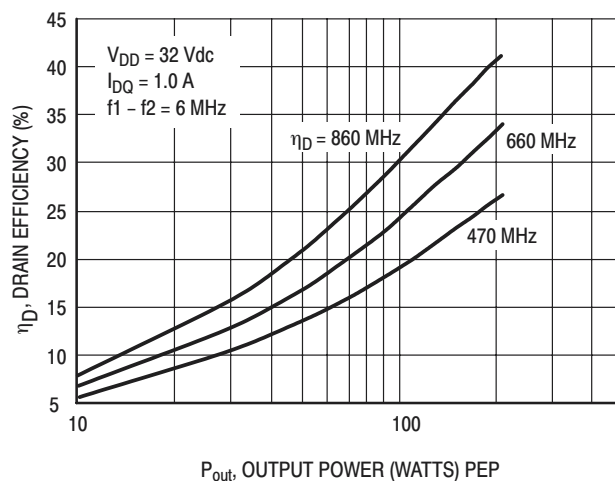
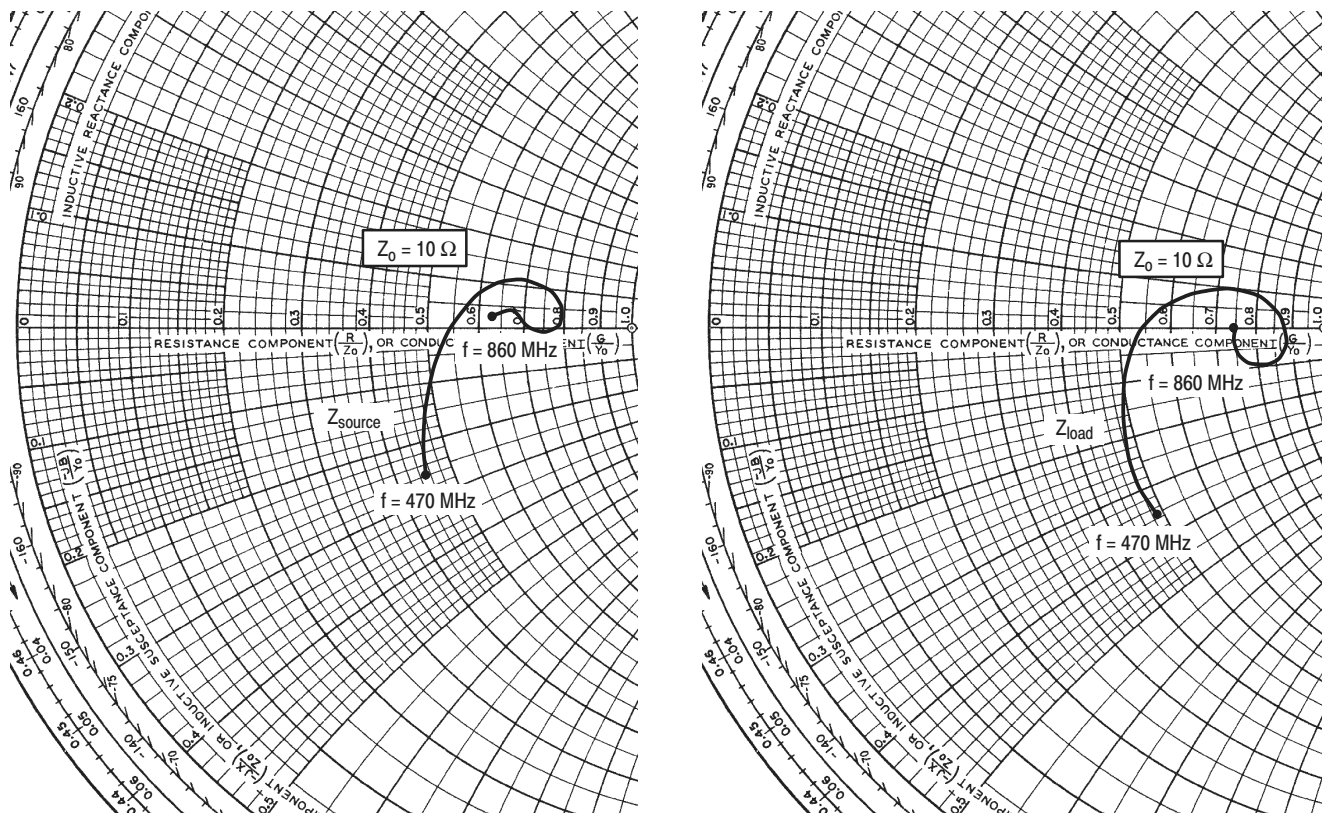


Figure 14. Drain Efficiency versus Output Power



$V_{DD} = 32 \text{ V}$, $I_{DQ} = 1.0 \text{ A}$, $P_{out} = 180 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
470	$4.46 - j2.57$	$4.88 - j3.50$
560	$6.40 + j1.06$	$5.45 - j0.07$
660	$7.84 + j0.14$	$8.13 + j0.73$
760	$6.67 + j0.46$	$8.27 - j1.00$
860	$6.25 + j0.31$	$7.52 + j0.02$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

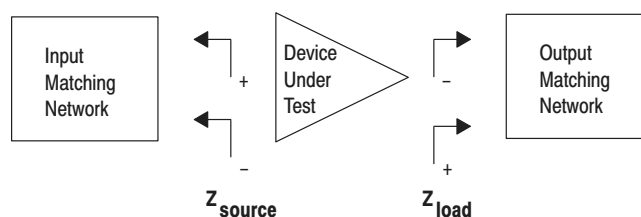


Figure 15. Broadband Series Equivalent Input and Output Impedance

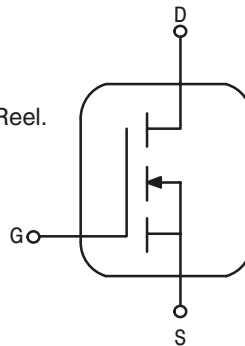
The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

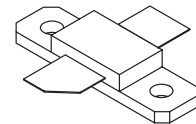
Designed for broadband commercial and industrial applications with frequencies from 470 to 860 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 28/32 volt transmitter equipment.

- Typical CW Performance at 860 MHz, 32 Volts, Narrowband Fixture
Output Power — 75 Watts
Power Gain — 18.2 dB
Efficiency — 60%
- 100% Tested for Load Mismatch Stress at All Phase Angles with 10:1 VSWR @ 32 Vdc, 860 MHz, 75 Watts CW
- Integrated ESD Protection
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R1 = 500 units per 32 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads.
L Suffix Indicates 40μ" Nominal.

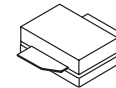


MRF373AR1 MRF373ALSR1

470 – 860 MHz, 75 W, 32 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B-05, STYLE 1
NI-360
MRF373AR1



CASE 360C-05, STYLE 1
NI-360S
MRF373ALSR1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	70	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	197 1.12 278 1.59	Watts W/ $^\circ\text{C}$ Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.89 0.63	$^\circ\text{C/W}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum) M1 (Minimum)

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 3

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 1 μA)	V _{(BR)DSS}	70	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 32 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 200 μA)	V _{GS(th)}	2	2.9	4	Vdc
Gate Quiescent Voltage (V _{DS} = 32 V, I _D = 100 mA)	V _{GS(Q)}	2.5	3.3	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 V, I _D = 3 A)	V _{DS(on)}	—	0.41	0.45	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V _{DS} = 32 V, V _{GS} = 0, f = 1 MHz)	C _{iss}	—	98.5	—	pF
Output Capacitance (V _{DS} = 32 V, V _{GS} = 0, f = 1 MHz)	C _{oss}	—	49	—	pF
Reverse Transfer Capacitance (V _{DS} = 32 V, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	2	—	pF
FUNCTIONAL CHARACTERISTICS (50 ohm system)					
Common Source Power Gain (V _{DD} = 32 V, P _{out} = 75 W CW, I _{DQ} = 200 mA, f = 860 MHz)	G _{ps}	16.5	18.2	—	dB
Drain Efficiency (V _{DD} = 32 V, P _{out} = 75 W CW, I _{DQ} = 200 mA, f = 860 MHz)	η	56	60	—	%
Load Mismatch (V _{DD} = 32 V, P _{out} = 75 W CW, I _{DQ} = 200 mA, f = 860 MHz, Load VSWR at 10:1 at All Phase Angles)	ψ	No Degradation in Output Power			

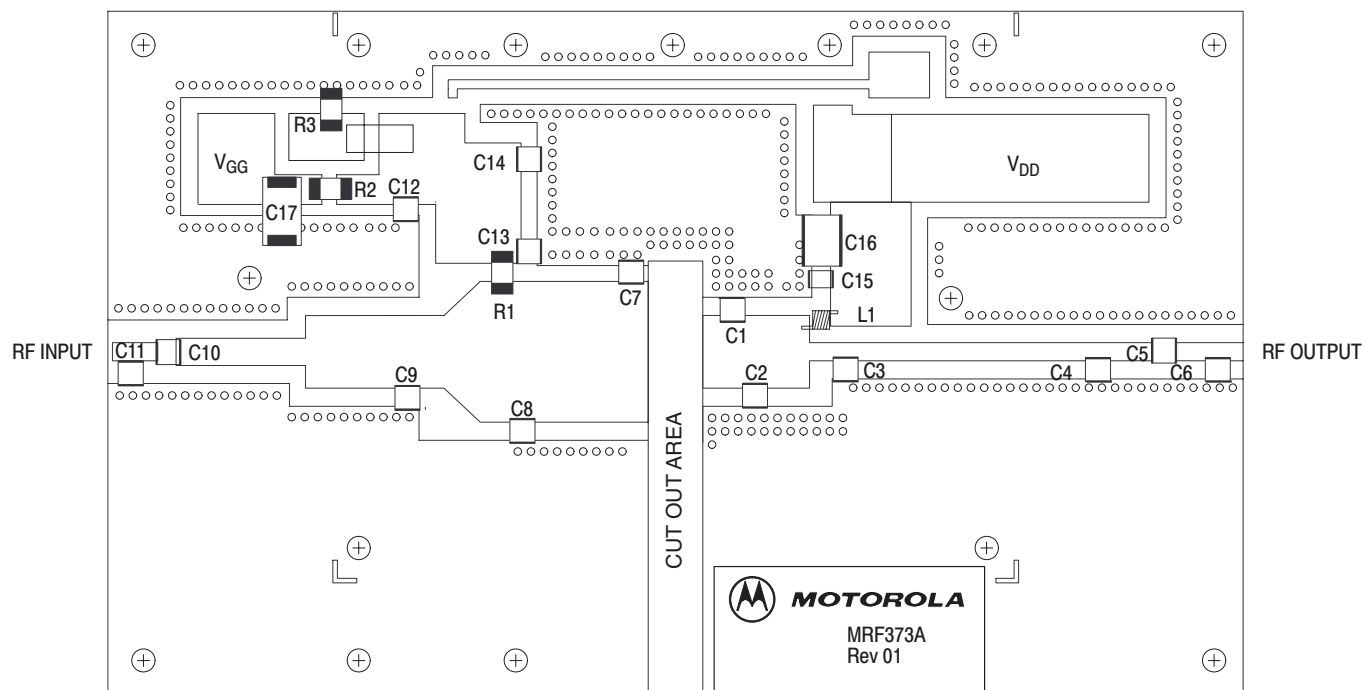


Figure 1. MRF373AR1/ALSR1 Narrowband Test Circuit Component Layout

Table 1. MRF373AR1/ALSR1 Narrowband Test Circuit Component Layout Designations and Values

Designation	Description
C1, C2	18 pF Chip Capacitors, B Case, ATC
C3	12 pF Chip Capacitor, B Case, ATC
C4	1.8 pF Chip Capacitor, B Case, ATC
C5, C10	51 pF Chip Capacitors, B Case, ATC
C6	0.3 pF Chip Capacitor, B Case, ATC (Used only on the MRF373AS)
C7	15 pF Chip Capacitor, B Case, ATC
C8	10 pF Chip Capacitor, B Case, ATC
C9	2.7 pF Chip Capacitor, B Case, ATC
C11	0.5 pF Chip Capacitor, B Case, ATC
C12	1000 pF Chip Capacitor, B Case, ATC
C13	39 pF Chip Capacitor, B Case, ATC
C14, C15	470 pF Chip Capacitors, B Case, ATC
C16	2.2 μ F, 100 V Chip Capacitor, Vishay #VJ3640Y225KXBAT
C17	10 μ F, 35 V Tantalum Capacitor, Kemet #T491D106K35AS
L1A	12 nH, Coilcraft #A04T
R1, R2	390 Ω , 1/2 Ω Chip Resistors, Vishay Dale (2010)
R3	1 k Ω , 1/2 Ω Chip Resistor, Vishay Dale (2010)
PCB	Arlon GX-0300-55, 30 mils, $\epsilon_r = 2.55$

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

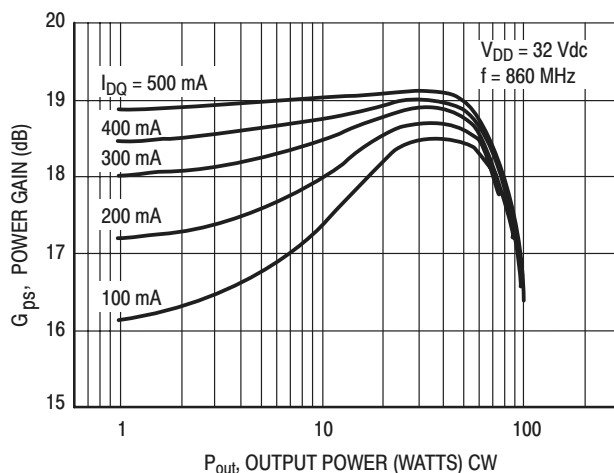


Figure 2. Power Gain versus Output Power

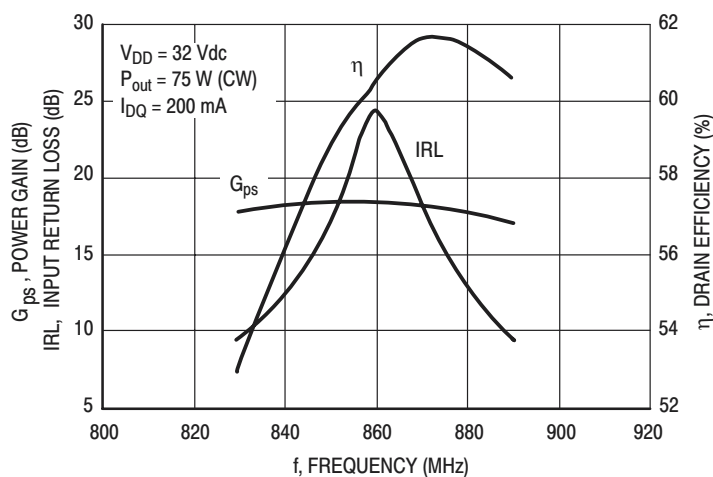


Figure 3. Performance in Narrowband Circuit

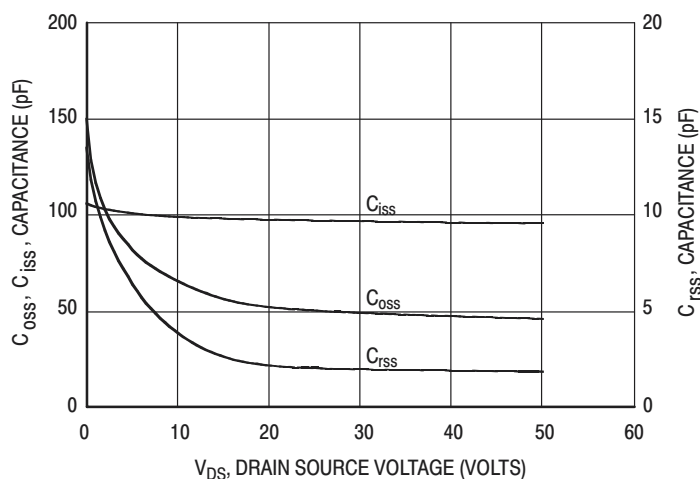
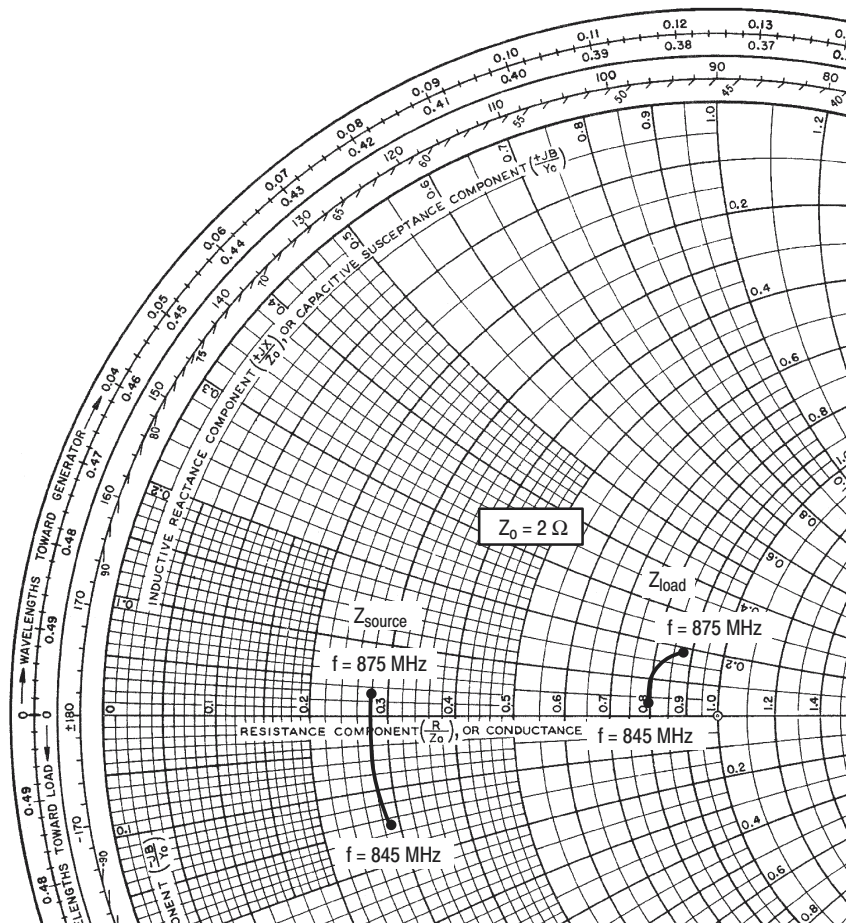


Figure 4. Capacitance versus Voltage



$V_{DD} = 32 \text{ V}$, $I_{DQ} = 200 \text{ mA}$, $P_{out} = 75 \text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
845	$0.58 - j0.29$	$1.60 + j0.07$
860	$0.56 - j0.11$	$1.65 + j0.22$
875	$0.56 + j0.06$	$1.79 + j0.38$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

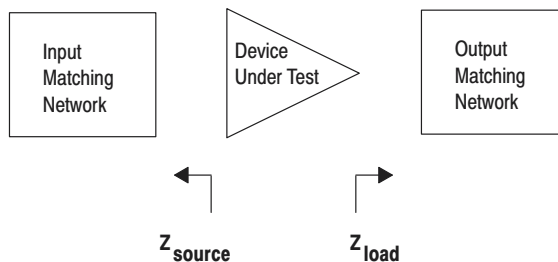
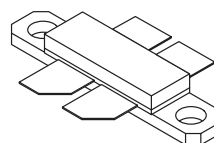


Figure 5. Series Equivalent Input and Output Impedance

The RF MOSFET Line
RF Power Field-Effect Transistor
N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies from 470 to 860 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common source amplifier applications in 28/32 volt transmitter equipment.

- Typical Two-Tone Performance @ 860 MHz, 32 Volts, Narrowband Fixture
Output Power — 130 Watts PEP
Power Gain — 17.3 dB
Efficiency — 41%
IMD — -32.5 dBc
- 100% Tested for Load Mismatch Stress at All Phase Angles with 10:1 VSWR @ 32 Vdc, 860 MHz, 130 Watts, f1 = 857 MHz, f2 = 863 MHz
- Integrated ESD Protection
- Excellent Thermal Stability
- Characterized with Differential Large-Signal Impedance Parameters

MRF374A
470 – 860 MHz, 130 W, 32 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET

CASE 375F-04, STYLE 1
NI-650
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	70	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	302 1.72	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.58	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

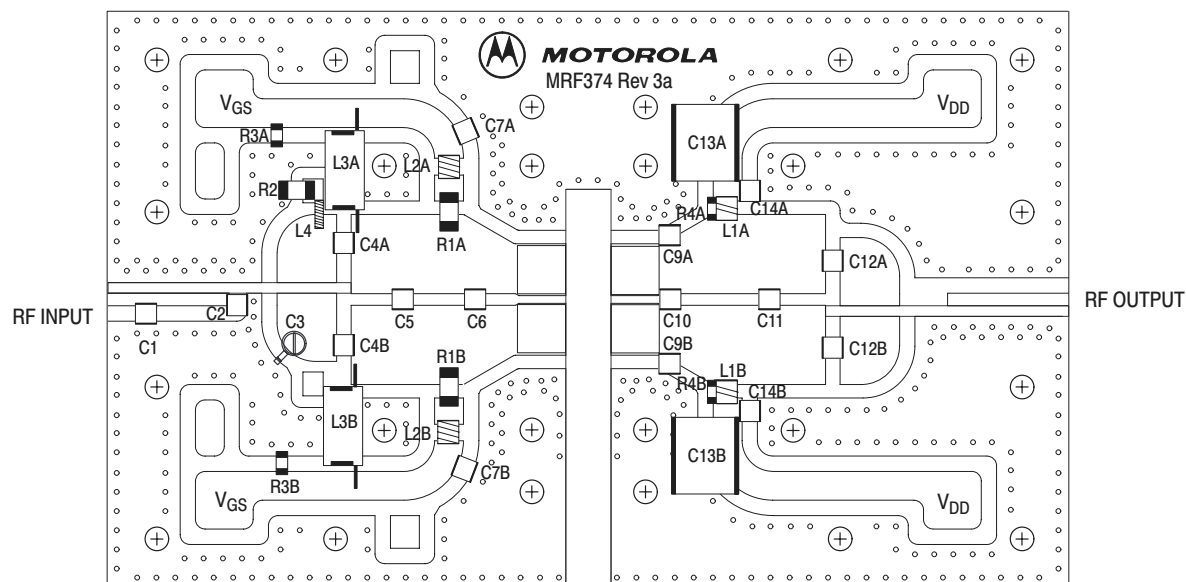
Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS ⁽¹⁾					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D =10 μA)	V _{(BR)DSS}	70	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 32 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS ⁽¹⁾					
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 200 μA)	V _{GS(th)}	2	2.9	4	Vdc
Gate Quiescent Voltage (V _{DS} = 32 V, I _D = 100 mA)	V _{GS(Q)}	2.5	3.3	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 V, I _D = 3 A)	V _{DS(on)}	—	0.41	0.45	Vdc
DYNAMIC CHARACTERISTICS ⁽¹⁾					
Input Capacitance (V _{DS} = 32 V, V _{GS} = 0 V, f = 1 MHz)	C _{iss}	—	97.3	—	pF
Output Capacitance (V _{DS} = 32 V, V _{GS} = 0 V, f = 1 MHz)	C _{oss}	—	49	—	pF
Reverse Transfer Capacitance (V _{DS} = 32 V, V _{GS} = 0 V, f = 1 MHz)	C _{rss}	—	1.91	—	pF
FUNCTIONAL CHARACTERISTICS, NARROWBAND OPERATION (In Motorola MRF374A Narrowband Circuit, 50 ohm system) ⁽²⁾					
Common Source Power Gain (V _{DD} = 32 Vdc, P _{out} = 130 W PEP, I _{DQ} = 2 x 200 mA, f1 = 857 MHz, f2 = 863 MHz)	G _{ps}	16	17.3	—	dB
Drain Efficiency (V _{DD} = 32 Vdc, P _{out} = 130 W PEP, I _{DQ} = 2 x 200 mA, f1 = 857 MHz, f2 = 863 MHz)	η	36	41.2	—	%
Intermodulation Distortion (V _{DD} = 32 Vdc, P _{out} = 130 W PEP, I _{DQ} = 2 x 200 mA, f1 = 857 MHz, f2 = 863 MHz)	IMD	—	–32.5	–28	dB
Load Mismatch (V _{DD} = 32 Vdc, P _{out} = 130 W Two–Tone, I _{DQ} = 2 x 200 mA, f1 = 857 MHz, f2 = 863 MHz, VSWR 10:1 at All Phase Angles of Test)		No Degradation in Output Power			
TYPICAL CHARACTERISTICS, BROADBAND OPERATION (In Motorola MRF374 Broadband Circuit, 50 ohm system)					
Common Source Power Gain (V _{DD} = 32 Vdc, P _{out} = 100 W PEP, I _{DQ} = 750 mA, f1 = 857 MHz, f2 = 863 MHz)	G _{ps}	—	15.8	—	dB
Drain Efficiency (V _{DD} = 32 Vdc, P _{out} = 100 W PEP, I _{DQ} = 750 mA, f1 = 857 MHz, f2 = 863 MHz)	η	—	35	—	%
Intermodulation Distortion (V _{DD} = 32 Vdc, P _{out} = 100 W PEP, I _{DQ} = 750 mA, f1 = 857 MHz, f2 = 863 MHz)	IMD	—	34.5	—	dB

(1) Each side of device measured separately.

(2) Measured in push–pull configuration.



Vertical Balun Mounting Detail

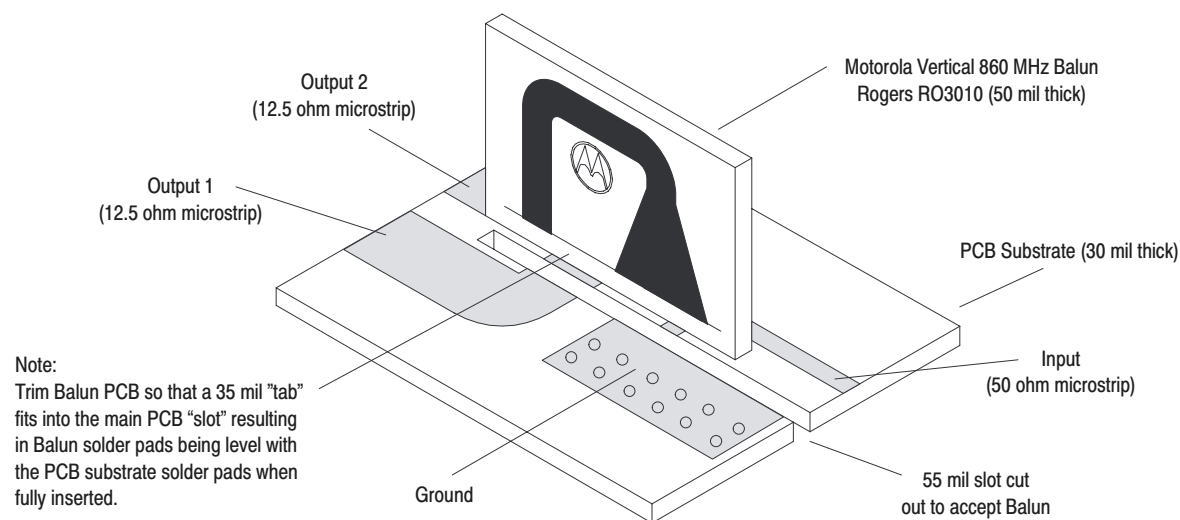
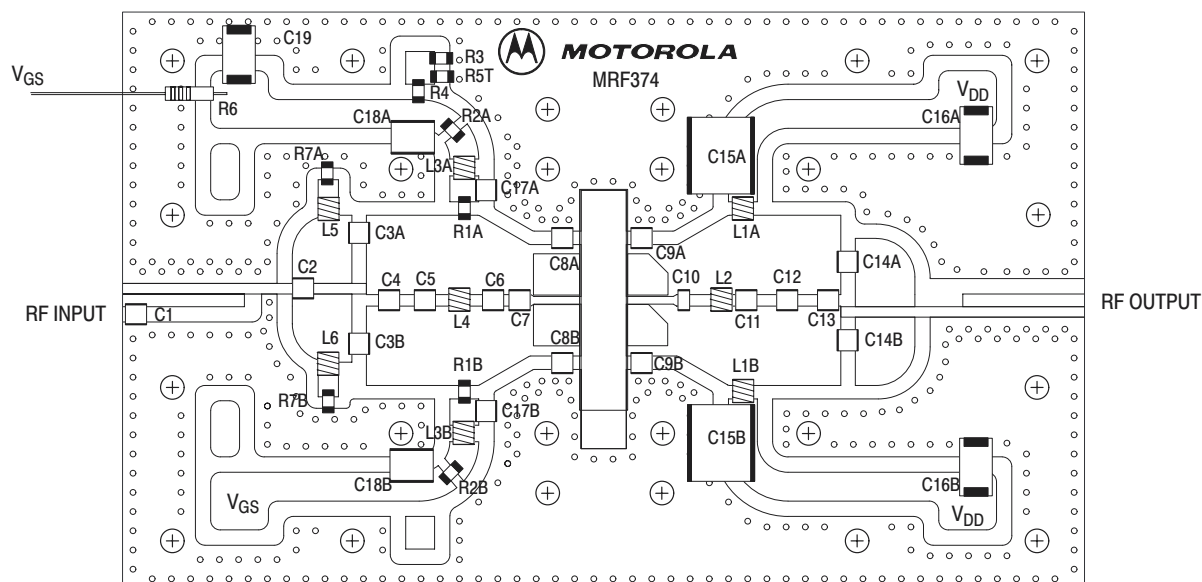


Figure 1. MRF374A Narrowband Test Circuit Component Layout

Freescale Semiconductor, Inc.

Table 1. MRF374A Narrowband Test Circuit Component Layout Designations and Values

Designation	Description
C1	0.8 pF Chip Capacitor, B Case, ATC
C2	2.2 pF Chip Capacitor, B Case, ATC
C3	0.5 – 5.0 pF Variable Capacitor, Johanson Gigatrim
C4A, B, C12A, B	47 pF Chip Capacitors, B Case, ATC
C5	1.0 pF Chip Capacitor, B Case, ATC
C6	10 pF Chip Capacitor, B Case, ATC
C7A, B, C14A, B	100,000 pF Chip Capacitors, B Case, ATC
C9A, B	15 pF Chip Capacitors, B Case, ATC
C10	3.9 pF Chip Capacitor, B Case, ATC
C11	5.1 pF Chip Capacitor, B Case, ATC
C13A, B	2.2 μ F, 100 V Chip Capacitors, Vishay #VJ3640Y225KXBAT
L1A, B	5.0 nH, Coilcraft #A02T
L2A, B	8.0 nH, Coilcraft #A03T
L3A, B	130.0 nH, Coilcraft #132–11SMJ
L4	8.8 nH, Coilcraft #1606–8
R1A, B	51 Ω , 1/4 W Chip Resistors, Vishay Dale (1210)
R2	10 Ω , 1/2 W Chip Resistor, Vishay Dale (2010)
R3A, B	3.3 k Ω , 1/8 W Chip Resistors, Vishay Dale (1206)
R4A, B	180 Ω , 1/4 W Chip Resistors, Vishay Dale (1210)
PCB	MRF374 Printed Circuit Board Rev 03, Rogers RO4350, Height 30 mils, $\epsilon_r = 3.48$
Balun B1A, B	Vertical 860 MHz Narrowband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, $\epsilon_r = 10.2$



Vertical Balun Mounting Detail

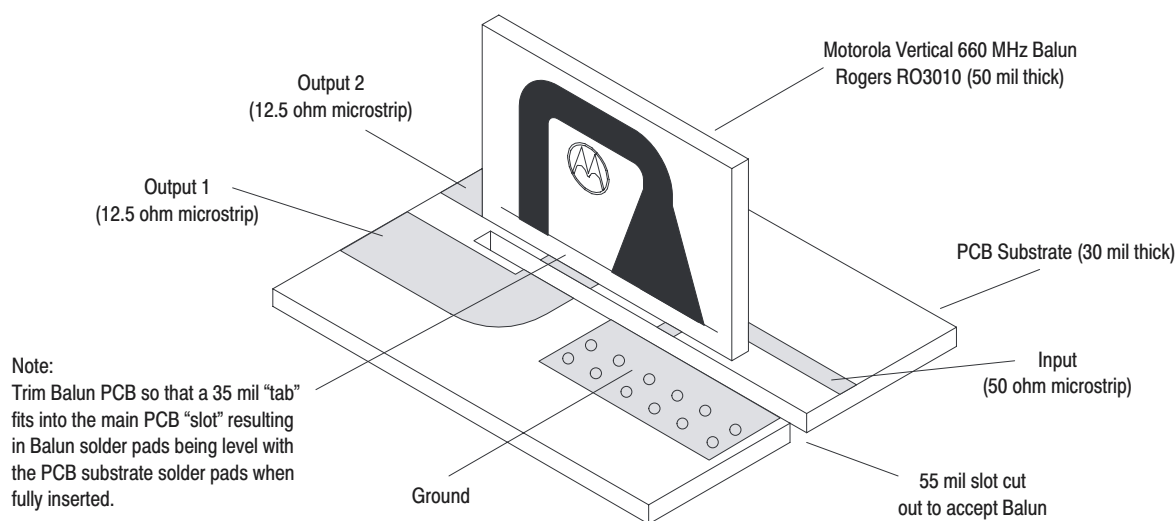


Figure 2. MRF374 Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

Table 2. MRF374 Broadband Test Circuit Component Designations and Values

Designation	Description
C1	0.8 pF Chip Capacitor, B Case, ATC
C2	8.2 pF Chip Capacitor, B Case, ATC
C3A, B, C14A, B	100 pF Chip Capacitors, B Case, ATC
C4	7.5 pF Chip Capacitor, B Case, ATC
C5	3.0 pF Chip Capacitor, B Case, ATC
C6	9.1 pF Chip Capacitor, B Case, ATC
C7	15 pF Chip Capacitor, B Case, ATC
C8A, B	12 pF Chip Capacitors, B Case, ATC
C9A, B	4.7 pF Chip Capacitors, B Case, ATC
C10	10 pF Chip Capacitor, B Case, ATC
C11	3.6 pF Chip Capacitor, B Case, ATC
C12	3.0 pF Chip Capacitor, B Case, ATC
C13	2.7 pF Chip Capacitor, B Case, ATC
C15A, B	3.3 μ F, 100 V Chip Capacitors, Vitramon #VJ3640Y335KXBAT
C16A, B	22 μ F, 35 V Chip Capacitors, Kemet #491D226K035AS
C17A, B	3.9 pF Chip Capacitors, B Case, ATC
C18A, B	2.2 μ F, 50 V Chip Capacitors, Vitramon #VJ2225Y225KXAAT
C19	10 μ F, 35 V Chip Capacitor, Kemet #T491D106K035AS
L1A, B, L3A, B, L4, L5	8.0 nH, Coilcraft #A03T
L2, L6	12.5 nH, Coilcraft #A04T
R1A, B	22 Ω , 1/8 W Chip Resistor, Vishay Dale (1206)
R2A, B, R7A, B	10 Ω , 1/8 W Chip Resistor, Vishay Dale (1206)
R3	390 Ω , 1/8 W Chip Resistor, Vishay Dale (1206)
R4	2.4 k Ω , 1/8 W Chip Resistor, Vishay Dale (1206)
R5T	470 Ω Thermistor, KOA SPEER MOT #0680149M01
R6	6.8 k Ω , 1/2 W Resistor (Axial Lead), Vishay Dale (2010)
PCB	MRF374 Printed Circuit Board Rev 03, Rogers RO4350, Height 30 mils, $\epsilon_r = 3.48$
Balun B1, B2	Vertical 660 MHz Broadband Balun, Printed Circuit Board Rev 01, Rogers RO3010, Height 50 mils, $\epsilon_r = 10.2$

Freescale Semiconductor, Inc.

MRF374A TYPICAL CHARACTERISTICS

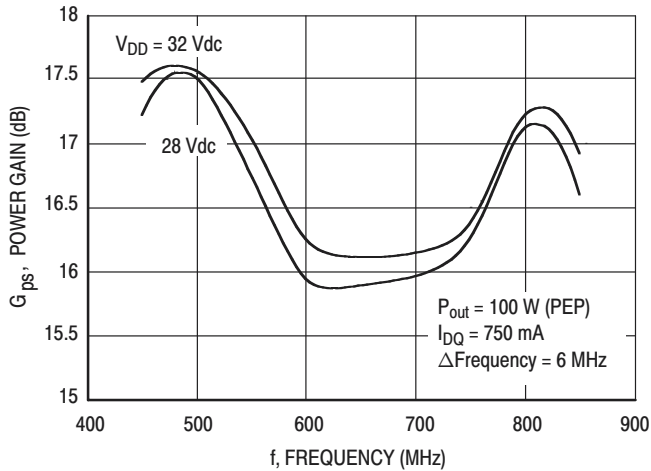


Figure 3. Gain versus Frequency in Broadband Circuit

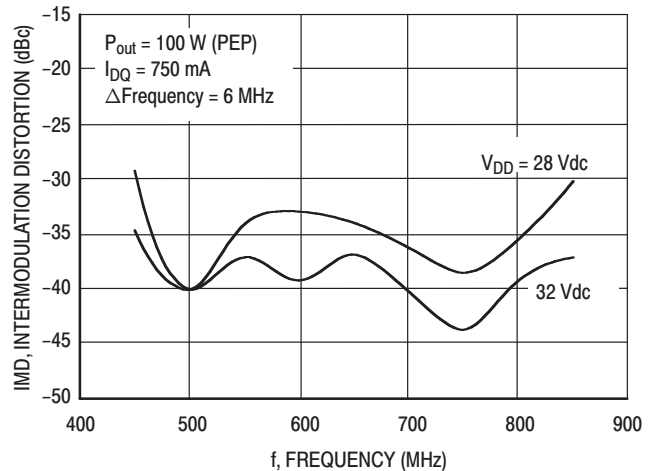


Figure 4. Intermodulation Distortion versus Frequency in Broadband Circuit

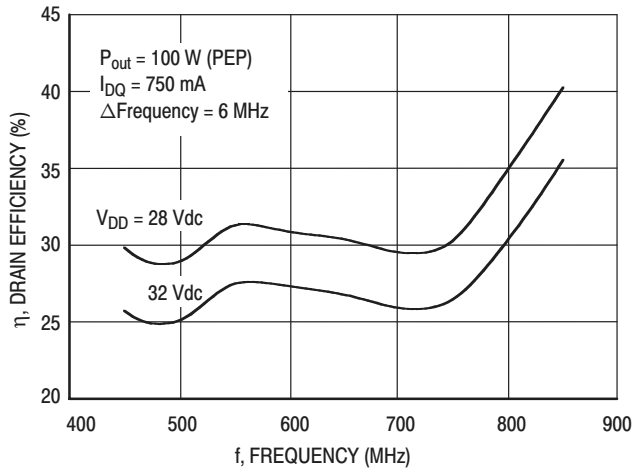


Figure 5. Drain Efficiency versus Frequency in Broadband Circuit

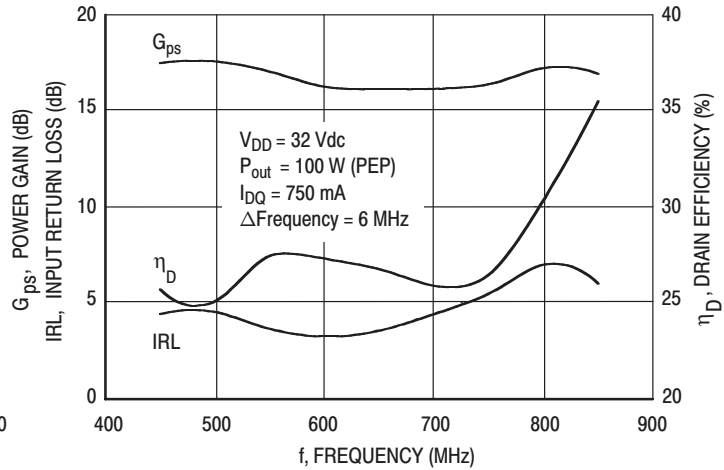


Figure 6. Performance in Broadband Circuit

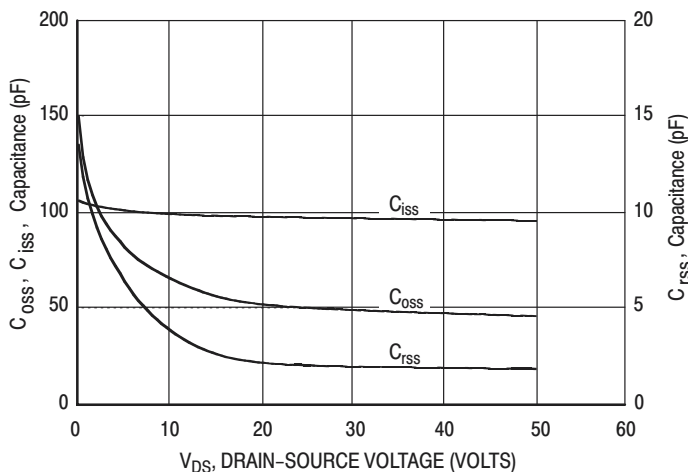


Figure 7. Capacitance versus Voltage

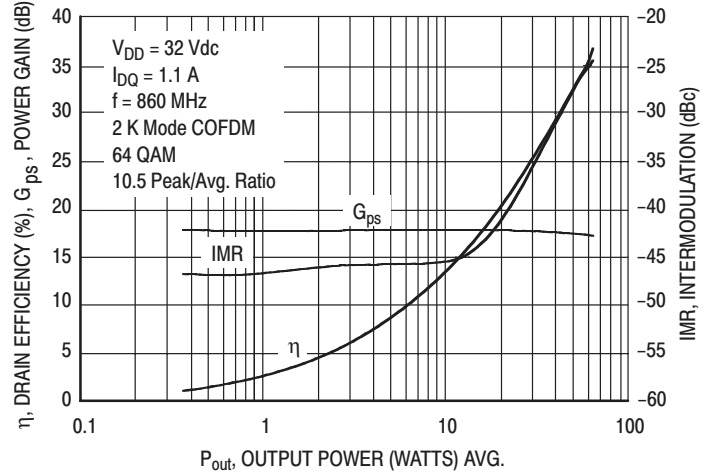


Figure 8. COFDM Intermodulation, Gain and Efficiency versus Output Power in Broadband Circuit

Freescale Semiconductor, Inc.

MRF374A TYPICAL CHARACTERISTICS

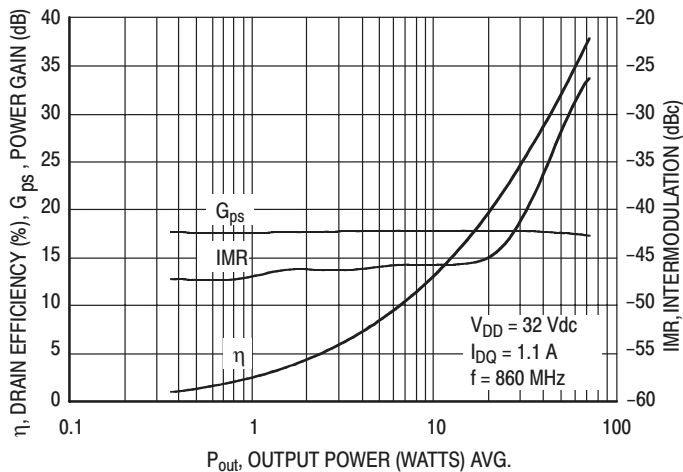


Figure 9. 8-VSB Intermodulation, Gain and Efficiency versus Output Power in Broadband Circuit

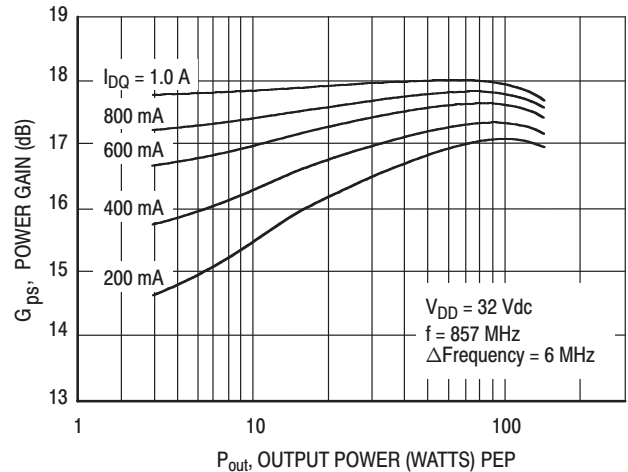


Figure 10. Power Gain versus Peak Output Power in Narrowband Circuit

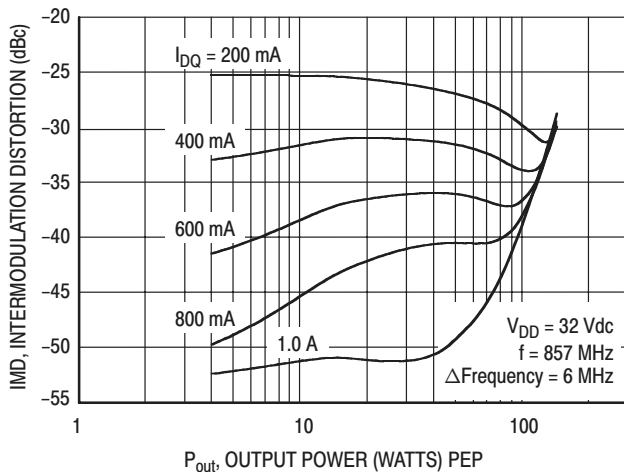


Figure 11. Intermodulation Distortion versus Peak Output Power in Narrowband Circuit

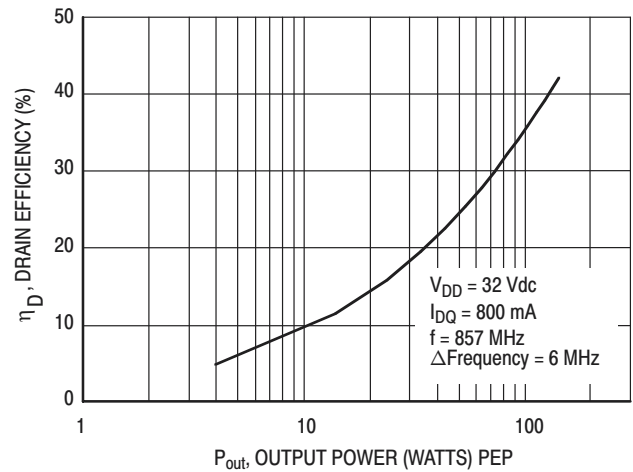


Figure 12. Drain Efficiency versus Peak Output Power in Narrowband Circuit

Freescale Semiconductor, Inc.

MRF374A TYPICAL CHARACTERISTICS

$V_{DD} = 28 \text{ Vdc}$

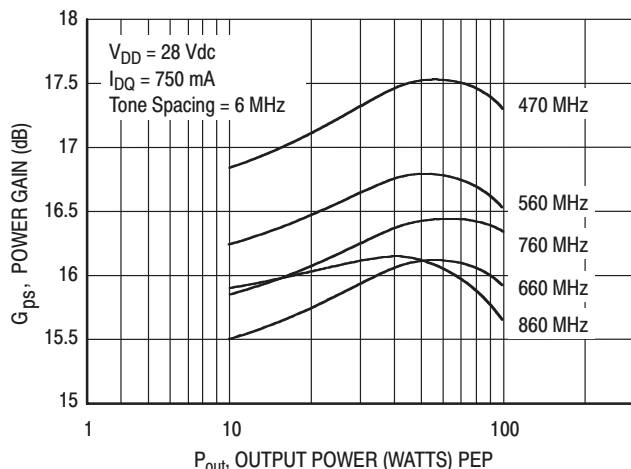


Figure 13. Power Gain versus Peak Output Power in Broadband Circuit

$V_{DD} = 32 \text{ Vdc}$

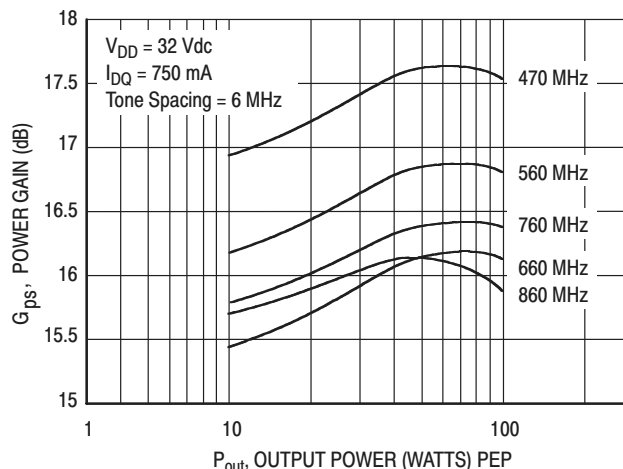


Figure 14. Power Gain versus Peak Output Power in Broadband Circuit

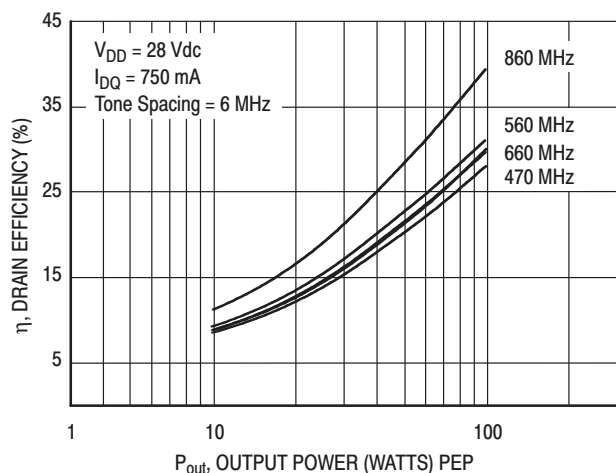


Figure 15. Drain Efficiency versus Peak Output Power in Broadband Circuit

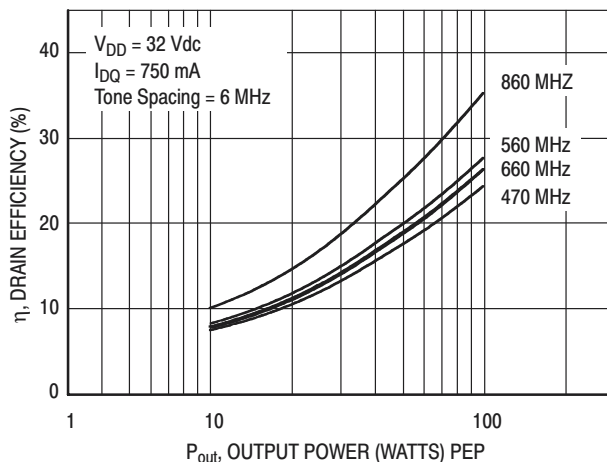


Figure 16. Drain Efficiency versus Peak Output Power in Broadband Circuit

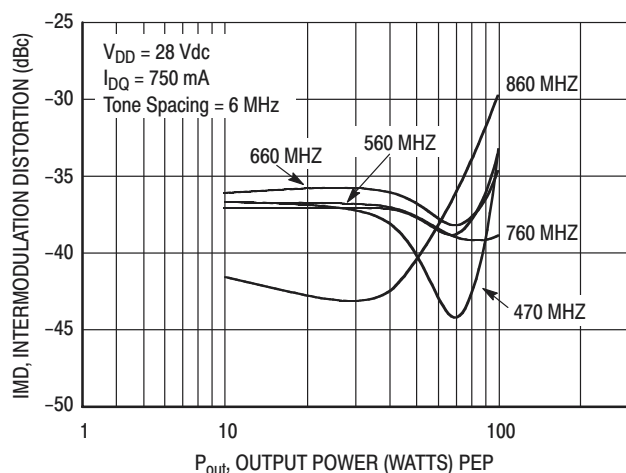


Figure 17. Intermodulation Distortion versus Peak Output Power in Broadband Circuit

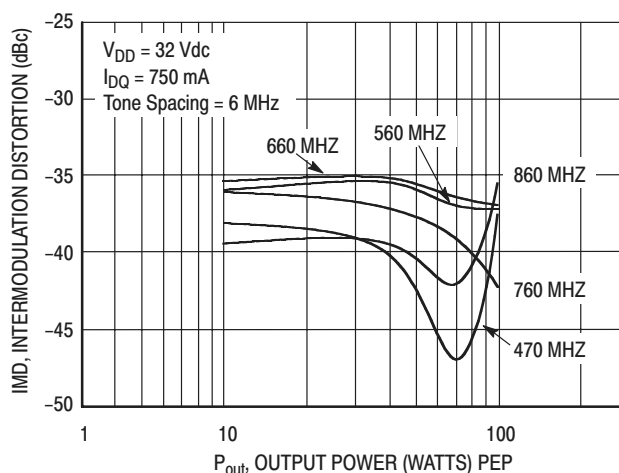
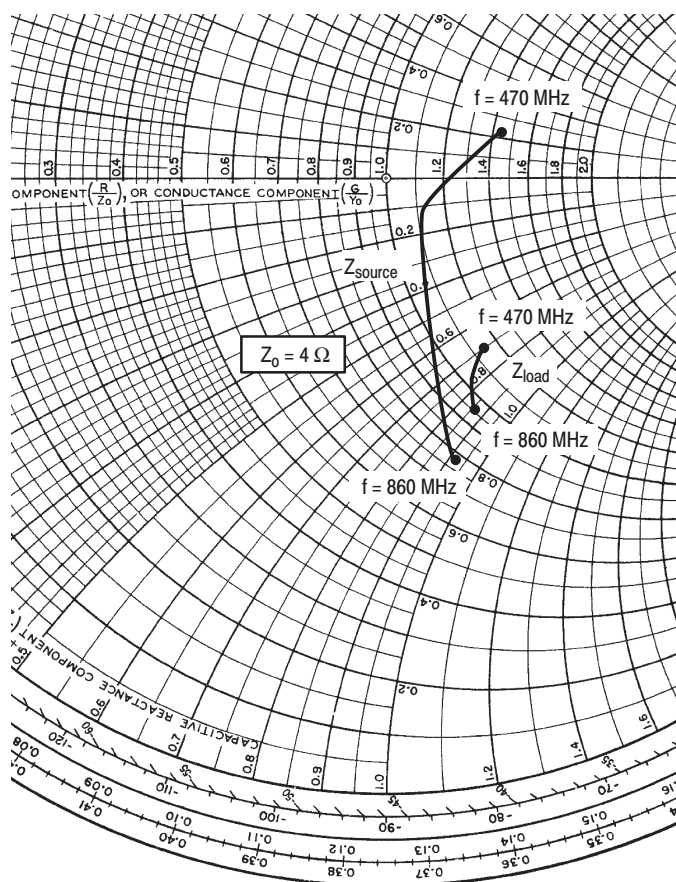


Figure 18. Intermodulation Distortion versus Peak Output Power in Broadband Circuit

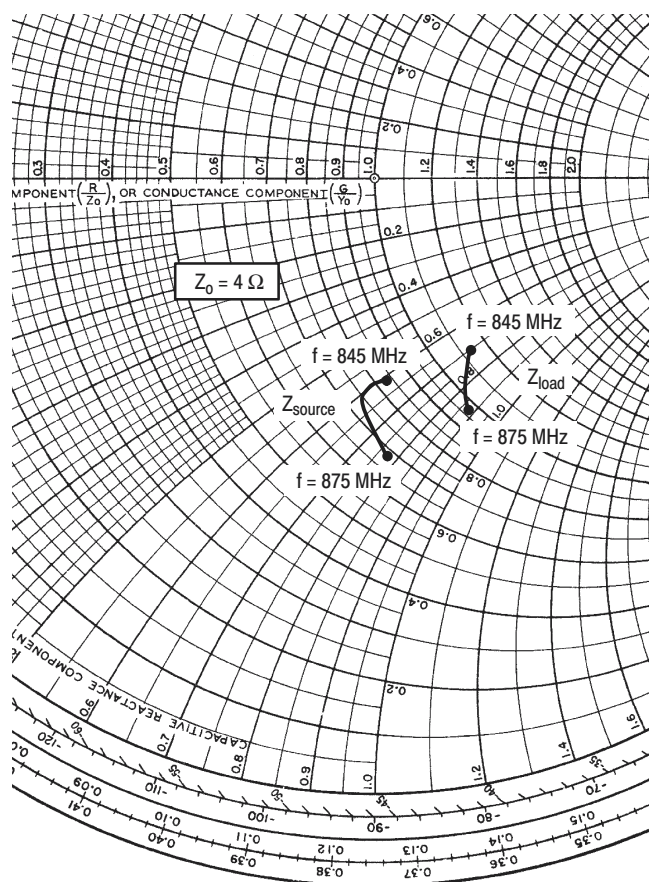
Freescale Semiconductor, Inc.



MRF374

$V_{DD} = 28 \text{ V}$, $I_{DQ} = 400 \text{ mA}$, $P_{out} = 100 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
470	$5.79 + j0.97$	$4.54 - j2.82$
660	$4.52 - j0.50$	$4.21 - j3.04$
860	$3.16 - j3.73$	$3.86 - j3.44$



MRF374A

$V_{DD} = 32 \text{ V}$, $I_{DQ} = 400 \text{ mA}$, $P_{out} = 130 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
845	$3.33 - j2.42$	$4.56 - j2.86$
860	$3.03 - j2.39$	$4.22 - j3.16$
875	$2.73 - j3.10$	$3.87 - j3.52$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

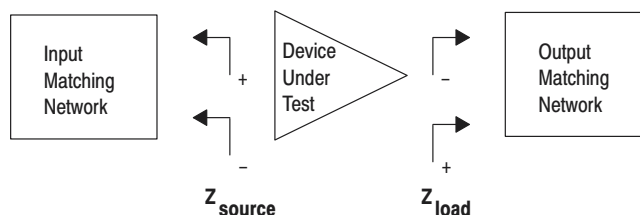


Figure 19. Series Equivalent Input and Output Impedance

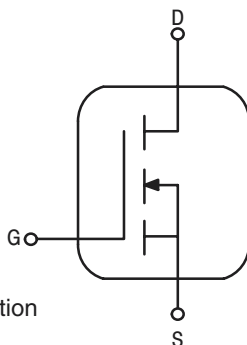
The RF MOSFET Line

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

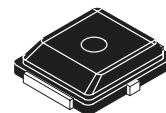
The MRF1511T1 is designed for broadband commercial and industrial applications at frequencies to 175 MHz. The high gain and broadband performance of this device makes it ideal for large-signal, common source amplifier applications in 7.5 volt portable FM equipment.

- Specified Performance @ 175 MHz, 7.5 Volts
Output Power — 8 Watts
Power Gain — 11.5 dB
Efficiency — 55%
- Capable of Handling 20:1 VSWR, @ 9.5 Vdc, 175 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- RF Power Plastic Surface Mount Package
- Available in Tape and Reel.
T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.



MRF1511T1

175 MHz, 8 W, 7.5 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 466-02, STYLE 1
(PLD-1.5)
PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	4	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ (1) Derate above 25°C	P_D	62.5 0.5	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	$^\circ\text{C/W}$

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Current (V _{DS} = 35 Vdc, V _{GS} = 0)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 10 Vdc, V _{DS} = 0)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 7.5 Vdc, I _D = 170 μA)	V _{GS(th)}	1.0	1.6	2.1	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.4	—	Vdc

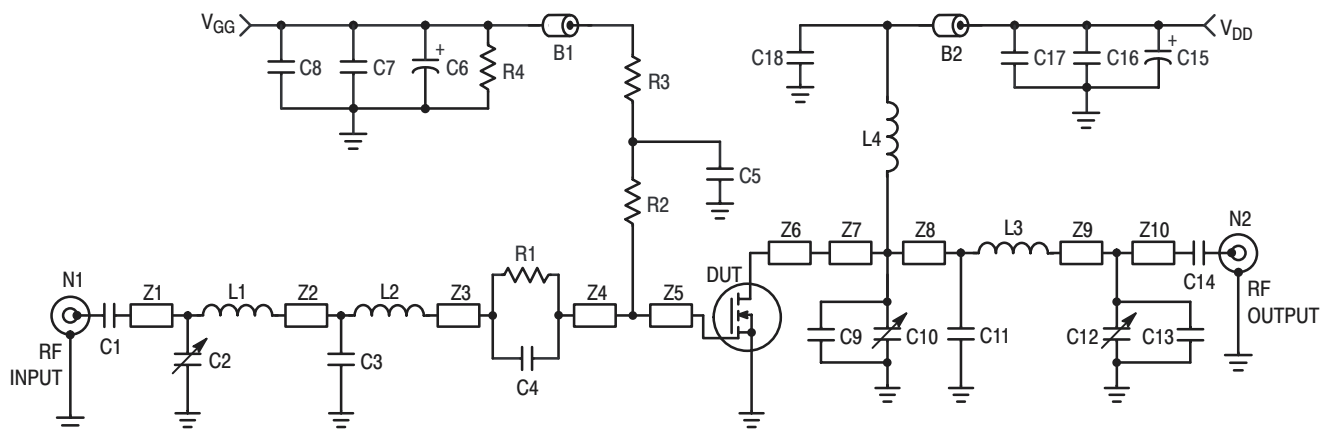
DYNAMIC CHARACTERISTICS

Input Capacitance (V _{DS} = 7.5 Vdc, V _{GS} = 0, f = 1 MHz)	C _{iss}	—	100	—	pF
Output Capacitance (V _{DS} = 7.5 Vdc, V _{GS} = 0, f = 1 MHz)	C _{oss}	—	53	—	pF
Reverse Transfer Capacitance (V _{DS} = 7.5 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	8	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain (V _{DD} = 7.5 Vdc, P _{out} = 8 Watts, I _{DQ} = 150 mA, f = 175 MHz)	G _{ps}	10	11.5	—	dB
Drain Efficiency (V _{DD} = 7.5 Vdc, P _{out} = 8 Watts, I _{DQ} = 150 mA, f = 175 MHz)	η	50	55	—	%

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	R1	15 Ω , 0805 Chip Resistor
C1, C5, C18	120 pF, 100 mil Chip Capacitor	R2	1.0 k Ω , 1/8 W Resistor
C2, C10, C12	0 to 20 pF, Trimmer Capacitor	R3	1.0 k Ω , 0805 Chip Resistor
C3	33 pF, 100 mil Chip Capacitor	R4	33 k Ω , 1/8 W Resistor
C4	68 pF, 100 mil Chip Capacitor	Z1	0.200" x 0.080" Microstrip
C6, C15	10 μ F, 50 V Electrolytic Capacitor	Z2	0.755" x 0.080" Microstrip
C7, C16	1,200 pF, 100 mil Chip Capacitor	Z3	0.300" x 0.080" Microstrip
C8, C17	0.1 μ F, 100 mil Chip Capacitor	Z4	0.065" x 0.080" Microstrip
C9	150 pF, 100 mil Chip Capacitor	Z5, Z6	0.260" x 0.223" Microstrip
C11	43 pF, 100 mil Chip Capacitor	Z7	0.095" x 0.080" Microstrip
C13	24 pF, 100 mil Chip Capacitor	Z8	0.418" x 0.080" Microstrip
C14	300 pF, 100 mil Chip Capacitor	Z9	1.057" x 0.080" Microstrip
L1, L3	12.5 nH, A04T, Coilcraft	Z10	0.120" x 0.080" Microstrip
L2	26 nH, 4 Turn, Coilcraft	Board	Glass Teflon [®] , 31 mils, 2 oz. Copper
L4	55.5 nH, 5 Turn, Coilcraft		
N1, N2	Type N Flange Mount		

Figure 1. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

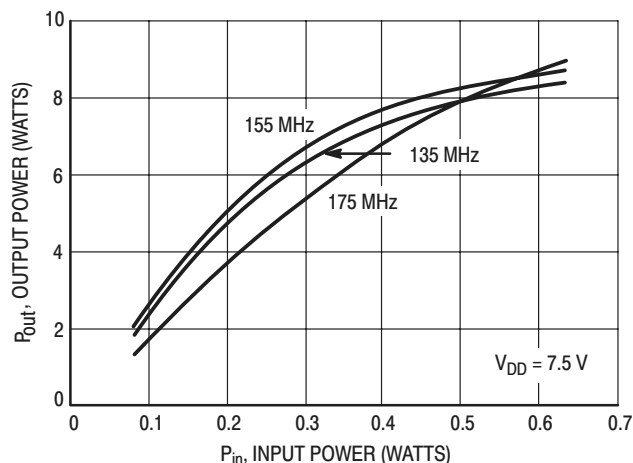


Figure 2. Output Power versus Input Power

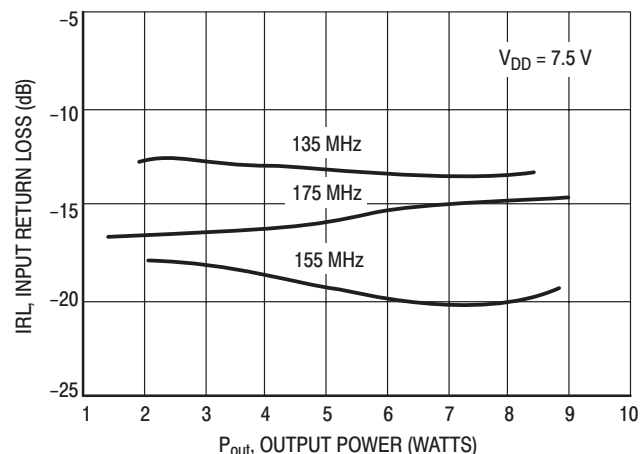


Figure 3. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 135 – 175 MHz

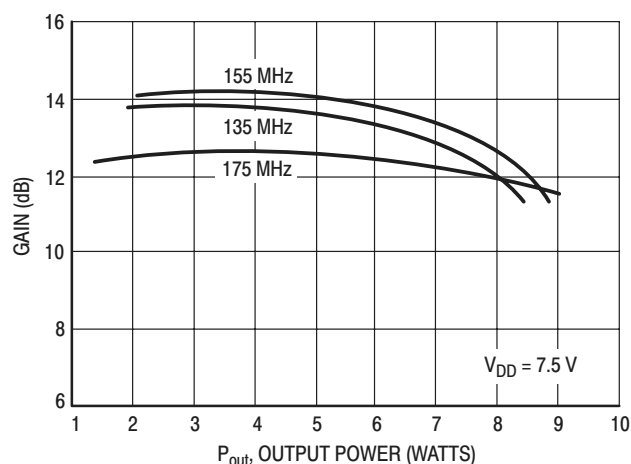


Figure 4. Gain versus Output Power

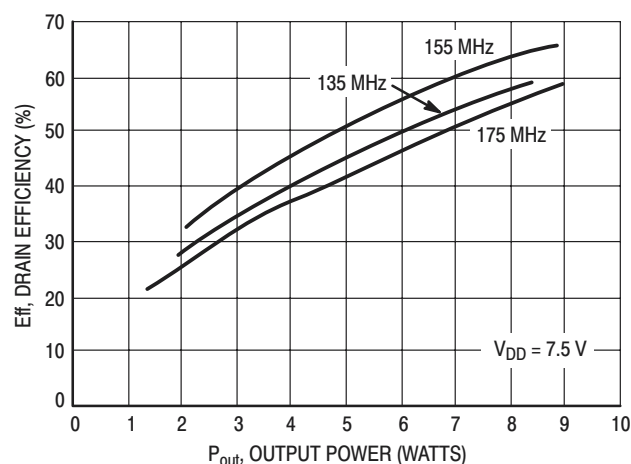


Figure 5. Drain Efficiency versus Output Power

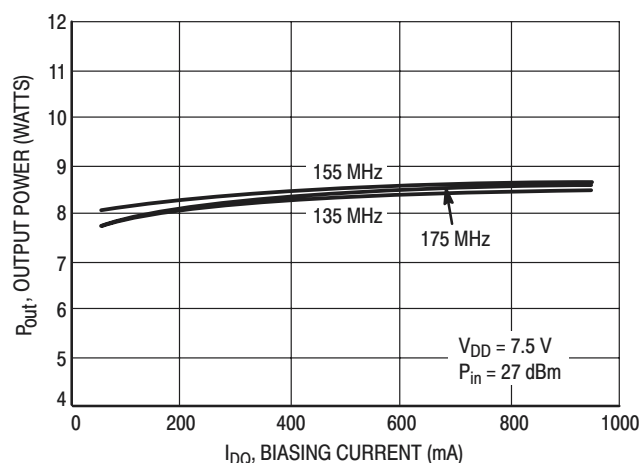


Figure 6. Output Power versus Biasing Current

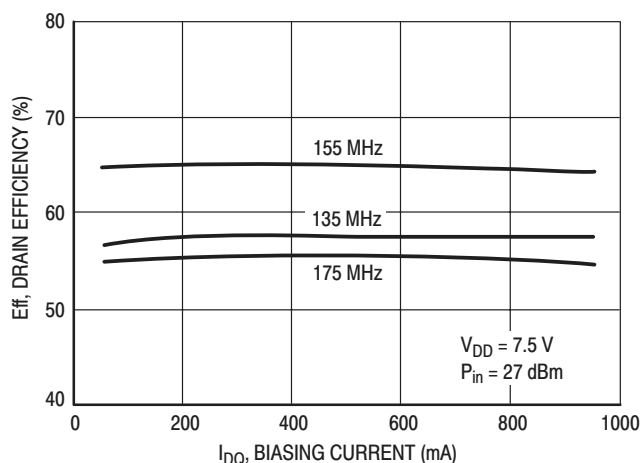


Figure 7. Drain Efficiency versus Biasing Current

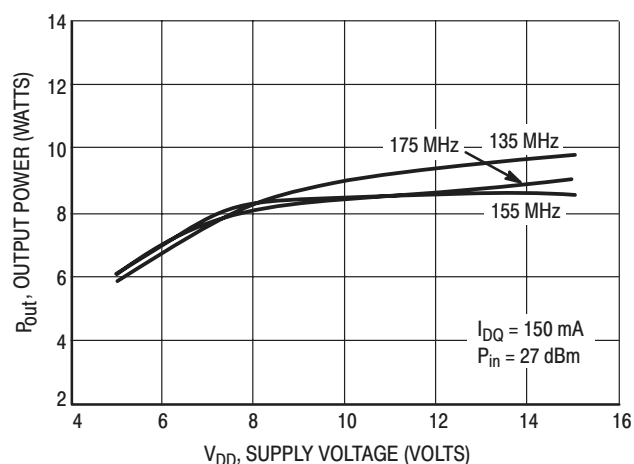


Figure 8. Output Power versus Supply Voltage

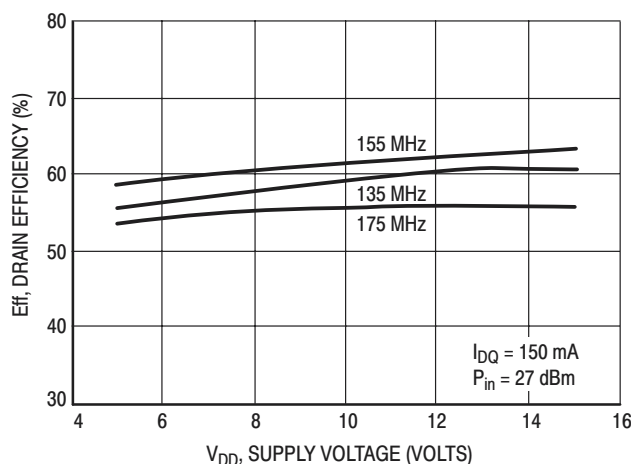
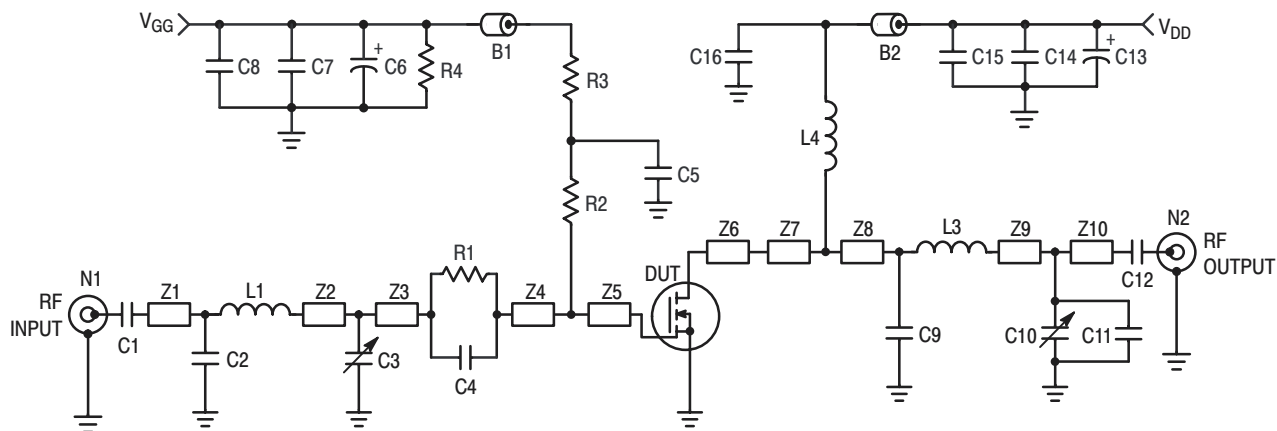


Figure 9. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)
C1, C12	330 pF, 100 mil Chip Capacitor
C2	43 pF, 100 mil Chip Capacitor
C3, C10	0 to 20 pF, Trimmer Capacitor
C4	24 pF, 100 mil Chip Capacitor
C5, C16	120 pF, 100 mil Chip Capacitor
C6, C13	10 μ F, 50 V Electrolytic Capacitor
C7, C14	1,200 pF, 100 mil Chip Capacitor
C8, C15	0.1 μ F, 100 mil Chip Capacitor
C9	380 pF, 100 mil Chip Capacitor
C11	75 pF, 100 mil Chip Capacitor
L1	82 nH, Coilcraft
L2	55.5 nH, 5 Turn, Coilcraft
L3	39 nH, 6 Turn, Coilcraft

N1, N2	Type N Flange Mount
R1	15 Ω , 0805 Chip Resistor
R2	51 Ω , 1/2 W Resistor
R3	100 Ω , 0805 Chip Resistor
R4	33 k Ω , 1/8 W Resistor
Z1	0.136" x 0.080" Microstrip
Z2	0.242" x 0.080" Microstrip
Z3	1.032" x 0.080" Microstrip
Z4	0.145" x 0.080" Microstrip
Z5, Z6	0.260" x 0.223" Microstrip
Z7	0.134" x 0.080" Microstrip
Z8	0.490" x 0.080" Microstrip
Z9	0.872" x 0.080" Microstrip
Z10	0.206" x 0.080" Microstrip
Board	Glass Teflon [®] , 31 mils, 2 oz. Copper

Figure 10. 66 – 88 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 66 – 88 MHz

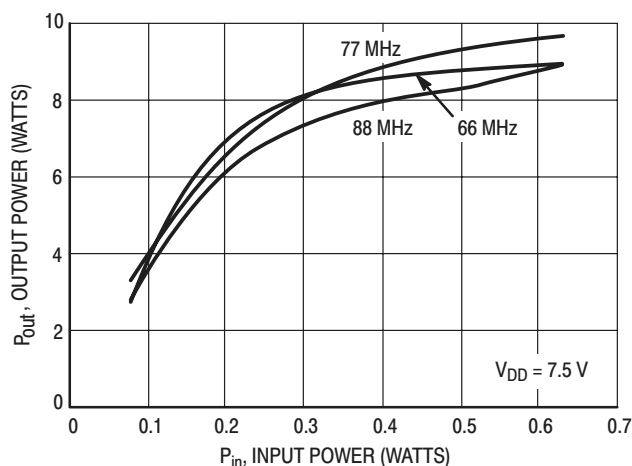


Figure 11. Output Power versus Input Power

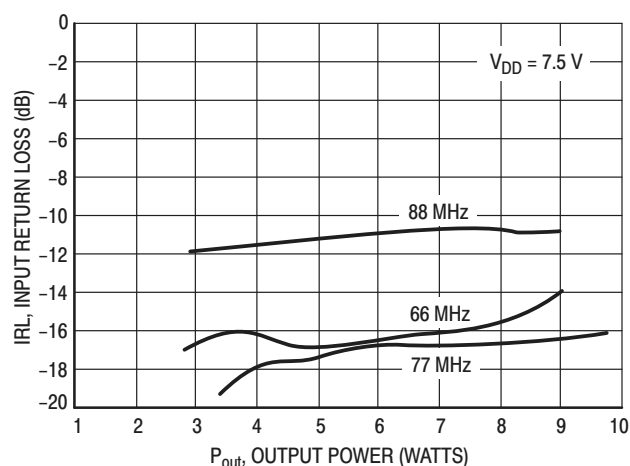


Figure 12. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 66 – 88 MHz

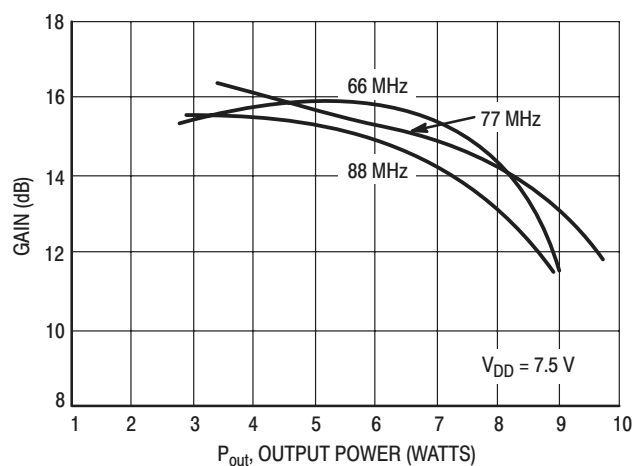


Figure 13. Gain versus Output Power

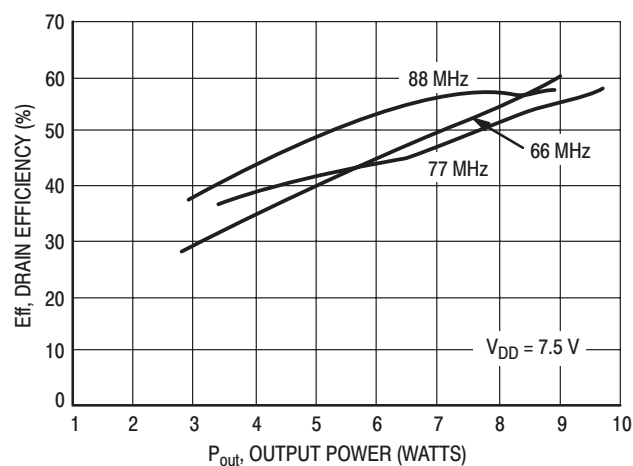


Figure 14. Drain Efficiency versus Output Power

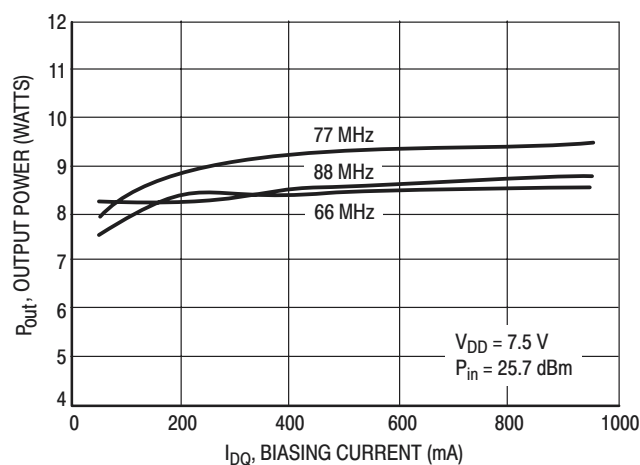


Figure 15. Output Power versus Biasing Current

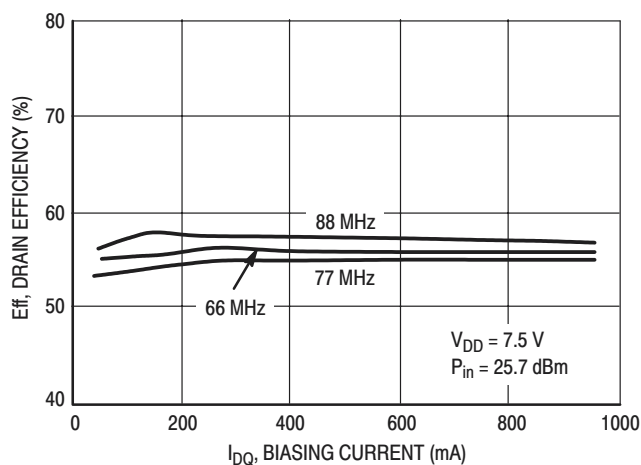


Figure 16. Drain Efficiency versus Biasing Current

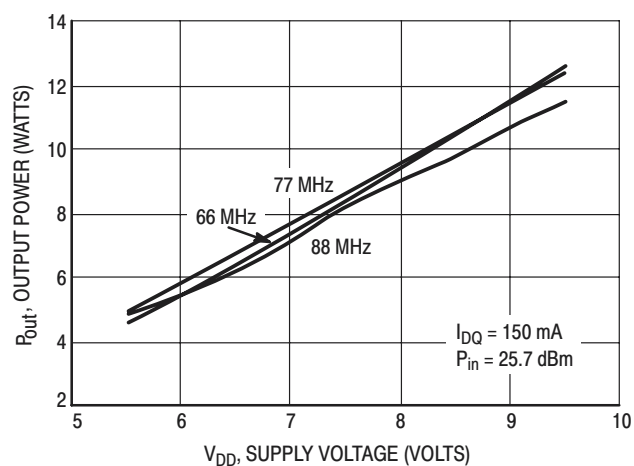


Figure 17. Output Power versus Supply Voltage

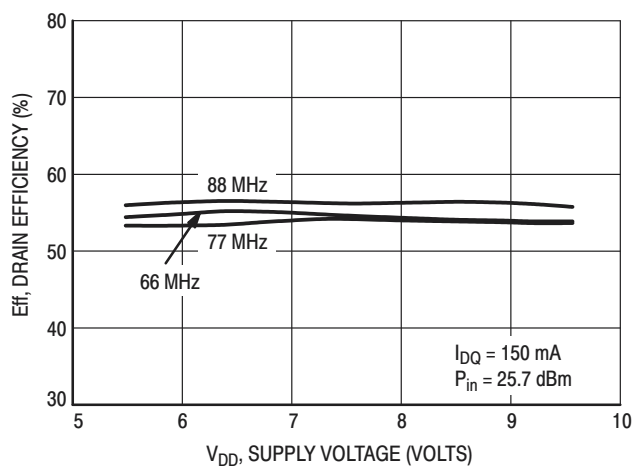
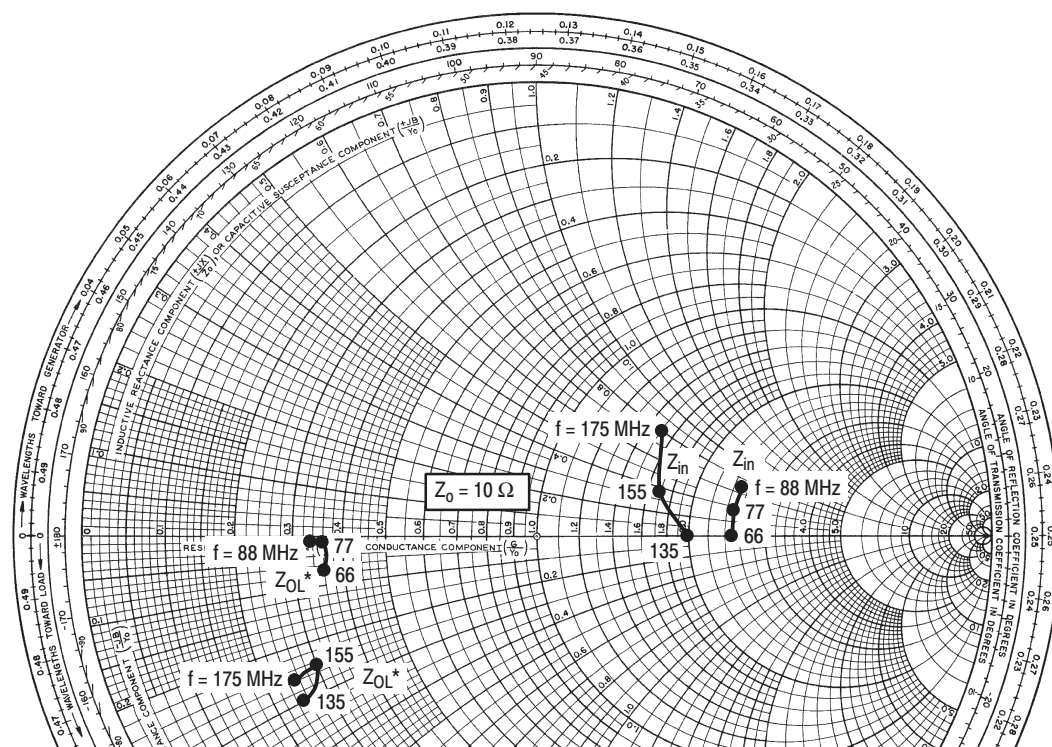


Figure 18. Drain Efficiency versus Supply Voltage



$V_{DD} = 7.5 \text{ V}$, $I_{DQ} = 150 \text{ mA}$, $P_{out} = 8 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
135	$20.1 - j0.5$	$2.53 - j2.61$
155	$17.0 + j3.6$	$3.01 - j2.48$
175	$15.2 + j7.9$	$2.52 - j3.02$

Z_{in} = Complex conjugate of source impedance with parallel 15Ω resistor and 68 pF capacitor in series with gate. (See Figure 1).

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

$V_{DD} = 7.5 \text{ V}$, $I_{DQ} = 150 \text{ mA}$, $P_{out} = 8 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
66	$25.3 - j0.31$	$3.62 - j0.751$
77	$25.6 + j3.62$	$3.59 - j0.129$
88	$26.7 + j6.79$	$3.37 - j0.173$

Z_{in} = Complex conjugate of source impedance with parallel 15Ω resistor and 24 pF capacitor in series with gate. (See Figure 10).

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

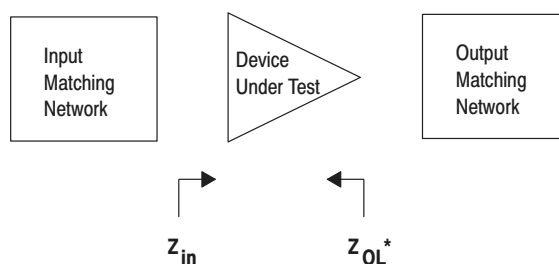


Figure 19. Series Equivalent Input and Output Impedance

Freescale Semiconductor, Inc.

Table 1. Common Source Scattering Parameters ($V_{DD} = 7.5$ Vdc)

$I_{DQ} = 150$ mA

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
30	0.88	-165	18.92	95	0.015	8	0.84	-169
50	0.88	-171	11.47	91	0.016	-5	0.84	-173
100	0.87	-175	5.66	85	0.016	-7	0.84	-176
150	0.87	-176	3.75	82	0.015	-5	0.85	-176
200	0.87	-177	2.78	78	0.014	-6	0.84	-176
250	0.87	-177	2.16	75	0.014	-10	0.85	-176
300	0.88	-177	1.77	72	0.012	-17	0.86	-176
350	0.88	-177	1.49	69	0.013	-11	0.86	-176
400	0.88	-177	1.26	66	0.013	-17	0.87	-175
450	0.88	-177	1.08	64	0.011	-20	0.87	-175
500	0.89	-176	0.96	63	0.012	-20	0.88	-175

$I_{DQ} = 800$ mA

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
30	0.89	-166	18.89	95	0.014	10	0.85	-170
50	0.88	-172	11.44	91	0.015	8	0.84	-174
100	0.87	-175	5.65	86	0.016	-2	0.85	-176
150	0.87	-177	3.74	82	0.014	-8	0.84	-177
200	0.87	-177	2.78	78	0.013	-18	0.85	-177
250	0.88	-177	2.16	75	0.012	-11	0.85	-176
300	0.88	-177	1.77	73	0.015	-15	0.86	-176
350	0.88	-177	1.50	70	0.009	-7	0.87	-176
400	0.88	-177	1.26	67	0.012	-3	0.87	-176
450	0.88	-177	1.09	65	0.012	-18	0.87	-175
500	0.89	-177	0.97	64	0.009	-10	0.88	-175

$I_{DQ} = 1.5$ A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
30	0.90	-168	17.89	95	0.013	2	0.86	-172
50	0.89	-173	10.76	91	0.013	3	0.86	-175
100	0.88	-176	5.32	86	0.014	-19	0.86	-177
150	0.88	-177	3.53	83	0.013	-6	0.86	-177
200	0.88	-177	2.63	80	0.011	-4	0.86	-177
250	0.88	-178	2.05	77	0.012	-14	0.86	-177
300	0.88	-177	1.69	75	0.013	-2	0.87	-177
350	0.89	-177	1.43	72	0.010	-9	0.87	-176
400	0.89	-177	1.22	70	0.014	-3	0.88	-176
450	0.89	-177	1.06	68	0.011	-8	0.88	-176
500	0.89	-177	0.94	67	0.011	-15	0.88	-176

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

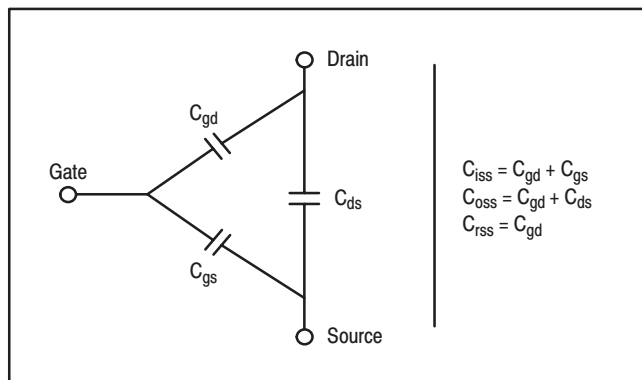
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high — on the order of $10^9 \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at $I_{DQ} = 150 \text{ mA}$, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065" x 0.180" source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal

impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device's S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

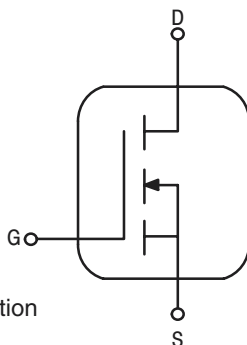
The RF MOSFET Line

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

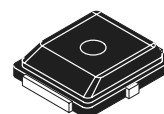
The MRF1513T1 is designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common source amplifier applications in 7.5 volt portable and 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts
 - Output Power — 3 Watts
 - Power Gain — 11 dB
 - Efficiency — 55%
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 520 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- In Tape and Reel. T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.



MRF1513T1

520 MHz, 3 W, 12.5 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 466-02, STYLE 1
PLD-1.5
PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	2	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ (1) Derate above 25°C	P_D	31.25 0.25	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4	$^\circ\text{C/W}$

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Current ($V_{DS} = 40\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μA_{dc}
Gate–Source Leakage Current ($V_{GS} = 10\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μA_{dc}

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = 12.5\text{ Vdc}$, $I_D = 60\text{ }\mu\text{A}$)	$V_{GS(th)}$	1.0	1.7	2.1	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 500\text{ mAdc}$)	$V_{DS(on)}$	—	0.65	—	Vdc

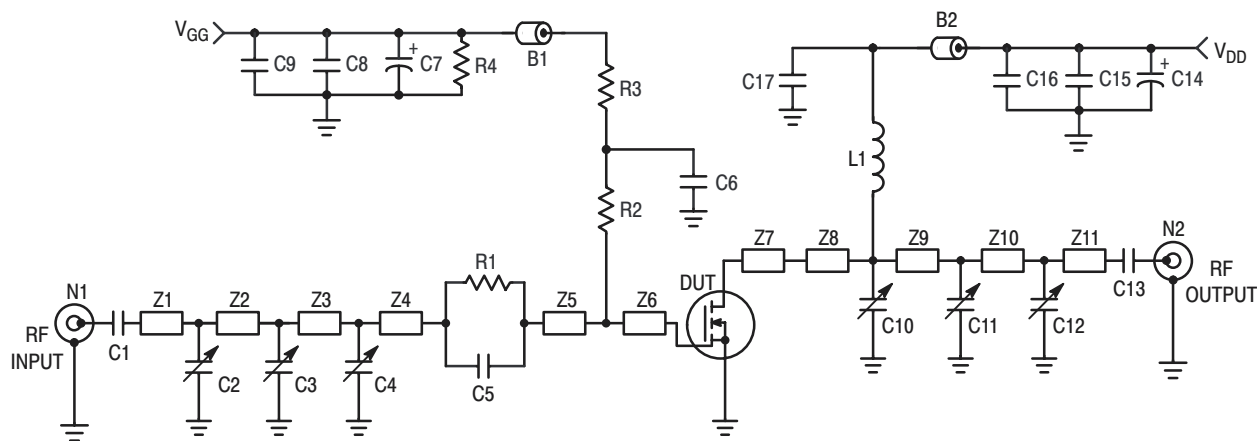
DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	33	—	pF
Output Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{oss}	—	16.5	—	pF
Reverse Transfer Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	2.2	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 3\text{ Watts}$, $I_{DQ} = 50\text{ mA}$, $f = 520\text{ MHz}$)	G_{ps}	10	11	—	dB
Drain Efficiency ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 3\text{ Watts}$, $I_{DQ} = 50\text{ mA}$, $f = 520\text{ MHz}$)	η	50	55	—	%

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Beads, Fair Rite Products #2743021446	R4	33 k Ω , 1/8 W Resistor
C1, C13	240 pF, 100 mil Chip Capacitors	Z1	0.236" x 0.080" Microstrip
C2, C3, C4, C10,	0 to 20 pF Trimmer Capacitors	Z2	0.981" x 0.080" Microstrip
C11, C12	120 pF, 100 mil Chip Capacitors	Z3	0.240" x 0.080" Microstrip
C5, C6, C17	10 μ F, 50 V Electrolytic Capacitors	Z4	0.098" x 0.080" Microstrip
C7, C14	1,200 pF, 100 mil Chip Capacitors	Z5	0.192" x 0.080" Microstrip
C8, C15	0.1 μ F, 100 mil Chip Capacitors	Z6, Z7	0.260" x 0.223" Microstrip
C9, C16	55.5 nH, 5 Turn, Coilcraft	Z8	0.705" x 0.080" Microstrip
L1	Type N Flange Mounts	Z9	0.342" x 0.080" Microstrip
N1, N2	15 Ω Chip Resistors (0805)	Z10	0.347" x 0.080" Microstrip
R1, R3	1 k Ω , 1/8 W Resistor	Z11	0.846" x 0.080" Microstrip
R2		Board	Glass Teflon [®] , 31 mils, 2 oz. Copper

Figure 1. 450 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 – 520 MHz

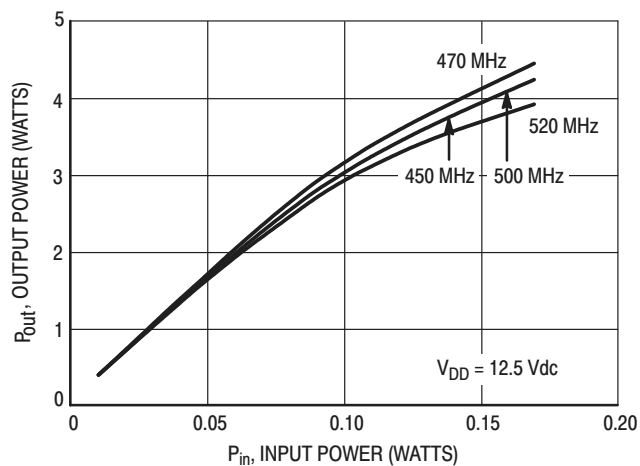


Figure 2. Output Power versus Input Power

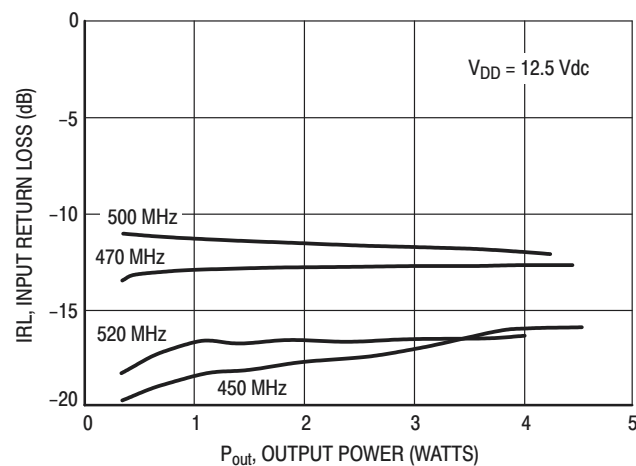


Figure 3. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 450 – 520 MHz

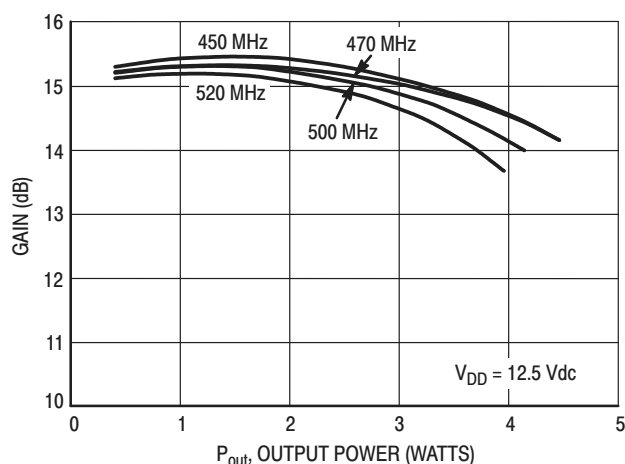


Figure 4. Gain versus Output Power

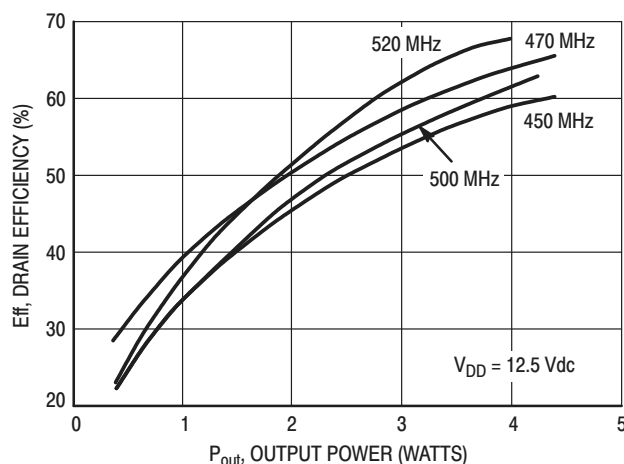


Figure 5. Drain Efficiency versus Output Power

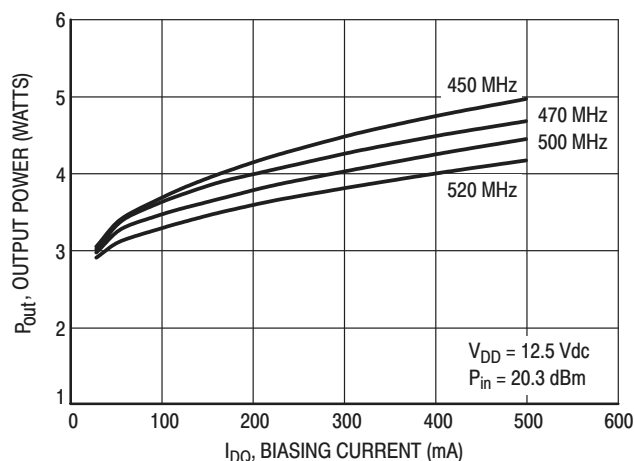


Figure 6. Output Power versus Biasing Current

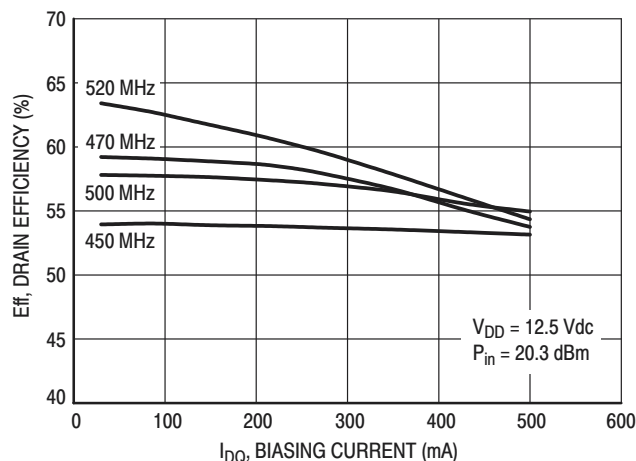


Figure 7. Drain Efficiency versus Biasing Current

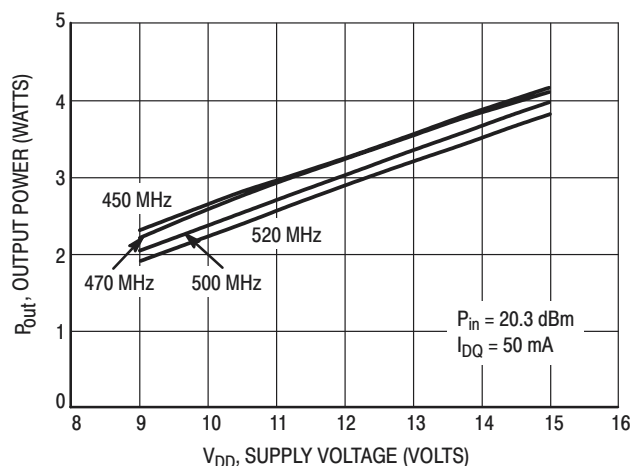


Figure 8. Output Power versus Supply Voltage

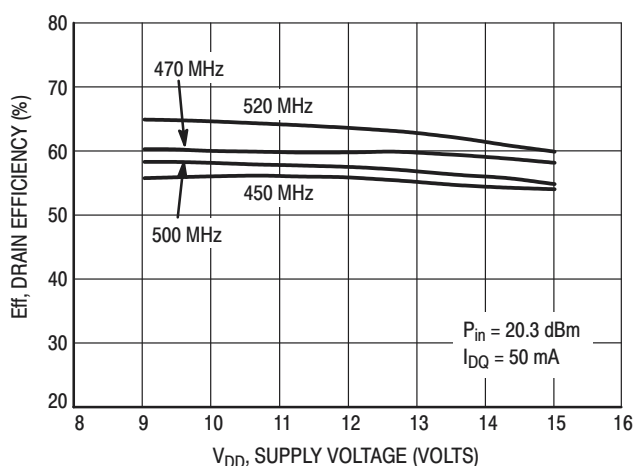
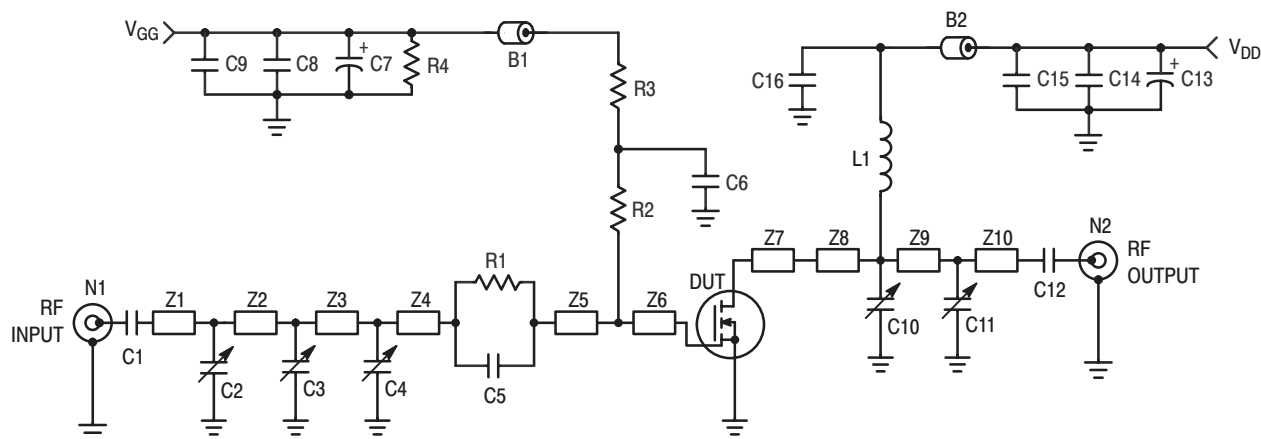


Figure 9. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Bead, Fair Rite Products #2743021446	R3	15 Ω Chip Resistor (0805)
C1, C12	330 pF, 100 mil Chip Capacitors	R4	33 k Ω , 1/8 W Resistor
C2, C3, C4,		Z1	0.253" x 0.080" Microstrip
C10, C11	1 to 20 pF Trimmer Capacitors	Z2	0.958" x 0.080" Microstrip
C5, C6, C16	120 pF, 100 mil Chip Capacitors	Z3	0.247" x 0.080" Microstrip
C7, C13	10 μ F, 50 V Electrolytic Capacitors	Z4	0.193" x 0.080" Microstrip
C8, C14	1,200 pF, 100 mil Chip Capacitors	Z5	0.132" x 0.080" Microstrip
C9, C15	0.1 μ F, 100 mil Chip Capacitors	Z6, Z7	0.260" x 0.223" Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z8	0.494" x 0.080" Microstrip
N1, N2	Type N Flange Mounts	Z9	0.941" x 0.080" Microstrip
R1	15 Ω Chip Resistor (0805)	Z10	0.452" x 0.080" Microstrip
R2	1 k Ω , 1/8 W Resistor	Board	Glass Teflon [®] , 31 mils, 2 oz. Copper

Figure 10. 400 – 470 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 400 – 470 MHz

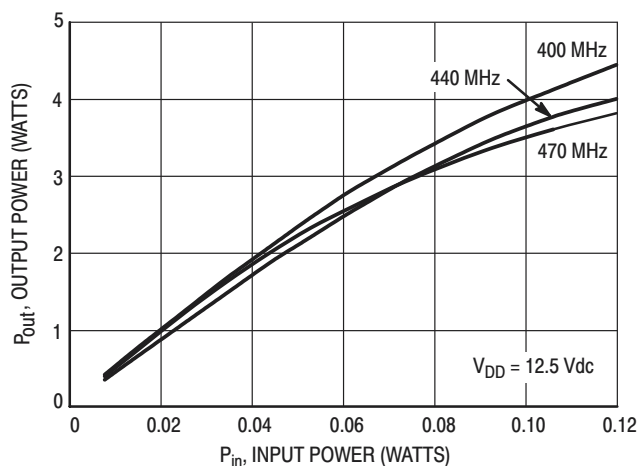


Figure 11. Output Power versus Input Power

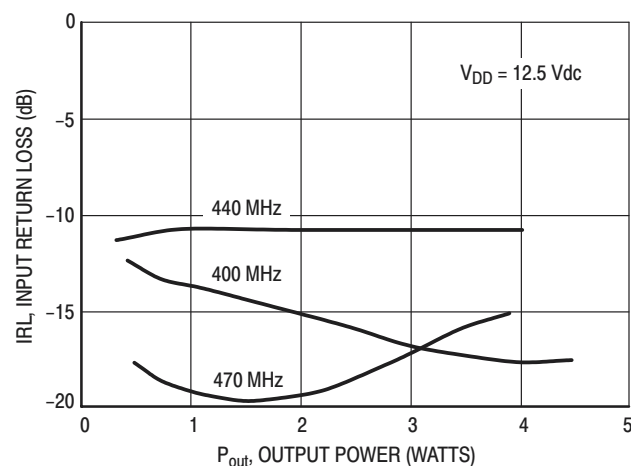


Figure 12. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 400 – 470 MHz

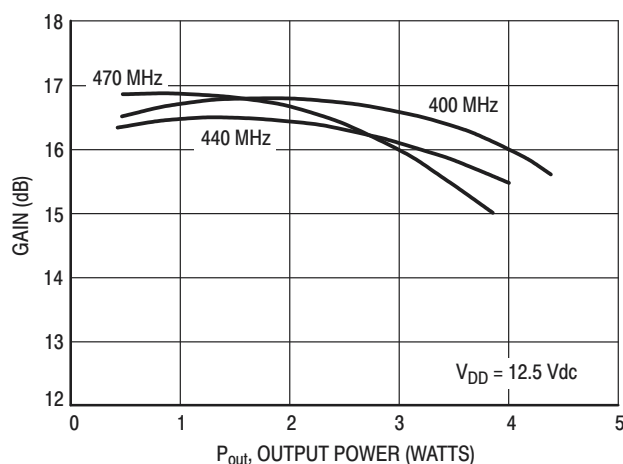


Figure 13. Gain versus Output Power

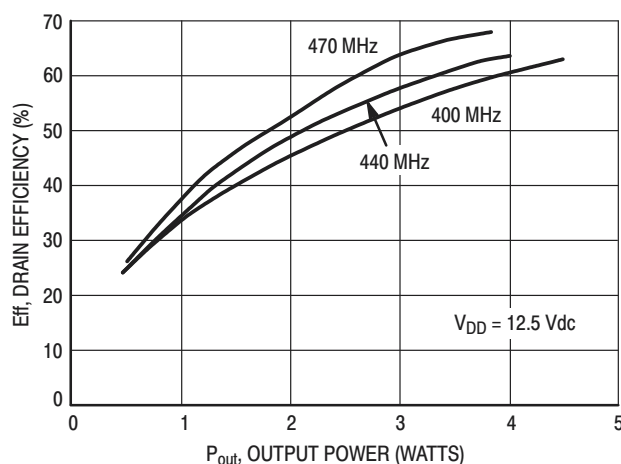


Figure 14. Drain Efficiency versus Output Power

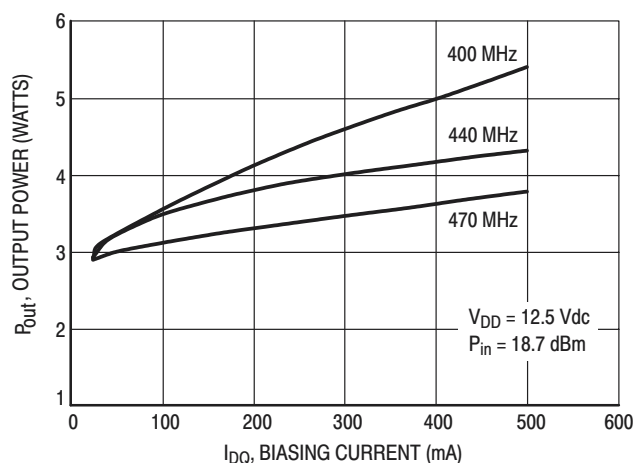


Figure 15. Output Power versus Biasing Current

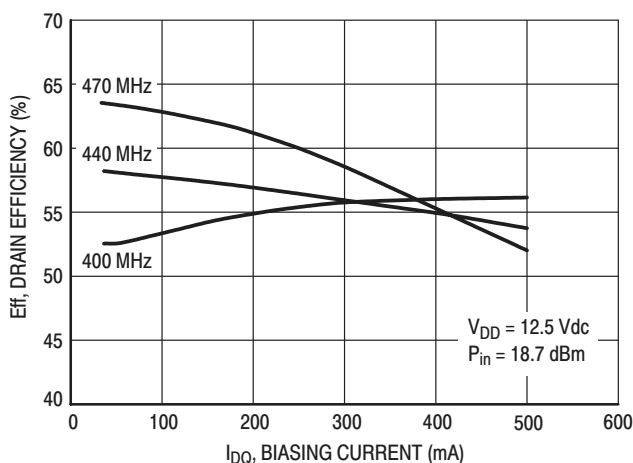


Figure 16. Drain Efficiency versus Biasing Current

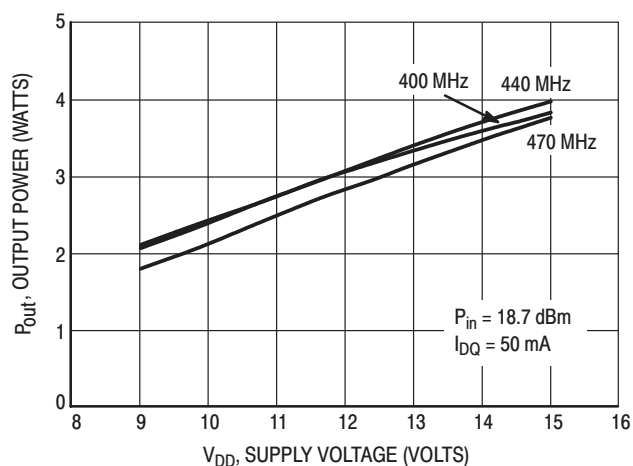


Figure 17. Output Power versus Supply Voltage

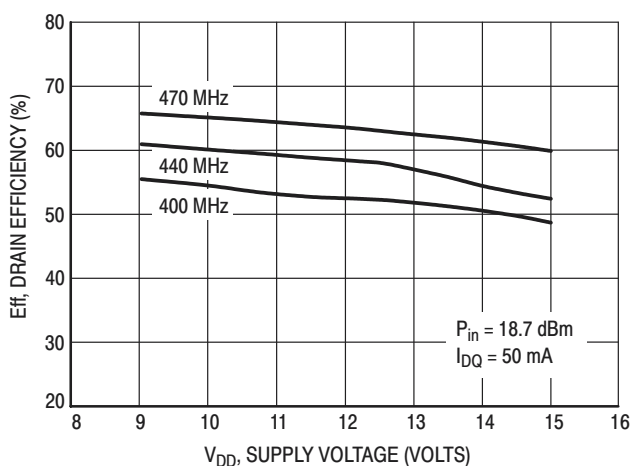
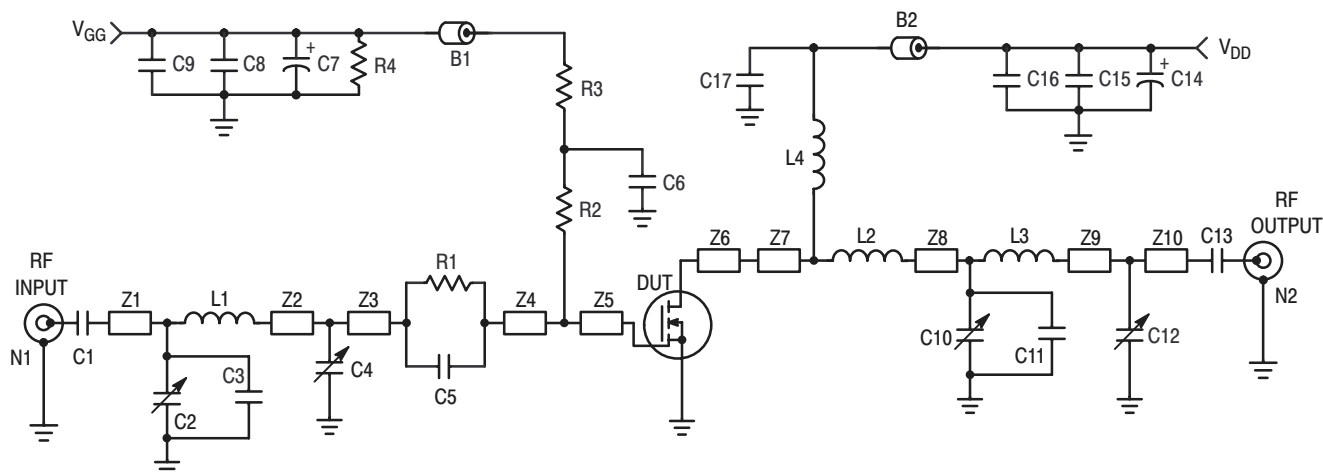


Figure 18. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Beads, Fair Rite Products #2743021446	L4	33 nH, 5 Turn, Coilcraft
C1, C13	330 pF, 100 mil Chip Capacitors	N1, N2	Type N Flange Mounts
C2, C4, C10, C12	0 to 20 pF Trimmer Capacitors	R1	15 Ω Chip Resistor (0805)
C3	12 pF, 100 mil Chip Capacitor	R2	56 Ω , 1/8 W Chip Resistor
C5	130 pF, 100 mil Chip Capacitor	R3	10 Ω , 1/8 W Chip Resistor
C6, C17	120 pF, 100 mil Chip Capacitors	R4	33 k Ω , 1/8 W Chip Resistor
C7, C14	10 μ F, 50 V Electrolytic Capacitors	Z1	0.115" x 0.080" Microstrip
C8, C15	1,000 pF, 100 mil Chip Capacitors	Z2	0.230" x 0.080" Microstrip
C9, C16	0.1 μ F, 100 mil Chip Capacitors	Z3	1.034" x 0.080" Microstrip
C11	18 pF, 100 mil Chip Capacitor	Z4	0.202" x 0.080" Microstrip
L1	26 nH, 4 Turn, Coilcraft	Z5, Z6	0.260" x 0.223" Microstrip
L2	8 nH, 3 Turn, Coilcraft	Z7	1.088" x 0.080" Microstrip
L3	55.5 nH, 5 Turn, Coilcraft	Z8	0.149" x 0.080" Microstrip
		Z9	0.171" x 0.080" Microstrip
		Z10	0.095" x 0.080" Microstrip
		Board	Glass Teflon [®] , 31 mils, 2 oz. Copper

Figure 19. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

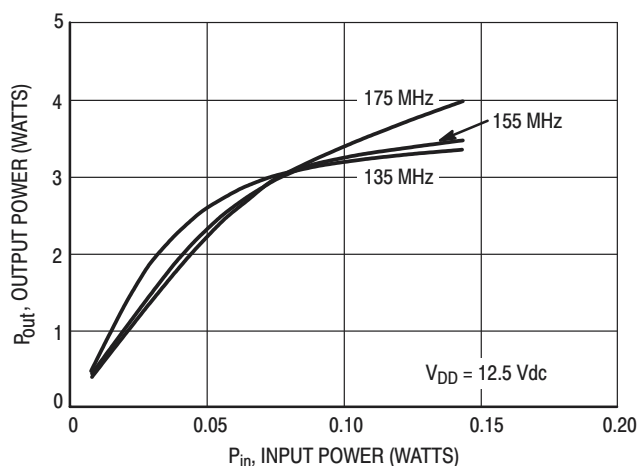


Figure 20. Output Power versus Input Power

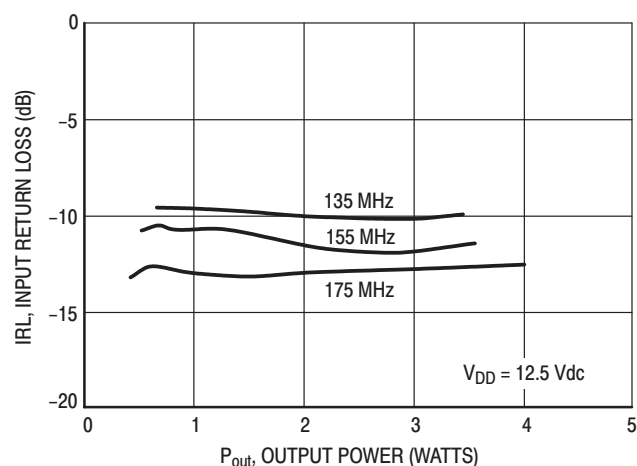


Figure 21. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 135 – 175 MHz

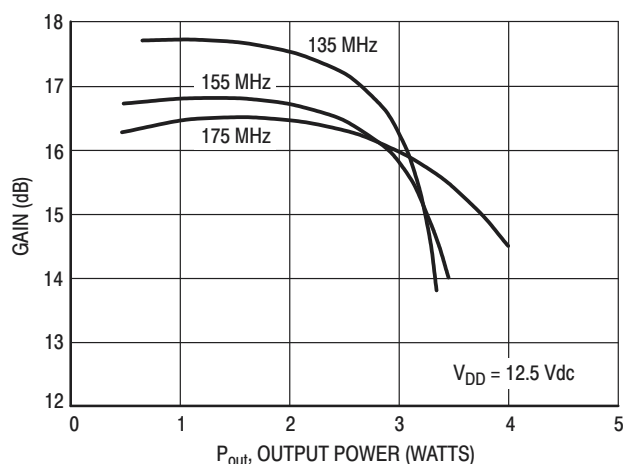


Figure 22. Gain versus Output Power

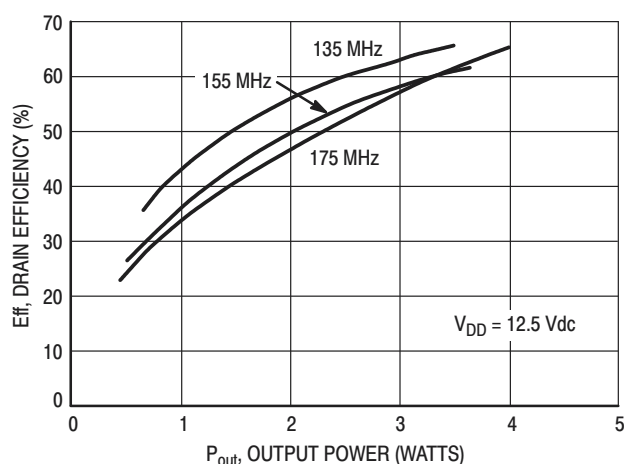


Figure 23. Drain Efficiency versus Output Power

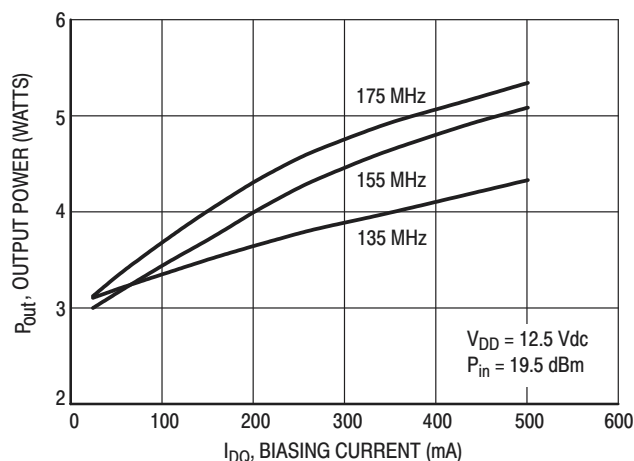


Figure 24. Output Power versus Biasing Current

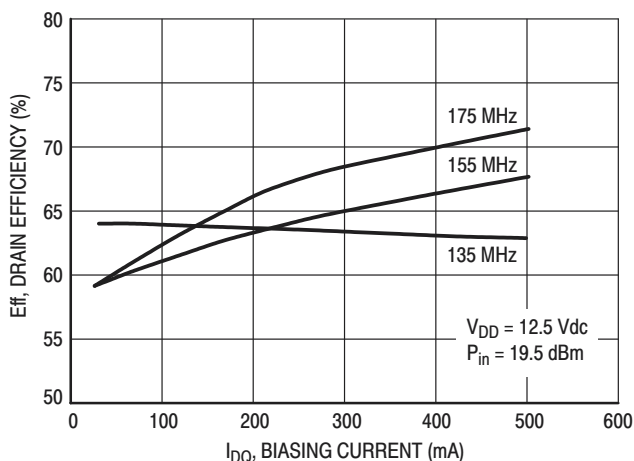


Figure 25. Drain Efficiency versus Biasing Current

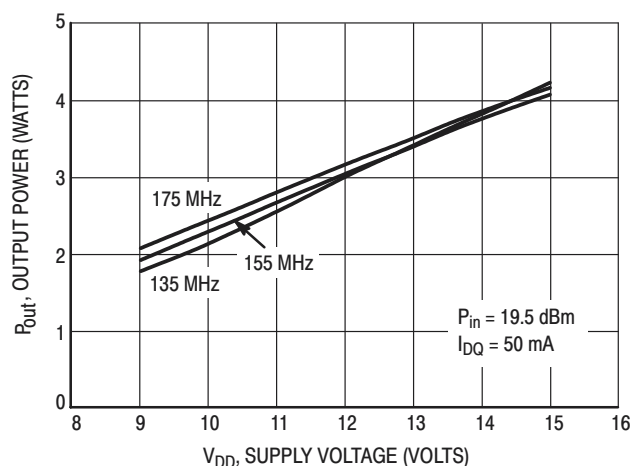


Figure 26. Output Power versus Supply Voltage

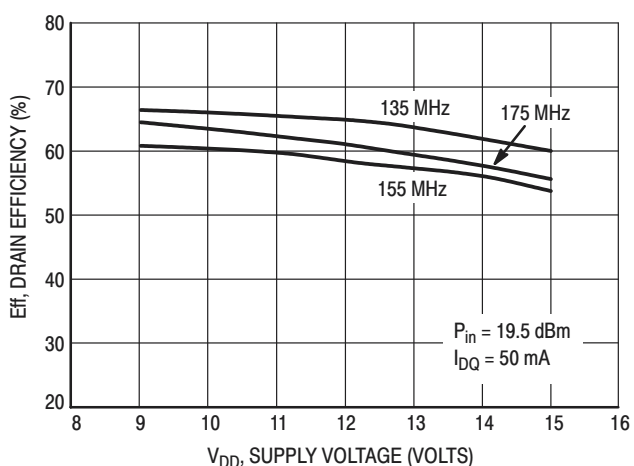
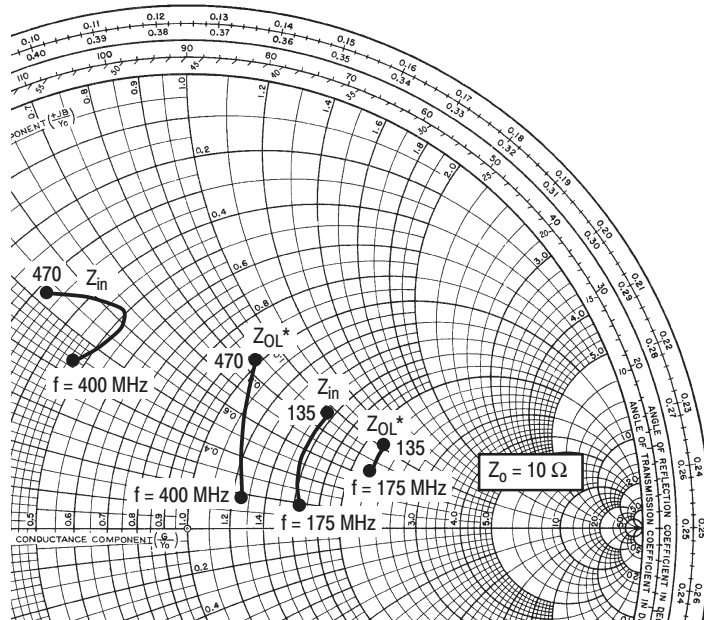
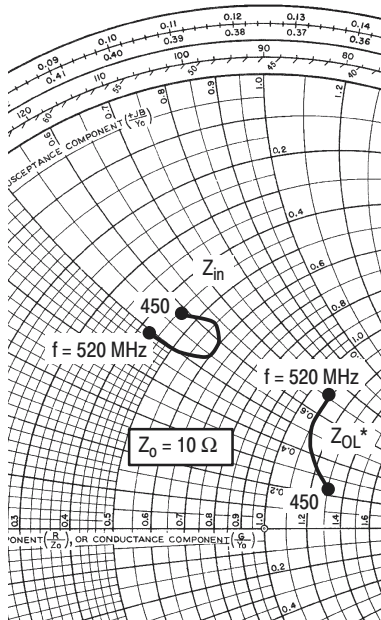


Figure 27. Drain Efficiency versus Supply Voltage



$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 50 \text{ mA}$, $P_{out} = 3 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
450	$4.64 + j5.82$	$13.11 + j2.15$
470	$5.42 + j6.34$	$12.16 + j3.26$
500	$5.96 + j5.45$	$11.03 + j5.42$
520	$4.28 + j4.94$	$10.99 + j7.18$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 50 \text{ mA}$, $P_{out} = 3 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
400	$4.72 + j4.38$	$12.57 + j1.88$
440	$4.88 + j6.34$	$11.21 + j5.87$
470	$3.22 + j5.24$	$9.82 + j8.63$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 50 \text{ mA}$, $P_{out} = 3 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
135	$16.55 + j1.82$	$22.01 + j10.32$
155	$15.59 + j5.38$	$22.03 + j8.07$
175	$15.55 + j9.43$	$22.08 + j6.85$

Z_{in} = Complex conjugate of source impedance with parallel 15Ω resistor and 120 pF capacitor in series with gate. (See Figure 1).

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Z_{in} = Complex conjugate of source impedance with parallel 15Ω resistor and 130 pF capacitor in series with gate. (See Figure 10).

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Z_{in} = Complex conjugate of source impedance with parallel 15Ω resistor and 130 pF capacitor in series with gate. (See Figure 19).

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

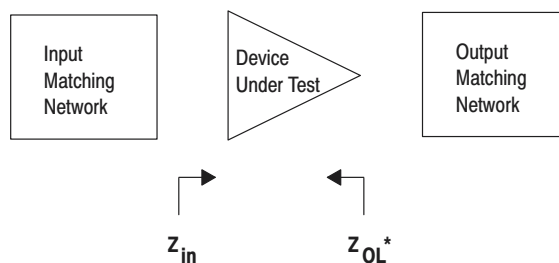


Figure 28. Series Equivalent Input and Output Impedance

Freescale Semiconductor, Inc.

Table 1. Common Source Scattering Parameters ($V_{DD} = 12.5$ Vdc)

$I_{DQ} = 50$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₂₁	∠φ	S ₁₂	∠φ	S ₂₂	∠φ
50	0.93	-94	22.09	125	0.044	33	0.77	-81
100	0.81	-131	12.78	101	0.052	6	0.61	-115
200	0.76	-153	6.31	81	0.047	-10	0.59	-135
300	0.76	-160	3.92	69	0.044	-19	0.64	-142
400	0.77	-164	2.74	60	0.040	-26	0.70	-147
500	0.79	-167	1.99	54	0.036	-31	0.75	-151
600	0.80	-169	1.55	48	0.034	-37	0.80	-155
700	0.81	-171	1.25	44	0.028	-40	0.82	-158
800	0.82	-172	1.02	38	0.027	-42	0.86	-161
900	0.83	-173	0.85	35	0.017	-42	0.88	-163
1000	0.84	-175	0.70	29	0.018	-49	0.91	-166

$I_{DQ} = 500$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₂₁	∠φ	S ₁₂	∠φ	S ₂₂	∠φ
50	0.84	-127	32.57	112	0.025	17	0.64	-130
100	0.80	-152	17.23	97	0.025	13	0.64	-153
200	0.78	-166	8.62	85	0.025	-9	0.65	-163
300	0.78	-171	5.58	79	0.023	-9	0.67	-166
400	0.78	-173	4.08	72	0.022	-9	0.69	-166
500	0.78	-175	3.14	68	0.020	-10	0.71	-167
600	0.79	-176	2.55	63	0.022	-15	0.74	-168
700	0.79	-177	2.14	60	0.019	-20	0.76	-168
800	0.80	-178	1.80	54	0.018	-31	0.79	-170
900	0.81	-178	1.54	51	0.015	-25	0.80	-170
1000	0.82	-179	1.31	46	0.012	-36	0.81	-172

$I_{DQ} = 1$ A

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₂₁	∠φ	S ₁₂	∠φ	S ₂₂	∠φ
50	0.84	-129	32.57	111	0.023	24	0.61	-137
100	0.80	-153	17.04	97	0.024	13	0.64	-156
200	0.78	-167	8.52	85	0.023	5	0.65	-165
300	0.77	-172	5.53	79	0.020	-7	0.67	-167
400	0.77	-174	4.06	73	0.020	-11	0.69	-167
500	0.78	-175	3.13	69	0.021	-9	0.72	-167
600	0.78	-177	2.54	64	0.017	-26	0.74	-168
700	0.78	-177	2.13	60	0.017	-14	0.75	-168
800	0.79	-178	1.81	55	0.015	-23	0.78	-170
900	0.80	-178	1.54	51	0.013	-31	0.79	-170
1000	0.80	-179	1.30	46	0.011	-17	0.80	-172

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

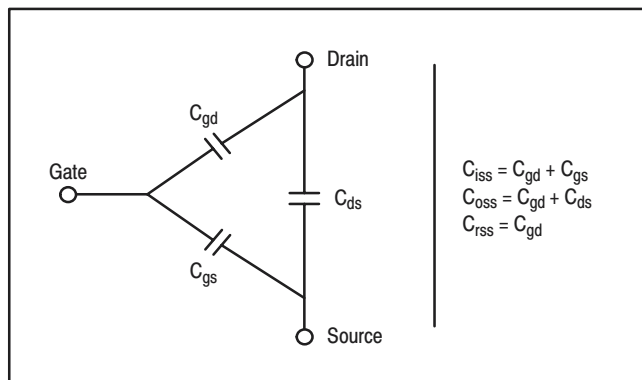
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high — on the order of $10^9 \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at $I_{DQ} = 150 \text{ mA}$, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

Freescale Semiconductor, Inc.

MOUNTING

The specified maximum thermal resistance of 4°C/W assumes a majority of the 0.065" x 0.180" source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal

impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device's S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

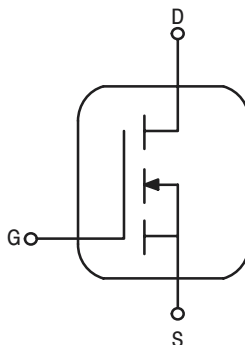
RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFETs

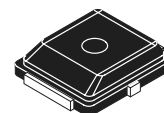
MRF1517T1

The MRF1517T1 is designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large-signal, common source amplifier applications in 7.5 volt portable FM equipment.

- Specified Performance @ 520 MHz, 7.5 Volts
 - Output Power — 8 Watts
 - Power Gain — 11 dB
 - Efficiency — 55%
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Excellent Thermal Stability
- Capable of Handling 20:1 VSWR, @ 9.5 Vdc, 520 MHz, 2 dB Overdrive
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- RF Power Plastic Surface Mount Package
- Available in Tape and Reel.
 - T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.



520 MHz, 8 W, 7.5 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 466-02, STYLE 1
(PLD-1.5)
PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage (1)	V_{DSS}	25	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	4	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ (2) Derate above 25°C	P_D	62.5 0.50	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	$^\circ\text{C/W}$

(1) Not designed for 12.5 volt applications.

(2) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Current ($V_{DS} = 35\text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current ($V_{GS} = 10\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = 7.5\text{ Vdc}$, $I_D = 120\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1.0	1.7	2.1	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$V_{DS(on)}$	—	0.5	—	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	g_{fs}	0.9	—	—	S

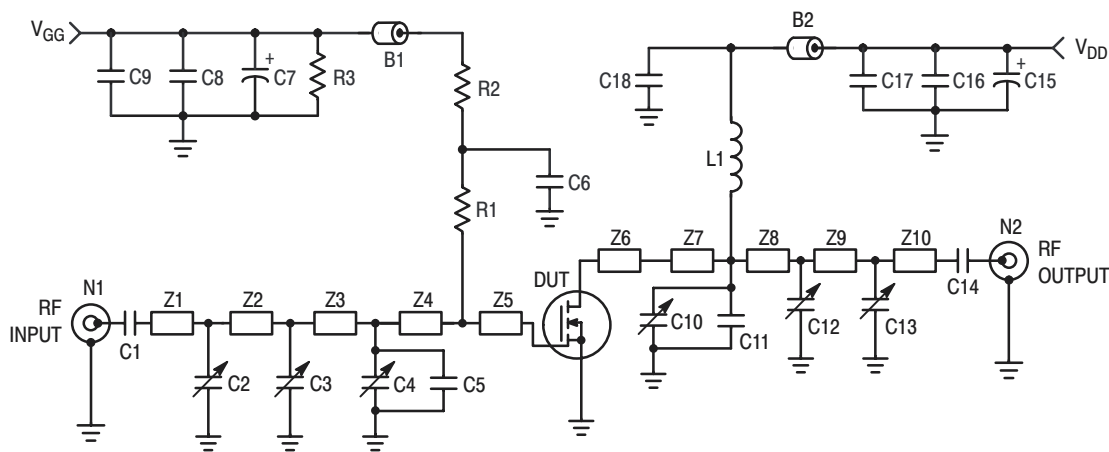
DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 7.5\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	66	—	pF
Output Capacitance ($V_{DS} = 7.5\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{oss}	—	38	—	pF
Reverse Transfer Capacitance ($V_{DS} = 7.5\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	6	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain ($V_{DD} = 7.5\text{ Vdc}$, $P_{out} = 8\text{ Watts}$, $I_{DQ} = 150\text{ mA}$, $f = 520\text{ MHz}$)	G_{ps}	10	11	—	dB
Drain Efficiency ($V_{DD} = 7.5\text{ Vdc}$, $P_{out} = 8\text{ Watts}$, $I_{DQ} = 150\text{ mA}$, $f = 520\text{ MHz}$)	η	50	55	—	%

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	R1	15 Ω , 0805 Chip Resistor
C1	300 pF, 100 mil Chip Capacitor	R2	1.0 k Ω , 1/8 W Resistor
C2, C3, C4, C10, C12, C13	0 to 20 pF, Trimmer Capacitor	R3	33 k Ω , 1/2 W Resistor
C5, C11	43 pF, 100 mil Chip Capacitor	Z1	0.315" x 0.080" Microstrip
C6, C18	120 pF, 100 mil Chip Capacitor	Z2	1.415" x 0.080" Microstrip
C7, C15	10 μ F, 50 V Electrolytic Capacitor	Z3	0.322" x 0.080" Microstrip
C8, C16	0.1 μ F, 100 mil Chip Capacitor	Z4	0.022" x 0.080" Microstrip
C9, C17	1,000 pF, 100 mil Chip Capacitor	Z5, Z6	0.260" x 0.223" Microstrip
C14	330 pF, 100 mil Chip Capacitor	Z7	0.050" x 0.080" Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z8	0.625" x 0.080" Microstrip
N1, N2	Type N Flange Mount	Z9	0.800" x 0.080" Microstrip
		Z10	0.589" x 0.080" Microstrip
		Board	Glass Teflon [®] , 31 mils, 2 oz. Copper

Figure 1. 480 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 480 – 520 MHz

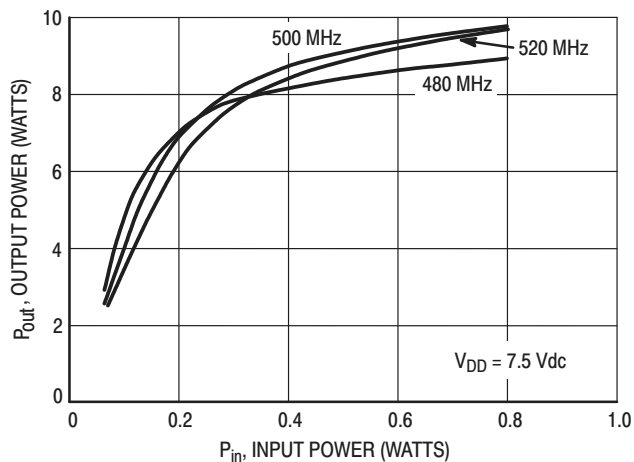


Figure 2. Output Power versus Input Power

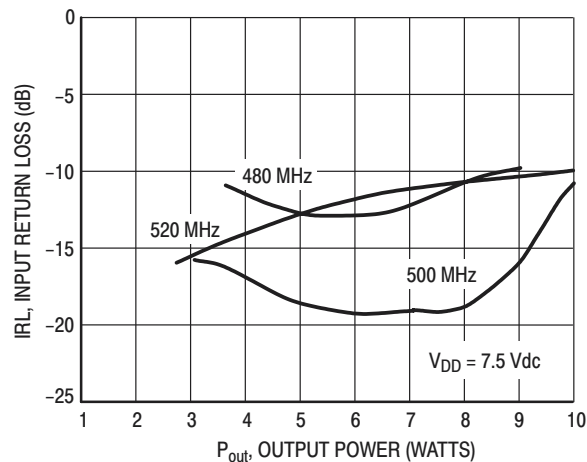


Figure 3. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 480 – 520 MHz

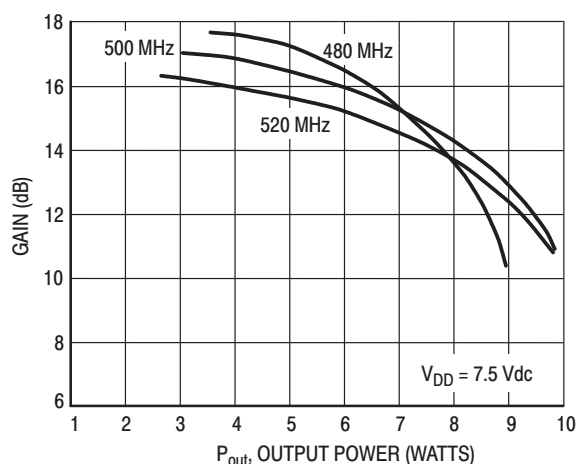


Figure 4. Gain versus Output Power

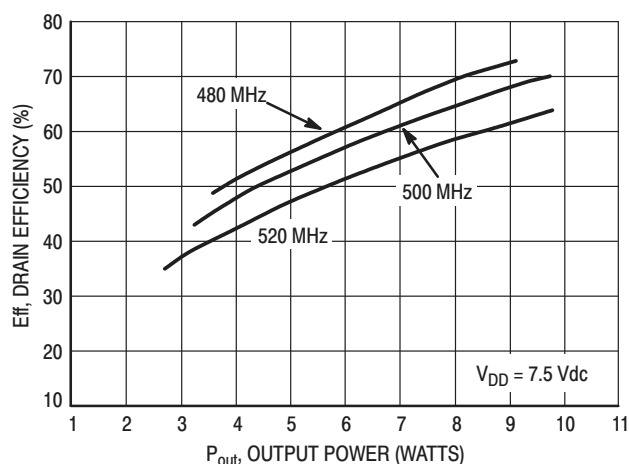


Figure 5. Drain Efficiency versus Output Power

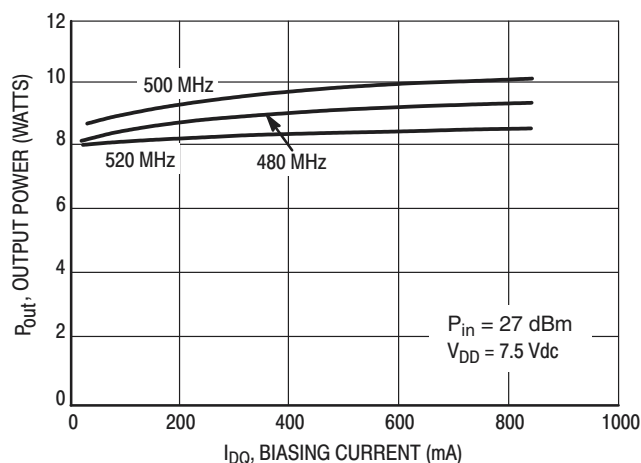


Figure 6. Output Power versus Biasing Current

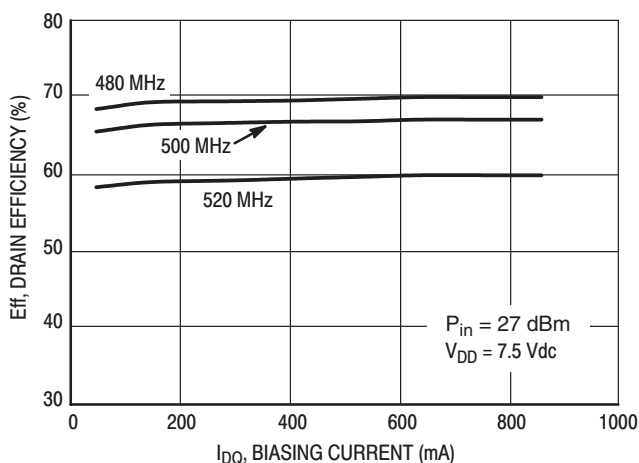


Figure 7. Drain Efficiency versus Biasing Current

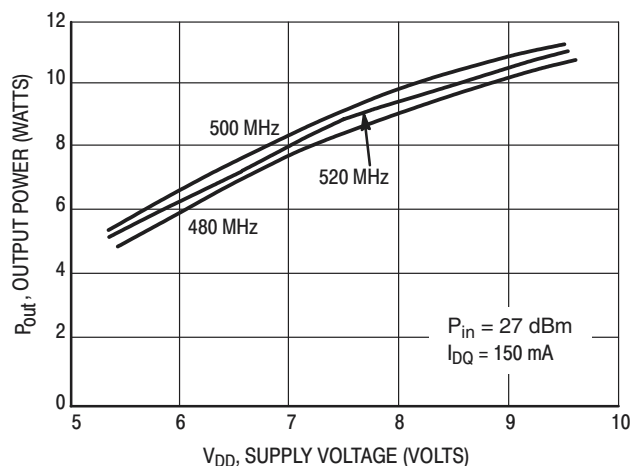


Figure 8. Output Power versus Supply Voltage

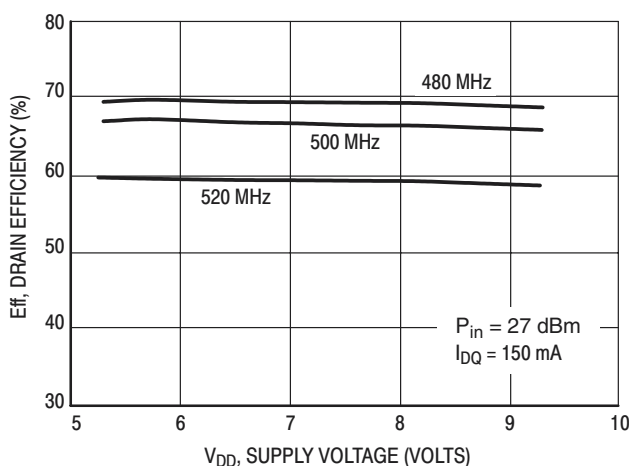
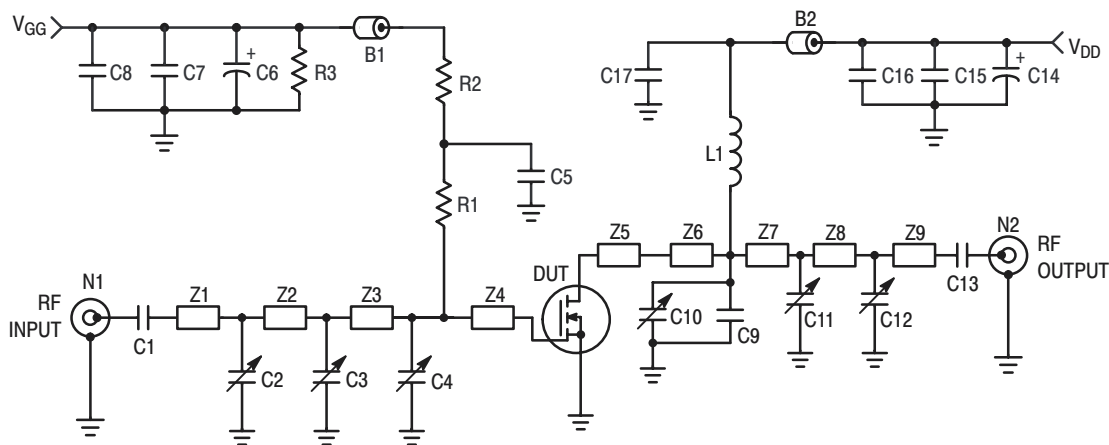


Figure 9. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	R1	12 Ω , 0805 Chip Resistor
C1, C13	300 pF, 100 mil Chip Capacitor	R2	1.0 k Ω , 1/8 W Resistor
C2, C3, C4, C10,	0 to 20 pF, Trimmer Capacitor	R3	33 k Ω , 1/2 W Resistor
C11, C12	130 pF, 100 mil Chip Capacitor	Z1	0.617" x 0.080" Microstrip
C5, C17	10 μ F, 50 V Electrolytic Capacitor	Z2	0.723" x 0.080" Microstrip
C6, C14	0.1 μ F, 100 mil Chip Capacitor	Z3	0.513" x 0.080" Microstrip
C7, C15	1,000 pF, 100 mil Chip Capacitor	Z4, Z5	0.260" x 0.223" Microstrip
C8, C16	33 pF, 100 mil Chip Capacitor	Z6	0.048" x 0.080" Microstrip
C9	55.5 nH, 5 Turn, Coilcraft	Z7	0.577" x 0.080" Microstrip
L1	Type N Flange Mount	Z8	1.135" x 0.080" Microstrip
N1, N2		Z9	0.076" x 0.080" Microstrip
		Board	Glass Teflon [®] , 31 mils, 2 oz. Copper

Figure 10. 400 – 440 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 400 – 440 MHz

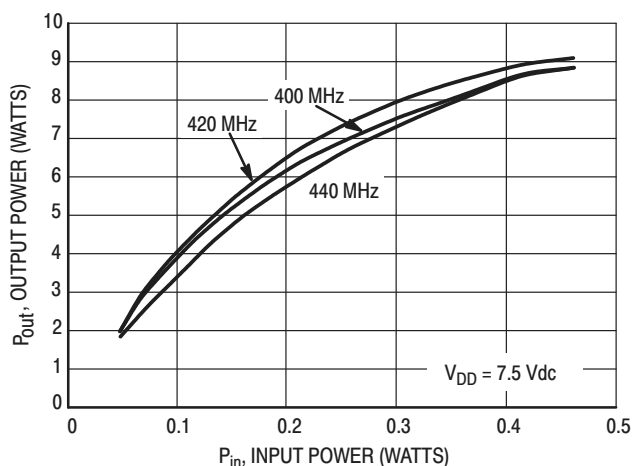


Figure 11. Output Power versus Input Power

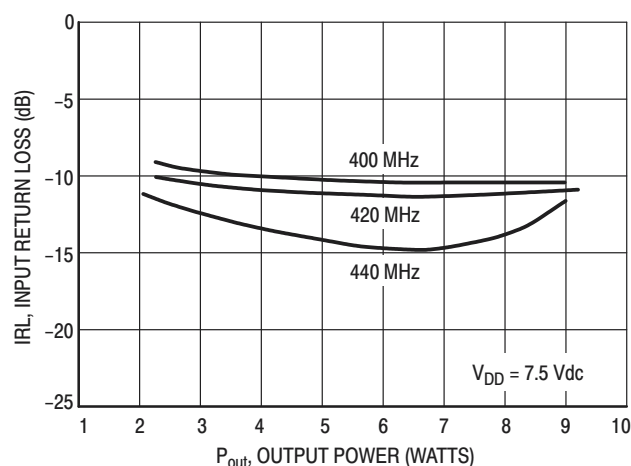


Figure 12. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 400 – 440 MHz

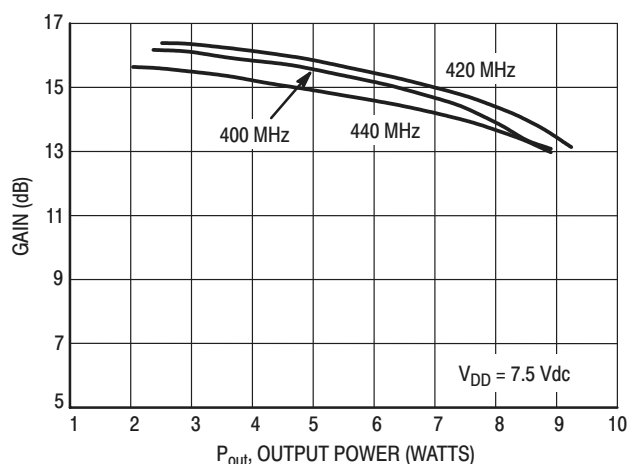


Figure 13. Gain versus Output Power

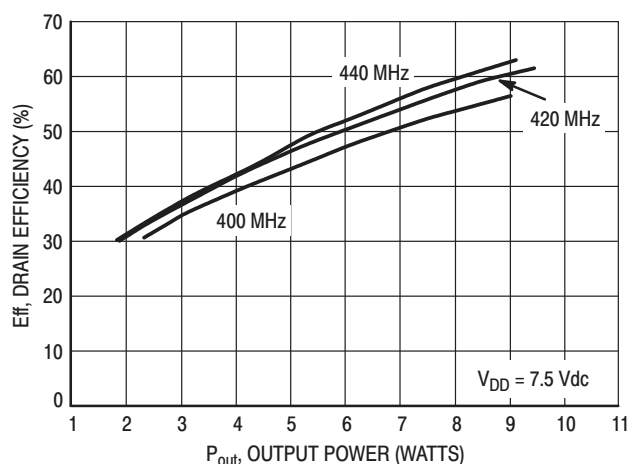


Figure 14. Drain Efficiency versus Output Power

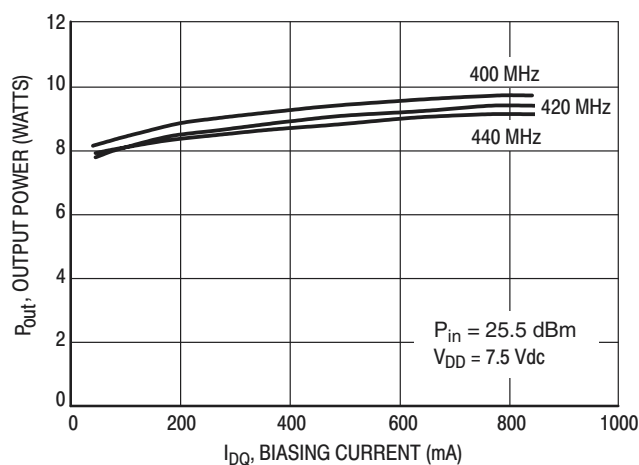


Figure 15. Output Power versus Biasing Current

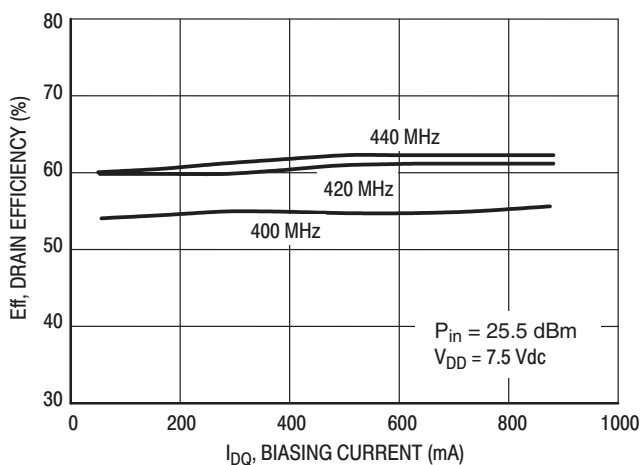


Figure 16. Drain Efficiency versus Biasing Current

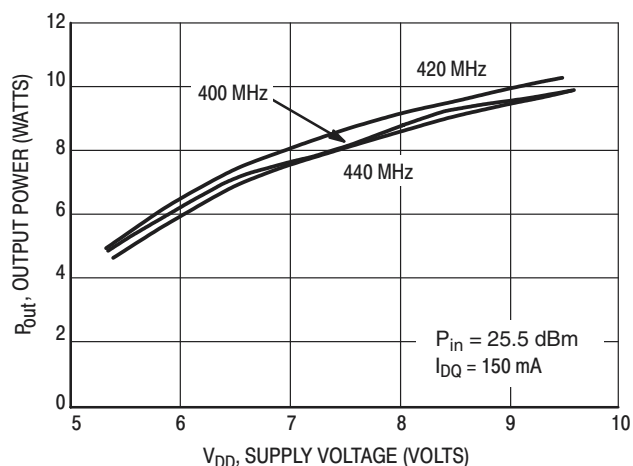


Figure 17. Output Power versus Supply Voltage

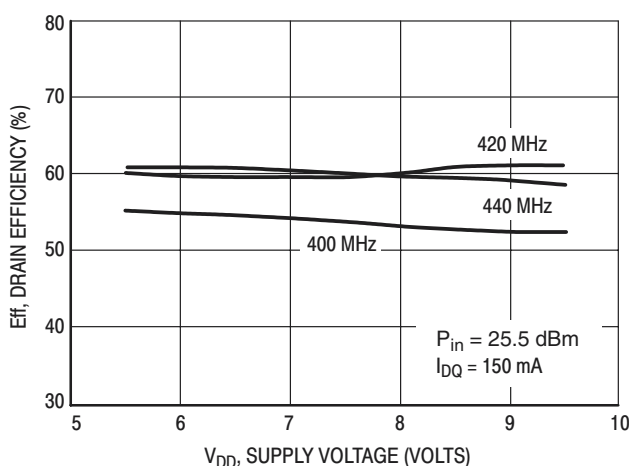
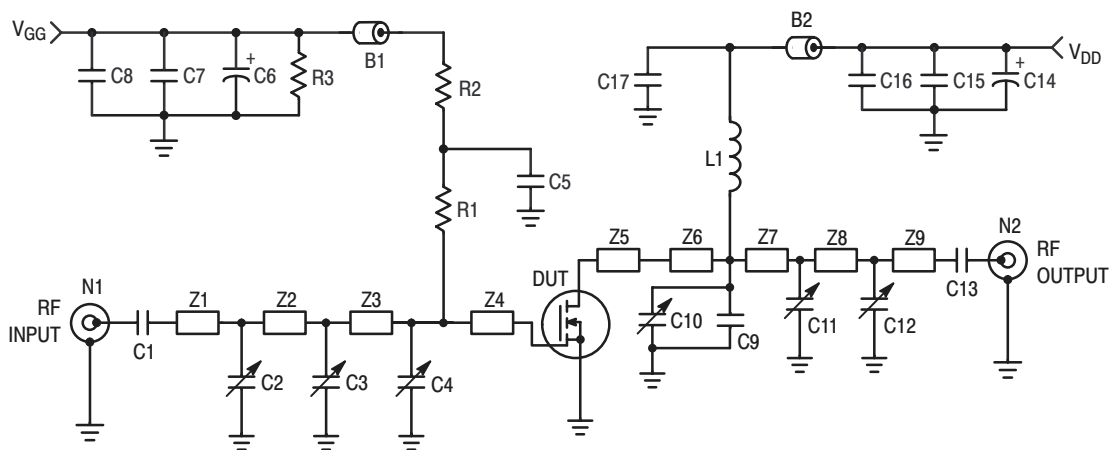


Figure 18. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	R1	15 Ω , 0805 Chip Resistor
C1	240 pF, 100 mil Chip Capacitor	R2	1.0 k Ω , 1/8 W Resistor
C2, C3, C4, C10,	0 to 20 pF, Trimmer Capacitor	R3	33 k Ω , 1/2 W Resistor
C11, C12	130 pF, 100 mil Chip Capacitor	Z1	0.471" x 0.080" Microstrip
C5, C17	10 mF, 50 V Electrolytic Capacitor	Z2	1.082" x 0.080" Microstrip
C6, C14	0.1 mF, 100 mil Chip Capacitor	Z3	0.372" x 0.080" Microstrip
C7, C15	1,000 pF, 100 mil Chip Capacitor	Z4, Z5	0.260" x 0.223" Microstrip
C8, C16	39 pF, 100 mil Chip Capacitor	Z6	0.050" x 0.080" Microstrip
C9	330 pF, 100 mil Chip Capacitor	Z7	0.551" x 0.080" Microstrip
C13	55.5 nH, 5 Turn, Coilcraft	Z8	0.825" x 0.080" Microstrip
L1	Type N Flange Mount	Z9	0.489" x 0.080" Microstrip
N1, N2		Board	Glass Teflon [®] , 31 mils, 2 oz. Copper

Figure 19. 440 – 480 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 440 – 480 MHz

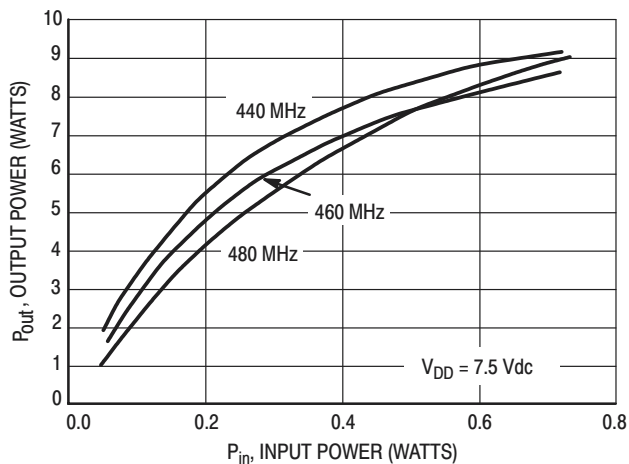


Figure 20. Output Power versus Input Power

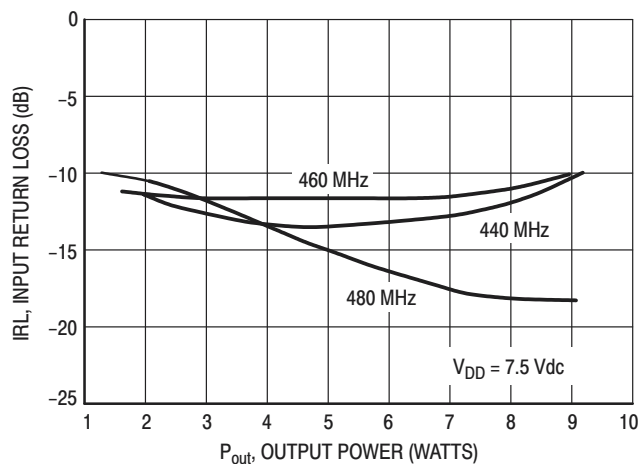


Figure 21. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 440 – 480 MHz

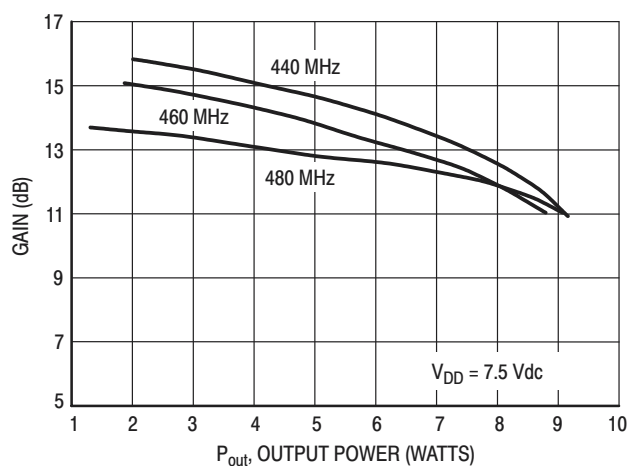


Figure 22. Gain versus Output Power

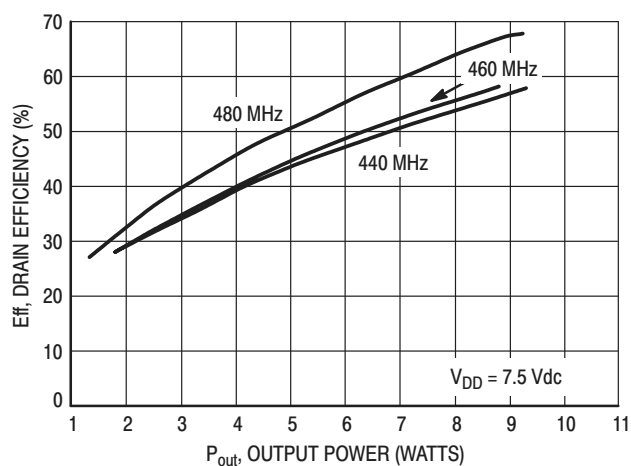


Figure 23. Drain Efficiency versus Output Power

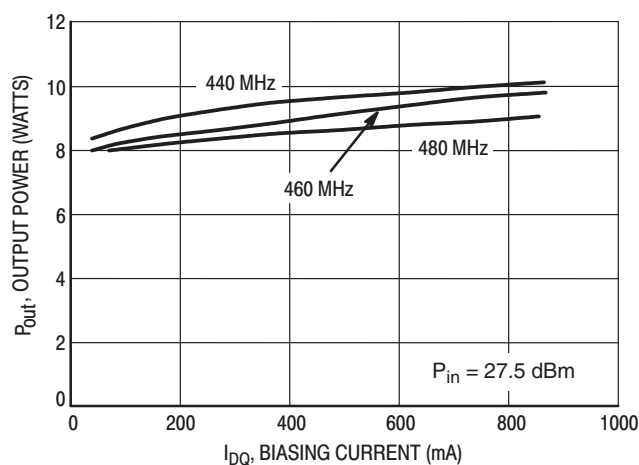


Figure 24. Output Power versus Biasing Current

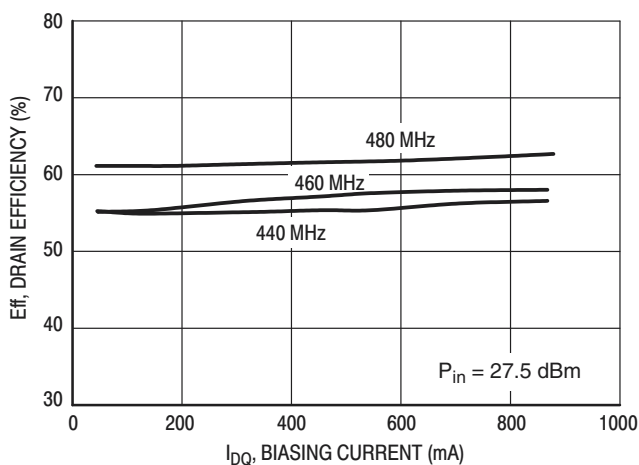


Figure 25. Drain Efficiency versus Biasing Current

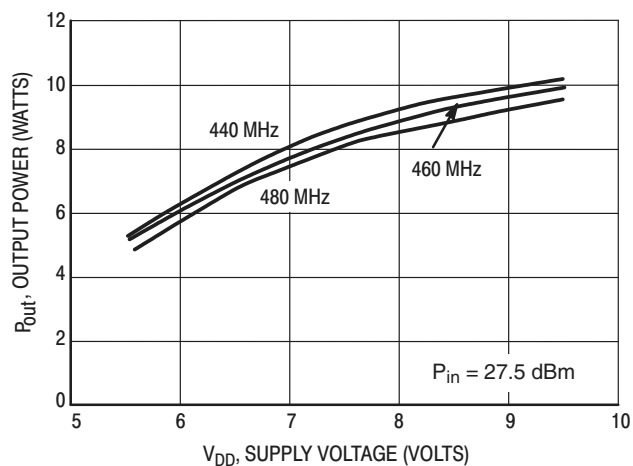


Figure 26. Output Power versus Supply Voltage

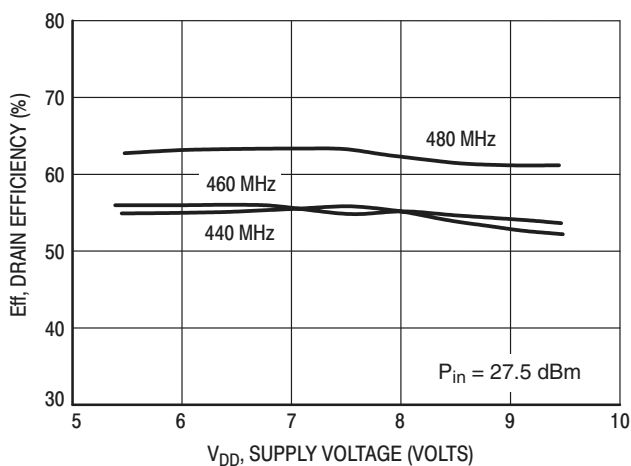
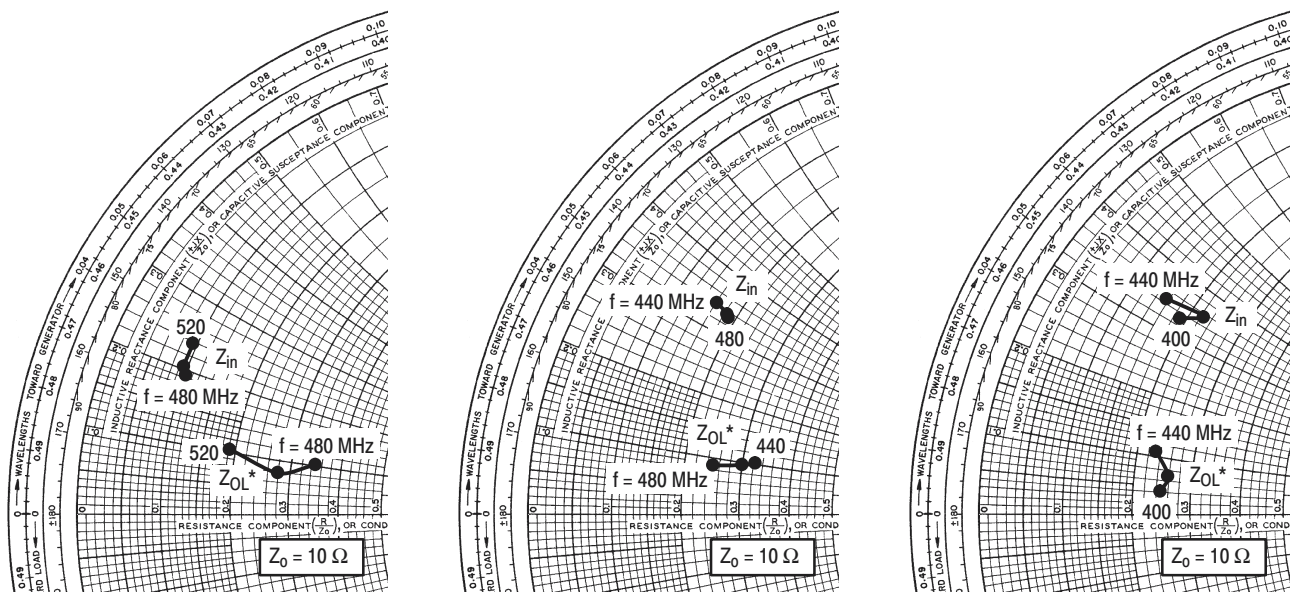


Figure 27. Drain Efficiency versus Supply Voltage



$V_{DD} = 7.5 \text{ V}$, $I_{DQ} = 150 \text{ mA}$, $P_{out} = 8 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
480	$1.06 + j1.82$	$3.51 + j0.99$
500	$0.97 + j2.01$	$2.82 + j0.75$
520	$0.975 + j2.37$	$1.87 + j1.03$

$V_{DD} = 7.5 \text{ V}$, $I_{DQ} = 150 \text{ mA}$, $P_{out} = 8 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
440	$1.62 + j3.41$	$3.25 + j0.98$
460	$1.85 + j3.35$	$3.05 + j0.93$
480	$1.91 + j3.31$	$2.54 + j0.84$

$V_{DD} = 7.5 \text{ V}$, $I_{DQ} = 150 \text{ mA}$, $P_{out} = 8 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
400	$1.96 + j3.32$	$2.52 + j0.39$
420	$2.31 + j3.56$	$2.61 + j0.64$
440	$1.60 + j3.45$	$2.37 + j1.04$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

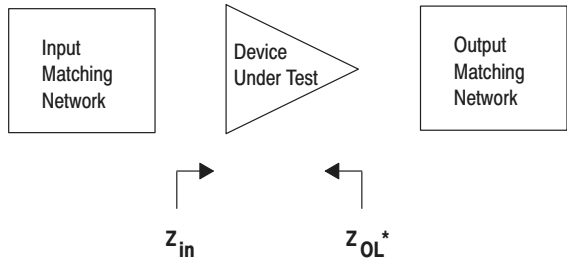


Figure 28. Series Equivalent Input and Output Impedance

Freescale Semiconductor, Inc.

Table 1. Common Source Scattering Parameters ($V_{DD} = 7.5$ Vdc)

$I_{DQ} = 150$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
50	0.84	-152	17.66	97	0.016	0	0.77	-167
100	0.84	-164	8.86	85	0.016	5	0.78	-172
200	0.86	-170	4.17	72	0.015	-5	0.79	-173
300	0.88	-171	2.54	62	0.014	-8	0.80	-172
400	0.90	-172	1.72	55	0.013	-25	0.83	-172
500	0.92	-172	1.28	50	0.013	-10	0.84	-172
600	0.94	-173	0.98	46	0.014	-22	0.86	-171
700	0.95	-173	0.76	41	0.010	-30	0.86	-172
800	0.96	-174	0.61	38	0.011	-14	0.86	-171
900	0.96	-175	0.50	33	0.011	-31	0.85	-172
1000	0.97	-175	0.40	31	0.006	55	0.88	-171

$I_{DQ} = 800$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
50	0.90	-165	20.42	94	0.018	1	0.76	-164
100	0.89	-172	10.20	87	0.015	-7	0.77	-170
200	0.90	-175	4.96	79	0.015	-12	0.77	-172
300	0.90	-176	3.17	73	0.017	-2	0.80	-171
400	0.91	-176	2.26	67	0.013	1	0.82	-172
500	0.92	-176	1.75	63	0.011	-6	0.83	-171
600	0.93	-176	1.39	59	0.012	-31	0.85	-171
700	0.94	-176	1.14	55	0.015	-34	0.88	-171
800	0.94	-176	0.93	51	0.008	-22	0.87	-171
900	0.95	-177	0.78	45	0.007	2	0.87	-172
1000	0.96	-177	0.65	43	0.008	-40	0.90	-170

$I_{DQ} = 1.5$ A

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
50	0.92	-165	19.90	95	0.017	3	0.76	-164
100	0.90	-172	9.93	88	0.018	2	0.77	-170
200	0.91	-176	4.84	80	0.016	-4	0.77	-172
300	0.91	-176	3.10	74	0.014	-11	0.80	-172
400	0.92	-176	2.22	68	0.014	-14	0.81	-172
500	0.93	-176	1.73	64	0.016	-8	0.83	-171
600	0.94	-176	1.39	61	0.013	-24	0.85	-171
700	0.94	-176	1.12	56	0.013	-24	0.87	-171
800	0.95	-176	0.93	52	0.009	-12	0.87	-171
900	0.96	-177	0.78	46	0.008	10	0.87	-173
1000	0.97	-177	0.64	44	0.012	4	0.89	-169

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

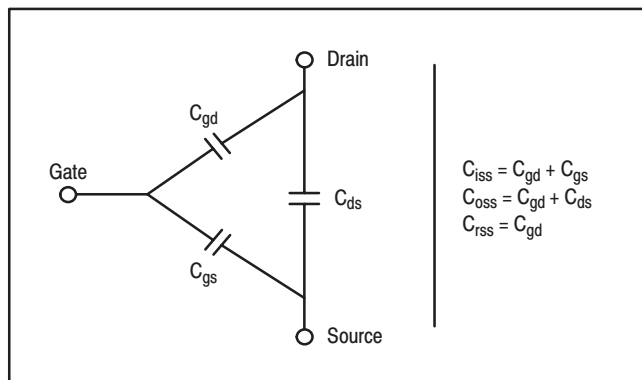
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high — on the order of $10^9 \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at $I_{DQ} = 150 \text{ mA}$, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065" x 0.180" source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal

impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device's S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

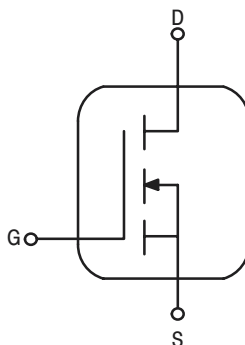
RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

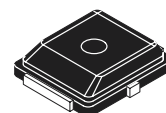
MRF1518T1

The MRF1518T1 is designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts
 - Output Power — 8 Watts
 - Power Gain — 11 dB
 - Efficiency — 55%
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 520 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- RF Power Plastic Surface Mount Package
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- Available in Tape and Reel. T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.



520 MHz, 8 W, 12.5 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 466-02, STYLE 1
(PLD-1.5)

PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	40	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	4	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ (1) Derate above 25°C	P_D	62.5 0.50	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	$^\circ\text{C/W}$

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Current (V _{DS} = 40 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 10 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 12.5 Vdc, I _D = 100 μA)	V _{GS(th)}	1.0	1.6	2.1	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.4	—	Vdc

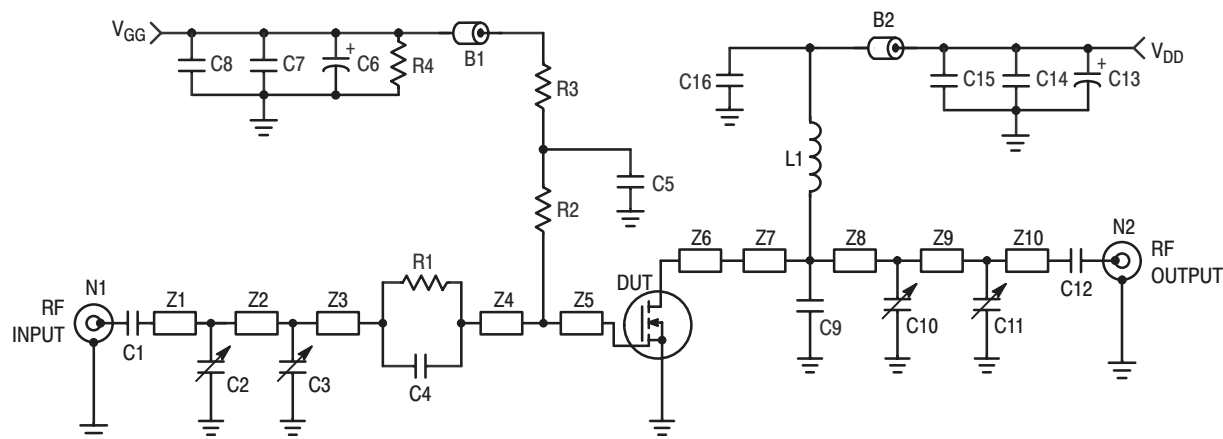
DYNAMIC CHARACTERISTICS

Input Capacitance (V _{DS} = 12.5 Vdc, V _{GS} = 0, f = 1 MHz)	C _{iss}	—	66	—	pF
Output Capacitance (V _{DS} = 12.5 Vdc, V _{GS} = 0, f = 1 MHz)	C _{oss}	—	33	—	pF
Reverse Transfer Capacitance (V _{DS} = 12.5 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	4.5	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain (V _{DD} = 12.5 Vdc, P _{out} = 8 Watts, I _{DQ} = 150 mA, f = 520 MHz)	G _{ps}	10	11	—	dB
Drain Efficiency (V _{DD} = 12.5 Vdc, P _{out} = 8 Watts, I _{DQ} = 150 mA, f = 520 MHz)	η	50	55	—	%

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Beads, Fair Rite Products (2743021446)	R4	33 k Ω , 1/8 W Resistor
C1, C12	240 pF, 100 mil Chip Capacitors	Z1	0.451" x 0.080" Microstrip
C2, C3, C10, C11	0 to 20 pF Trimmer Capacitors	Z2	1.005" x 0.080" Microstrip
C4	82 pF, 100 mil Chip Capacitor	Z3	0.020" x 0.080" Microstrip
C5, C16	120 pF, 100 mil Chip Capacitors	Z4	0.155" x 0.080" Microstrip
C6, C13	10 μ F, 50 V Electrolytic Capacitors	Z5, Z6	0.260" x 0.223" Microstrip
C7, C14	1,200 pF, 100 mil Chip Capacitors	Z7	0.065" x 0.080" Microstrip
C8, C15	0.1 μ F, 100 mil Chip Capacitors	Z8	0.266" x 0.080" Microstrip
C9	30 pF, 100 mil Chip Capacitor	Z9	1.113" x 0.080" Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z10	0.433" x 0.080" Microstrip
N1, N2	Type N Flange Mounts	Board	Glass Teflon [®] , 31 mils, 2 oz. Copper
R1	15 Ω Chip Resistor (0805)		
R2	51 Ω , 1/2 W Resistor		
R3	10 Ω Chip Resistor (0805)		

Figure 1. 450 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 – 520 MHz

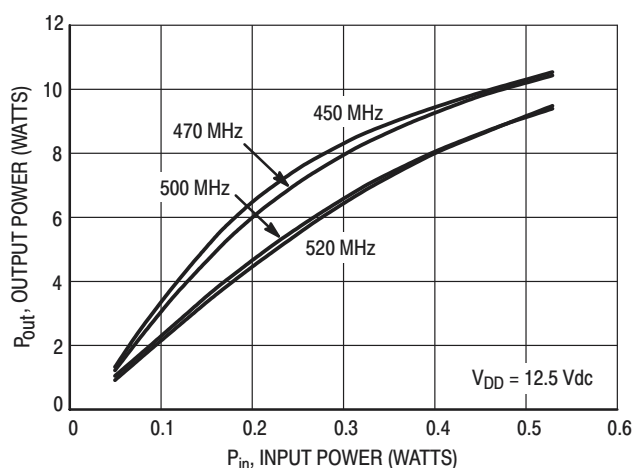


Figure 2. Output Power versus Input Power

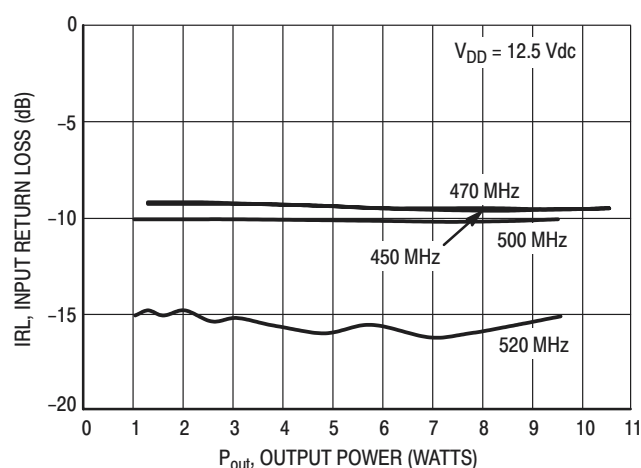


Figure 3. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 450 – 520 MHz

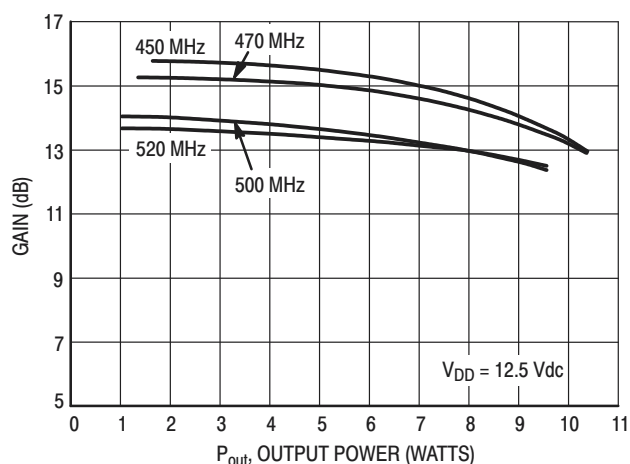


Figure 4. Gain versus Output Power

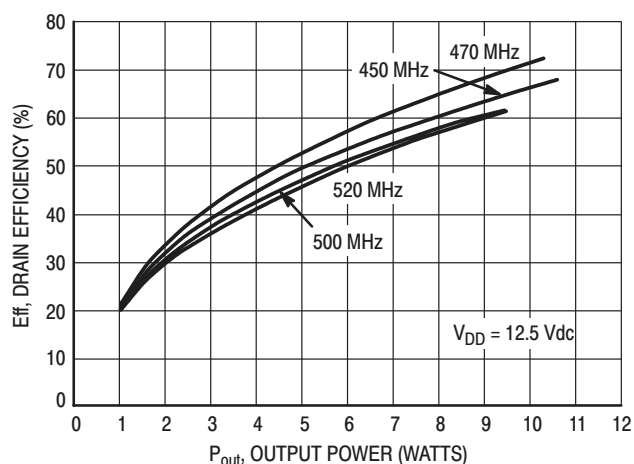


Figure 5. Drain Efficiency versus Output Power

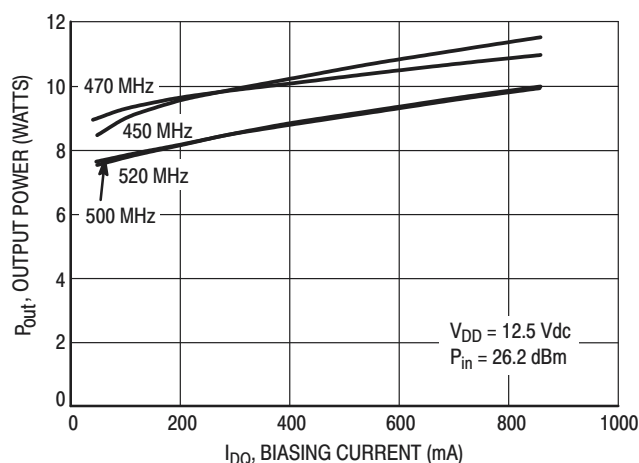


Figure 6. Output Power versus Biasing Current

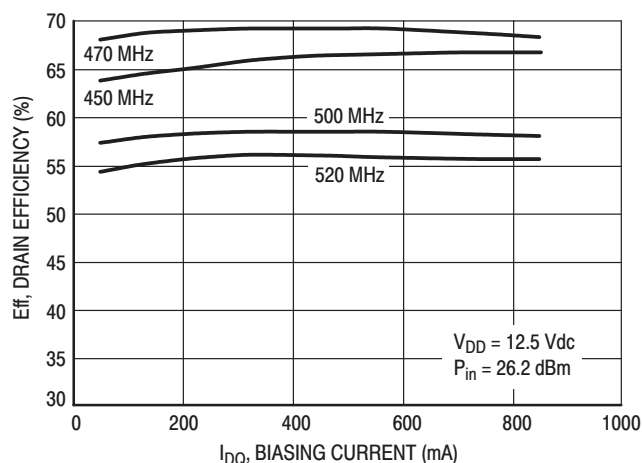


Figure 7. Drain Efficiency versus Biasing Current

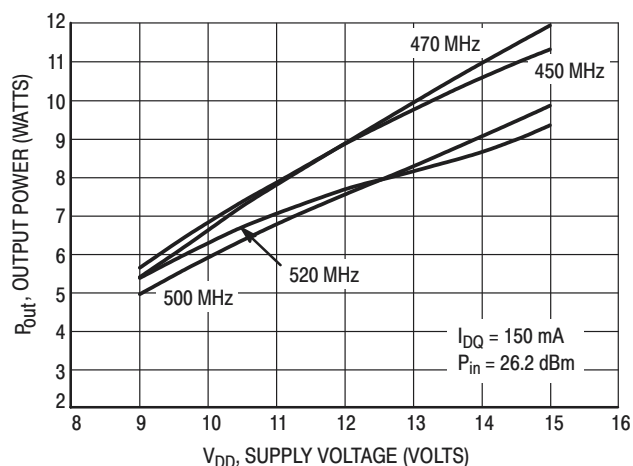


Figure 8. Output Power versus Supply Voltage

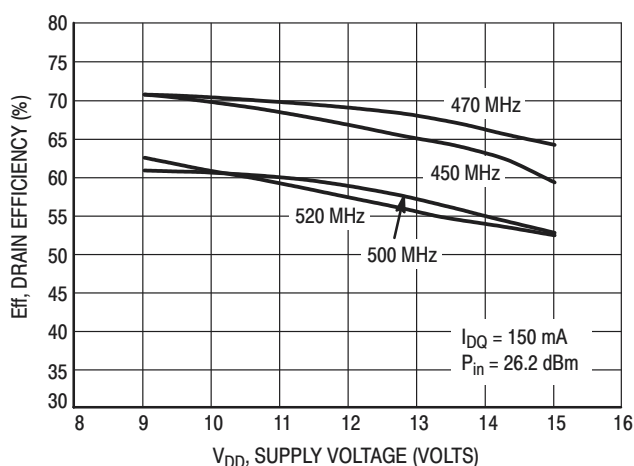
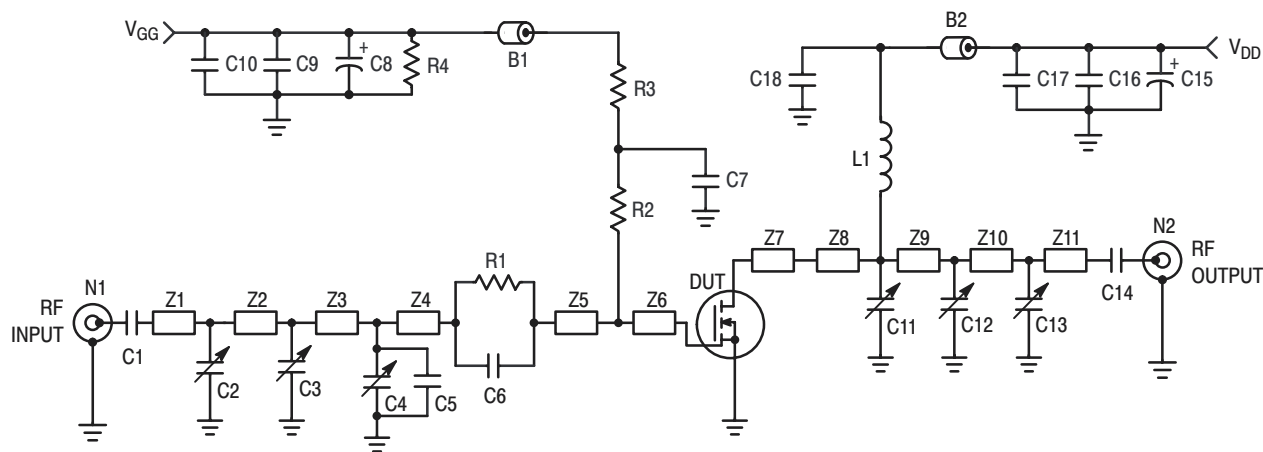


Figure 9. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Beads, Fair Rite Products (2743021446)	R3	10 Ω Chip Resistor (0805)
C1, C14	240 pF, 100 mil Chip Capacitors	R4	33 k Ω , 1/8 W Resistor
C2, C3, C4, C11, C12, C13	0 to 20 pF Trimmer Capacitors	Z1	0.476" x 0.080" Microstrip
C5	30 pF, 100 mil Chip Capacitor	Z2	0.724" x 0.080" Microstrip
C6	47 pF, 100 mil Chip Capacitor	Z3	0.348" x 0.080" Microstrip
C7, C18	120 pF, 100 mil Chip Capacitors	Z4	0.048" x 0.080" Microstrip
C8, C15	10 μ F, 50 V Electrolytic Capacitors	Z5	0.175" x 0.080" Microstrip
C9, C16	1,200 pF, 100 mil Chip Capacitors	Z6, Z7	0.260" x 0.223" Microstrip
C10, C17	0.1 μ F, 100 mil Chip Capacitors	Z8	0.239" x 0.080" Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z9	0.286" x 0.080" Microstrip
N1, N2	Type N Flange Mounts	Z10	0.806" x 0.080" Microstrip
R1	15 Ω Chip Resistor (0805)	Z11	0.553" x 0.080" Microstrip
R2	51 Ω , 1/2 W Resistor	Board	Glass Teflon [®] , 31 mils, 2 oz. Copper

Figure 10. 400 – 470 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 400 – 470 MHz

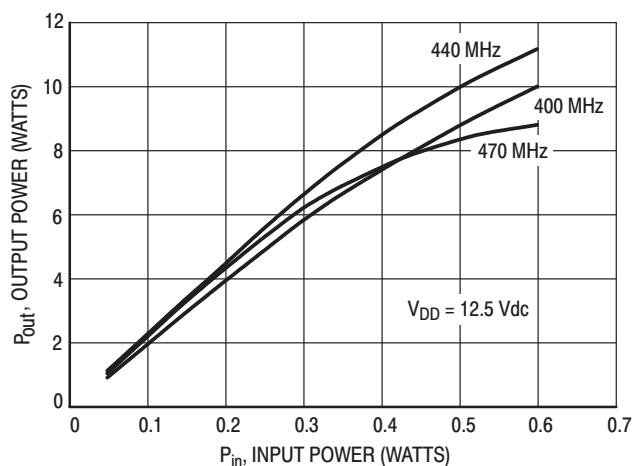


Figure 11. Output Power versus Input Power

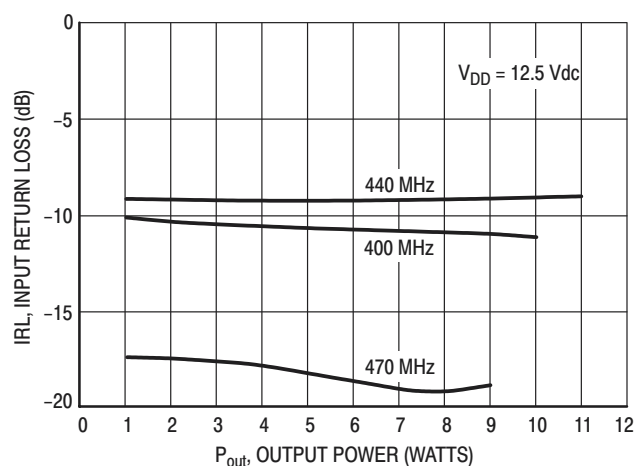


Figure 12. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 400 – 470 MHz

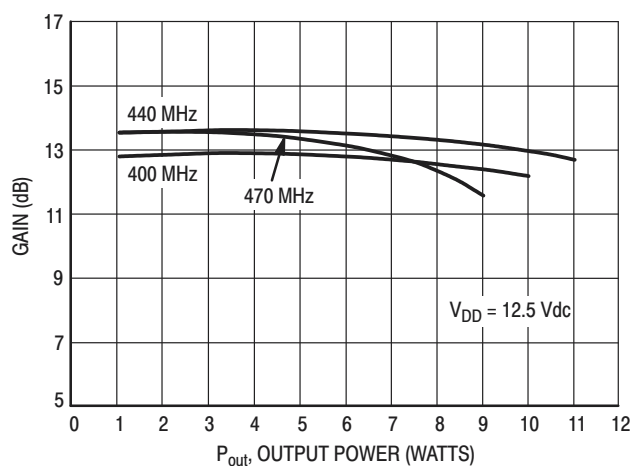


Figure 13. Gain versus Output Power

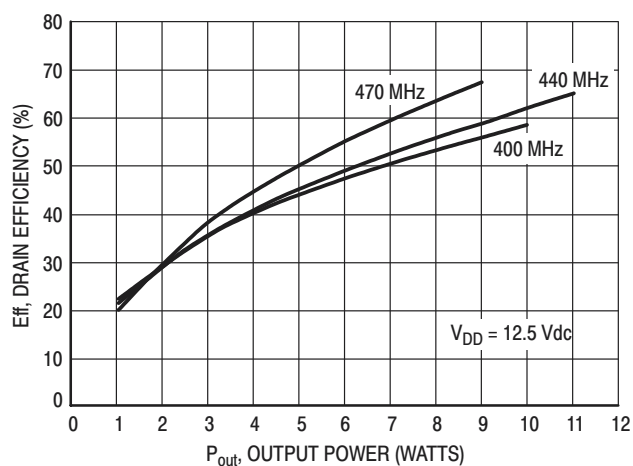


Figure 14. Drain Efficiency versus Output Power

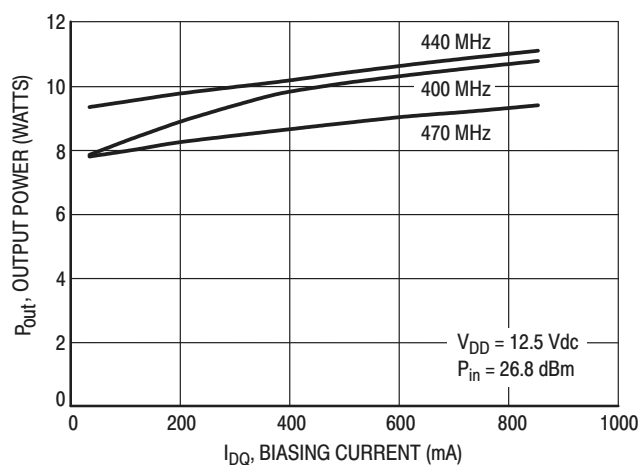


Figure 15. Output Power versus Biasing Current

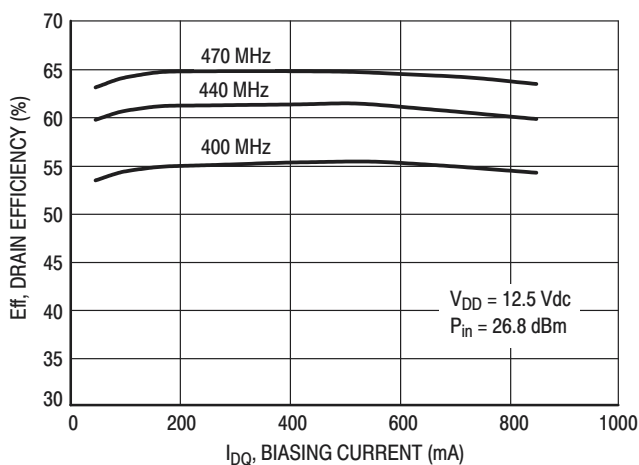


Figure 16. Drain Efficiency versus Biasing Current

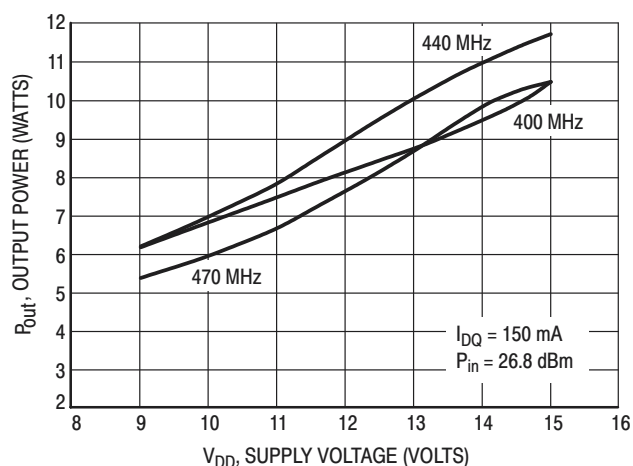


Figure 17. Output Power versus Supply Voltage

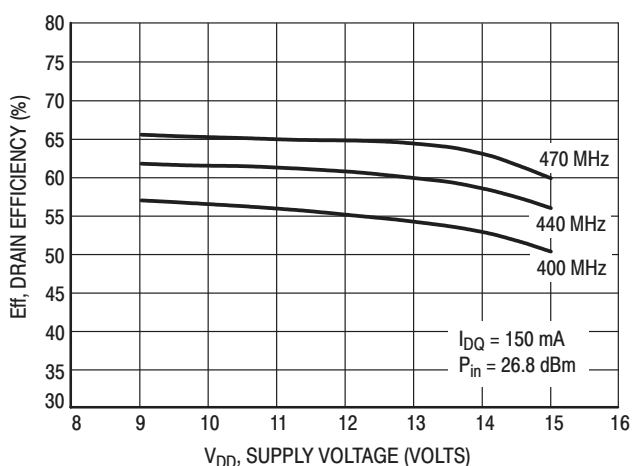
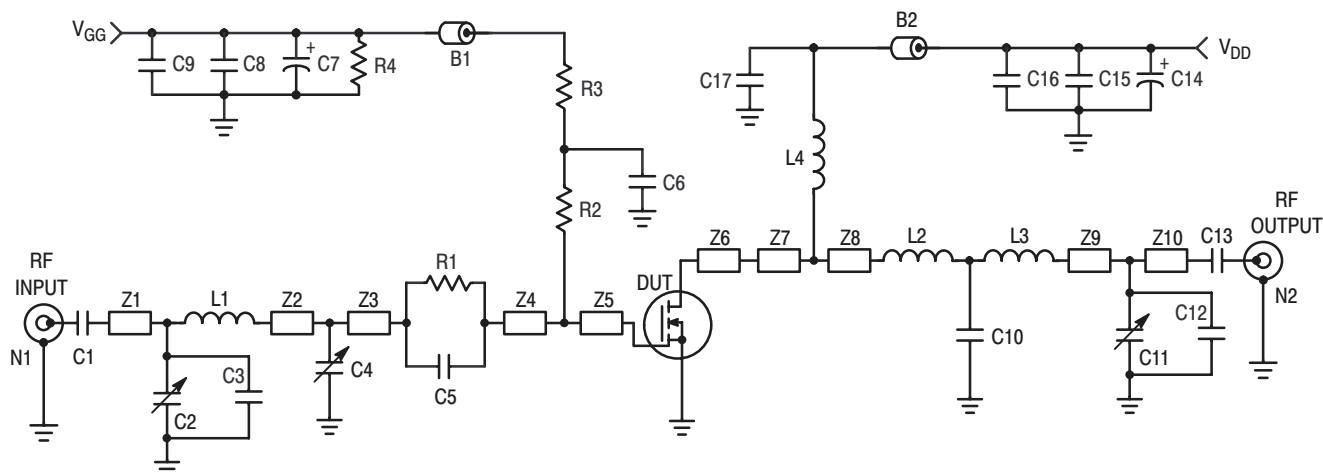


Figure 18. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Beads, Fair Rite Products (2743021446)	L4	55.5 nH, 5 Turn, Coilcraft
C1, C13	330 pF, 100 mil Chip Capacitors	N1, N2	Type N Flange Mounts
C2, C4, C11	0 to 20 pF Trimmer Capacitors	R1	15 Ω Chip Resistor (0805)
C3	12 pF, 100 mil Chip Capacitor	R2	56 Ω , 1/4 W Carbon Resistor
C5	43 pF, 100 mil Chip Capacitor	R3	100 Ω Chip Resistor (0805)
C6, C17	75 pF, 100 mil Chip Capacitors	R4	33 k Ω , 1/8 W Carbon Resistor
C7, C14	10 μ F, 50 V Electrolytic Capacitors	Z1	0.115" x 0.080" Microstrip
C8, C15	1,200 pF, 100 mil Chip Capacitors	Z2	0.255" x 0.080" Microstrip
C9, C16	0.1 μ F, 100 mil Chip Capacitors	Z3	1.037" x 0.080" Microstrip
C10	75 pF, 100 mil Chip Capacitor	Z4	0.192" x 0.080" Microstrip
C12	13 pF, 100 mil Chip Capacitor	Z5, Z6	0.260" x 0.223" Microstrip
L1	26 nH, 4 Turn, Coilcraft	Z7	0.125" x 0.080" Microstrip
L2	5 nH, 2 Turn, Coilcraft	Z8	0.962" x 0.080" Microstrip
L3	33 nH, 5 Turn, Coilcraft	Z9	0.305" x 0.080" Microstrip
		Z10	0.155" x 0.080" Microstrip
		Board	Glass Teflon [®] , 31 mils, 2 oz. Copper

Figure 19. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

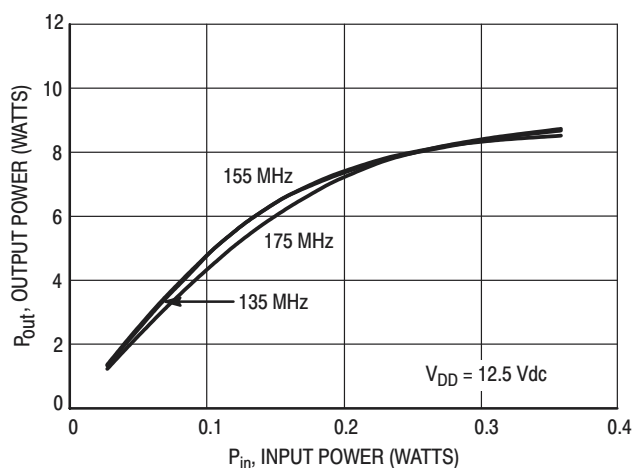


Figure 20. Output Power versus Input Power

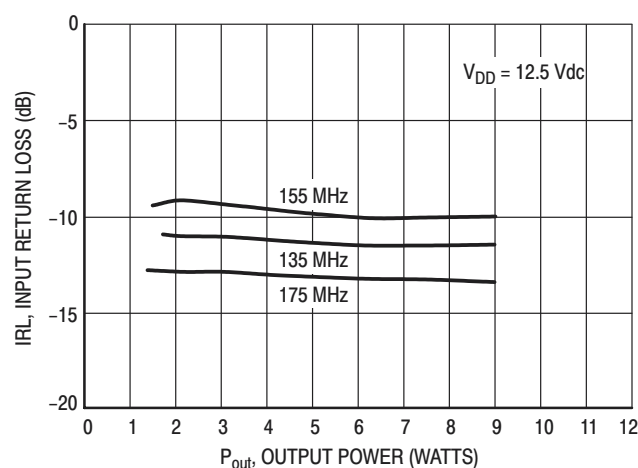


Figure 21. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 135 – 175 MHz

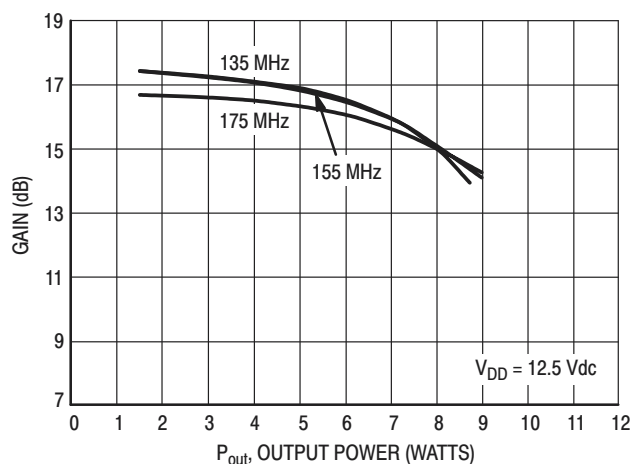


Figure 22. Gain versus Output Power

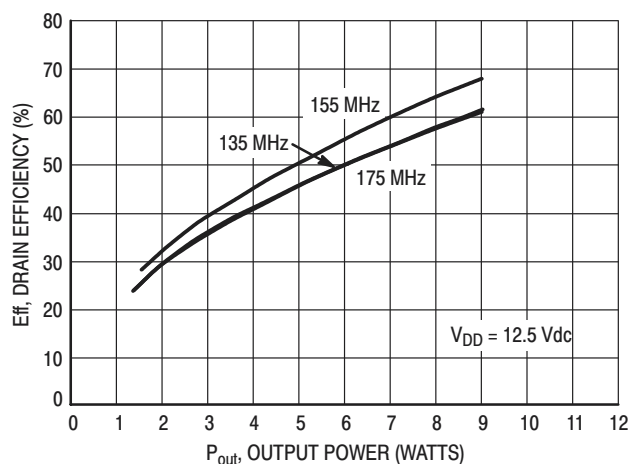


Figure 23. Drain Efficiency versus Output Power

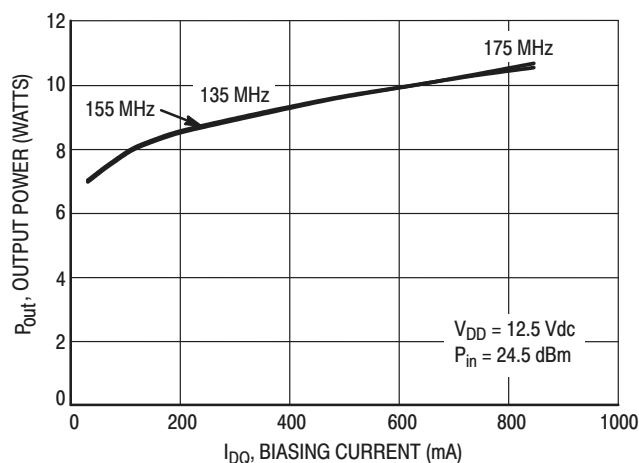


Figure 24. Output Power versus Biasing Current

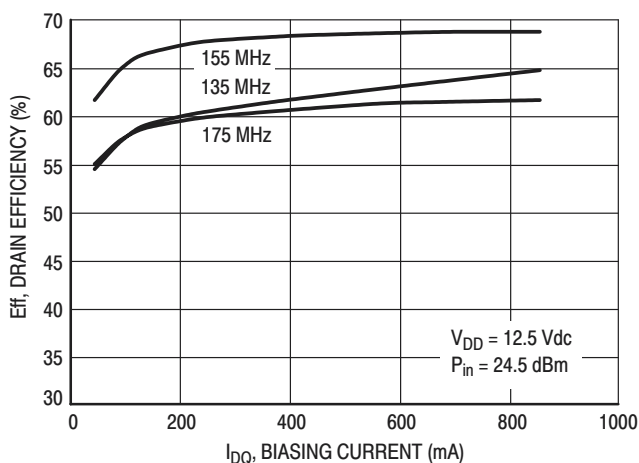


Figure 25. Drain Efficiency versus Biasing Current

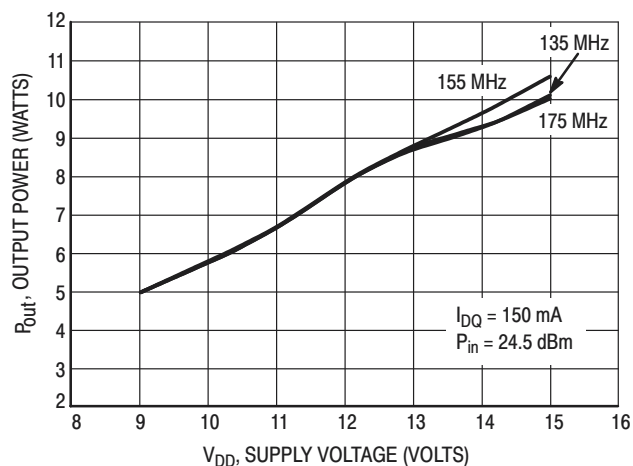


Figure 26. Output Power versus Supply Voltage

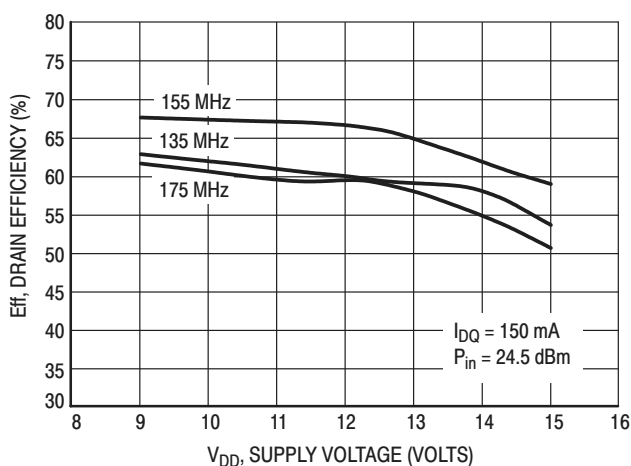
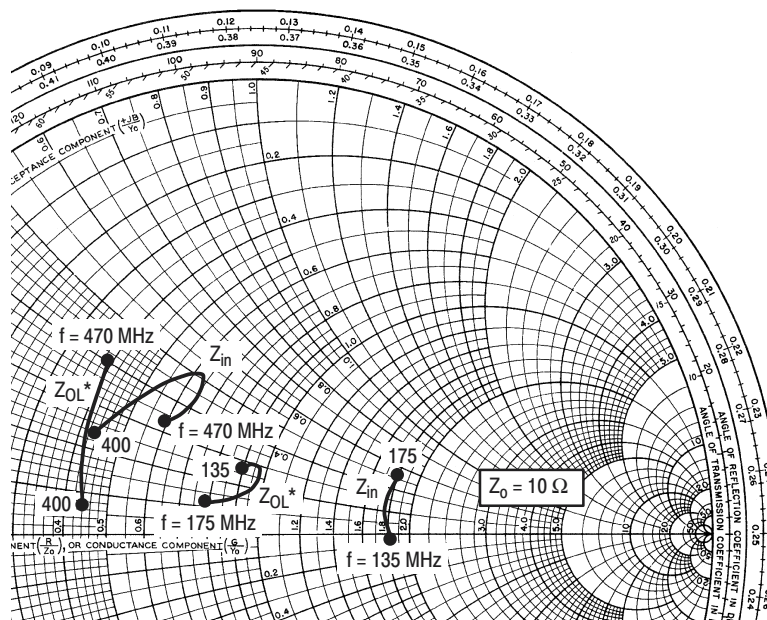
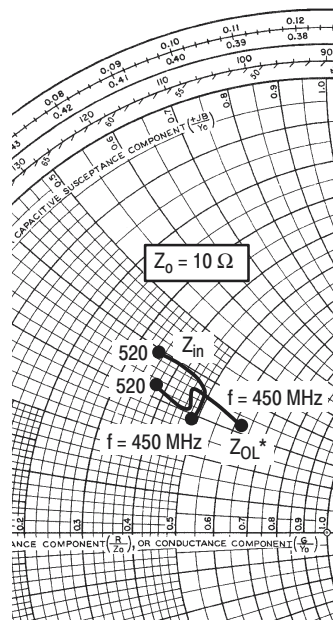


Figure 27. Drain Efficiency versus Supply Voltage



$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 150 \text{ mA}$, $P_{out} = 8 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
450	$4.9 + j2.85$	$6.42 + j3.23$
470	$4.85 + j3.71$	$4.59 + j3.61$
500	$4.63 + j3.84$	$4.72 + j3.12$
520	$3.52 + j3.92$	$3.81 + j3.27$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 150 \text{ mA}$, $P_{out} = 8 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
400	$4.28 + j2.36$	$4.41 + j0.67$
440	$6.45 + j5.13$	$4.14 + j2.53$
470	$5.91 + j3.34$	$3.92 + j4.02$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 150 \text{ mA}$, $P_{out} = 8 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
135	$18.31 - j0.76$	$8.97 + j2.62$
155	$17.72 + j1.85$	$9.69 + j2.81$
175	$18.06 + j5.23$	$7.94 + j1.14$

Z_{in} = Complex conjugate of source impedance with parallel 15Ω resistor and 82 pF capacitor in series with gate. (See Figure 1).

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Z_{in} = Complex conjugate of source impedance with parallel 15Ω resistor and 47 pF capacitor in series with gate. (See Figure 10).

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Z_{in} = Complex conjugate of source impedance with parallel 15Ω resistor and 43 pF capacitor in series with gate. (See Figure 19).

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

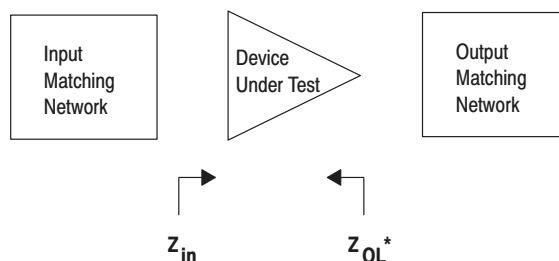


Figure 28. Series Equivalent Input and Output Impedance

Freescale Semiconductor, Inc.

Table 1. Common Source Scattering Parameters ($V_{DD} = 12.5$ Vdc)

$I_{DQ} = 150$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₂₁	∠φ	S ₁₂	∠φ	S ₂₂	∠φ
50	0.88	-148	18.91	99	0.033	11	0.67	-144
100	0.85	-163	9.40	86	0.033	-6	0.66	-158
200	0.85	-170	4.47	73	0.026	-17	0.69	-162
300	0.87	-171	2.72	64	0.025	-28	0.74	-163
400	0.88	-172	1.85	56	0.021	-21	0.79	-164
500	0.90	-173	1.35	52	0.019	-30	0.83	-165
600	0.92	-173	1.04	47	0.014	-26	0.85	-167
700	0.93	-174	0.83	44	0.015	-39	0.88	-168
800	0.94	-175	0.68	39	0.014	-31	0.90	-169
900	0.94	-175	0.55	36	0.010	-41	0.91	-170
1000	0.96	-176	0.46	30	0.011	-38	0.95	-170

$I_{DQ} = 800$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₂₁	∠φ	S ₁₂	∠φ	S ₂₂	∠φ
50	0.90	-159	20.80	97	0.020	14	0.73	-162
100	0.88	-169	10.35	88	0.018	1	0.74	-169
200	0.88	-174	5.09	79	0.017	-9	0.75	-171
300	0.89	-175	3.23	73	0.015	-18	0.77	-171
400	0.89	-175	2.30	67	0.015	-17	0.80	-171
500	0.90	-176	1.74	63	0.014	-22	0.82	-170
600	0.91	-176	1.39	59	0.014	-19	0.83	-171
700	0.92	-176	1.16	55	0.009	-23	0.85	-171
800	0.93	-176	0.96	50	0.011	-14	0.87	-172
900	0.94	-177	0.80	46	0.007	4	0.88	-173
1000	0.94	-177	0.67	41	0.010	-15	0.89	-173

$I_{DQ} = 1.5$ A

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠φ	S ₂₁	∠φ	S ₁₂	∠φ	S ₂₂	∠φ
50	0.91	-159	20.18	97	0.015	11	0.73	-165
100	0.89	-169	10.05	89	0.016	-5	0.74	-171
200	0.88	-174	4.93	80	0.015	-3	0.75	-172
300	0.89	-175	3.14	73	0.014	-14	0.78	-172
400	0.89	-176	2.24	67	0.014	-20	0.80	-171
500	0.90	-176	1.70	64	0.014	-22	0.82	-170
600	0.92	-176	1.36	59	0.010	-16	0.84	-171
700	0.92	-176	1.13	55	0.013	-10	0.85	-171
800	0.93	-177	0.94	50	0.008	-13	0.87	-172
900	0.94	-177	0.78	46	0.013	-26	0.87	-173
1000	0.94	-178	0.65	41	0.007	8	0.87	-172

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

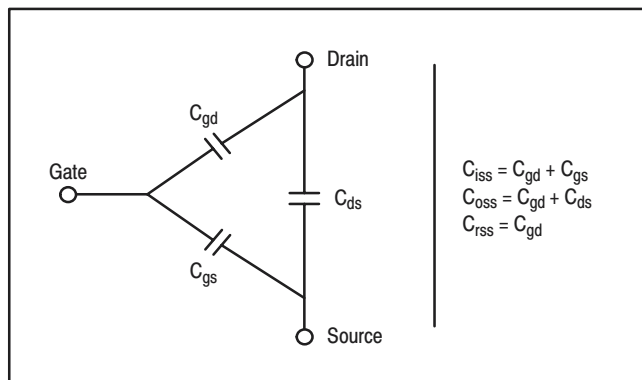
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high — on the order of $10^9 \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at $I_{DQ} = 150 \text{ mA}$, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

Freescale Semiconductor, Inc.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065" x 0.180" source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal

impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device's S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

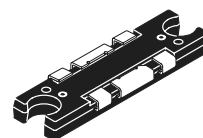
Designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts
 - Output Power — 35 Watts
 - Power Gain — 10.0 dB
 - Efficiency — 50%
- Capable of Handling 20:1 VSWR, @ 15.6 Vdc, 520 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Broadband-Full Power Across the Band: 135–175 MHz
400–470 MHz
450–520 MHz
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- In Tape and Reel. T1 Suffix = 500 Units per 44 mm, 13 inch Reel.

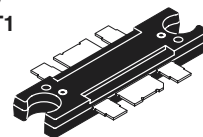
MRF1535T1

MRF1535FT1

520 MHz, 35 W, 12.5 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 1264-08, STYLE 1
TO-272
PLASTIC
MRF1535T1



CASE 1264A-02, STYLE 1
TO-272 STRAIGHT LEAD
PLASTIC
MRF1535FT1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	6	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ (1) Derate above 25°C	P_D	135 0.50	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.90	$^\circ\text{C/W}$

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

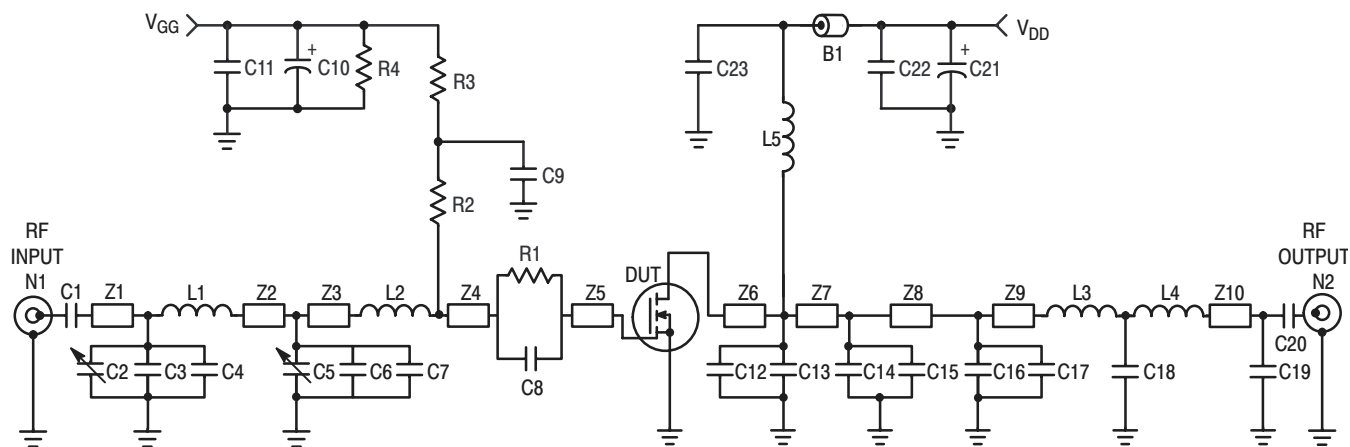
NOTE — CAUTION — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 100\text{ }\mu\text{Adc}$)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current ($V_{GS} = 10\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	0.3	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 12.5\text{ Vdc}$, $I_D = 400\text{ }\mu\text{A}$)	$V_{GS(th)}$	1	—	2.6	Vdc
Drain–Source On–Voltage ($V_{GS} = 5\text{ Vdc}$, $I_D = 0.6\text{ A}$)	$R_{DS(on)}$	—	—	0.7	Ω
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.0\text{ Adc}$)	$V_{DS(on)}$	—	—	1	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (Includes Input Matching Capacitance) ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{iss}	—	—	250	pF
Output Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{oss}	—	—	150	pF
Reverse Transfer Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{rss}	—	—	20	pF
RF CHARACTERISTICS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 35\text{ Watts}$, $I_{DQ} = 500\text{ mA}$) $f = 520\text{ MHz}$	G_{ps}	10	—	—	dB
Drain Efficiency ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 35\text{ Watts}$, $I_{DQ} = 500\text{ mA}$) $f = 520\text{ MHz}$	η	50	—	—	%
Load Mismatch ($V_{DD} = 15.6\text{ Vdc}$, $f = 520\text{ MHz}$, 2 dB Input Overdrive, VSWR 20:1 at All Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			

Freescale Semiconductor, Inc.



B1	Ferroxcube #VK200	L4	1 Turn, #26 AWG, 0.240" ID
C1, C9, C20, C23	330 pF, 100 mil Chip Capacitors	L5	4 Turn, #24 AWG, 0.180" ID
C2, C5	0 to 20 pF Trimmer Capacitors	N1, N2	Type N Flange Mounts
C3, C15	33 pF, 100 mil Chip Capacitors	R1	6.5 Ω , 1/4 W Chip Resistor
C4, C6, C19	18 pF, 100 mil Chip Capacitors	R2	39 Ω Chip Resistor (0805)
C7	160 pF, 100 mil Chip Capacitor	R3	1.2 k Ω , 1/8 W Chip Resistor
C8	240 pF, 100 mil Chip Capacitor	R4	33 k Ω , 1/4 W Chip Resistor
C10, C21	10 μ F, 50 V Electrolytic Capacitors	Z1	0.970" x 0.080" Microstrip
C11, C22	470 pF, 100 mil Chip Capacitors	Z2	0.380" x 0.080" Microstrip
C12, C13	150 pF, 100 mil Chip Capacitors	Z3	0.190" x 0.080" Microstrip
C14	110 pF, 100 mil Chip Capacitor	Z4	0.160" x 0.080" Microstrip
C16	68 pF, 100 mil Chip Capacitor	Z5, Z6	0.110" x 0.200" Microstrip
C17	120 pF, 100 mil Chip Capacitor	Z7	0.490" x 0.080" Microstrip
C18	51 pF, 100 mil Chip Capacitor	Z8	0.250" x 0.080" Microstrip
L1	17.5 nH, Coilcraft #A05T	Z9	0.320" x 0.080" Microstrip
L2	5 nH, Coilcraft #A02T	Z10	0.240" x 0.080" Microstrip
L3	1 Turn, #26 AWG, 0.250" ID	Board	Glass Teflon [®] , 31 mils

Figure 1. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

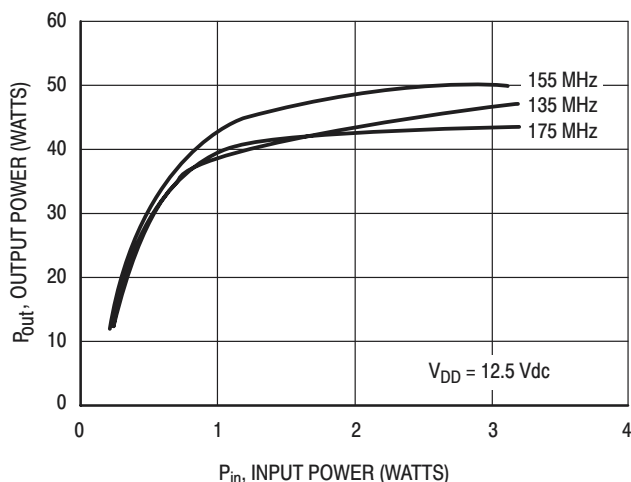


Figure 2. Output Power versus Input Power

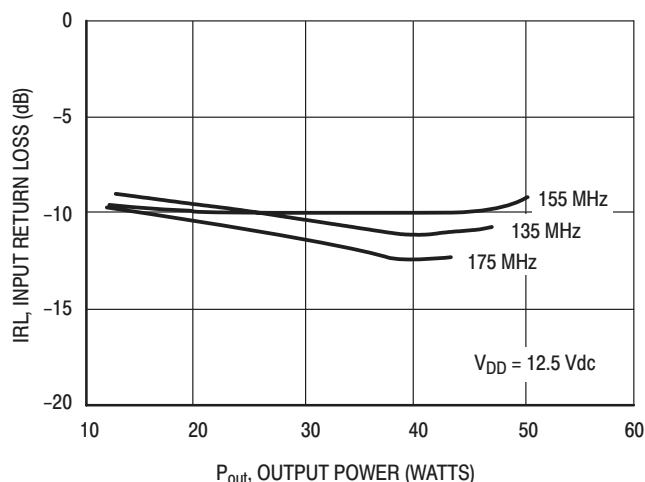


Figure 3. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 135 – 175 MHz

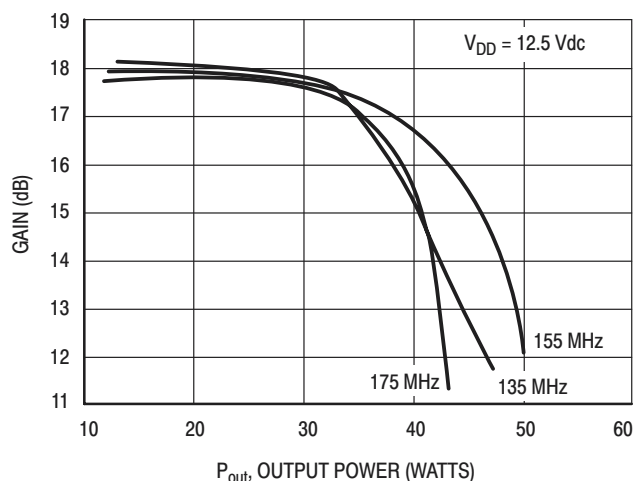


Figure 4. Gain versus Output Power

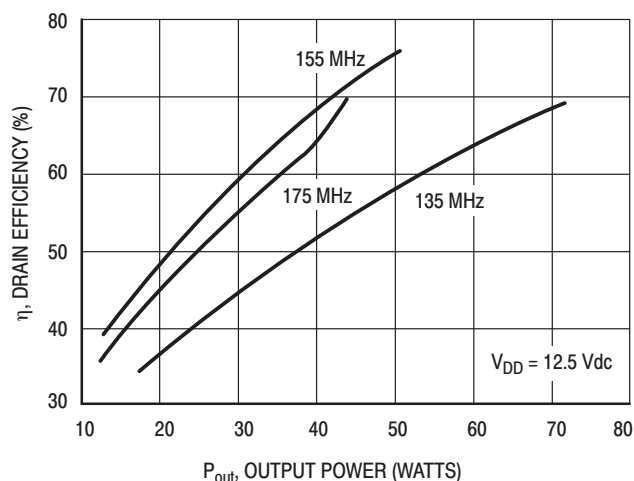


Figure 5. Drain Efficiency versus Output Power

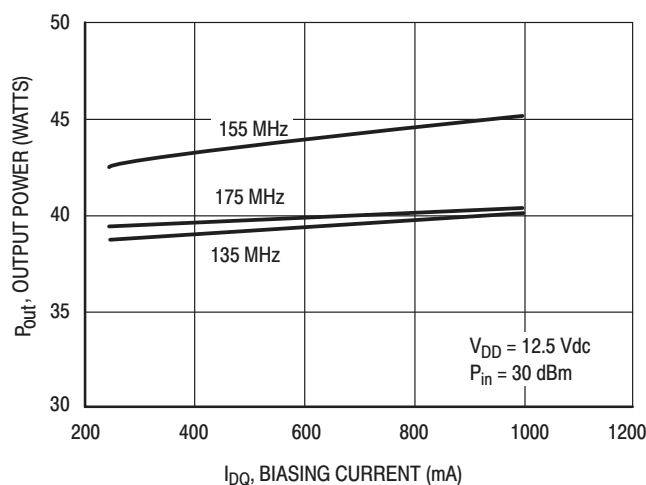


Figure 6. Output Power versus Biasing Current

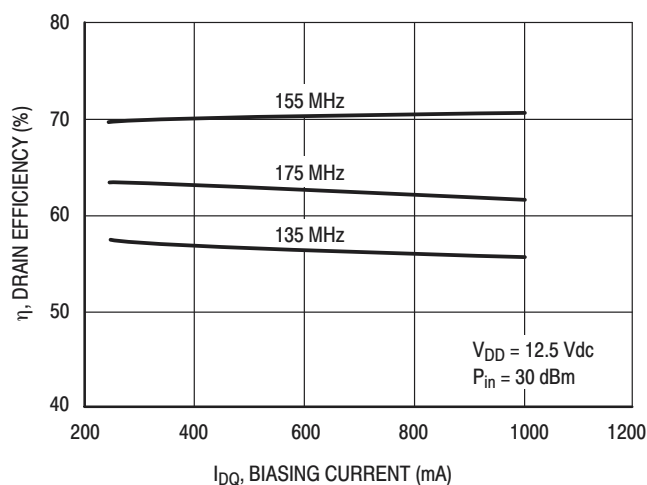


Figure 7. Drain Efficiency versus Biasing Current

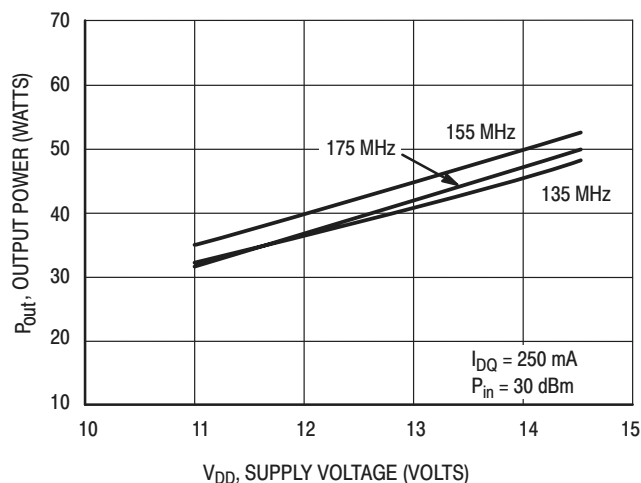


Figure 8. Output Power versus Supply Voltage

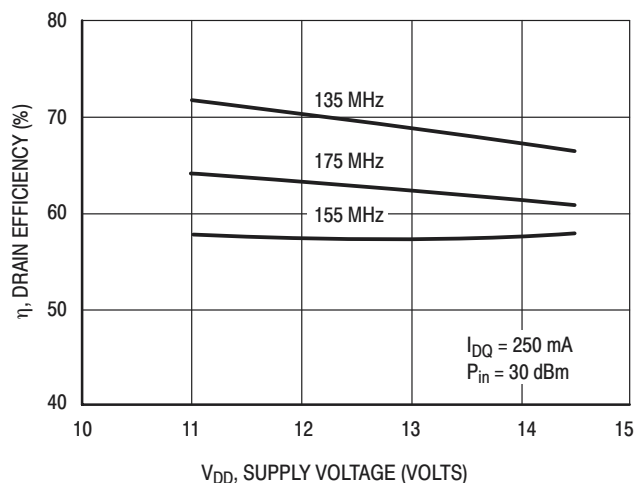
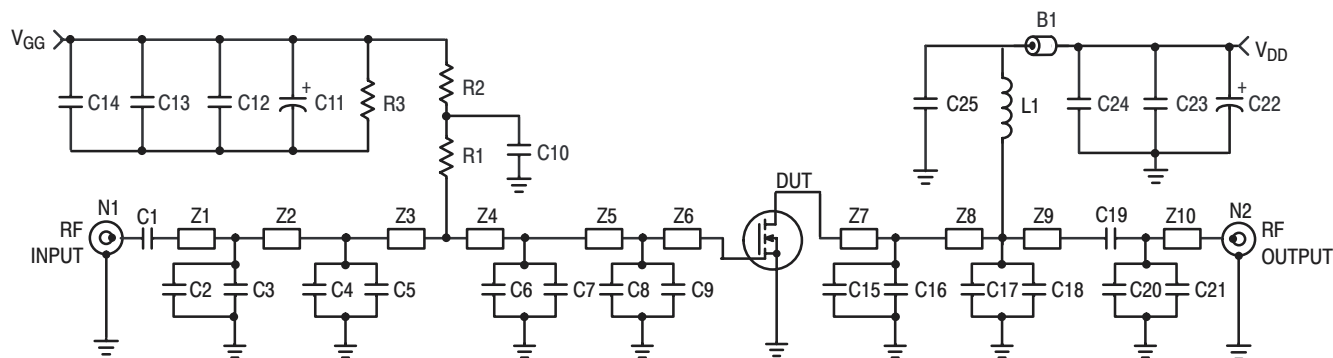


Figure 9. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1	Ferroxcube VK200	C21	1.8 pF, 100 mil Chip Capacitor
C1	160 pF, 100 mil Chip Capacitor	L1	47.5 nH, 5 Turn, Coilcraft
C2	3 pF, 100 mil Chip Capacitor	N1, N2	Type N Flange Mounts
C3	3.6 pF, 100 mil Chip Capacitor	R1	500 Ω Chip Resistor (0805)
C4	2.2 pF, 100 mil Chip Capacitor	R2	1 k Ω Chip Resistor (0805)
C5	10 pF, 100 mil Chip Capacitor	R3	33 k Ω , 1/8 W Chip Resistor
C6, C7	16 pF, 100 mil Chip Capacitors	Z1	0.480" x 0.080" Microstrip
C8, C15, C16	27 pF, 100 mil Chip Capacitors	Z2	1.070" x 0.080" Microstrip
C9	43 pF, 100 mil Chip Capacitor	Z3	0.290" x 0.080" Microstrip
C10, C14, C25	160 pF, 100 mil Chip Capacitors	Z4	0.160" x 0.080" Microstrip
C11, C22	10 μ F, 50 V Electrolytic Capacitors	Z5, Z8	0.120" x 0.080" Microstrip
C12, C24	1,200 pF, 100 mil Chip Capacitors	Z6, Z7	0.120" x 0.223" Microstrip
C13, C23	0.1 μ F, 100 mil Chip Capacitors	Z9	1.380" x 0.080" Microstrip
C17, C18	24 pF, 100 mil Chip Capacitors	Z10	0.625" x 0.080" Microstrip
C19	160 pF, 100 mil Chip Capacitor	Board	Glass Teflon [®] , 31 mils
C20	8.2 pF, 100 mil Chip Capacitor		

Figure 10. 450 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 – 520 MHz

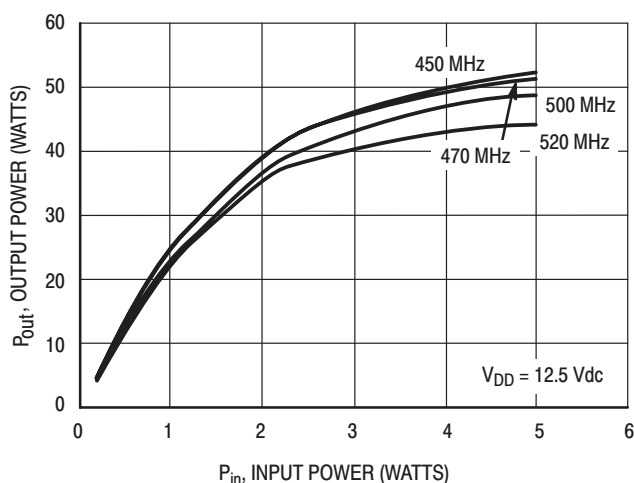


Figure 11. Output Power versus Input Power

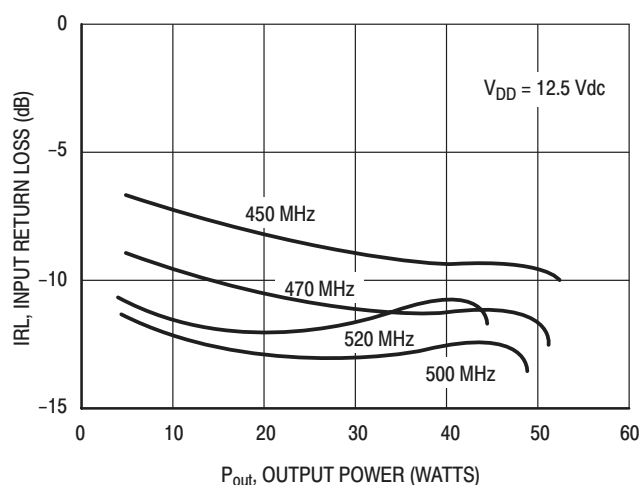


Figure 12. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 450 – 520 MHz

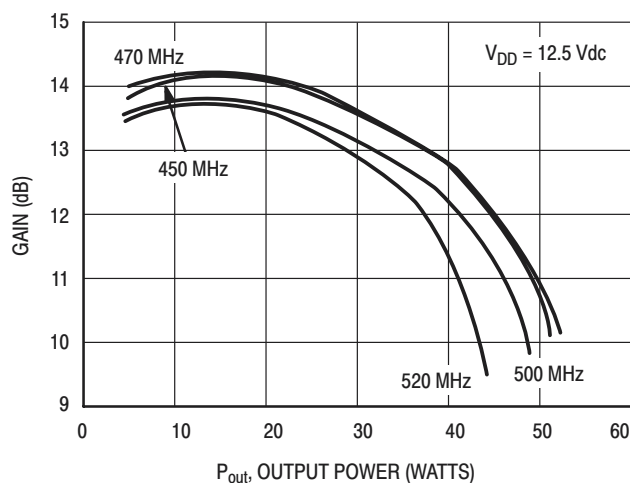


Figure 13. Gain versus Output Power

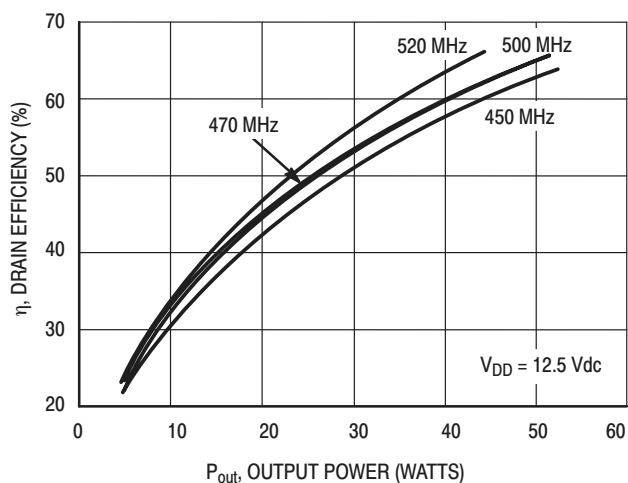


Figure 14. Drain Efficiency versus Output Power

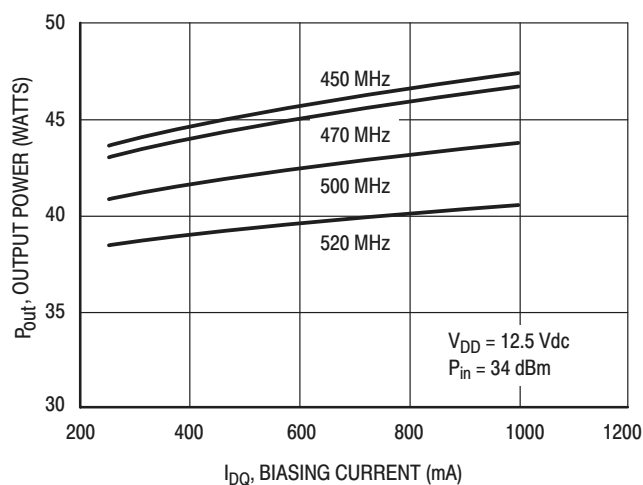


Figure 15. Output Power versus Biasing Current

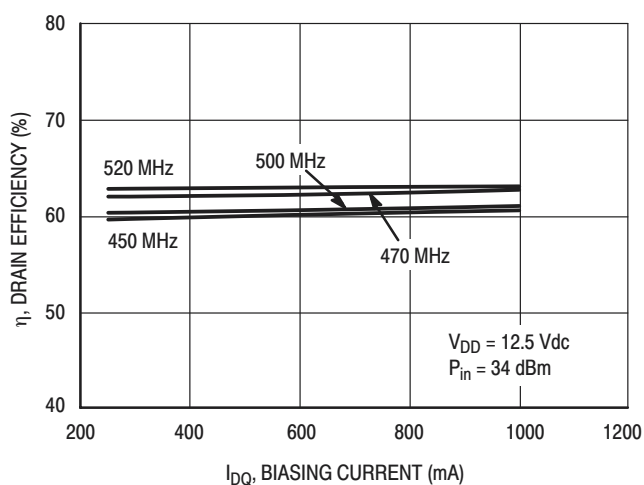


Figure 16. Drain Efficiency versus Biasing Current

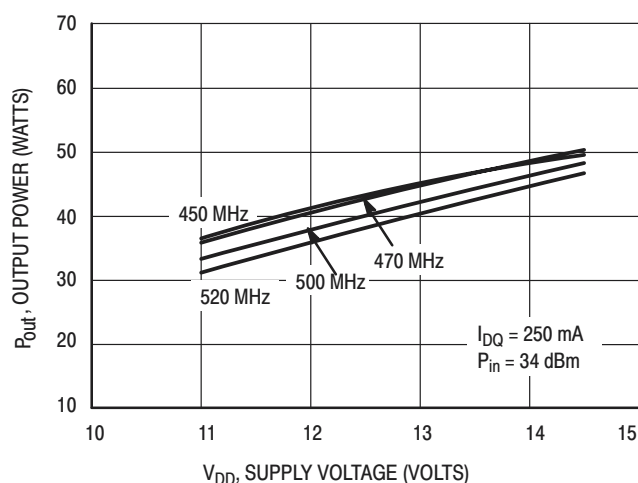


Figure 17. Output Power versus Supply Voltage

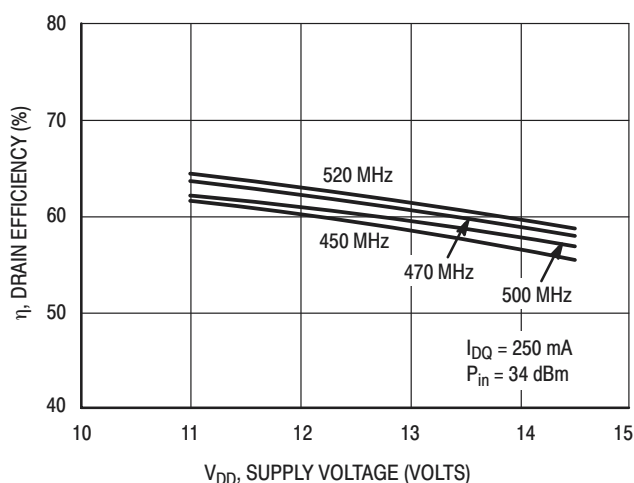
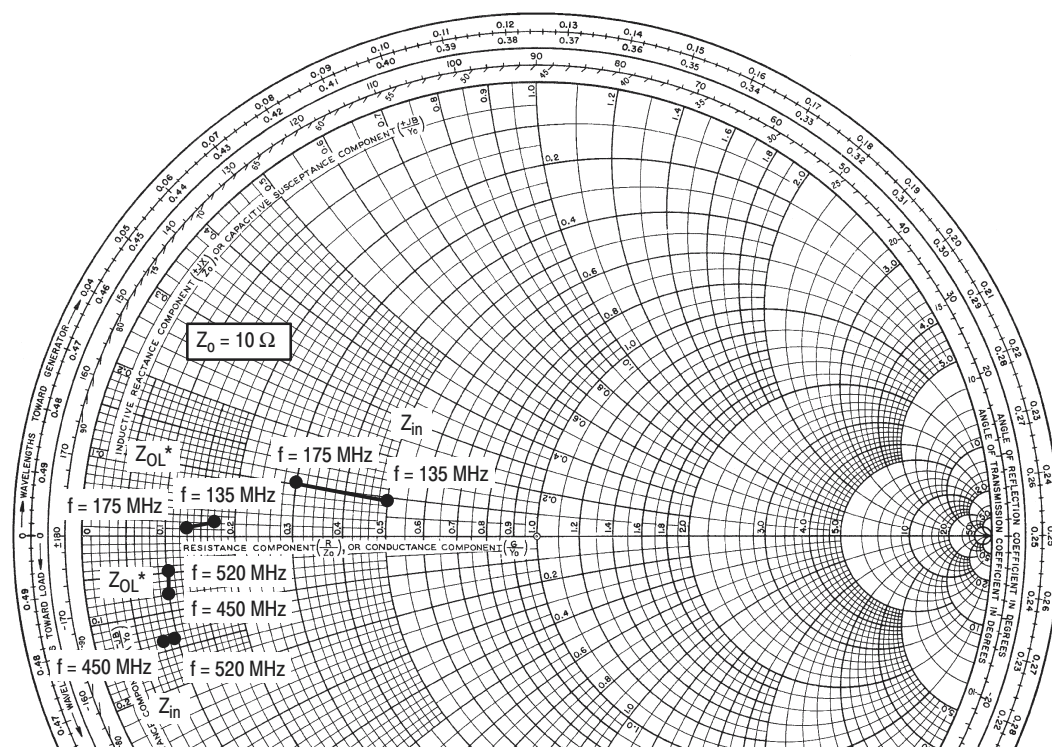


Figure 18. Drain Efficiency versus Supply Voltage



$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 35 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
135	$5.0 + j0.9$	$1.7 + j0.2$
155	$5.0 + j0.9$	$1.7 + j0.2$
175	$3.0 + j1.0$	$1.3 + j0.1$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 35 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
450	$0.8 - j1.4$	$1.0 - j0.8$
470	$0.9 - j1.4$	$1.1 - j0.6$
500	$1.0 - j1.4$	$1.1 - j0.6$
520	$0.9 - j1.4$	$1.1 - j0.5$

Z_{in} = Complex conjugate of source impedance.

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50\%$.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50\%$.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

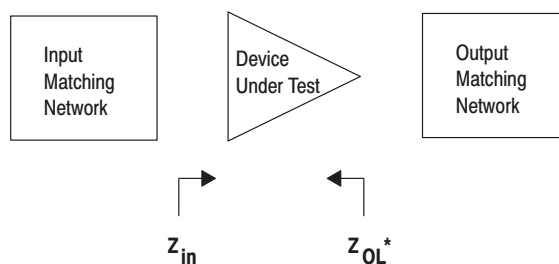


Figure 19. Series Equivalent Input and Output Impedance

Freescale Semiconductor, Inc.

Table 1. Common Source Scattering Parameters ($V_{DD} = 12.5$ Vdc)

$I_{DQ} = 250$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
50	0.89	-173	8.496	83	0.014	-26	0.76	-170
100	0.90	-175	3.936	72	0.014	-14	0.79	-170
150	0.91	-175	2.429	63	0.011	-23	0.82	-170
200	0.92	-175	1.627	57	0.010	-44	0.86	-170
250	0.94	-176	1.186	53	0.007	-16	0.88	-170
300	0.95	-176	0.888	49	0.005	-44	0.91	-171
350	0.96	-176	0.686	48	0.005	36	0.92	-170
400	0.96	-176	0.568	44	0.005	-1	0.94	-171
450	0.97	-176	0.457	44	0.004	49	0.94	-172
500	0.97	-176	0.394	44	0.003	-51	0.95	-171
550	0.98	-176	0.332	42	0.001	31	0.95	-173
600	0.98	-177	0.286	41	0.013	99	0.94	-173

$I_{DQ} = 1.0$ A

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
50	0.90	-173	8.49	83	0.006	-39	0.86	-176
100	0.90	-175	3.92	72	0.009	-5	0.86	-176
150	0.91	-175	2.44	63	0.006	7	0.87	-176
200	0.92	-175	1.62	57	0.008	21	0.88	-175
250	0.94	-176	1.19	53	0.006	8	0.89	-174
300	0.95	-176	0.89	48	0.008	3	0.89	-174
350	0.96	-176	0.69	48	0.007	48	0.91	-174
400	0.96	-176	0.57	44	0.004	41	0.93	-173
450	0.97	-176	0.46	44	0.004	43	0.93	-173
500	0.97	-176	0.39	44	0.003	57	0.94	-173
550	0.98	-176	0.33	41	0.006	62	0.94	-174
600	0.98	-177	0.28	41	0.009	96	0.93	-173

$I_{DQ} = 2.0$ A

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
50	0.94	-176	9.42	88	0.005	-72	0.89	-177
100	0.94	-178	4.56	82	0.005	4	0.89	-177
150	0.94	-178	2.99	78	0.003	7	0.89	-177
200	0.94	-178	2.14	74	0.005	17	0.90	-176
250	0.95	-178	1.67	71	0.004	40	0.90	-175
300	0.95	-178	1.32	67	0.007	35	0.91	-175
350	0.95	-178	1.08	67	0.005	57	0.92	-174
400	0.96	-178	0.93	63	0.003	50	0.93	-173
450	0.96	-178	0.78	62	0.007	68	0.93	-173
500	0.96	-177	0.68	61	0.004	99	0.94	-173
550	0.97	-177	0.59	58	0.008	78	0.93	-175
600	0.97	-178	0.51	57	0.009	92	0.92	-174

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF mobile power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

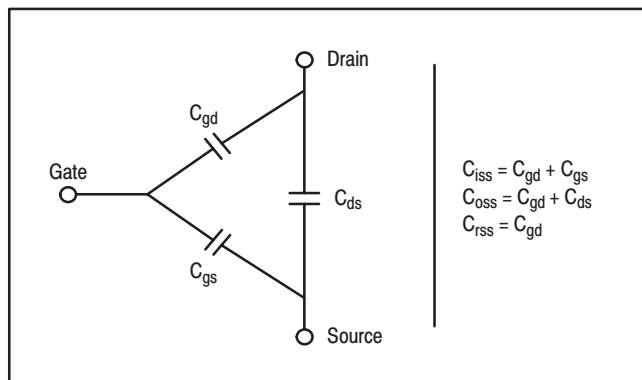
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high — on the order of $10^9 \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at $I_{DQ} = 150 \text{ mA}$, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

Freescale Semiconductor, Inc.

MOUNTING

The specified maximum thermal resistance of 0.9°C/W assumes a majority of the 0.170" x 0.608" source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal

impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device's S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

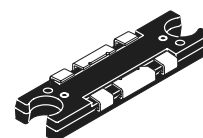
Designed for broadband commercial and industrial applications with frequencies to 175 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 175 MHz, 12.5 Volts
 - Output Power — 50 Watts
 - Power Gain — 12 dB
 - Efficiency — 50%
- Capable of Handling 20:1 VSWR, @ 15.6 Vdc, 175 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Broadband-Full Power Across the Band: 135–175 MHz
- Broadband Demonstration Amplifier Information Available Upon Request
- In Tape and Reel. T1 Suffix = 500 Units per 44 mm, 13 inch Reel.

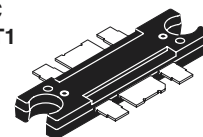
MRF1550T1

MRF1550FT1

175 MHz, 50 W, 12.5 V
 LATERAL N-CHANNEL
 BROADBAND
 RF POWER MOSFETs



CASE 1264-08, STYLE 1
 TO-272
 PLASTIC
 MRF1550T1



CASE 1264A-02, STYLE 1
 TO-272 STRAIGHT LEAD
 PLASTIC
 MRF1550FT1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	12	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ (1) Derate above 25°C	P_D	165 0.50	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.75	$^\circ\text{C}/\text{W}$

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

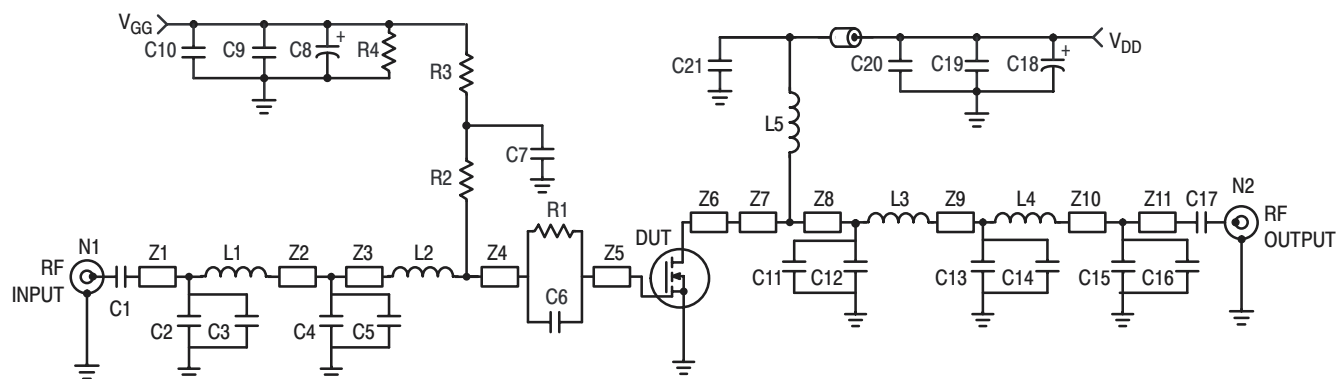
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Current ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μA_{dc}
Gate–Source Leakage Current ($V_{GS} = 10\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	0.5	μA_{dc}
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 12.5\text{ Vdc}$, $I_D = 800\text{ }\mu\text{A}$)	$V_{GS(th)}$	1	—	3	Vdc
Drain–Source On–Voltage ($V_{GS} = 5\text{ Vdc}$, $I_D = 1.2\text{ A}$)	$R_{DS(on)}$	—	—	0.5	Ω
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 4.0\text{ A}$)	$V_{DS(on)}$	—	—	1	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (Includes Input Matching Capacitance) ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{iss}	—	—	500	pF
Output Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{oss}	—	—	250	pF
Reverse Transfer Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{rss}	—	—	35	pF
RF CHARACTERISTICS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 50\text{ Watts}$, $I_{DQ} = 500\text{ mA}$) $f = 175\text{ MHz}$	G_{ps}	10	—	—	dB
Drain Efficiency ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 50\text{ Watts}$, $I_{DQ} = 500\text{ mA}$) $f = 175\text{ MHz}$	η	50	—	—	%
Load Mismatch ($V_{DD} = 15.6\text{ Vdc}$, $f = 175\text{ MHz}$, 2 dB Input Overdrive, VSWR 20:1 at All Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			

Freescale Semiconductor, Inc.



B1	Ferroxcube #VK200	L4	1 Turn, #26 AWG, 0.240" ID
C1	180 pF, 100 mil Chip Capacitor	L5	3 Turn, #24 AWG, 0.180" ID
C2	10 pF, 100 mil Chip Capacitor	N1, N2	Type N Flange Mounts
C3	33 pF, 100 mil Chip Capacitor	R1	5.1 Ω , 1/4 W Chip Resistor
C4, C16	24 pF, 100 mil Chip Capacitors	R2	39 Ω Chip Resistor (0805)
C5	160 pF, 100 mil Chip Capacitor	R3	1 k Ω , 1/8 W Chip Resistor
C6	240 pF, 100 mil Chip Capacitor	R4	33 k Ω , 1/4 W Chip Resistor
C7, C17	300 pF, 100 mil Chip Capacitors	Z1	1.000" x 0.080" Microstrip
C8, C18	10 μ F, 50 V Electrolytic Capacitors	Z2	0.400" x 0.080" Microstrip
C9, C19	0.1 μ F, 100 mil Chip Capacitors	Z3	0.200" x 0.080" Microstrip
C10	470 pF, 100 mil Chip Capacitor	Z4	0.200" x 0.080" Microstrip
C11, C12	200 pF, 100 mil Chip Capacitors	Z5, Z6	0.100" x 0.223" Microstrip
C13	22 pF, 100 mil Chip Capacitor	Z7	0.160" x 0.080" Microstrip
C14	30 pF, 100 mil Chip Capacitor	Z8	0.260" x 0.080" Microstrip
C15	6.8 pF, 100 mil Chip Capacitor	Z9	0.280" x 0.080" Microstrip
C20	1,000 pF, 100 mil Chip Capacitor	Z10	0.270" x 0.080" Microstrip
L1	18.5 nH, Coilcraft #A05T	Z11	0.730" x 0.080" Microstrip
L2	5 nH, Coilcraft #A02T	Board	Glass Teflon [®] , 31 mils
L3	1 Turn, #24 AWG, 0.250" ID		

Figure 1. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS

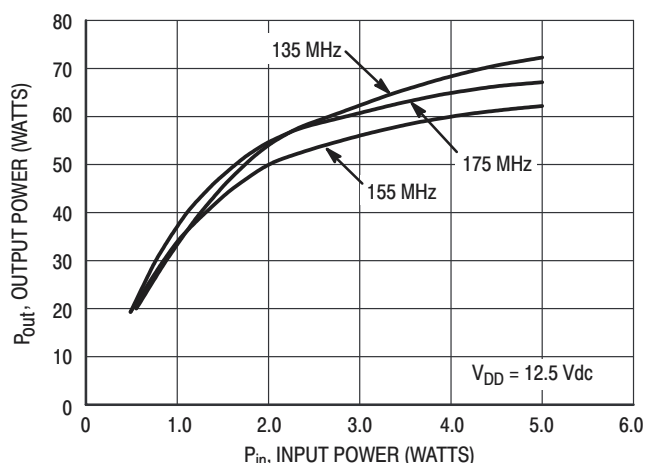


Figure 2. Output Power versus Input Power

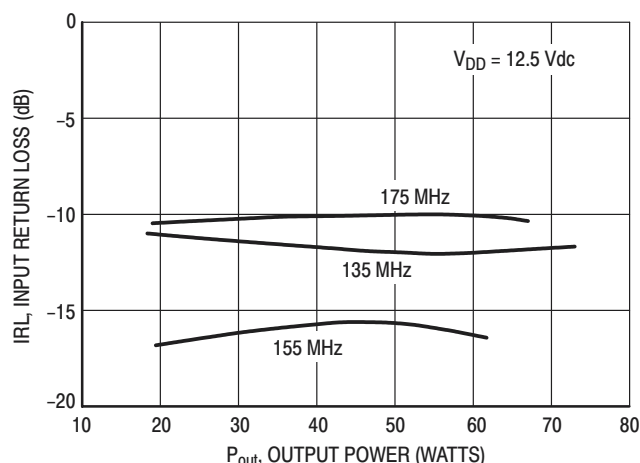


Figure 3. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

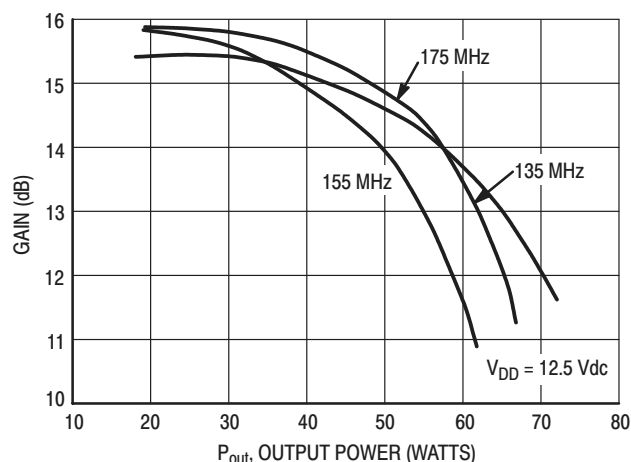


Figure 4. Gain versus Output Power

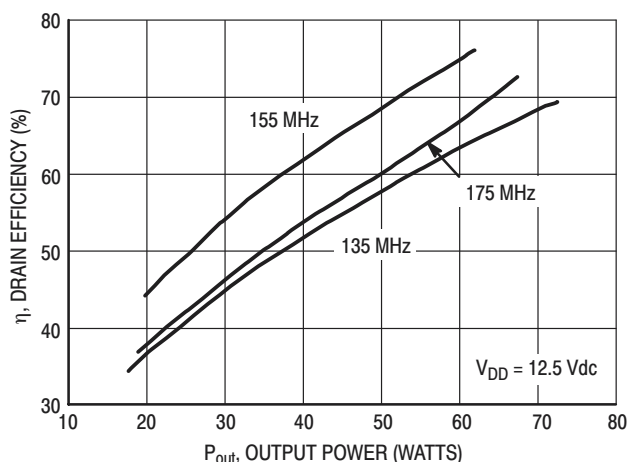


Figure 5. Drain Efficiency versus Output Power

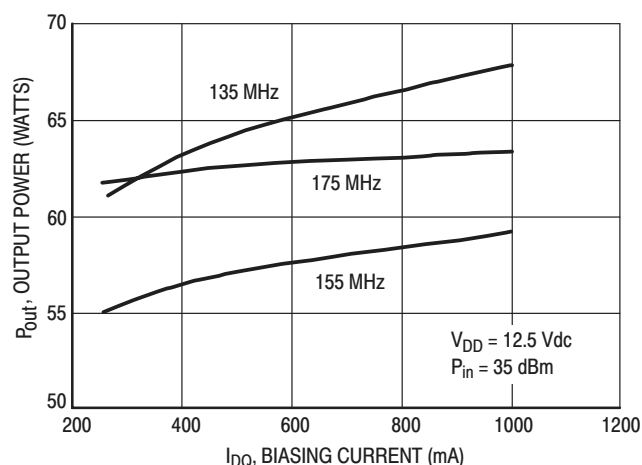


Figure 6. Output Power versus Biasing Current

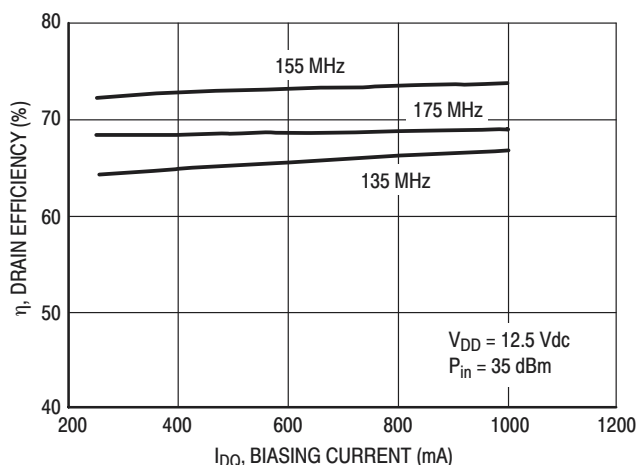


Figure 7. Drain Efficiency versus Biasing Current

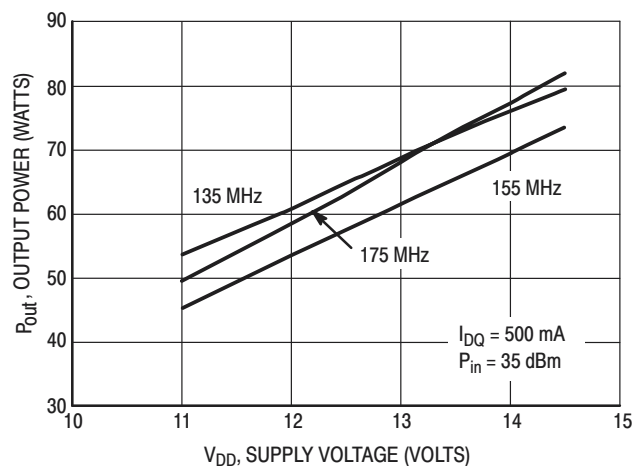


Figure 8. Output Power versus Supply Voltage

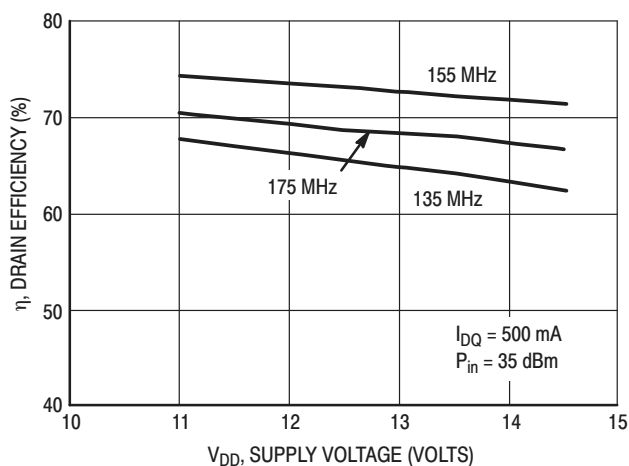
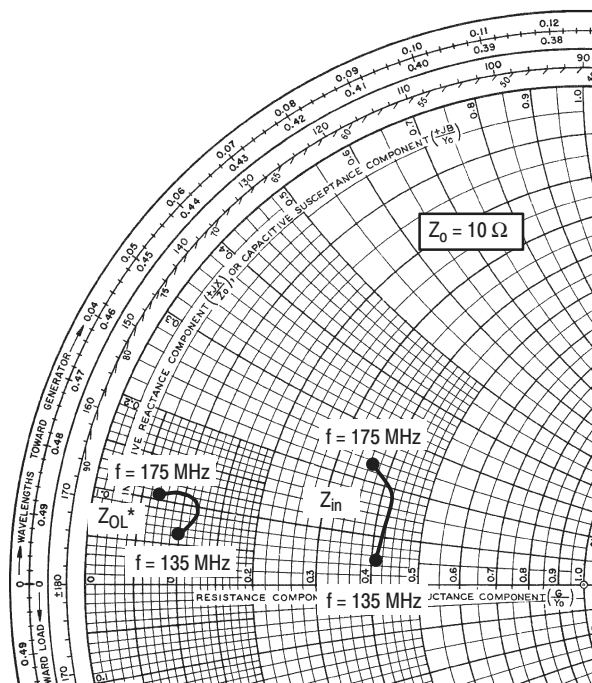


Figure 9. Drain Efficiency versus Supply Voltage



$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 50 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
135	$4.1 + j0.5$	$1.0 + j0.6$
155	$4.2 + j1.7$	$1.2 + j.09$
175	$3.7 + j2.3$	$0.7 + j1.1$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

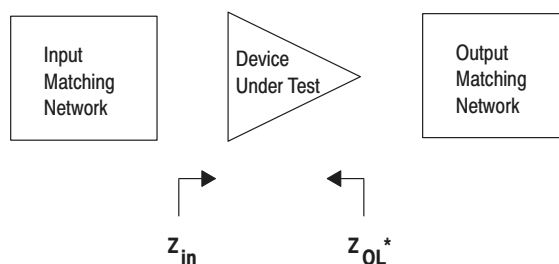


Figure 10. Series Equivalent Input and Output Impedance

Freescale Semiconductor, Inc.

Table 1. Common Source Scattering Parameters ($V_{DD} = 12.5$ Vdc)

$I_{DQ} = 500$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
50	0.93	-178	4.817	80	0.009	-39	0.86	-176
100	0.94	-178	2.212	69	0.009	-3	0.88	-175
150	0.95	-178	1.349	61	0.008	-8	0.90	-174
200	0.95	-178	0.892	54	0.006	-13	0.92	-174
250	0.96	-178	0.648	51	0.005	-7	0.93	-174
300	0.97	-178	0.481	47	0.004	-8	0.95	-174
350	0.97	-178	0.370	46	0.005	4	0.95	-174
400	0.98	-178	0.304	43	0.001	15	0.97	-174
450	0.98	-178	0.245	43	0.005	81	0.97	-174
500	0.98	-178	0.209	43	0.003	84	0.97	-174
550	0.99	-177	0.178	41	0.007	70	0.98	-175
600	0.98	-178	0.149	41	0.010	106	0.96	-175

$I_{DQ} = 2.0$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
50	0.93	-177	4.81	80	0.003	-119	0.93	-178
100	0.94	-178	2.20	69	0.006	4	0.93	-178
150	0.95	-178	1.35	61	0.003	-1	0.93	-177
200	0.95	-178	0.89	54	0.004	18	0.93	-176
250	0.96	-178	0.65	51	0.001	28	0.94	-176
300	0.97	-178	0.48	47	0.004	77	0.94	-175
350	0.97	-178	0.37	46	0.006	85	0.95	-175
400	0.98	-178	0.30	43	0.007	53	0.96	-174
450	0.98	-178	0.25	43	0.006	74	0.97	-174
500	0.98	-177	0.21	44	0.006	84	0.97	-174
550	0.99	-177	0.18	41	0.002	106	0.97	-175
600	0.98	-178	0.15	41	0.004	116	0.96	-174

$I_{DQ} = 4.0$ mA

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
50	0.97	-179	5.04	87	0.002	-116	0.94	-179
100	0.96	-179	2.43	82	0.006	42	0.94	-178
150	0.96	-179	1.60	77	0.004	13	0.94	-177
200	0.96	-179	1.14	74	0.003	43	0.95	-176
250	0.97	-179	0.89	71	0.004	65	0.95	-175
300	0.97	-179	0.71	68	0.006	68	0.95	-175
350	0.97	-179	0.57	67	0.006	74	0.97	-174

Freescale Semiconductor, Inc.

Table 1. Common Source Scattering Parameters ($V_{DD} = 12.5$ Vdc) (continued)

$I_{DQ} = 4.0$ mA (continued)

f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
400	0.97	−179	0.49	63	0.005	58	0.97	−173
450	0.98	−178	0.41	63	0.005	73	0.98	−173
500	0.98	−178	0.36	62	0.003	128	0.98	−173
550	0.98	−178	0.32	58	0.004	57	0.99	−174
600	0.98	−178	0.27	58	0.009	83	0.98	−174

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF mobile power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

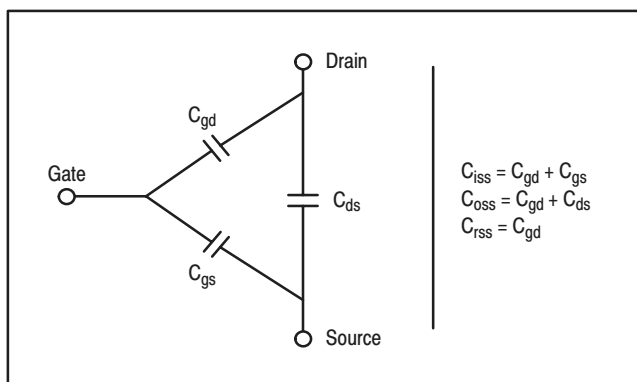
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.

**DRAIN CHARACTERISTICS**

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of $10^9 \Omega$ – resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at $I_{DQ} = 150 \text{ mA}$, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of $0.75^{\circ}\text{C}/\text{W}$ assumes a majority of the $0.170'' \times 0.608''$ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal

impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device's S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

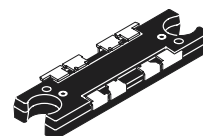
RF Power Field Effect Transistors N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 470 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 12.5 volt mobile FM equipment.

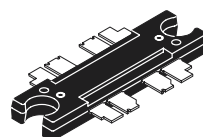
- Specified Performance @ 470 MHz, 12.5 Volts
 - Output Power — 70 Watts
 - Power Gain — 10 dB
 - Efficiency — 50%
- Capable of Handling 20:1 VSWR, @ 15.6 Vdc, 470 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Broadband-Full Power Across the Band: 135–175 MHz
400–470 MHz
- Broadband Demonstration Amplifier Information Available Upon Request
- Available in Tape and Reel. T1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MRF1570T1
MRF1570FT1

470 MHz, 70 W, 12.5 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 1366-03, STYLE 1
TO-272 SPLIT LEAD
PLASTIC
MRF1570T1



CASE 1366A-02, STYLE 1
TO-272 STRAIGHT LEAD
PLASTIC
MRF1570FT1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	40	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	165 0.5	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	175	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)
Charge Device Model	C2 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.75	$^\circ\text{C}/\text{W}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Current ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μA
---	-----------	---	---	---	---------------

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = 12.5\text{ Vdc}$, $I_D = 0.8\text{ mAdc}$)	$V_{GS(th)}$	1.0	—	3	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.0\text{ Adc}$)	$V_{DS(on)}$	—	—	1	Vdc

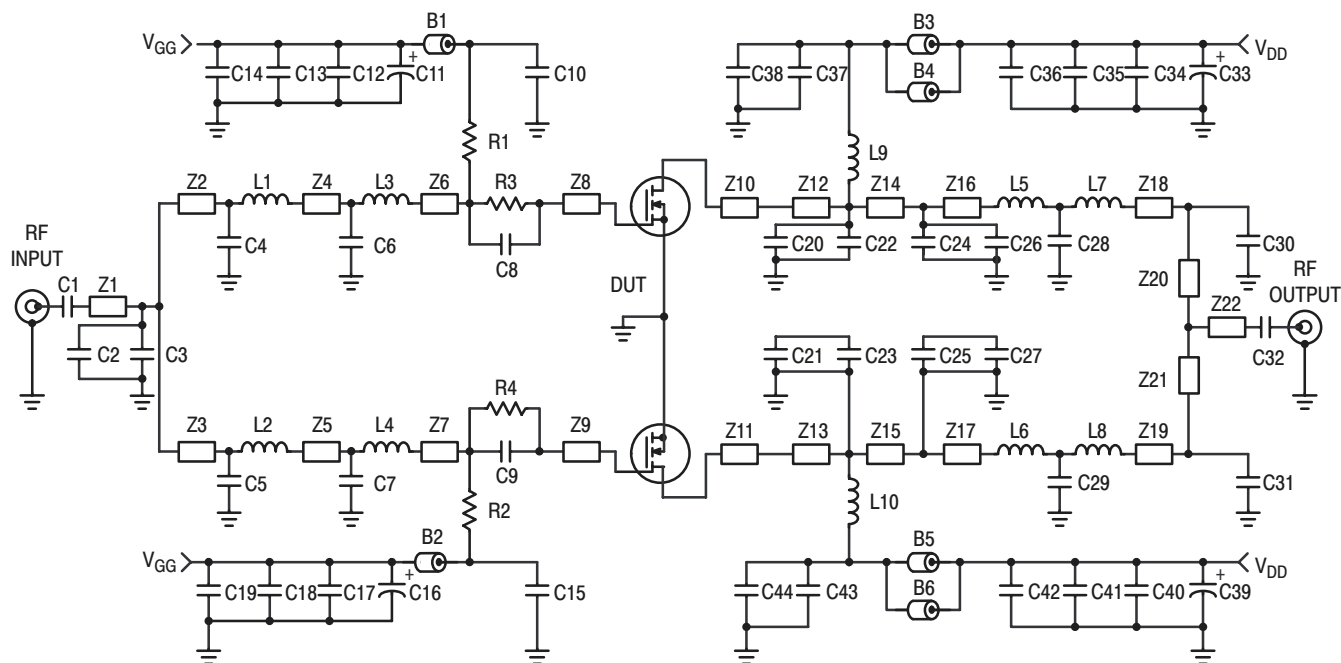
DYNAMIC CHARACTERISTICS

Input Capacitance (Includes Input Matching Capacitance) ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{iss}	—	—	500	pF
Output Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{oss}	—	—	250	pF
Reverse Transfer Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{rss}	—	—	35	pF

RF CHARACTERISTICS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 70\text{ W}$, $I_{DQ} = 800\text{ mA}$) $f = 470\text{ MHz}$	G_{ps}	10	—	—	dB
Drain Efficiency ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 70\text{ W}$, $I_{DQ} = 800\text{ mA}$) $f = 470\text{ MHz}$	η	50	—	—	%
Load Mismatch ($V_{DD} = 15.6\text{ Vdc}$, $f = 470\text{ MHz}$, 2 dB Input Overdrive, VSWR 20:1 at All Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			

Freescale Semiconductor, Inc.



B1, B2, B3, B4, B5, B6	Long Ferrite Beads, Fair Rite Products
C1, C32, C37, C43	270 pF, 100 mil Chip Capacitors
C2, C20, C21	33 pF, 100 mil Chip Capacitors
C3	18 pF, 100 mil Chip Capacitor
C4, C5	30 pF, 100 mil Chip Capacitors
C6, C7	180 pF, 100 mil Chip Capacitors
C8, C9	150 pF, 100 mil Chip Capacitors
C10, C15	300 pF, 100 mil Chip Capacitors
C11, C16, C33, C39	10 μ F, 50 V Electrolytic Capacitors
C12, C17, C34, C40	0.1 μ F, 100 mil Chip Capacitors
C13, C18, C35, C41	1000 pF, 100 mil Chip Capacitors
C14, C19, C36, C42	470 pF, 100 mil Chip Capacitors
C22, C23	110 pF, 100 mil Chip Capacitors
C24, C25	68 pF, 100 mil Chip Capacitors
C26, C27	120 pF, 100 mil Chip Capacitors
C28, C29	24 pF, 100 mil Chip Capacitors
C30, C31	27 pF, 100 mil Chip Capacitors
C38, C44	240 pF, 100 mil Chip Capacitors
L1, L2	17.5 nH, 6 Turn Inductors, Coilcraft

L3, L4	5 nH, 2 Turn Inductors, Coilcraft
L5, L6, L7, L8	1 Turn, #18 AWG, 0.33" ID Inductors
L9, L10	3 Turn, #16 AWG, 0.165" ID Inductors
N1, N2	Type N Flange Mounts
R1, R2	25.5 Ω Chip Resistors (1206)
R3, R4	9.3 Ω Chip Resistors (1206)
Z1	0.32" x 0.080" Microstrip
Z2, Z3	0.46" x 0.080" Microstrip
Z4, Z5	0.34" x 0.080" Microstrip
Z6, Z7	0.45" x 0.080" Microstrip
Z8, Z9, Z10, Z11	0.28" x 0.240" Microstrip
Z12, Z13	0.39" x 0.080" Microstrip
Z14, Z15	0.27" x 0.080" Microstrip
Z16, Z17	0.25" x 0.080" Microstrip
Z18, Z19	0.29" x 0.080" Microstrip
Z20, Z21	0.14" x 0.080" Microstrip
Z22	0.32" x 0.080" Microstrip
Board	31 mil Glass Teflon [®]

Figure 1. 135 – 175 MHz Broadband Test Circuit Schematic

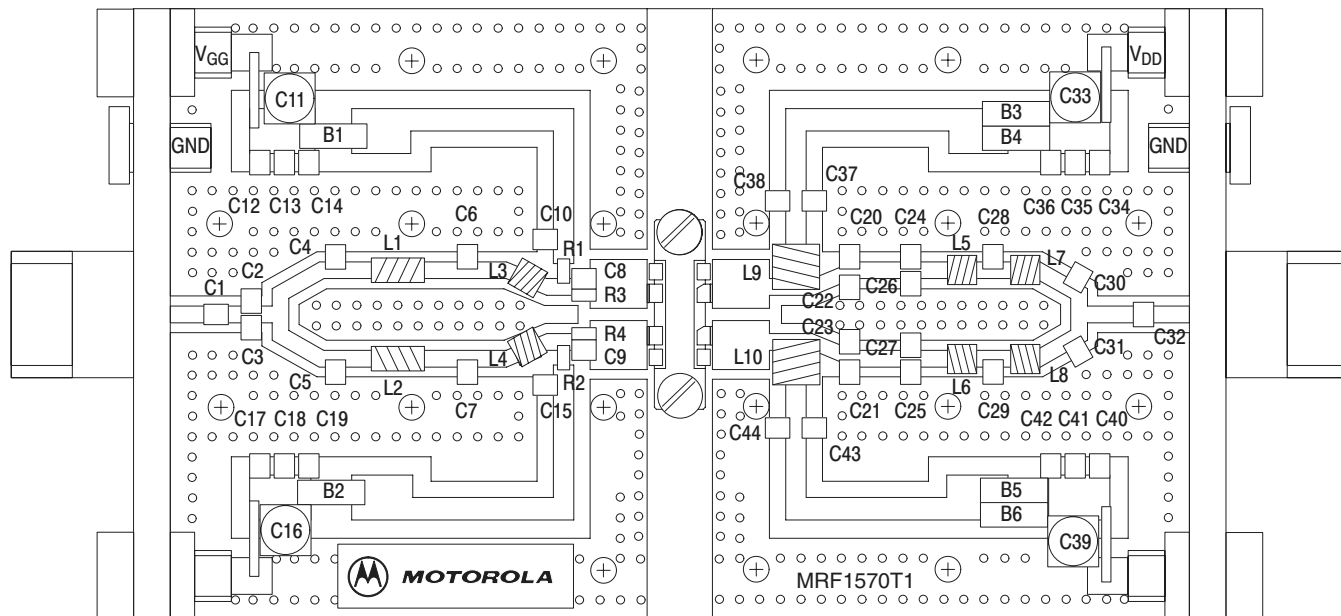


Figure 2. 135 – 175 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS, 135 – 175 MHz

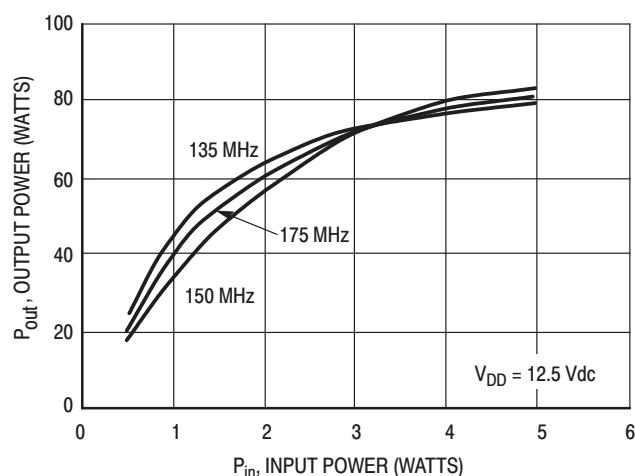


Figure 3. Output Power versus Input Power

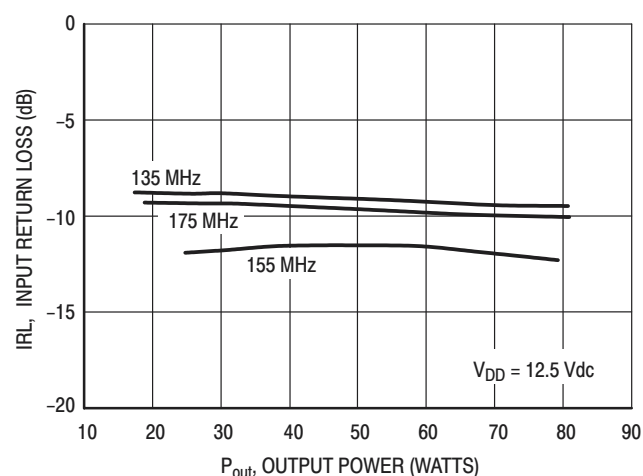


Figure 4. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 135 – 175 MHz

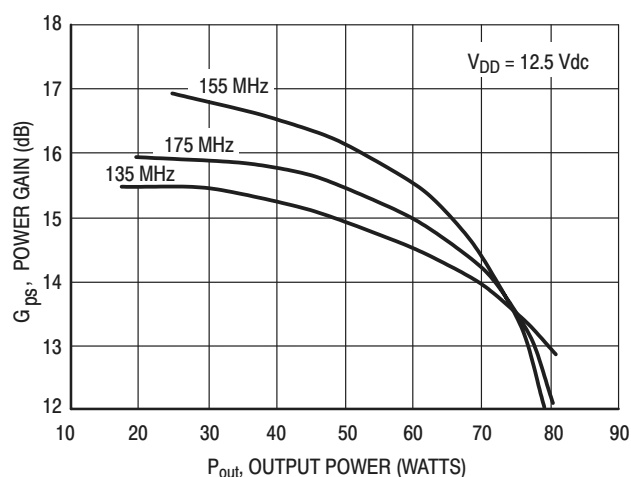


Figure 5. Gain versus Output Power

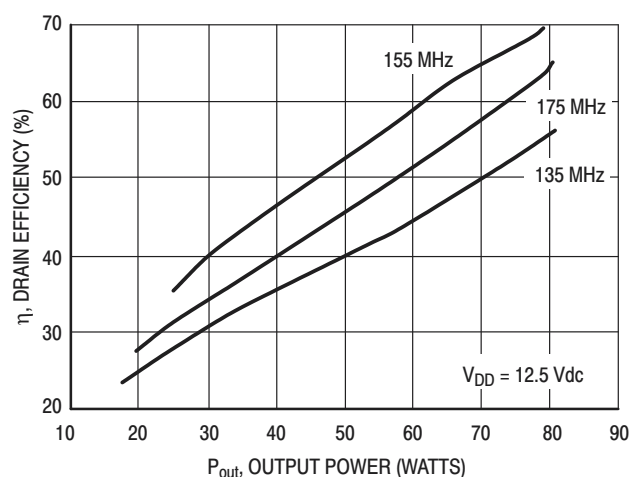


Figure 6. Drain Efficiency versus Output Power

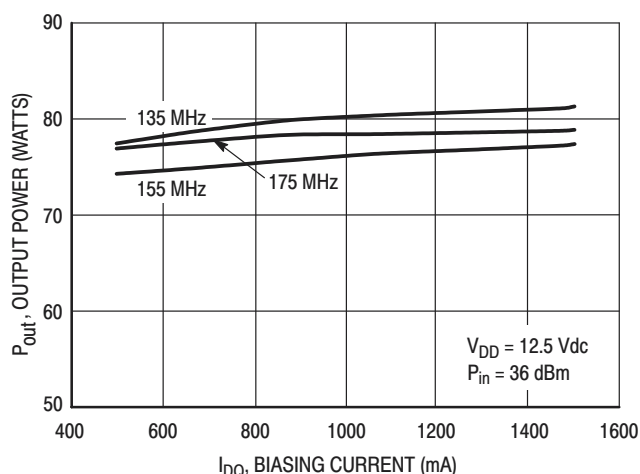


Figure 7. Output Power versus Biasing Current

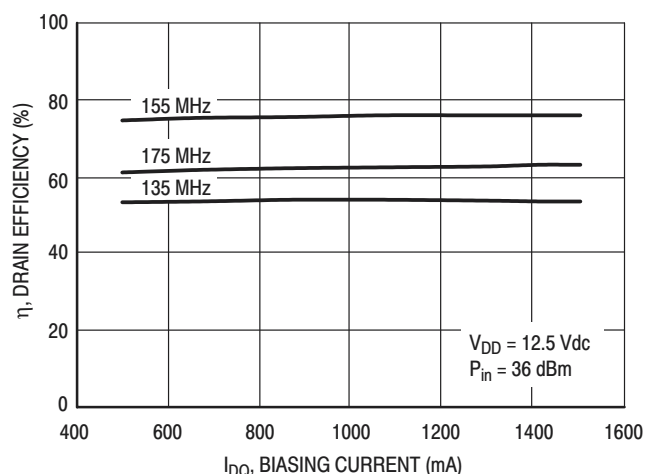


Figure 8. Drain Efficiency versus Biasing Current

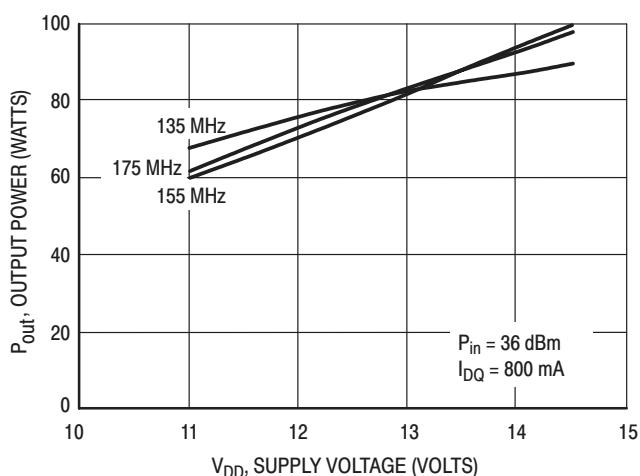


Figure 9. Output Power versus Supply Voltage

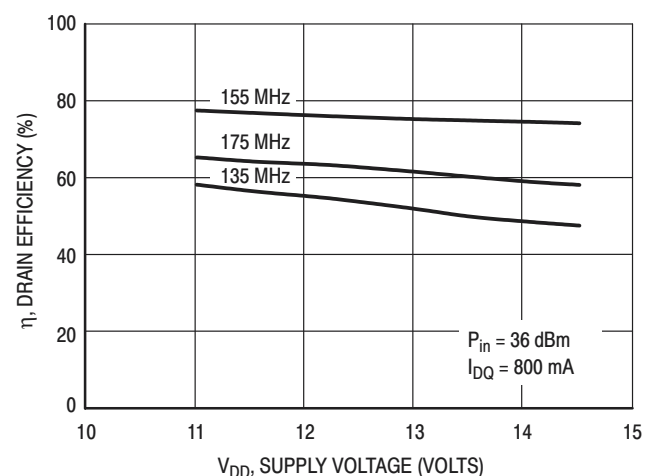
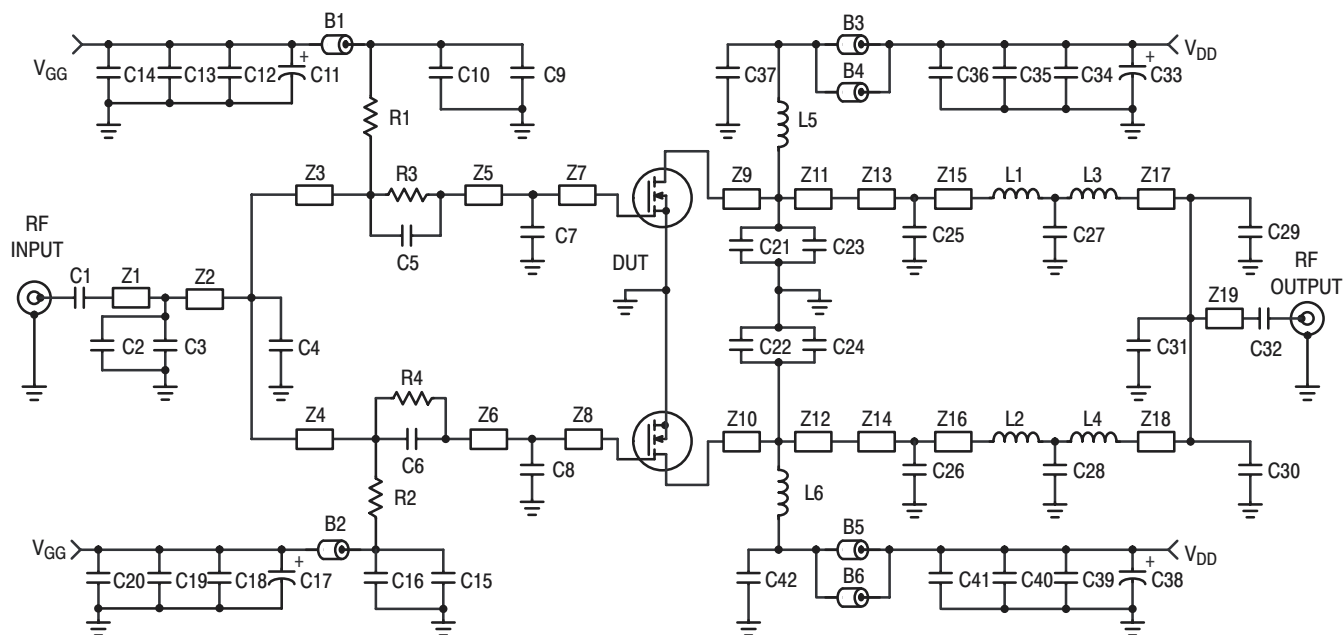


Figure 10. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1, B2, B3, B4, B5, B6	Long Ferrite Beads, Fair Rite Products	L1, L2, L3, L4	1 Turn, #18 AWG, 0.085" ID Inductors
C1, C9, C15, C32	270 pF, 100 mil Chip Capacitors	L5, L6	2 Turn, #16 AWG, 0.165" ID Inductors
C2, C3	7.5 pF, 100 mil Chip Capacitors	N1, N2	Type N Flange Mounts
C4	5.1 pF, 100 mil Chip Capacitor	R1, R2	25.5 Ω Chip Resistors (1206)
C5, C6	180 pF, 100 mil Chip Capacitors	R3, R4	10 Ω Chip Resistors (1206)
C7, C8	47 pF, 100 mil Chip Capacitors	Z1	0.240" x 0.080" Microstrip
C10, C16, C37, C42	120 pF, 100 mil Chip Capacitors	Z2	0.185" x 0.080" Microstrip
C11, C17, C33, C38	10 μ F, 50 V Electrolytic Capacitors	Z3, Z4	1.500" x 0.080" Microstrip
C12, C18, C34, C39	470 pF, 100 mil Chip Capacitors	Z5, Z6	0.150" x 0.240" Microstrip
C13, C19, C35, C40	1200 pF, 100 mil Chip Capacitors	Z7, Z8	0.140" x 0.240" Microstrip
C14, C20, C36, C41	0.1 μ F, 100 mil Chip Capacitors	Z9, Z10	0.140" x 0.240" Microstrip
C21, C22	33 pF, 100 mil Chip Capacitors	Z11, Z12	0.150" x 0.240" Microstrip
C23, C24	27 pF, 100 mil Chip Capacitors	Z13, Z14	0.270" x 0.080" Microstrip
C25, C26	15 pF, 100 mil Chip Capacitors	Z15, Z16	0.680" x 0.080" Microstrip
C27, C28	2.2 pF, 100 mil Chip Capacitors	Z17, Z18	0.320" x 0.080" Microstrip
C29, C30	6.2 pF, 100 mil Chip Capacitors	Z19	0.380" x 0.080" Microstrip
C31	1.0 pF, 100 mil Chip Capacitor	Board	31 mil Glass Teflon®

Figure 11. 400 – 470 MHz Broadband Test Circuit Schematic

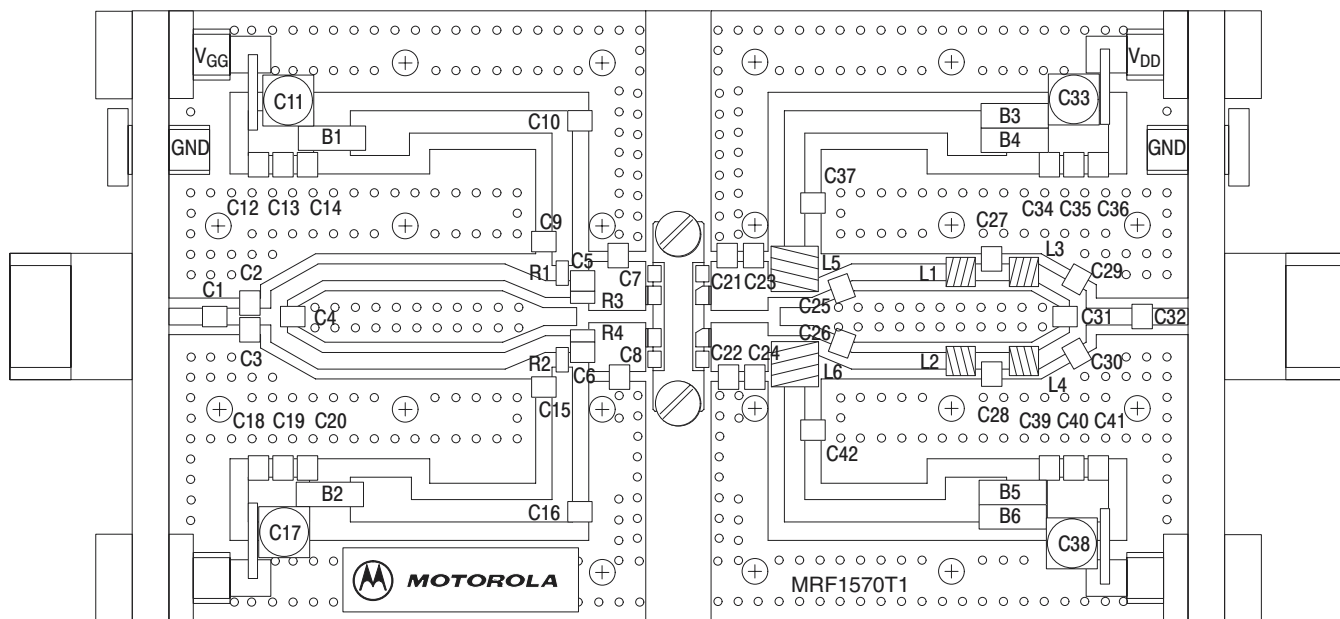


Figure 12. 400 – 470 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS, 400 – 470 MHz

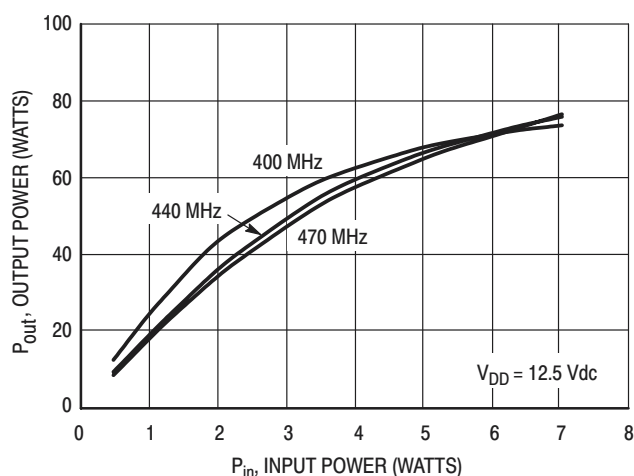


Figure 13. Output Power versus Input Power

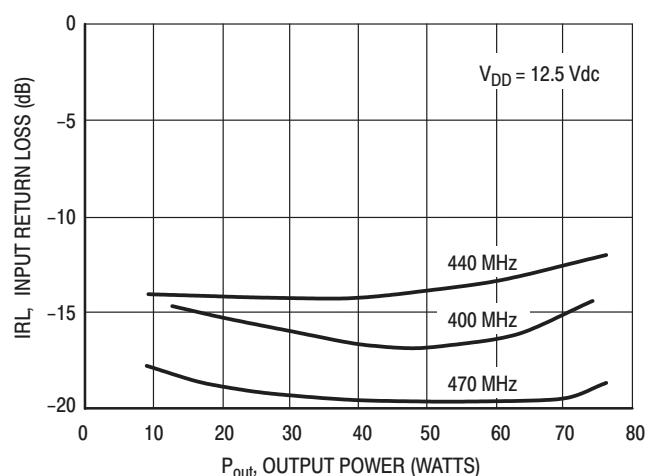


Figure 14. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 400 – 470 MHz

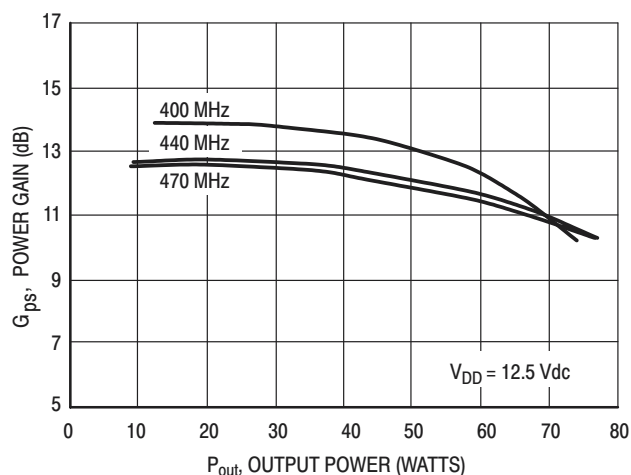


Figure 15. Gain versus Output Power

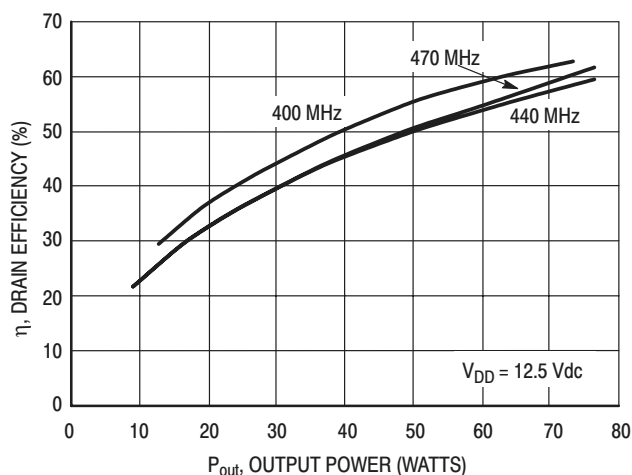


Figure 16. Drain Efficiency versus Output Power

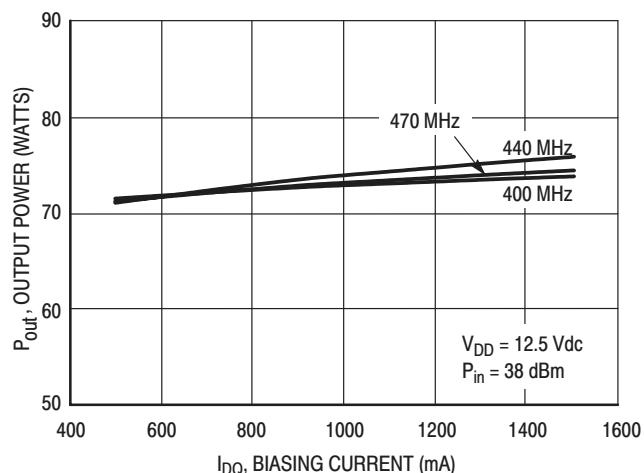


Figure 17. Output Power versus Biasing Current

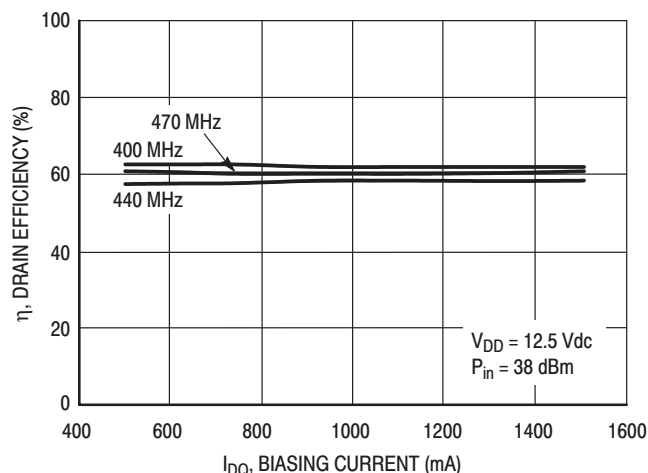


Figure 18. Drain Efficiency versus Biasing Current

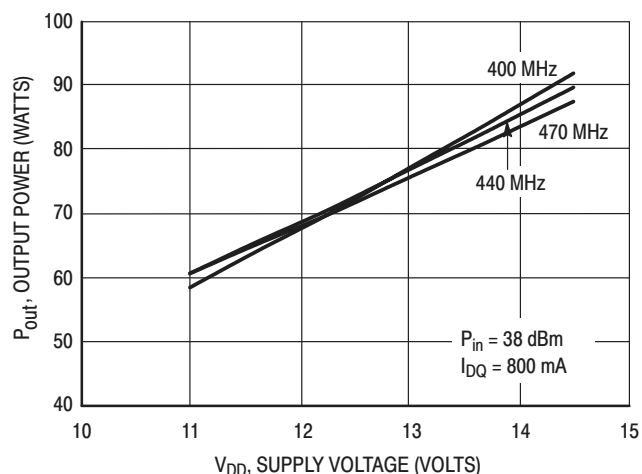


Figure 19. Output Power versus Supply Voltage

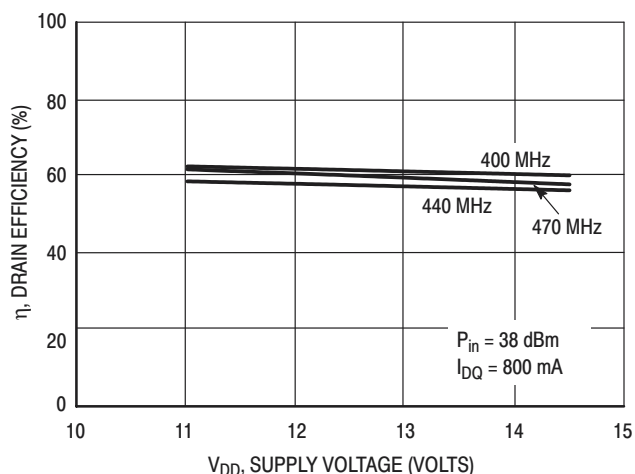
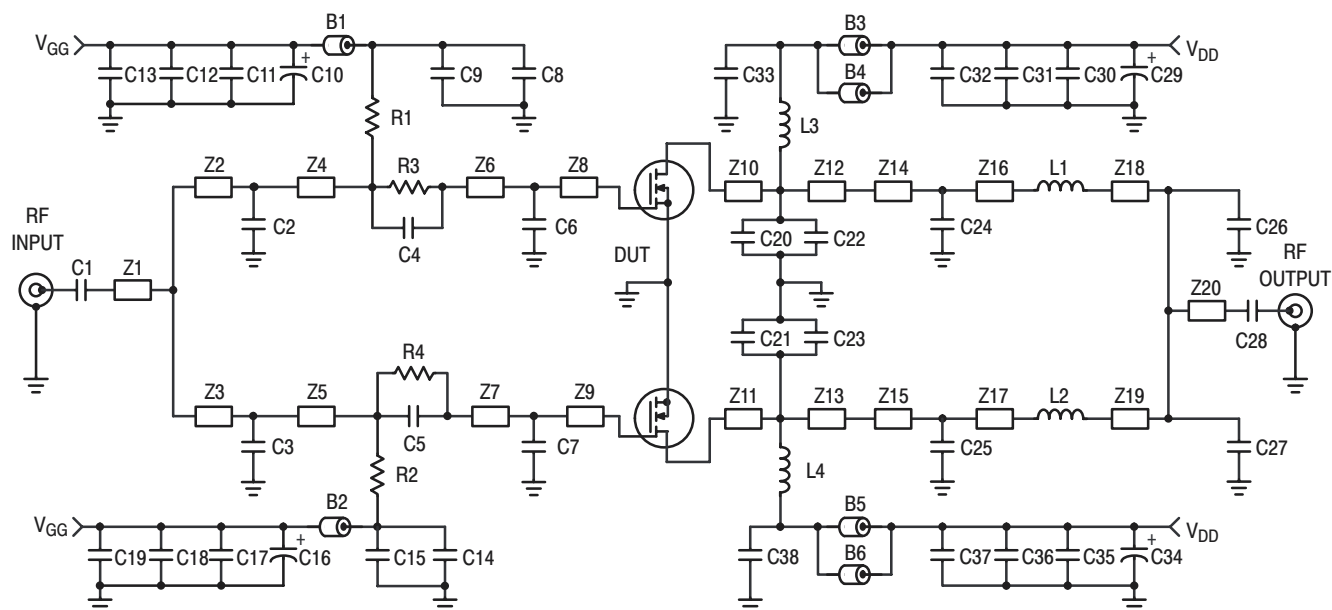


Figure 20. Drain Efficiency versus Supply Voltage

Freescale Semiconductor, Inc.



B1, B2, B3, B4, B5, B6	Long Ferrite Beads, Fair Rite Products	N1, N2	Type N Flange Mounts
C1, C8, C14, C28	270 pF, 100 mil Chip Capacitors	R1, R2	1.0 k Ω Chip Resistors (1206)
C2, C3	10 pF, 100 mil Chip Capacitors	R3, R4	10 Ω Chip Resistors (1206)
C4, C5	180 pF, 100 mil Chip Capacitors	Z1	0.40" x 0.080" Microstrip
C6, C7	47 pF, 100 mil Chip Capacitors	Z2, Z3	0.26" x 0.080" Microstrip
C9, C15, C33, C38	120 pF, 100 mil Chip Capacitors	Z4, Z5	1.35" x 0.080" Microstrip
C10, C16, C29, C34	10 μ F, 50 V Electrolytic Capacitors	Z6, Z7	0.17" x 0.240" Microstrip
C11, C17, C30, C35	470 pF, 100 mil Chip Capacitors	Z8, Z9	0.12" x 0.240" Microstrip
C12, C18, C31, C36	1200 pF, 100 mil Chip Capacitors	Z10, Z11	0.14" x 0.240" Microstrip
C13, C19, C32, C37	0.1 μ F, 100 mil Chip Capacitors	Z12, Z13	0.15" x 0.240" Microstrip
C20, C21	22 pF, 100 mil Chip Capacitors	Z14, Z15	0.18" x 0.172" Microstrip
C22, C23	20 pF, 100 mil Chip Capacitors	Z16, Z17	1.23" x 0.080" Microstrip
C24, C25, C26, C27	5.1 pF, 100 mil Chip Capacitors	Z18, Z19	0.12" x 0.080" Microstrip
L1, L2	1 Turn, #18 AWG, 0.115" ID Inductors	Z20	0.40" x 0.080" Microstrip
L3, L4	2 Turn, #16 AWG, 0.165" ID Inductors	Board	31 mil Glass Teflon [®]

Figure 21. 450 – 520 MHz Broadband Test Circuit Schematic

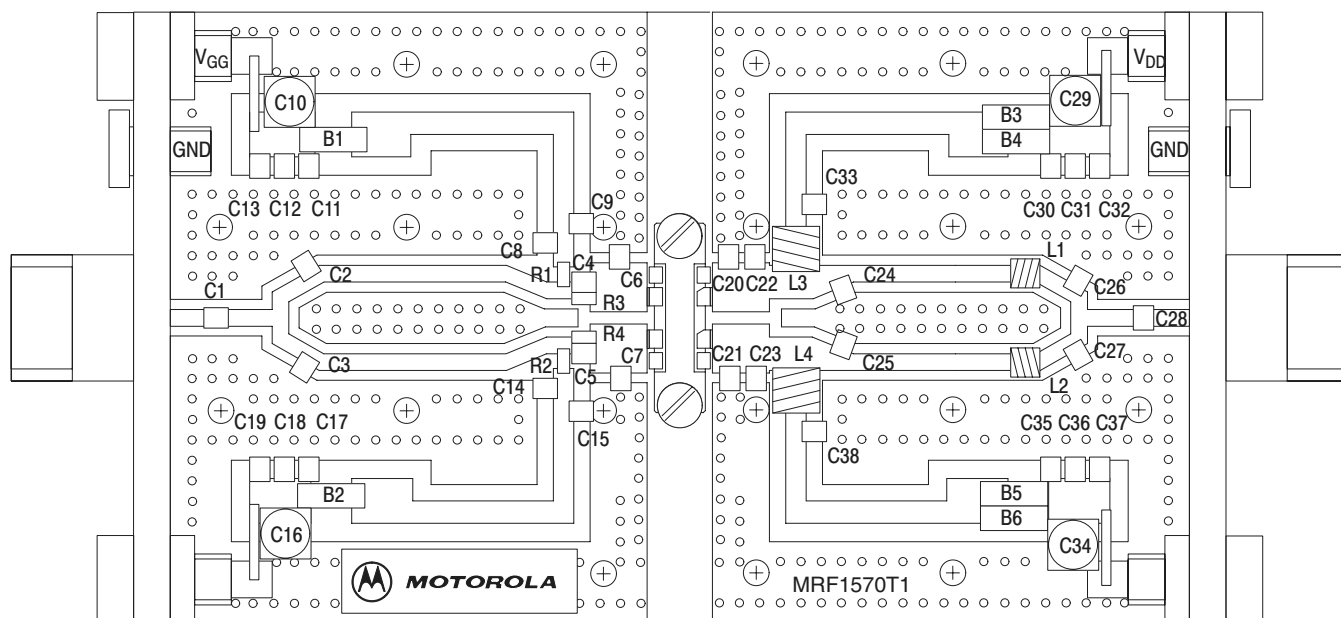


Figure 22. 450 – 520 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS, 450 – 520 MHz

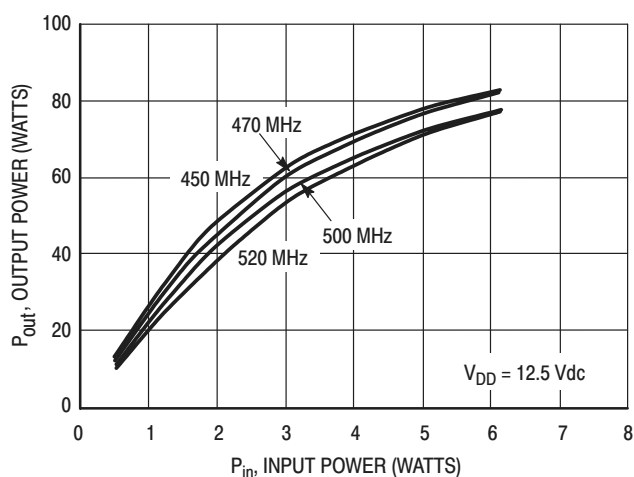


Figure 23. Output Power versus Input Power

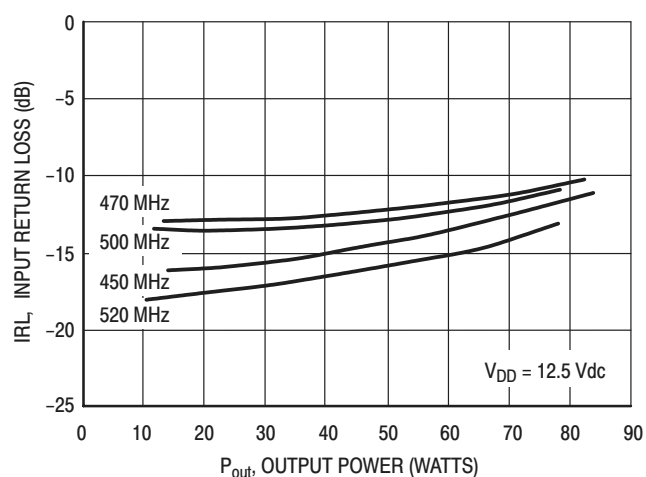


Figure 24. Input Return Loss versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS, 450 – 520 MHz

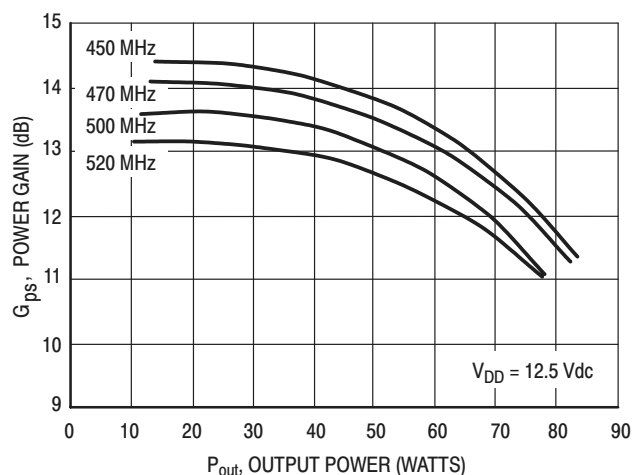


Figure 25. Gain versus Output Power

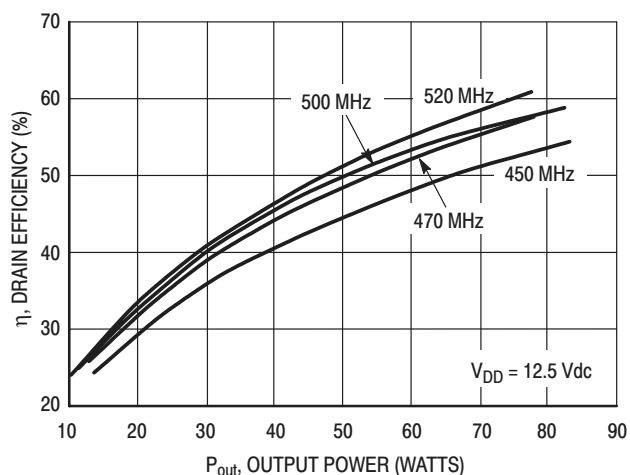


Figure 26. Drain Efficiency versus Output Power

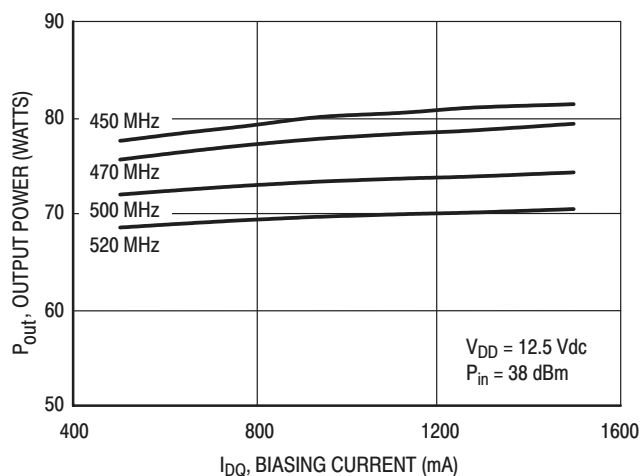


Figure 27. Output Power versus Biasing Current

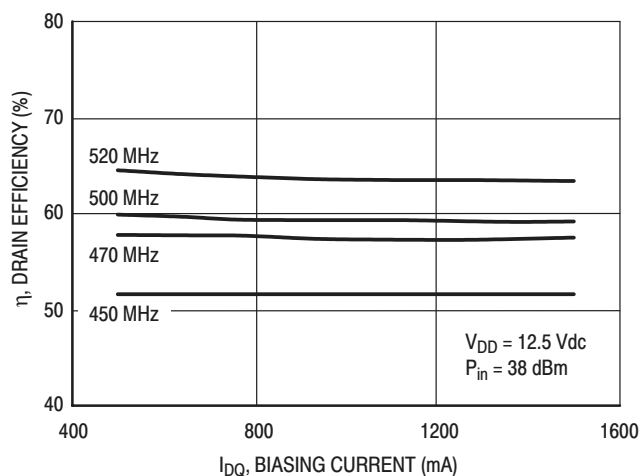


Figure 28. Drain Efficiency versus Biasing Current

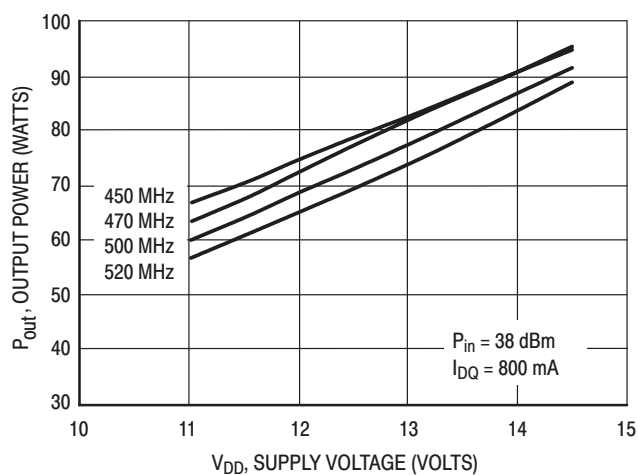


Figure 29. Output Power versus Supply Voltage

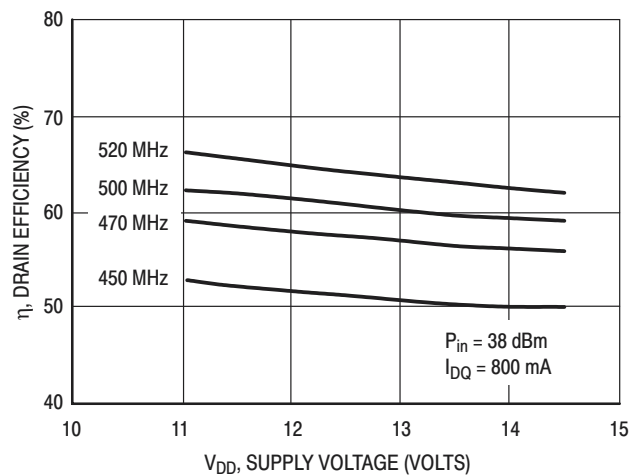
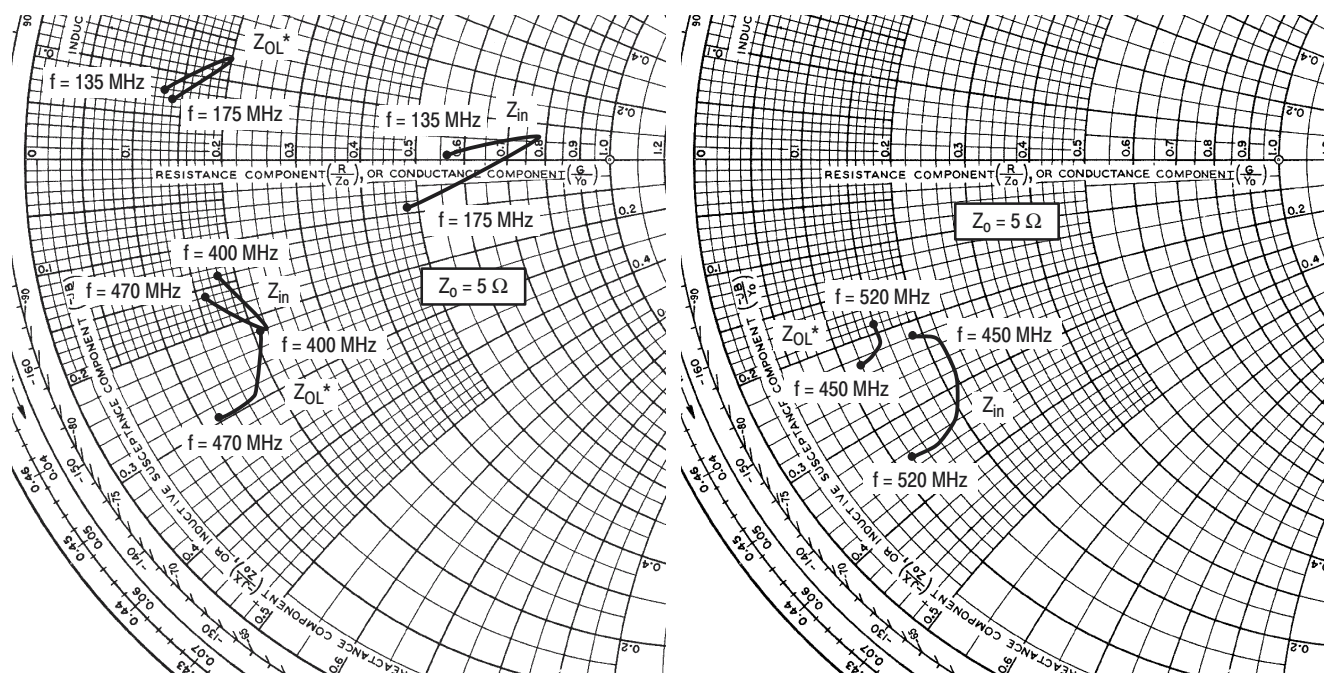


Figure 30. Drain Efficiency versus Supply Voltage



$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 0.8 \text{ A}$, $P_{out} = 70 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
135	$2.8 + j0.05$	$0.65 + j0.42$
155	$3.9 + j0.34$	$1.01 + j0.63$
175	$2.4 - j0.47$	$0.71 + j0.37$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 0.8 \text{ A}$, $P_{out} = 70 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
400	$0.92 - j0.71$	$1.05 - j1.10$
440	$1.12 - j1.11$	$0.83 - j1.45$
470	$0.82 - j0.79$	$0.59 - j1.43$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 0.8 \text{ A}$, $P_{out} = 70 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
450	$0.94 - j1.12$	$0.61 - j1.14$
470	$1.03 - j1.17$	$0.62 - j1.12$
500	$0.95 - j1.71$	$0.75 - j1.03$
520	$0.62 - j1.74$	$0.77 - j0.97$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50 \%$.

Notes: Impedance Z_{in} was measured with input terminated at 50Ω .
Impedance Z_{OL} was measured with output terminated at 50Ω .

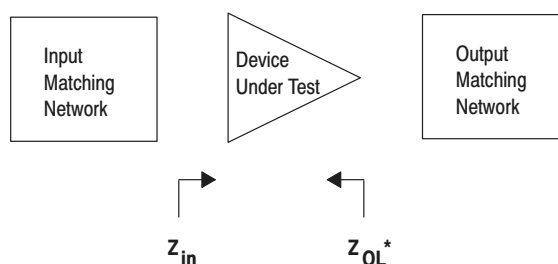


Figure 31. Series Equivalent Input and Output Impedance

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF mobile power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

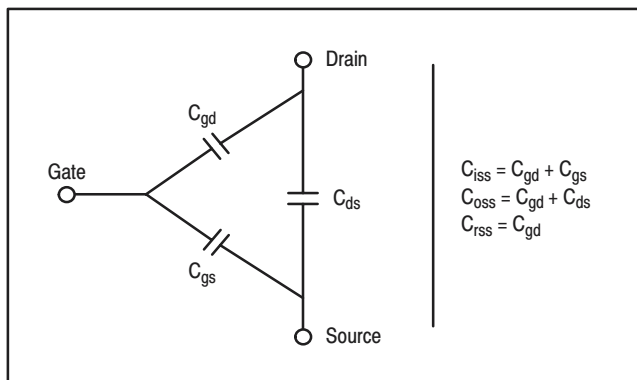
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.

**DRAIN CHARACTERISTICS**

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of $10^9 \Omega$ – resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at $I_{DQ} = 800 \text{ mA}$, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of $0.75^{\circ}\text{C}/\text{W}$ assumes a majority of the $0.170'' \times 0.608''$ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD-1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples

see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region. See Motorola Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

The RF MOSFET Line

RF Power Field Effect Transistors

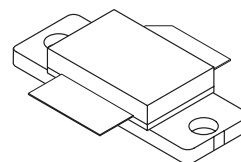
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM 900 frequency band, the high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 26 volt base station equipment.

- Specified Performance @ Full GSM Band, 921–960 MHz, 26 Volts
Output Power, P1dB — 80 Watts (Typ)
Power Gain @ P1dB — 16 dB (Typ)
Efficiency @ P1dB — 58% (Typ)
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

MRF6522-70
MRF6522-70R3

921 – 960 MHz, 70 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465D-05, STYLE 1
(NI-600)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	7	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	159 0.9	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 20 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 400 mAdc)	V _{GS(Q)}	3	4	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.15	0.6	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	2	3	—	S

DYNAMIC CHARACTERISTICS

Input Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{iss}	—	130	—	pF
Output Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{oss}	41	47	52	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	2.4	3	3.4	pF

FUNCTIONAL TESTS (In Motorola Test Fixture)

Output Power (2) (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	P _{1dB}	73	80	—	W
Common–Source Amplifier Power Gain @ P _{1dB} (Min) (2) (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	G _{ps}	14	16	18	dB
Drain Efficiency @ P _{out} = 50 W (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	η ₁	47	51	—	%
Drain Efficiency @ P _{1dB} (2) (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz)	η ₂	—	58	—	%
Input Return Loss @ P _{out} = 50 W (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = 921 MHz and 960 MHz f = 940 MHz)	IRL	— —	— —	–10 –15	dB
Output Mismatch Stress (2) (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 – 960 MHz, VSWR = 5:1, All Phase Angles)	Ψ	No Degradation In Output Power Before and After Test			

(1) Value excludes the input matching.

(2) To meet application requirements, Motorola test fixtures have been designed to cover full GSM 900 band ensuring batch-to-batch consistency.

Freescale Semiconductor, Inc.

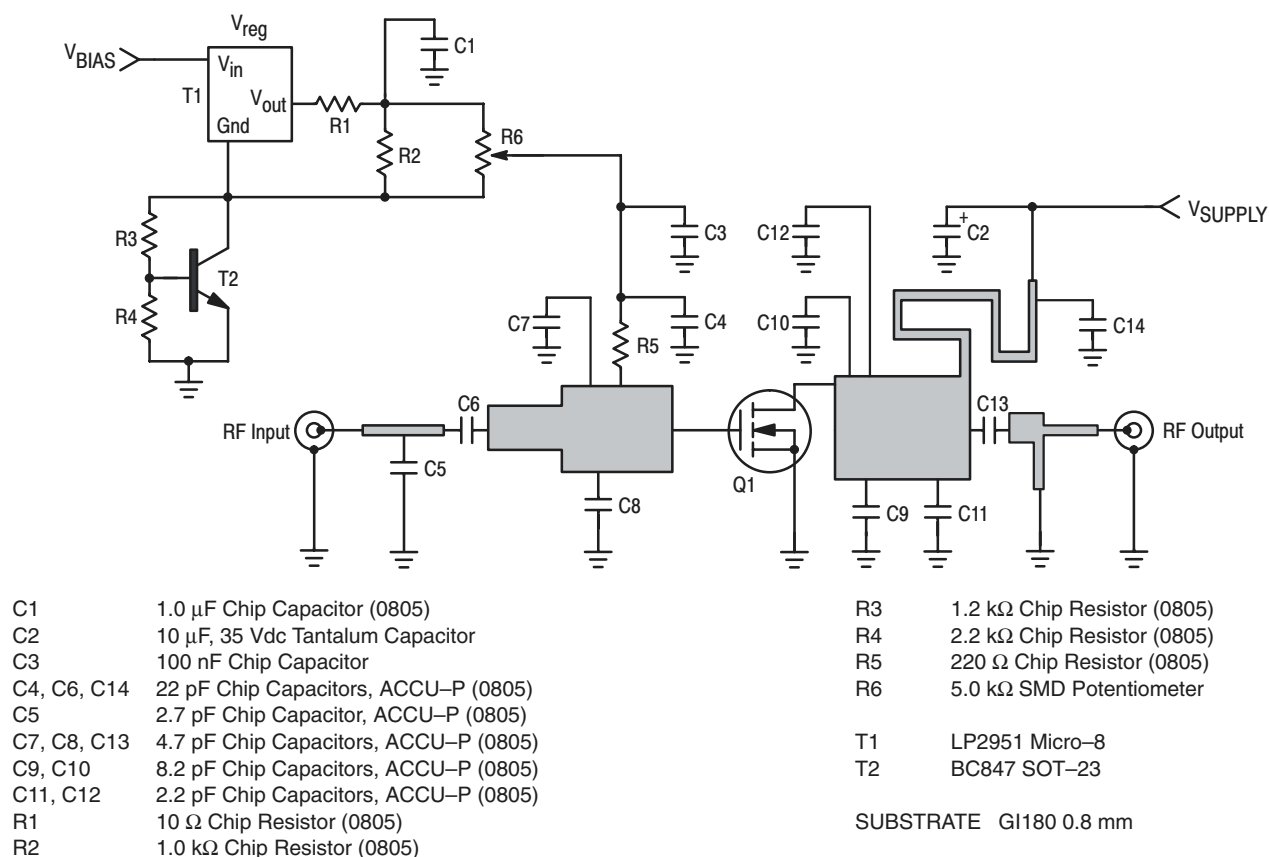


Figure 1. MRF6522-70 Test Circuit Schematic

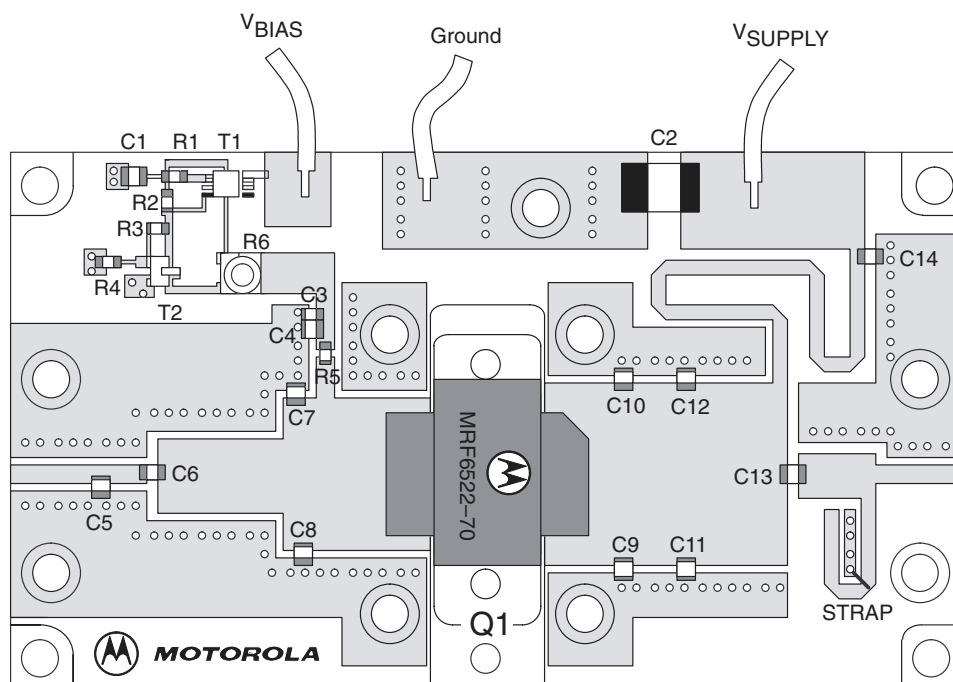


Figure 2. MRF6522-70 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

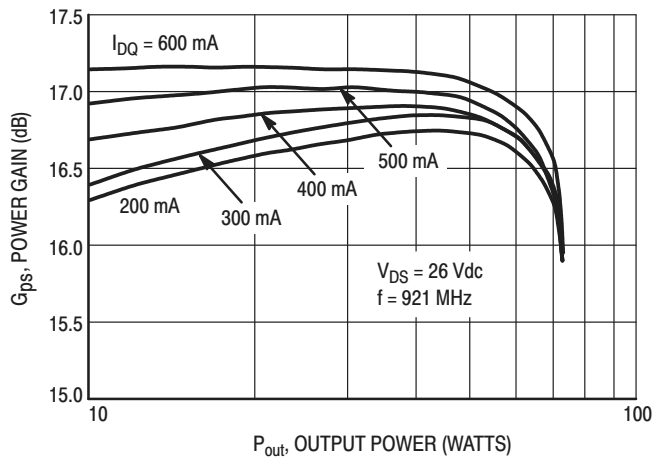


Figure 3. Power Gain versus Output Power

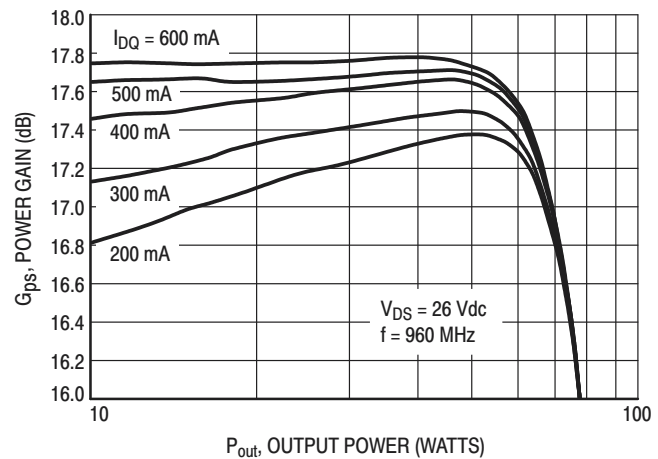


Figure 4. Power Gain versus Output Power

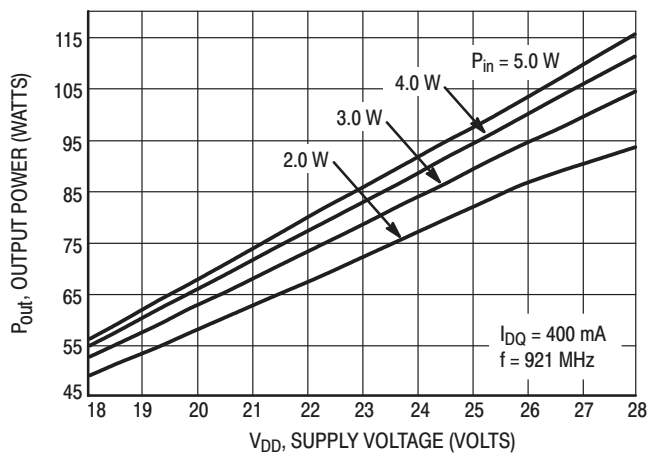


Figure 5. Output Power versus Supply Voltage

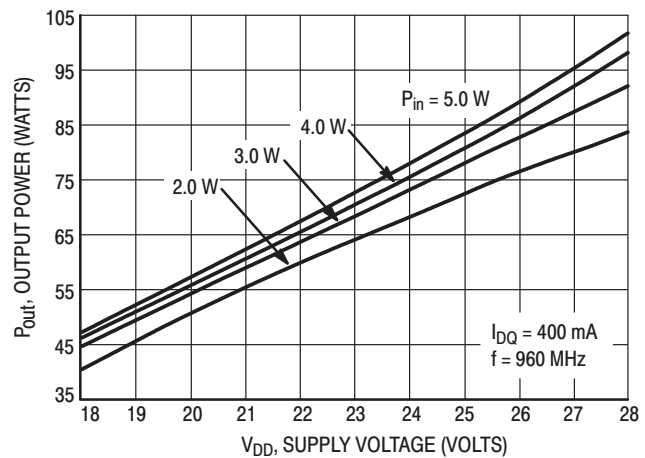


Figure 6. Output Power versus Supply Voltage

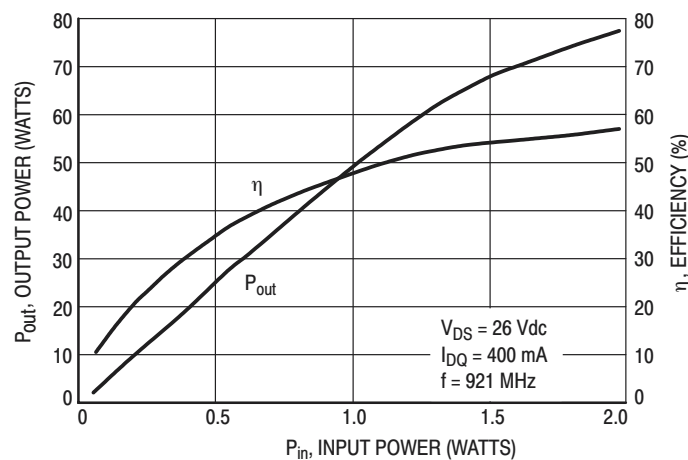


Figure 7. Efficiency and Output Power versus Input Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

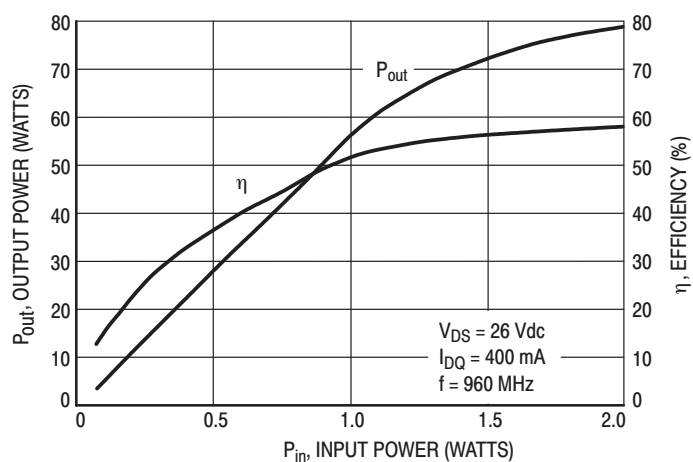


Figure 8. Efficiency and Output Power versus Input Power

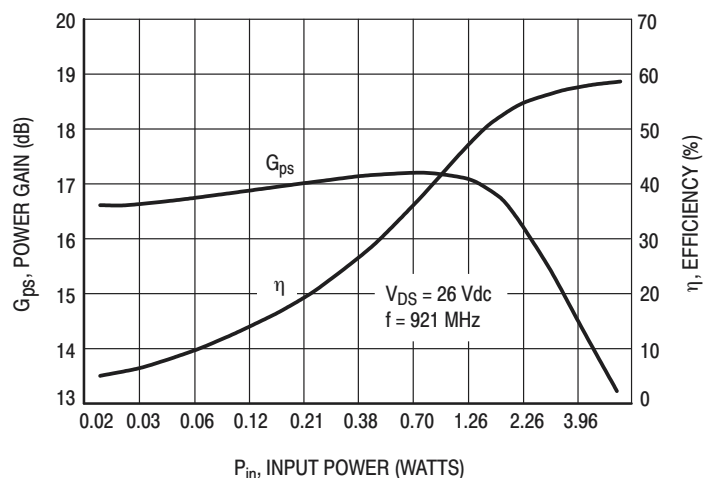


Figure 9. Power Gain and Efficiency versus Input Power

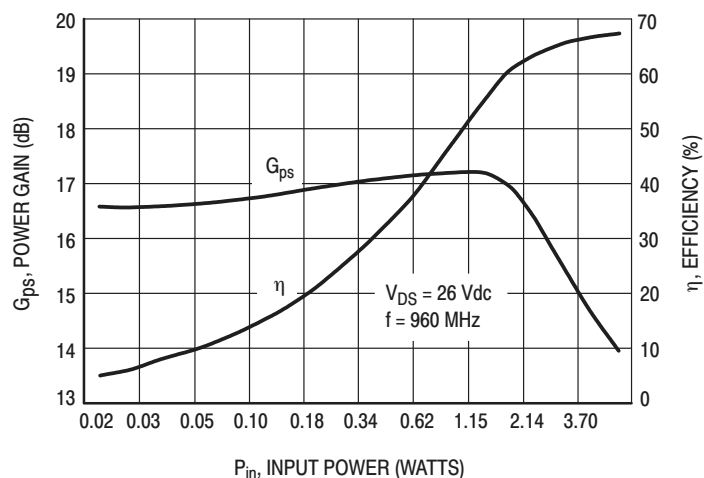


Figure 10. Power Gain and Efficiency versus Input Power

Freescale Semiconductor, Inc.

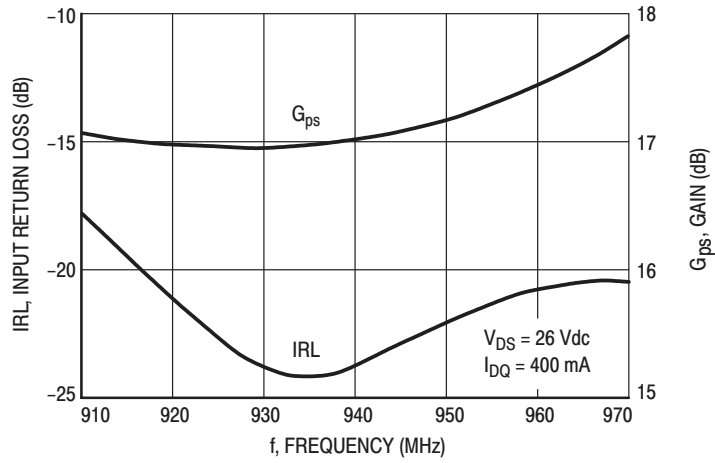
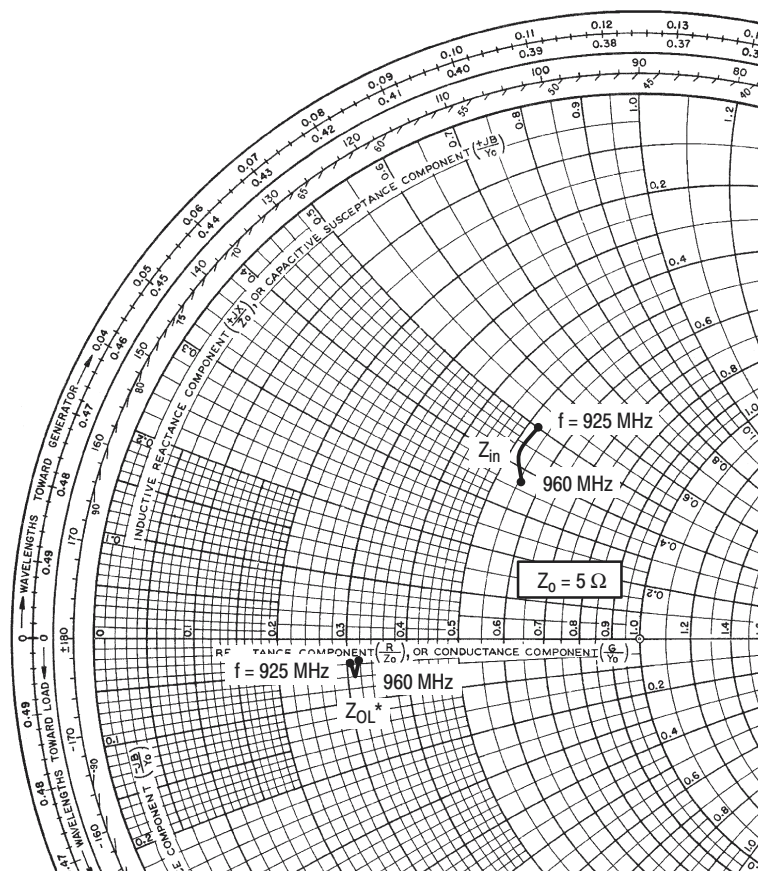


Figure 11. Performance in Broadband Circuit (at Small Signal)



$V_{\text{SUPPLY}} = 26 \text{ Vdc}$, $I_{\text{BIAS}} = 400 \text{ mA}$, CW = Room Temperature

f MHz	Z_{in} Ω	Z_{OL}^* Ω
925	$2.65 + j2.53$	$1.62 - j0.2$
940	$2.67 + j2.14$	$1.56 - j0.34$
960	$2.85 + j1.87$	$1.55 - j0.2$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

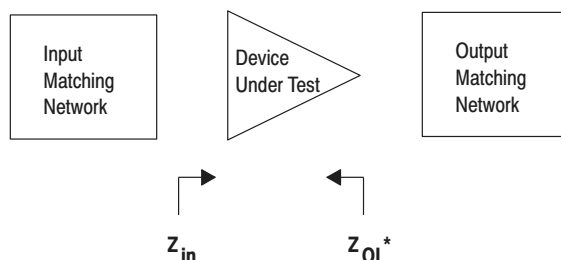


Figure 12. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistor Array

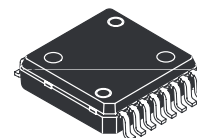
N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies to 1.0 GHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

- Typical Performance at 960 MHz, 26 Volts
Output Power — 2 Watts Per Transistor
Power Gain — 18 dB
Efficiency — 50%
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 960 MHz, 2 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

MRF9002R2

1.0 GHz, 2 W, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 978-03
PLASTIC
PFP-16

PIN CONNECTIONS

N.C.	1	16	DRAIN 1-1
N.C.	2	15	DRAIN 1-2
GATE1	3	14	DRAIN 2-1
N.C.	4	13	DRAIN 2-2
GATE2	5	12	N.C.
N.C.	6	11	DRAIN 3-1
GATE3	7	10	DRAIN 3-2
N.C.	8	9	N.C.

(Top View)

NOTE: Exposed backside flag is source terminal for transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Dissipation Per Transistor @ $T_C = 25^\circ\text{C}$	P_D	4	Watts
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case, Single Transistor	$R_{\theta JC}$	12	$^\circ\text{C/W}$

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	3

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 20 μAdc)	V _{GS(th)}	2.4	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 25 mAdc)	V _{GS(Q)}	3	—	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 0.1 Adc)	V _{DS(on)}	—	0.3	—	Vdc

FUNCTIONAL TESTS (Per Transistor in Motorola Test Fixture, 50 ohm system)

Common–Source Amplifier Power Gain @ P1dB (V _{DD} = 26 Vdc, I _{DQ} = 25 mA, f = 960.0 MHz)	G _{ps}	15	18	—	dB
Drain Efficiency @ P1dB (V _{DD} = 26 Vdc, I _{DQ} = 25 mA, f = 960.0 MHz)	η	35	50	—	%
Input Return Loss @ P1dB (V _{DD} = 26 Vdc, I _{DQ} = 25 mA, f = 960.0 MHz)	IRL	—	–15	–9	dB
Power Output, 1 dB Compression Point (V _{DD} = 26 Vdc, I _{DQ} = 25 mA, f = 960.0 MHz)	P _{1dB}	34	37	—	dBm
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 2 W CW, I _{DQ} = 25 mA, f = 960.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			

Freescale Semiconductor, Inc.

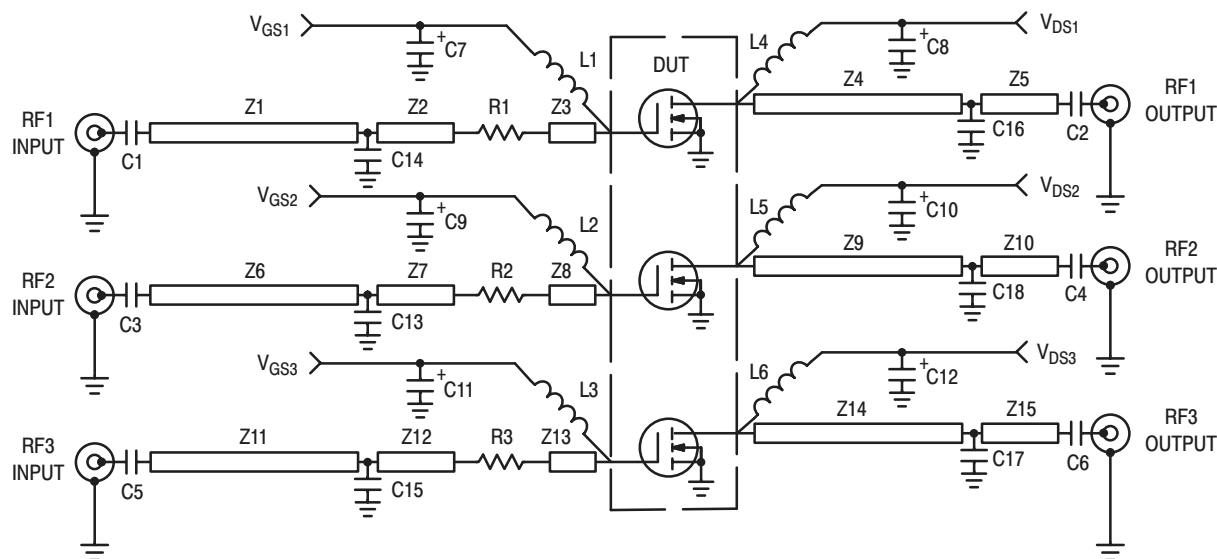


Figure 1. MRF9002R2 Broadband Test Circuit Schematic

Table 1. MRF9002R2 Broadband Test Circuit Component Designations and Values

Designators	Description
C1–C6	33 pF Chip Capacitors (0805)
C7–C12	1.0 μ F, 35 V Tantalum Capacitors, B Case, Kemet
C13	8.2 pF Chip Capacitor (0805)
C14, C15	10 pF Chip Capacitors (0805)
C16, C17	2.7 pF Chip Capacitors (0805)
C18	3.3 pF Chip Capacitor (0805)
L1–L6	12 nH Chip Inductors (0805)
R1–R3	0 Ω Chip Resistors (0805)
Z1, Z11	1.16 x 28.5 mm Microstrip
Z2, Z7, Z12	0.65 x 5.6 mm Microstrip
Z3, Z8, Z13	0.65 x 2.6 mm Microstrip
Z4, Z14	1.16 x 19.5 mm Microstrip
Z5, Z15	1.16 x 17.5 mm Microstrip
Z6	1.16 x 12.9 mm Microstrip
Z9	1.16 x 27.2 mm Microstrip
Z10	1.16 x 4.3 mm Microstrip
PCB	Etched Circuit Board
Raw PCB Material	Rogers RO4350, 0.020", 2.5", x 2.5", $\epsilon_r = 3.5$
Bedstead	Copper Heatsink

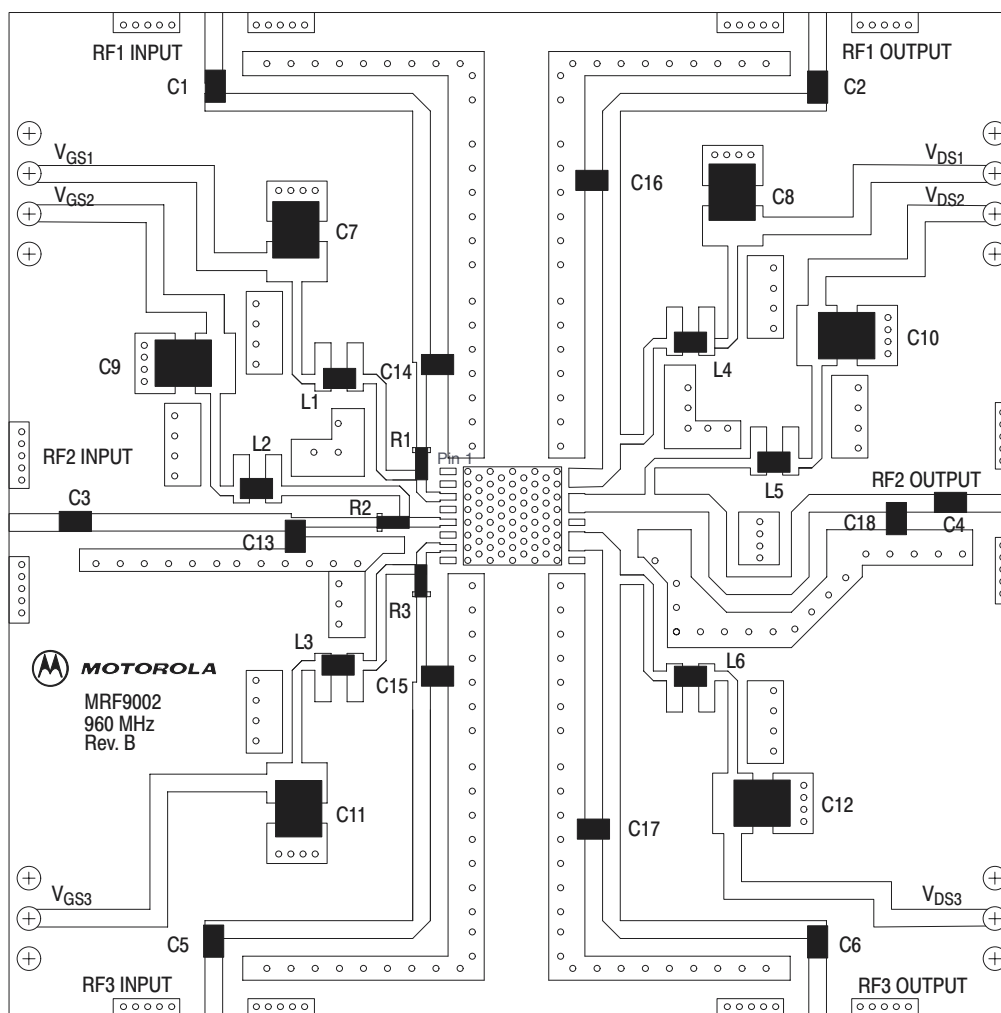


Figure 2. MRF9002R2 Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

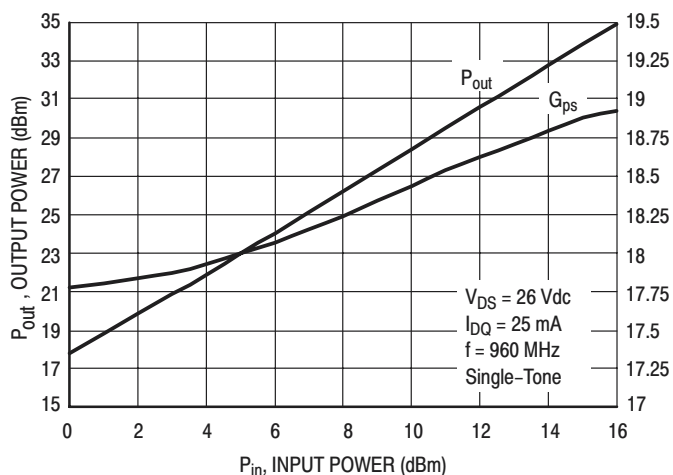


Figure 3. Output Power and Power Gain versus Input Power

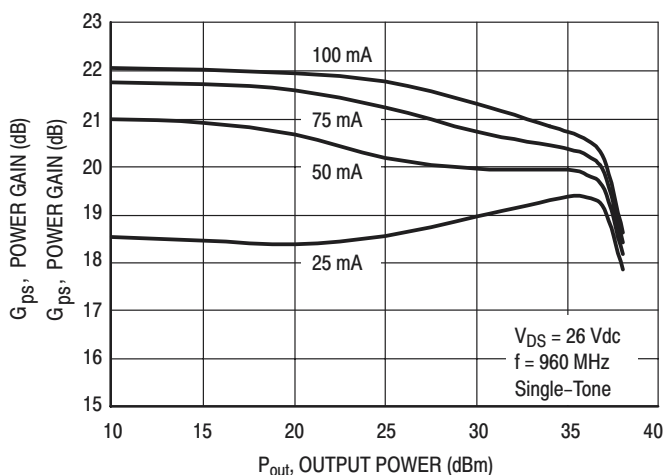


Figure 4. Power Gain versus Output Power

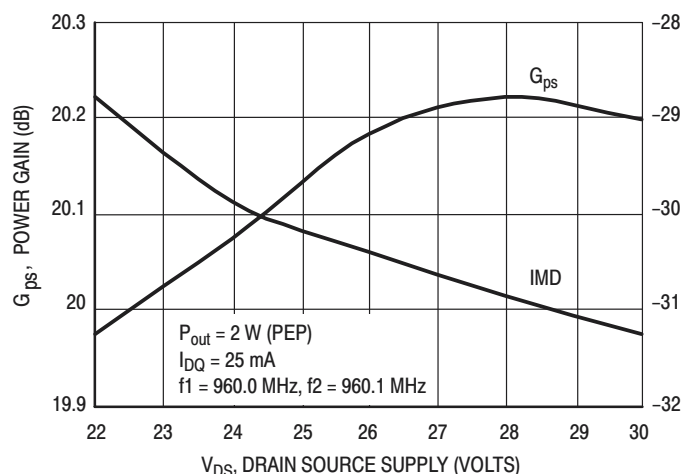


Figure 5. Power Gain and Intermodulation Distortion versus Supply Voltage

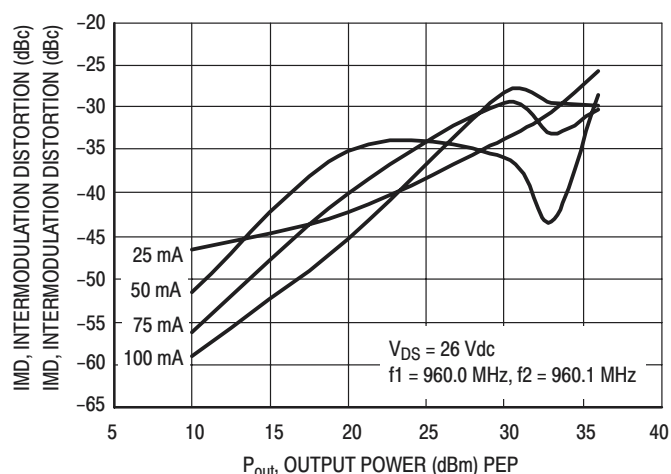


Figure 6. Intermodulation Distortion versus Output Power

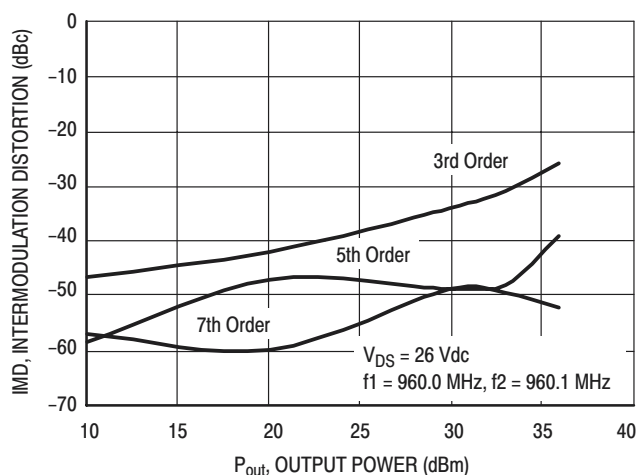


Figure 7. Intermodulation Distortion Products versus Output Power

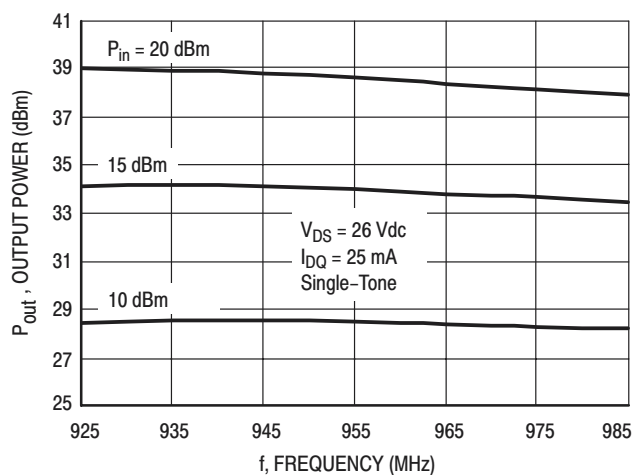


Figure 8. Output Power versus Frequency

Freescale Semiconductor, Inc.

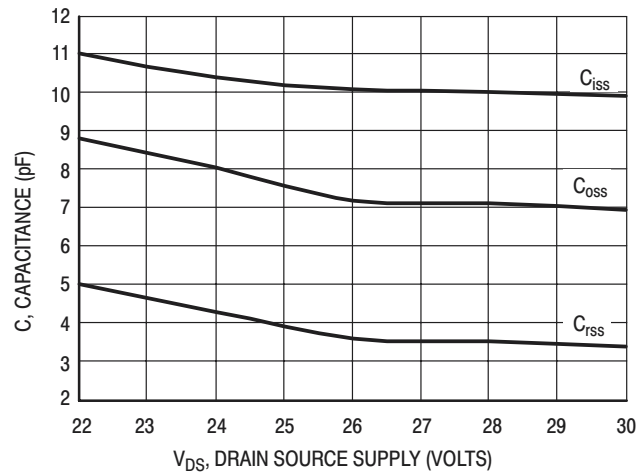
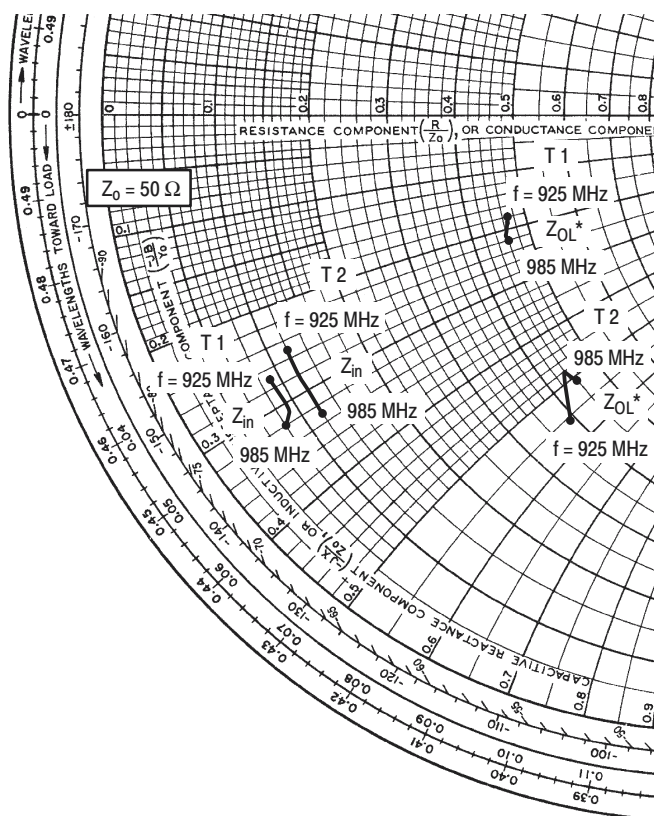
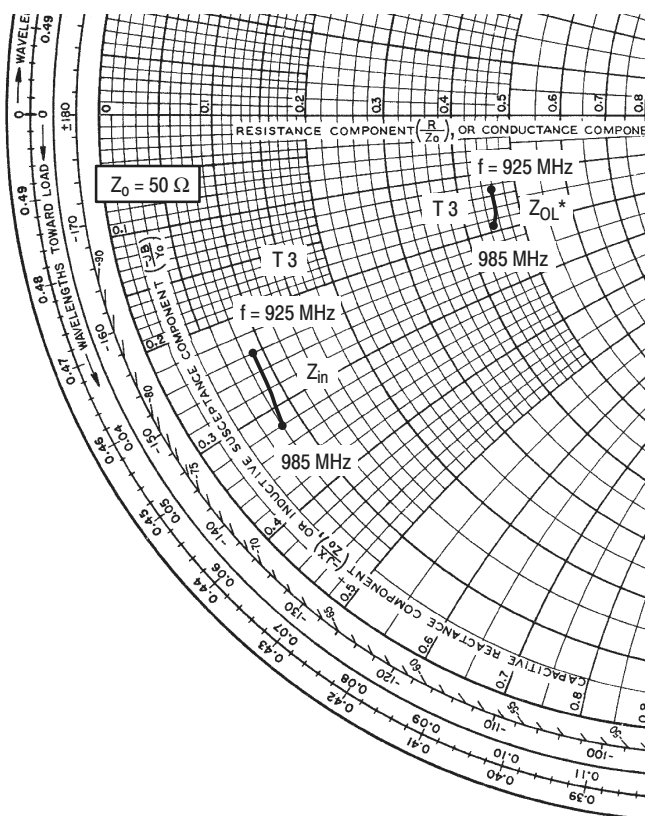


Figure 9. Capacitance versus Drain Source Voltage



TRANSISTORS 1 and 2



TRANSISTOR 3

$V_{DD} = 26 \text{ V}$, $I_{DQ} = 25 \text{ mA}$, $P_{out} = 2 \text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
925	$4.5 - j13.3$	$23.4 - j9.2$
960	$4.3 - j15.3$	$23.2 - j10.4$
985	$4.1 - j15.8$	$23.0 - j11.1$

Transistor 1

$V_{DD} = 26 \text{ V}$, $I_{DQ} = 25 \text{ mA}$, $P_{out} = 2 \text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
925	$6.0 - j12.3$	$19.7 - j27.8$
960	$5.9 - j14.3$	$22.0 - j23.9$
985	$5.8 - j16.5$	$22.5 - j25.4$

Transistor 2

$V_{DD} = 26 \text{ V}$, $I_{DQ} = 25 \text{ mA}$, $P_{out} = 2 \text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
925	$4.3 - j12.2$	$23.1 - j6.5$
960	$4.3 - j14.0$	$22.8 - j8.4$
985	$3.9 - j15.9$	$22.6 - j9.3$

Transistor 3

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

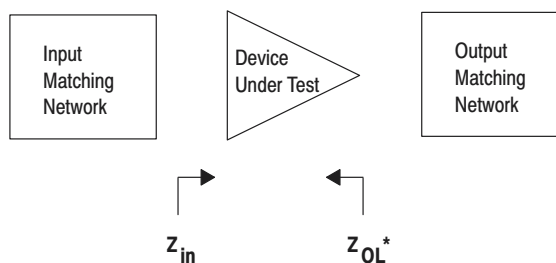


Figure 10. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

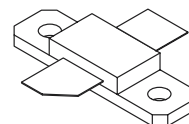
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

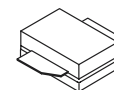
- Typical Two-Tone Performance at 945 MHz, 26 Volts
 - Output Power — 30 Watts PEP
 - Power Gain — 19 dB
 - Efficiency — 41.5%
 - IMD — -32.5 dBc
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 945 MHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μm Nominal.

MRF9030R1
MRF9030LSR1

945 MHz, 30 W, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B-05, STYLE 1
NI-360
MRF9030R1



CASE 360C-05, STYLE 1
NI-360S
MRF9030LSR1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	92 0.53 117 0.67	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.9 1.5	$^\circ\text{C}/\text{W}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

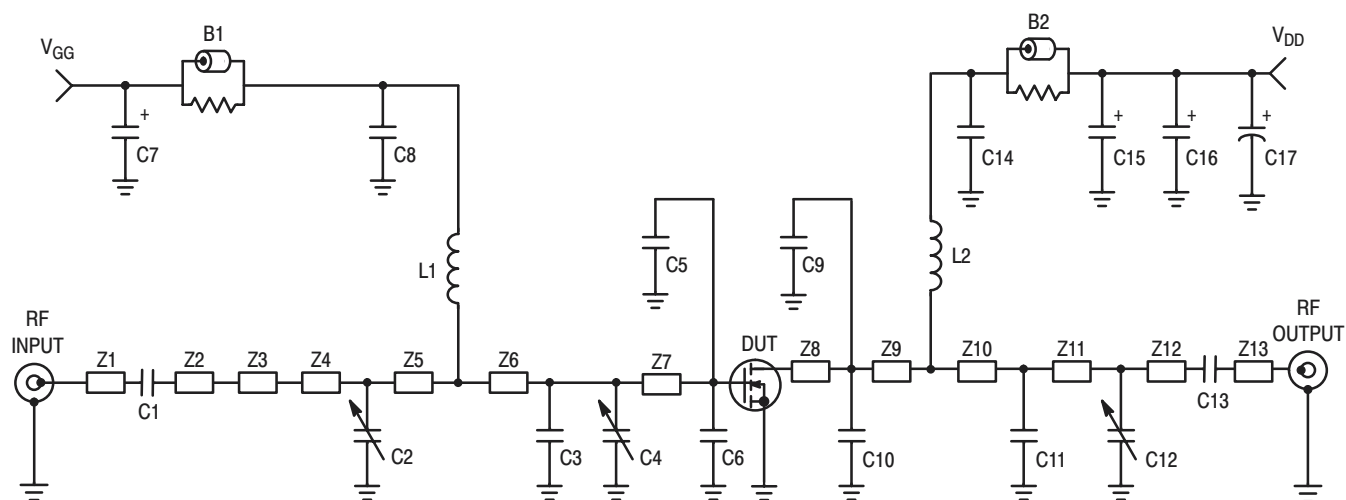
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 68 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc)	V _{GS(th)}	2	2.9	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 250 mAdc)	V _{GS(Q)}	—	3.8	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 0.7 Adc)	V _{DS(on)}	—	0.19	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	3	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{iss}	—	49.5	—	pF
Output Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	26.5	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	1	—	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	G_{ps}	18	19	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	η	37	41.5	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	IMD	—	-32.5	-28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	IRL	—	-15.5	-9	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	G_{ps}	—	19	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	η	—	41.5	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	IMD	—	-33	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	IRL	—	-14	—	dB
Power Output, 1 dB Compression Point ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$)	P_{1dB}	—	30	—	W
Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$)	G_{ps}	—	19	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$)	η	—	60	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 250\text{ mA}$, $f = 945.0\text{ MHz}$, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			

Freescale Semiconductor, Inc.



B1	Short Ferrite Bead	Z3	0.500" x 0.100" Microstrip
B2	Long Ferrite Bead	Z4	0.215" x 0.270" Microstrip
C1, C8, C13, C14	47 pF Chip Capacitors, B Case	Z5	0.315" x 0.270" Microstrip
C2, C4	0.8 pF to 8.0 pF Trim Capacitors	Z6	0.160" x 0.270" x 0.520", Taper
C3	3.9 pF Chip Capacitor, B Case	Z7	0.285" x 0.520" Microstrip
C5, C6	7.5 pF Chip Capacitors, B Case	Z8	0.140" x 0.270" Microstrip
C7, C15, C16	10 μ F, 35 V Tantalum Capacitors	Z9	0.450" x 0.270" Microstrip
C9, C10	10 pF Chip Capacitors, B Case	Z10	0.250" x 0.060" Microstrip
C11	9.1 pF Chip Capacitor, B Case	Z11	0.720" x 0.060" Microstrip
C12	0.6 pF to 4.5 pF Trim Capacitor	Z12	0.490" x 0.060" Microstrip
C17	220 μ F, 50 V Electrolytic Capacitor	Z13	0.290" x 0.060" Microstrip
L1, L2	12.5 nH Surface Mount Inductors	PCB	Taconic RF-35-0300, 30 mil, $\epsilon_r = 3.55$
Z1	0.260" x 0.060" Microstrip		
Z2	0.240" x 0.060" Microstrip		

Figure 1. 945 MHz Broadband Test Circuit Schematic

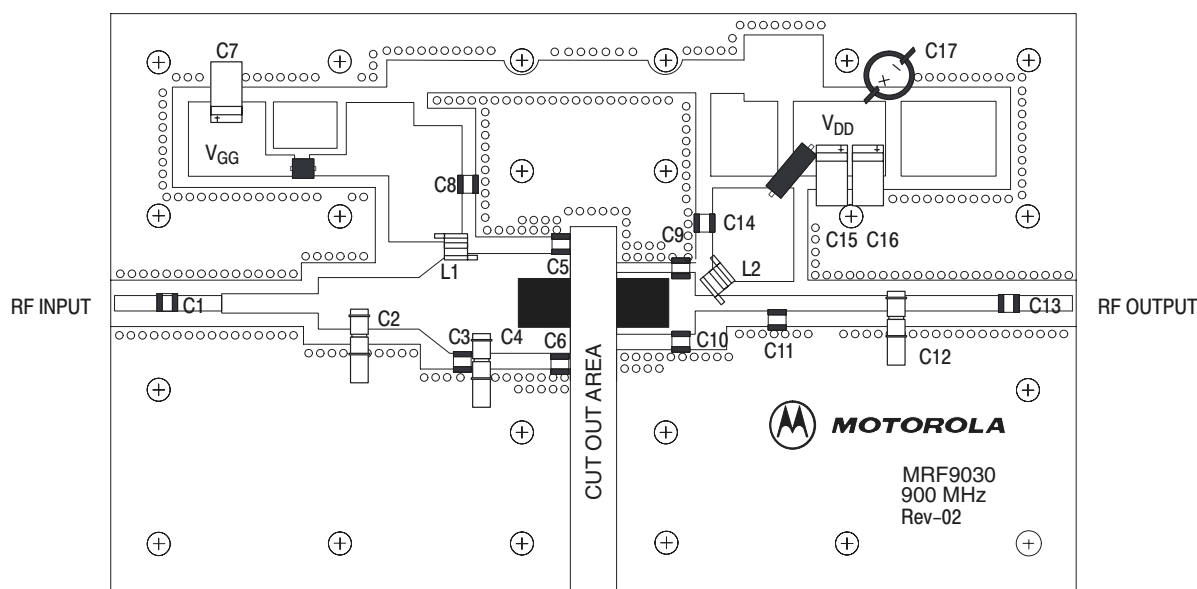


Figure 2. 945 MHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

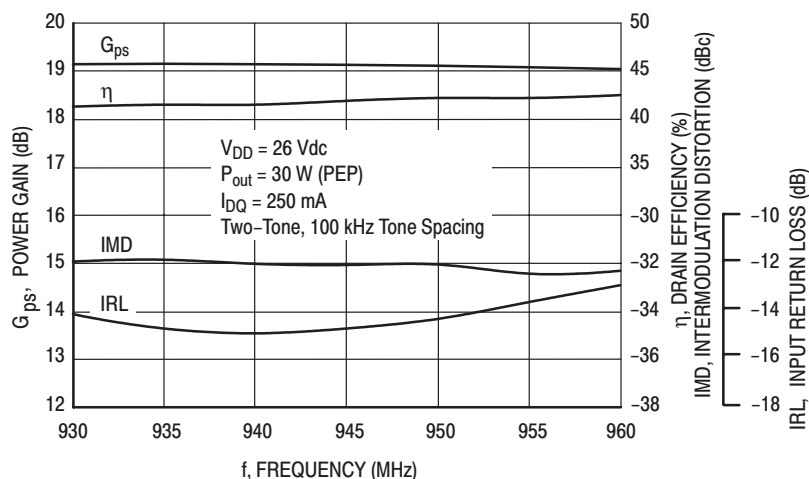


Figure 3. Class AB Broadband Circuit Performance

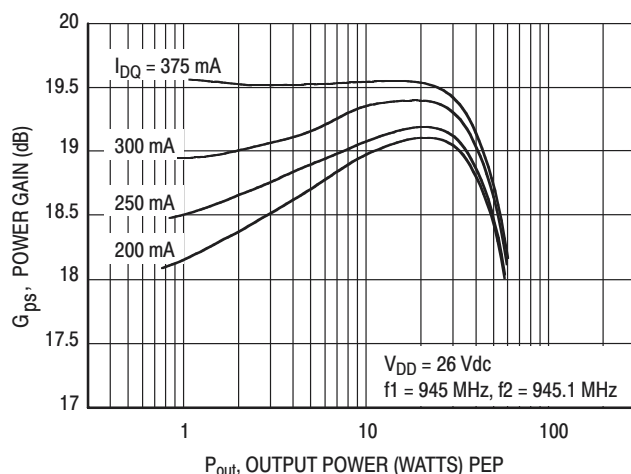


Figure 4. Power Gain versus Output Power

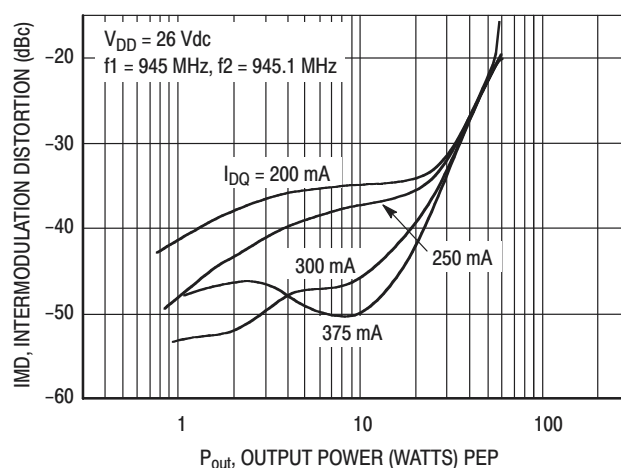


Figure 5. Intermodulation Distortion versus Output Power

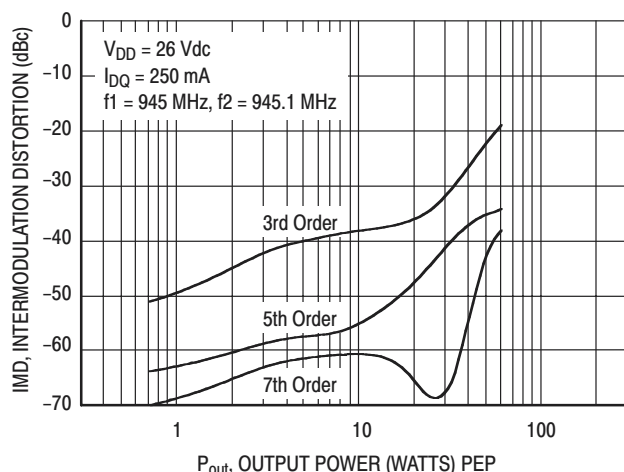


Figure 6. Intermodulation Distortion Products versus Output Power

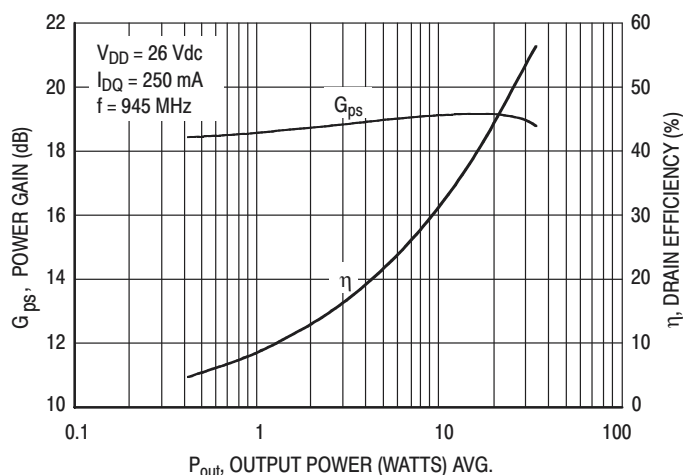


Figure 7. Power Gain and Efficiency versus Output Power

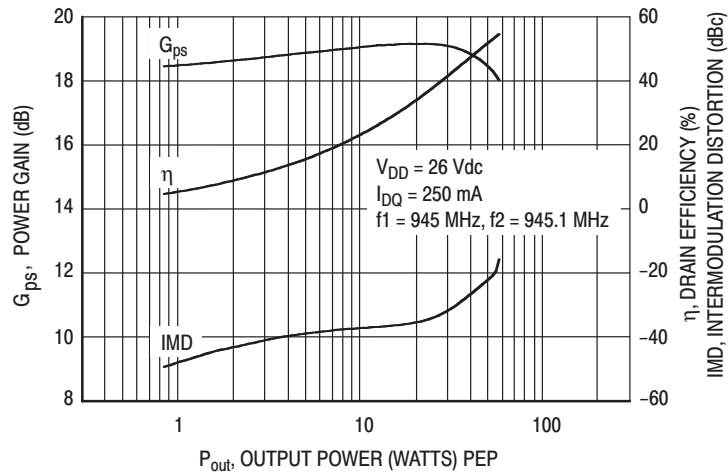
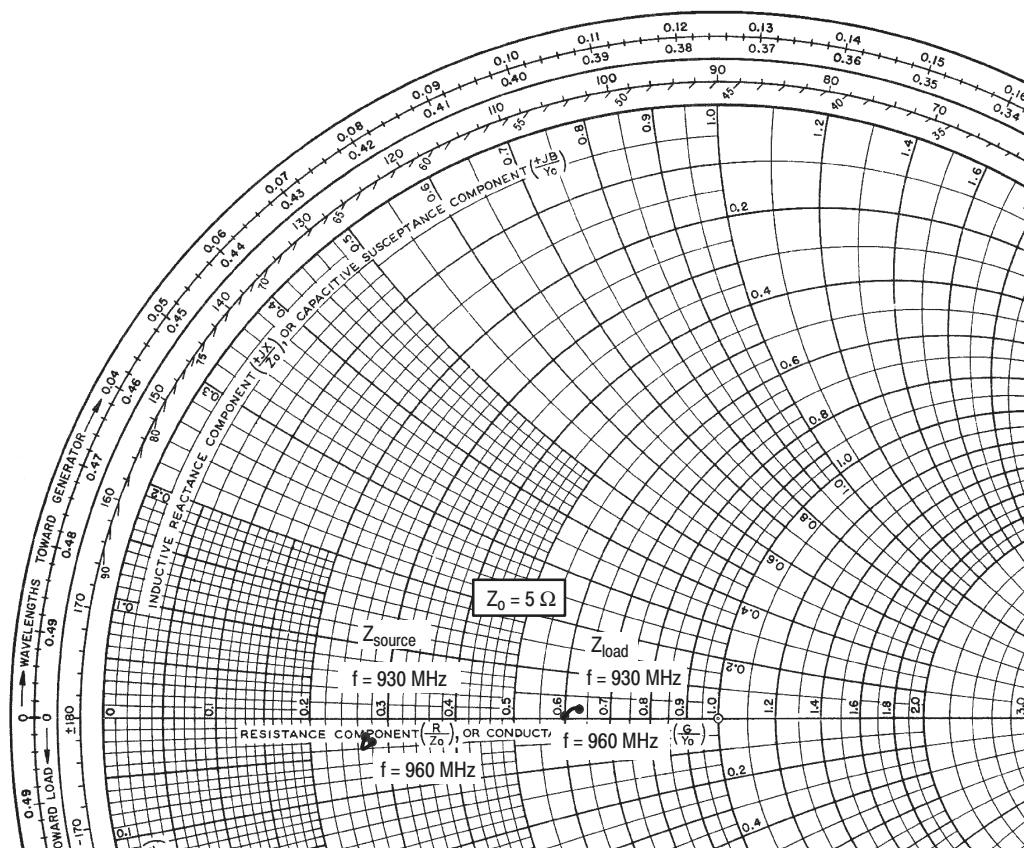


Figure 8. Power Gain, Efficiency and IMD versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 30 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
930	$1.34 - j0.1$	$3.175 + j0.09$
945	$1.36 - j0.2$	$3.1 + j0.08$
960	$1.4 - j0.14$	$3.0 + j0.05$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

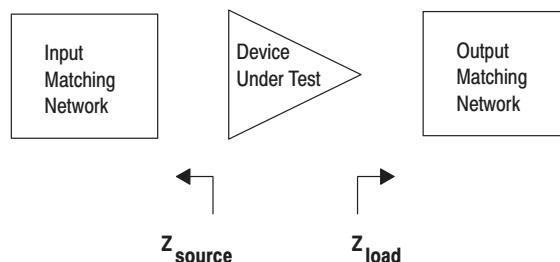


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

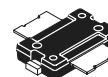
- Typical Performance at 945 MHz, 26 Volts
Output Power — 30 Watts PEP
Power Gain — 20 dB
Efficiency — 41% (Two Tones)
IMD — -31 dBc
- Integrated ESD Protection
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 945 MHz, 30 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Moisture Sensitivity Level 3
- Dual-Lead Bolt-down Plastic Package Can Also Be Used As Surface Mount.
- TO-272 Available in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.
- TO-270 Available in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

MRF9030MR1

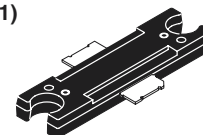
MRF9030MBR1

945 MHz, 30 W, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs

CASE 1265-07, STYLE 1
(TO-270)
PLASTIC
(MRF9030MR1)



CASE 1337-02, STYLE 1
(TO-272 DUAL LEAD)
PLASTIC
(MRF9030MBR1)



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	139 0.93	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	175	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)
Charge Device Model MRF9030MR1 MRF9030MBR1	C7 (Minimum) C6 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.08	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc)	V _{GS(th)}	2	2.9	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 250 mA)	V _{GS(Q)}	3	3.8	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 0.7 Adc)	V _{DS(on)}	—	0.23	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	2.7	—	S

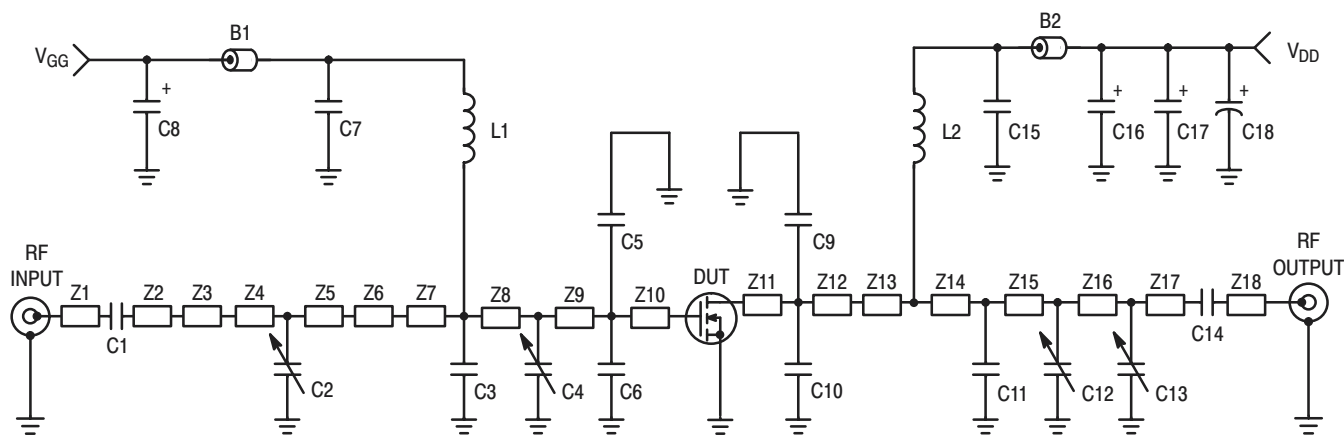
DYNAMIC CHARACTERISTICS

Input Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{iss}	—	49	—	pF
Output Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	27	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	1.2	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture)

Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	G _{ps}	18	20	—	dB
Two–Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	η	37	41	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IRL	—	–13	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	G _{ps}	—	20	—	dB
Two–Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	η	—	40.5	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IRL	—	–12	—	dB

Freescale Semiconductor, Inc.



Z1	0.260" x 0.060" Microstrip	Z11	0.360" x 0.270" Microstrip
Z2	0.240" x 0.060" Microstrip	Z12	0.050" x 0.270" Microstrip
Z3	0.500" x 0.100" Microstrip	Z13	0.110" x 0.060" Microstrip
Z4	0.200" x 0.270" Microstrip	Z14	0.220" x 0.060" Microstrip
Z5	0.330" x 0.270" Microstrip	Z15	0.100" x 0.060" Microstrip
Z6	0.140" x 0.270" x 0.520", Taper	Z16	0.870" x 0.060" Microstrip
Z7	0.040" x 0.520" Microstrip	Z17	0.240" x 0.060" Microstrip
Z8	0.090" x 0.520" Microstrip	Z18	0.340" x 0.060" Microstrip
Z9	0.370" x 0.520" Microstrip (MRF9030MR1)	Board	Taconic RF-35-0300, $\epsilon_r = 3.5$
	0.290" x 0.520" Microstrip (MRF9030MBR1)		
Z10	0.130" x 0.520" Microstrip (MRF9030MR1)		
	0.210" x 0.520" Microstrip (MRF9030MBR1)		

Figure 1. 930–960 MHz Broadband Test Circuit Schematic

Table 1. 930 – 960 MHz Broadband Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1	Short Ferrite Bead, Surface Mount	95F786	Newark
B2	Long Ferrite Bead, Surface Mount	95F787	Newark
C1, C7, C14, C15	47 pF Chip Capacitors, B Case	100B470JP 500X	ATC
C2	0.6–4.5 Variable Capacitor, Gigatrim	44F3360	Newark
C3, C11	3.9 pF Chip Capacitors, B Case	100B3R6BP 500X	ATC
C4, C12	0.8–8.0 Variable Capacitors, Gigatrim	44F3360	Newark
C5, C6	6.8 pF Chip Capacitors, B Case	100B7R5JP 500X	ATC
C8, C16, C17	10 μ F, 35 V Tantalum Chip Capacitors	93F2975	Newark
C9, C10	10 pF Chip Capacitors, B Case	100B100JP 500X	ATC
C13	1.8 pF Chip Capacitor, B Case (MRF9030MR1) 0.6–4.5 Variable Capacitor, Gigatrim (MRF9030MBR1)	100B1R8BP 44F3360	ATC Newark
C18	220 μ F Electrolytic Chip Capacitor	14F185	Newark
L1, L2	12.5 nH Coilcraft Inductors	A04T-5	Coilcraft
WB1, WB2	20 mil Brass Shim (0.250 x 0.250)	RF-Design Lab	RF-Design Lab
PCB	Etched Circuit Board	900 MHz μ 250/Viper Rev 02	DSelectronics

Freescale Semiconductor, Inc.

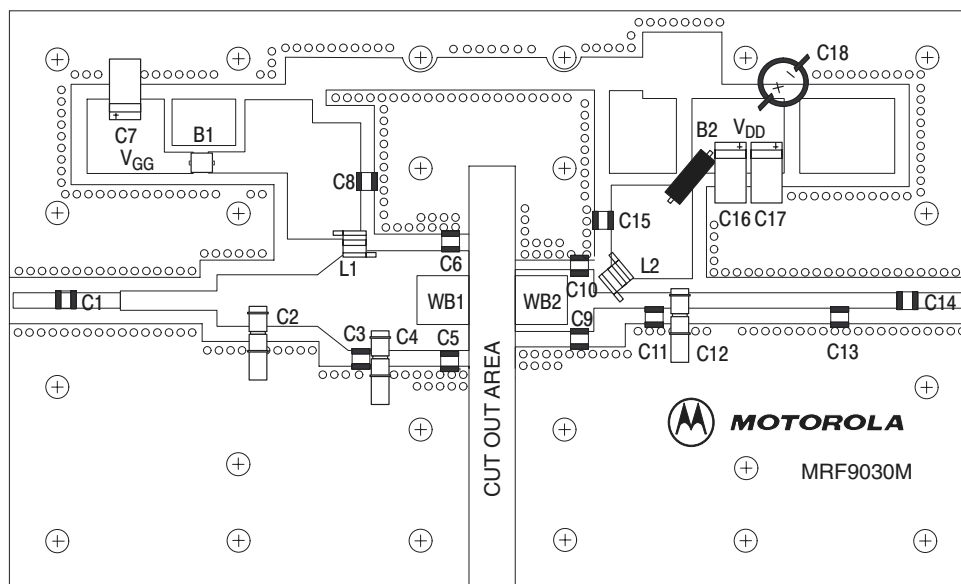


Figure 2. 930–960 MHz Broadband Test Circuit Component Layout (MRF9030MR1)

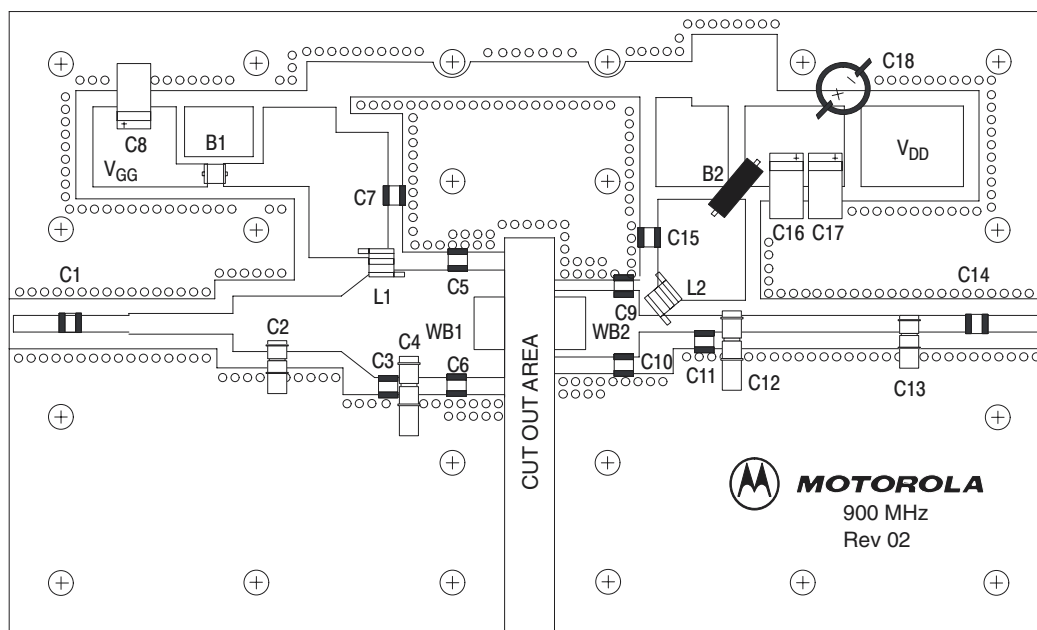


Figure 3. 930–960 MHz Broadband Test Circuit Component Layout (MRF9030MBR1)

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

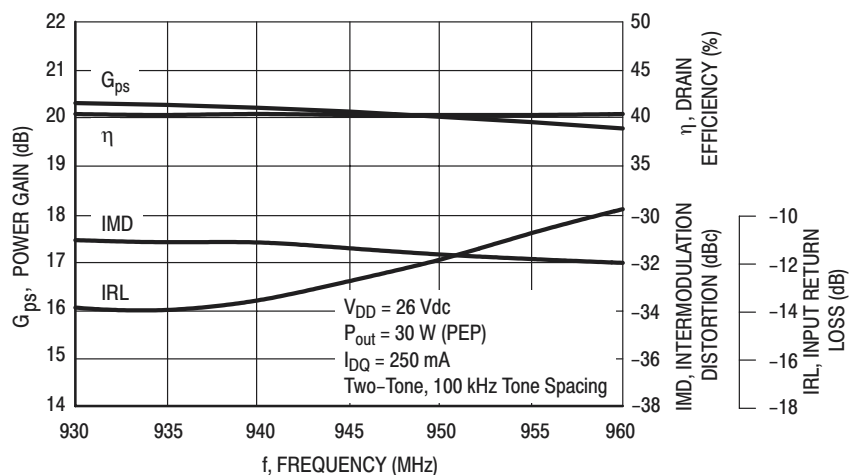


Figure 4. Class AB Broadband Circuit Performance

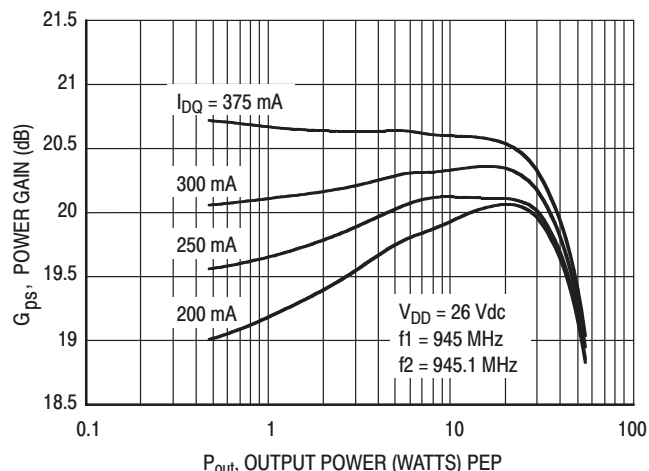


Figure 5. Power Gain versus Output Power

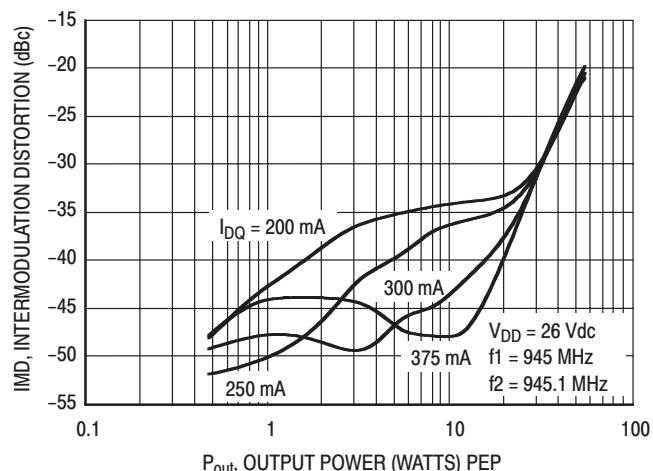


Figure 6. Intermodulation Distortion versus Output Power

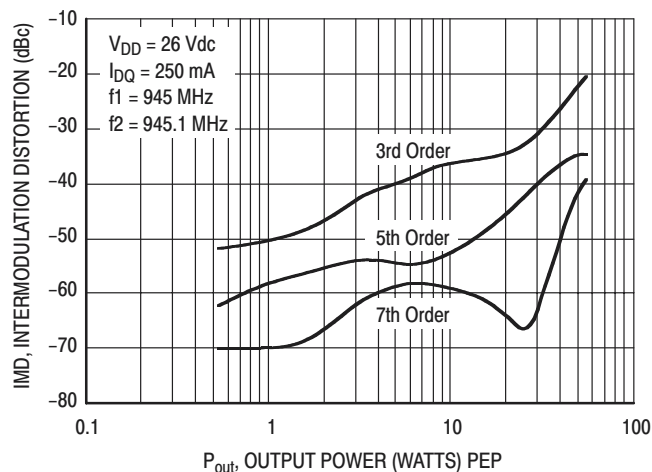


Figure 7. Intermodulation Distortion Products versus Output Power

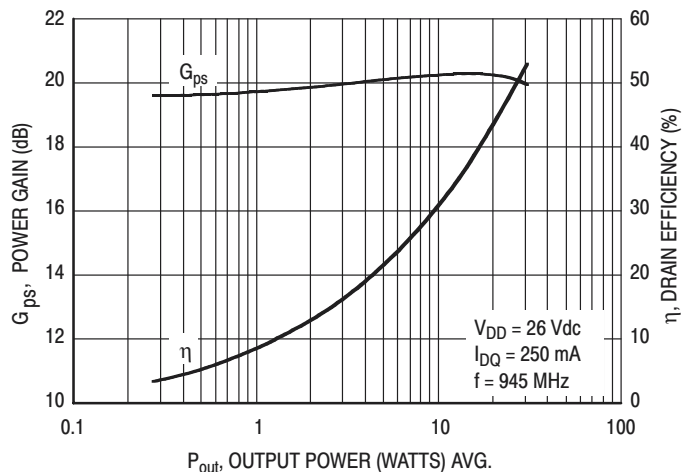


Figure 8. Power Gain and Efficiency versus Output Power

Freescale Semiconductor, Inc.

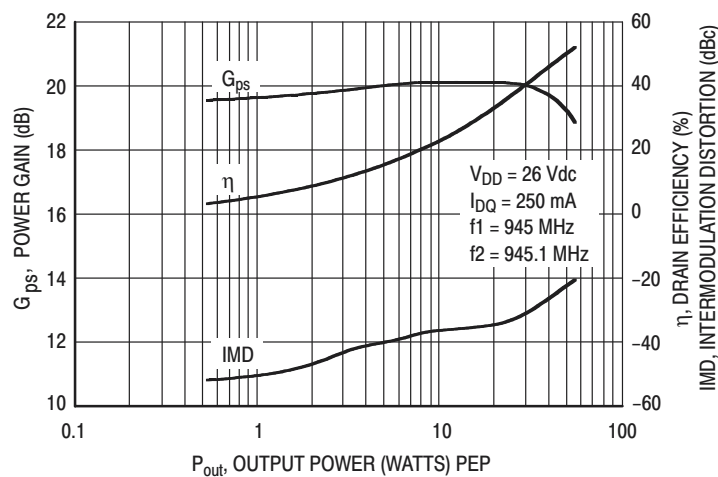
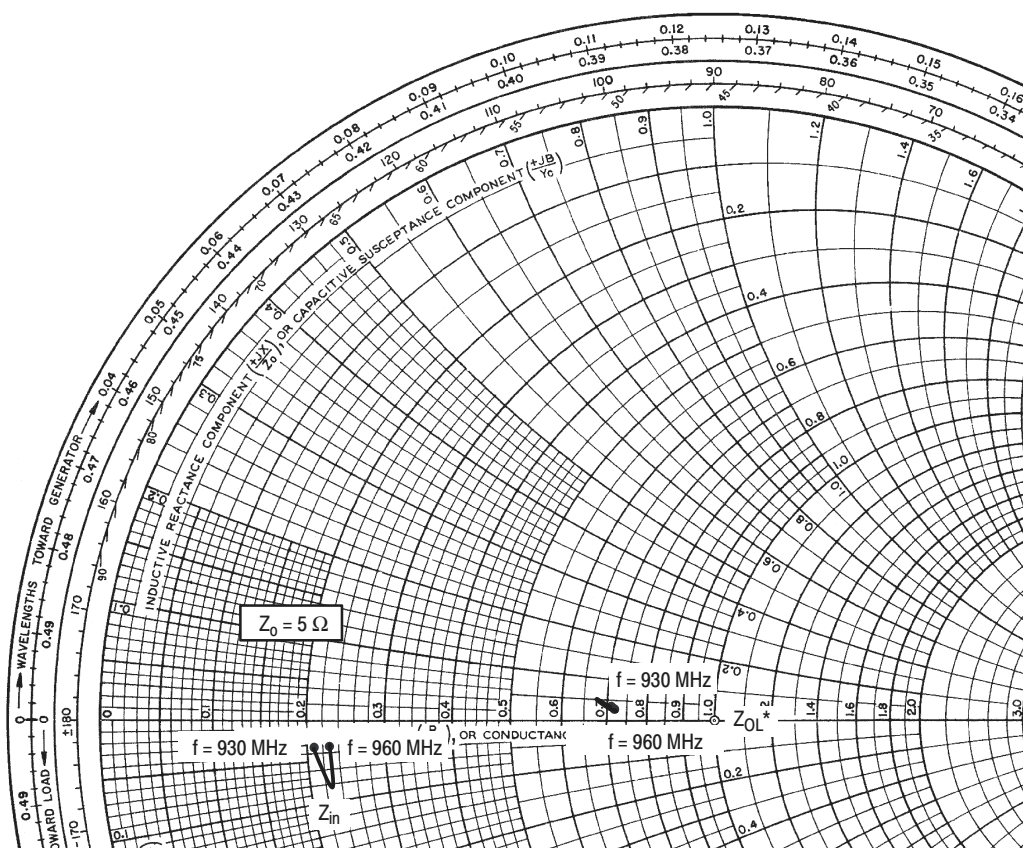


Figure 9. Power Gain, Efficiency and IMD versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 30 \text{ Watts (PEP)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
930	$1.07 - j0.160$	$3.53 + j0.20$
945	$1.14 - j0.385$	$3.41 + j0.24$
960	$1.17 - j0.170$	$3.60 + j0.17$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

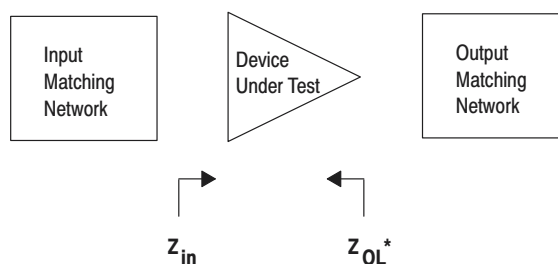
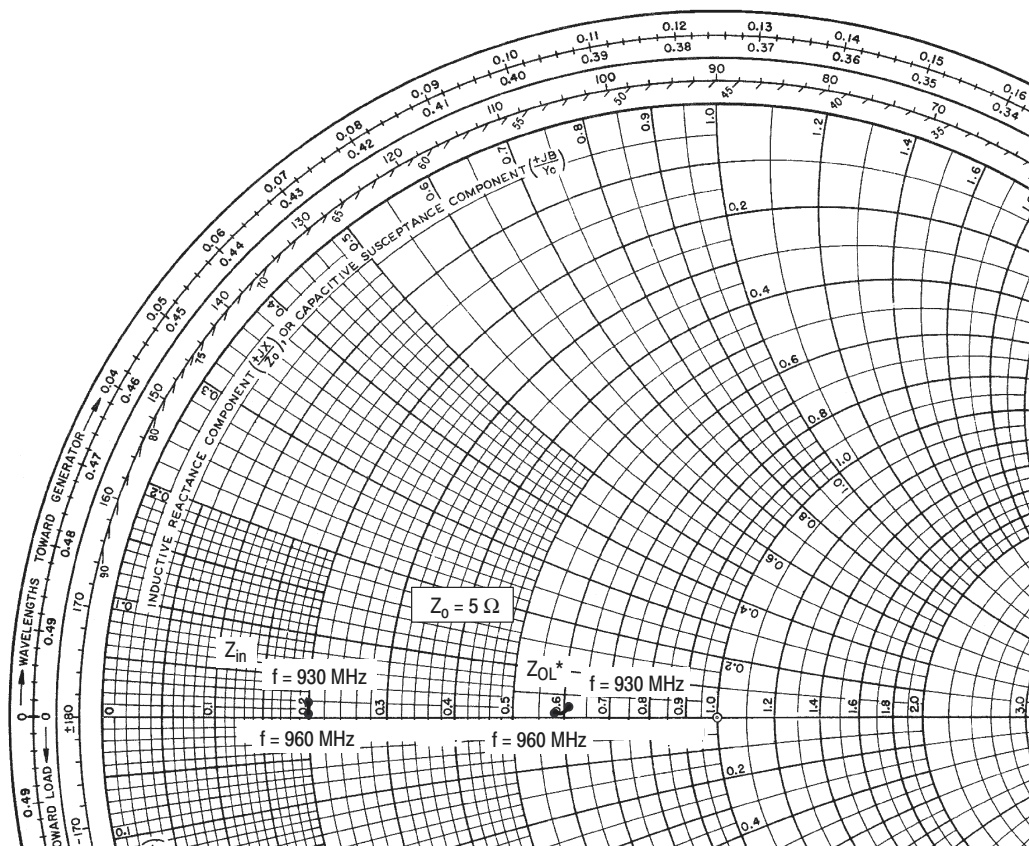


Figure 10. Series Equivalent Input and Output Impedance (MRF9030MR1)



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 30 \text{ Watts (PEP)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
930	$1.0 + j0.18$	$3.05 + j0.09$
945	$1.0 + j0.10$	$3.00 + j0.07$
960	$1.0 + j0.03$	$2.95 + j0.03$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

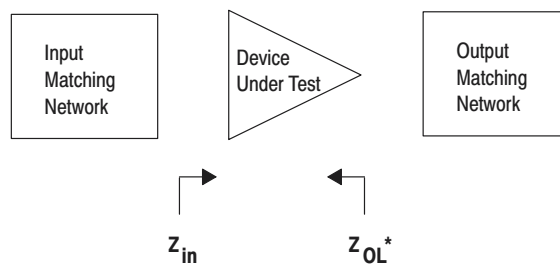


Figure 11. Series Equivalent Input and Output Impedance (MRF9030MBR1)

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

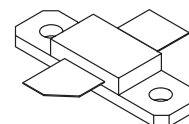
Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

- Typical Two-Tone Performance at 945 MHz, 28 Volts
Output Power — 45 Watts PEP
Power Gain — 18.8 dB
Efficiency — 42%
IMD — -32 dBc
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 945 MHz, 45 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

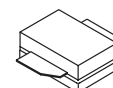
MRF9045R1

MRF9045LSR1

945 MHz, 45 W, 28 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B-05, STYLE 1
NI-360
MRF9045R1



CASE 360C-05, STYLE 1
NI-360S
MRF9045LSR1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	125 0.71 175 1	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4 1.0	$^\circ\text{C/W}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

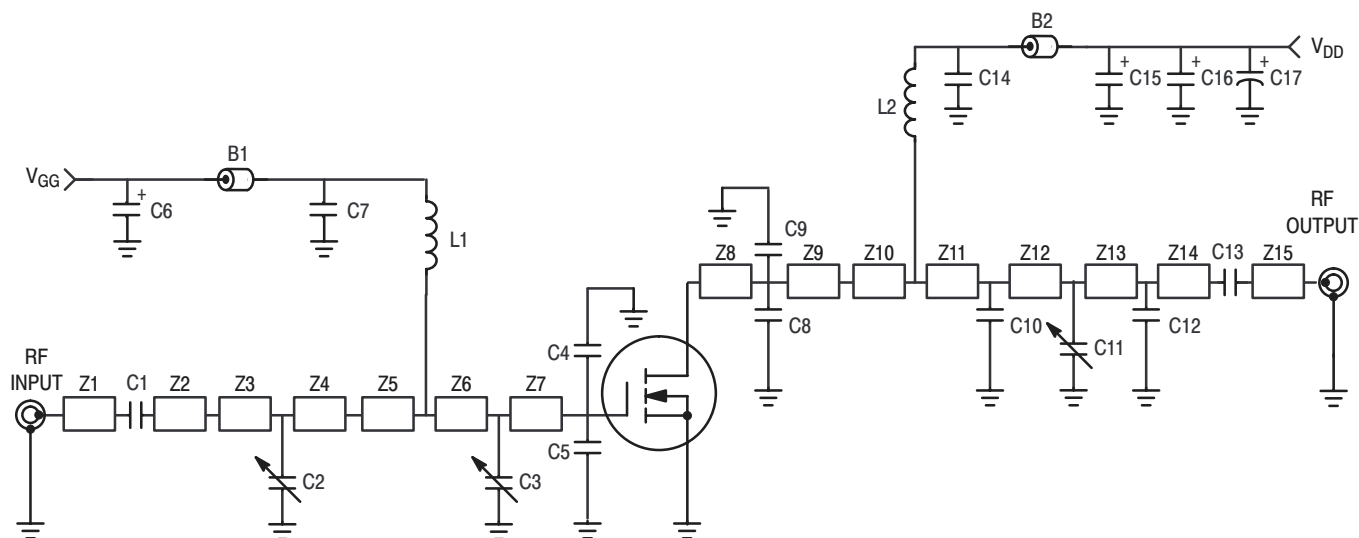
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μA _{dc}
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μA _{dc}
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μA _{dc}
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 150 μA _{dc})	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 350 mA _{dc})	V _{GS(Q)}	—	3.7	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 A _{dc})	V _{DS(on)}	—	0.19	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 A _{dc})	g _{fs}	—	4	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms) _{ac} @ 1 MHz, V _{GS} = 0 Vdc)	C _{iss}	—	69	—	pF
Output Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms) _{ac} @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	37	—	pF
Reverse Transfer Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms) _{ac} @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	1.5	—	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	G _{ps}	17	18.8	—	dB
Two-Tone Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	η	38	42	—	%
3rd Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IMD	—	−32	−28	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IRL	—	−14	−9	dB
Two-Tone Common-Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	G _{ps}	—	18.5	—	dB
Two-Tone Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	η	—	41	—	%
3rd Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IMD	—	−33	—	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IRL	—	13	—	dB
Power Output, 1 dB Compression Point (V _{DD} = 28 Vdc, P _{out} = 45 W CW, I _{DQ} = 350 mA, f ₁ = 945.0 MHz)	P _{1dB}	—	55	—	W
Common-Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 45 W CW, I _{DQ} = 350 mA, f ₁ = 945.0 MHz)	G _{ps}	—	18	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 45 W CW, I _{DQ} = 350 mA, f ₁ = 945.0 MHz)	η	—	60	—	%
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 45 W CW, I _{DQ} = 350 mA, f = 945.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			

Freescale Semiconductor, Inc.



B1	Short Ferrite Bead Surface Mount	Z4	0.360" x 0.320" Microstrip
B2	Long Ferrite Bead Surface Mount	Z5	0.240" x 0.320" x 0.620", Taper
C1, C7, C13, C14	47 pF Chip Capacitors, B Case	Z6	0.140" x 0.620" Microstrip
C2, C3, C11	0.8–8.0 pF Gigatrim Variable Trim Capacitors	Z7	0.510" x 0.620" Microstrip
C4, C5, C8, C9	10 pF Chip Capacitors, B Case	Z8	0.330" x 0.320" Microstrip
C6, C15, C16	10 μ F, 35 V Tantalum Surface Mount Chip Capacitors	Z9	0.140" x 0.320" Microstrip
C10	2.2 pF Chip Capacitor, B Case	Z10	0.070" x 0.080" Microstrip
C12	0.7 pF Chip Capacitor, B Case – MRF9045LS	Z11	0.240" x 0.080" Microstrip
C17	220 μ F, 50 V Electrolytic Capacitor	Z12	0.140" x 0.080" Microstrip
L1, L2	12.5 nH Surface Mount Inductors, Coilcraft	Z13	0.930" x 0.080" Microstrip
Z1	0.260" x 0.080" Microstrip	Z14	0.180" x 0.080" Microstrip
Z2	0.610" x 0.120" Microstrip	Z15	0.350" x 0.080" Microstrip
Z3	0.260" x 0.320" Microstrip	PCB	Arlon GX-0300-55-22, 0.03", $\epsilon_r = 2.55$

Figure 1. 930 – 960 MHz Broadband Test Circuit Schematic

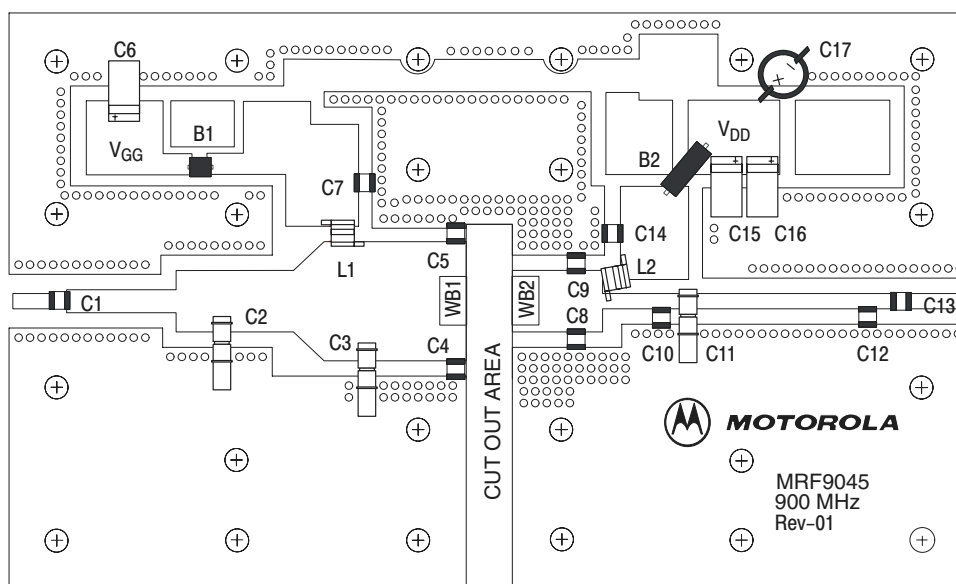


Figure 2. 930 – 960 MHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

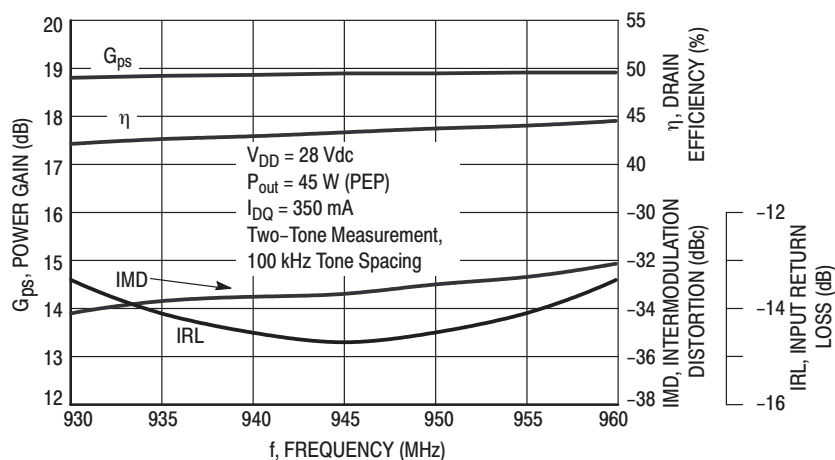


Figure 3. Class AB Broadband Circuit Performance

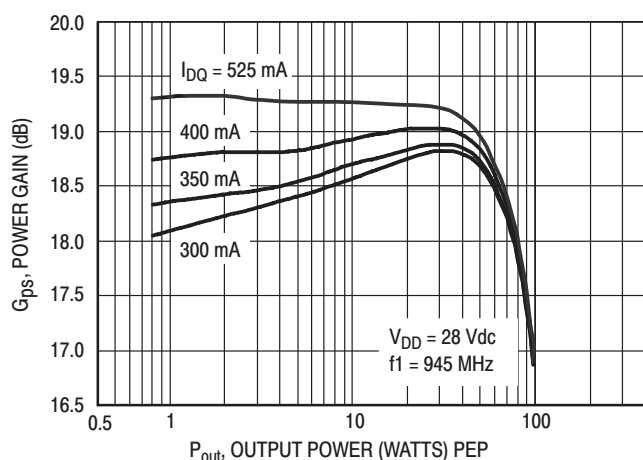


Figure 4. Power Gain versus Output Power

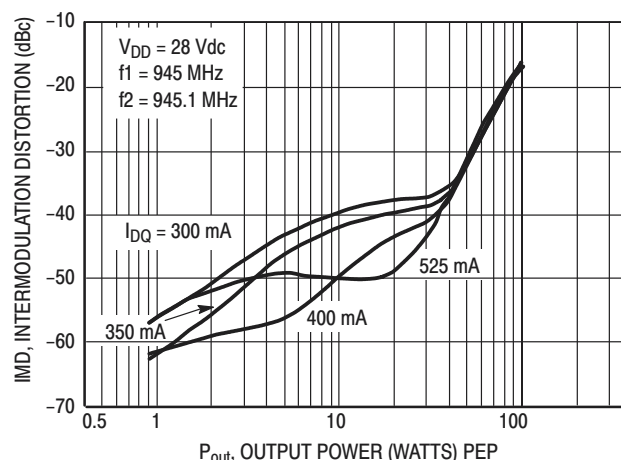


Figure 5. Intermodulation Distortion versus Output Power

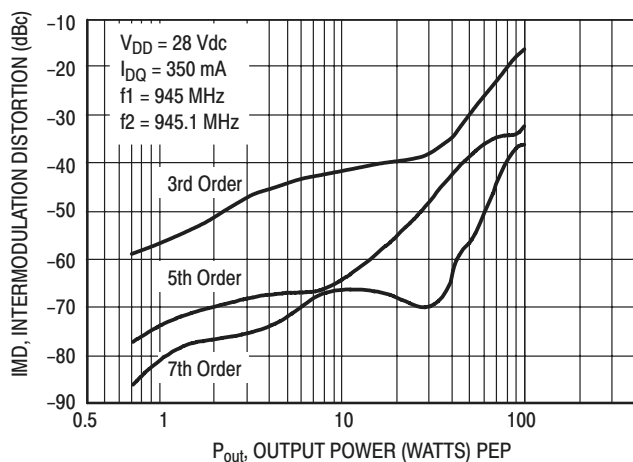


Figure 6. Intermodulation Distortion Products versus Output Power

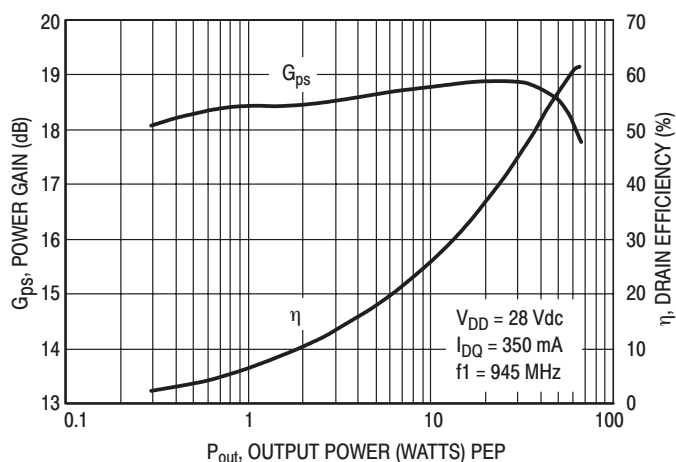
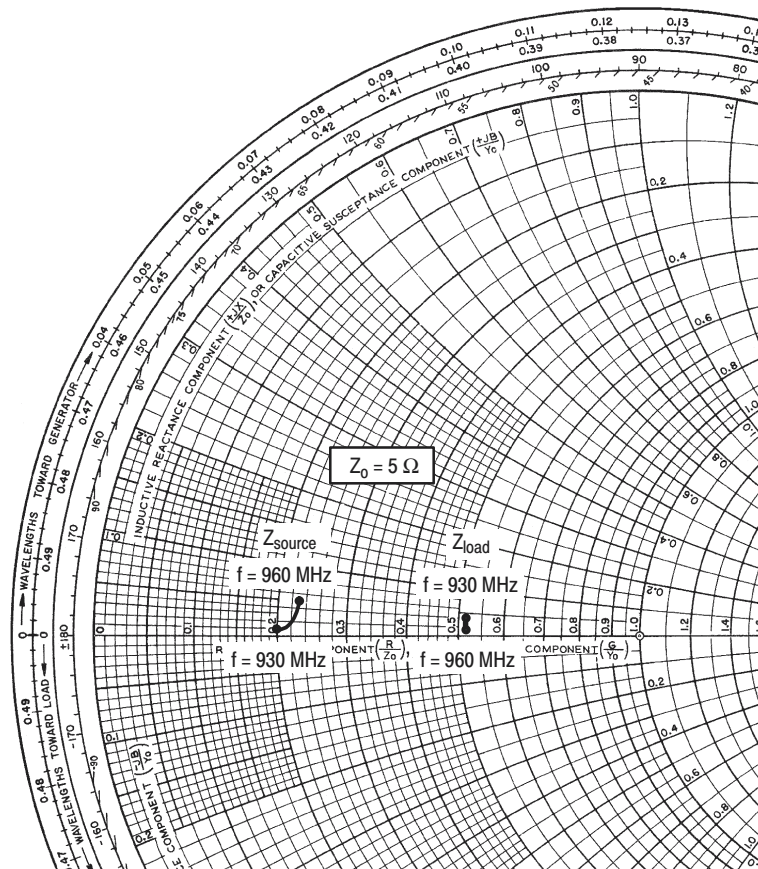


Figure 7. Power Gain, Efficiency versus Output Power



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 350 \text{ mA}$, $P_{out} = 45 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
930	$1.02 + j0.06$	$2.6 + j0.20$
945	$1.10 + j0.11$	$2.6 + j0.16$
960	$1.15 + j0.25$	$2.6 + j0.10$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

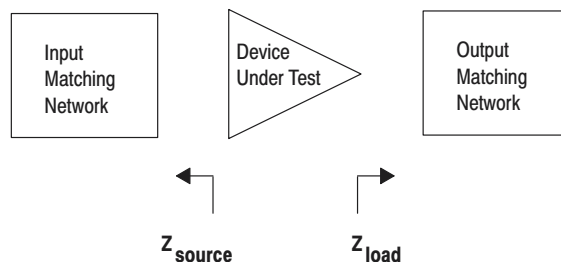


Figure 8. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

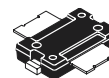
Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

- Typical Performance at 945 MHz, 28 Volts
Output Power — 45 Watts PEP
Power Gain — 19 dB
Efficiency — 41% (Two Tones)
IMD — -31 dBc
- Integrated ESD Protection
- Guaranteed Ruggedness @ Load VSWR = 5:1, @ 28 Vdc, 945 MHz, 45 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Moisture Sensitivity Level 3
- Dual-Lead Bolt-down Plastic Package Can Also Be Used As Surface Mount.
- TO-272 Available in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.
- TO-270 Available in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

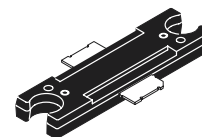
MRF9045MR1

MRF9045MBR1

945 MHz, 45 W, 28 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 1265-07, STYLE 1
TO-270
PLASTIC
MRF9045MR1



CASE 1337-02, STYLE 1
TO-272 DUAL LEAD
PLASTIC
MRF9045MBR1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	177 1.18	Watts $W/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.85	$^\circ\text{C/W}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 150 μAdc)	V _{GS(th)}	2	2.8	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 350 mA)	V _{GS(Q)}	3	3.7	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.22	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 Adc)	g _{fs}	—	4	—	S

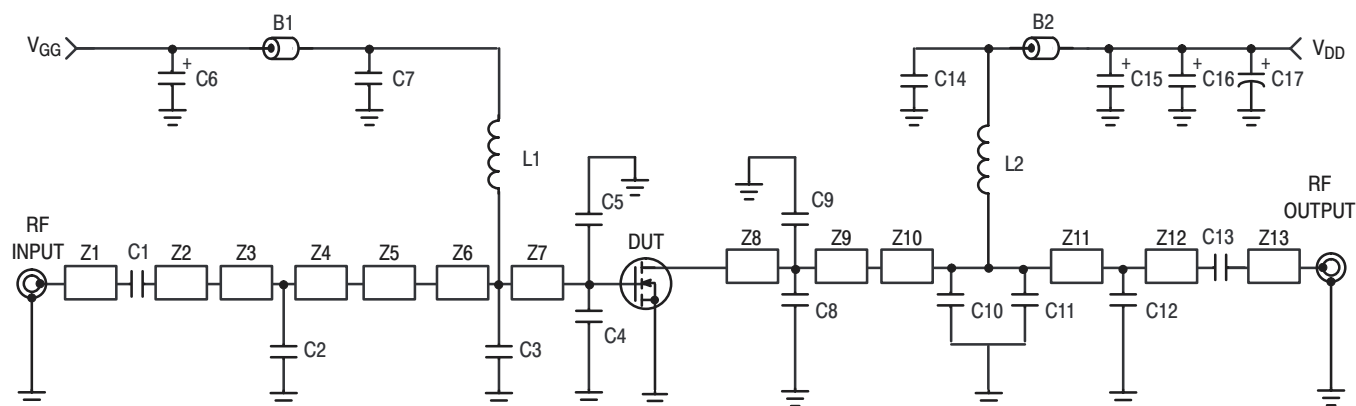
DYNAMIC CHARACTERISTICS

Input Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{iss}	—	70	—	pF
Output Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	38	—	pF
Reverse Transfer Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	1.7	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	G _{ps}	17	19	—	dB
Two–Tone Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	η	38	41	—	%
3rd Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IRL	—	–14	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	G _{ps}	—	19	—	dB
Two–Tone Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	η	—	41	—	%
3rd Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 45 W PEP, I _{DQ} = 350 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IRL	—	–13	—	dB

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Beads, Surface Mount	Z3	0.14" x 0.32" Microstrip
C1, C7, C13, C14	47 pF Chip Capacitors, B Case	Z4	0.47" x 0.32" Microstrip
C2, C8	2.7 pF Chip Capacitors, B Case	Z5	0.16" x 0.32" x 0.62" Taper
C3	3.9 pF Chip Capacitor, B Case	Z6	0.18" x 0.62" Microstrip
C4, C5, C8, C9	10 pF Chip Capacitors, B Case	Z7	0.56" x 0.62" Microstrip
C6, C15, C16	10 μ F, 35 V Tantalum Surface Mount Capacitors	Z8	0.33" x 0.32" Microstrip
C10	2.2 pF Chip Capacitor, B Case	Z9	0.14" x 0.32" Microstrip
C11	4.7 pF Chip Capacitor, B Case	Z10	0.36" x 0.08" Microstrip
C12	1.2 pF Chip Capacitor, B Case	Z11	1.01" x 0.08" Microstrip
C17	220 μ F, 50 V Electrolytic Capacitor	Z12	0.15" x 0.08" Microstrip
L1, L2	12.5 nH Inductors	Z13	0.29" x 0.08" Microstrip
Z1	0.20" x 0.08" Microstrip		
Z2	0.57" x 0.12" Microstrip		

Figure 1. MRF9045MR1 930–960 MHz Broadband Test Circuit Schematic

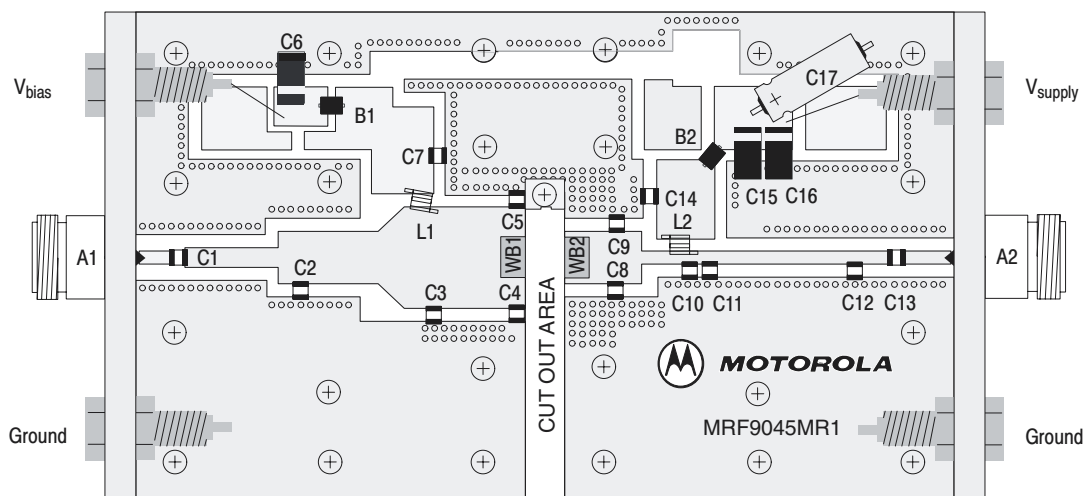
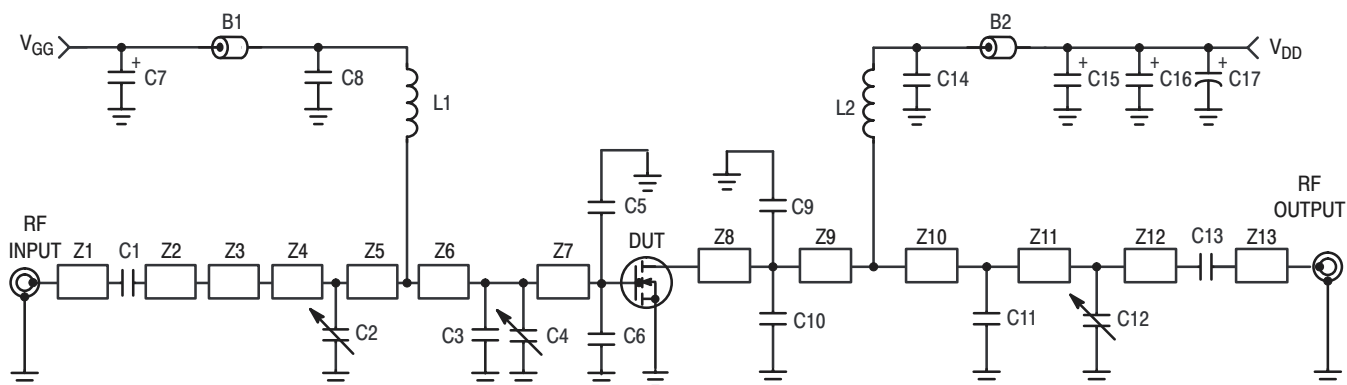


Figure 2. MRF9045MR1 930–960 MHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.



B1	Short Ferrite Bead	Z1	0.260" x 0.060" Microstrip
B2	Long Ferrite Bead	Z2	0.240" x 0.060" Microstrip
C1, C8, C13, C14	47 pF Chip Capacitors, B Case	Z3	0.500" x 0.100" Microstrip
C2	0.4–2.5 pF Variable Capacitor, Johanson Gigatrim	Z4	0.215" x 0.270" Microstrip
C3	3.6 pF Chip Capacitor, B Case	Z5	0.315" x 0.270" Microstrip
C4	0.8–8.0 pF Variable Capacitor, Johanson Gigatrim	Z6	0.160" x 0.270" x 0.520" Taper
C5, C6, C9, C10	10 pF Chip Capacitors, B Case	Z7	0.285" x 0.520" Microstrip
C7, C15, C16	10 μ F, 35 V Tantalum Chip Capacitors	Z8	0.140" x 0.270" Microstrip
C11	7.5 pF Chip Capacitor, B Case	Z9	0.450" x 0.270" Microstrip
C12	0.6–4.5 pF Variable Capacitor, Johanson Gigatrim	Z10	0.250" x 0.060" Microstrip
C17	220 μ F Electrolytic Chip Capacitor	Z11	0.720" x 0.060" Microstrip
L1, L2	12.5 nH Surface Mount Inductors	Z12	0.490" x 0.060" Microstrip
WB1, WB2	10 mil Brass Wear Blocks	Z13	0.290" x 0.060" Microstrip
		Board	Taconic RF-35-0300, $\epsilon_r = 3.5$

Figure 3. MRF9045MBR1 930–960 MHz Broadband Test Circuit Schematic

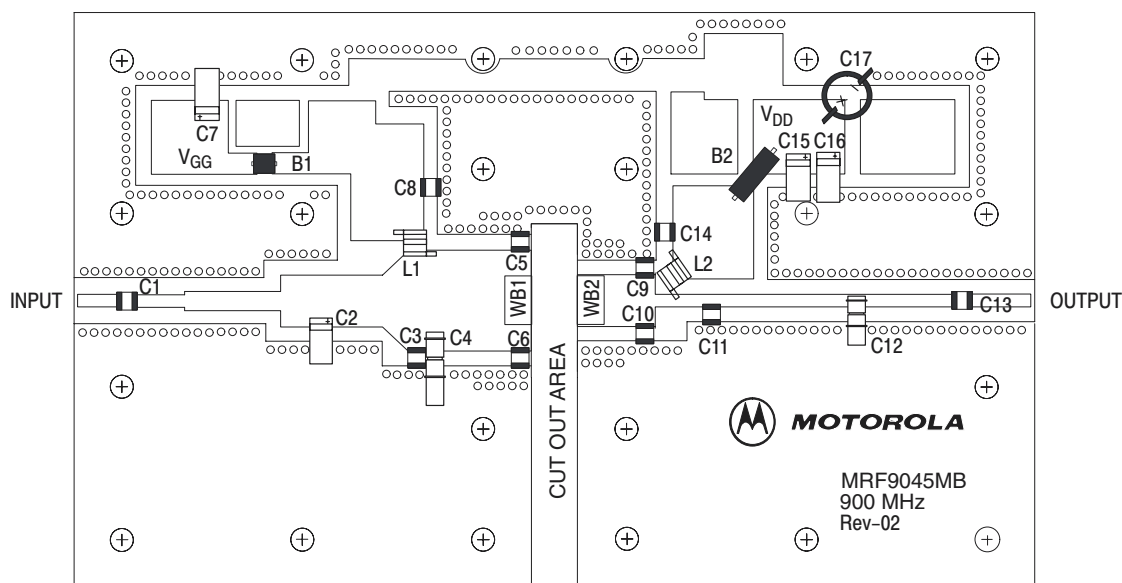


Figure 4. MRF9045MBR1 930–960 MHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

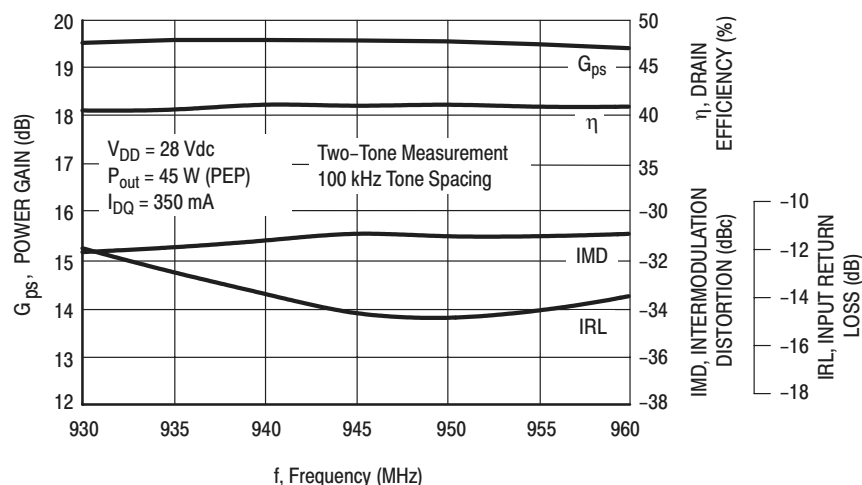


Figure 5. Class AB Broadband Circuit Performance

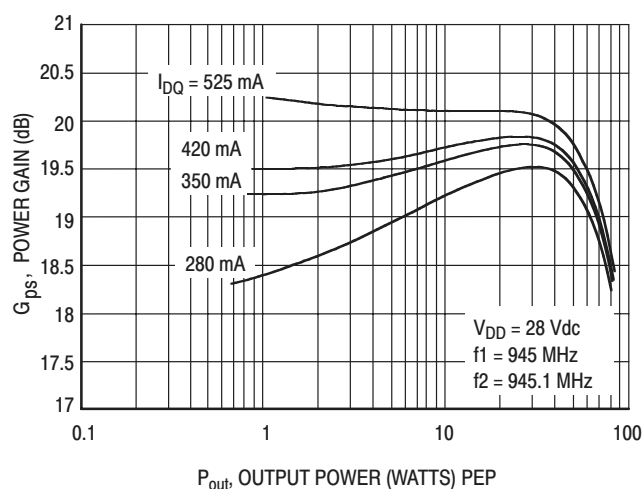


Figure 6. Power Gain versus Output Power

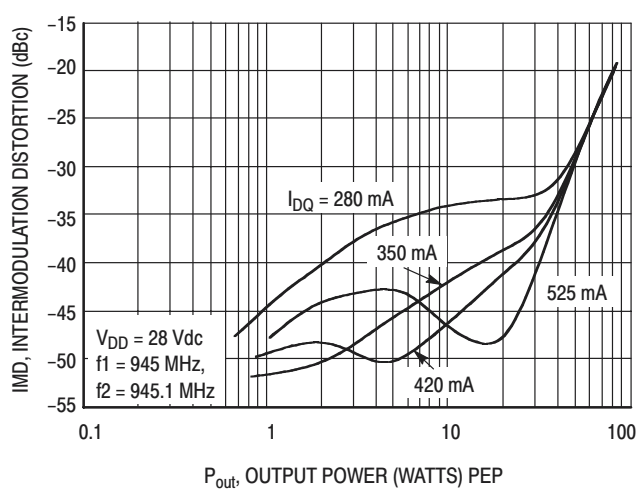


Figure 7. Intermodulation Distortion versus Output Power

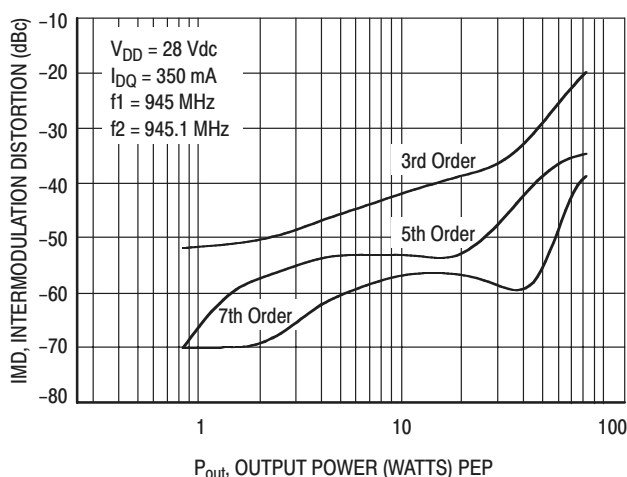


Figure 8. Intermodulation Distortion Products versus Output Power

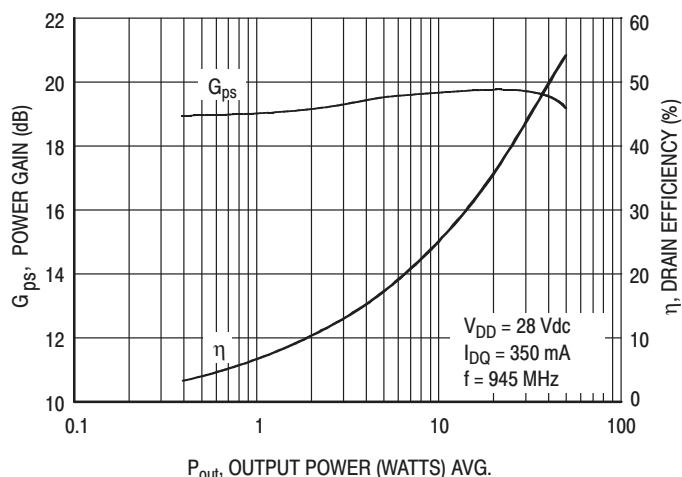


Figure 9. Power Gain and Efficiency versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

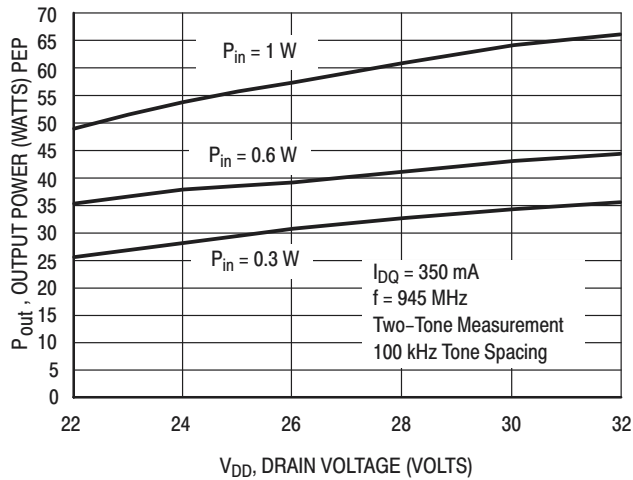


Figure 10. Output Voltage versus Supply Voltage (MRF9045MR1)

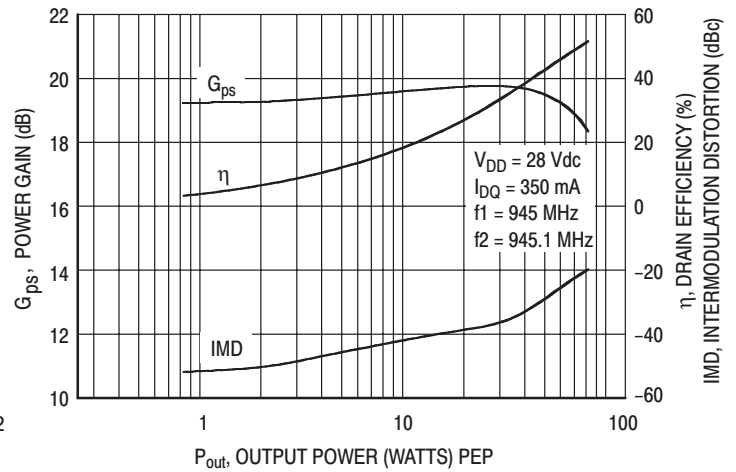
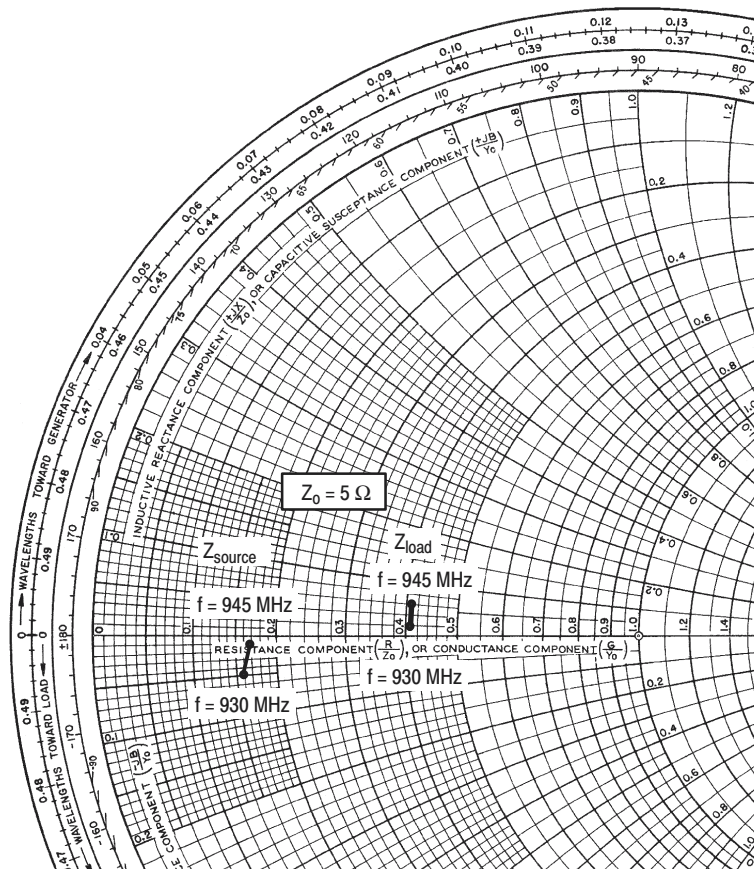


Figure 11. Power Gain, Efficiency and IMD versus Output Power (MRF9045MR1)



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 350 \text{ mA}$, $P_{out} = 45 \text{ W (PEP)}$

f MHz	Z_{source} Ω	Z_{load} Ω
930	$0.81 - j0.25$	$2.03 + j0.09$
945	$0.85 - j0.05$	$2.03 + j0.28$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

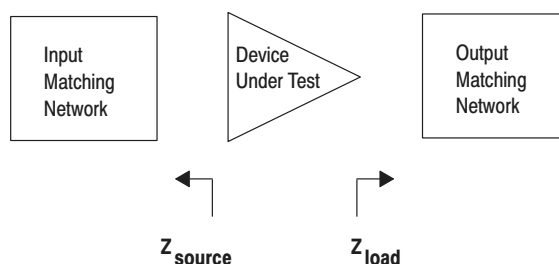
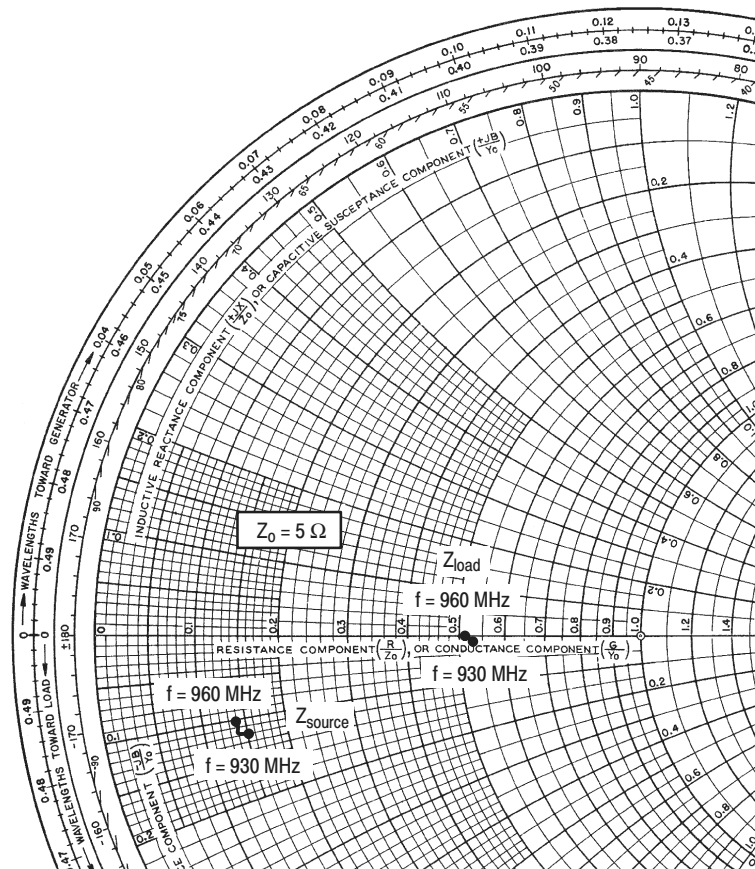


Figure 12. Series Equivalent Input and Output Impedance (MRF9045MR1)



$V_{\text{DD}} = 28 \text{ V}$, $I_{\text{DQ}} = 350 \text{ mA}$, $P_{\text{out}} = 45 \text{ W (PEP)}$

f MHz	Z_{source} Ω	Z_{load} Ω
930	$0.75 - j0.6$	$2.65 - j0.05$
945	$0.72 - j0.6$	$2.60 - j0.05$
960	$0.70 - j0.5$	$2.55 - j0.02$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

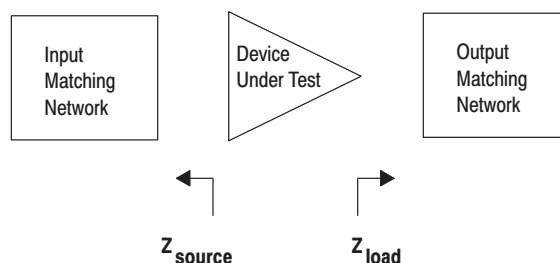


Figure 13. Series Equivalent Input and Output Impedance (MRF9045MBR1)

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

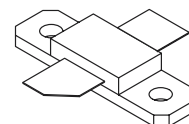
Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

- Typical Two-Tone Performance at 945 MHz, 26 Volts
Output Power — 60 Watts PEP
Power Gain — 17 dB
Efficiency — 40%
IMD — -31 dBc
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 945 MHz, 60 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

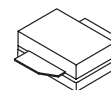
MRF9060R1

MRF9060LSR1

945 MHz, 60 W, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B-05, STYLE 1
NI-360
MRF9060R1



CASE 360C-05, STYLE 1
NI-360S
MRF9060LSR1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	159 0.91 219 1.25	Watts $W/^\circ\text{C}$ Watts $W/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1 0.8	$^\circ\text{C/W}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

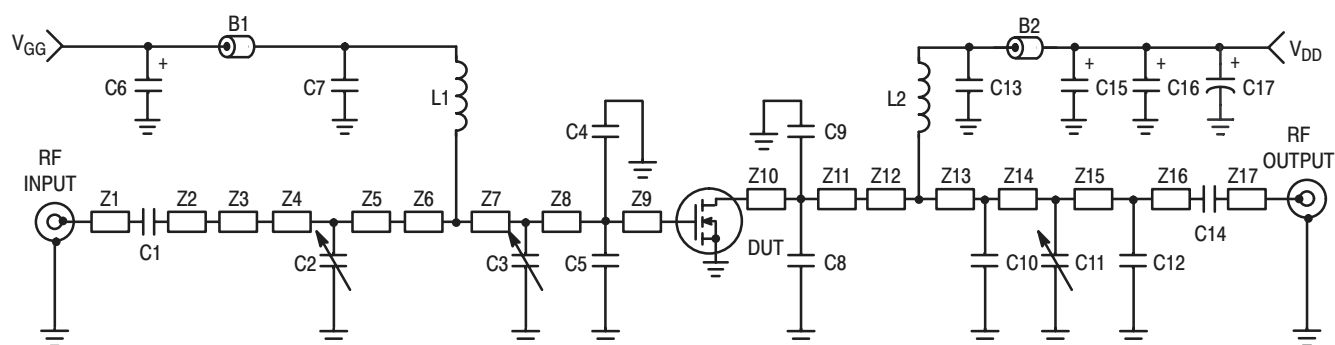
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μA _{dc}
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μA _{dc}
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μA _{dc}
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 μA _{dc})	V _{GS(th)}	2	2.9	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 450 mA _{dc})	V _{GS(Q)}	—	3.7	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1.3 A _{dc})	V _{DS(on)}	—	0.17	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 4 A _{dc})	g _{fs}	—	5.3	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{iss}	—	98	—	pF
Output Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	50	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	2	—	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	G _{ps}	16	17	—	dB
Two-Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	η	36	40	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IMD	—	−31	−28	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IRL	—	−16	−9	dB
Two-Tone Common-Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	G _{ps}	—	17	—	dB
Two-Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	η	—	39	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IMD	—	−31	—	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IRL	—	−16	—	dB
Power Output, 1 dB Compression Point (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 450 mA, f ₁ = 945.0 MHz)	P _{1dB}	—	70	—	W
Common-Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 450 mA, f ₁ = 945.0 MHz)	G _{ps}	—	17	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 450 mA, f ₁ = 945.0 MHz)	η	—	51	—	%
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 450 mA, f = 945.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			

Freescale Semiconductor, Inc.



Z1	0.240" x 0.060" Microstrip	Z10	0.360" x 0.270" Microstrip
Z2	0.240" x 0.060" Microstrip	Z11	0.060" x 0.270" Microstrip
Z3	0.500" x 0.100" Microstrip	Z12	0.110" x 0.060" Microstrip
Z4	0.180" x 0.270" Microstrip	Z13	0.330" x 0.060" Microstrip
Z5	0.350" x 0.270" Microstrip	Z14	0.230" x 0.060" Microstrip
Z6	0.270" x 0.520 x 0.140" Taper	Z15	0.740" x 0.060" Microstrip
Z7	0.170" x 0.520" Microstrip	Z16	0.130" x 0.060" Microstrip
Z8	0.410" x 0.520" Microstrip	Z17	0.340" x 0.060" Microstrip
Z9	0.060" x 0.520" Microstrip	PCB	Taconic RF-35-0300, 30 mil, $\epsilon_r = 3.55$

Figure 1. 945 MHz Broadband Test Circuit Schematic

Table 1. 945 MHz Broadband Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1	Short Ferrite Bead	95F786	Newark
B2	Long Ferrite Bead	95F787	Newark
C1, C7, C13, C14	47 pF Chip Capacitors, B Case	100B470JP 500X	ATC
C2, C3, C11	0.8–8.0 Gigatrim Variable Capacitors	44F3360	Newark
C4, C5, C8, C9	10 pF Chip Capacitors, B Case	100B100JP 500X	ATC
C6, C15, C16	10 μ F, 35 V Tantalum Chip Capacitor	93F2975	Newark
C10	3.0 pF Chip Capacitor, B Case	100B3R0JP 500X	ATC
C12	0.5 pF Chip Capacitor, B Case (MRF9060) 0.7 pF Chip Capacitor, B Case (MRF9060S)	100B0R5BP 500X 100B0R7BP 500X	ATC ATC
C17	220 μ F Electrolytic Chip Capacitor	14F185	Newark
L1, L2	12.5 nH Inductors	A04T-5	Coilcraft
N1, N2	N-Type Panel Mount, Stripline	3052-1648-10	Avnet
WB1, WB2	10 mil Brass Wear Blocks		

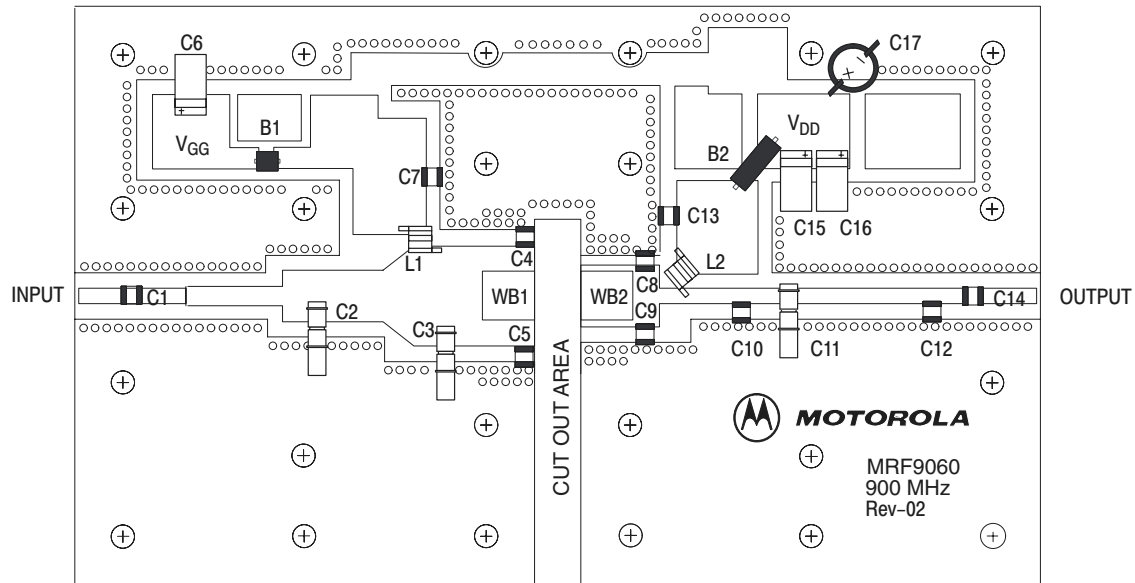


Figure 2. 930 – 960 MHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

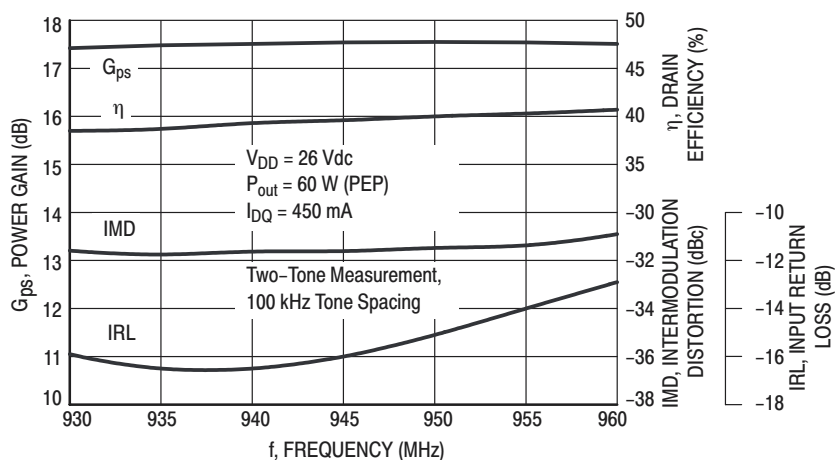


Figure 3. Class AB Broadband Circuit Performance

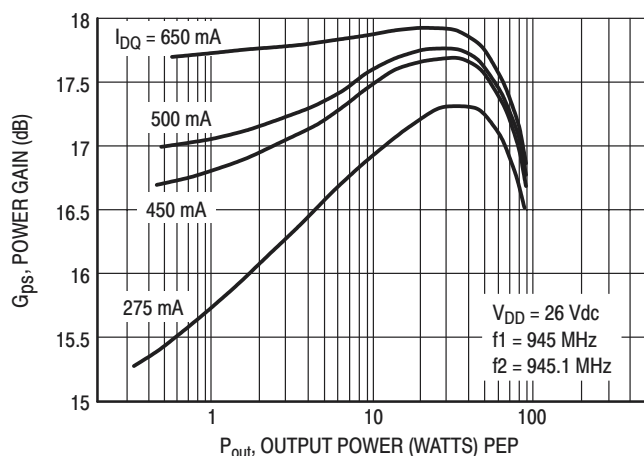


Figure 4. Power Gain versus Output Power

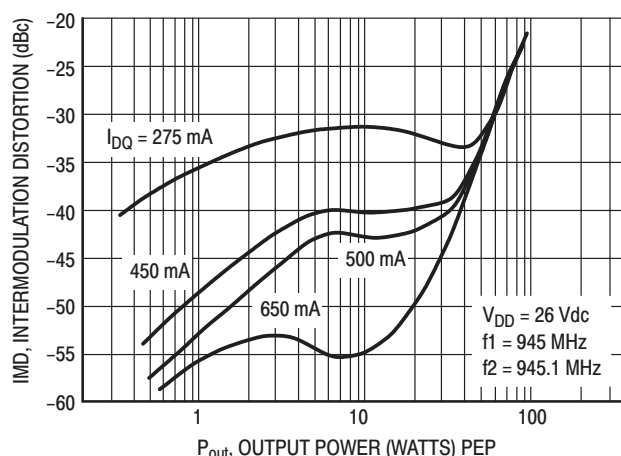


Figure 5. Intermodulation Distortion versus Output Power

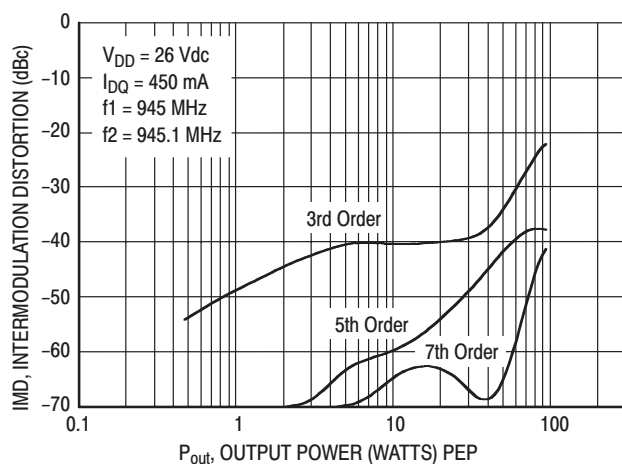


Figure 6. Intermodulation Distortion Products versus Output Power

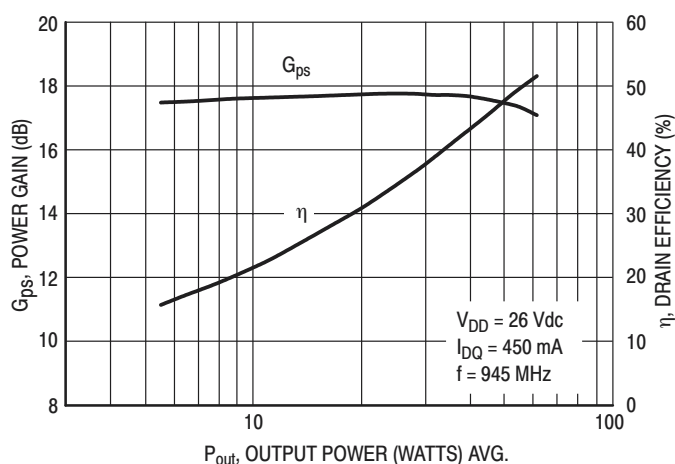


Figure 7. Power Gain and Efficiency versus Output Power

Freescal Semiconductor, Inc.

TYPICAL CHARACTERISTICS

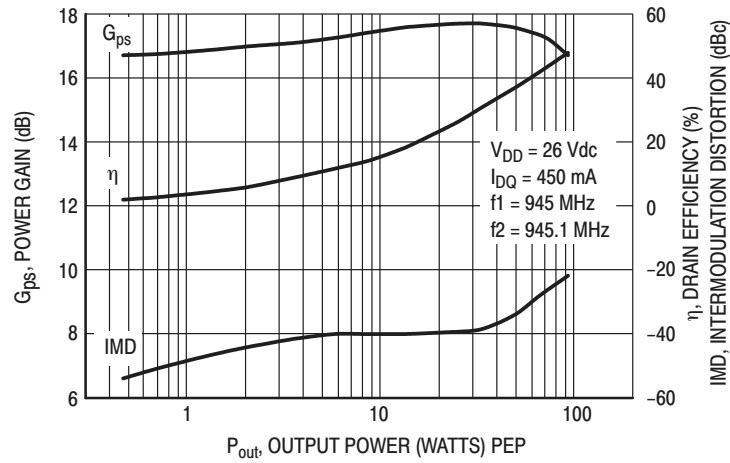
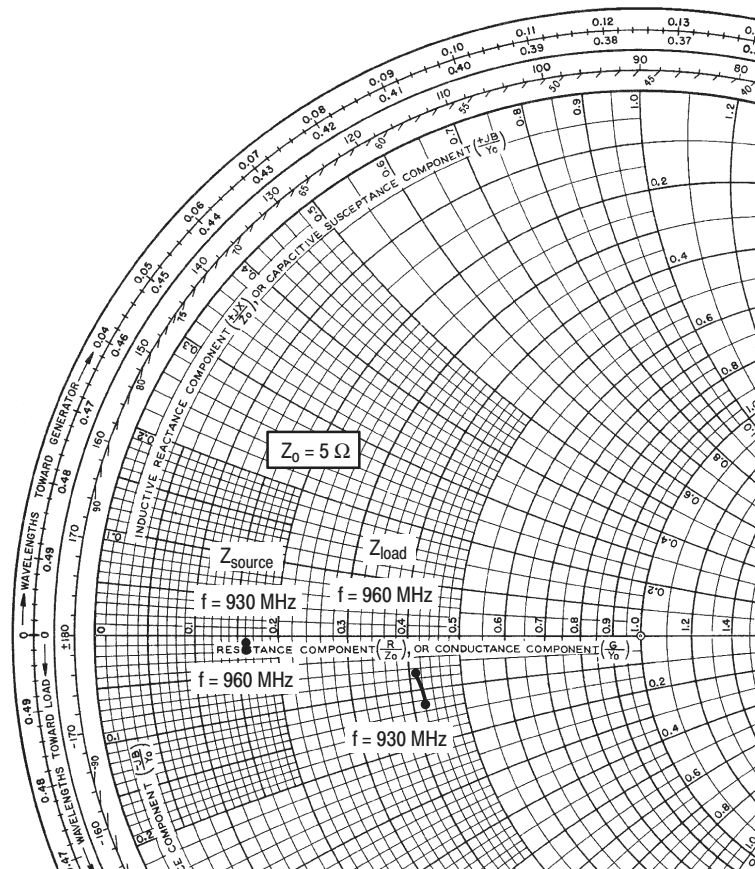


Figure 8. Power Gain, Efficiency, and IMD versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 450 \text{ mA}$, $P_{out} = 60 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
930	$0.80 - j0.10$	$2.08 - j0.65$
945	$0.80 - j0.05$	$2.07 - j0.38$
960	$0.81 - j0.10$	$2.04 - j0.37$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

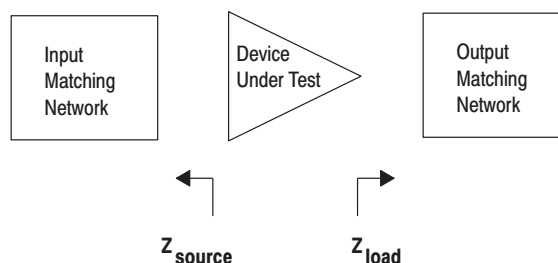


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

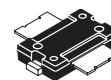
Designed for broadband commercial and industrial applications with frequencies up to 1.0 GHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

- Typical Performance at 945 MHz, 26 Volts
 Output Power — 60 Watts PEP
 Power Gain — 18.0 dB
 Efficiency — 40% (Two Tones)
 IMD — -31.5 dBc
- Integrated ESD Protection
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 945 MHz, 60 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- TO-270 Dual Lead Available in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.
- TO-272 Dual Lead Available in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

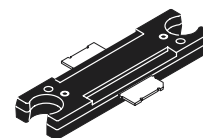
MRF9060MR1

MRF9060MBR1

945 MHz, 60 W, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 1265-08, STYLE 1
TO-270 DUAL LEAD
PLASTIC
MRF9060MR1



CASE 1337-02, STYLE 1
TO-272 DUAL LEAD
PLASTIC
MRF9060MBR1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	223 1.79	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.56	$^\circ\text{C/W}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)
Charge Device Model	C6 (Minimum) C5 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	1 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 μAdc)	V _{GS(th)}	2	2.8	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 450 mAdc)	V _{GS(Q)}	3	3.7	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1.3 Adc)	V _{DS(on)}	—	0.21	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 4 Adc)	g _{fs}	—	5.3	—	S

DYNAMIC CHARACTERISTICS

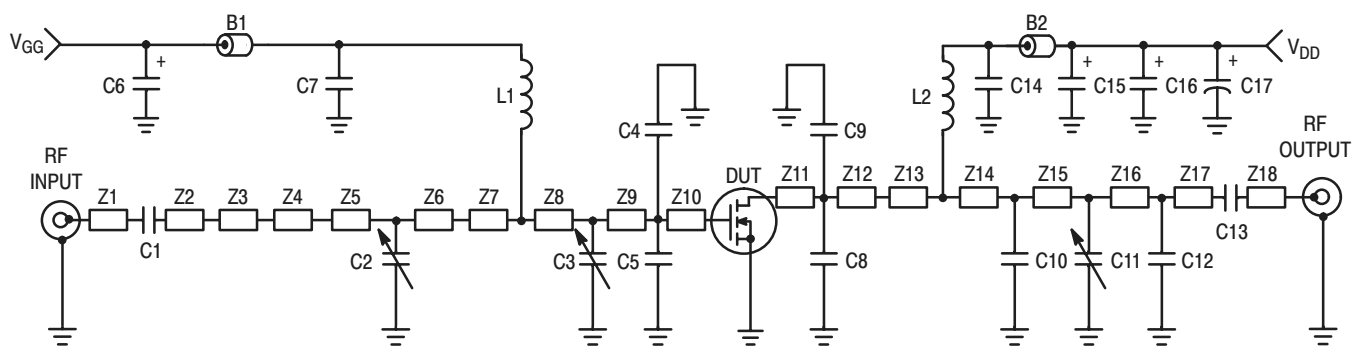
Input Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{iss}	—	101	—	pF
Output Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	53	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	2.5	—	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	G _{ps}	17	18	—	dB
Two-Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	η	37	40	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IMD	—	−31.5	−28	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 945.0 MHz, f ₂ = 945.1 MHz)	IRL	—	−14.5	−9	dB
Two-Tone Common-Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	G _{ps}	—	18	—	dB
Two-Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	η	—	40	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IMD	—	−31	—	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 450 mA, f ₁ = 930.0 MHz, f ₂ = 930.1 MHz and f ₁ = 960.0 MHz, f ₂ = 960.1 MHz)	IRL	—	−12.5	—	dB

Freescale Semiconductor, Inc.



Z1	0.240" x 0.060" Microstrip	Z10	0.060" x 0.520" Microstrip
Z2	0.240" x 0.060" Microstrip	Z11	0.360" x 0.270" Microstrip
Z3	0.500" x 0.100" Microstrip	Z12	0.060" x 0.270" Microstrip
Z4	0.100" x 0.270" x 0.080", Taper	Z13	0.130" x 0.060" Microstrip
Z5	0.330" x 0.270" Microstrip	Z14	0.300" x 0.060" Microstrip
Z6	0.120" x 0.270" Microstrip	Z15	0.210" x 0.060" Microstrip
Z7	0.270" x 0.520" x 0.140", Taper	Z16	0.600" x 0.060" Microstrip
Z8	0.240" x 0.520" Microstrip	Z17	0.290" x 0.060" Microstrip
Z9	0.340" x 0.520" Microstrip	Z18	0.340" x 0.060" Microstrip

Figure 1. 930–960 MHz Broadband Test Circuit Schematic

Table 1. 930–960 MHz Broadband Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1	Short Ferrite Bead	95F786	Newark
B2	Long Ferrite Bead	95F787	Newark
C1, C7, C13, C14	47 pF Chip Capacitors, B Case	100B470JP 500X	ATC
C2, C3, C11	0.8–8.0 Gigatrim Variable Capacitors	44F3360	Newark
C4, C5	11 pF Chip Capacitors, B Case (MRF9060MR1) 10 pF Chip Capacitors, B Case (MRF9060MBR1)	100B110JP 500X 100B100JP 500X	ATC
C6, C15, C16	10 μ F, 35 V Tantalum Chip Capacitors	93F2975	Newark
C8, C9	10 pF Chip Capacitors, B Case	100B100JP 500X	Newark
C10	3.9 pF Chip Capacitor, B Case	100B3R9CP 500X	ATC
C12	1.7 pF Chip Capacitor, B Case	100B1R7BP 500X	ATC
C17	220 μ F Electrolytic Chip Capacitor	14F185	Newark
L1, L2	12.5 nH Inductors	A04T–5	Coilcraft
N1, N2	N-Type Panel Mount, Stripline	3052–1648–10	Avnet
WB1, WB2	15 mil Brass Wear Blocks		
Board Material	30 mil Glass Teflon®, $\epsilon_r = 2.55$ Copper Clad, 2 oz Cu	RF–35–0300	Taconic
PCB	Etched Circuit Board	TO–270/TO–272 Surface/Bolt	DSelectronics

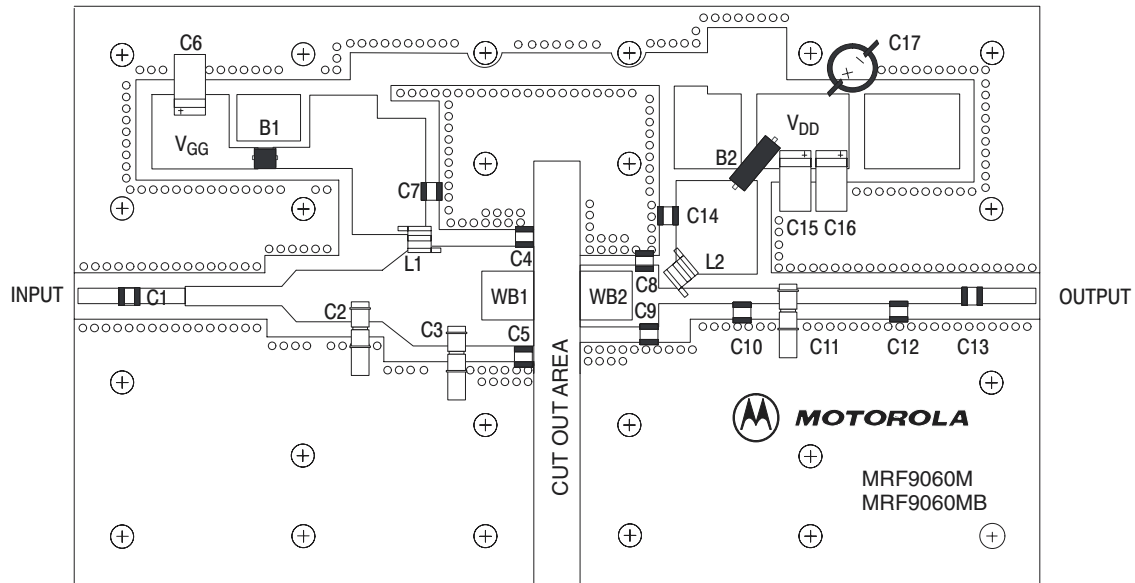


Figure 2. 930–960 MHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

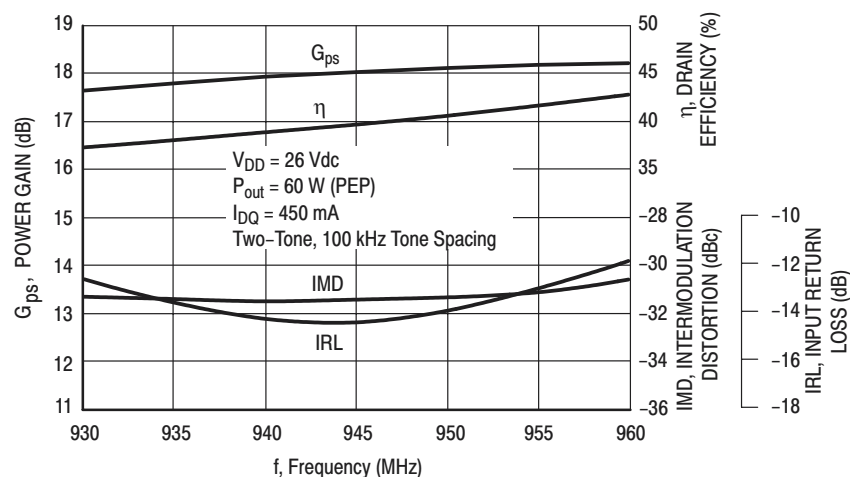


Figure 3. Class AB Broadband Circuit Performance

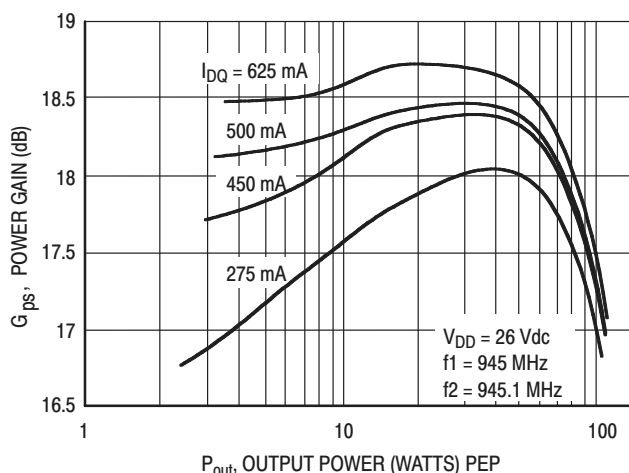


Figure 4. Power Gain versus Output Power

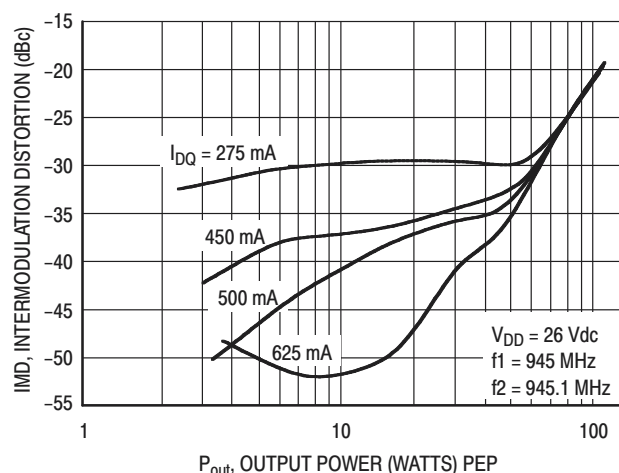


Figure 5. Intermodulation Distortion versus Output Power

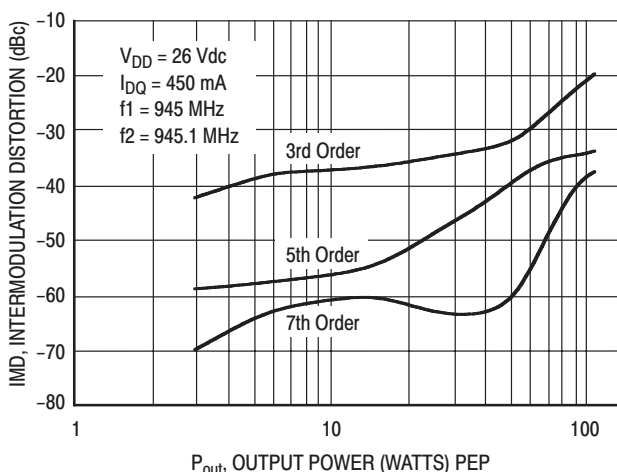


Figure 6. Intermodulation Distortion Products versus Output Power

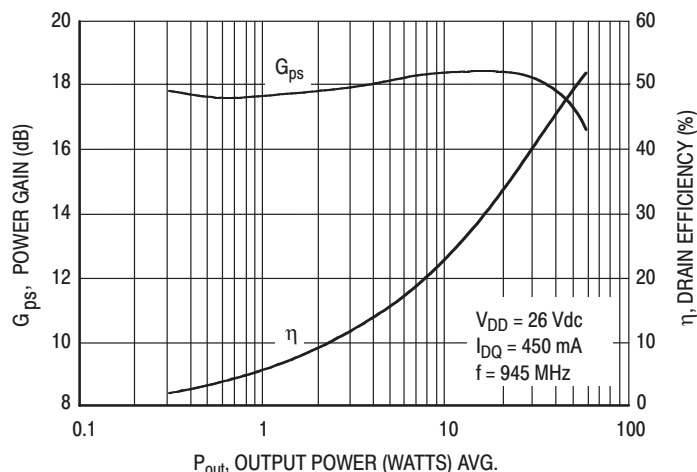


Figure 7. Power Gain and Efficiency versus Output Power

Freescalse Semiconductor, Inc.

TYPICAL CHARACTERISTICS

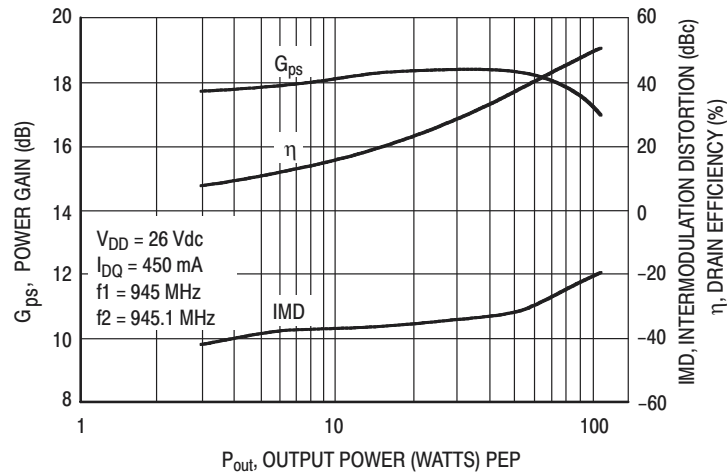
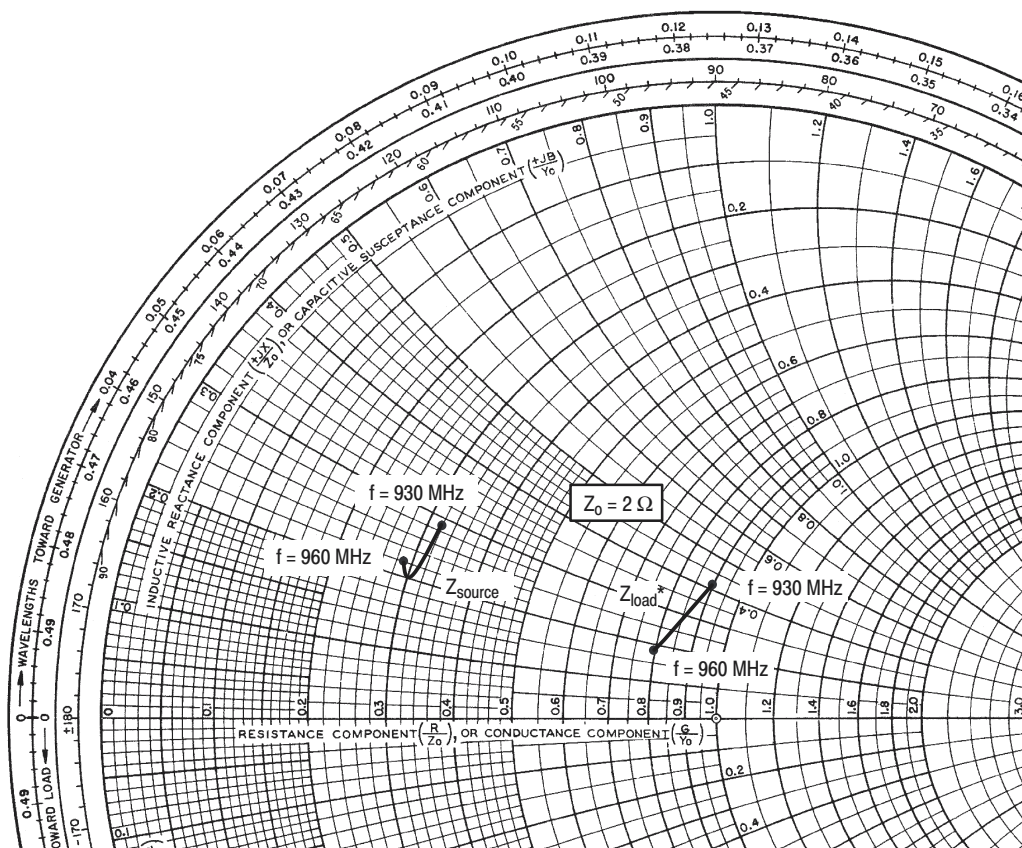


Figure 8. Power Gain, Efficiency, and IMD versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 450 \text{ mA}$, $P_{out} = 60 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
930	$0.63 + j0.57$	$1.8 + j0.84$
945	$0.60 + j0.41$	$1.7 + j0.55$
960	$0.57 + j0.45$	$1.6 + j0.36$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

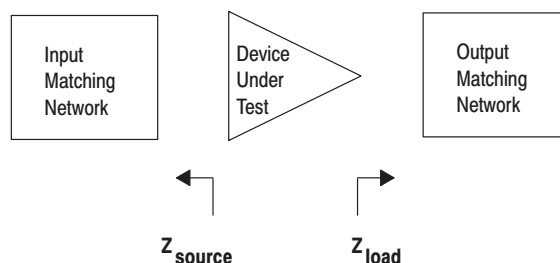


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

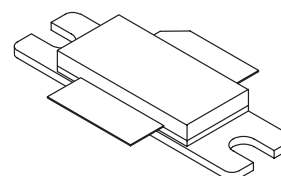
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM 900 MHz frequency band, the high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

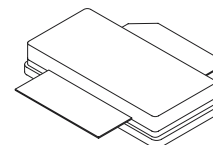
- Typical Performance for GSM Frequencies, 921 to 960 MHz, 26 Volts
Output Power @ P1db: 75 Watts
Power Gain @ P1db: 18.5 dB
Efficiency @ P1db: 55%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 921 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

MRF9080
MRF9080R3
MRF9080SR3
MRF9080LSR3

**GSM 900 MHz FREQUENCY BAND,
 75 W, 26 V
 LATERAL N-CHANNEL
 BROADBAND RF POWER MOSFETs**



CASE 465-06, STYLE 1
NI-780
MRF9080



CASE 465A-06, STYLE 1
NI-780S
MRF9080SR3, MRF9080LSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65 \text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}	—	—	10	μA_{dc}
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 26 \text{ Vds}$, $V_{GS} = 0$)	I_{DSS}	—	—	1	μA_{dc}
Gate–Source Leakage Current ($V_{GS} = 5 \text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	—	1	μA_{dc}

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = 10 \text{ Vdc}$, $I_D = 300 \mu\text{A}_{dc}$)	$V_{GS(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage ($V_{DS} = 26 \text{ Vdc}$, $I_D = 700 \text{ mA}_{dc}$)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage ($V_{GS} = 10 \text{ Vdc}$, $I_D = 2 \text{ Adc}$)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ Vdc}$, $I_D = 6 \text{ Adc}$)	g_{fs}	—	8.0	—	S

DYNAMIC CHARACTERISTICS (1)

Output Capacitance ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{oss}	—	73	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{rss}	—	2.9	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)

Power Output, 1 dB Compression Point ($V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 600 \text{ mA}$, $f = 921$ and 960 MHz)	P_{1dB}	68	75	—	W
Common–Source Amplifier Power Gain @ 70 W (Min) ($V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 600 \text{ mA}$, $f = 921$ and 960 MHz)	G_{ps}	17	18.5	20	dB
Drain Efficiency @ $P_{out} = 70 \text{ W}$ ($V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 600 \text{ mA}$, $f = 921$ and 960 MHz)	η_1	47	52	—	%
Drain Efficiency @ P_{1dB} ($V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 600 \text{ mA}$, $f = 921$ and 960 MHz)	η_2	—	55	—	%
Input Return Loss ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 70 \text{ W}$, $I_{DQ} = 600 \text{ mA}$, $f = 921$ and 960 MHz)	IRL	9.5	12.5	—	dB
Output Mismatch Stress ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 90 \text{ W CW}$, $I_{DQ} = 600 \text{ mA}$, $f = 921 \text{ MHz}$, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally input matched.

(2) To meet application requirements, Motorola test fixtures are designed to cover full GSM 900 band ensuring batch to batch consistency

Freescale Semiconductor, Inc.

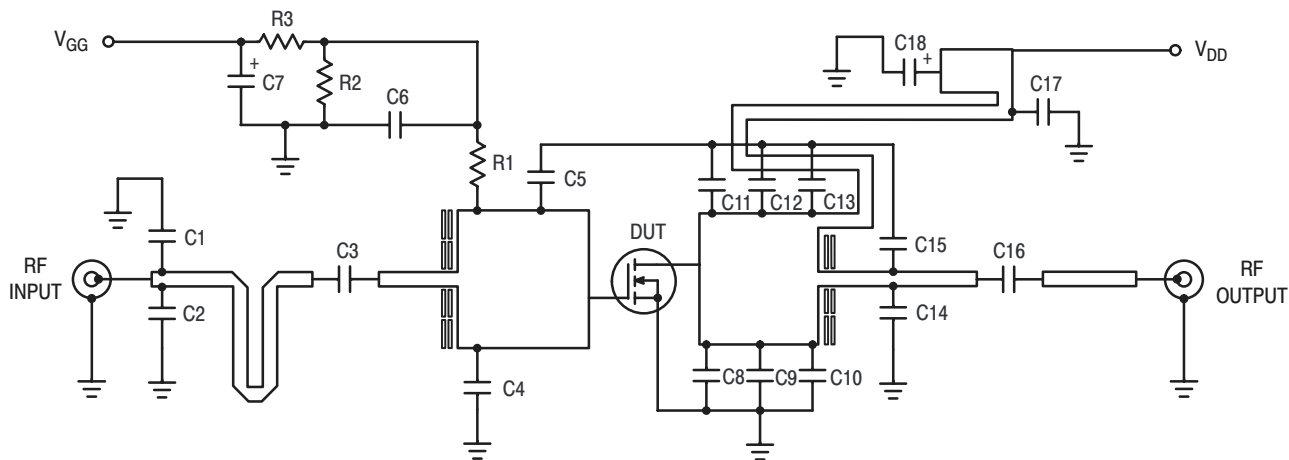


Figure 1. Broadband GSM 900 Test Circuit Schematic

Table 1. Broadband GSM 900 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1	4.7 pF Chip Capacitor, B Case	100B4R7BW	ATC
C2	2.7 pF Chip Capacitor, B Case	100B2R7BW	ATC
C3	1.5 pF Chip Capacitor, B Case	100B1R5BW	ATC
C4, C5, C9, C10, C12, C13	5.6 pF Chip Capacitors, B Case	100B5R6CW	ATC
C6, C16, C17	22 pF Chip Capacitors, B Case	100B220GW	ATC
C7, C18	10 μ F, 35 V Tantalum Chip Capacitors	293D106X9035D2T	Sprague–Vishay
C8, C11	10 pF Chip Capacitors, B Case	100B100JW	ATC
C14	0.8 pF Chip Capacitor, B Case	100B0R8BW	ATC
C15	8.2 pF Chip Capacitor, B Case	100B8R2GW	ATC
R1, R2, R3	1.0 k Ω , ??? W Chip Resistors (0805)		
WB1, WB2	Beryllium Copper Wear Blocks	0.004" x 0.210" x 0.520"	
Raw PCB Material	30 mil Glass Teflon [®] , $\epsilon_r = 2.55$	TLX8–0300	Taconic
PCB	Etched Circuit Board	C–GY–00–001–02	Cibel

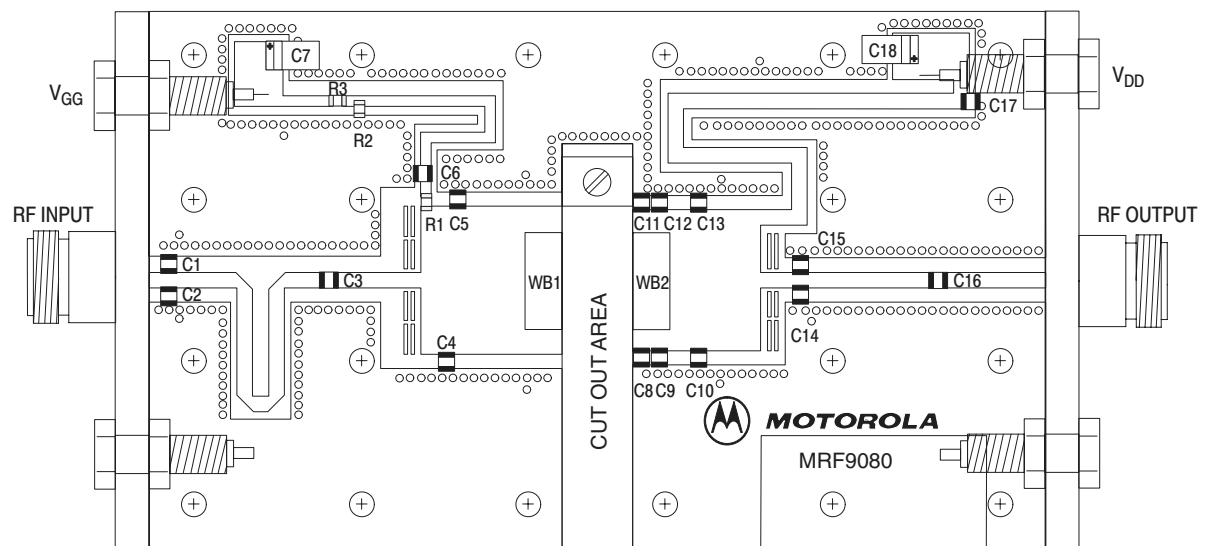


Figure 2. Broadband GSM 900 Test Circuit Component Layout

Freescale Semiconductor, Inc.

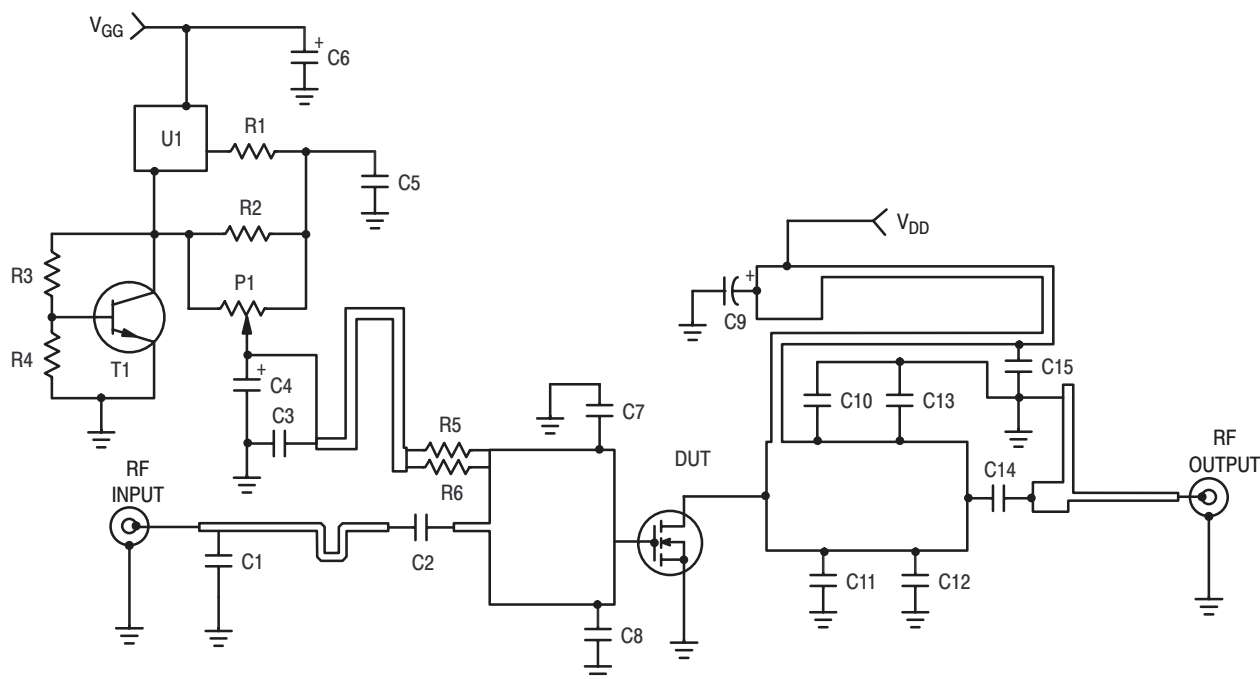


Figure 3. Broadband GSM 900 Optimized Demo Board Schematic

Table 2. Broadband GSM 900 Optimized Demo Board Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1	4.7 pF Chip Capacitor, ACCU-P (0805)	#08051J3R9CBT	AVX
C2	3.9 pF Chip Capacitor, ACCU-P (0805)	#08051J3R9CBT	AVX
C3, C15	22 pF Chip Capacitors, ACCU-P (0805)	#08051J221	AVX
C4, C6	22 μ F, 35 V Tantalum Chip Capacitors	#T491X226K035AS4394	Kemet
C5	1.0 μ F Chip Capacitor, ACCU-P (0805)	#08053G105ZATEA	AVX
C7, C8	5.6 pF Chip Capacitors, ACCU-P (0805)	#08051J5R18CBT	AVX
C9	220 μ F, 63 V Electrolytic Capacitor		
C10, C11	3.3 pF Chip Capacitors, ACCU-P (0805)	#08051J8R2CBT	AVX
C12, C13	2.2 pF Chip Capacitors, ACCU-P (0805)	#08051J2R2CBT	AVX
C14	4.7 pF Chip Capacitor	#100B	ATC
P1	5.0 k Ω Potentiometer CMS Cermet Multi-turn	#3224W	Bourns
R1	10 Ω , 1/8 W Chip Resistor (0805)		
R2	1.0 k Ω , 1/8 W Chip Resistor (0805)		
R3	1.2 k Ω , 1/8 W Chip Resistor (0805)		
R4	2.2 k Ω , 1/8 W Chip Resistor (0805)		
R5, R6	1.0 k Ω , 1/8 W Chip Resistors (0805)		
T1	Bipolar NPN Transistor, SOT-23	#BC847ALT1	ON Semiconductor
U1	Voltage Regulator, Micro-8	#LP2951ACDM-5.0R2	ON Semiconductor
	RF Connectors, Type SMA	#R125510001	Radial
	Substrate = Taconic RF35, Thickness 0.5 mm		

Freescale Semiconductor, Inc.

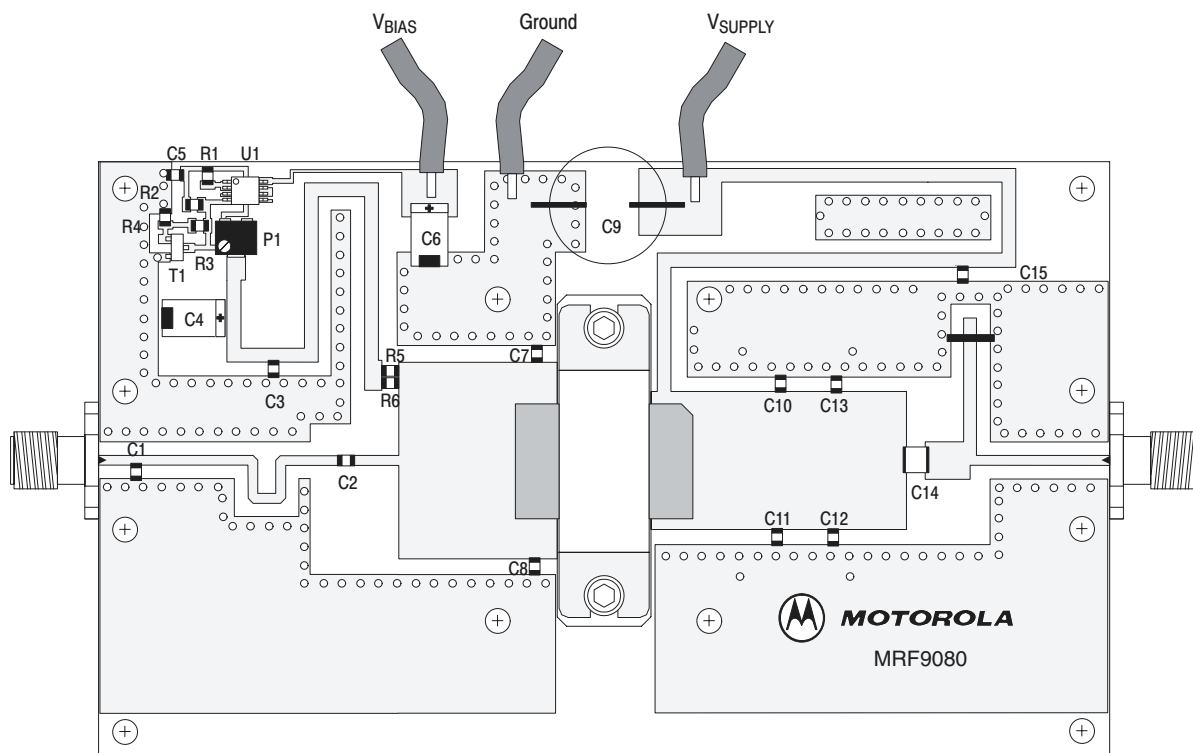


Figure 4. Broadband GSM 900 Optimized Demo Board Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS (IN MOTOROLA BROADBAND GSM 900 OPTIMIZED DEMO BOARD)

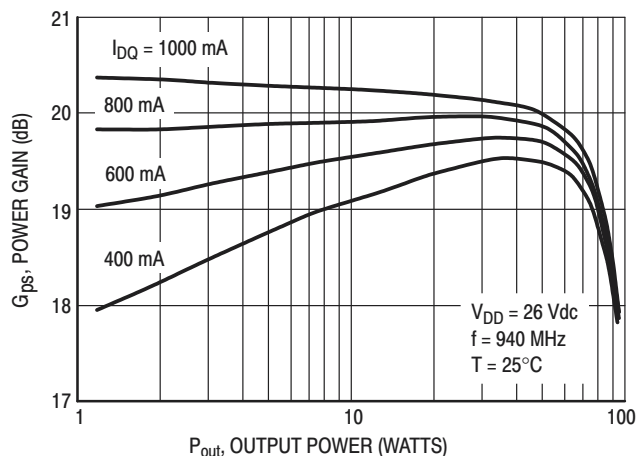


Figure 5. Power Gain versus Output Power

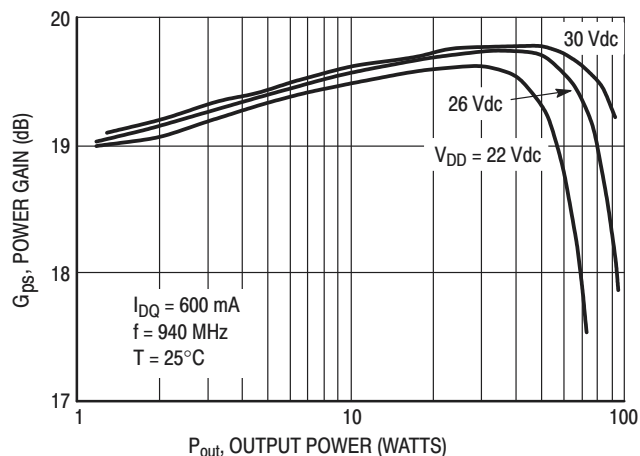


Figure 6. Power Gain versus Output Power

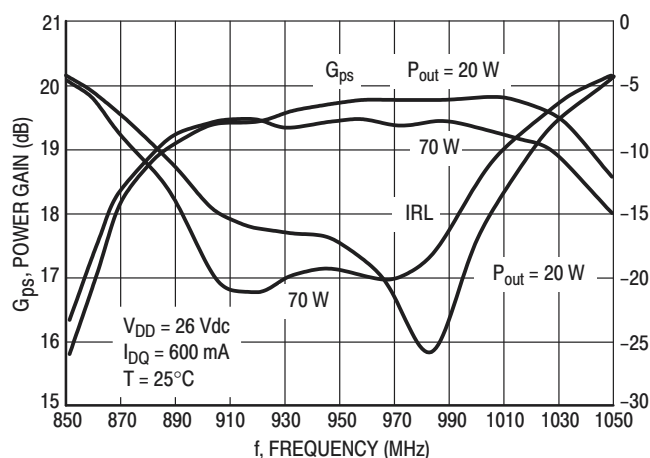


Figure 7. Power Gain and Input Return Loss versus Frequency

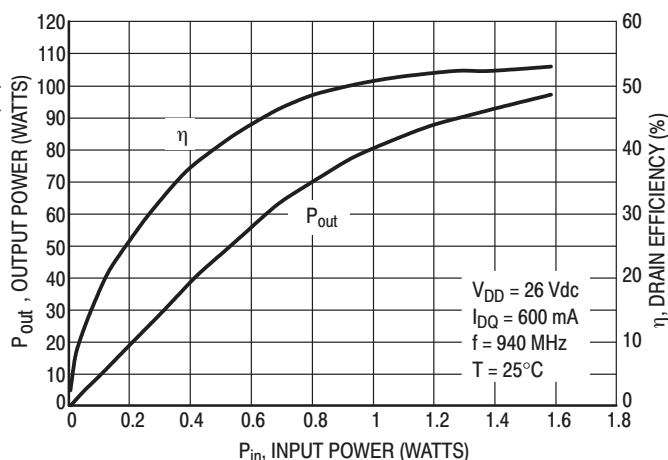


Figure 8. Output Power and Efficiency versus Input Power

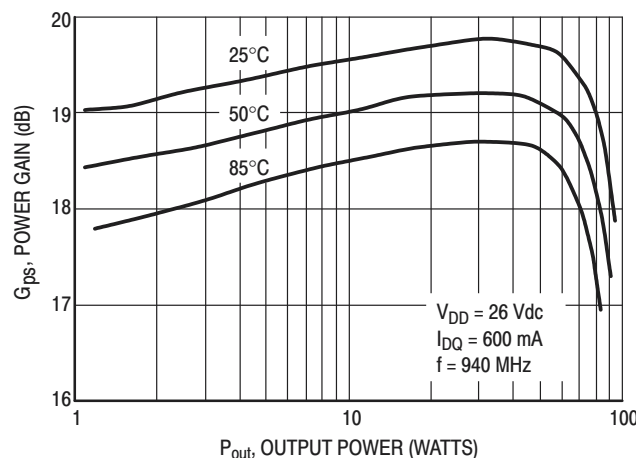


Figure 9. Power Gain versus Output Power

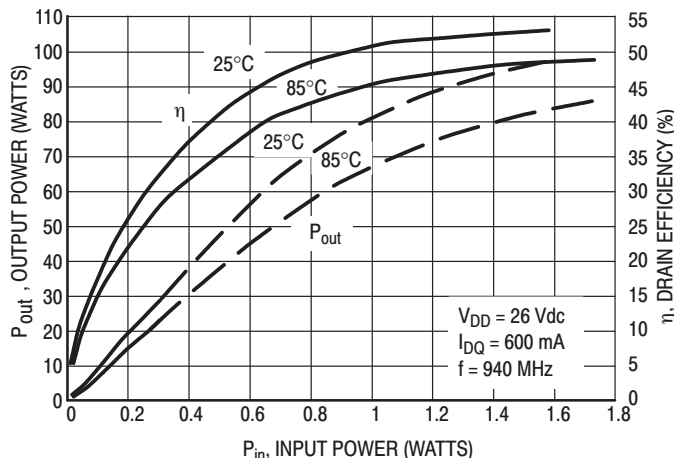
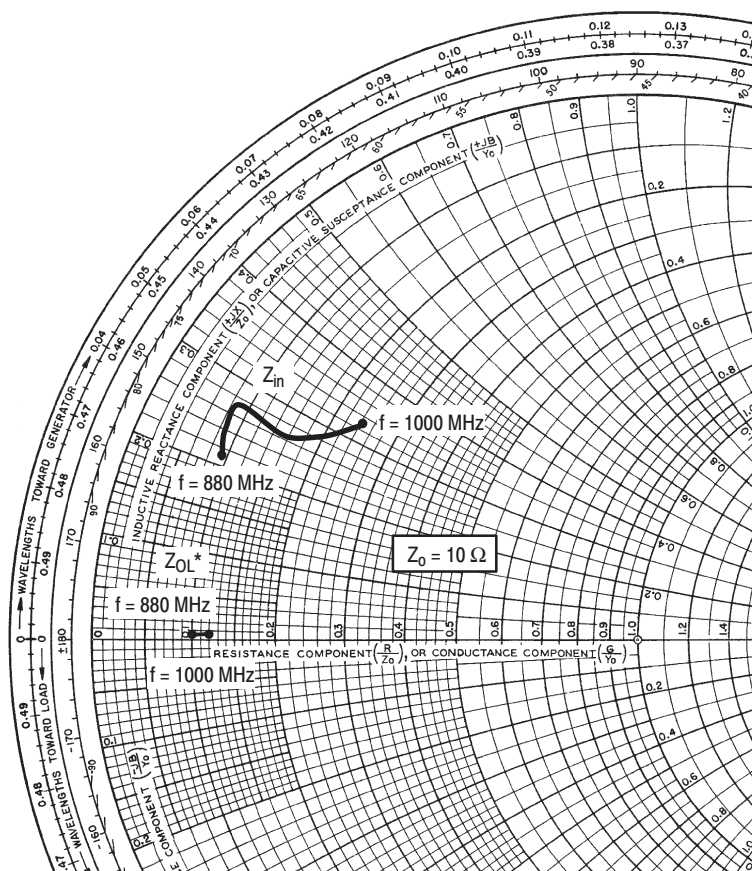


Figure 10. Output Power and Efficiency versus Input Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 600 \text{ mA}$, $P_{out} = 90 \text{ W CW}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
880	$0.91 + j2.11$	$1.22 + j0.12$
920	$0.88 + j2.65$	$1.00 + j0.16$
960	$1.6 + j2.61$	$1.22 + j0.22$
1000	$2.45 + j3.38$	$1.14 + j0.41$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power and drain efficiency.

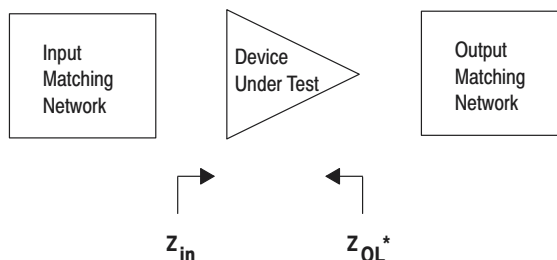


Figure 11. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

- Typical CDMA Performance @ 880 MHz, 26 Volts, $I_{DQ} = 700$ mA
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 20 Watts
Power Gain — 17.9 dB
Efficiency — 28%
Adjacent Channel Power —
750 kHz: -45.0 dBc @ 30 kHz BW
1.98 MHz: -60.0 dBc @ 30 kHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40 μ Nominal.

MRF9085
MRF9085R3
MRF9085SR3
MRF9085LSR3

880 MHz, 90 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs

CASE 465-06, STYLE 1
NI-780)
MRF9085

CASE 465A-06, STYLE 1
NI-780S
MRF9085SR3, MRF9085LSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model MRF9085 MRF9085SR3/MRF9085LSR3	M2 (Minimum) M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μA _{dc}
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μA _{dc}
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μA _{dc}
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μA _{dc})	V _{GS(th)}	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 700 mA _{dc})	V _{GS(Q)}	—	3.7	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 A _{dc})	V _{DS(on)}	—	0.19	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 6 A _{dc})	g _{fs}	—	8.0	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms) _{ac} @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	73	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms) _{ac} @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	2.9	—	pF

(1) Part is internally input matched.

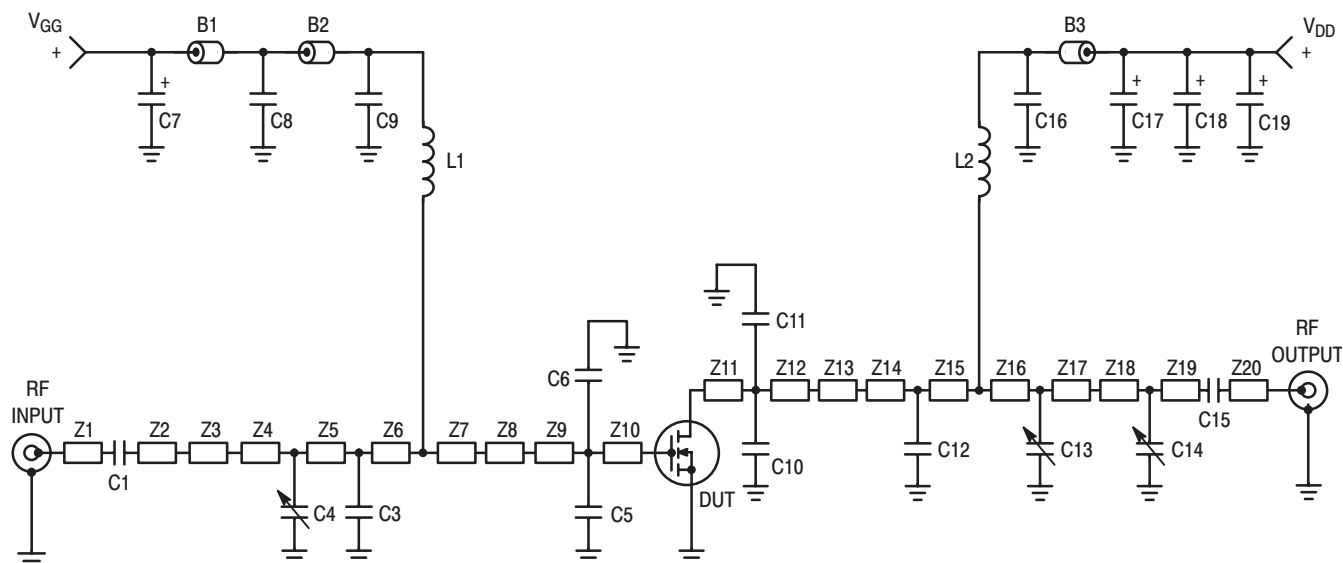
(continued)

ELECTRICAL CHARACTERISTICS – continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	G_{ps}	17	17.9	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	η	36	40	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IMD	—	-31	-28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IRL	—	-21	-9	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	G_{ps}	—	17.9	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	η	—	40.0	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	IMD	—	-31	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	IRL	—	-16	—	dB
Power Output, 1 dB Compression Point, CW ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	P_{1dB}	—	105	—	W
Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	G_{ps}	—	17.5	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	η	—	51	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 700\text{ mA}$, $f = 880.0\text{ MHz}$, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			
Power Output, 1 dB Compression Point, CW (1) ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 960\text{ MHz}$)	P_{1dB}	—	105	—	W

(1) These values are derived from a 960 MHz optimized test fixture. Values are not applicable to Figures 1 and 2.

Freescale Semiconductor, Inc.



B1, B2, B3	Short Ferrite Beads, Surface Mount	Z6	0.076" x 0.220" Microstrip
C1, C9, C15, C16	47 pF Chip Capacitors, B Case, ATC	Z7	0.261" x 0.220" Microstrip
C3	5.6 pF Chip Capacitor, B Case, ATC	Z8	0.220" x 0.630" x 0.200" Taper
C4, C13	0.8 – 8.0 Variable Capacitors, Gigatrim	Z9	0.240" x 0.630" Microstrip
C5, C6, C12	8.2 pF Chip Capacitors, B Case, ATC	Z10	0.060" x 0.630" Microstrip
C7, C17, C18, C19	10 μ F, 35 V Tantalum Surface Mount Capacitors, Kemet	Z11	0.067" x 0.630" Microstrip
C8	20 K pF Chip Capacitor, B Case, ATC	Z12	0.233" x 0.630" Microstrip
C10, C11	16 pF Chip Capacitors, B Case, ATC	Z13	0.630" x 0.220" x 0.200" Taper
C14	0.6 – 4.5 Variable Capacitor, Gigatrim	Z14	0.200" x 0.220" Microstrip
L1	7.15 nH Inductor, Coilcraft	Z15	0.055" x 0.220" Microstrip
L2	17.5 nH Inductor, Coilcraft	Z16	0.088" x 0.220" Microstrip
N1, N2	N-Type Panel Mount, Stripline, M/A-Com	Z17	0.226" x 0.220" Microstrip
WB1, WB2	5 Mil BeCu Shim (0.225 x 0.525)	Z18	0.868" x 0.080" Microstrip
Z1	0.219" x 0.080" Microstrip	Z19	0.129" x 0.080" Microstrip
Z2	0.150" x 0.080" Microstrip	Z20	0.223" x 0.080" Microstrip
Z3	0.851" x 0.080" Microstrip	PCB	Arlon GX-0300-55-22, 30 mils
Z4	0.125" x 0.220" Microstrip		$\epsilon_r = 2.55$
Z5	0.123" x 0.220" Microstrip		

Figure 1. 865–895 MHz Broadband Test Circuit Schematic

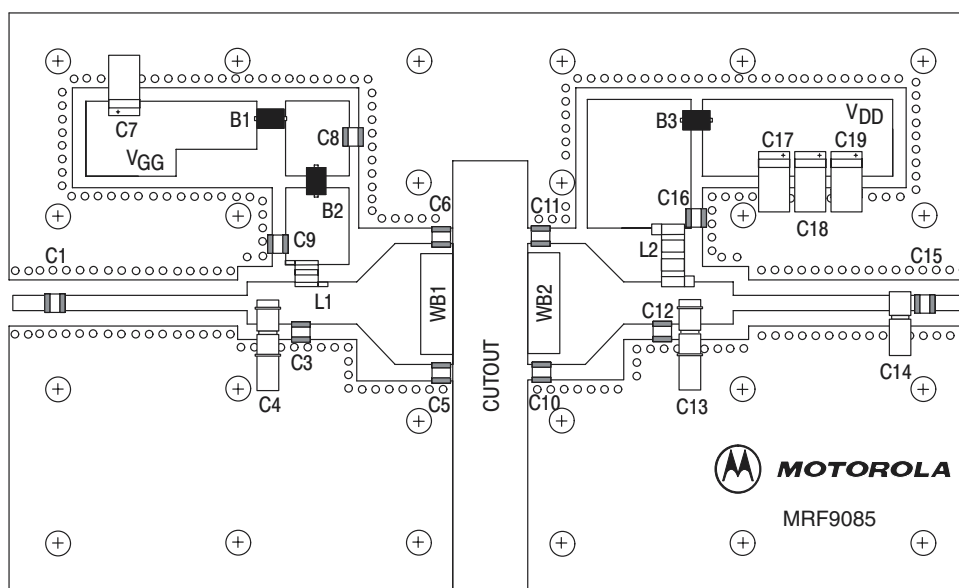


Figure 2. 865–895 MHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

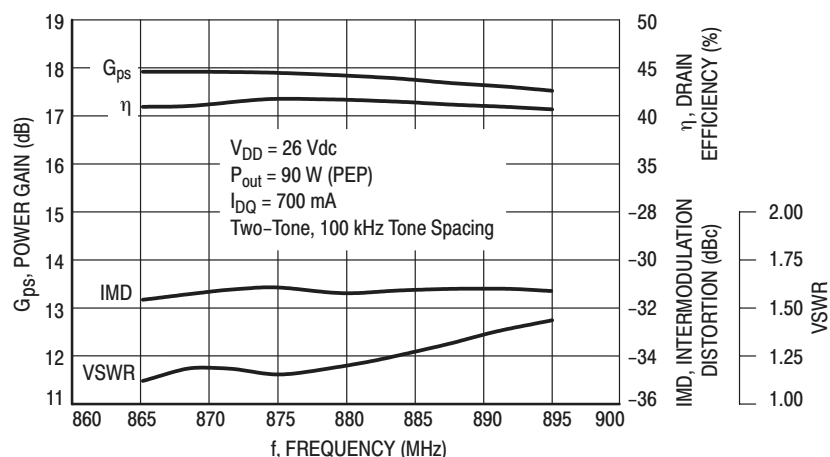


Figure 3. Class AB Broadband Circuit Performance

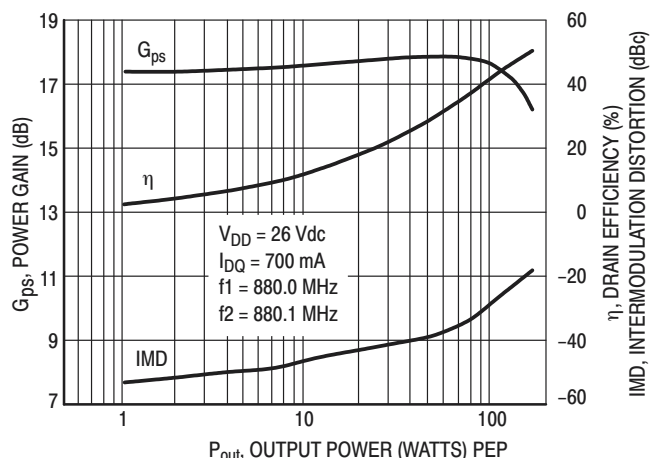


Figure 4. Power Gain, Efficiency, IMD versus Output Power

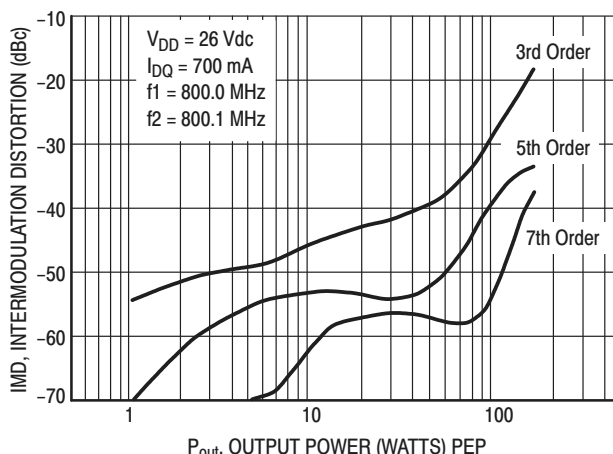


Figure 5. Intermodulation Distortion Products versus Output Power

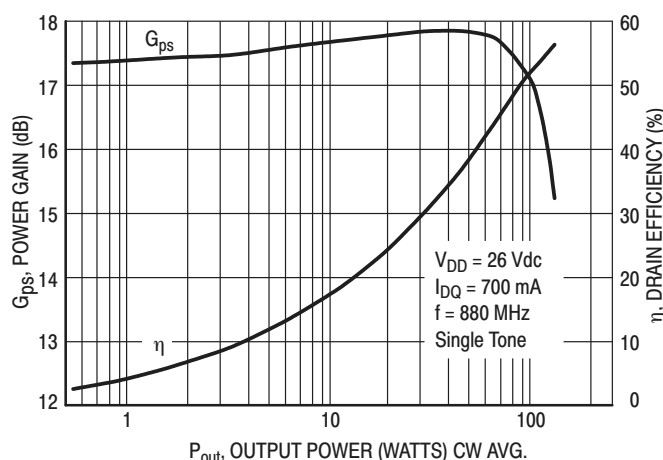


Figure 6. Power Gain, Efficiency versus Output Power

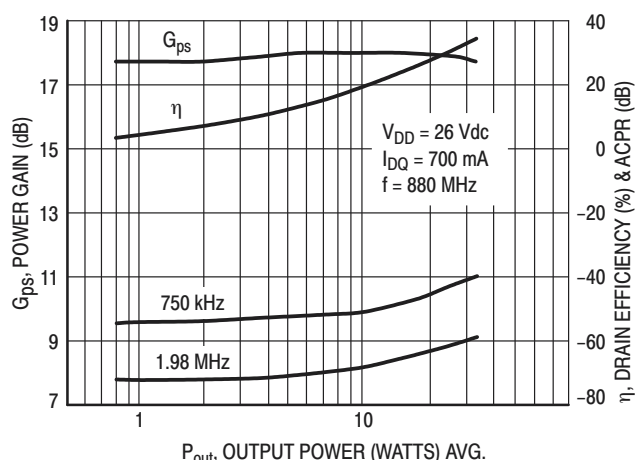
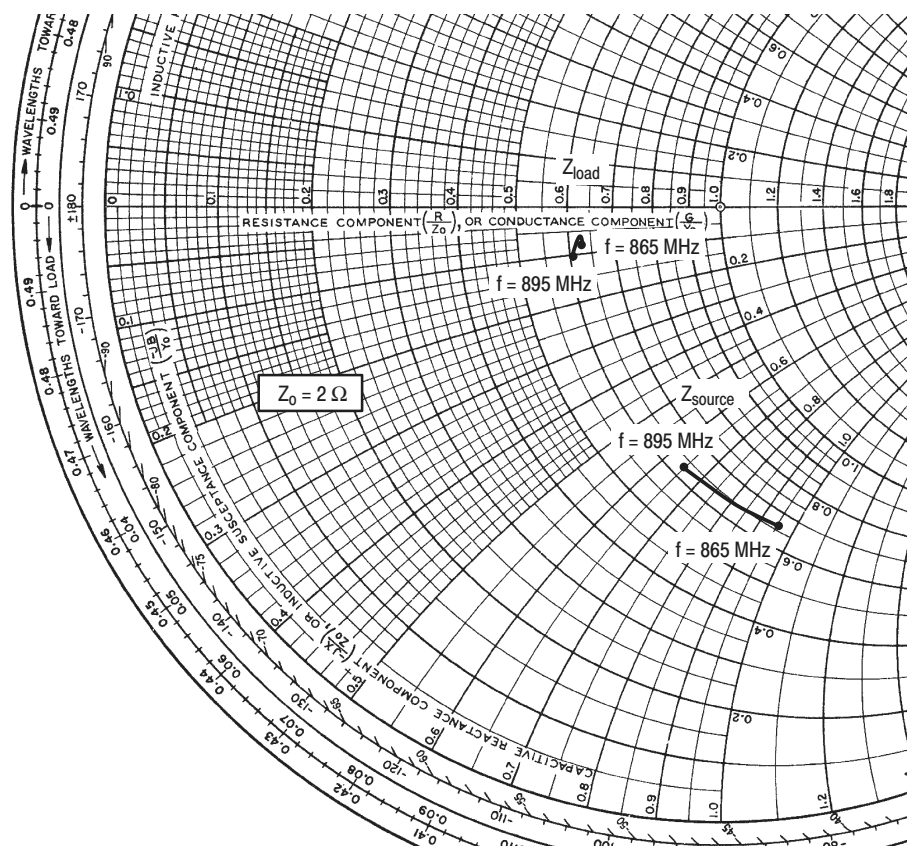


Figure 7. Power Gain, Efficiency, ACPR versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 700 \text{ mA}$, $P_{out} = 90 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
865	$1.35 - j1.92$	$1.26 - j0.15$
880	$1.33 - j1.66$	$1.26 - j0.10$
895	$1.28 - j1.30$	$1.21 - j0.20$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

Note: Z_{load} was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

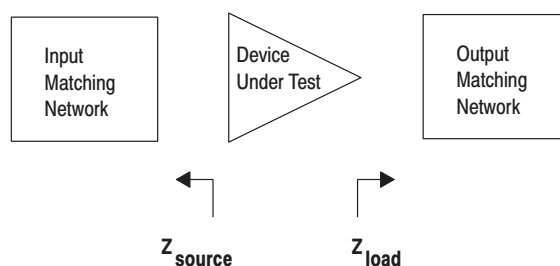


Figure 8. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

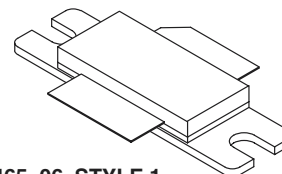
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and EDGE base station applications with frequencies from 921 to 960 MHz, the high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 26 volt base station equipment.

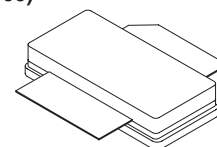
- On-Die Integrated Input Match
- Typical Performance @ Full GSM Band, 921 to 960 MHz, 26 Volts
Output Power, P1dB — 110 Watts (Typ)
Power Gain @ P1dB — 16.5 dB (Typ)
Efficiency @ P1dB — 53% (Typ)
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 921 MHz,
100 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF9100
MRF9100R3
MRF9100SR3

GSM/EDGE 900 MHz, 110 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
(NI-780)
(MRF9100)



CASE 465A-06, STYLE 1
(NI-780S)
(MRF9100SR3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	175 1.0	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C7 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, 50 ohm system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 500 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 800 mA)	V _{GS(Q)}	3	—	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.19	0.5	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	8	—	S

DYNAMIC CHARACTERISTICS (1)

Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	1.0	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture)

Output Power, 1 dB Compression Point, CW (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 960 MHz)	P _{1dB}	100	110	—	W
Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 100 W CW, I _{DQ} = 800 mA, f = 960 MHz)	G _{ps}	16	17	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 100 W CW, I _{DQ} = 800 mA, f = 960 MHz)	η	47	51	—	%
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 100 W CW, I _{DQ} = 800 mA, f ₁ = 921 MHz and 960 MHz, f ₂ = 940 MHz)	IRL	— —	— –20	–10 —	dB
Third Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 100 W PEP, I _{DQ} = 800 mA, f = Full GSM Band 921–960 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	—	dBc
Output Mismatch Stress (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, P _{out} = 100 W CW, f = 921 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.

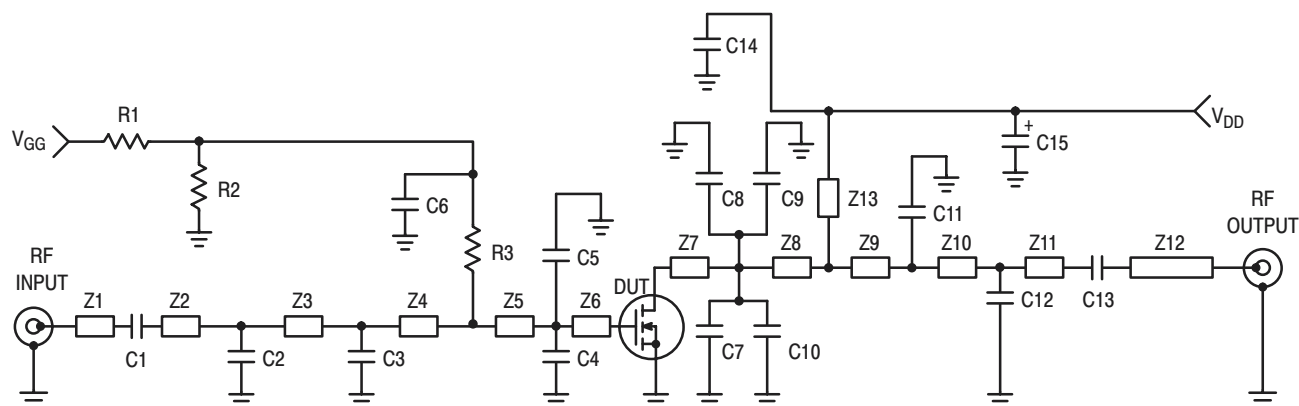


Figure 1. MRF9100 Test Circuit Schematic

Table 1. MRF9100 Test Circuit Component Designations and Values

Designators	Description
C1, C13	22 pF, 100B Chip Capacitors, ATC #100B220GW
C2, C12	2.2 pF, 100B Chip Capacitors, ATC #100B2R2BW
C3	6.8 pF, 100B Chip Capacitor, ATC #100B6R8CW
C4, C5	10 pF, 100B Chip Capacitors, ATC #100B100GW
C6, C14	33 pF, 100B Chip Capacitors, ATC #100B330JW
C7, C8, C9, C10	4.7 pF, 100B Chip Capacitors, ATC #100B4R7BW
C11	2.7 pF, 100B Chip Capacitor, ATC #100B2R7BW
C15	10 μ F, 35 V Tantalum Chip Capacitor, Vishay–Sprague #293D106X9035D
R1, R2	10 k Ω , 1/8 W Chip Resistors (0805)
R3	1 k Ω , 1/8 W Chip Resistor (0805)
Z1	0.495" x 0.087" Microstrip
Z2	0.657" x 0.087" Microstrip
Z3	0.324" x 0.087" Microstrip
Z4	0.429" x 0.087" Microstrip
Z5	0.250" x 0.790" Microstrip
Z6	0.535" x 0.790" Microstrip
Z7	0.312" x 0.790" Microstrip
Z8	0.409" x 0.790" Microstrip
Z9	0.432" x 0.087" Microstrip
Z10	0.220" x 0.087" Microstrip
Z11	0.828" x 0.087" Microstrip
Z12	0.485" x 0.087" Microstrip
Z13	1.602" x 0.087" Microstrip
Substrate	Taconic TLX8, Thickness 0.8 mm

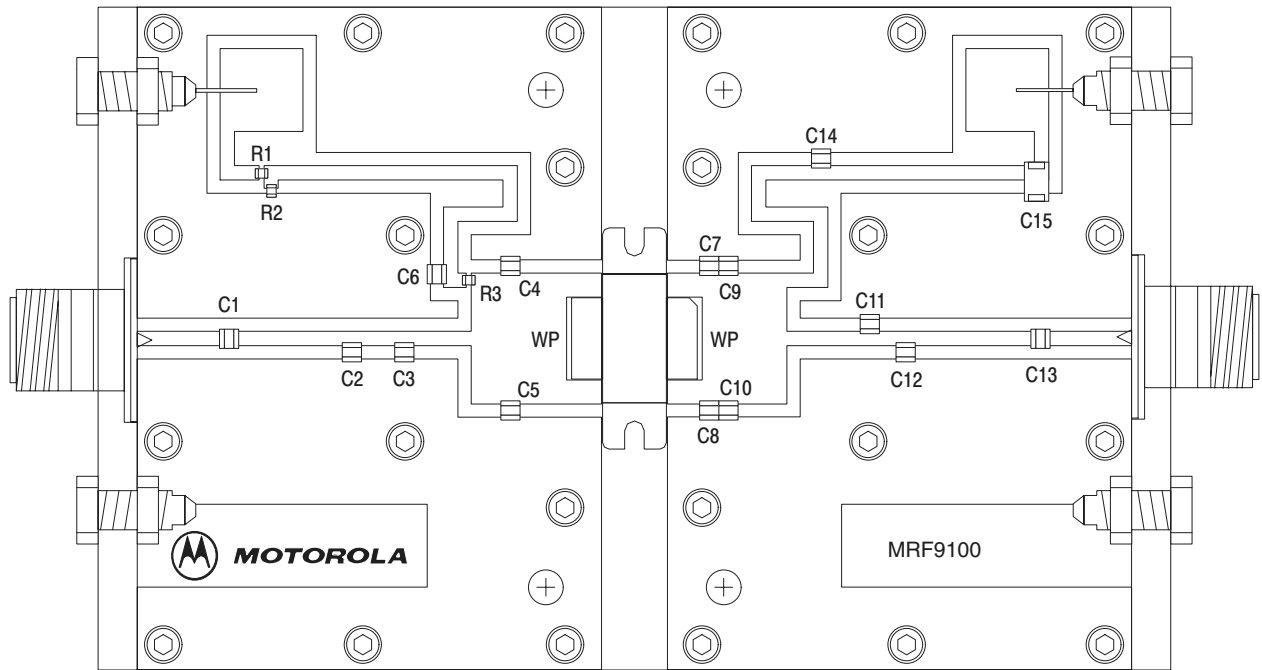


Figure 2. MRF9100 Test Circuit Component Layout

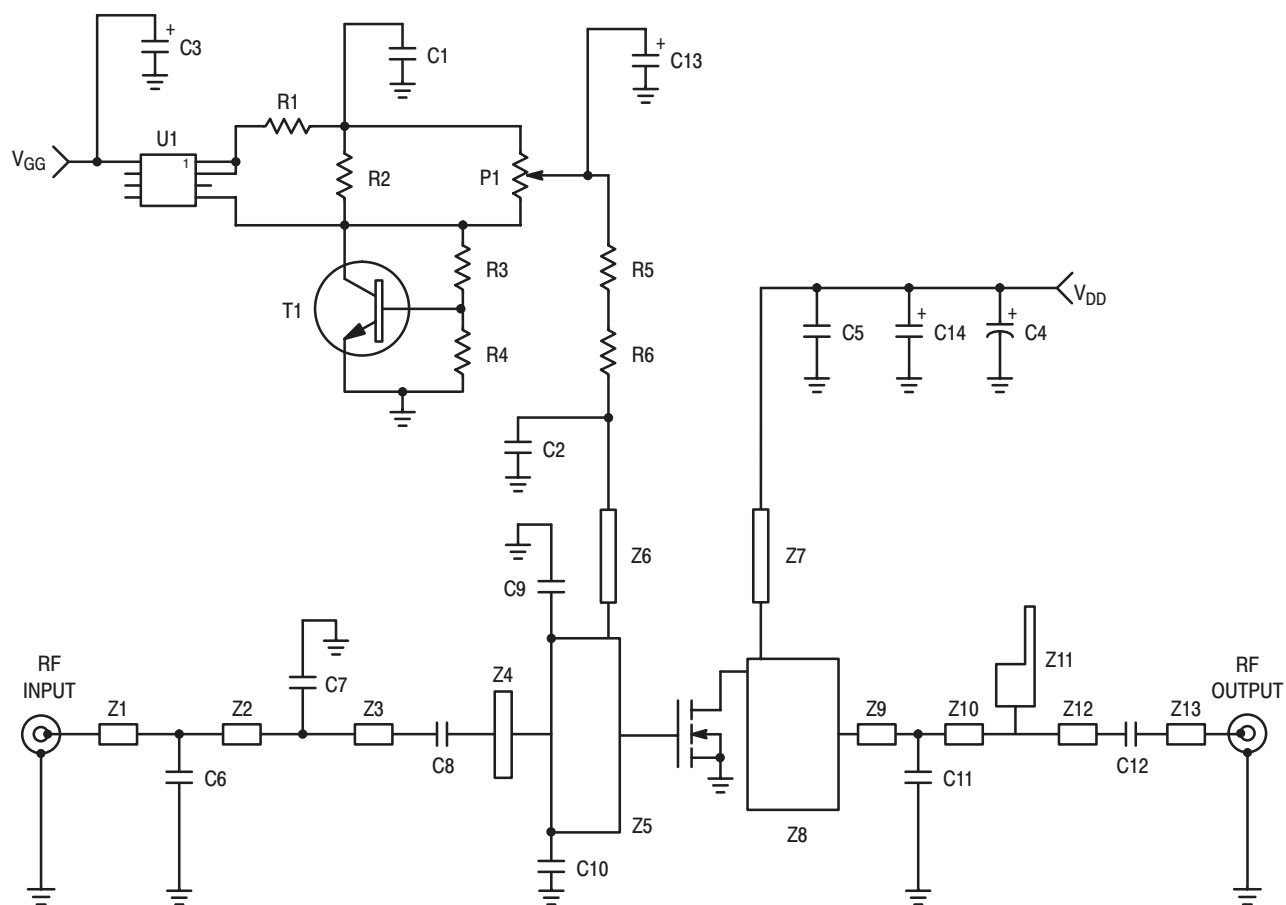


Figure 3. MRF9100 Demo Board Schematic

Freescale Semiconductor, Inc.

Table 2. GSM 900 Optimized Demo Board Component Designations and Values

Designators	Description
C1	1.0 μ F Chip Capacitor, AVX #08053G105ZATEA (0805)
C2, C5	33 pF Chip Capacitors, AVX #08051J330GBT, ACCU-P (0805)
C3, C13, C14	22 μ F, 35 V Tantalum Chip Capacitors, Kemet #T491x226K035AS4394
C4	220 μ F, 63 V Electrolytic Capacitor Radial, Philips #13668221
C6	5.6 pF Chip Capacitor, AVX #08051J5R6CBT, ACCU-P (0805)
C7	4.7 pF Chip Capacitor, AVX #08051J4R7CBT, ACCU-P (0805)
C8	22 pF Chip Capacitor, AVX #08051J220GBT, ACCU-P (0805)
C9, C10	3.9 pF Chip Capacitors, AVX #08051J3R9BBT, ACCU-P (0805)
C11	2.2 pF Chip Capacitor, AVX #08051J2R2BBT, ACCU-P (0805)
C12	33 pF, 100B Chip Capacitor, ATC #100B330JW
P1	5.0 k Ω Potentiometer CMS Cermet multi-turn, Bourns #3224W
R1	10 Ω , 1/8 W Chip Resistor (0805)
R2	1.0 k Ω , 1/8 W Chip Resistor (0805)
R3	1.2 k Ω , 1/8 W Chip Resistor (0805)
R4	2.2 k Ω , 1/8 W Chip Resistor (0805)
R5	100 Ω , 1/8 W Chip Resistor (0805)
R6	1.0 Ω , 1/8 W Chip Resistor (0805)
T1	NPN Bipolar Transistor, SOT-23, Motorola #BC847
U1	Voltage Regulator, Micro-8, Motorola #LP2951
Z1	0.916" x 0.042" Microstrip
Z2	0.169" x 0.042" Microstrip
Z3	0.212" x 0.042" Microstrip
Z4	0.090" x 0.465" Microstrip
Z5	0.465" x 0.842" Microstrip
Z6	1.776" x 0.059" Microstrip
Z7	1.802" x 0.059" Microstrip
Z8	1.094" x 0.592" Microstrip
Z9	0.085" x 0.042" Microstrip
Z10	0.198" x 0.042" Microstrip
Z11	0.253" x 0.191" + 0.292" x 0.061" Microstrip
Z12	0.181" x 0.042" Microstrip
Z13	0.282" x 0.042" Microstrip
Substrate	Taconic RF35, Thickness 0.5 mm, $\epsilon_r = 3.5$

Freescale Semiconductor, Inc.

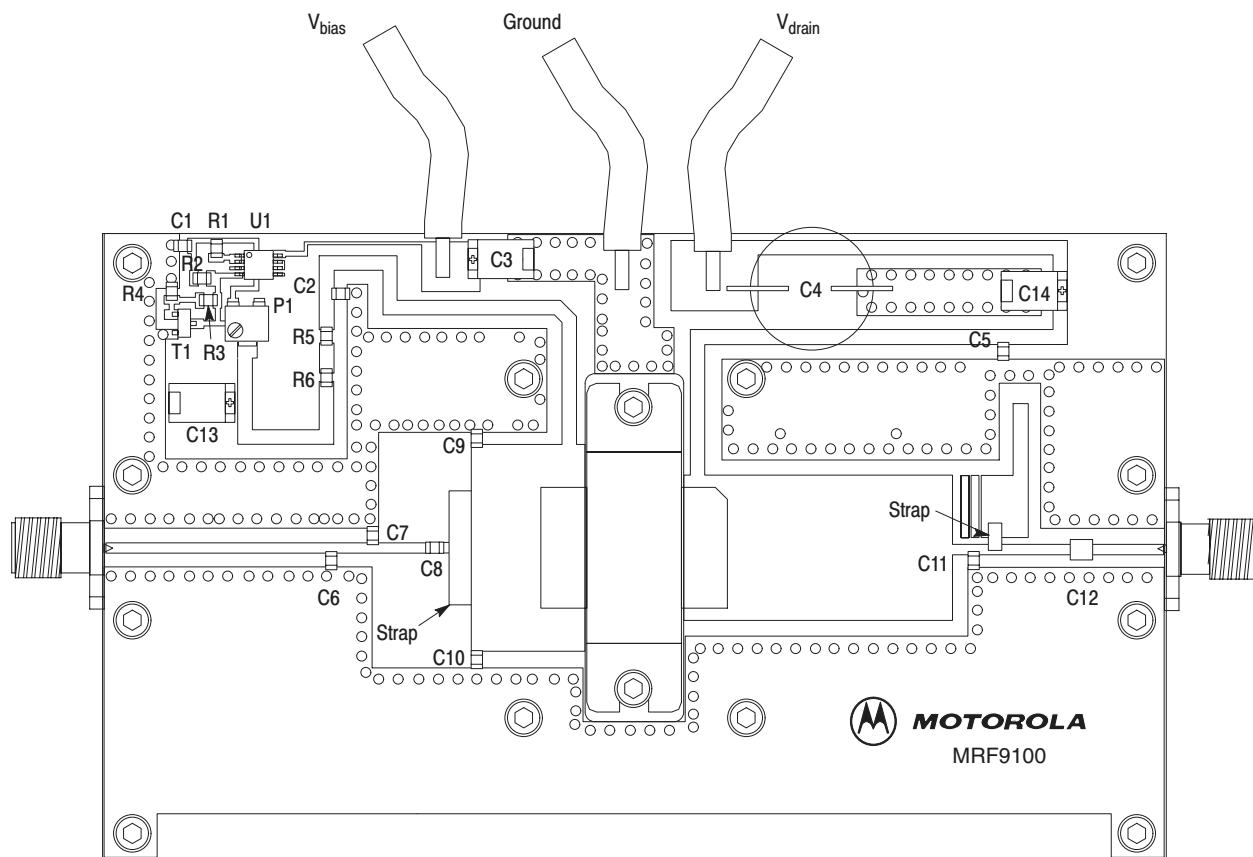


Figure 4. MRF9100 Demo Board Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

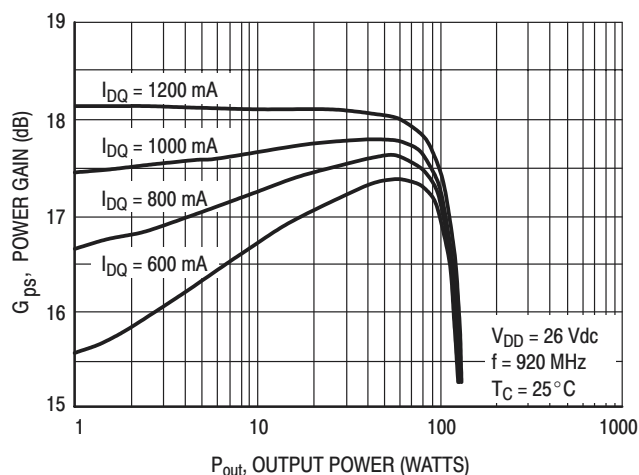


Figure 5. Power Gain versus Output Power

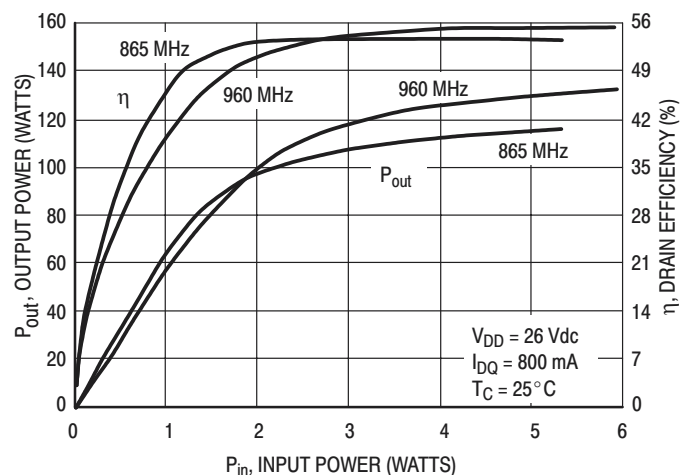


Figure 6. Output Power and Efficiency versus Input Power

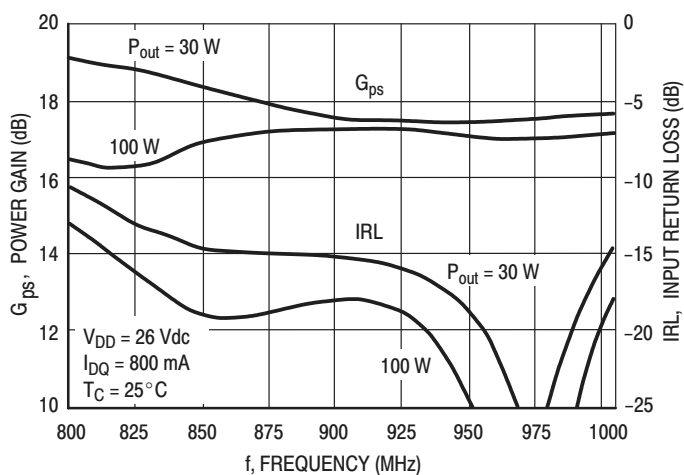


Figure 7. Power Gain and Input Return Loss versus Frequency

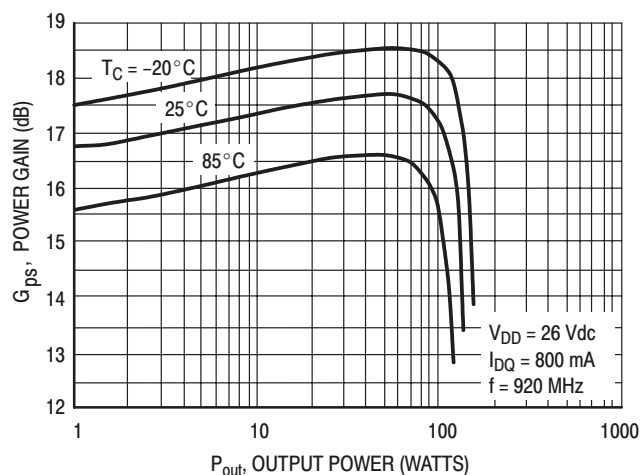


Figure 8. Power Gain versus Output Power

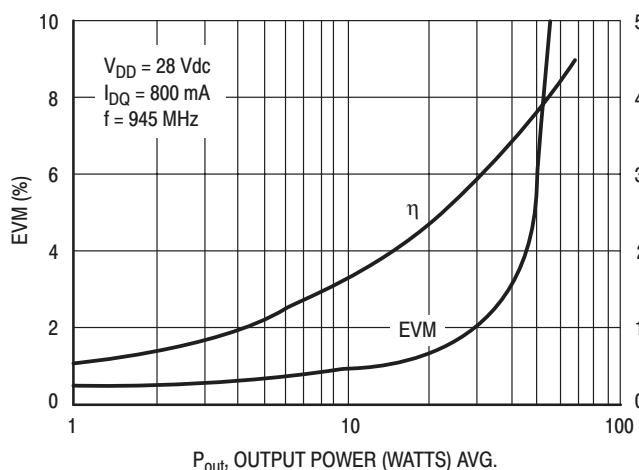


Figure 9. EVM and Efficiency versus Output Power

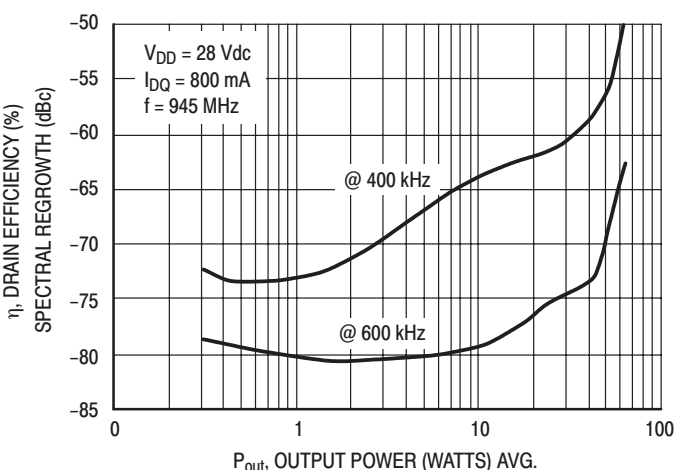
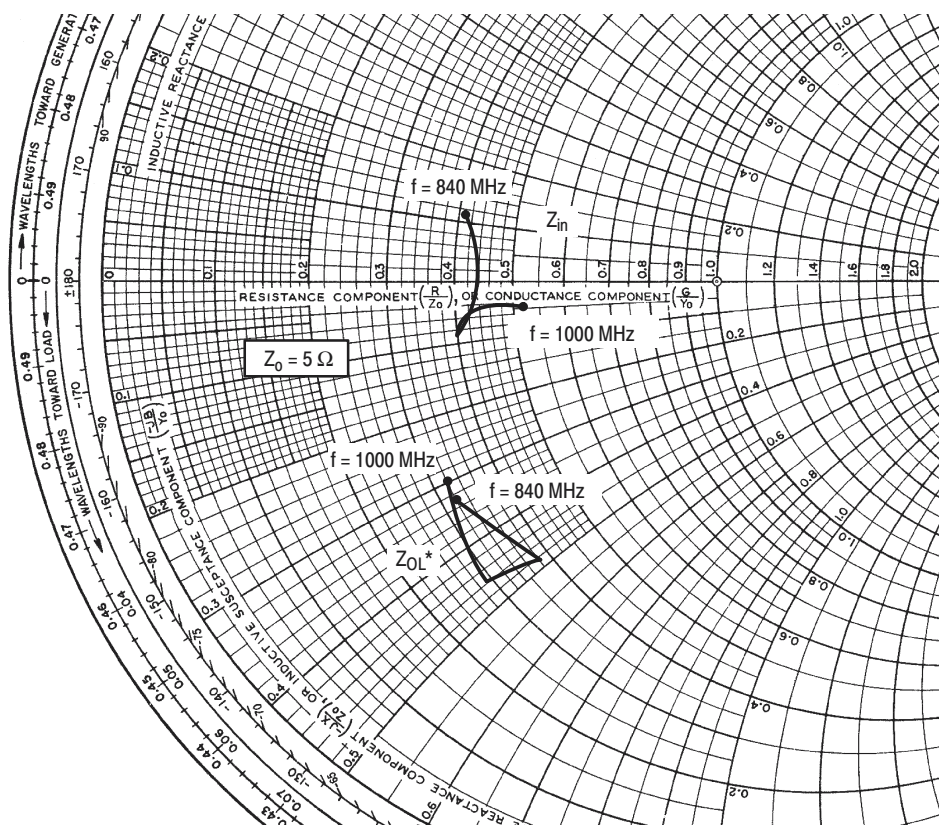


Figure 10. Spectral Regrowth versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 800 \text{ mA}$, $P_{out} = 110 \text{ W (CW)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
840	$2.04 + j0.57$	$1.62 - j1.65$
880	$2.20 + j0.16$	$1.88 - j2.45$
920	$2.00 - j0.44$	$1.79 - j2.40$
960	$2.16 - j0.25$	$1.47 - j1.82$
1000	$2.62 - j0.25$	$1.58 - j1.52$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

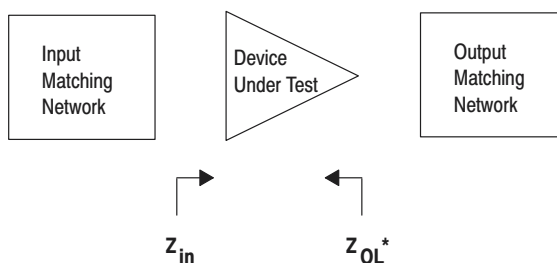


Figure 11. Series Equivalent Input and Output Impedance

The RF MOSFET Line

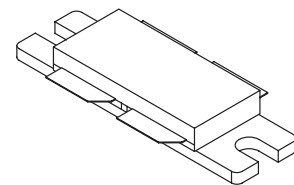
RF Power Field Effect Transistors N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 26 volt base station equipment.

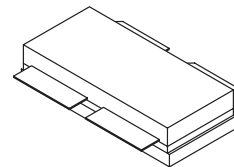
- Typical CDMA Performance @ 880 MHz, 26 Volts, $I_{DQ} = 2 \times 500 \text{ mA}$
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 26 Watts
Power Gain — 16 dB
Efficiency — 26%
Adjacent Channel Power —
750 kHz: -45 dBc @ 30 kHz BW
1.98 MHz: -60 dBc @ 30 kHz BW
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 120 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

**MRF9120
MRF9120S**

**880 MHz, 120 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs**



**CASE 375B-04, STYLE 1
NI-860
MRF9120**



**CASE 375H-03, STYLE 1
NI-860S
MRF9120S**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS ⁽¹⁾					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS ⁽¹⁾					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 μAdc)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 450 mAdc)	V _{GS(Q)}	—	3.8	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1.3 Adc)	V _{DS(on)}	—	0.17	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 4 Adc)	g _{fs}	—	5.3	—	S
DYNAMIC CHARACTERISTICS ⁽¹⁾					
Output Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	50	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	2	—	pF

(1) Each side of device measured separately.

(continued)

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W PEP}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	G_{ps}	15	16.5	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W PEP}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	η	36	39	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W PEP}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IMD	—	−31	−28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W PEP}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IRL	—	−16	−9	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W PEP}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 895.0\text{ MHz}$, $f_2 = 895.1\text{ MHz}$)	G_{ps}	—	16.5	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W PEP}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 895.0\text{ MHz}$, $f_2 = 895.1\text{ MHz}$)	η	—	40.5	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W PEP}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 895.0\text{ MHz}$, $f_2 = 895.1\text{ MHz}$)	IMD	—	−30	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W PEP}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 895.0\text{ MHz}$, $f_2 = 895.1\text{ MHz}$)	IRL	—	−13	—	dB
Power Output, 1 dB Compression Point ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W CW}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	P_{1dB}	—	120	—	W
Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W CW}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	G_{ps}	—	16	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W CW}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	η	—	51	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W CW}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f = 880.0\text{ MHz}$, $VSWR = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			

(2) Device measured in push-pull configuration.

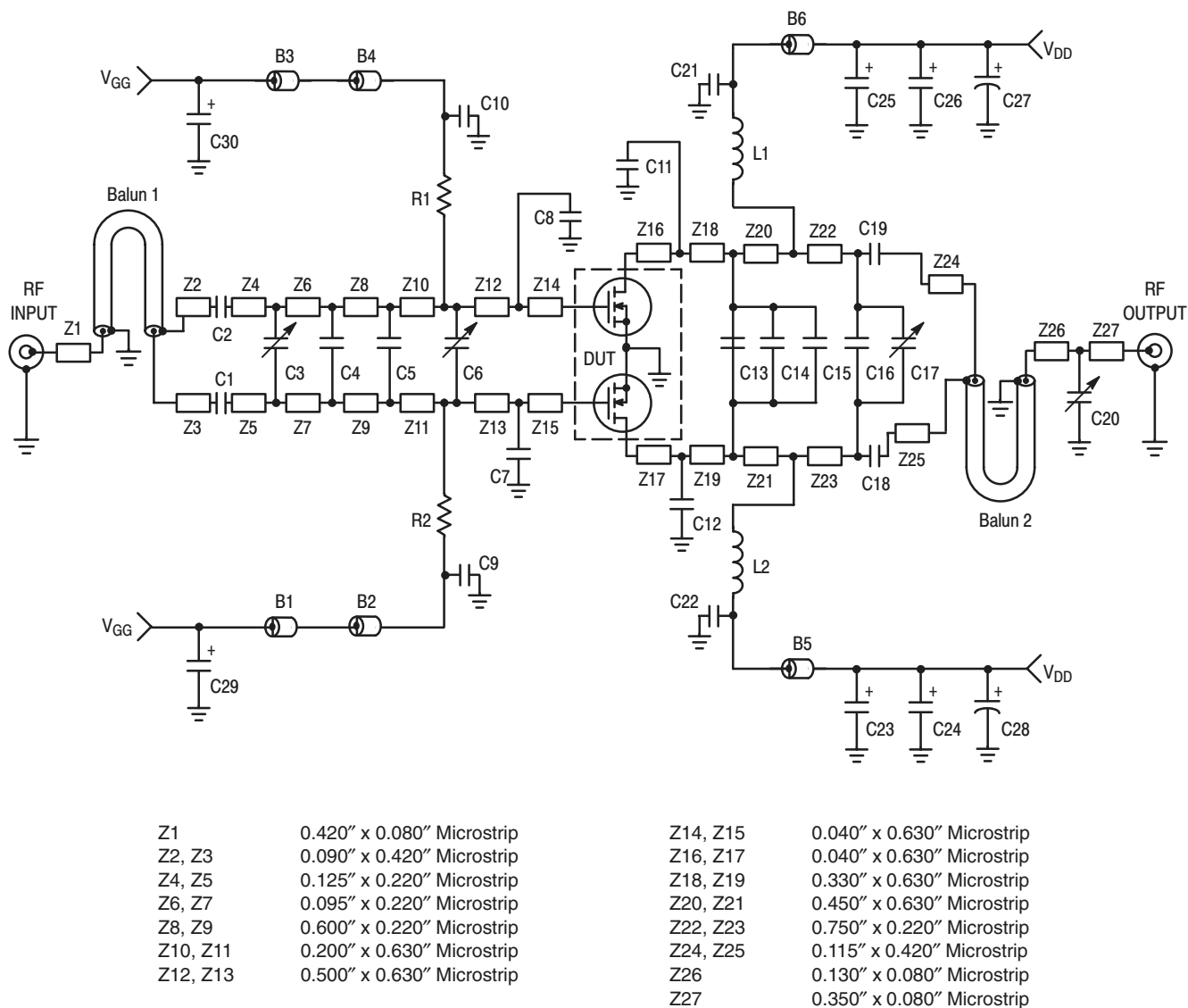


Figure 1. 880 MHz Broadband Test Circuit Schematic

Freescale Semiconductor, Inc.

Table 1. 880 MHz Broadband Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1, B3, B5, B6	Long Ferrite Beads, Surface Mount	95F787	Newark
B2, B4	Short Ferrite Beads, Surface Mount	95F786	Newark
C1, C2	68 pF Chip Capacitors, B Case	100B680JP500X	ATC
C3, C6	0.8 – 8.0 pF Variable Capacitors	44F3360	Newark
C4	7.5 pF Chip Capacitor, B Case	100B7R5JP150X	ATC
C5	3.3 pF Chip Capacitor, B Case	100B3R3CP150X	ATC
C7, C8	11 pF Chip Capacitors, B Case	100B110BCA500X	ATC
C9, C10, C21, C22	51 pF Chip Capacitors, B Case	100B510JP500X	ATC
C11, C12	6.2 pF Chip Capacitors, B Case	100B6R2BCA150X	ATC
C13	4.7 pF Chip Capacitor, B Case	100B4R7BCA150X	ATC
C14	5.1 pF Chip Capacitor, B Case	100B5R1BCA150X	ATC
C15	3.0 pF Chip Capacitor, B Case	100B2R7BCA150X	ATC
C16	2.7 pF Chip Capacitor, B Case	100B3R0BCA150X	ATC
C17	0.6 – 4.5 pF Variable Capacitor	44F3358	Newark
C18, C19	47 pF Chip Capacitors, B Case	100B470JP500X	ATC
C20	0.4 – 2.5 pF Variable Capacitor	44F3367	Newark
C29, C30	10 μ F, 35 V Tantalum Chip Capacitors	93F2975	Newark
C23, C24, C25, C26	22 μ F, 35 V Tantalum Chip Capacitors	92F1853	Newark
C27, C28	220 μ F, 50 V Electrolytic Capacitors	14F185	Newark
Balun 1, Balun 2	Xinger Surface Mount Balun Transformers	3A412	Anaren
L1, L2	12.5 nH Mini Spring Inductors	A04T–5	Coilcraft
R1, R2	510 Ω , 1/4 W Chip Resistors		Garret
WB1, WB2, WB3, WB4	10 mil Brass Wear Blocks		
Board Material	30 mil Glass Teflon [®] , $\epsilon_r = 2.55$ Copper Clad, 2 oz Cu	900 MHz Push–Pull Rev 01B	CMR
PCB	Etched Circuit Board	900 MHz Push–Pull Rev 01B	CMR

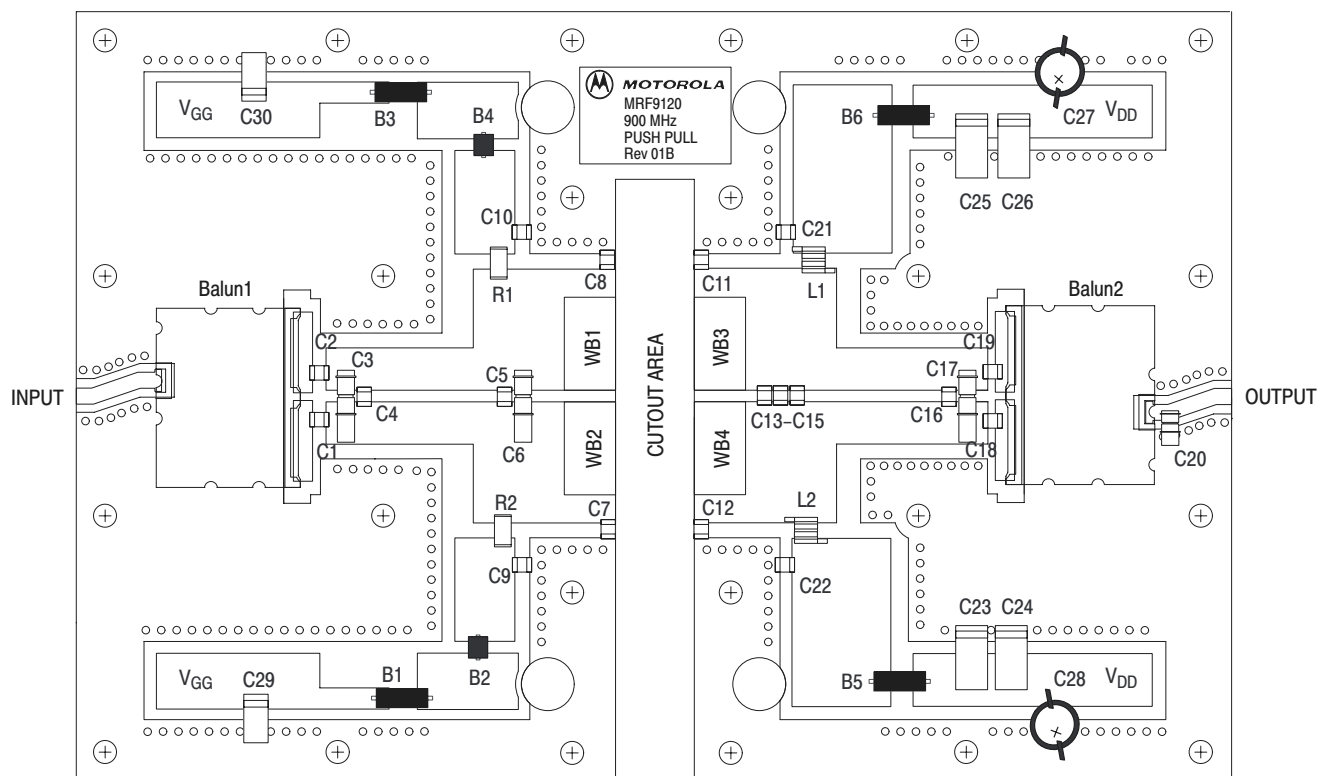


Figure 2. 865–895 MHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

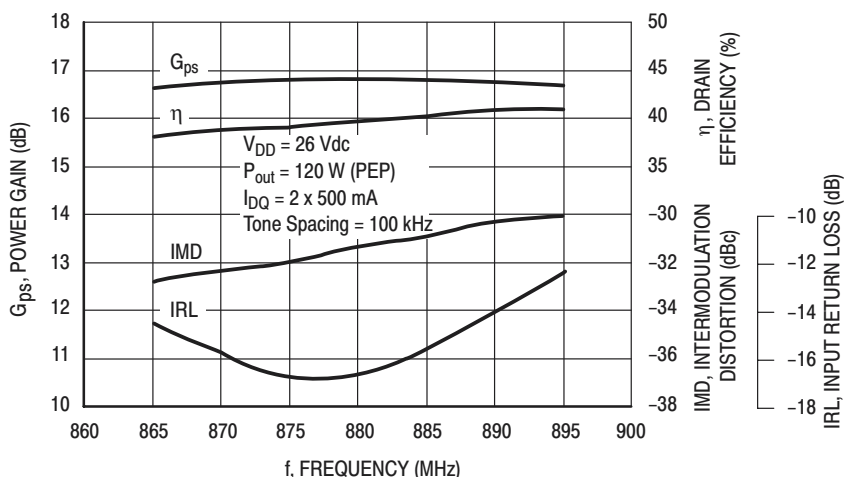


Figure 3. Class AB Broadband Circuit Performance

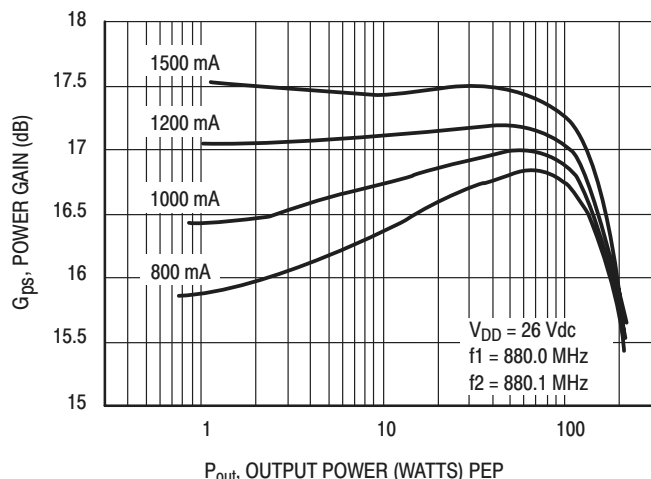


Figure 4. Power Gain versus Output Power

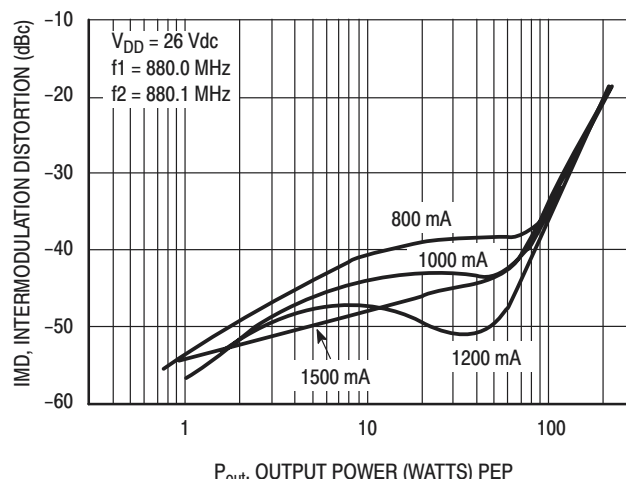


Figure 5. Intermodulation Distortion versus Output Power

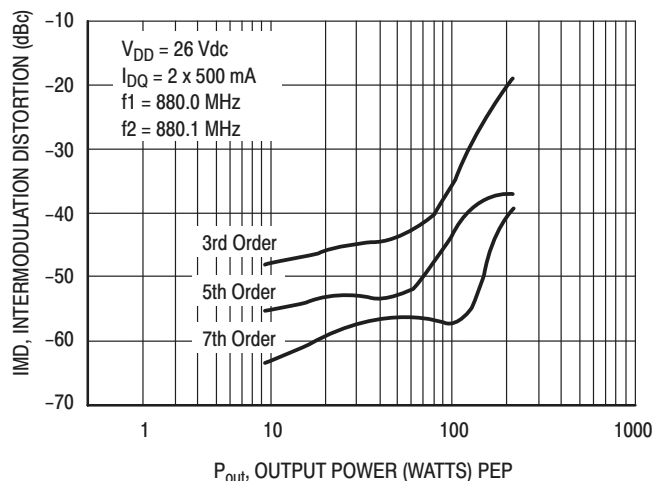


Figure 6. Intermodulation Distortion Products versus Output Power

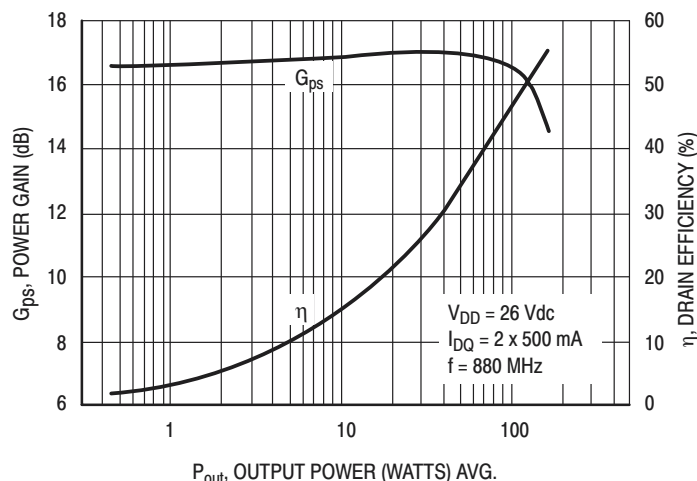


Figure 7. Power Gain and Efficiency versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

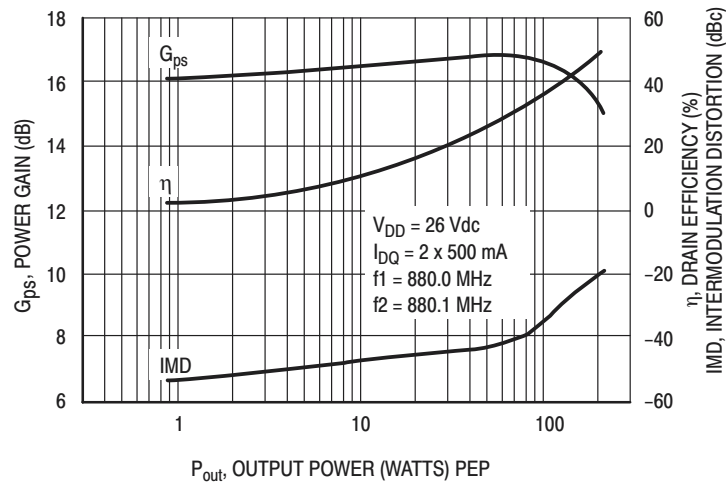


Figure 8. Power Gain, Efficiency and IMD versus Output Power

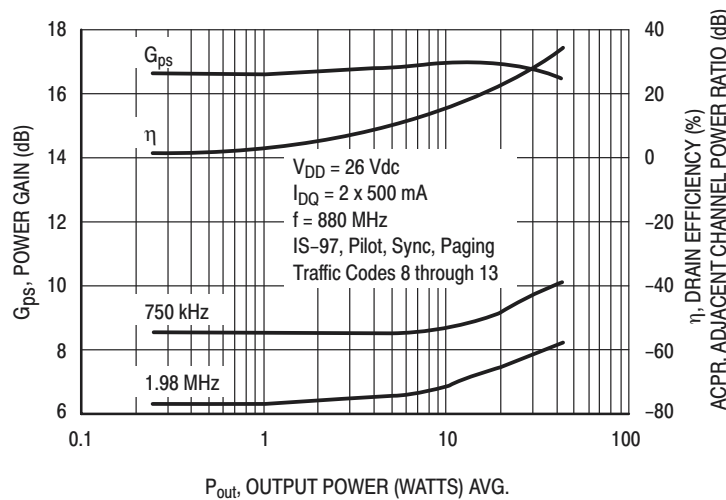
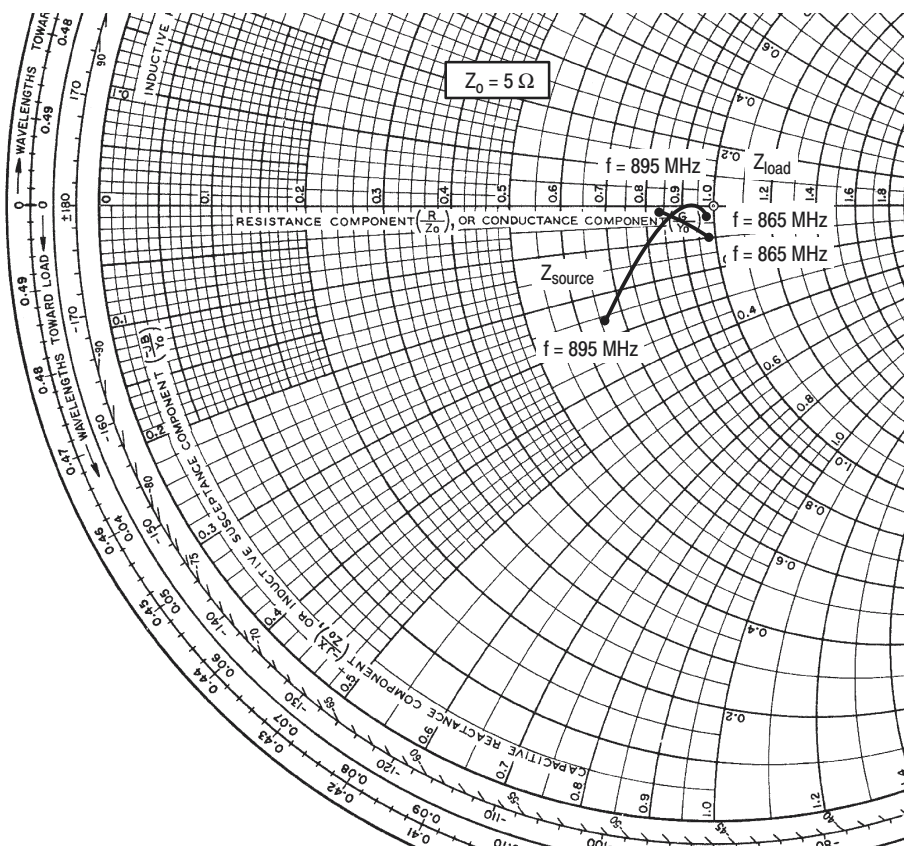


Figure 9. Power Gain, Efficiency and ACPR versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 2 \times 500 \text{ mA}$, $P_{out} = 120 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
865	$4.89 - j0.2$	$4.9 - j0.5$
880	$4.54 + j0.07$	$4.6 - j0.32$
895	$3.29 - j1.3$	$4.2 - j0.04$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

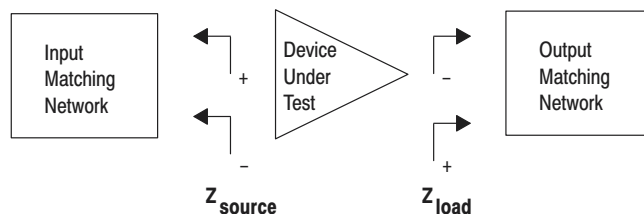


Figure 10. Series Equivalent Input and Output Impedance

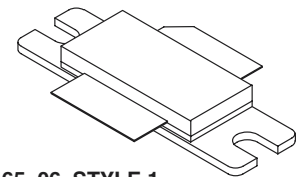
The RF Sub-Micron MOSFET Line RF Power Field Effect Transistors N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and EDGE base station applications with frequencies from 921 to 960 MHz, the high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

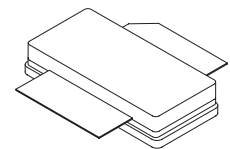
- Typical Performance for GSM Frequencies, 921 to 960 MHz, 28 Volts Output Power @ P1dB — 135 Watts
Power Gain — 16.5 dB @ 130 Watts Output Power
Efficiency — 48% @ 130 Watts Output Power
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, All Frequency Band, 130 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

MRF9130L
MRF9130LR3
MRF9130LSR3

GSM/EDGE
921–960 MHz, 130 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
(NI-780)
(MRF9130L)



CASE 465A-06, STYLE 1
(NI-780S)
(MRF9130LSR3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	298 1.7	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)
Charge Device Model	C7

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	$^\circ\text{C}/\text{W}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 0

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vds, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vds, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 450 μAdc)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 1000 mAdc)	V _{GS(Q)}	—	3.6	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 3 Adc)	V _{DS(on)}	—	0.2	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 9 Adc)	g _{fs}	—	12	—	S

DYNAMIC CHARACTERISTICS (1)

Output Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	110	—	pF
Reverse Transfer Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	4.4	—	pF

FUNCTIONAL TESTS (In Motorola Test Fixture)

Power Output, 1 dB Compression Point (V _{DD} = 28 Vdc, I _{DQ} = 1000 mA, f = 921 and 960 MHz)	P _{1dB}	120	135	—	W
Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 130 W, I _{DQ} = 1000 mA, f = 921 and 960 MHz)	G _{ps}	15.5	16.5	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 130 W, I _{DQ} = 1000 mA, f = 921 and 960 MHz)	η	43	48	—	%
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 130 W, I _{DQ} = 1000 mA, f = 921 and 960 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 130 W CW, I _{DQ} = 1000 mA, f = 921 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally input matched.

Freescale Semiconductor, Inc.

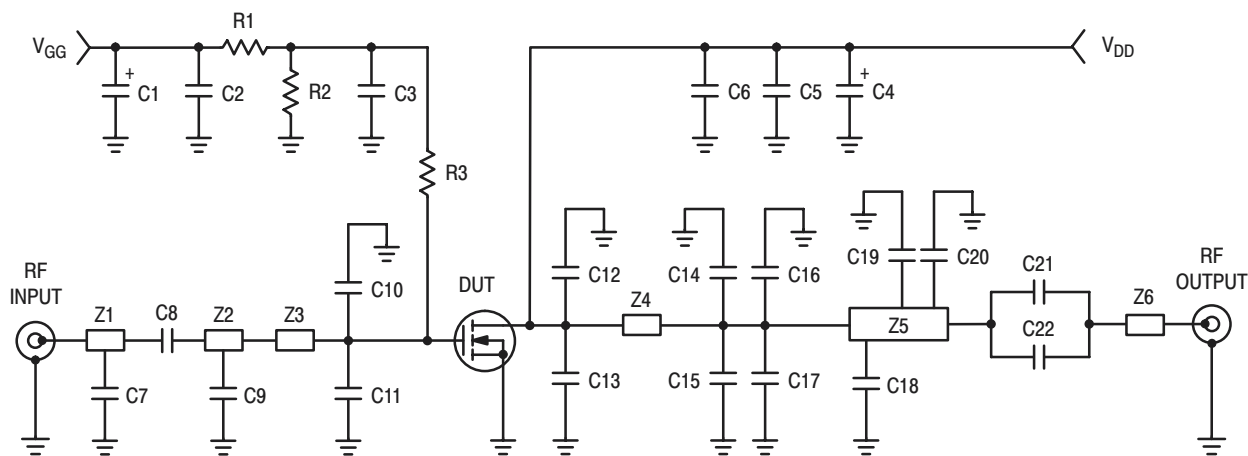


Figure 1. 921–960 MHz Test Circuit Schematic

Table 1. 921–960 MHz Test Circuit Component Designations and Values

Designators	Description
C1, C4	10 μ F, 35 V Tantalum Capacitors, Vishay–Sprague #293D106X9035D
C2, C5	100 nF Chip Capacitors (1206), AVX #1206C104KATDA
C3, C8, C21, C22	22 pF, 100B Chip Capacitors, ATC #100B220C
C6	33 pF, 100B Chip Capacitor, ATC #100B330JW
C7	1.0 pF, 100B Chip Capacitor, ATC #100B1R0BW
C9	4.7 pF, 100B Chip Capacitor, ATC #100B4R7BW
C10	8.2 pF, 100B Chip Capacitor, ATC #100B8R2CW
C11	10 pF, 100B Chip Capacitor, ATC #100B100GW
C12, C13	12 pF, 100B Chip Capacitors, ATC #100B120GW
C14, C15	2.7 pF, 100B Chip Capacitors, ATC #100B2R7BW
C16, C17, C18	3.9 pF, 100B Chip Capacitors, ATC #100B3R9BW
C19	3.3 pF, 100B Chip Capacitor, ATC #100B3R3BW
C20	1.8 pF, 100B Chip Capacitor, ATC #100B1R8BW
R1	18 k Ω , 1/8 W Chip Resistor (1206)
R2	10 k Ω , 1/8 W Chip Resistor (1206)
R3	1.0 k Ω , 1/8 W Chip Resistor (1206)
Z1	0.117" x 0.600" Microstrip
Z2	0.117" x 1.851" Microstrip
Z3	1.074" x 1.068" Microstrip
Z4	1.074" x 0.980" Microstrip
Z5	0.117" x 1.933" Microstrip
Z6	0.117" x 0.605" Microstrip
Substrate	Taconic TLX8, Thickness 0.8 mm
	RF Connectors, Type N, Macom #3052–1648–10

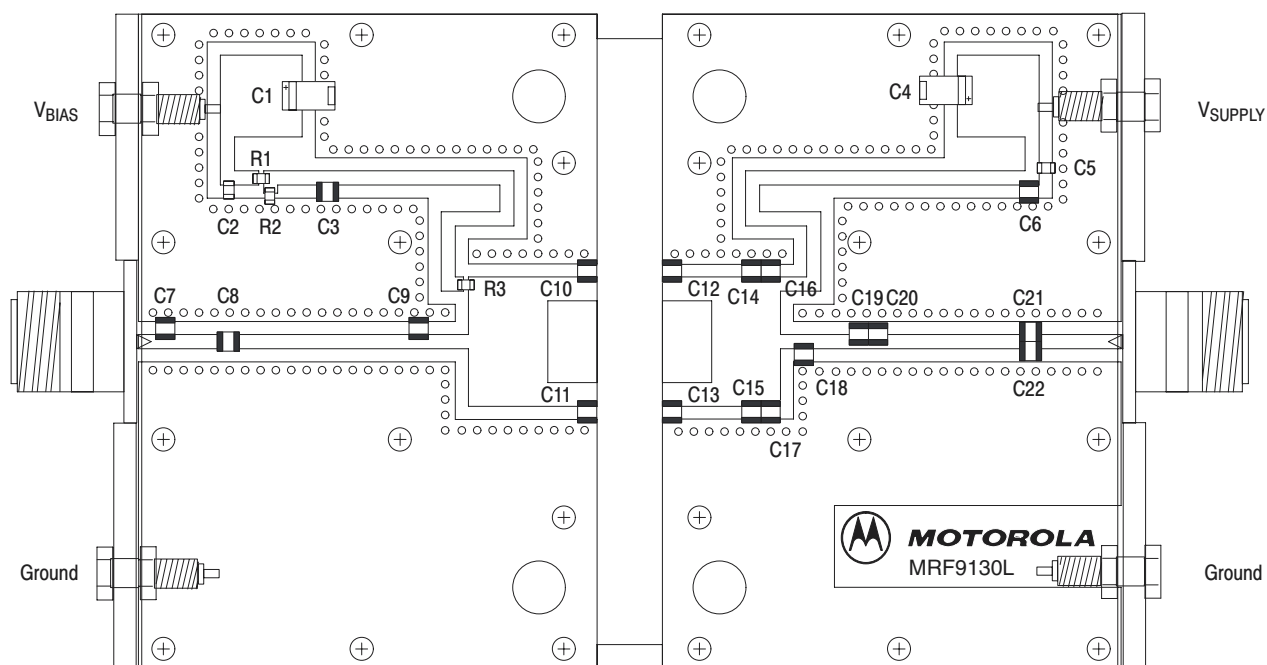


Figure 2. 921-960 MHz Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

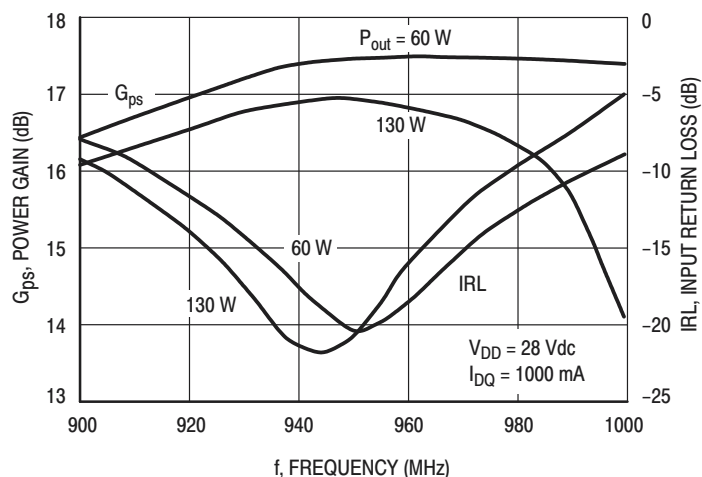


Figure 3. Power Gain and Input Return Loss versus Frequency

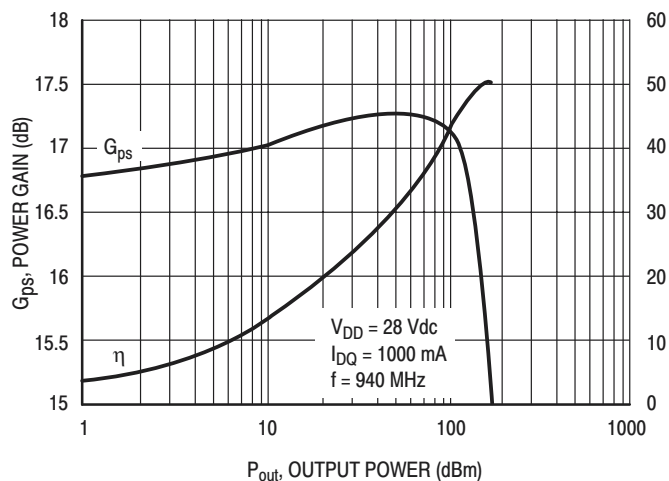


Figure 4. Power Gain and Efficiency versus Output Power

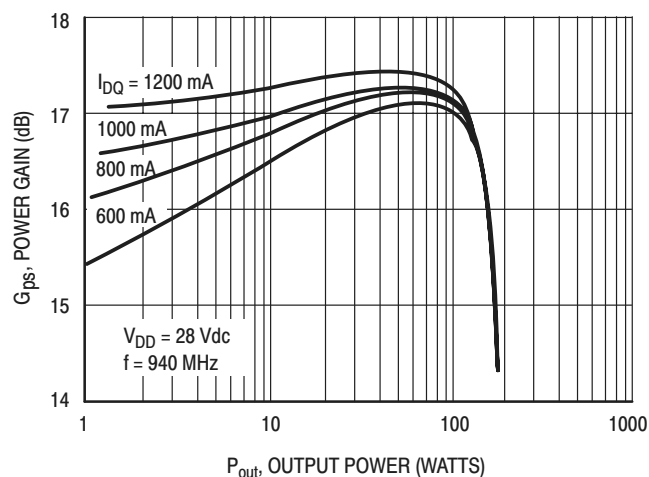


Figure 5. Power Gain versus Output Power

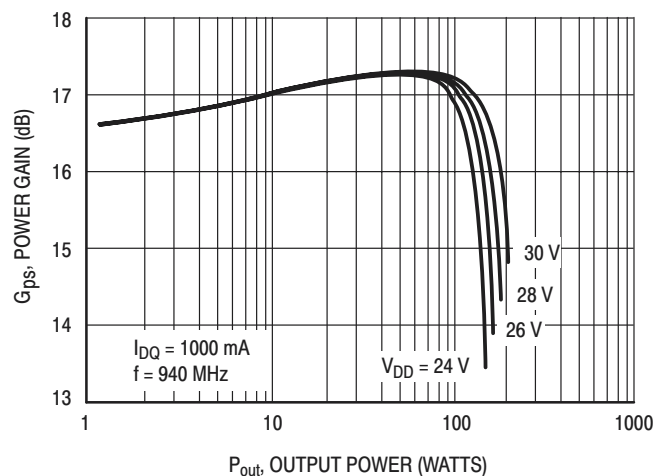


Figure 6. Power Gain versus Output Power

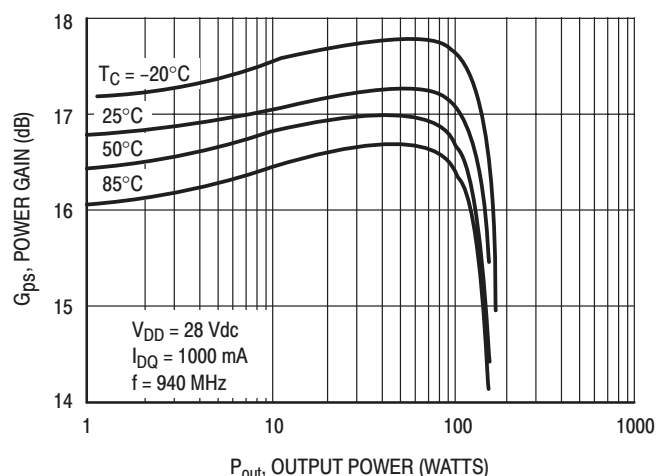


Figure 7. Power Gain versus Output Power

Freescale Semiconductor, Inc.

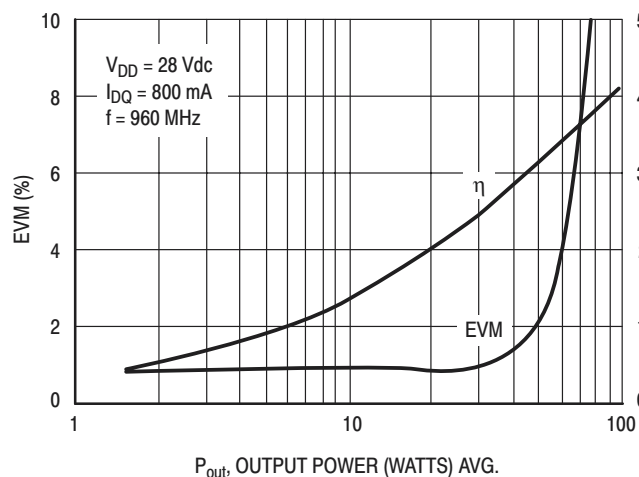


Figure 8. EVM and Efficiency versus Output Power

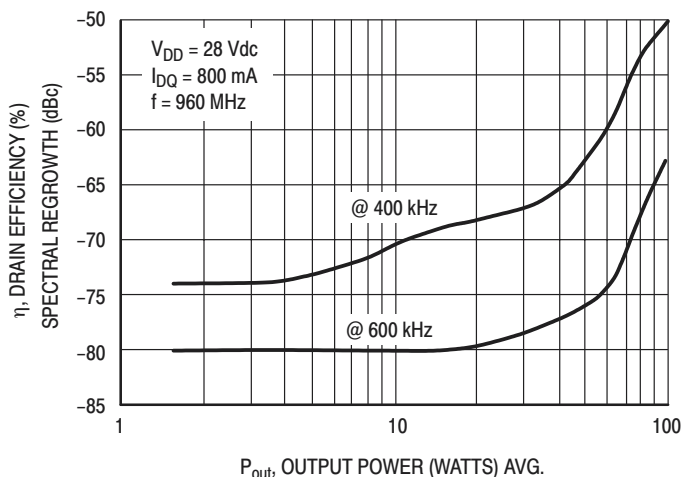
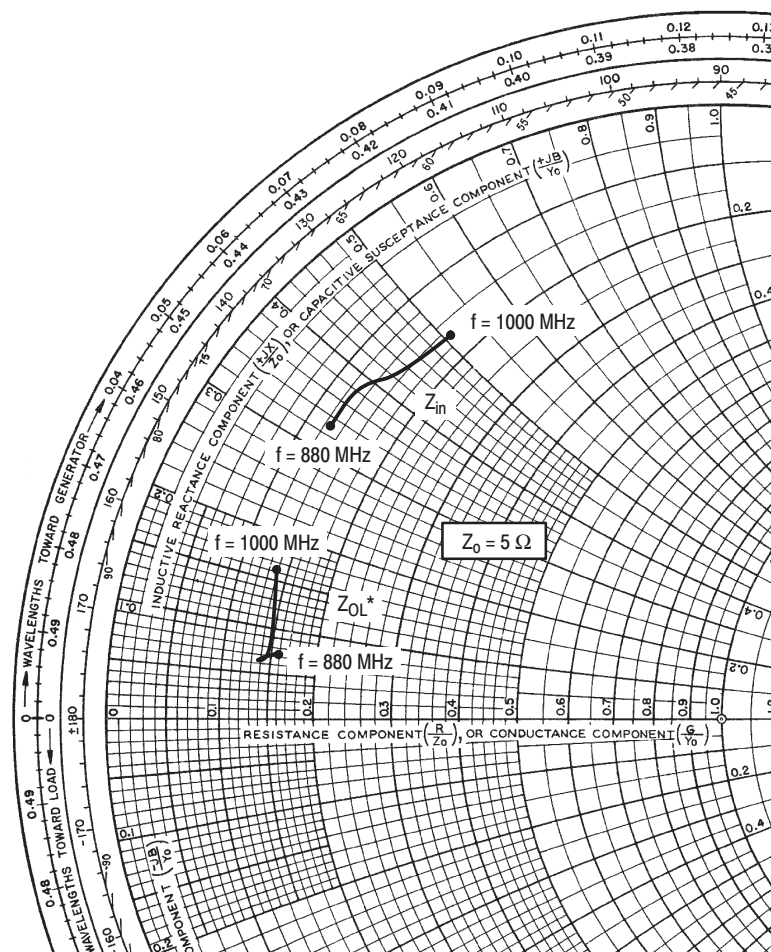


Figure 9. Spectral Regrowth versus Output Power

NOTE: Curves on Figure 8 and 9 gathered on a GSM EDGE optimized text fixture.



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1000 \text{ mA}$, $P_{out} = 135 \text{ W (CW)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
880	$0.63 + j1.66$	$0.82 + j0.36$
920	$0.67 + j1.88$	$0.72 + j0.30$
960	$0.82 + j2.18$	$0.74 + j0.37$
1000	$0.86 + j2.56$	$0.69 + j0.79$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

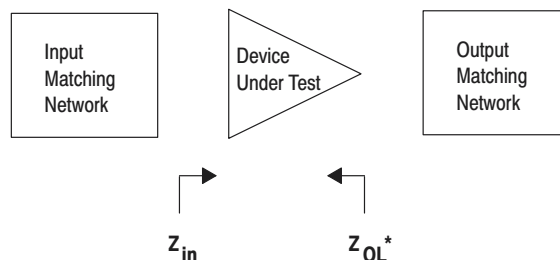


Figure 10. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

- Typical N-CDMA Performance @ 880 MHz, 26 Volts, $I_{DQ} = 1100$ mA
IS-95 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 25 Watts Avg.
Power Gain — 17.8 dB
Efficiency — 25%
Adjacent Channel Power —
750 kHz: -47 dBc @ 30 kHz BW
- Internally Matched, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 135 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40 μ m Nominal.

MRF9135L
MRF9135LR3
MRF9135LSR3

880 MHz, 135 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs

CASE 465-06, STYLE 1
NI-780
MRF9135L

CASE 465A-06, STYLE 1
NI-780S
MRF9135LSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	298 1.7	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	$^\circ\text{C}/\text{W}$

ESD PROTECTION CHARACTERISTICS

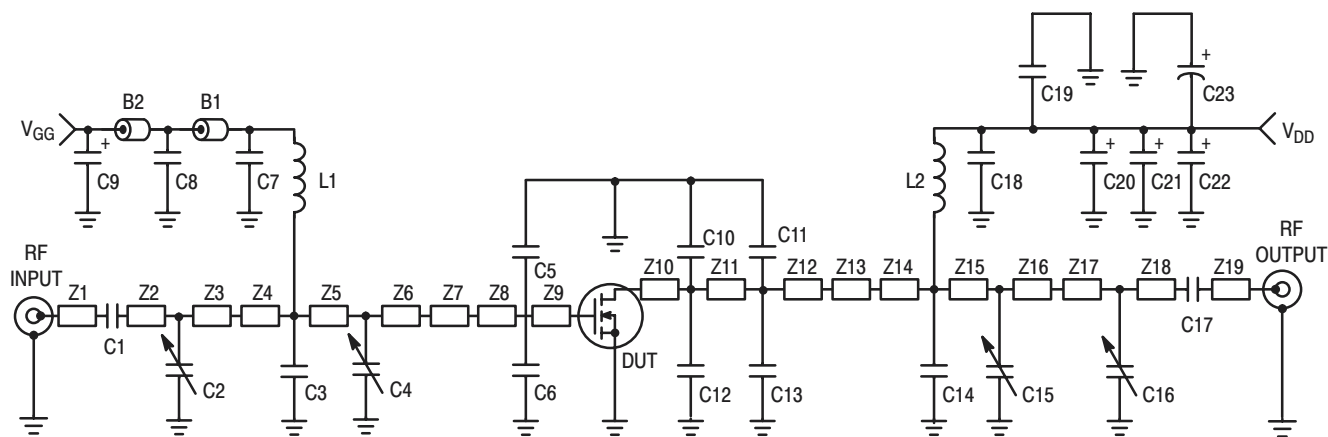
Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)
Charge Device Model	C7 (Minimum)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, 50 ohm system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current ($V_{GS} = 5 \text{ Vdc}$, $V_{DS} = 0 \text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 10 \text{ Vdc}$, $I_D = 450 \mu\text{A}$)	$V_{GS(th)}$	2	2.8	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26 \text{ Vdc}$, $I_D = 1100 \text{ mAdc}$)	$V_{GS(Q)}$	3	3.7	5	Vdc
Drain–Source On–Voltage ($V_{GS} = 10 \text{ Vdc}$, $I_D = 3 \text{ Adc}$)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ Vdc}$, $I_D = 9 \text{ Adc}$)	g_{fs}	—	12	—	S
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{DS} = 26 \text{ Vdc} \pm 30 \text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0 \text{ Vdc}$)	C_{oss}	—	109	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26 \text{ Vdc} \pm 30 \text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0 \text{ Vdc}$)	C_{rss}	—	4.4	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) Single–Carrier N–CDMA, 1.2288 MHz Channel Bandwidth Carrier, Peak/Avg. Ratio = 9.8 dB @ 0.01% Probability on CCDF					
Common–Source Amplifier Power Gain ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg. N–CDMA}$, $I_{DQ} = 1100 \text{ mA}$, $f = 880.0 \text{ MHz}$)	G_{ps}	16	17.8	—	dB
Drain Efficiency ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg. N–CDMA}$, $I_{DQ} = 1100 \text{ mA}$, $f = 880.0 \text{ MHz}$)	η	22	25	—	%
Adjacent Channel Power Ratio ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg. N–CDMA}$, $I_{DQ} = 1100 \text{ mA}$, $f = 880.0 \text{ MHz}$; ACPR @ 25 W, 1.23 MHz Bandwidth, 750 kHz Channel Spacing)	ACPR	—	–47	–45	dBc
Input Return Loss ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg. N–CDMA}$, $I_{DQ} = 1100 \text{ mA}$, $f = 880.0 \text{ MHz}$)	IRL	—	–13.5	–9	dB
Common–Source Amplifier Power Gain ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg. N–CDMA}$, $I_{DQ} = 1100 \text{ mA}$, $f = 865 \text{ MHz}$ and 895 MHz)	G_{ps}	—	17	—	dB
Drain Efficiency ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg. N–CDMA}$, $I_{DQ} = 1100 \text{ mA}$, $f = 865 \text{ MHz}$ and 895 MHz)	η	—	24	—	%
Adjacent Channel Power Ratio ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg. N–CDMA}$, $I_{DQ} = 1100 \text{ mA}$, $f = 865 \text{ MHz}$ and 895 MHz ; ACPR @ 25 W, 1.23 MHz Bandwidth, 750 kHz Channel Spacing)	ACPR	—	–46	—	dBc
Input Return Loss ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 25 \text{ W Avg. N–CDMA}$, $I_{DQ} = 1100 \text{ mA}$, $f = 865 \text{ MHz}$ and 895 MHz)	IRL	—	–12.5	—	dB
Output Mismatch Stress ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 135 \text{ W CW}$, $I_{DQ} = 1100 \text{ mA}$, $f = 880.0 \text{ MHz}$, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			



Z1	0.430" x 0.080" Microstrip	Z11	0.105" x 0.630" Microstrip
Z2	0.430" x 0.080" Microstrip	Z12	0.145" x 0.630" Microstrip
Z3	0.800" x 0.080" Microstrip	Z13	0.200" x 0.630" x 0.220" Taper
Z4	0.200" x 0.220" Microstrip	Z14	0.180" x 0.220" Microstrip
Z5	0.110" x 0.220" Microstrip	Z15	0.110" x 0.220" Microstrip
Z6	0.175" x 0.220" Microstrip	Z16	0.200" x 0.220" Microstrip
Z7	0.200" x 0.220" x 0.630" Taper	Z17	0.900" x 0.080" Microstrip
Z8	0.250" x 0.630" Microstrip	Z18	0.360" x 0.080" Microstrip
Z9	0.050" x 0.630" Microstrip	Z19	0.410" x 0.080" Microstrip
Z10	0.050" x 0.630" Microstrip	PCB	Arlon GX-0300-55-22, 30 mil, $\epsilon_r = 2.55$

Figure 1. 880 MHz Test Circuit Schematic

Table 1. 880 MHz Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1, B2	Short Ferrite Beads, Surface Mount	95F786	Newark
C1, C7, C17, C18	47 pF Chip Capacitors, B Case	100B470JP 500X	ATC
C2, C16	0.6–4.5 Gigatrim Variable Capacitors	44F3360	Newark
C3	8.2 pF Chip Capacitor, B Case	100B8R2BP 500X	ATC
C4, C15	0.8–8.0 Gigatrim Variable Capacitors	44F3360	Newark
C5, C6	12 pF Chip Capacitors, B Case	100B120JP 500X	ATC
C8	20K pF Chip Capacitor, B Case	200B203MP50X	ATC
C9, C20, C21, C22	10 μ F, 35 V Tantalum Capacitors	93F2975	Newark
C10, C11, C12, C13	7.5 pF Chip Capacitors, B Case	100B7R5JP 500X	ATC
C14	11 pF Chip Capacitor, B Case	100B110JP 500X	ATC
C19	0.56 μ F, 50 V Chip Capacitor	C1825C564K5RA7800	Kemet
C23	470 μ F Electrolytic Capacitor	14F185	Newark
L1, L2	12.5 nH Coilcraft inductors	A04T-5	Coilcraft
WB1, WB2	10 mil Brass Shim (0.205 x 0.530)	RF-Design Lab	RF-Design Lab

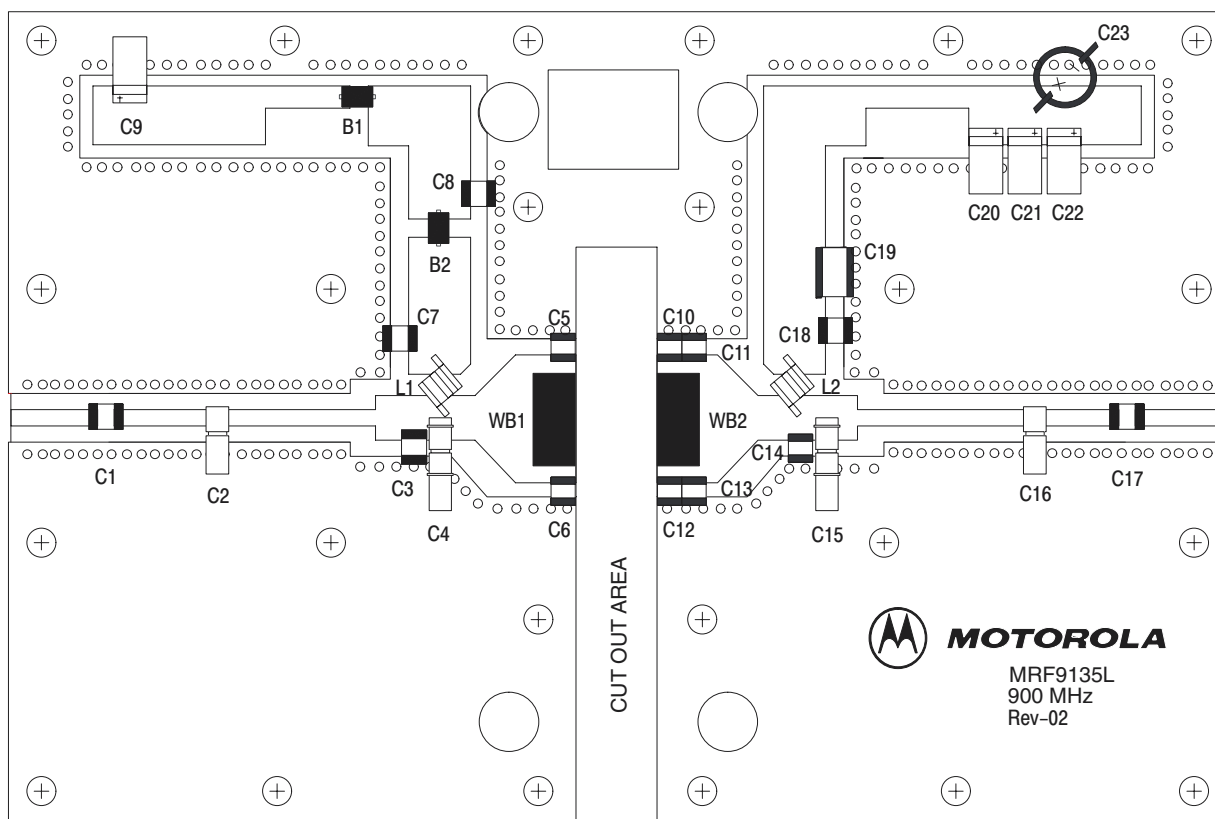


Figure 2. 880 MHz Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

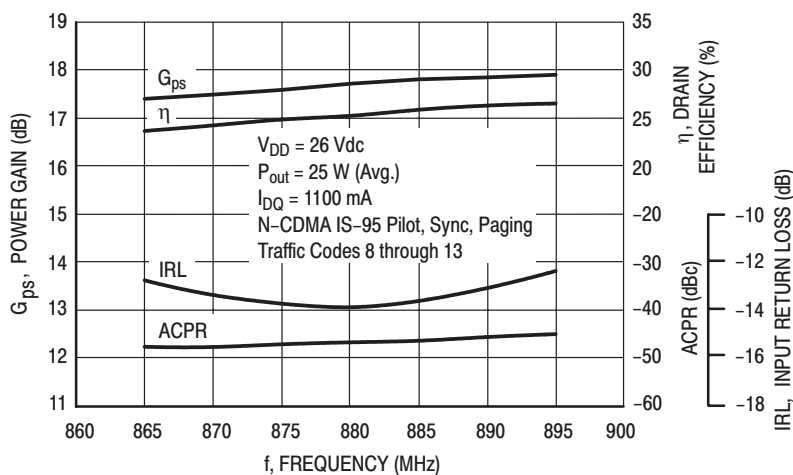


Figure 3. Class AB Broadband Circuit Performance

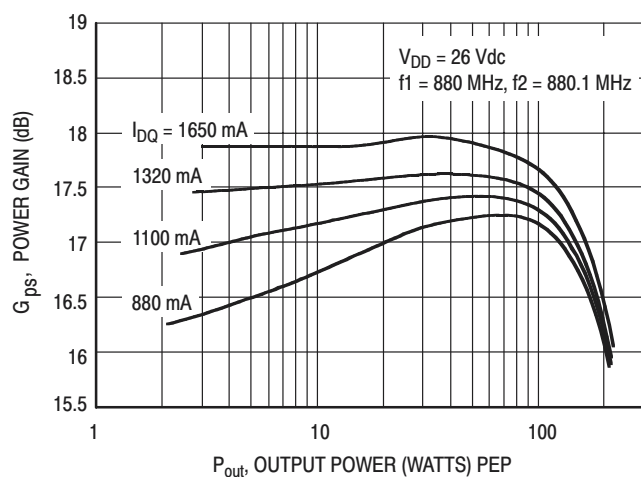


Figure 4. Power Gain versus Output Power

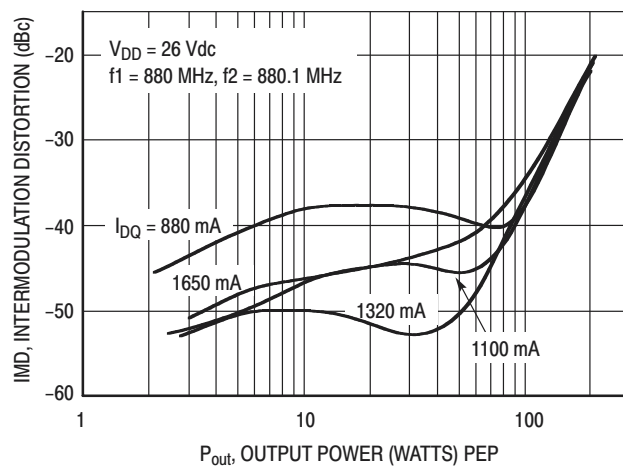


Figure 5. Intermodulation Distortion versus Output Power

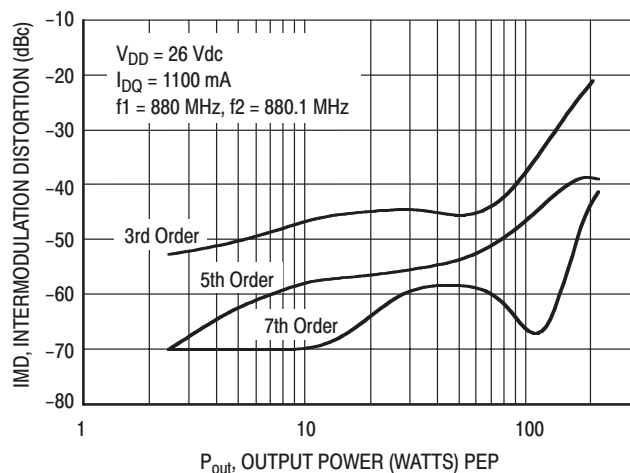


Figure 6. Intermodulation Distortion Products versus Output Power

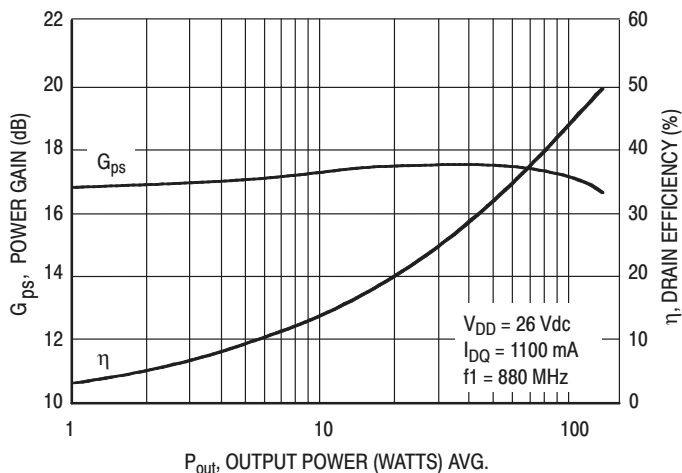


Figure 7. Power Gain and Efficiency versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

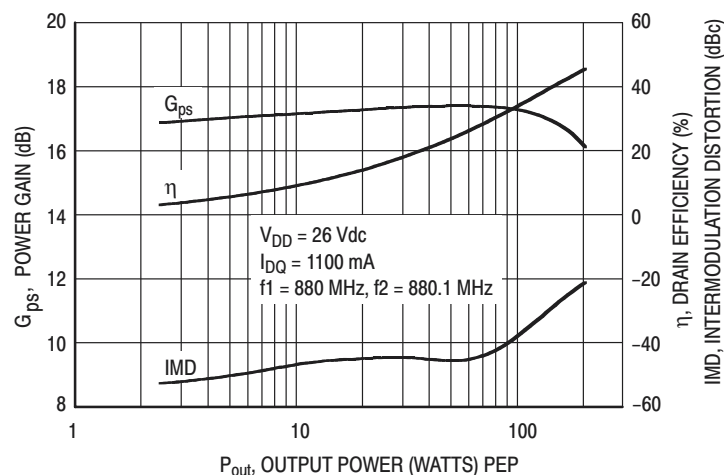


Figure 8. Power Gain, Efficiency and IMD versus Output Power

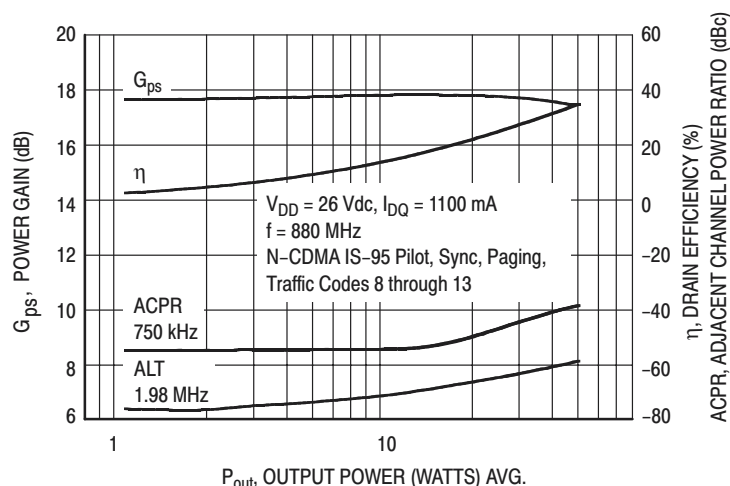


Figure 9. N-CDMA Performance Output Power versus Gain, ACPR, Efficiency

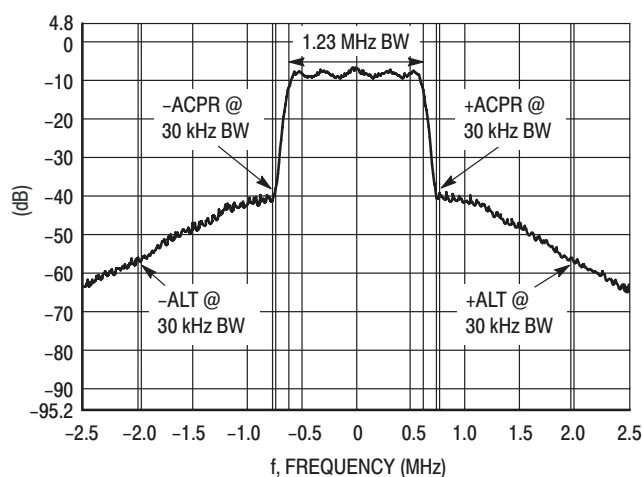
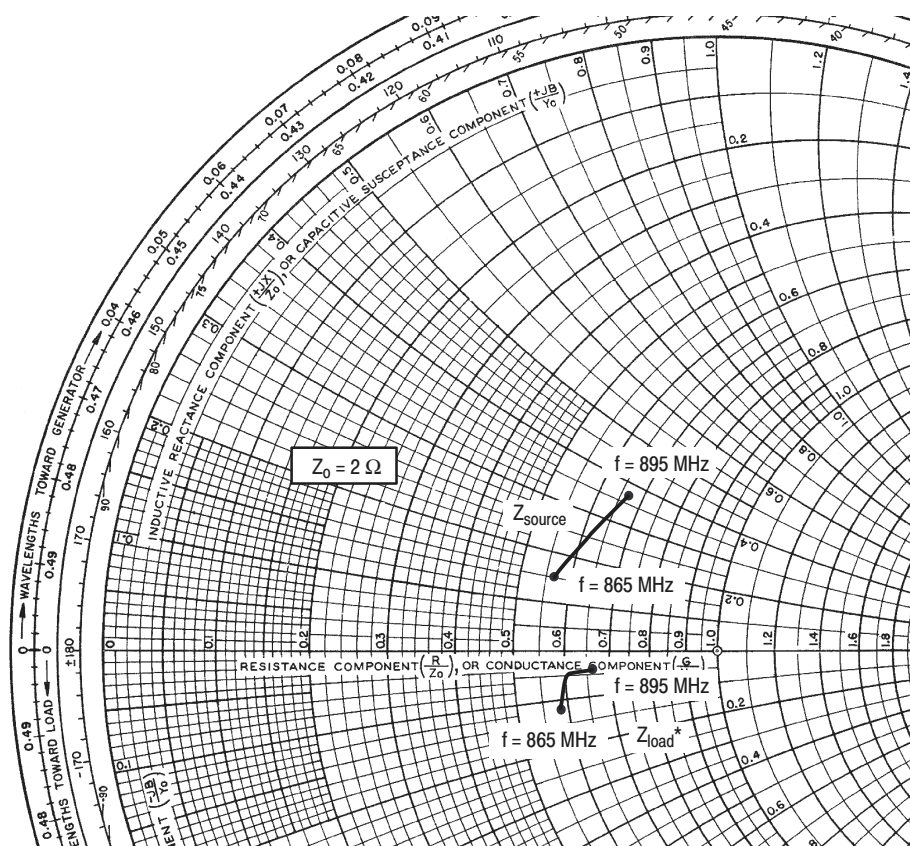


Figure 10. Typical CDMA Spectrum



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 1100 \text{ mA}$, $P_{out} = 25 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
865	$1.15 + j0.3$	$1.17 - j0.24$
880	$1.25 + j0.5$	$1.22 - j0.1$
895	$1.35 + j0.75$	$1.32 - j0.07$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

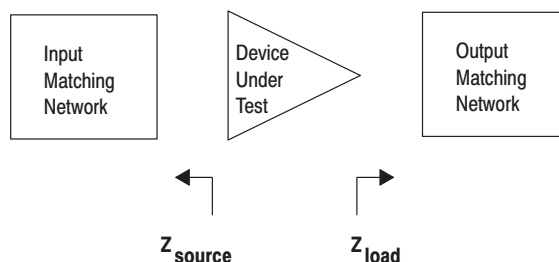


Figure 11. Series Equivalent Input and Output Impedance

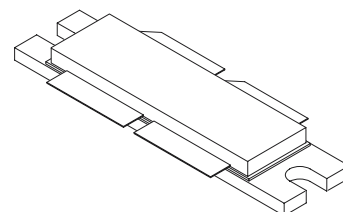
The RF Sub-Micron MOSFET Line RF Power Field Effect Transistors N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

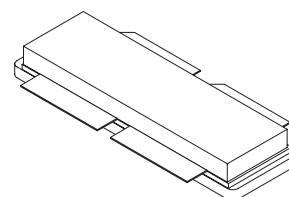
- Typical CDMA Performance @ 880 MHz, 26 Volts, $I_{DQ} = 2 \times 700$ mA
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 40 Watts
Power Gain — 17 dB
Efficiency — 26%
Adjacent Channel Power —
750 kHz: -45.0 dBc @ 30 kHz BW
1.98 MHz: -60.0 dBc @ 30 kHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 170 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

MRF9180
MRF9180S

880 MHz, 170 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 375D-04, STYLE 1
NI-1230
MRF9180



CASE 375E-03, STYLE 1
NI-1230S
MRF9180S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	388 2.22	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2	2.9	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 700 mAdc)	V _{GS(Q)}	—	3.7	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.19	0.5	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 6 Adc)	g _{fs}	—	6	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	77	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	3.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)					
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 170 W PEP, I _{DQ} = 2 × 700 mA, f ₁ = 880.0 MHz, f ₂ = 880.1 MHz)	G _{ps}	16	17.5	—	dB
Two–Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 170 W PEP, I _{DQ} = 2 × 700 mA, f ₁ = 880.0 MHz, f ₂ = 880.1 MHz)	η	35	39	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 170 W PEP, I _{DQ} = 2 × 700 mA, f ₁ = 880.0 MHz, f ₂ = 880.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 170 W PEP, I _{DQ} = 2 × 700 mA, f ₁ = 880.0 MHz, f ₂ = 880.1 MHz)	IRL	—	–15	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 170 W PEP, I _{DQ} = 2 × 700 mA, f ₁ = 865.0 MHz, f ₂ = 865.1 MHz)	G _{ps}	—	17.5	—	dB
Two–Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 170 W PEP, I _{DQ} = 2 × 700 mA, f ₁ = 865.0 MHz, f ₂ = 865.1 MHz)	η	—	38.5	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 170 W PEP, I _{DQ} = 2 × 700 mA, f ₁ = 865.0 MHz, f ₂ = 865.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 170 W PEP, I _{DQ} = 2 × 700 mA, f ₁ = 865.0 MHz, f ₂ = 865.1 MHz)	IRL	—	–13	—	dB
Power Output, 1 dB Compression Point (V _{DD} = 26 Vdc, CW, I _{DQ} = 2 × 700 mA, f ₁ = 880.0 MHz)	P _{1dB}	—	170	—	W

(1) Each side of device measured separately.

(2) Device measured in push–pull configuration.

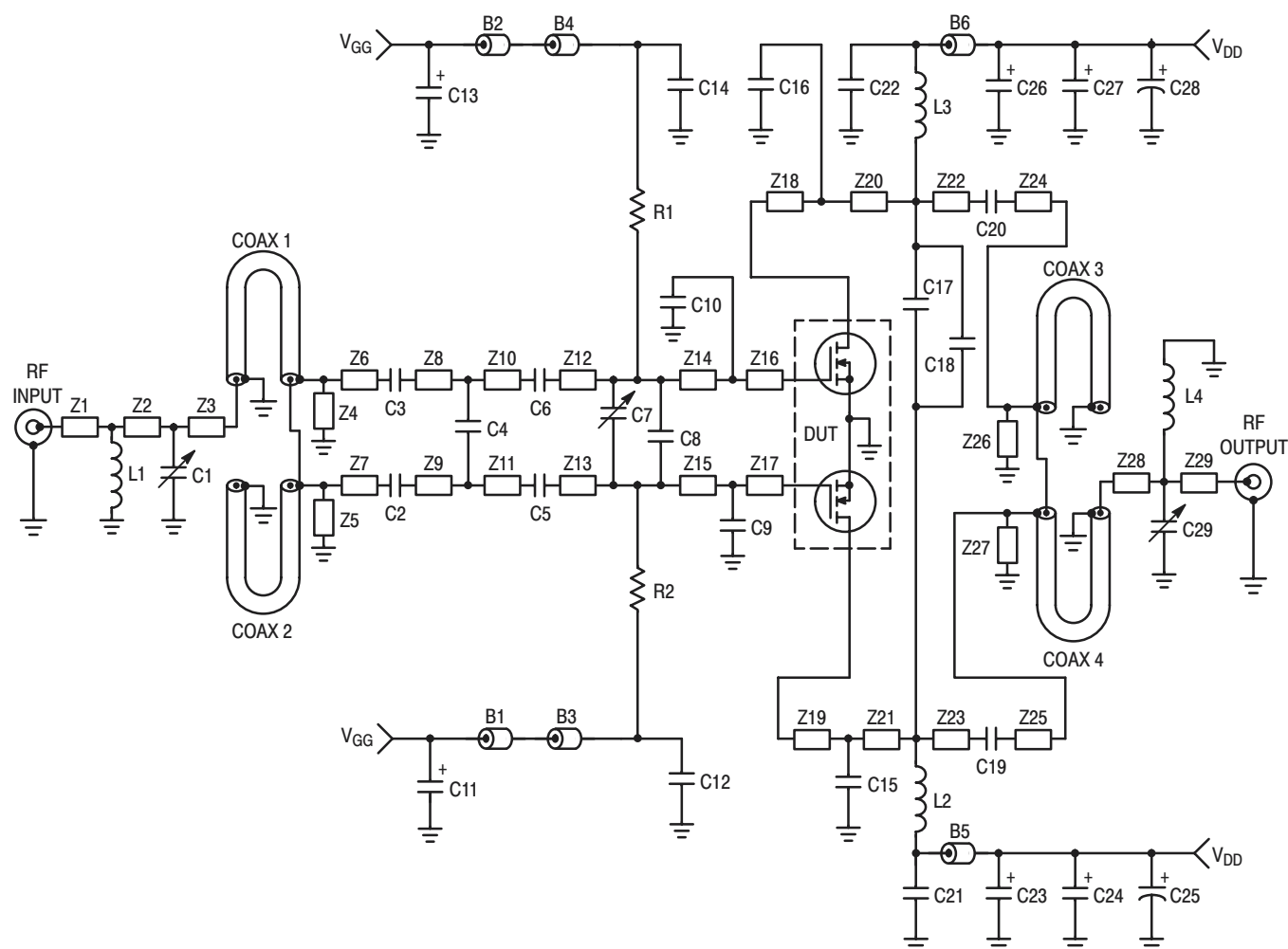
Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) (continued)					
Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W CW}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	G_{ps}	—	16.5	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W CW}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	η	—	55	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W CW}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f = 880\text{ MHz}$, $VSWR = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(2) Device measured in push–pull configuration.

Freescale Semiconductor, Inc.



B1, B2, B5, B6	Long Ferrite Beads, Surface Mount	Z1	0.420" x 0.080" Microstrip
B3, B4	Short Ferrite Beads, Surface Mount	Z2	0.190" x 0.080" Microstrip
C1	0.6–4.5 pF Variable Capacitor	Z3	0.097" x 0.080" Microstrip
C2, C3, C5, C6, C12, C14, C19, C20, C21, C22	47 pF Chip Capacitors, B Case	Z4, Z5, Z26, Z27	2.170" x 0.080" Microstrip
C4, C9, C10, C15, C16	12 pF Chip Capacitors, B Case	Z6, Z7	0.075" x 0.080" Microstrip
C7	0.8–9.1 pF Variable Capacitor	Z8, Z9	0.088" x 0.220" Microstrip
C8	7.5 pF Chip Capacitor, B Case	Z10, Z11	0.088" x 0.220" Microstrip
C11, C13	10 μ F, 35 V Tantalum Surface Mount Chip Capacitors	Z12, Z13	0.460" x 0.220" Microstrip
C17	3.6 pF Chip Capacitor, B Case	Z14, Z15	0.685" x 0.625" Microstrip
C18	5.1 pF Chip Capacitor, B Case	Z16, Z17	0.055" x 0.625" Microstrip
C23, C24, C26, C27	22 μ F, 35 V Tantalum Surface Mount Chip Capacitors	Z18, Z19	0.055" x 0.632" Microstrip
C25, C28	220 μ F, 50 V Electrolytic Capacitors	Z20, Z21	0.685" x 0.632" Microstrip
C29	0.4–2.5 pF Variable Capacitor	Z22, Z23	0.732" x 0.080" Microstrip
Coax1, Coax2	25 Ω , Semi Rigid Coax, 70 mil OD, 1.05" Long	Z24, Z25	0.060" x 0.080" Microstrip
Coax3, Coax4	50 Ω , Semi Rigid Coax, 85 mil OD, 1.05" Long	Z28	0.230" x 0.080" Microstrip
L1, L2, L3	18.5 nH Mini Spring Inductors, Coilcraft	Z29	0.460" x 0.080" Microstrip
L4	12.5 nH Mini Spring Inductor, Coilcraft	Board	30 mil Teflon [®] , $\epsilon_r = 2.55$,
R1, R2	510 Ω , 1/10 W Chip Resistors	Material	Copper Clad, 2 oz Cu

Figure 1. 880 MHz Broadband Test Circuit Schematic

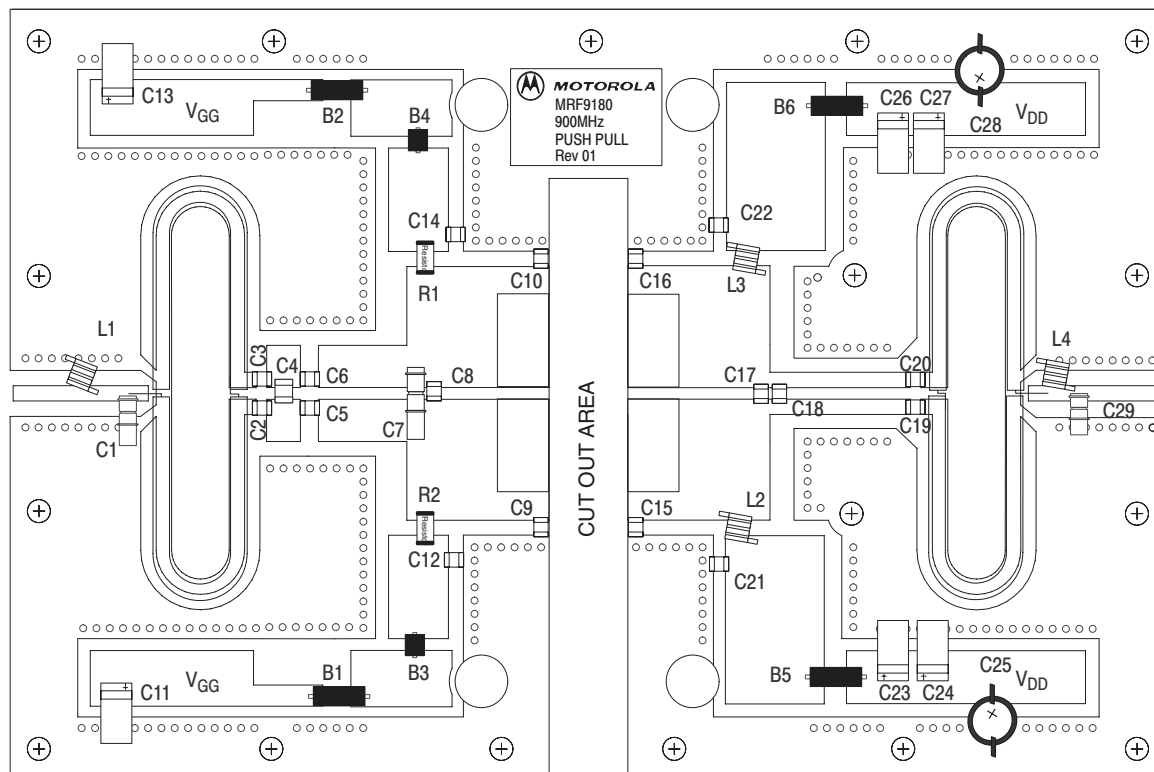


Figure 2. 880 MHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

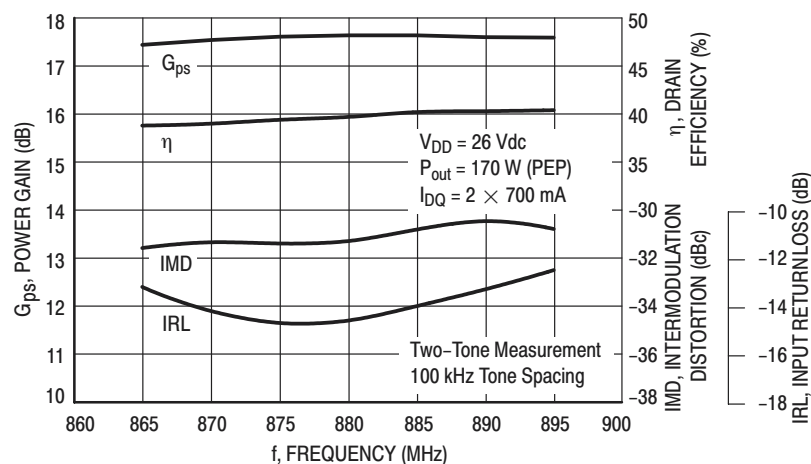


Figure 3. Class AB Broadband Circuit Performance

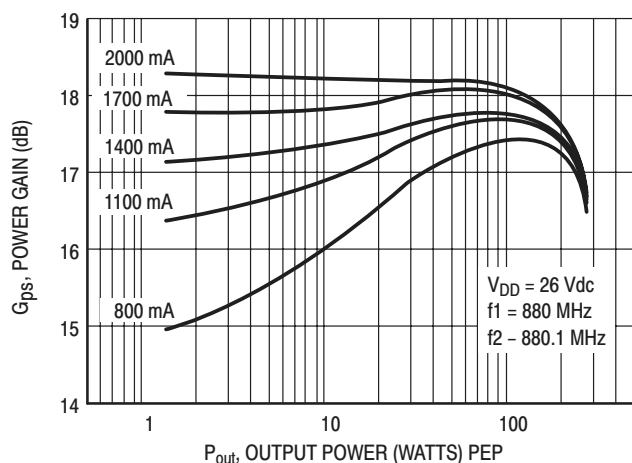


Figure 4. Power Gain versus Output Power

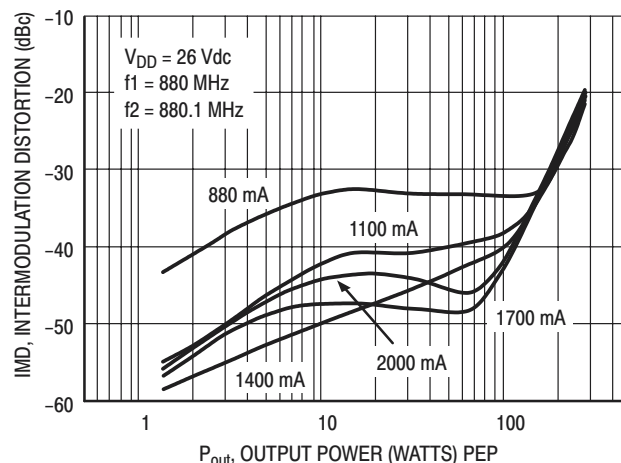


Figure 5. Intermodulation Distortion versus Output Power

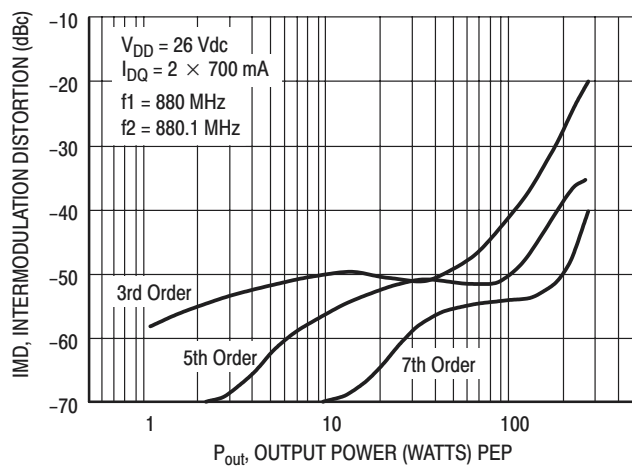


Figure 6. Intermodulation Distortion Products versus Output Power

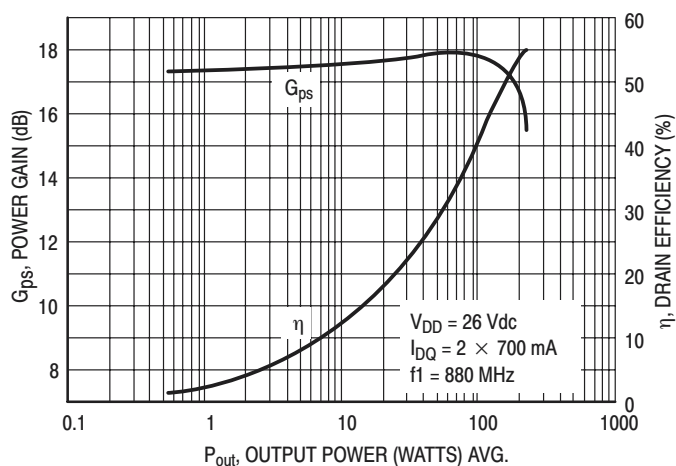


Figure 7. Power Gain and Efficiency versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

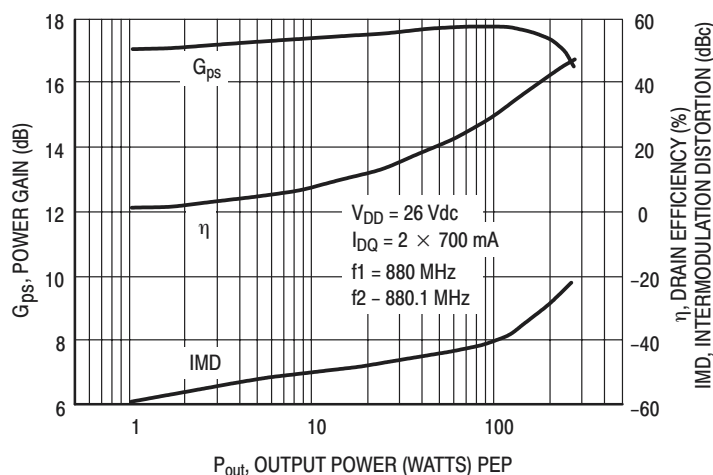


Figure 8. Power Gain, Efficiency and IMD versus Output Power

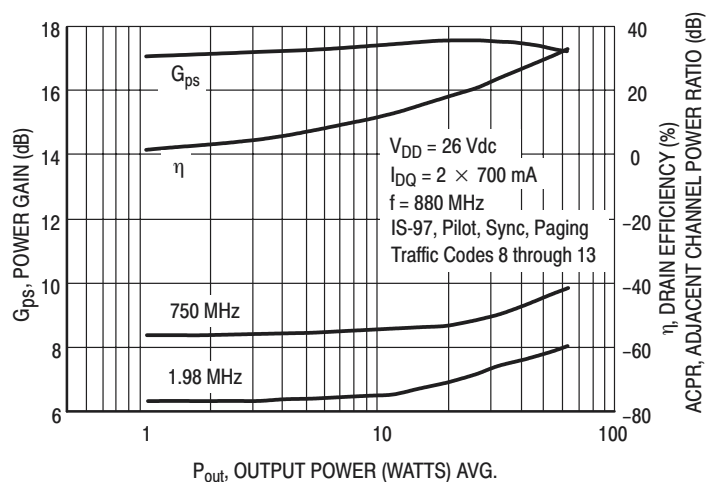
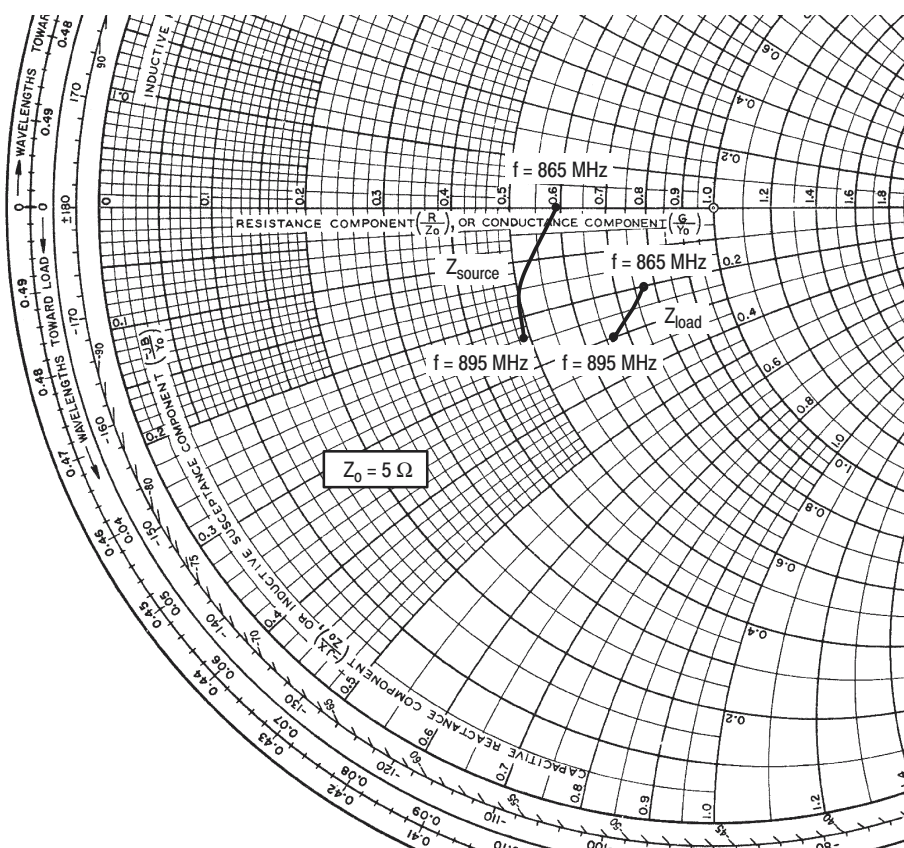


Figure 9. Power Gain, Efficiency and ACPR versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 2 \times 700 \text{ mA}$, $P_{out} = 170 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
865	$2.95 - j0.00$	$3.83 - j1.02$
880	$2.48 - j0.67$	$3.55 - j1.38$
895	$2.44 - j1.18$	$3.34 - j1.51$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

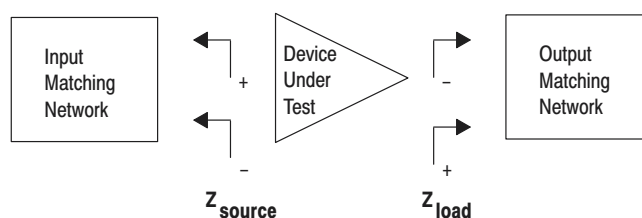


Figure 10. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors N-Channel Enhancement-Mode Lateral MOSFETs

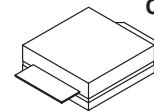
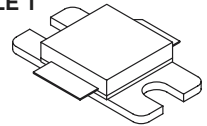
Designed for GSM and EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. Specified for GSM 1805 – 1880 MHz.

- Typical GSM Performance:
Power Gain – 14 dB (Typ) @ 30 Watts
Efficiency – 50% (Typ) @ 30 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 30 W Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

MRF18030AR3
MRF18030ASR3

**GSM/GSM EDGE 1.8 – 1.88 GHz,
30 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs**

**CASE 465E-04, STYLE 1
NI-400
MRF18030AR3**



**CASE 465F-04, STYLE 1
NI-400S
MRF18030ASR3**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	83.3 0.48	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, 50 ohm system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 20 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 250 mAdc)	V _{GS(Q)}	2	3.9	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.29	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 1 Adc)	g _{fs}	—	2	—	S

DYNAMIC CHARACTERISTICS

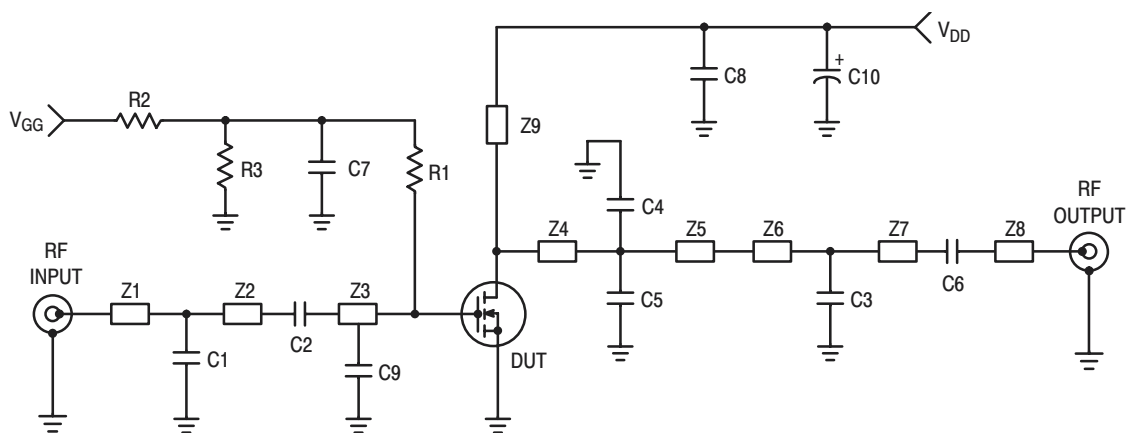
Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	1.3	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture) (2)

Output Power, 1 dB Compression Point (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1805 – 1880 MHz)	P _{1dB}	27	30	—	Watts
Common–Source Amplifier Power Gain @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1805 – 1880 MHz)	G _{ps}	13	14	—	dB
Drain Efficiency @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1805 – 1880 MHz)	η	46.5	50	—	%
Input Return Loss @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1805 – 1880 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f ₁ = 1805 – 1880 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

- (1) Part is internally matched both on input and output.
(2) Device specifications obtained on a Production Test Fixture.

Freescale Semiconductor, Inc.



C1	1.8 pF, 100B Chip Capacitor	Z1	0.874" x 0.087" Microstrip
C2	0.8 pF, 100B Chip Capacitor	Z2	1.094" x 0.087" Microstrip
C3	1.0 pF, 100B Chip Capacitor	Z3	0.257" x 0.633" Microstrip
C4, C5	1.2 pF, 100B Chip Capacitors	Z4	0.189" x 0.394" Microstrip
C6, C7, C8	8.2 pF, 100B Chip Capacitors	Z5	0.335" x 0.394" Microstrip
C9	0.3 pF, 100B Chip Capacitor	Z6	0.484" x 0.087" Microstrip
C10	220 μ F, 63 V Electrolytic Capacitor	Z7	0.877" x 0.087" Microstrip
R1	1.0 k Ω , 1/8 W Chip Resistor (0805)	Z8	0.366" x 0.087" Microstrip
R2, R3	10 k Ω , 1/8 W Chip Resistors (0805)	Z9	$\approx$ 0.600" x 0.087" Microstrip

Figure 1. 1805 – 1880 MHz Test Fixture Schematic

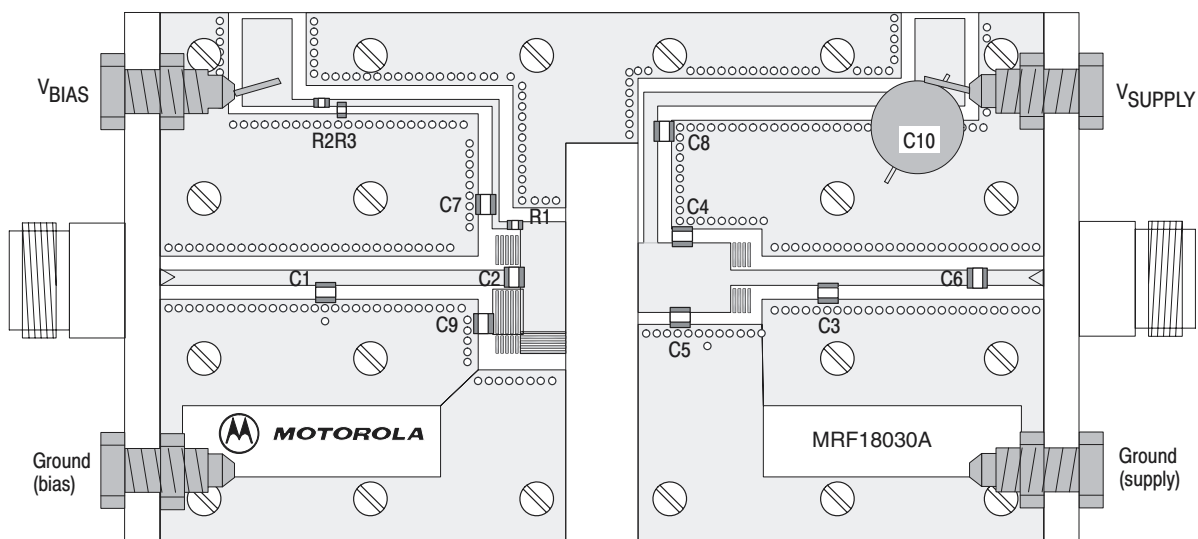


Figure 2. 1805 – 1880 MHz Test Fixture Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

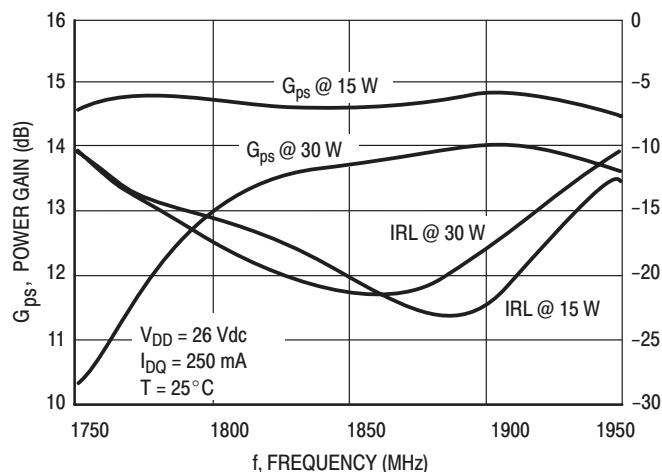


Figure 3. Wideband Gain and IRL at 30 W and 15 W Output Power

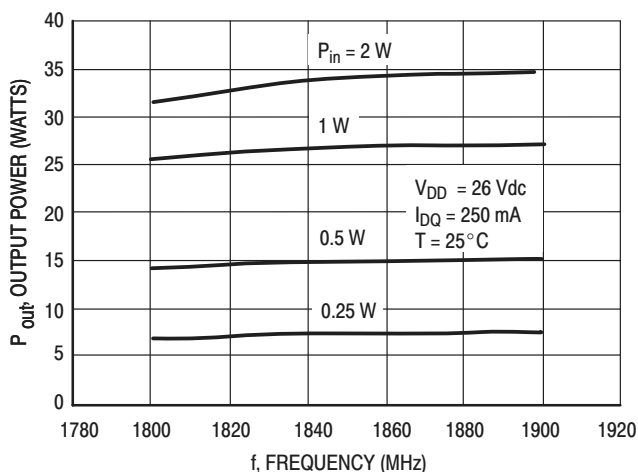


Figure 4. Output Power versus Frequency

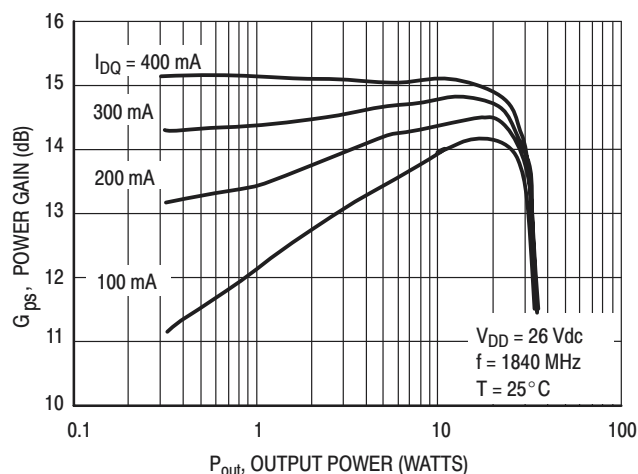


Figure 5. Power Gain versus Output Power

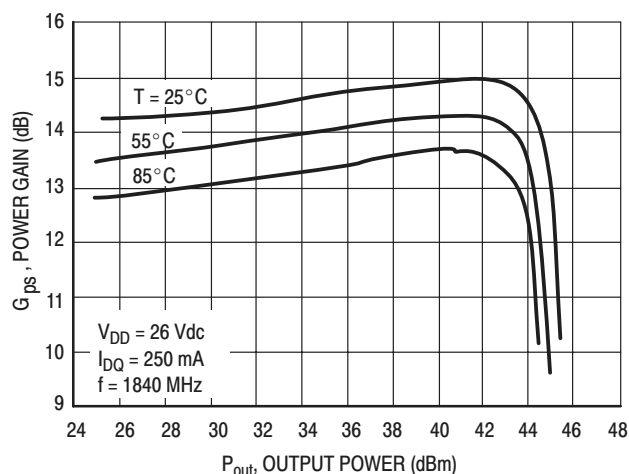


Figure 6. Power Gain versus Output Power

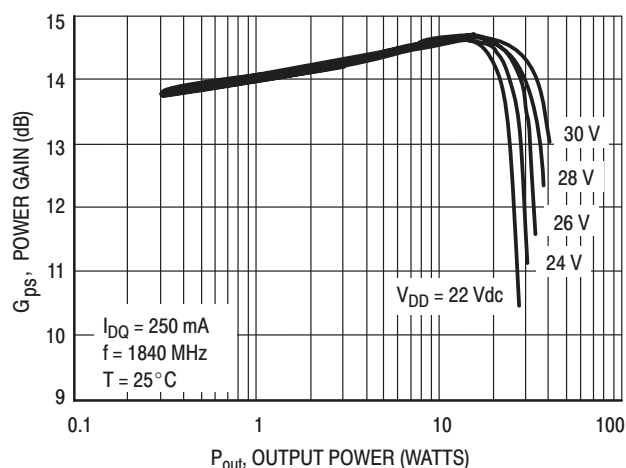


Figure 7. Power Gain versus Output Power

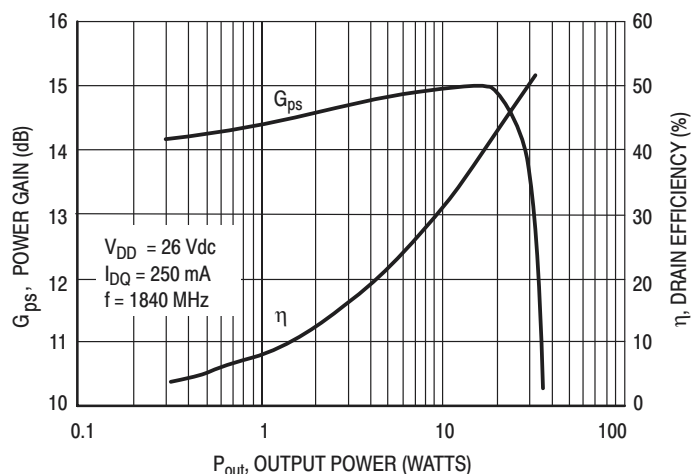
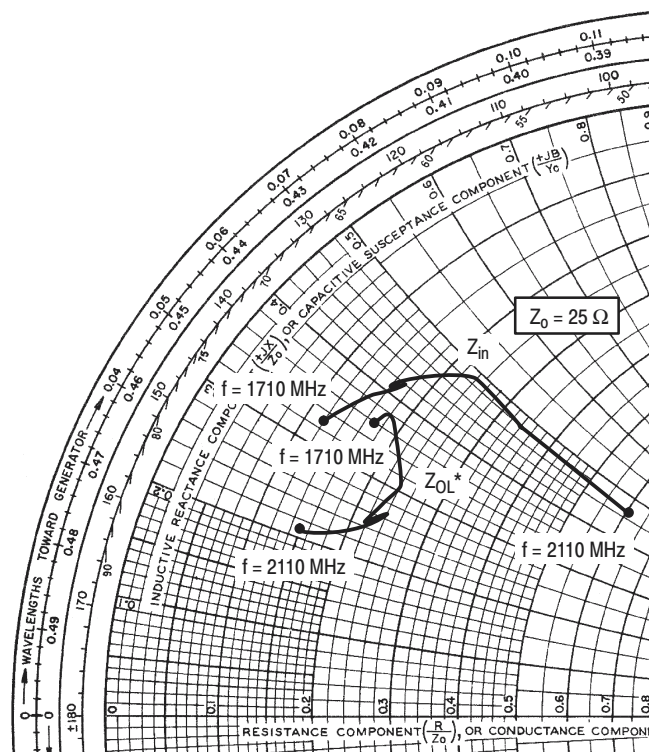


Figure 8. Power Gain and Efficiency versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 30 \text{ W (CW)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1710	$2.92 + j8.24$	$4.18 + j9.06$
1785	$3.84 + j9.75$	$4.59 + j9.46$
1805	$4.15 + j10.38$	$4.98 + j9.06$
1840	$4.04 + j10.22$	$6.10 + j7.63$
1880	$6.12 + j12.29$	$5.83 + j6.89$
1960	$6.20 + j12.29$	$5.55 + j6.33$
1990	$8.61 + j12.10$	$5.93 + j6.66$
2110	$15.19 + j11.85$	$3.82 + j5.33$

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given power, voltage, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, and drain efficiency.

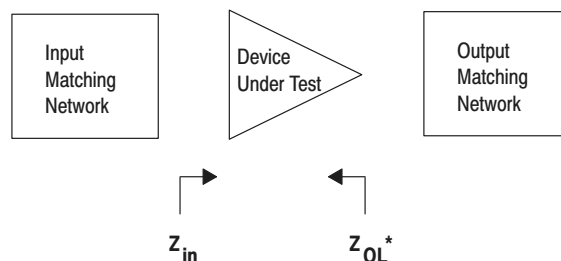


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. Specified for GSM 1930 – 1990 MHz.

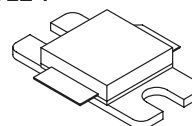
- Typical GSM Performance:
Power Gain – 14 dB (Typ) @ 30 Watts
Efficiency – 50% (Typ) @ 30 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 30 W CW Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

MRF18030BR3

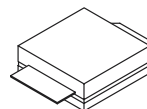
MRF18030BSR3

**GSM/GSM EDGE 1.93 – 1.99 GHz,
30 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs**

**CASE 465E-04, STYLE 1
NI-400
MRF18030BR3**



**CASE 465F-04, STYLE 1
NI-400S
MRF18030BSR3**



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	83.3 0.48	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, 50 ohm system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 20 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 250 mAdc)	V _{GS(Q)}	2	3.9	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.29	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 1 Adc)	g _{fs}	—	2	—	S

DYNAMIC CHARACTERISTICS

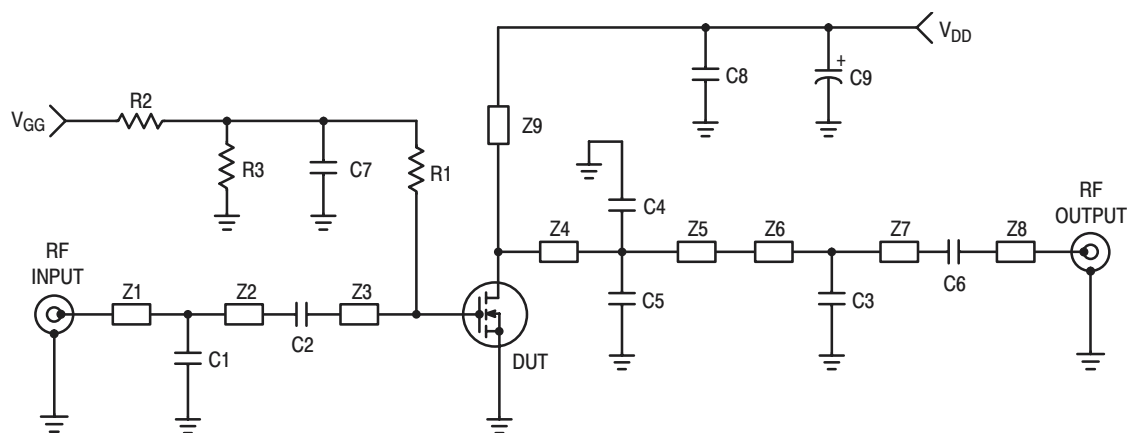
Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	1.3	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture) (2)

Output Power, 1 dB Compression Point (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1930 – 1990 MHz)	P1dB	27	30	—	Watts
Common–Source Amplifier Power Gain @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1930 – 1990 MHz)	G _{ps}	13	14	—	dB
Drain Efficiency @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1930 – 1990 MHz)	η	46.5	50	—	%
Input Return Loss @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f = 1930 – 1990 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress @ 30 W (V _{DD} = 26 Vdc, I _{DQ} = 250 mA, f1 = 1930 – 1990 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

- (1) Part is internally matched both on input and output.
(2) Device specifications obtained on a Production Test Fixture.

Freescale Semiconductor, Inc.



C1	1.8 pF, 100B Chip Capacitor	Z2	1.022" x 0.087" Microstrip
C2	0.8 pF, 100B Chip Capacitor	Z3	0.257" x 0.633" Microstrip
C3	0.8 pF, 100B Chip Capacitor	Z4	0.189" x 0.394" Microstrip
C4, C5	1.2 pF, 100B Chip Capacitors	Z5	0.335" x 0.394" Microstrip
C6, C7, C8	8.2 pF, 100B Chip Capacitors	Z6	0.616" x 0.087" Microstrip
C9	220 μ F, 63 V Electrolytic Capacitor	Z7	0.845" x 0.087" Microstrip
R1	1.0 k Ω , 1/8 W Chip Resistor (0805)	Z8	0.366" x 0.087" Microstrip
R2, R3	10 k Ω , 1/8 W Chip Resistors (0805)	Z9	$\approx$ 0.500" x 0.087" Microstrip
Z1	0.496" x 0.087" Microstrip		

Figure 1. 1930 – 1990 MHz Test Fixture Schematic

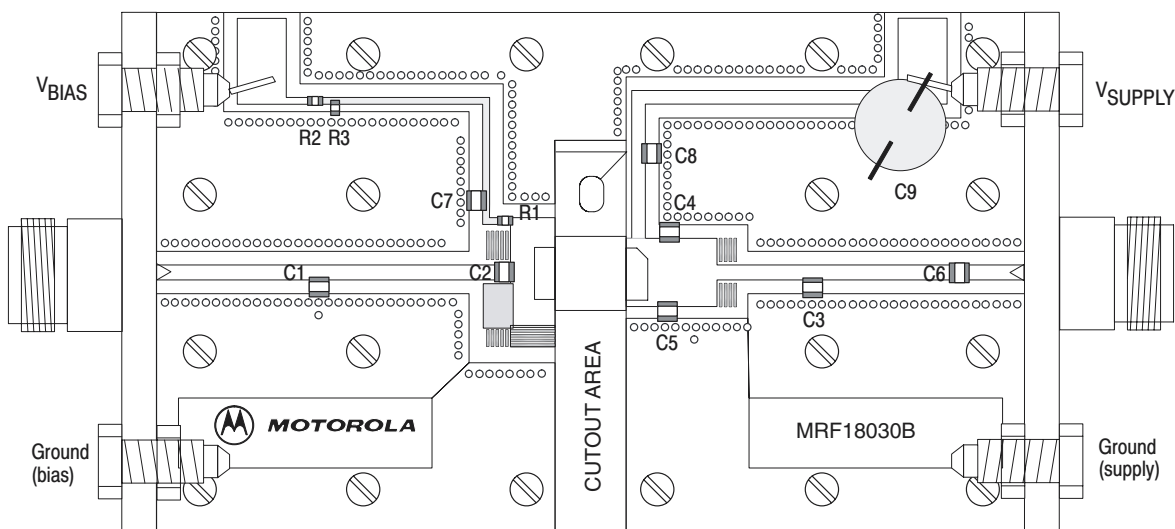


Figure 2. 1930 – 1990 MHz Test Fixture Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

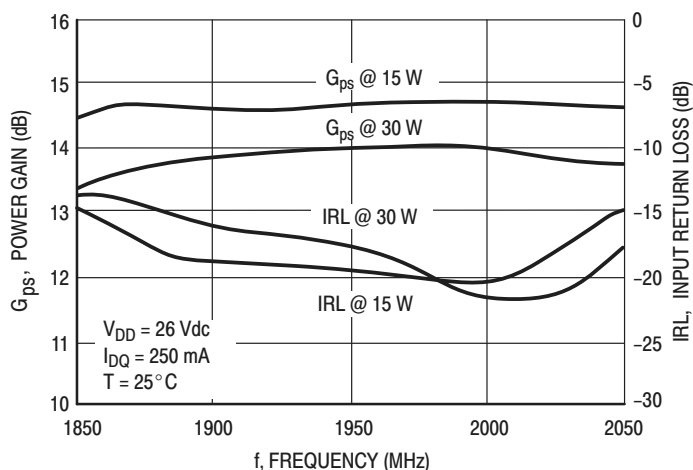


Figure 3. Wideband Gain and IRL at 30 W and 15 W Output Power

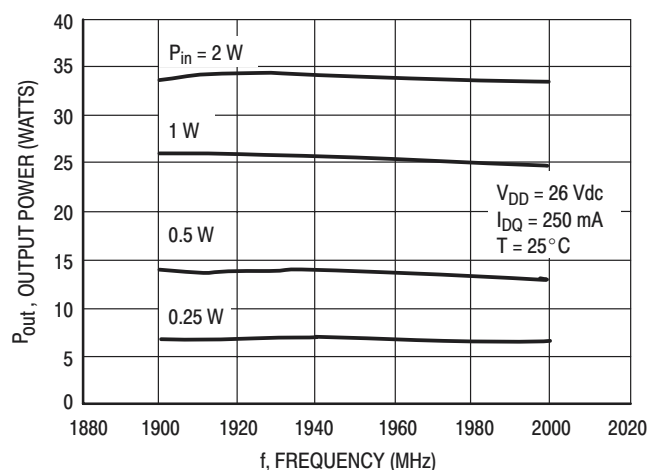


Figure 4. Output Power versus Frequency

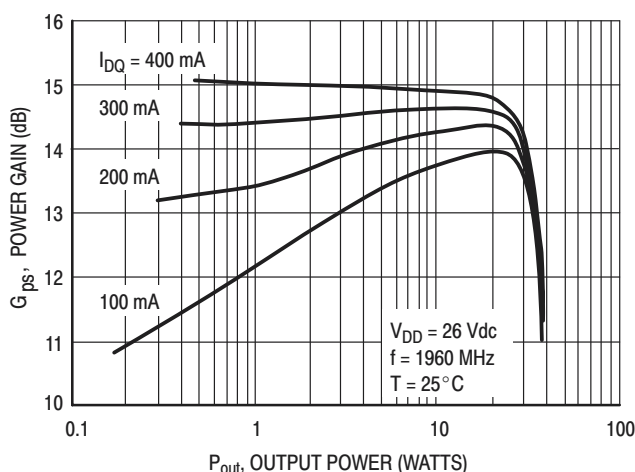


Figure 5. Power Gain versus Output Power

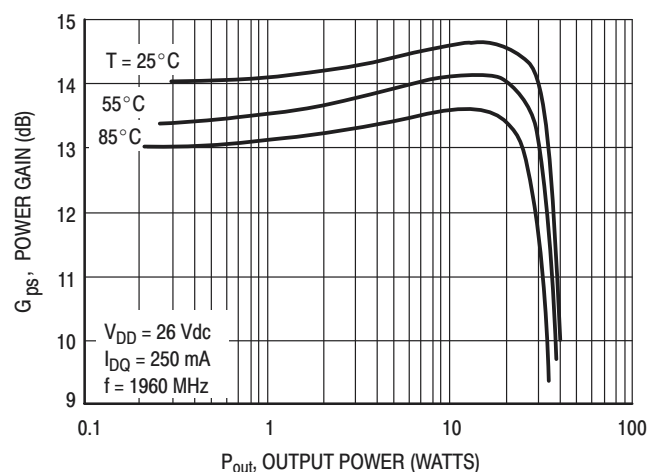


Figure 6. Power Gain versus Output Power

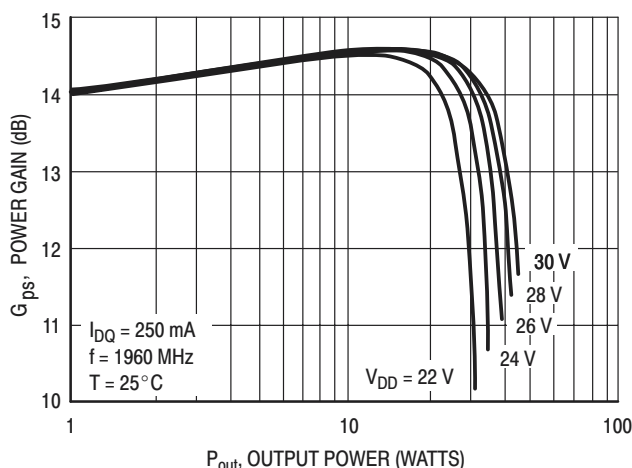


Figure 7. Power Gain versus Output Power

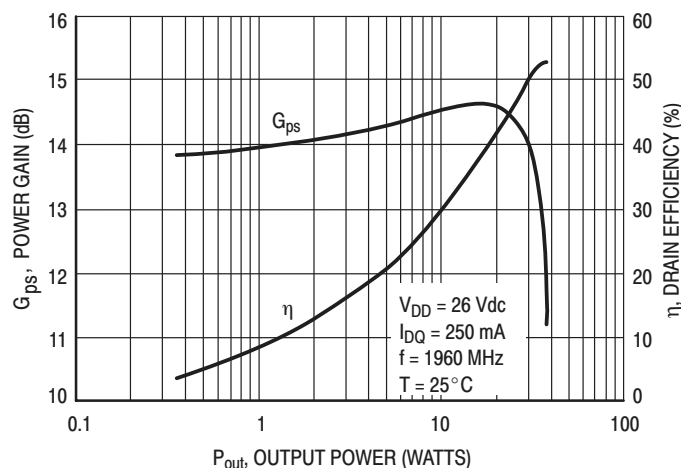
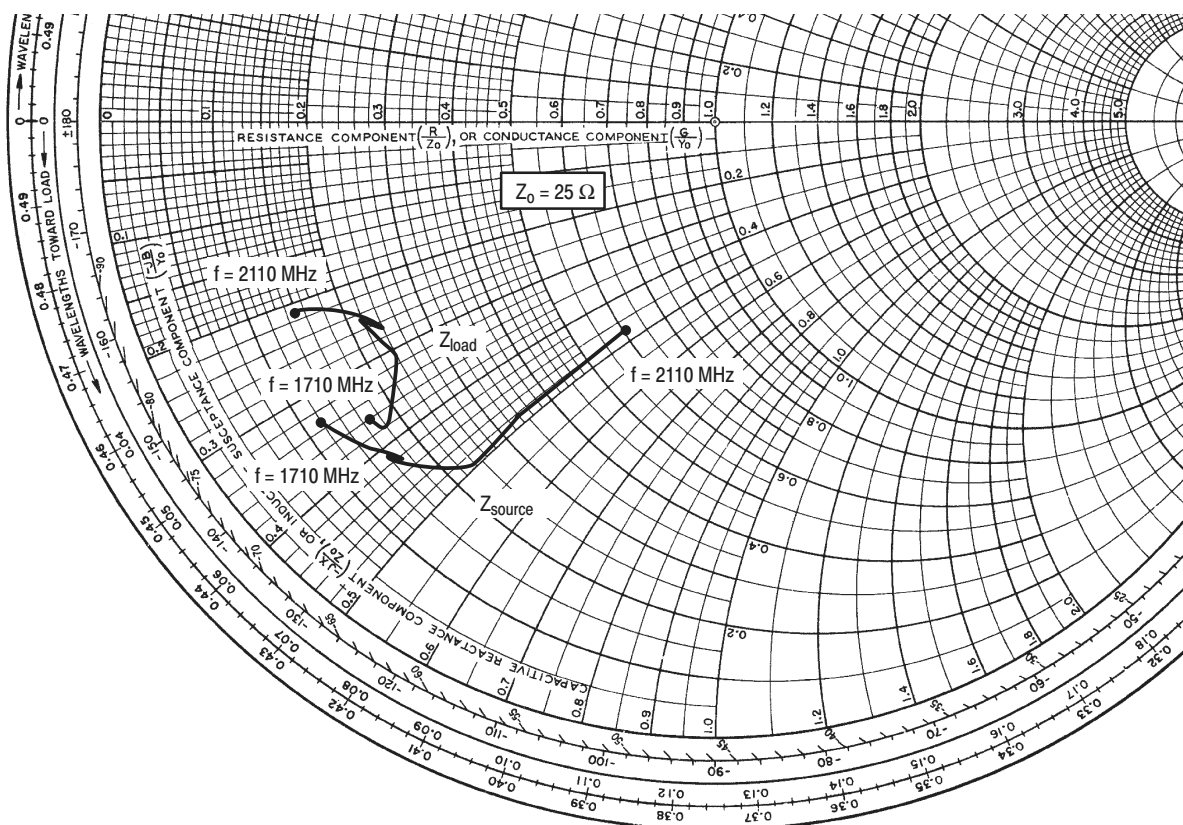


Figure 8. Power Gain and Efficiency versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 30 \text{ W (CW)}$

f MHz	Z_{source} Ω	Z_{load} Ω
1710	$2.92 - j8.24$	$4.18 - j9.06$
1785	$3.84 - j9.75$	$4.59 - j9.46$
1805	$4.15 - j10.38$	$4.98 - j9.06$
1840	$4.04 - j10.22$	$6.10 - j7.63$
1880	$6.12 - j12.29$	$5.83 - j6.89$
1960	$6.20 - j12.29$	$5.55 - j6.33$
1990	$8.61 - j12.10$	$5.93 - j6.66$
2110	$15.19 - j11.85$	$3.82 - j5.33$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

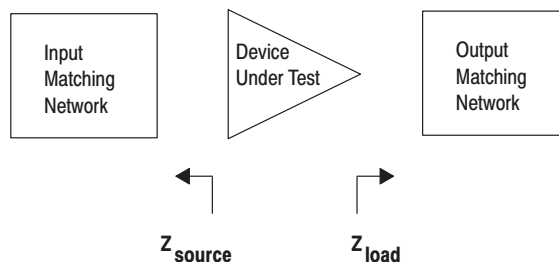


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

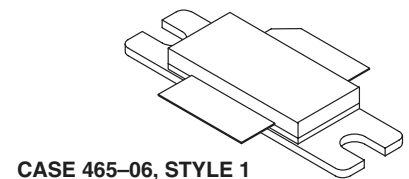
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications. Specified for GSM1805 – 1880 MHz.

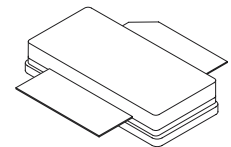
- Typical GSM Performance, Full Frequency Band (1805 – 1880 MHz)
Power Gain — 13 dB (Typ) @ 60 Watts
Efficiency — 45% (Typ) @ 60 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts CW Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

MRF18060A
MRF18060AR3
MRF18060ALSR3
MRF18060ASR3

1.80 – 1.88 GHz, 60 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF18060A



CASE 465A-06, STYLE 1
NI-780S
MRF18060ALSR3, MRF18060ASR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C \geq 25^\circ\text{C}$ Derate above 25°C	P_D	180 1.03	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	$^\circ\text{C/W}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 10 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 500 mAdc)	V _{GS(Q)}	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.27	—	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.7	—	S

DYNAMIC CHARACTERISTICS

Input Capacitance (Including Input Matching Capacitor in Package) (1) (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{iss}	—	160	—	pF
Output Capacitance (1) (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	740	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	2.7	—	pF

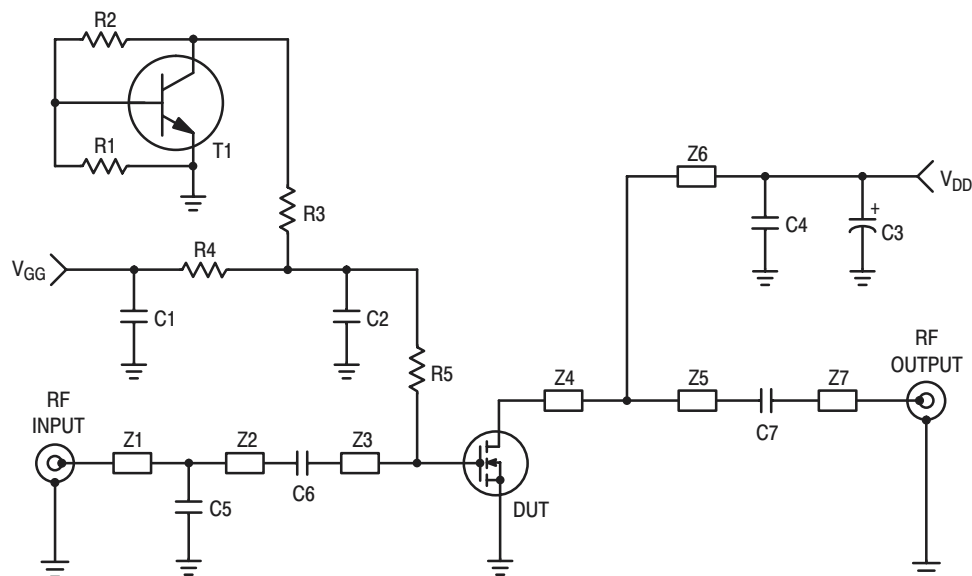
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Common–Source Amplifier Power Gain @ 60 W (2) (V _{DD} = 26 Vdc, I _{DQ} = 500 mA, f = 1805 – 1880 MHz)	G _{ps}	11.5	13	—	dB
Drain Efficiency @ 60 W (2) (V _{DD} = 26 Vdc, I _{DQ} = 500 mA, f = 1805 – 1880 MHz)	η	43	45	—	%
Input Return Loss (2) (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 500 mA, f = 1805 – 1880 MHz)	IRL	—	—	–10	dB
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 500 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.

Freescale Semiconductor, Inc.



C1	100 nF Chip Capacitor (1203)	Z1	0.47" x 0.09" Microstrip
C2, C4, C7	10 pF Chip Capacitors	Z2	1.16" x 0.09" Microstrip
C3	10 μ F, 35 V Electrolytic Tantalum Capacitor	Z3	0.57" x 0.95" Microstrip
C5	1.2 pF Chip Capacitor	Z4	0.59" x 1.18" Microstrip
C6	1.0 pF Chip Capacitor	Z5	1.26" x 0.15" Microstrip
R1, R3	2.2 k Ω Chip Resistors (0805)	Z6	1.15" x 0.09" Microstrip
R2, R4	2.7 k Ω Chip Resistors (0805)	Z7	0.37" x 0.09" Microstrip
R5	1.1 k Ω Chip Resistor (0805)		
T1	BC847 Transistor SOT-23		

Figure 1. 1805 – 1880 MHz Test Fixture Schematic

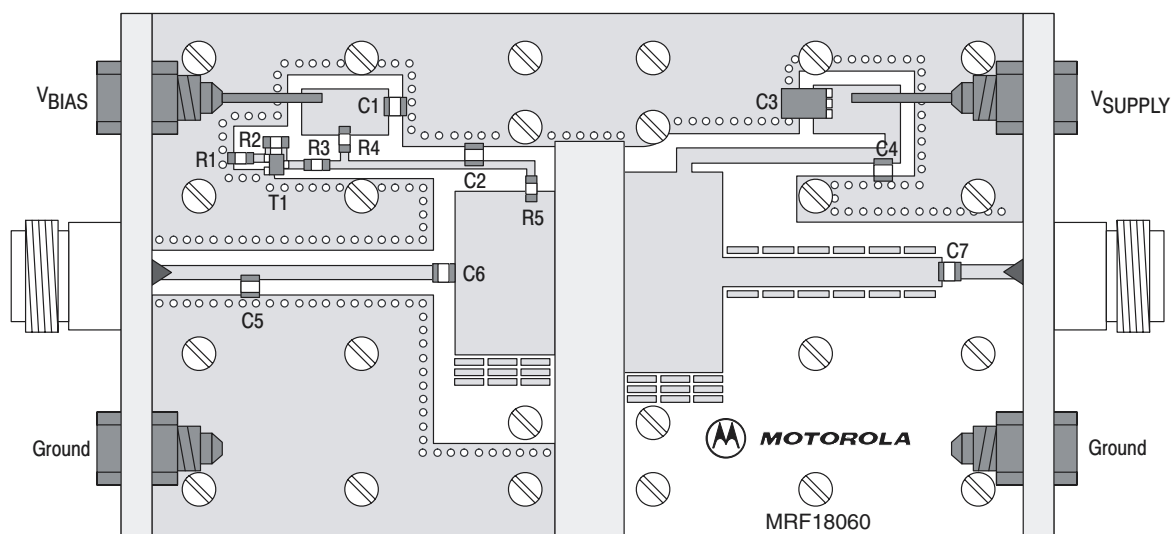


Figure 2. 1805 – 1880 MHz Test Fixture Component Layout

Freescale Semiconductor, Inc.

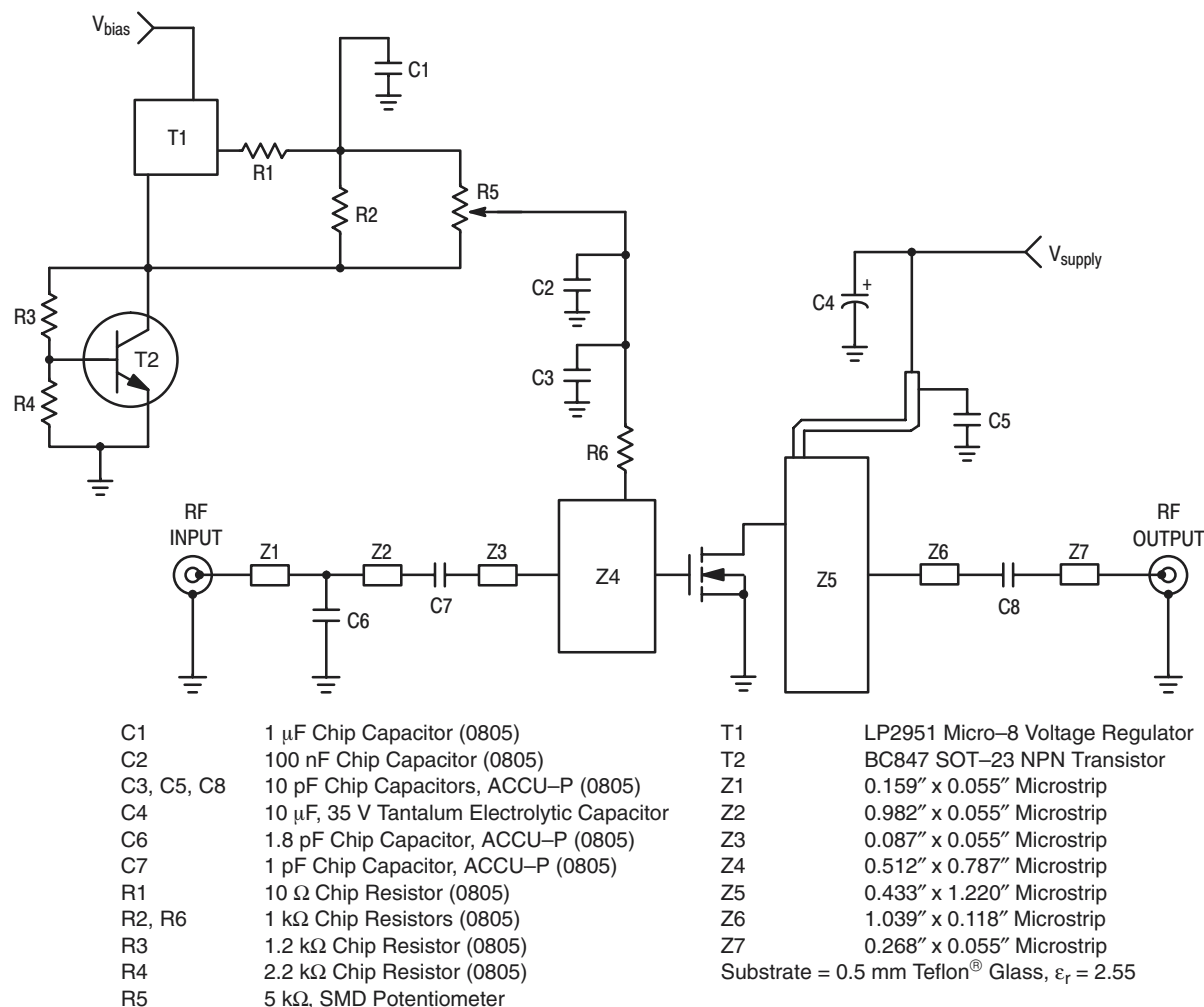


Figure 3. 1800 – 2000 MHz Demo Board Schematic

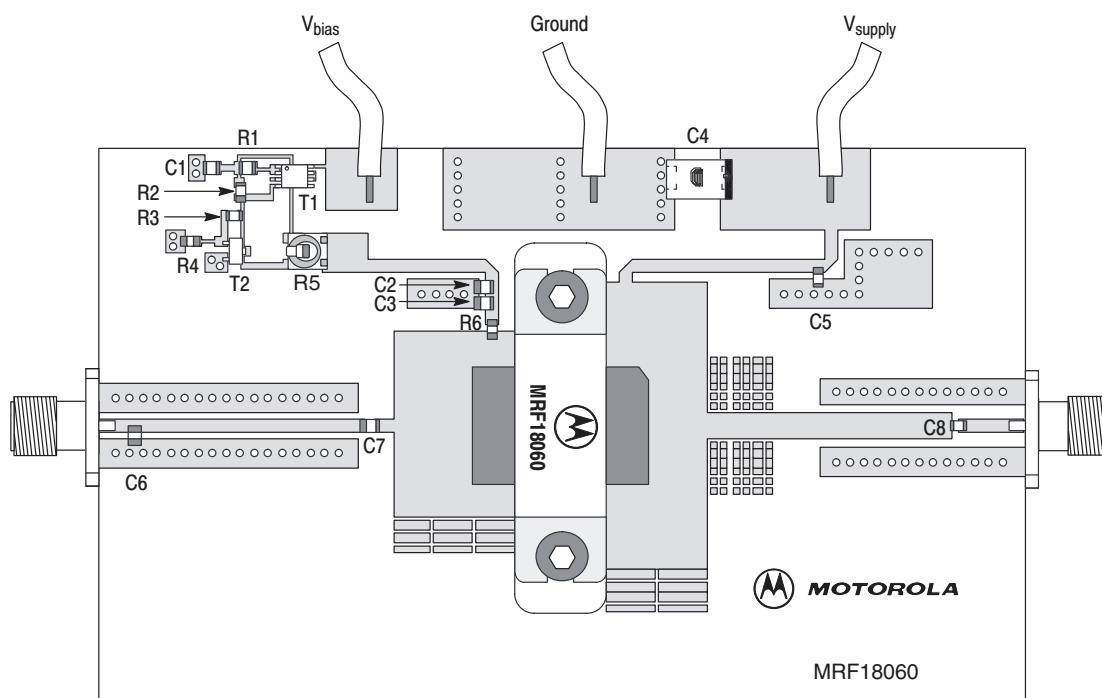


Figure 4. 1800 – 2000 MHz Demo Board Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)

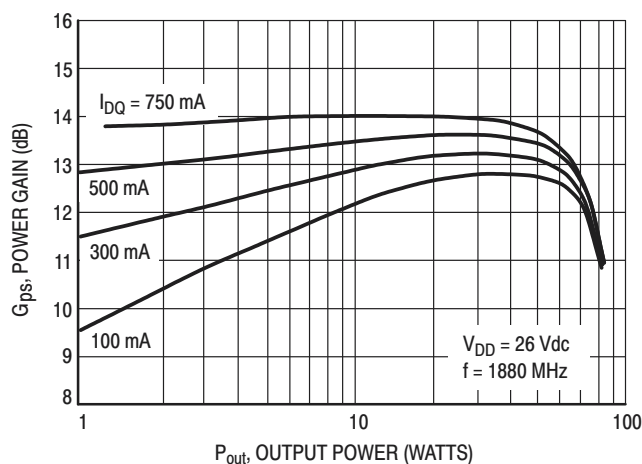


Figure 5. Power Gain versus Output Power

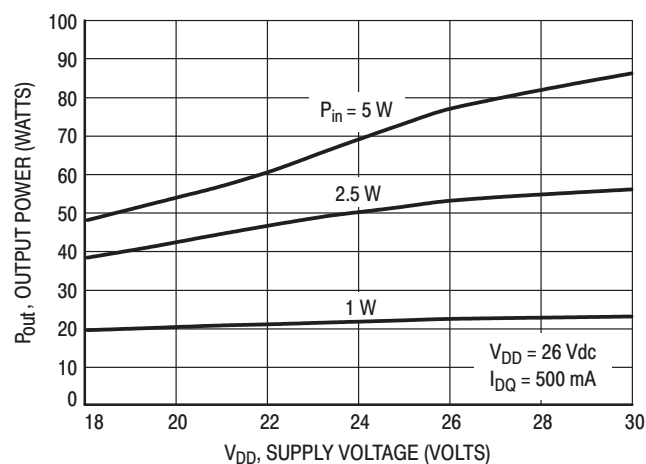


Figure 6. Output Power versus Supply Voltage

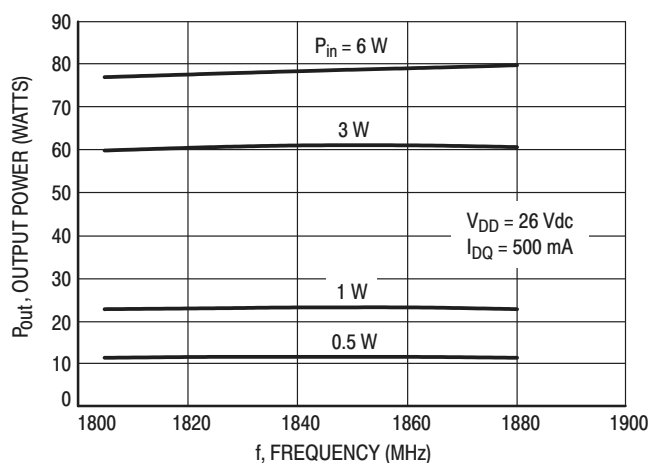


Figure 7. Output Power versus Frequency

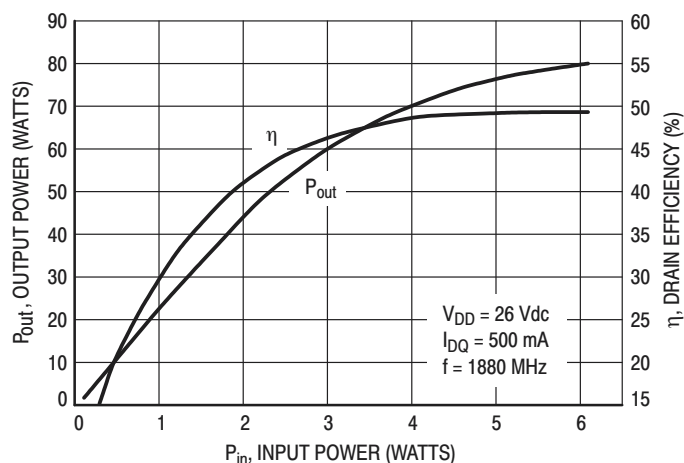


Figure 8. Output Power and Efficiency versus Input Power

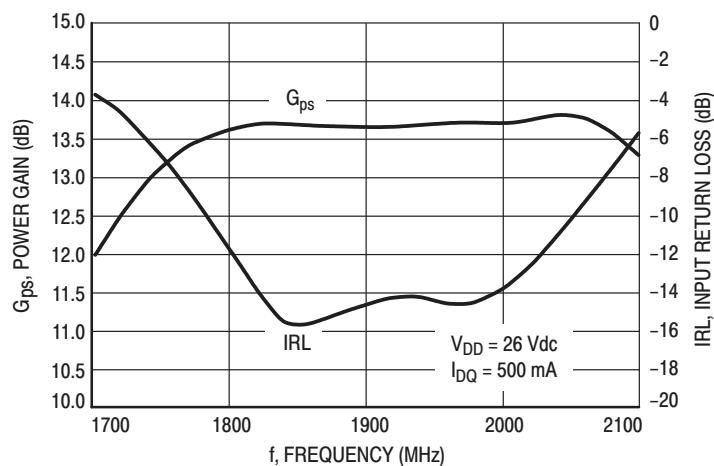
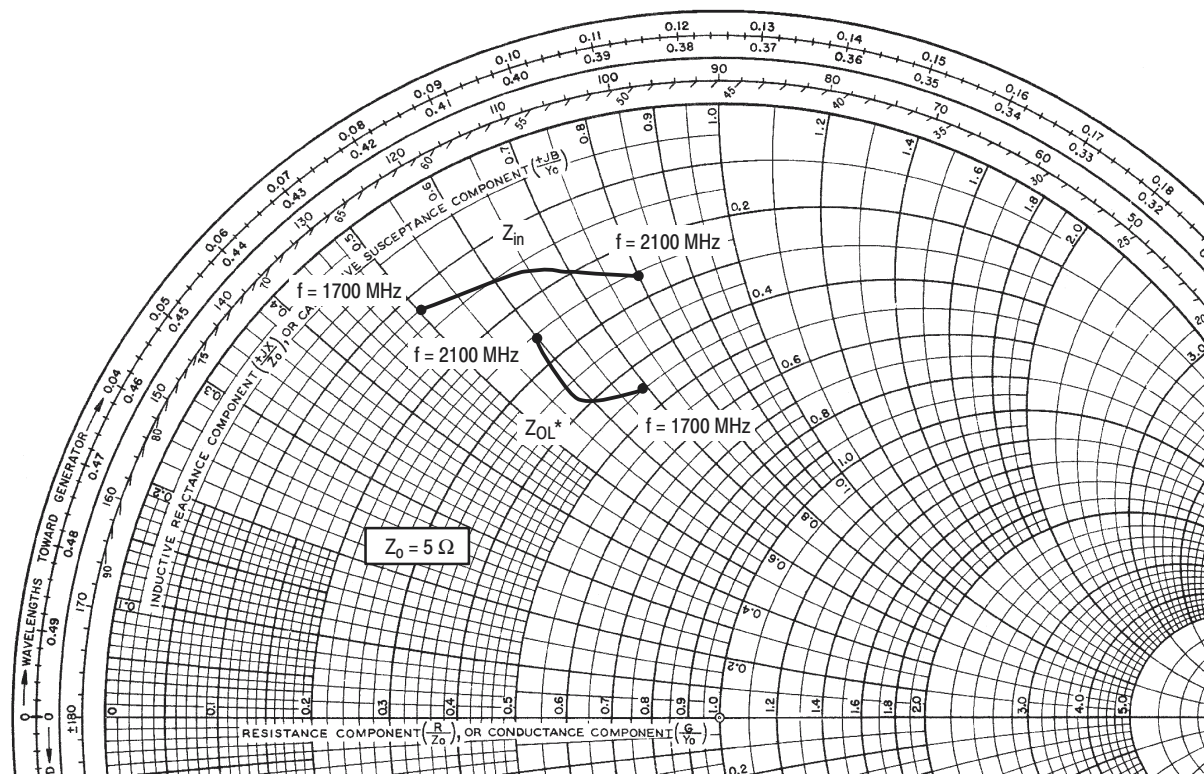


Figure 9. Wideband Gain and IRL (at Small Signal)



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 60 \text{ W CW}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1700	$0.60 + j2.53$	$2.27 + j3.44$
1800	$0.80 + j3.20$	$2.05 + j3.05$
1900	$0.92 + j3.42$	$1.90 + j2.90$
2000	$1.07 + j3.59$	$1.64 + j2.88$
2100	$1.31 + j4.00$	$1.29 + j2.99$

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}^* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, and drain efficiency.

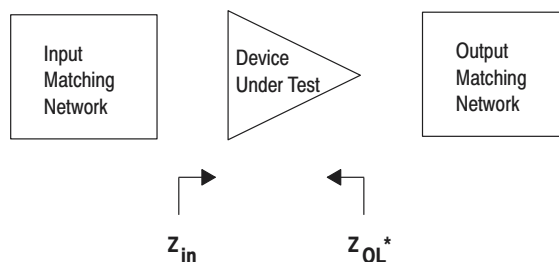


Figure 10. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

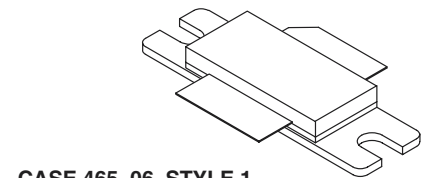
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications. Specified for GSM1930 – 1990 MHz.

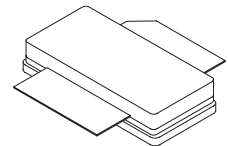
- GSM Performance, Full Frequency Band (1930 – 1990 MHz)
Power Gain — 13 dB (Typ) @ 60 Watts CW
Efficiency — 45% (Typ) @ 60 Watts CW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts CW Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

MRF18060B
MRF18060BR3
MRF18060BLSR3
MRF18060BSR3

1.90 – 1.99 GHz, 60 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF18060B



CASE 465A-06, STYLE 1
NI-780S
MRF18060BLSR3, MRF18060BSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C > 25^\circ\text{C}$ Derate above 25°C	P_D	180 1.03	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	$^\circ\text{C}/\text{W}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 10 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 500 mAdc)	V _{GS(Q)}	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.27	—	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.7	—	S

DYNAMIC CHARACTERISTICS

Input Capacitance (Including Input Matching Capacitor in Package) (1) (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{iss}	—	160	—	pF
Output Capacitance (1) (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	740	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	2.7	—	pF

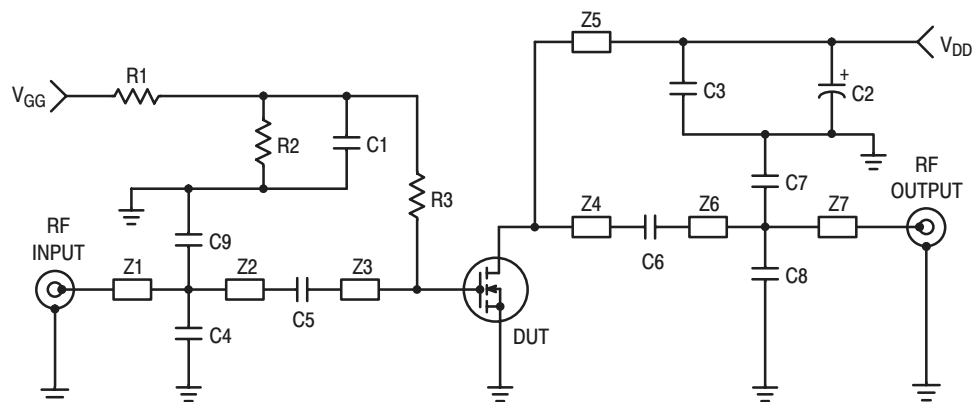
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Common–Source Amplifier Power Gain @ 60 W (2) (V _{DD} = 26 Vdc, I _{DQ} = 500 mA, f = 1930 – 1990 MHz)	G _{ps}	11.5	13	—	dB
Drain Efficiency @ 60 W (2) (V _{DD} = 26 Vdc, I _{DQ} = 500 mA, f = 1930 – 1990 MHz)	η	40	45	—	%
Input Return Loss (2) (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 500 mA, f = 1930 – 1990 MHz)	IRL	—	—	–10	dB
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 500 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1900 band, ensuring batch–to–batch consistency.

Freescale Semiconductor, Inc.



C1, C3	10 pF, 100B Chip Capacitors	Z1	0.60" x 0.09" Microstrip
C2	10 μ F, 35 V Electrolytic Tantalum Capacitor	Z2	1.00" x 0.09" Microstrip
C4, C8	1.2 pF, 100B Chip Capacitors	Z3	0.51" x 0.94" Microstrip
C5	1.0 pF, 100B Chip Capacitor	Z4	0.59" x 0.98" Microstrip
C6	2.2 pF, 100B Chip Capacitor	Z5	0.79" x 0.09" Microstrip
C7, C9	0.3 pF, 100B Chip Capacitors	Z6	1.38" x 0.09" Microstrip
R1, R2	10 k Ω Chip Resistors (0805)	Z7	0.79" x 0.09" Microstrip
R3	1.0 k Ω Chip Resistor (0805)	PCB	Teflon [®] Glass

Figure 1. 1930 – 1990 MHz Test Fixture Schematic

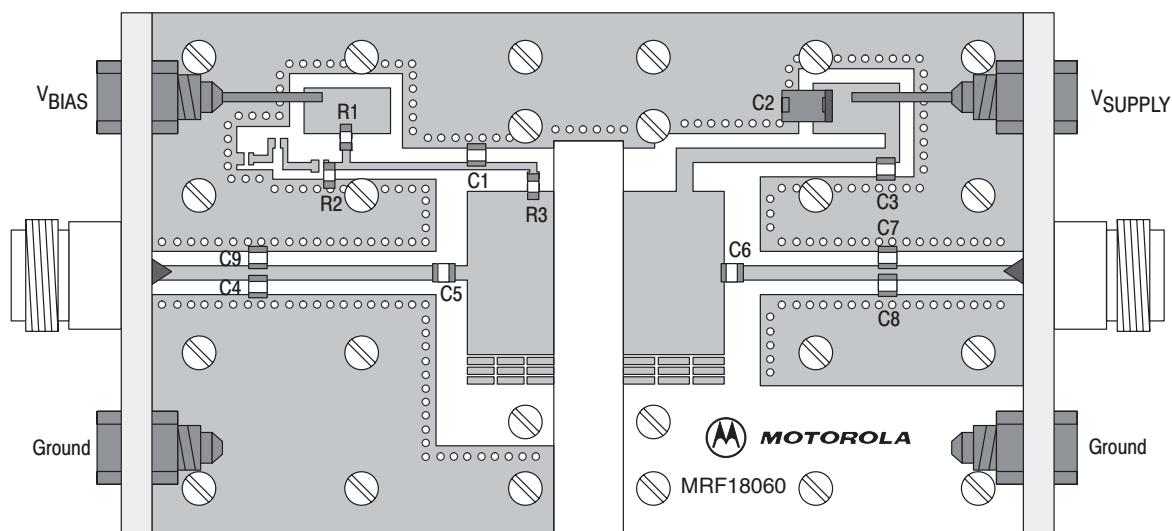


Figure 2. 1930 – 1990 MHz Test Fixture Component Layout

Freescale Semiconductor, Inc.

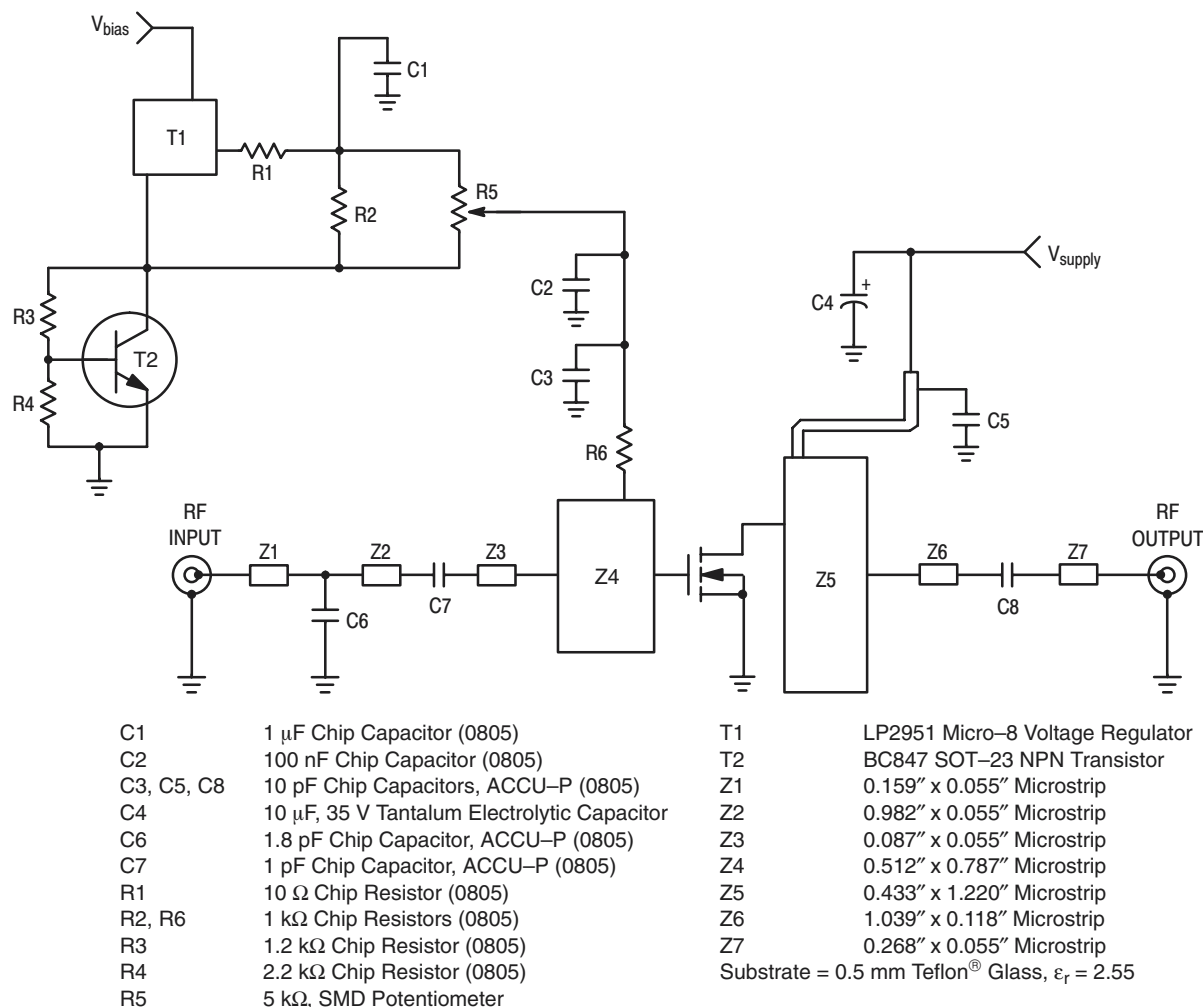


Figure 3. 1800 – 2000 MHz Demo Board Schematic

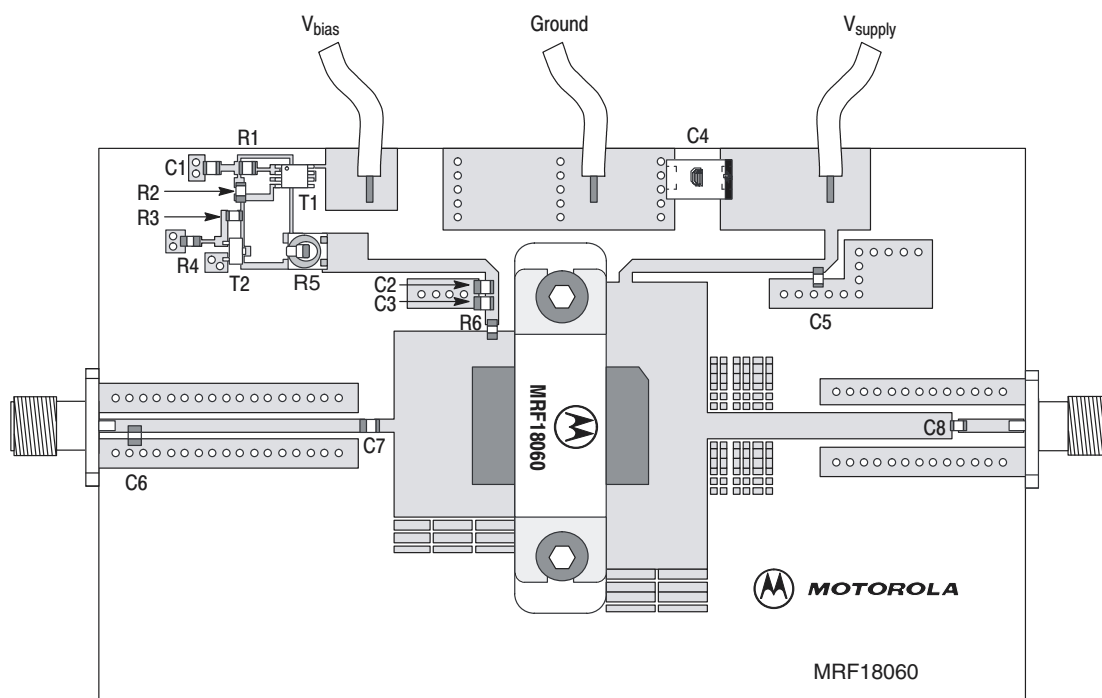


Figure 4. 1800 – 2000 MHz Demo Board Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)

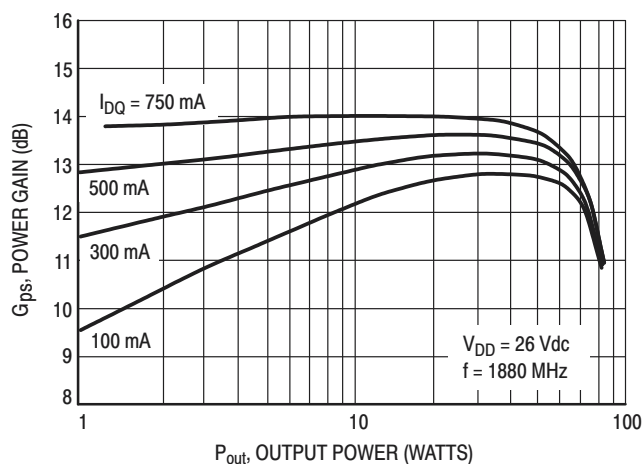


Figure 5. Power Gain versus Output Power

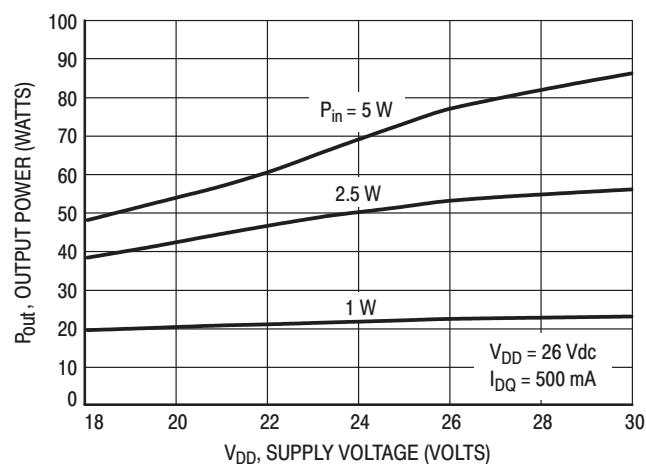


Figure 6. Output Power versus Supply Voltage

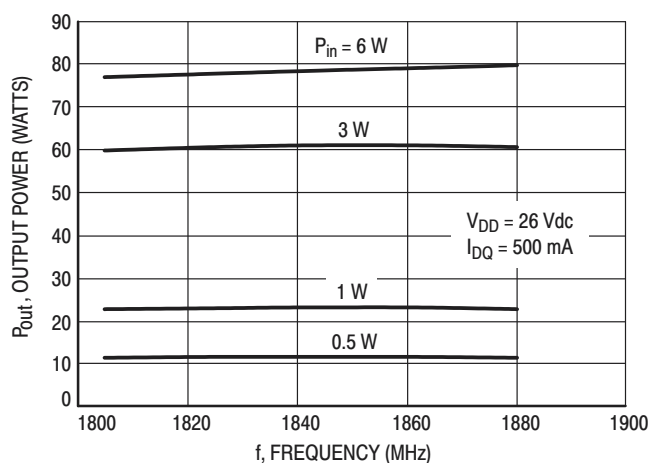


Figure 7. Output Power versus Frequency

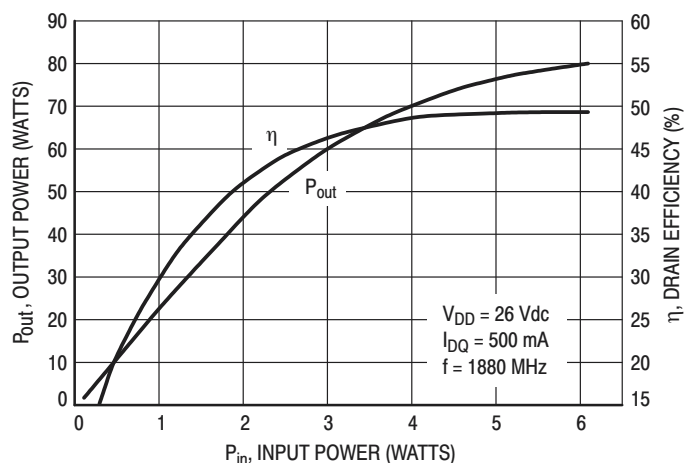


Figure 8. Output Power and Efficiency versus Input Power

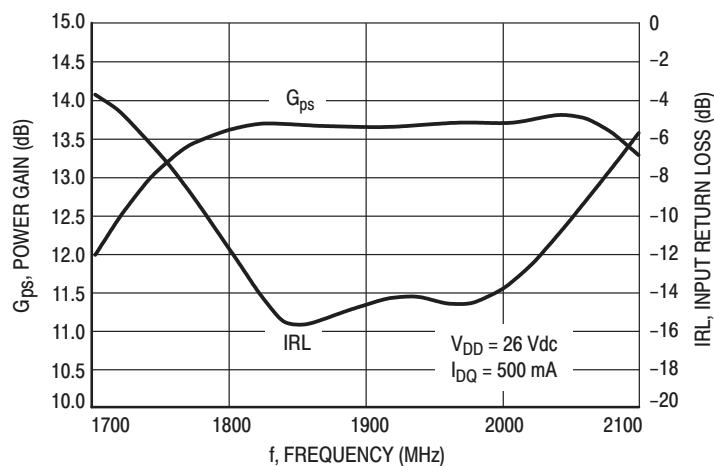
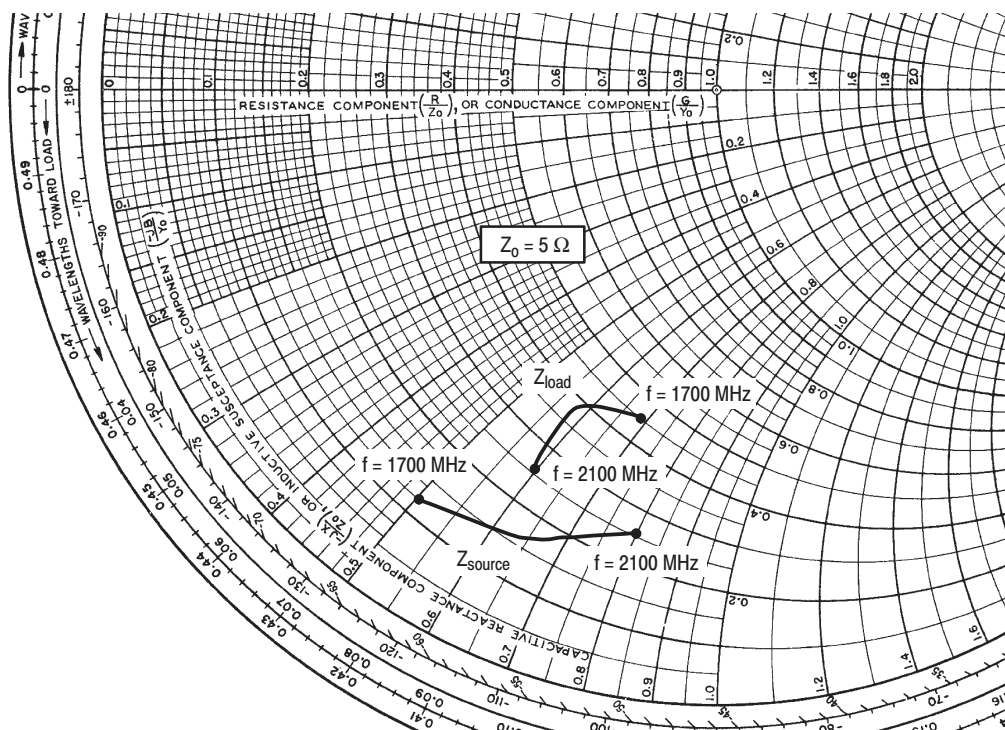


Figure 9. Wideband Gain and IRL (at Small Signal)



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 60 \text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
1700	$0.60 - j2.53$	$2.27 - j3.44$
1800	$0.80 - j3.20$	$2.05 - j3.05$
1900	$0.92 - j3.42$	$1.90 - j2.90$
2000	$1.07 - j3.59$	$1.64 - j2.88$
2100	$1.31 - j4.00$	$1.29 - j2.99$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

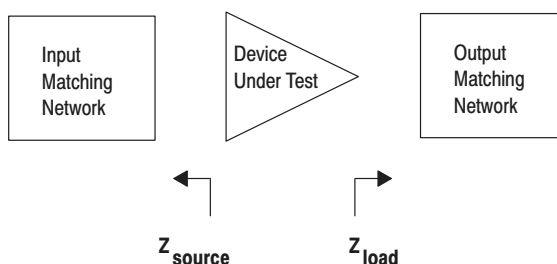


Figure 10. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

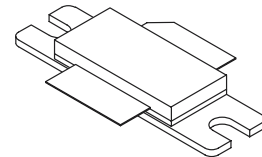
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and GSM EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications. Specified for GSM-GSM EDGE 1805 – 1880 MHz.

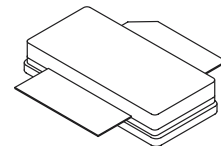
- GSM and GSM EDGE Performance, Full Frequency Band (1805–1880 MHz)
Power Gain – 15 dB (Typ) @ 85 Watts CW
Efficiency – 52% (Typ) @ 85 Watts CW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, @ P1dB Output Power, @ f = 1805 MHz
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

MRF18085A
MRF18085AR3
MRF18085ALSR3

GSM/GSM EDGE
1.8 – 1.88 GHz, 85 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF18085A, MRF18085AR3



CASE 465A-06, STYLE 1
NI-780S
MRF18085ALSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	273 1.56	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.79	$^\circ\text{C}/\text{W}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Typical)
Machine Model	M3 (Typical)

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

For More Information On This Product,
Go to: www.freescale.com

MRF18085A MRF18085AR3 MRF18085ALSR3

5-285

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 µAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	µAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	µAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 µAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 600 mAdc)	V _{GS(Q)}	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.15	—	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	6.0	—	S

DYNAMIC CHARACTERISTICS

Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	3.6	—	pF
--	------------------	---	-----	---	----

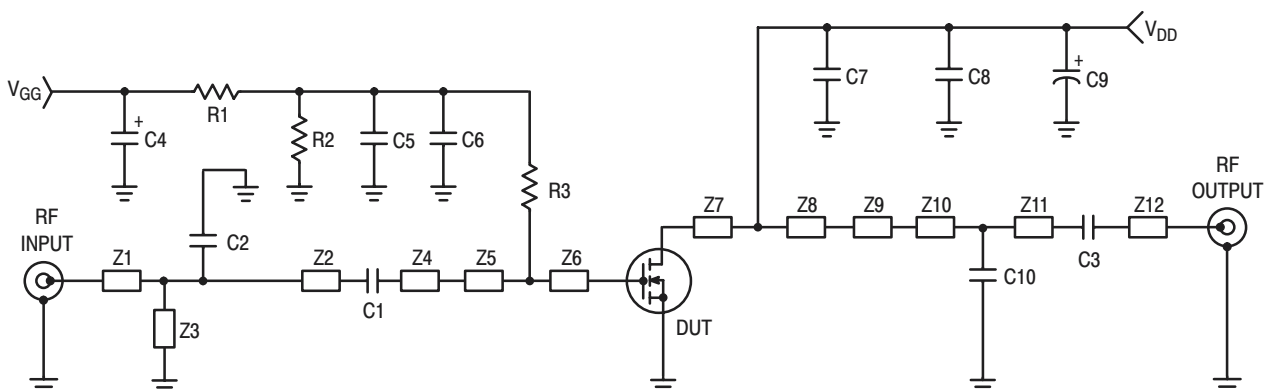
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Common–Source Amplifier Power Gain @ 85 W (2) (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 1805 – 1880 MHz)	G _{ps}	13.5	15	—	dB
Drain Efficiency @ 85 W (2) (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 1805 – 1880 MHz)	η	48	52	—	%
Input Return Loss @ 85 W (2) (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 1805 – 1880 MHz)	IRL	—	–12	–9	dB
P _{out} , 1 dB Compression Point (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 1805 – 1880 MHz)	P1dB	83	90	—	Watts
Output Mismatch Stress @ P1dB (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 1805 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.

Freescale Semiconductor, Inc.



C1, C3, C6, C7	10 pF Chip Capacitors, B Case, ATC	Z4	0.610" x 0.118" Microstrip
C2	1.8 pF Chip Capacitor, B Case, ATC	Z5	0.331" x 1.153" Microstrip
C4	10 μ F, 35 V Tantalum Capacitor, AVX	Z6	0.063" x 1.153" Microstrip
C5, C8	1 nF Chip Capacitors, B Case, ATC	Z7	0.122" x 0.925" Microstrip
C9	220 μ F, 63 V Electrolytic Capacitor, Radial, Philips	Z8	0.547" x 0.925" Microstrip
C10	0.3 pF Chip Capacitor, B Case, ATC	Z9	0.394" x 0.177" Microstrip
R1, R2	10 k Ω , 1/4 W Chip Resistors (1206)	Z10	0.180" x 0.087" Microstrip
R3	1.0 k Ω , 1/4 W Chip Resistor (1206)	Z11	0.686" x 0.087" Microstrip
Z1	0.671" x 0.087" Microstrip	Z12	0.294" x 0.087" Microstrip
Z2	0.568" x 0.087" Microstrip	PCB	Taconic TLX8, 30 mils, $\epsilon_r = 2.55$
Z3	0.500" x 0.098" Microstrip Shorted Stub		

Figure 1. 1.80 – 1.88 GHz Test Fixture Schematic

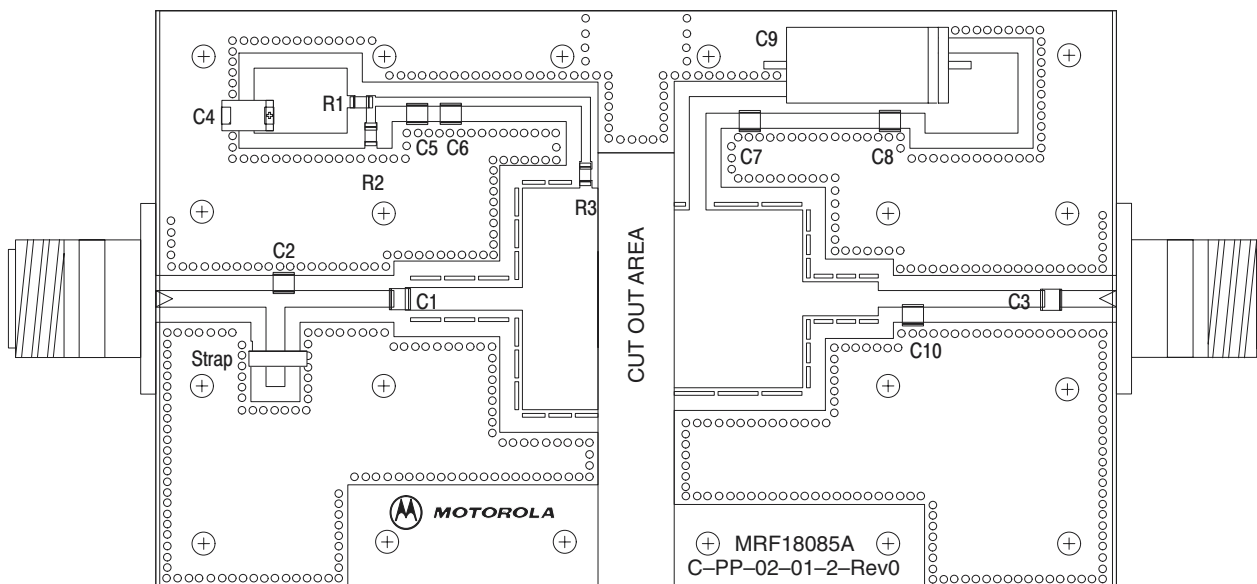


Figure 2. 1.80 – 1.88 GHz Test Fixture Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

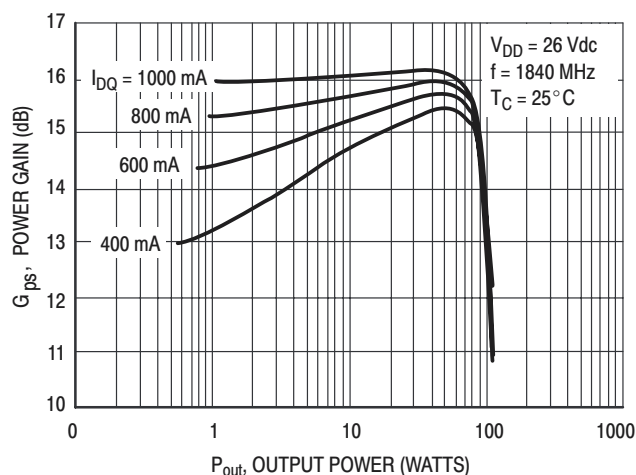


Figure 3. Power Gain versus Output Power

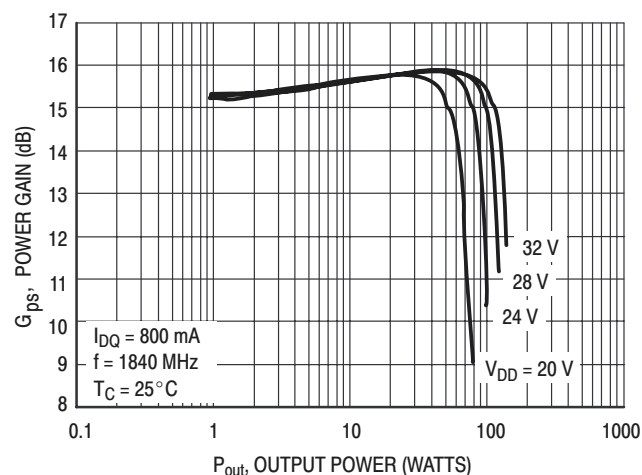


Figure 4. Power Gain versus Output Power

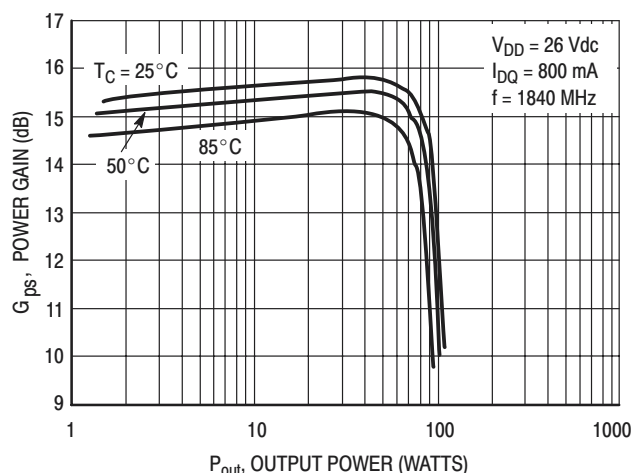


Figure 5. Power Gain versus Output Power

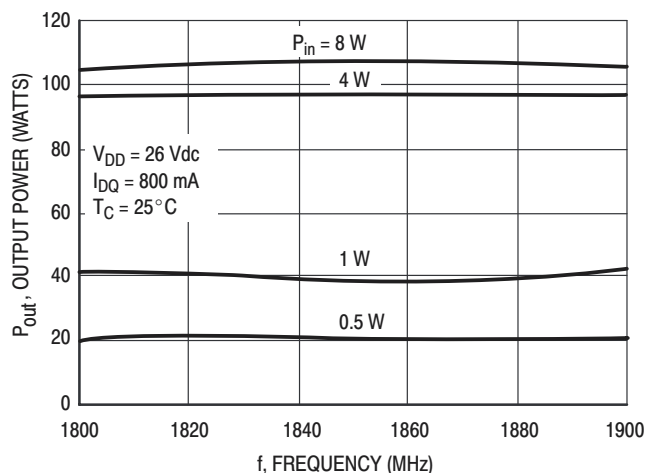


Figure 6. Output Power versus Frequency

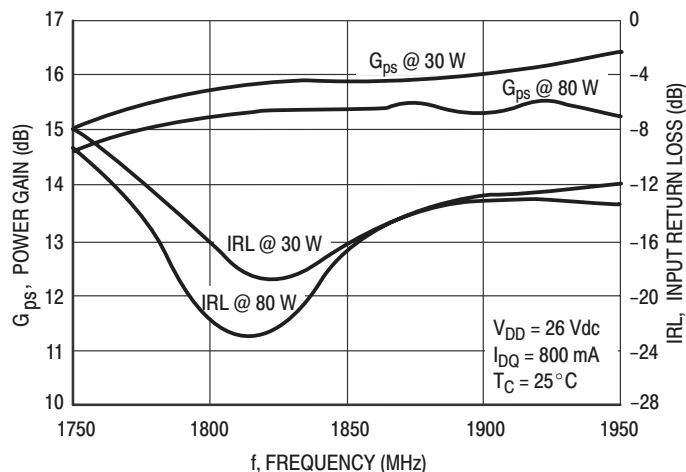


Figure 7. Power Gain versus Frequency

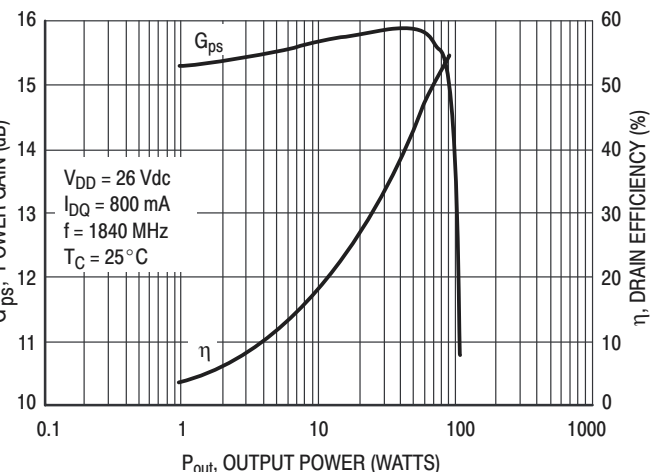
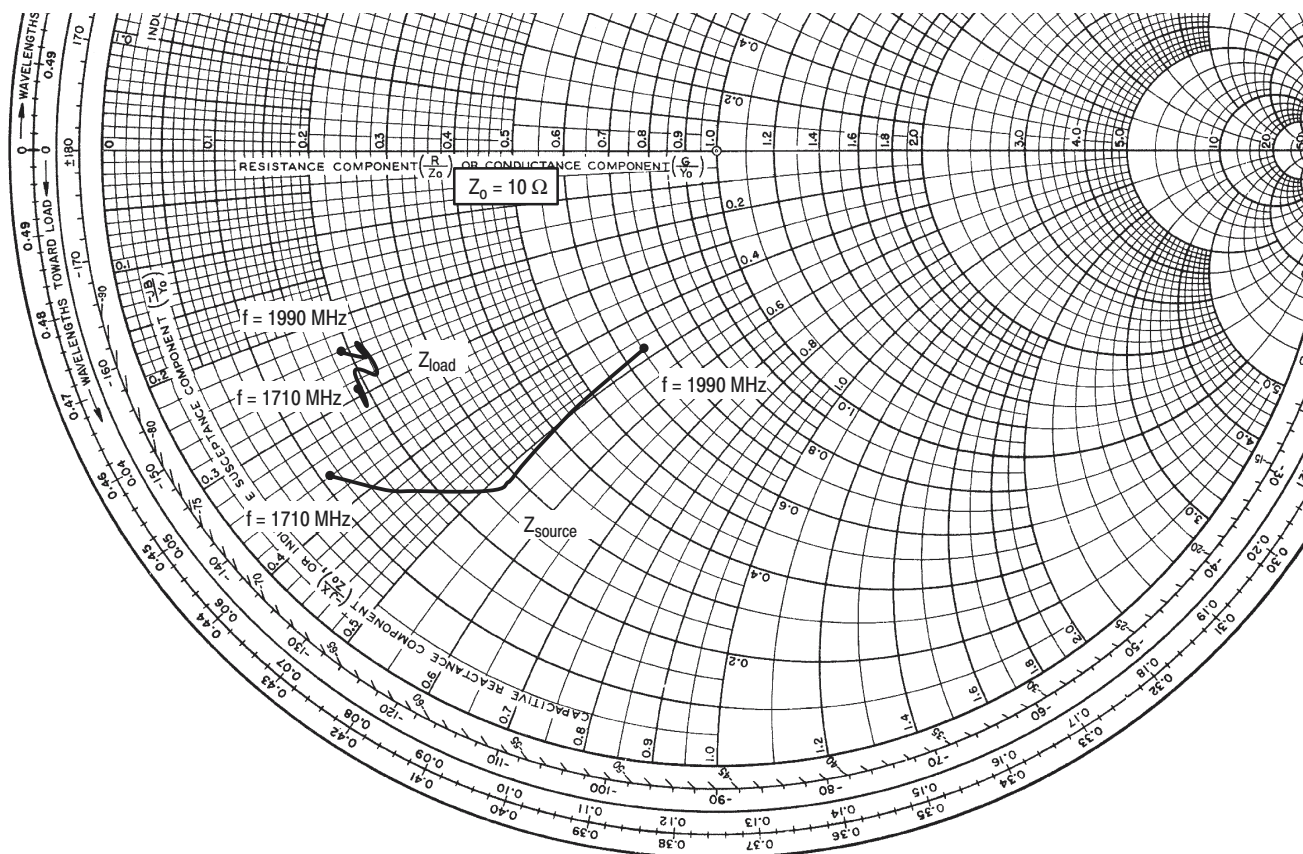


Figure 8. Power Gain and Efficiency versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 800 \text{ mA}$, $P_{out} = 85 \text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
1710	$1.13 - j3.62$	$1.79 - j2.88$
1785	$1.61 - j4.23$	$1.82 - j3.15$
1805	$1.69 - j4.34$	$1.90 - j2.66$
1880	$2.83 - j5.25$	$2.09 - j2.77$
1930	$3.00 - j5.18$	$2.01 - j2.44$
1960	$4.39 - j4.97$	$2.01 - j2.57$
1990	$6.59 - j4.74$	$1.79 - j2.37$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

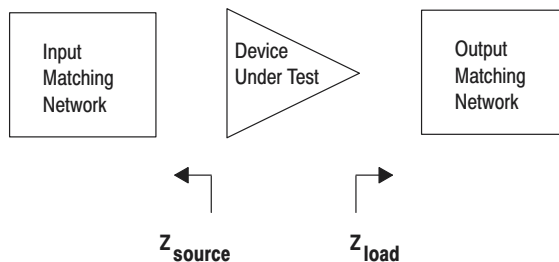


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

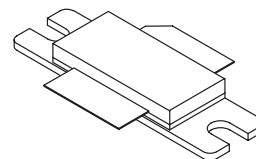
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and GSM EDGE base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA, and multicarrier amplifier applications.

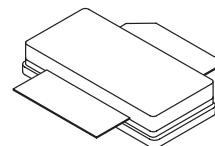
- GSM and GSM EDGE Performance, Full Frequency Band (1930 – 1990 MHz)
Power Gain – 12.5 dB (Typ) @ 85 Watts CW
Efficiency – 50% (Typ) @ 85 Watts CW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency, and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, @ P1dB Output Power, @ $f = 1930$ MHz
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40 μ m Nominal.

MRF18085B
MRF18085BR3
MRF18085BLSR3

GSM/GSM EDGE
1.9 – 1.99 GHz, 85 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF18085B, MRF18085BR3



CASE 465A-06, STYLE 1
NI-780S
MRF18085BLSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	273 1.56	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.79	$^\circ\text{C/W}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 2

MRF18085B MRF18085BR3 MRF18085BLSR3
 5-290

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 600 mAdc)	V _{GS(Q)}	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.18	0.21	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	6.0	—	S

DYNAMIC CHARACTERISTICS

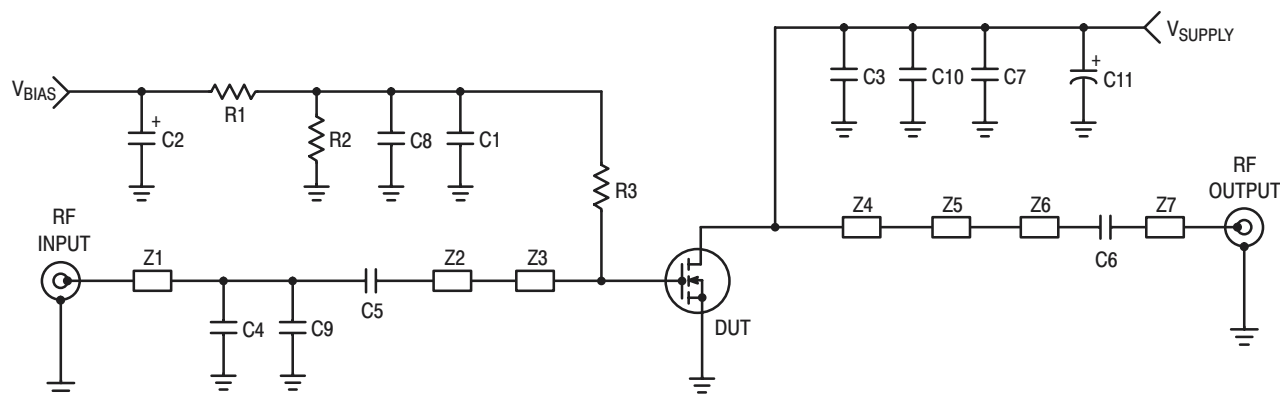
Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	3.6	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Common–Source Amplifier Power Gain @ 85 W (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 1930 – 1990 MHz)	G _{ps}	11.5	12.5	—	dB
Drain Efficiency @ 85 W (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 1930 – 1990 MHz)	η	46	50	—	%
Input Return Loss @ 85 W (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 1930 – 1990 MHz)	IRL	—	–12	–9	dB
P1 dB Output Power (V _{DD} = 26 Vdc, I _{DQ} = 800 mA, f = 1930 – 1990 MHz)	P1dB	80	90	—	Watts
Output Mismatch Stress @ P1dB (V _{DD} = 26 Vdc, I _{DQ} = 600 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.



C1, C10	1.0 nF Chip Capacitors, B Case, ATC	Z1	1.654" x 0.082" Microstrip
C2	10 μ F, 35 V Tantalum Capacitor	Z2	0.207" x 0.082" Microstrip
C3, C6	10 pF Chip Capacitors, B Case, ATC	Z3	0.362" x 1.260" Microstrip
C4	3.3 pF Chip Capacitor, B Case, ATC	Z4	0.583" x 0.669" Microstrip
C5	4.7 pF Chip Capacitor, B Case, ATC	Z5	0.449" x 0.179" Microstrip
C7, C8	100 nF Chip Capacitors, ACCU-P (1206)	Z6	0.877" x 0.082" Microstrip
C9	3.9 pF Chip Capacitor, B Case, ATC	Z7	0.326" x 0.082" Microstrip
C11	470 μ F, 63 V Electrolytic Capacitor	PCB	0.030" Glass Teflon [®] ($\epsilon_r = 2.55$)
R1, R2	1.0 k Ω Chip Resistors (0805)		
R3	2 x 18 k Ω Chip Resistor (1206)		

Figure 1. 1.93 – 1.99 GHz Test Fixture Schematic

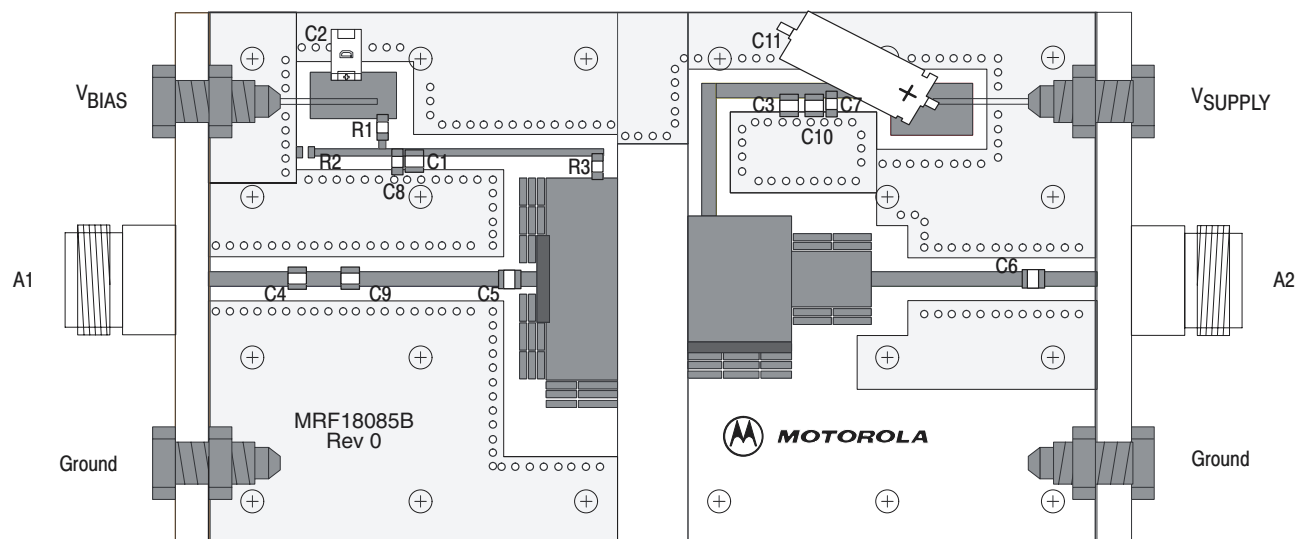


Figure 2. 1.93 – 1.99 GHz Test Fixture Component Layout

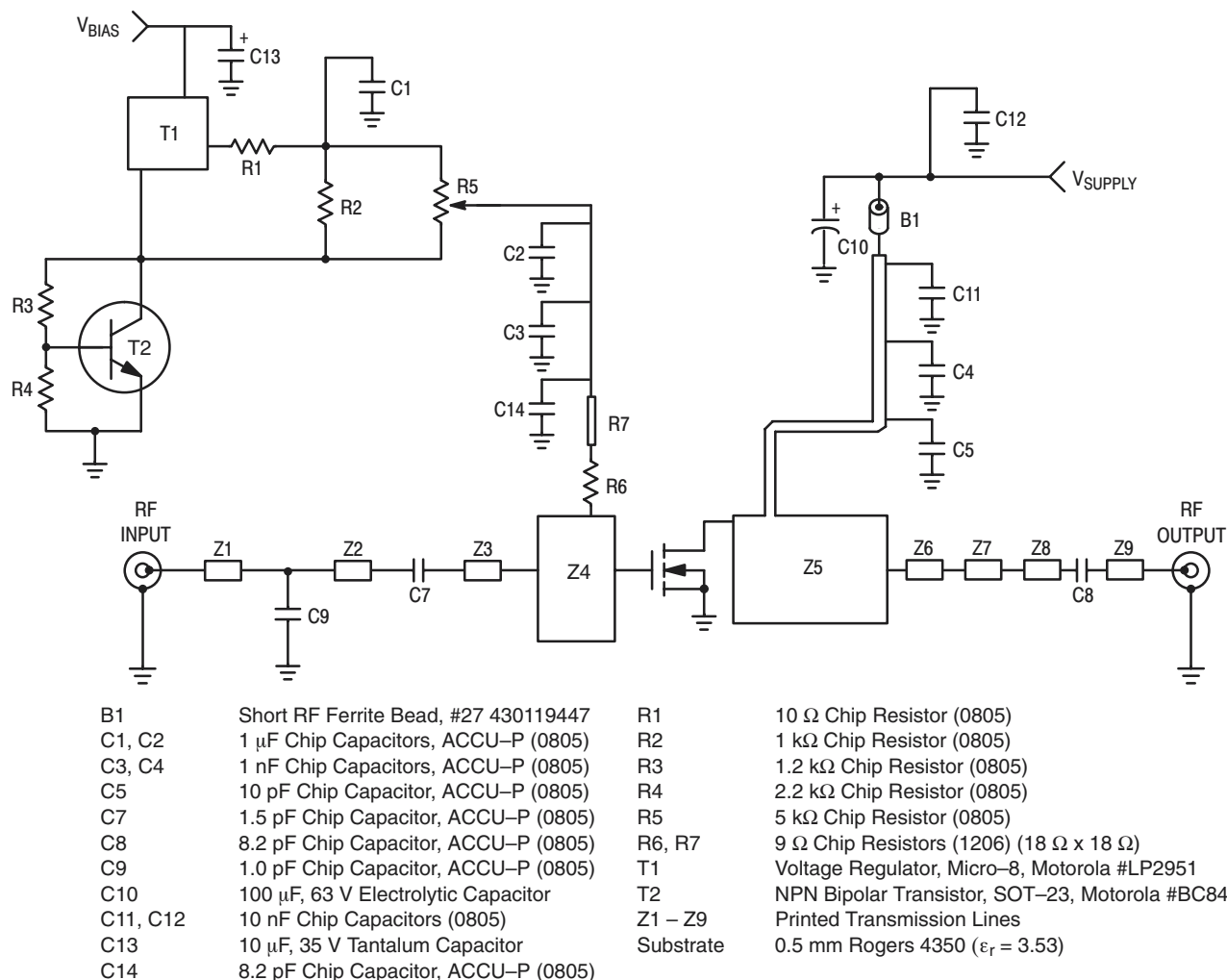


Figure 3. 1.93 – 1.99 GHz GSM EDGE Optimized Demo Board Schematic

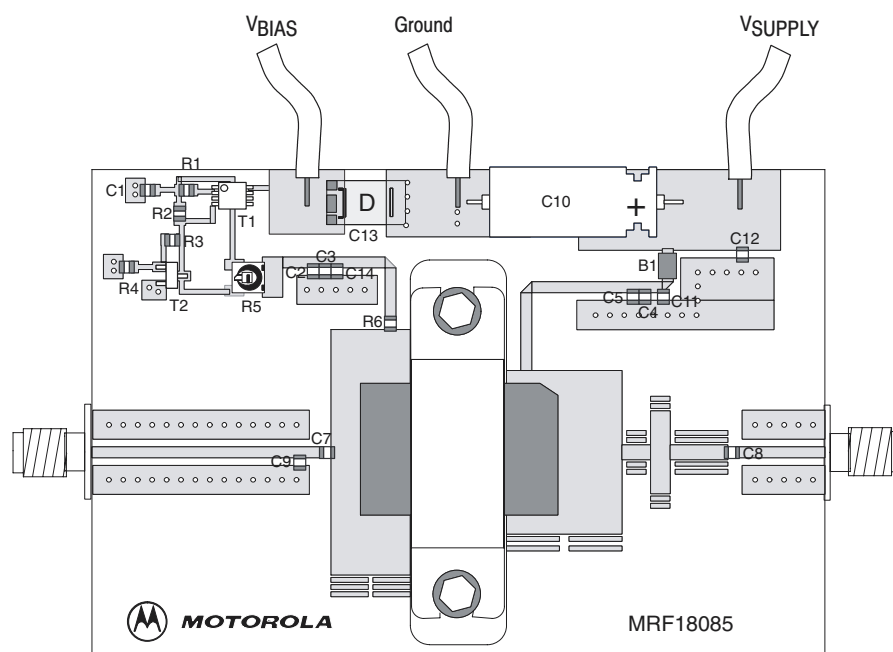


Figure 4. 1.93 – 1.99 GHz GSM EDGE Optimized Demo Board Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS (Performed on a GSM EDGE Optimized Demo Board)

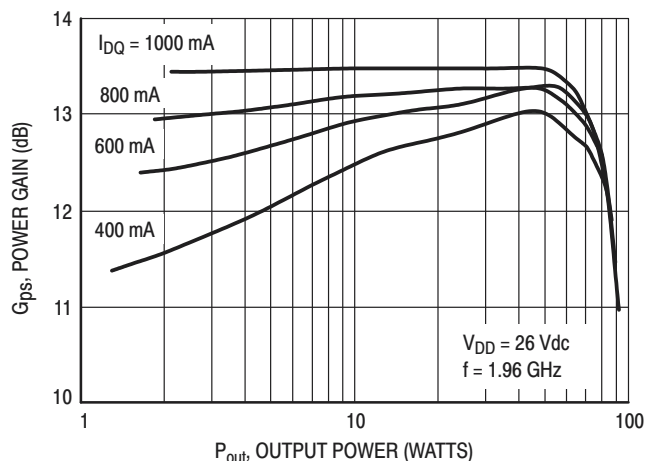


Figure 5. Power Gain versus Output Power

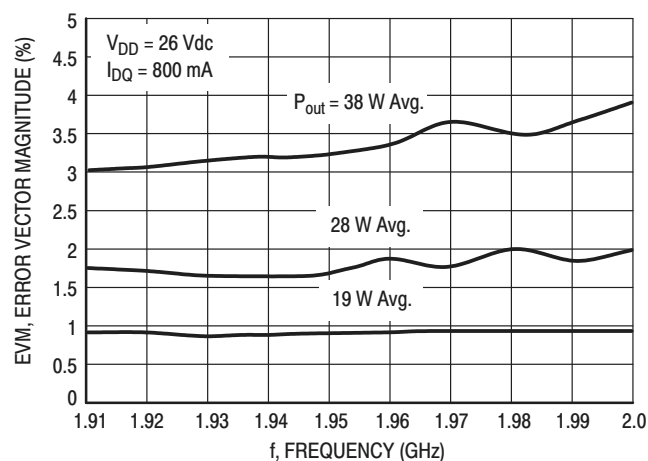


Figure 6. Error Vector Magnitude versus Frequency

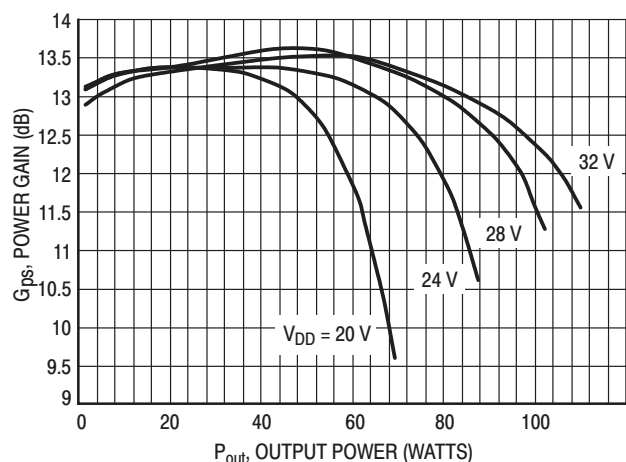


Figure 7. Power Gain versus Output Power

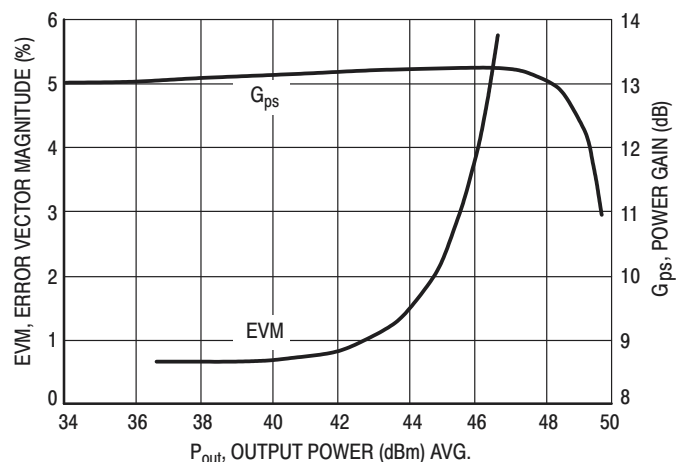


Figure 8. EVM and Gain versus Output Power

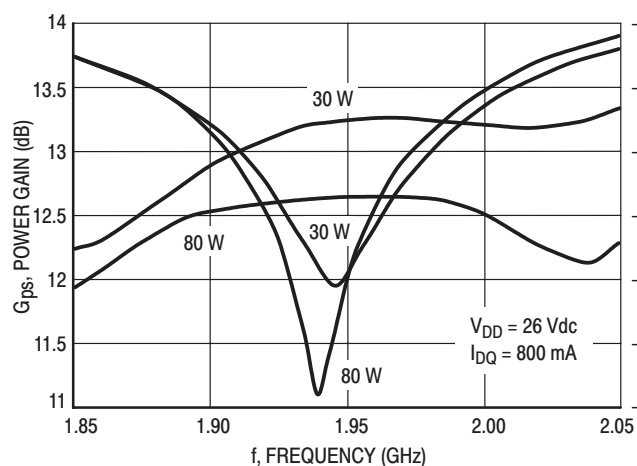


Figure 9. Power Gain and IRL
versus Frequency

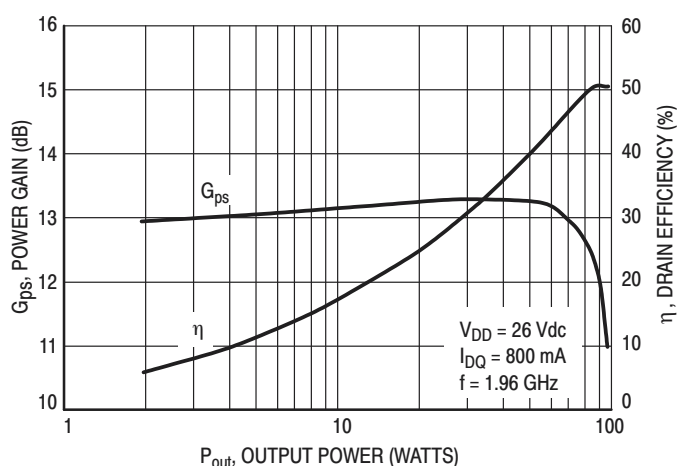


Figure 10. Power Gain and Efficiency
versus Output Power

Freescal Semiconductor, Inc.

TYPICAL CHARACTERISTICS
(Performed on a GSM EDGE Optimized Demo Board)

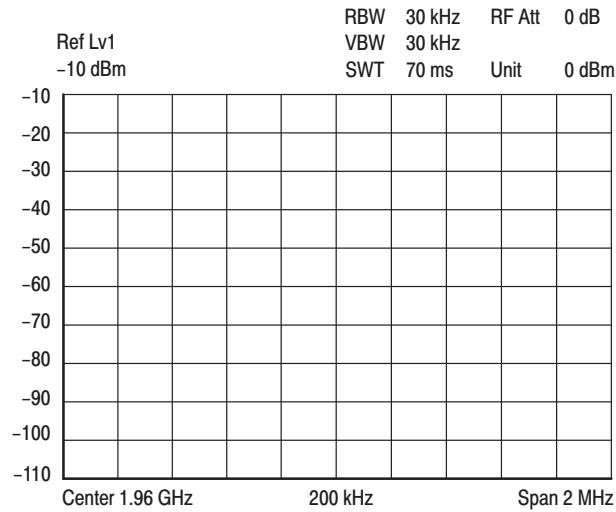
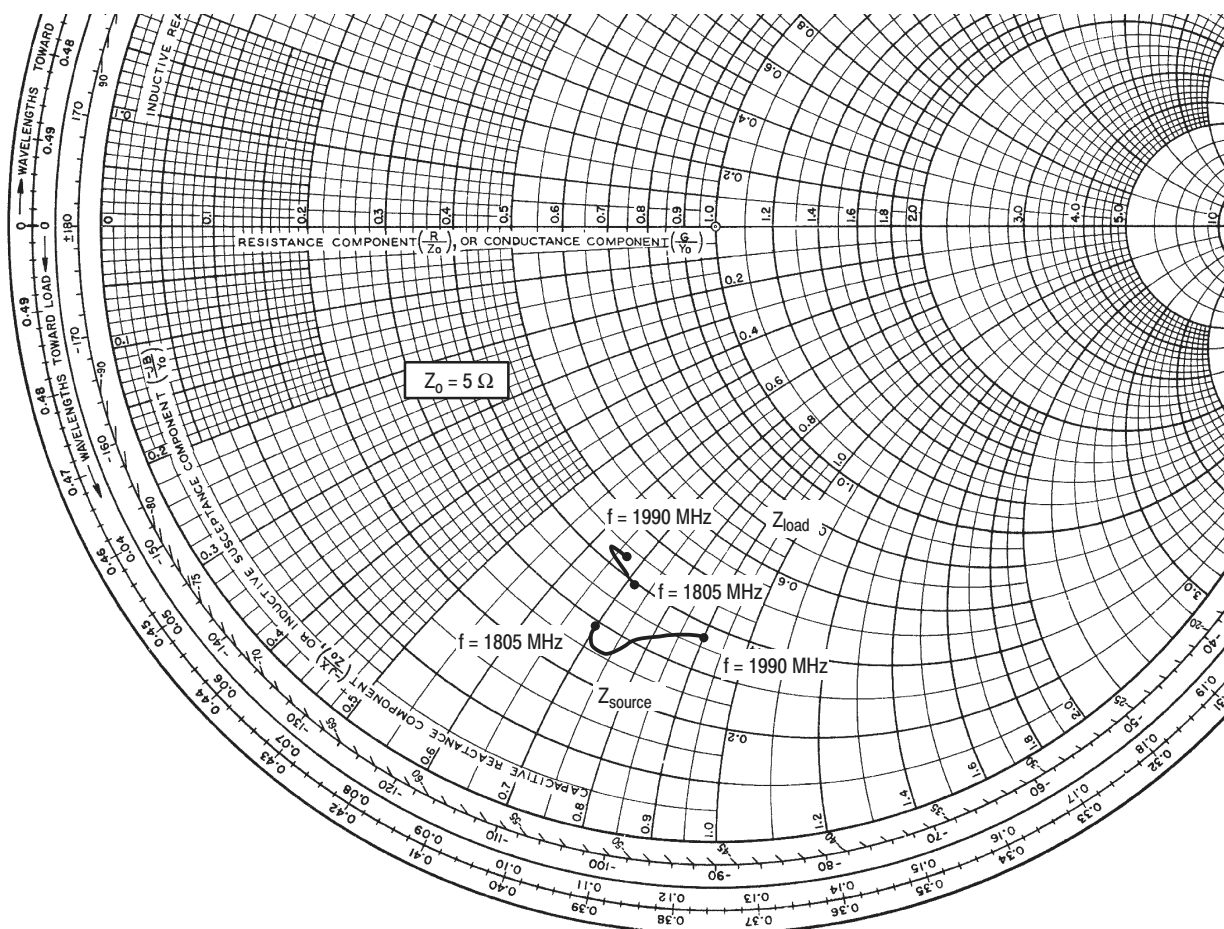


Figure 11. EDGE Spectrum at 40 Watts (Avg.) Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 800 \text{ mA}$, $P_{out} = 85 \text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
1805	$1.43 - j3.74$	$2 - j3.60$
1880	$1.27 - j3.95$	$1.98 - j3.57$
1930	$1.5 - j4.13$	$2.13 - j3.16$
1990	$1.86 - j4.76$	$2.17 - j3.36$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

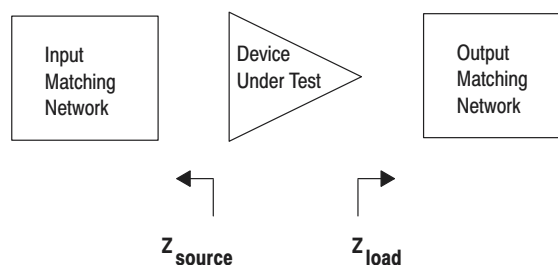


Figure 12. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

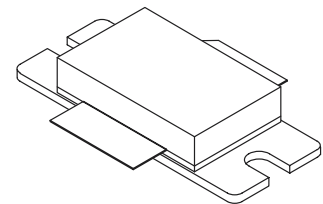
Designed for GSM and GSM EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for GSM and GSM EDGE cellular radio applications.

- GSM and GSM EDGE Performances, Full Frequency Band
Power Gain — 13.5 dB (Typ) @ 90 Watts CW
Efficiency — 52% (Typ) @ 90 Watts CW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

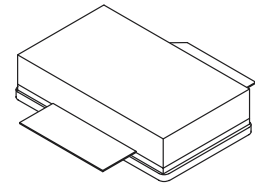
MRF18090A

MRF18090AS

1.80 – 1.88 GHz, 90 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETS



CASE 465B-03, STYLE 1
NI-880
MRF18090A



CASE 465C-02, STYLE 1
NI-880S
MRF18090AS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 4

MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

For More Information On This Product,
Go to: www.freescale.com

MRF18090A MRF18090AS
5-297

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 750 mAdc)	V _{GS(Q)}	2.5	3.7	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.1	—	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 Adc)	g _{fs}	—	7.2	—	S

DYNAMIC CHARACTERISTICS

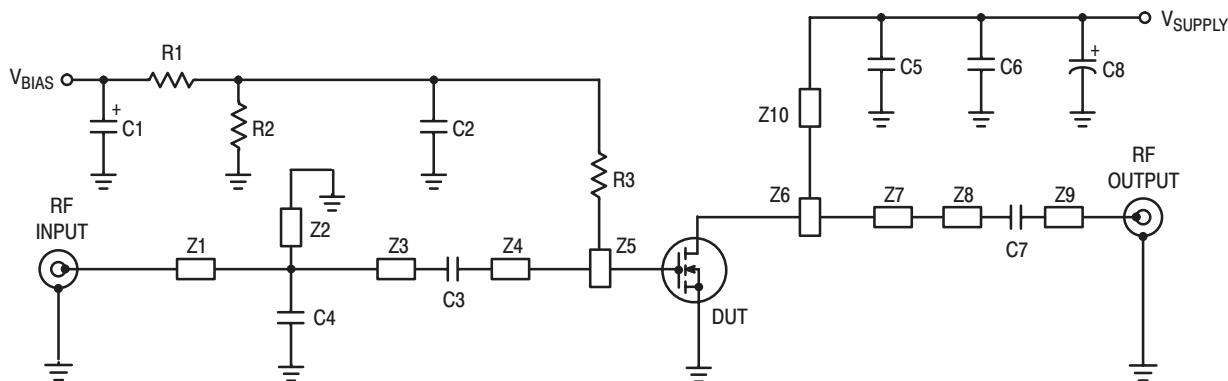
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	4.2	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain @ 90 W (1) (V _{DD} = 26 Vdc, I _{DQ} = 750 mA, f = 1805 – 1880 MHz)	G _{ps}	12.0	13.5	—	dB
Drain Efficiency @ 90 W (1) (V _{DD} = 26 Vdc, I _{DQ} = 750 mA, f = 1805 – 1880 MHz)	η	47	52	—	%
Input Return Loss (1) (V _{DD} = 26 Vdc, P _{out} = 90 W CW, I _{DQ} = 750 mA, f = 1805 – 1880 MHz)	IRL	—	—	–10	dB
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 90 W CW, I _{DQ} = 750 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.

Freescale Semiconductor, Inc.



C1	10 μ F, 35 V Tantalum Capacitor, Vishay–Sprague #293D106X9035D	Z3	0.819" x 0.087" Microstrip
C2, C3	10 pF, 100B Chip Capacitor, ATC #100B100GW	Z4	0.181" x 0.144" Microstrip
C4	3.3 pF, 100B Chip Capacitor, ATC #100B3R3BW	Z5	0.383" x 1.148" Microstrip
C5, C6	6.8 pF, 100B Chip Capacitors, ATC #100B6R8CW	Z6	0.400" x 1.380" Microstrip
C7	12 pF, 100B Chip Capacitors, ATC #100B120GW	Z7	0.351" x 0.351" Microstrip
C8	220 μ F, 63 V Electrolytic Capacitor, Philips #13668221	Z8	0.126" x 0.087" Microstrip
R1, R2	10 k Ω , 1/8 W Chip Resistors (0805)	Z9	1.280" x 0.087" Microstrip
R3	1.0 k Ω , 1/8 W Chip Resistor (0805)	Z10	$\approx$ 1.275" x 0.055" Microstrip
Z1	0.697" x 0.087" Microstrip	PCB	Taconic TLX8–0300, 0.030", $\epsilon_r = 2.55$
Z2	0.087" x 0.197" Microstrip		

Figure 1. MRF18090A 1.80 – 1.88 GHz Test Fixture Schematic

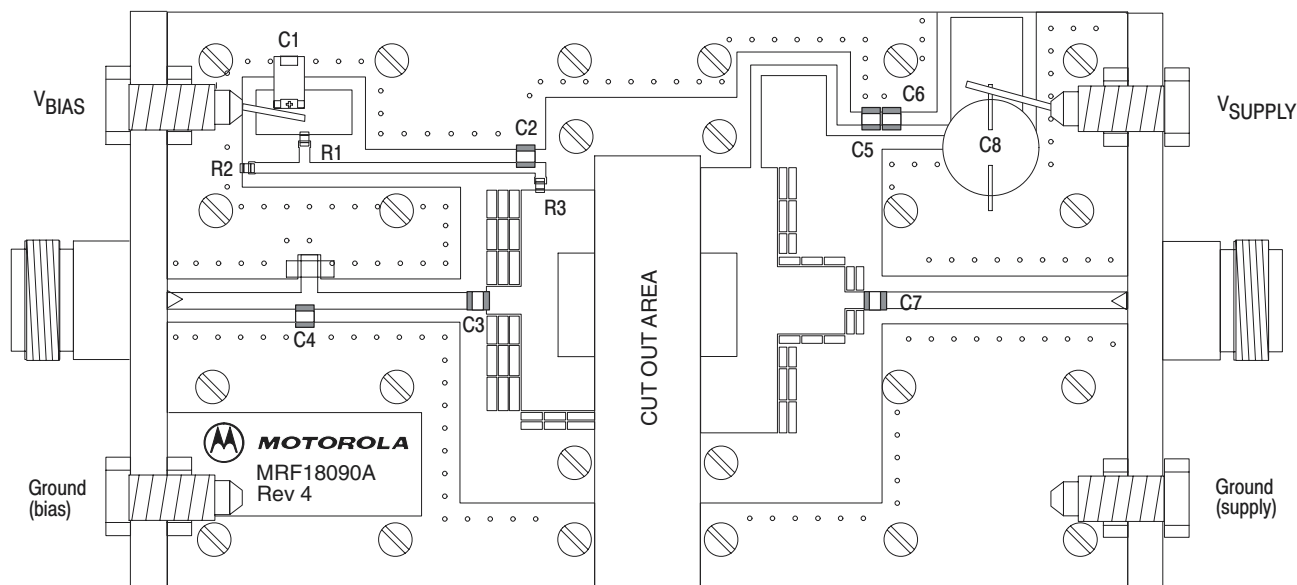
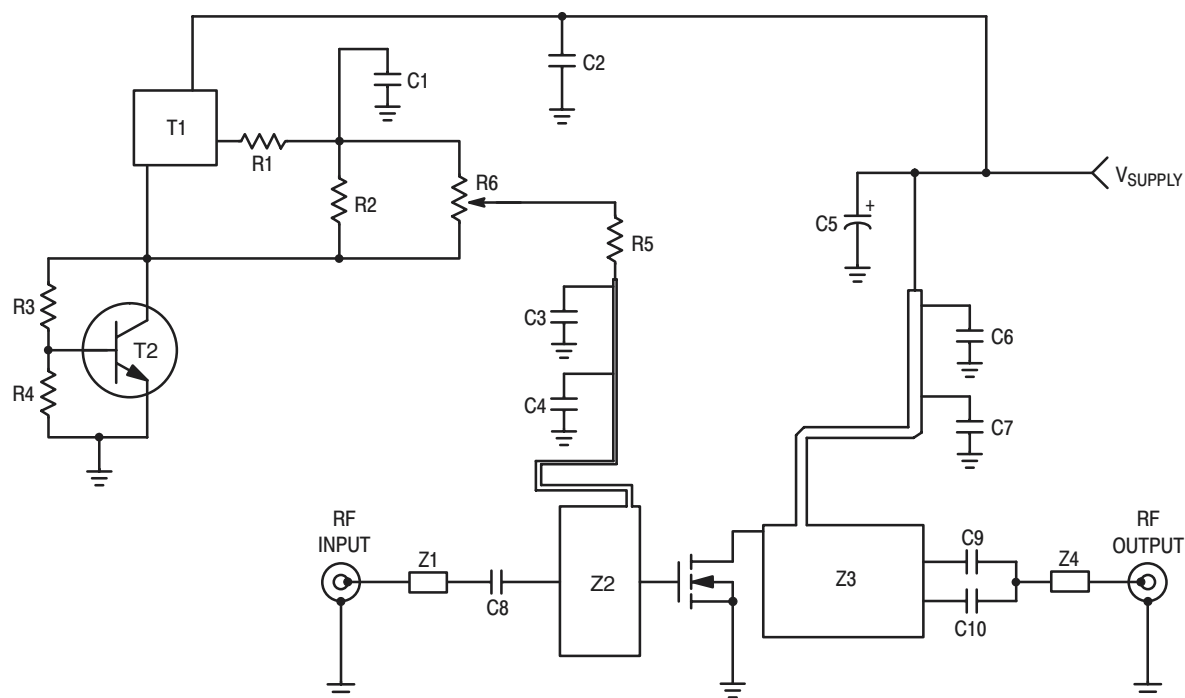


Figure 2. MRF18090A 1.80 – 1.88 GHz Test Fixture Component Layout

Freescale Semiconductor, Inc.



C1, C3	1 μ F Chip Capacitors (0805)	R5	10 k Ω Chip Resistor (0603)
C2	0.1 μ F Chip Capacitor (0805)	R6	5 k Ω , SMD Potentiometer
C4	1 nF Chip Capacitor (0805)	T1	LP2951 Micro-8 Voltage Regulator
C5	220 μ F, 50 V Electrolytic Capacitor	T2	BC847 SOT-23 NPN Transistor
C6, C7	8.2 pF, 100A Chip Capacitors	Z1	0.210" x 0.055" Microstrip
C8, C9, C10	22 pF, 100A Chip Capacitors	Z2	0.419" x 0.787" Microstrip
R1	10 Ω Chip Resistor (0805)	Z3	0.836" x 0.512" Microstrip
R2, R3	1 k Ω Chip Resistors (0805)	Z4	0.164" x 0.055" Microstrip
R4	2.2 k Ω Chip Resistor (0805)	Substrate = 0.5 mm Teflon [®] Glass	

Figure 3. 1.80 – 1.88 GHz Demo Board Schematic

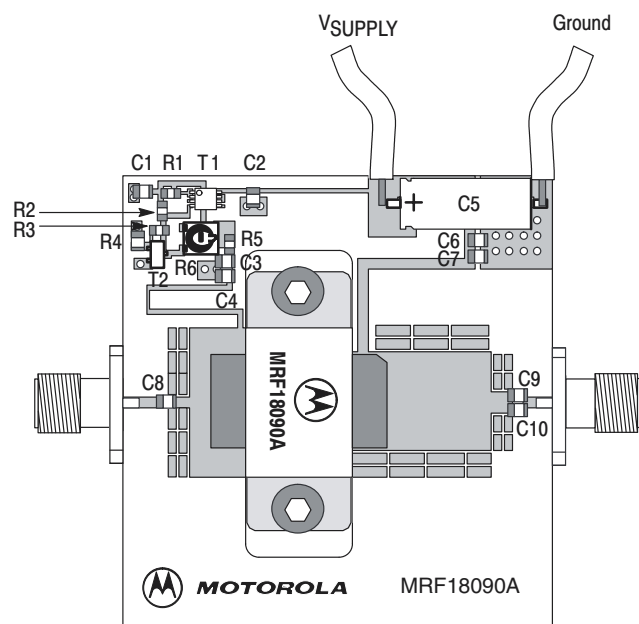


Figure 4. 1.80 – 1.88 GHz Demo Board Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

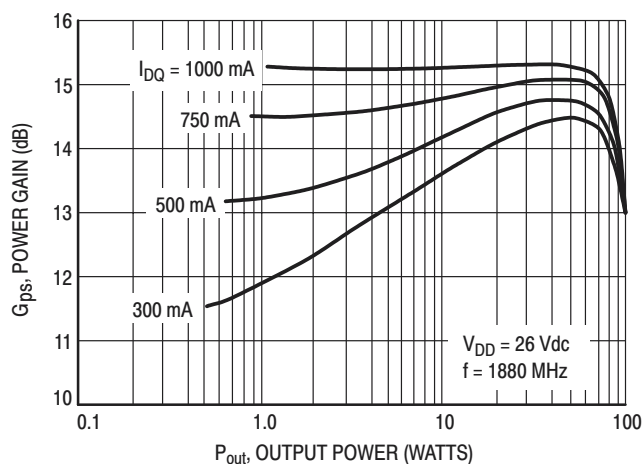


Figure 5. Power Gain versus Output Power

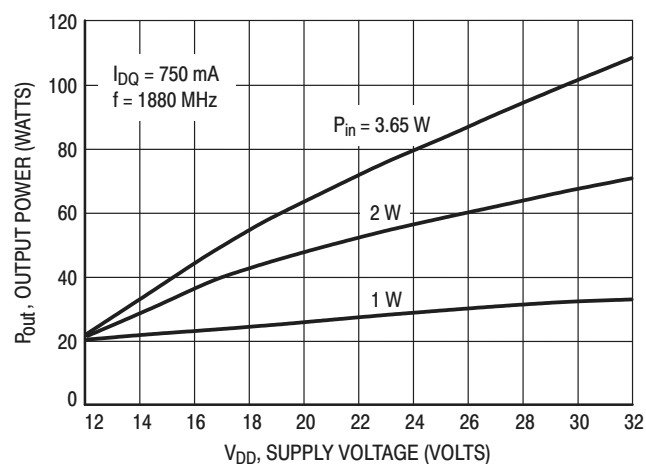


Figure 6. Output Power versus Supply Voltage

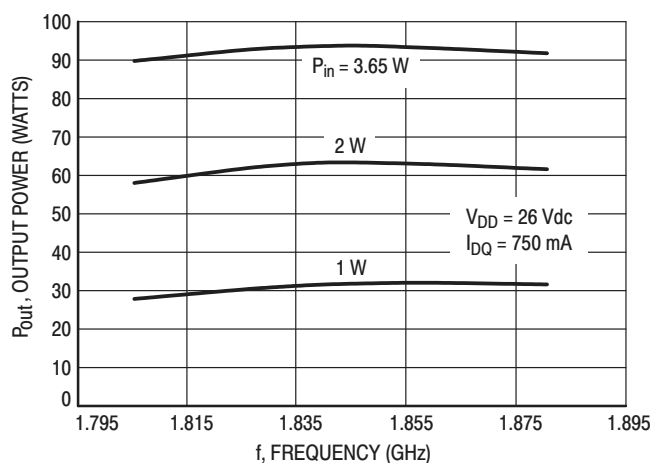


Figure 7. Output Power versus Frequency

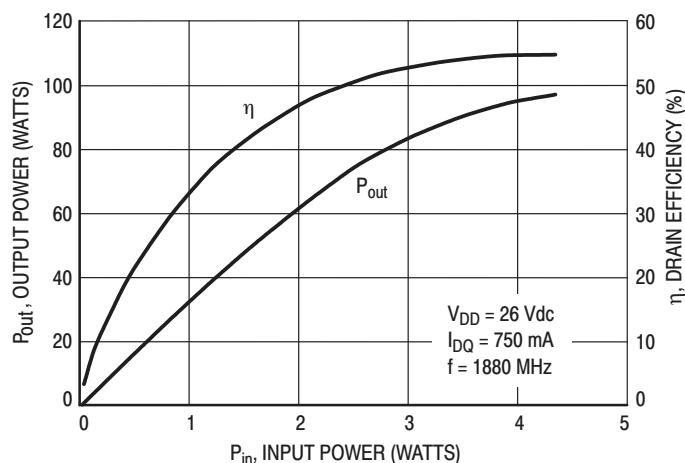


Figure 8. Output Power and Efficiency versus Input Power

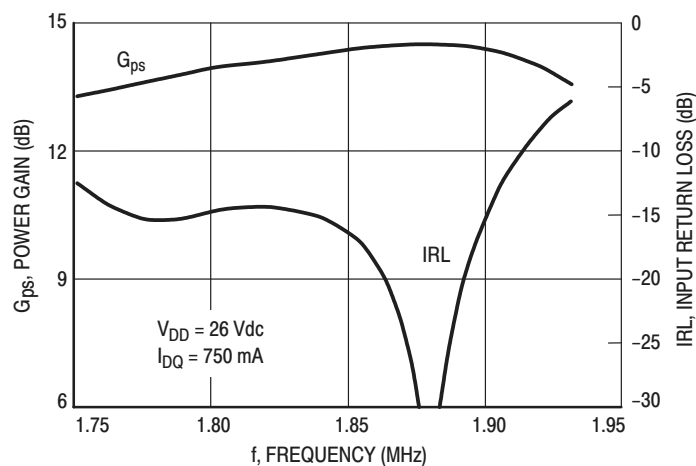
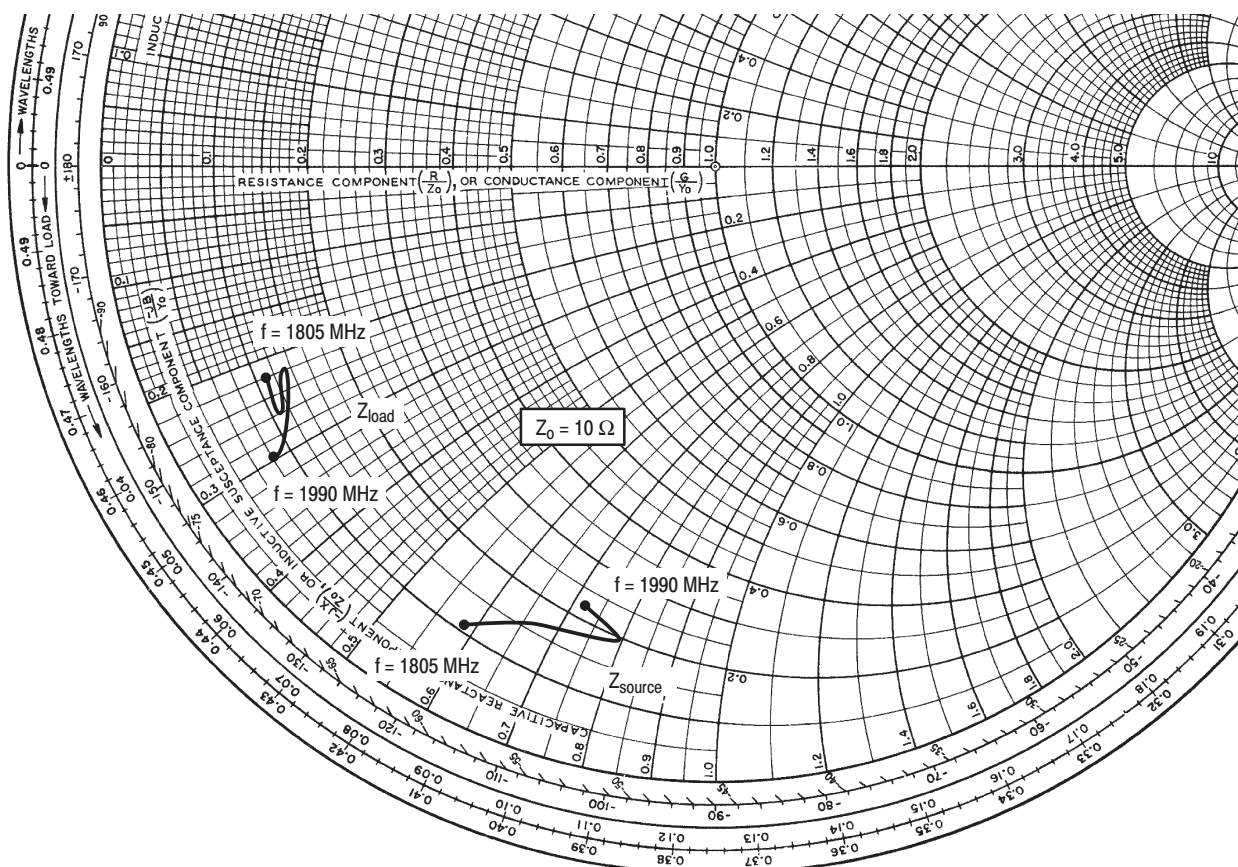


Figure 9. Wideband Gain and IRL (at Small Signal)



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 750 \text{ mA}$, $P_{out} = 90 \text{ Watts (CW)}$

f MHz	Z_{source} Ω	Z_{load} Ω
1805	$1.10 - j5.85$	$1.15 - j2.16$
1880	$1.56 - j6.75$	$1.13 - j2.60$
1930	$2.05 - j8.00$	$1.30 - j2.23$
1990	$2.30 - j7.30$	$0.82 - j2.90$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

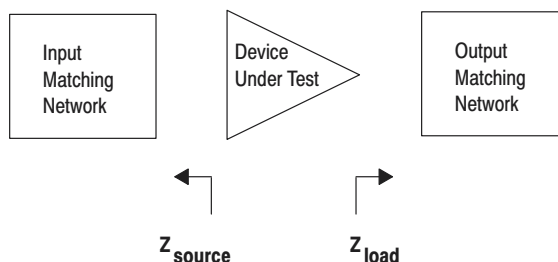


Figure 10. Large Signal Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

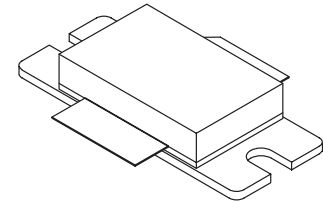
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and EDGE base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for GSM and EDGE cellular radio applications.

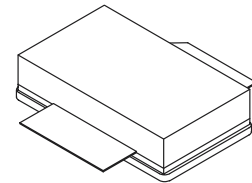
- GSM and EDGE Performances, Full Frequency Band
Power Gain — 13.5 dB (Typ) @ 90 Watts (CW)
Efficiency — 45% (Typ) @ 90 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

MRF18090B
MRF18090BS

1.90 – 1.99 GHz, 90 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETS



CASE 465B-03, STYLE 1
(NI-880)
(MRF18090B)



CASE 465C-02, STYLE 1
(NI-880S)
(MRF18090BS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 4

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 750 mAdc)	V _{GS(Q)}	2.5	3.7	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.1	—	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 Adc)	g _{fs}	—	7.2	—	S

DYNAMIC CHARACTERISTICS

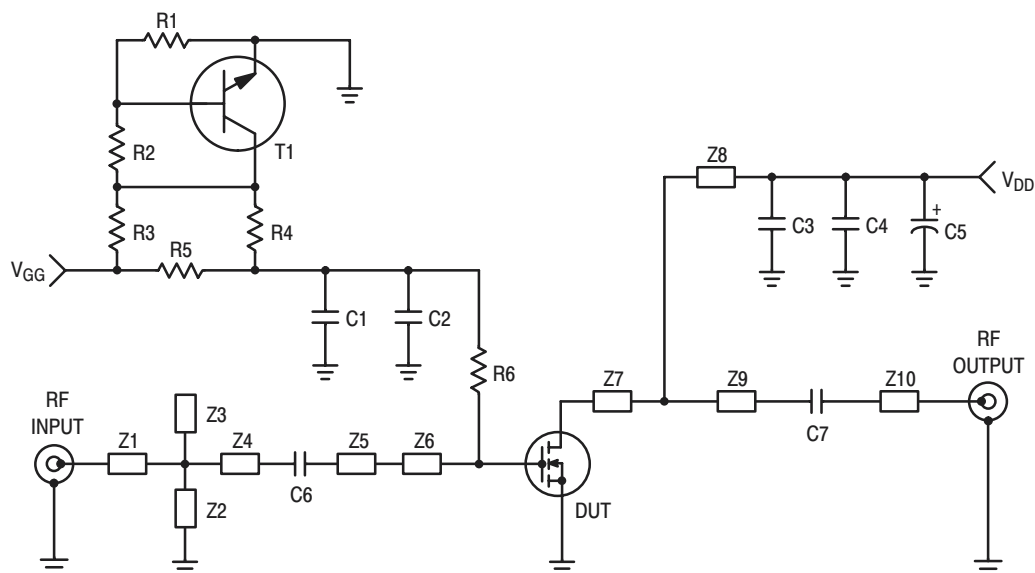
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	4.2	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain @ 90 W (1) (V _{DD} = 26 Vdc, I _{DQ} = 750 mA, f = 1930 – 1990 MHz)	G _{ps}	12	13.5	—	dB
Drain Efficiency @ 90 W (1) (V _{DD} = 26 Vdc, I _{DQ} = 750 mA, f = 1930 – 1990 MHz)	η	40	45	—	%
Input Return Loss (1) (V _{DD} = 26 Vdc, P _{out} = 90 W CW, I _{DQ} = 750 mA, f = 1930 – 1990 MHz)	IRL	—	—	–10	dB
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 90 W CW, I _{DQ} = 750 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1900 band, ensuring batch–to–batch consistency.

Freescale Semiconductor, Inc.



C1	1.0 μ F Chip Capacitor (0805)	Z2	Printed Inductance
C2	1.0 nF Chip Capacitor (0805)	Z3	Printed Inductance (Butterfly)
C3, C4	6.8 pF, 100B Chip Capacitors	Z4	0.70" x 0.09" Microstrip
C5	220 μ F, 50 V Electrolytic Capacitor	Z5	0.36" x 0.09" Microstrip
C6, C7	12 pF, 100B Chip Capacitors	Z6	0.21" x 1.25" Microstrip
R1	2.2 k Ω Chip Resistor (0805)	Z7	0.45" x 1.18" Microstrip
R2, R3, R6	1.0 k Ω Chip Resistors (0805)	Z8	1.37" x 0.05" Microstrip
R4	10 k Ω Chip Resistor (0805)	Z9	0.39" x 0.09" Microstrip
R5	6.8 k Ω Chip Resistor (0805)	Z10	1.25" x 0.09" Microstrip
T1	BC847 SOT-23	PCB	Teflon [®] Glass
Z1	0.85" x 0.09" Microstrip		

Figure 1. 1.93 – 1.99 MHz Test Fixture Schematic

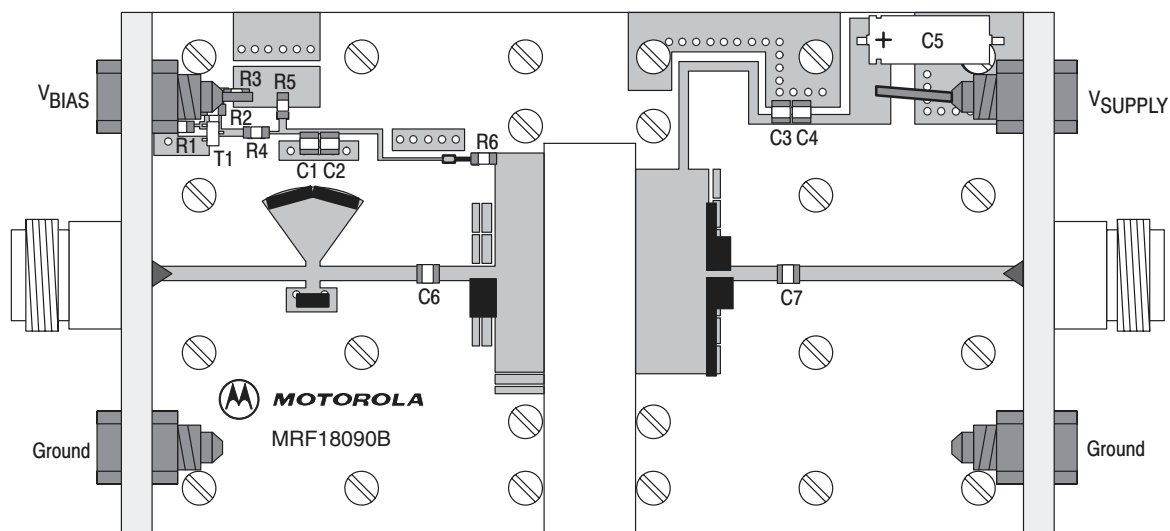
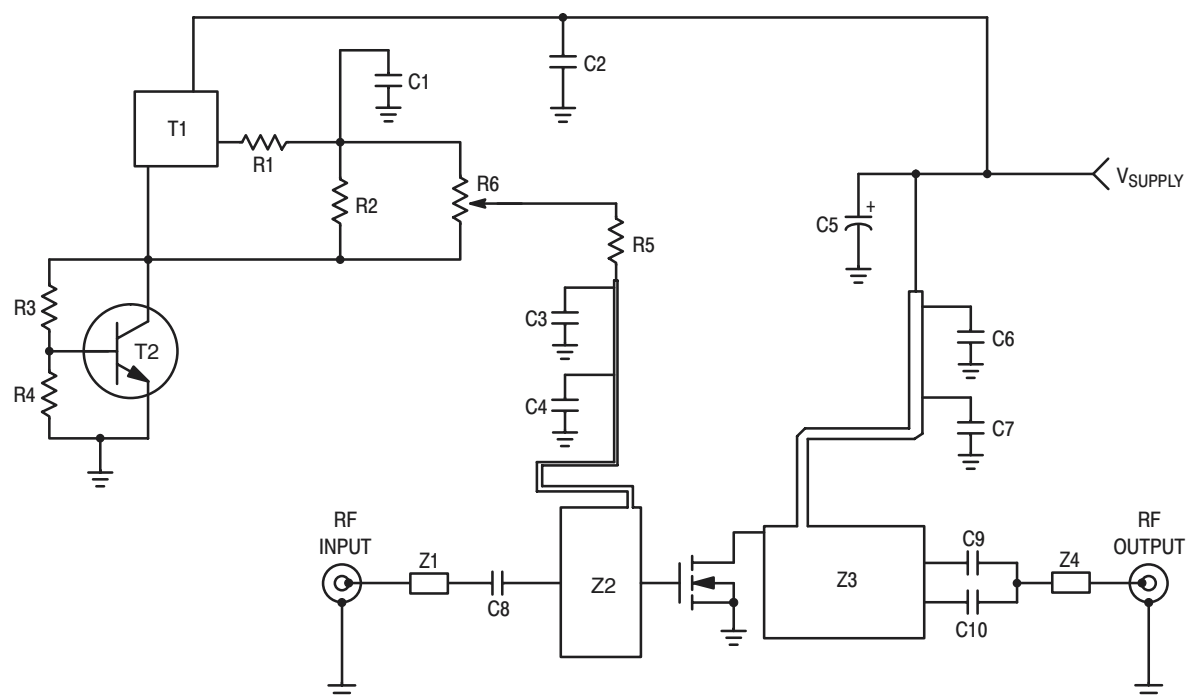


Figure 2. 1.93 – 1.99 GHz Test Fixture Component Layout

Freescale Semiconductor, Inc.



C1, C3	1 μ F Chip Capacitors (0805)	R5	10 k Ω Chip Resistor (0603)
C2	0.1 μ F Chip Capacitor (0805)	R6	5 k Ω , SMD Potentiometer
C4	1 nF Chip Capacitor (0805)	T1	LP2951 Micro-8 Voltage Regulator
C5	220 μ F, 50 V Electrolytic Capacitor	T2	BC847 SOT-23 NPN Transistor
C6, C7	8.2 pF, 100A Chip Capacitors	Z1	0.491" x 0.110" Microstrip
C8, C9, C10	22 pF, 100A Chip Capacitors	Z2	0.756" x 1.260" Microstrip
R1	10 Ω Chip Resistor (0805)	Z3	1.433" x 1.260" Microstrip
R2, R3	1 k Ω Chip Resistors (0805)	Z4	0.567" x 0.110" Microstrip
R4	2.2 k Ω Chip Resistor (0805)	Substrate = 0.5 mm Teflon [®] Glass	

Figure 3. 1.93 – 1.99 GHz Demo Board Schematic

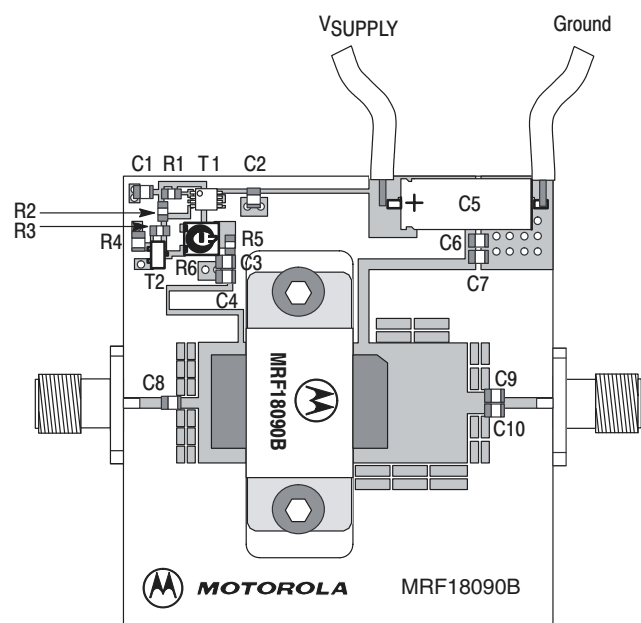


Figure 4. 1.93 – 1.99 GHz Demo Board Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

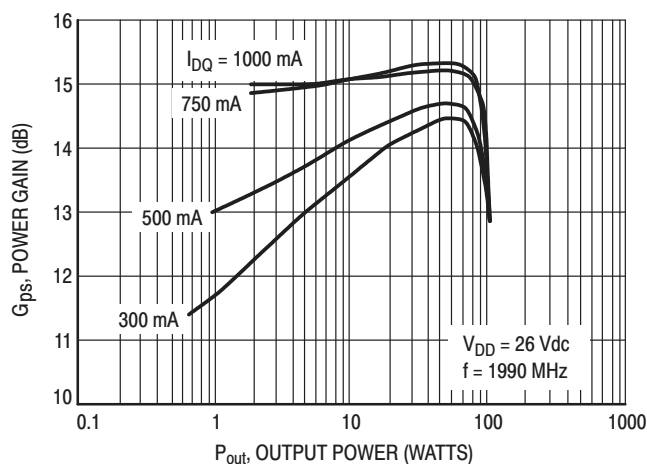


Figure 5. Power Gain versus Output Power

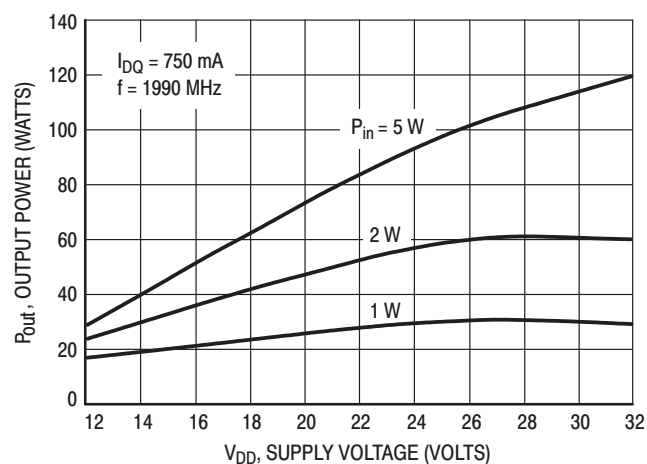


Figure 6. Output Power versus Supply Voltage

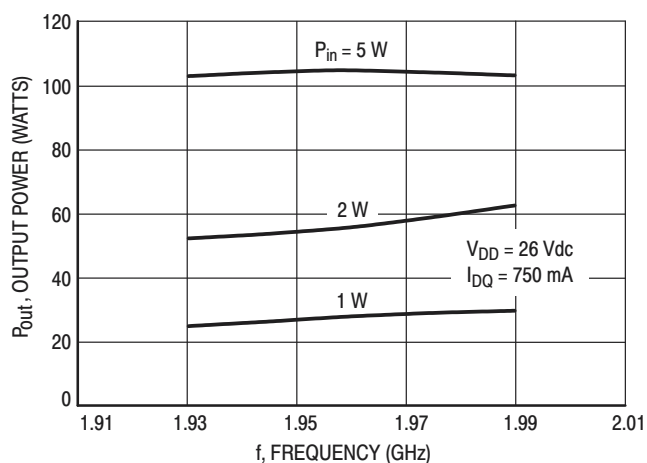


Figure 7. Output Power versus Frequency

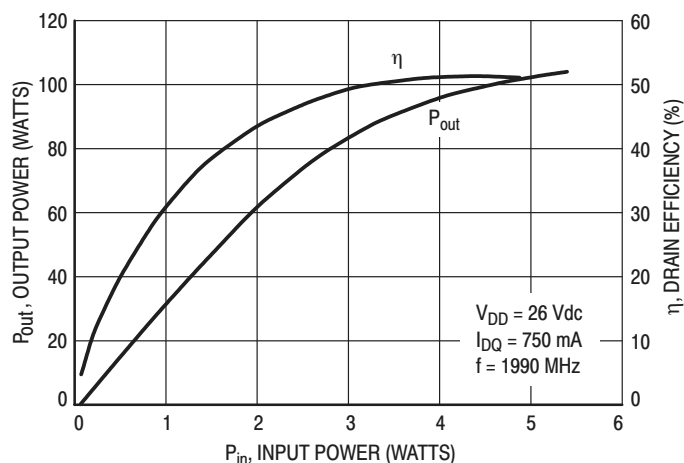


Figure 8. Output Power and Efficiency versus Input Power

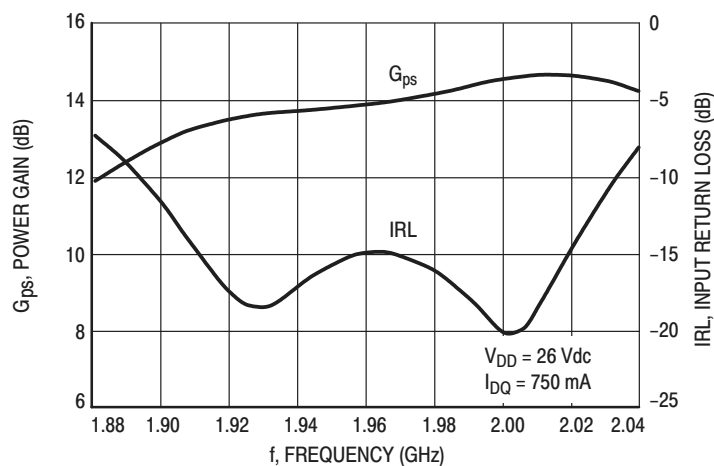


Figure 9. Wideband Gain and IRL (at Small Signal)



f MHz	Z_{source} Ω	Z_{load} Ω
1805	1.10 – j5.85	1.15 – j2.16
1880	1.56 – j6.75	1.13 – j2.60
1930	2.05 – j8.00	1.30 – j2.23
1990	2.30 – j7.30	0.82 – j2.90

Z_{load} = Test circuit impedance as measured from drain to ground.

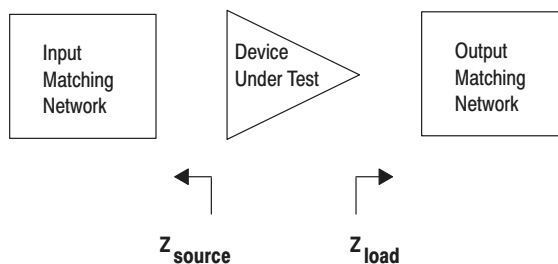


Figure 10. Large Signal Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

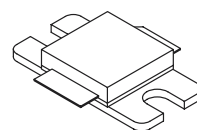
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for class AB PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

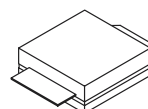
- CDMA Performance @ 1990 MHz, 26 Volts
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
885 kHz — -47 dBc @ 30 kHz BW
1.25 MHz — -55 dBc @ 12.5 kHz BW
2.25 MHz — -55 dBc @ 1 MHz BW
Output Power — 4.5 Watts Avg.
Power Gain — 13.5 dB
Efficiency — 17%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

MRF19030R3
MRF19030SR3

2.0 GHz, 30 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-04, STYLE 1
NI-400
MRF19030R3



CASE 465F-04, STYLE 1
NI-400S
MRF19030SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	83.3 0.48	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 20 μA)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 300 mA)	V _{GS(Q)}	2	3.3	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.29	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 1 Adc)	g _{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{iss}	—	98.5	—	pF
Output Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{oss}	—	37	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 300 mA, f ₁ = 1960.0 MHz, f ₂ = 1960.1 MHz)	G _{ps}	—	13	—	dB
Two–Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 300 mA, f ₁ = 1960.0 MHz, f ₂ = 1960.1 MHz)	η	—	36	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 300 mA, f ₁ = 1960.0 MHz, f ₂ = 1960.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 300 mA, f ₁ = 1960.0 MHz, f ₂ = 1960.1 MHz)	IRL	—	–13	—	dB
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 300 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz and f ₁ = 1990.0 MHz, f ₂ = 1990.1 MHz)	G _{ps}	12	13	—	dB
Two–Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 300 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz and f ₁ = 1990.0 MHz, f ₂ = 1990.1 MHz)	η	33	36	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 300 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz and f ₁ = 1990.0 MHz, f ₂ = 1990.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 30 W PEP, I _{DQ} = 300 mA, f ₁ = 1930.0 MHz, f ₂ = 1930.1 MHz and f ₁ = 1990.0 MHz, f ₂ = 1990.1 MHz)	IRL	—	–13	–9	dB
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 30 W CW, I _{DQ} = 300 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.

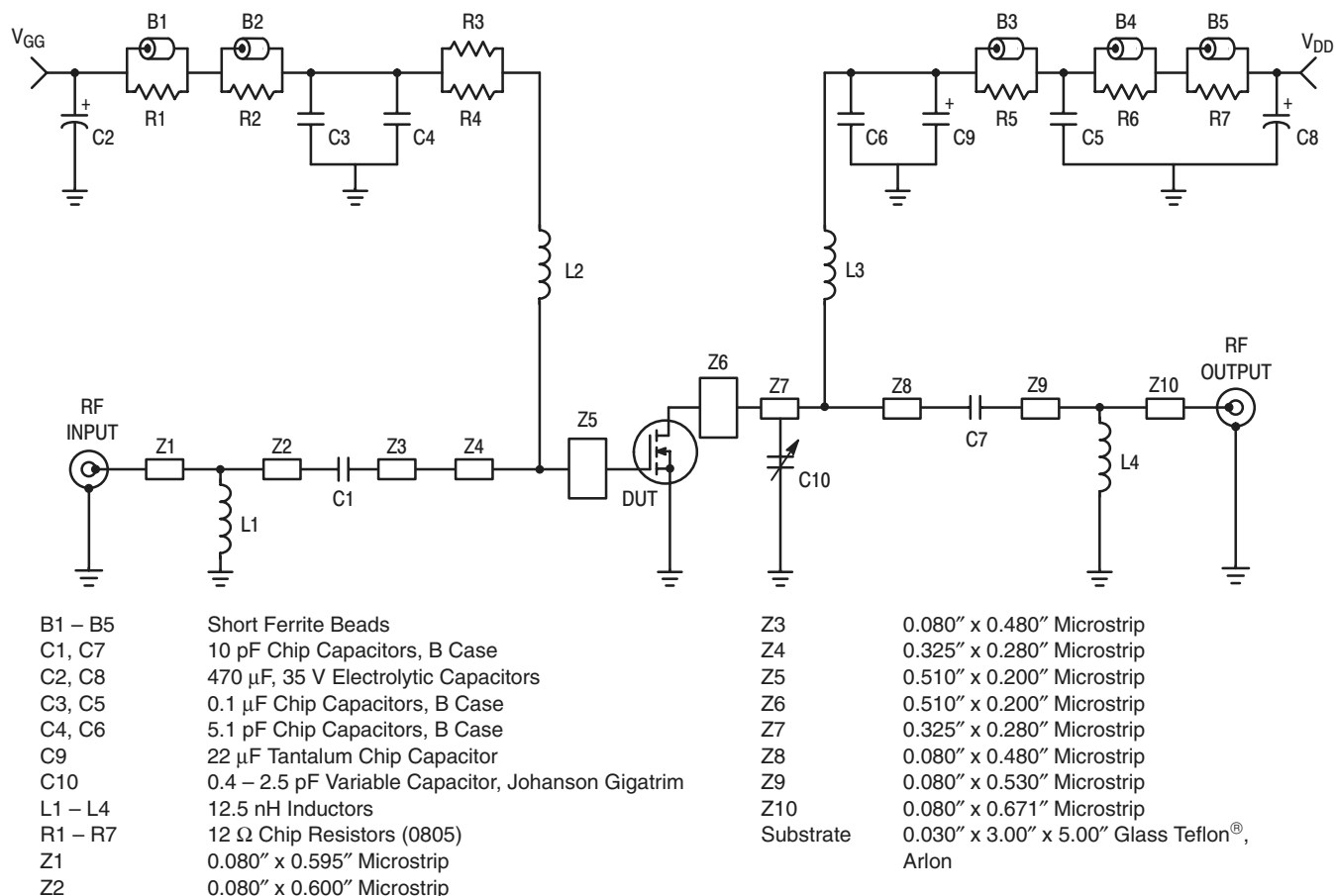


Figure 1. MRF19030 Test Circuit Schematic

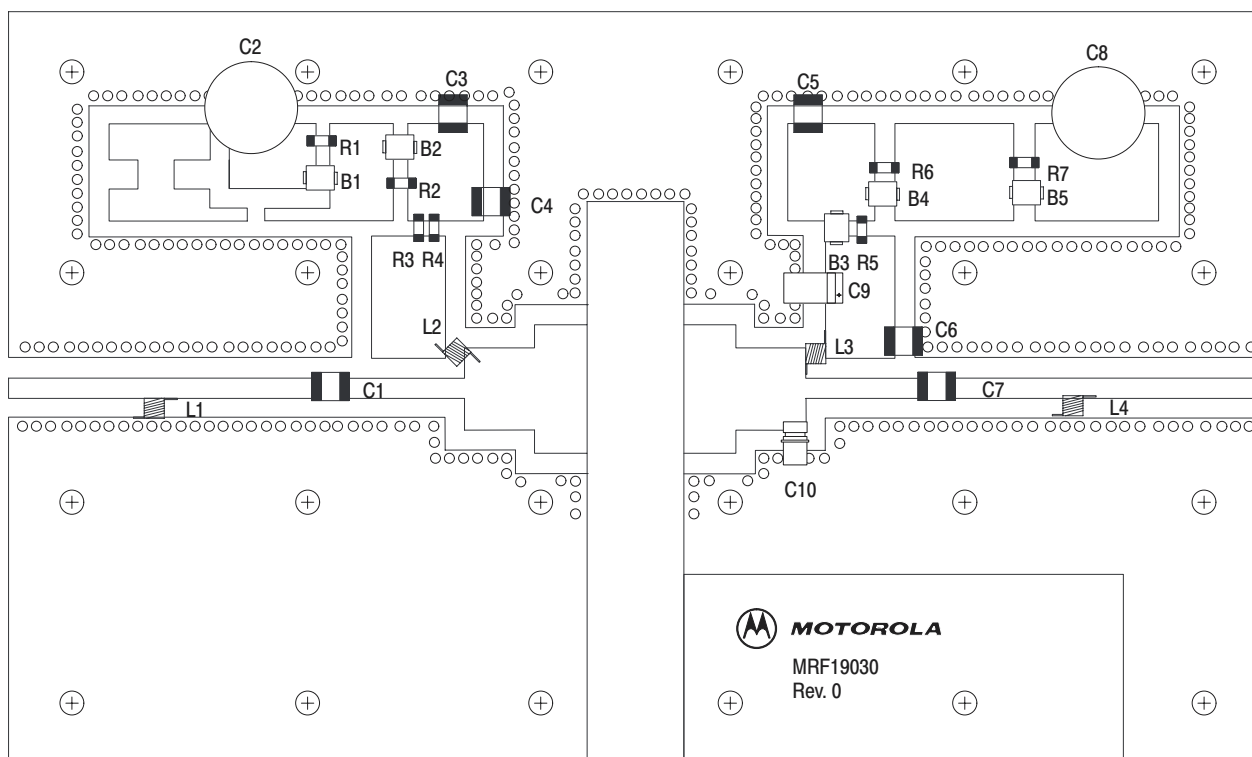


Figure 2. MRF19030 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

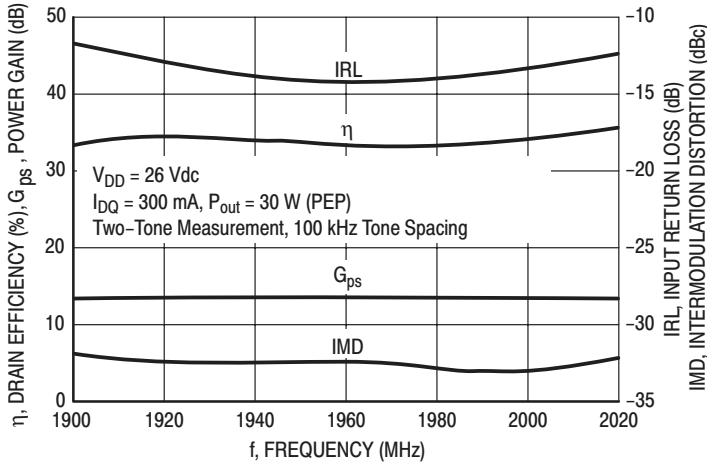


Figure 3. Class AB Broadband Circuit Performance

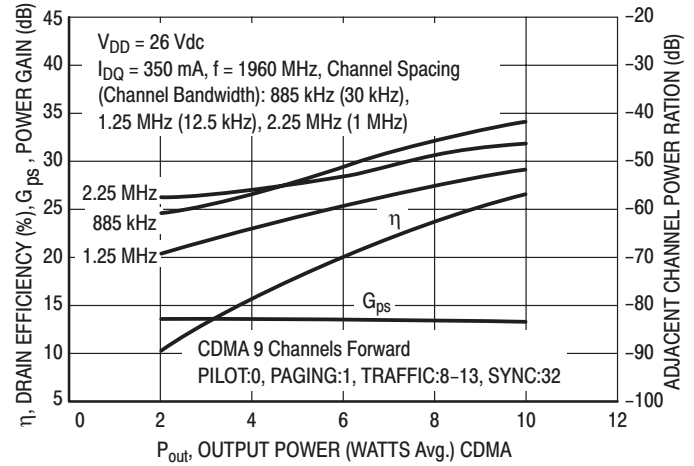


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

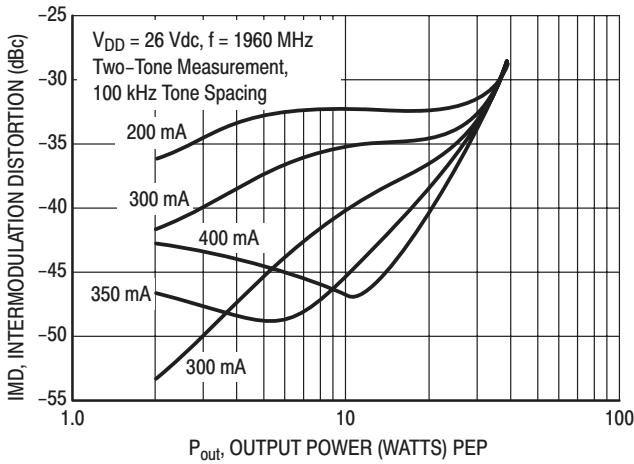


Figure 5. Intermodulation Distortion versus Output Power

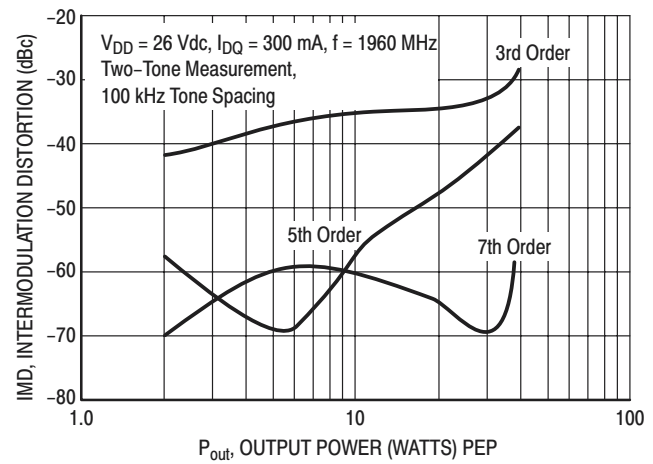


Figure 6. Intermodulation Distortion Products versus Output Power

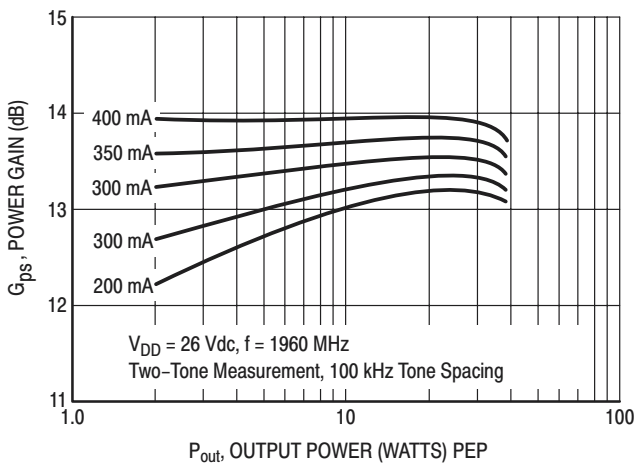


Figure 7. Power Gain versus Output Power

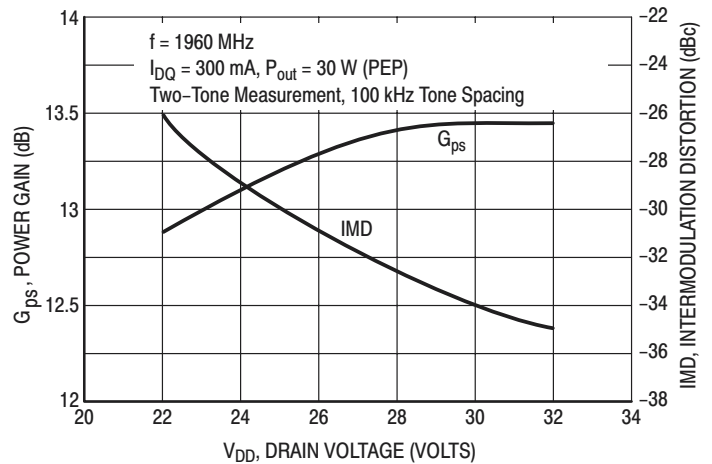
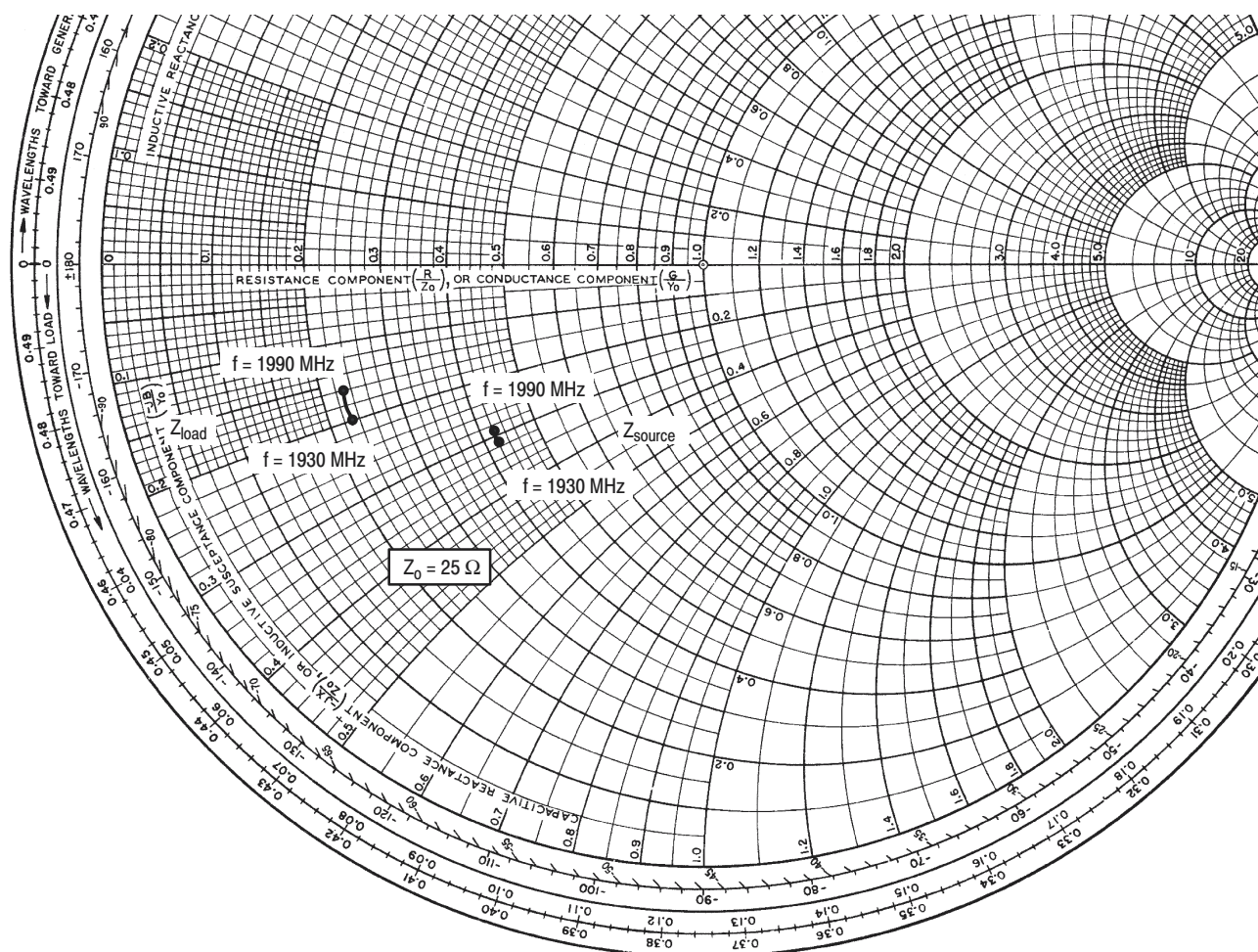


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 300 \text{ mA}$, $P_{\text{out}} = 30 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$10.57 - j7.69$	$5.81 - j5.01$
1960	$10.54 - j7.43$	$5.84 - j4.67$
1990	$10.47 - j7.21$	$5.84 - j4.35$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

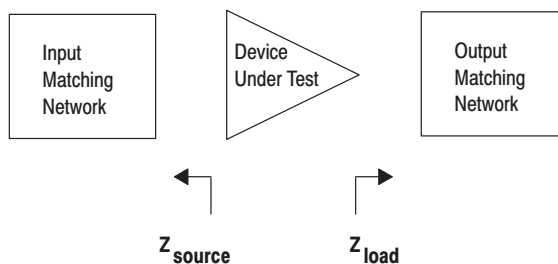


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

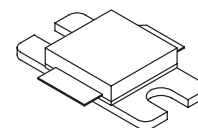
Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications.

- Typical CDMA Performance @ 1960 MHz, 26 Volts, $I_{DQ} = 550$ mA
Multi-carrier CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 9.5 Watts Avg.
Power Gain — 14.9 dB
Efficiency — 23.5%
Adjacent Channel Power —
885 kHz: -50 dBc @ 30 kHz BW
IM3 — -37 dBc
- 100% Tested Under 2-Carrier N-CDMA
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1.93 GHz, 45 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

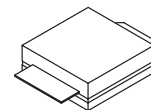
MRF19045R3

MRF19045SR3

1990 MHz, 45 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-04, STYLE 1
NI-400
MRF19045R3



CASE 465F-04, STYLE 1
NI-400S
MRF19045SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	105 0.60	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.65	$^\circ\text{C/W}$

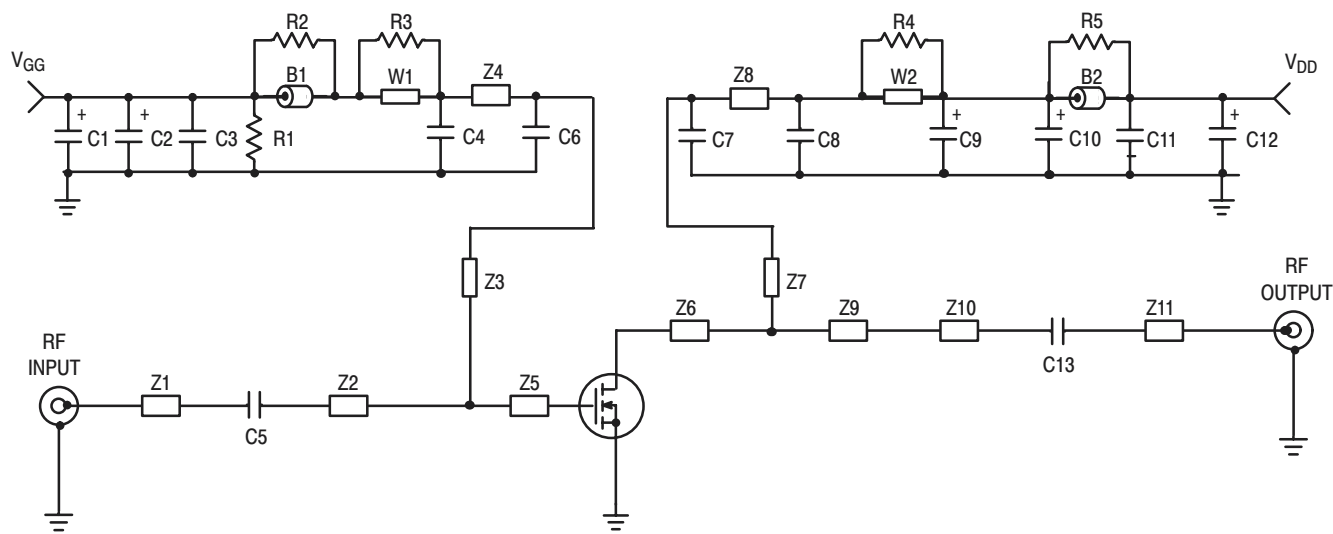
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (DC)					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 550 mA)	V _{GS(Q)}	3	3.8	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.19	0.21	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{rss}	—	1.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier N–CDMA, 1.2288 MHz Channel Bandwidth, IM3 measured in 1.2288 MHz Integrated Bandwidth. ACPR measured in 30 kHz Integrated Bandwidth.					
Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 9.5 W Avg, 2–Carrier N–CDMA, I _{DQ} = 550 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz)	G _{ps}	13	14.5	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 9.5 W Avg, 2–Carrier N–CDMA, I _{DQ} = 550 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz)	η	21	23.5	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 9.5 W Avg, 2–Carrier N–CDMA, I _{DQ} = 550 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz; IM3 Measured in a 1.2288 MHz Integrated Bandwidth Centered at f ₁ –2.5 Mhz and f ₂ +2.5 MHz, Referenced to the Carrier Channel Power)	IM3	—	–37	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 26 Vdc, P _{out} = 9.5 W Avg, 2–carrier N–CDMA, I _{DQ} = 550 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz; ACPR measured in a 30 kHz Integrated Bandwidth Centered at f ₁ –885 kHz and f ₂ +885 kHz)	ACPR	—	–51	–45	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 9.5 W Avg, 2–Carrier N–CDMA, I _{DQ} = 550 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz)	IRL	—	–16	–9	dB
P _{out} , 1 dB Compression Point (V _{DD} = 26 Vdc, I _{DQ} = 550 mA, f = 1990 MHz)	P1dB	—	45	—	W
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 45 W CW, I _{DQ} = 550 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.



Z1	1.336" x 0.081" Microstrip	Z8	0.216" x 0.047" Microstrip
Z2	0.693" x 0.081" Microstrip	Z9	0.519" x 0.254" Microstrip
Z3	1.033" x 0.047" Microstrip	Z10	0.874" x 0.081" Microstrip
Z4	0.468" x 0.047" Microstrip	Z11	0.645" x 0.081" Microstrip
Z5	0.271" x 0.460" Microstrip	PCB	Arlon GX0300-55-22, 30 mils, $\epsilon_r = 2.55$
Z6	0.263" x 0.930" Microstrip		
Z7	1.165" x 0.047" Microstrip		

NOTE: Z3, Z4, Z7, Z8 lengths and component placement tolerances are $\pm 0.050"$.
 Zx lengths are microstrip lengths between components, center-line to center-line.
 All component and z-length tolerances are $\pm 0.015"$, except as noted.

Figure 1. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Schematic

Table 1. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Component Designations and Values

Designators	Description
B1, B2	0.120" x 0.333" x 0.100", Surface Mount Ferrite Beads, Fair Rite #2743019446
C1, C2	10 μ F, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T495X106K035AS4394
C3, C11	0.1 μ F Chip Capacitors, Kemet #CDR33BX104AKWS
C4, C8	24 pF Chip Capacitors, B Case, ATC #100B240JP500X
C5	470 pF Chip Capacitor, B Case, ATC #100B471JP200X
C6, C7	11 pF Chip Capacitors, B Case, ATC #100B110JP500X
C9, C10, C12	22 μ F, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T491X226K035AS4394
C13	8.2 pF Chip Capacitor, B Case, ATC #100B8R2CP500X
R1	560 k Ω , 1/4 W Chip Resistor (0.08" x 0.13")
R2, R3, R4, R5	8.2 Ω , 1/4 W Chip Resistors (0.08" x 0.13"), Garrett Instruments #RM73B2B110JT
W1, W2	Solid Copper Buss Wire, 16 AWG
WS1, WS2	Beryllium Copper Wear Blocks (0.005" x 0.150" x 0.350") Nominal

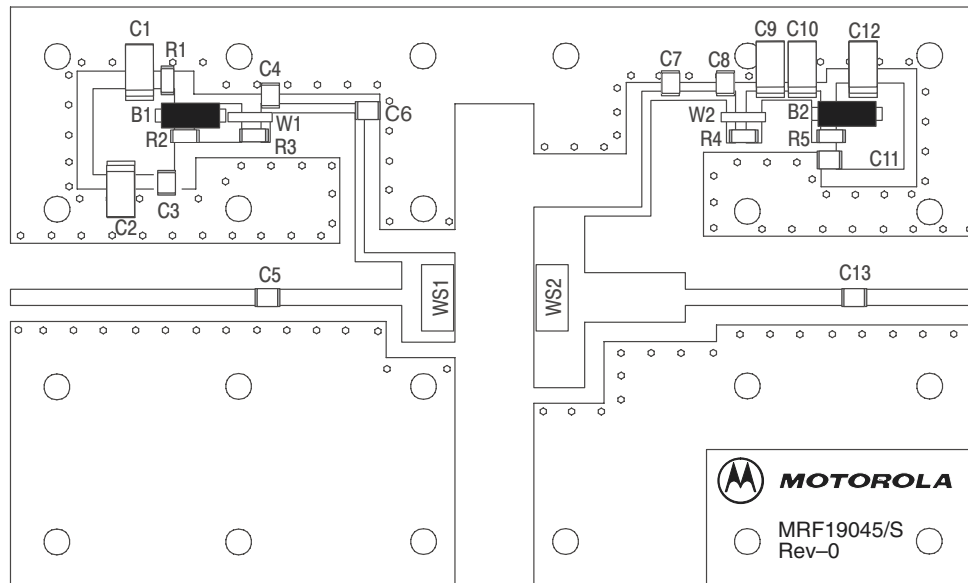


Figure 2. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

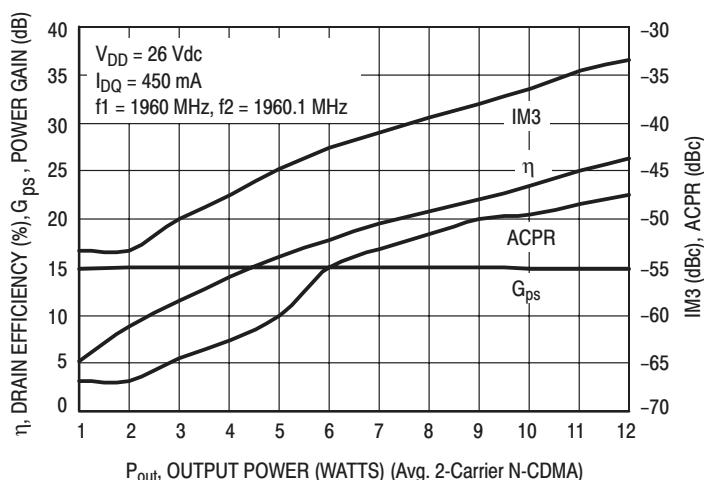


Figure 3. 2-Carrier N-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

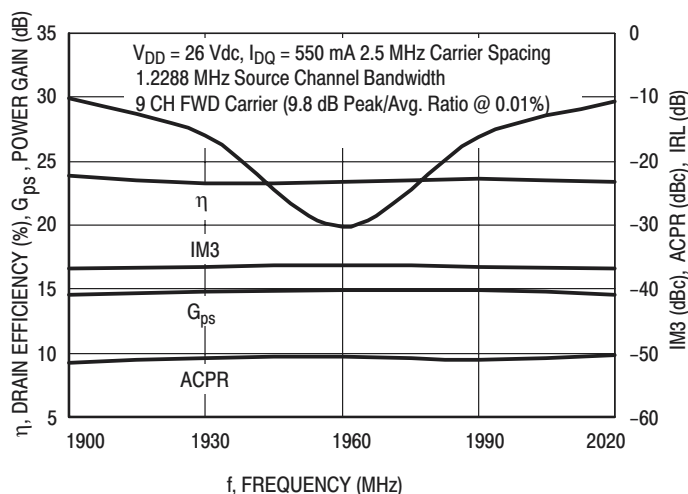


Figure 4. 2-Carrier N-CDMA ACPR, IM3, Power Gain, IRL and Drain Efficiency versus Output Power

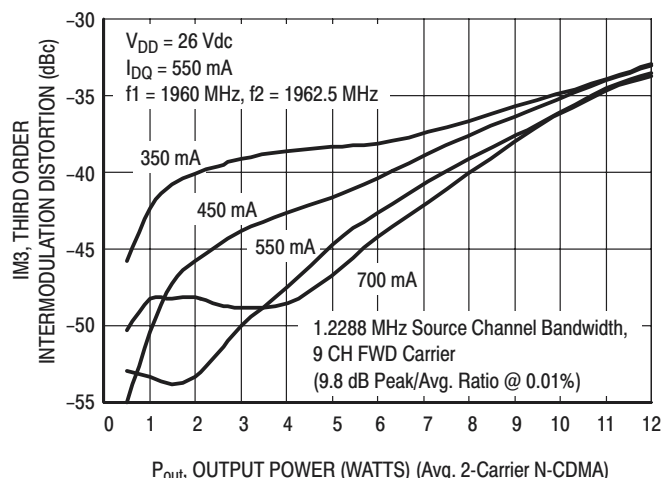


Figure 5. 2-Carrier N-CDMA IM3 versus Output Power

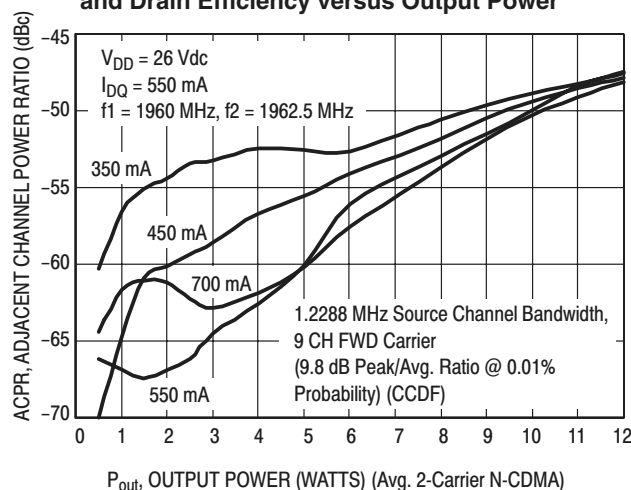


Figure 6. 2-Carrier N-CDMA ACPR versus Output Power

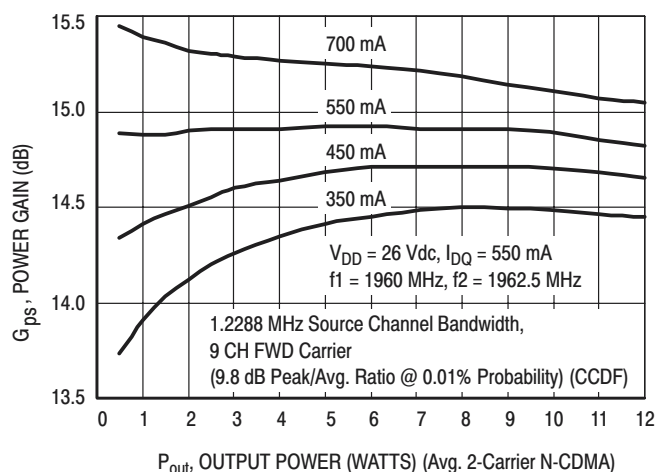


Figure 7. 2-Carrier N-CDMA Power Gain versus Output Power

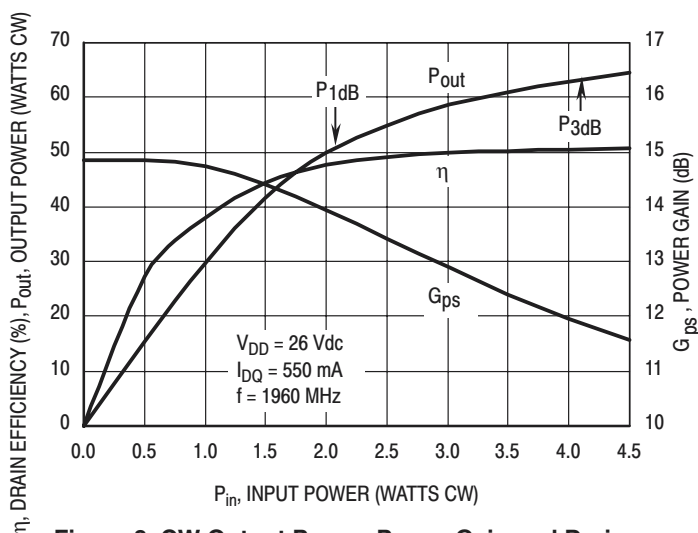


Figure 8. CW Output Power, Power Gain and Drain Efficiency versus Input Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

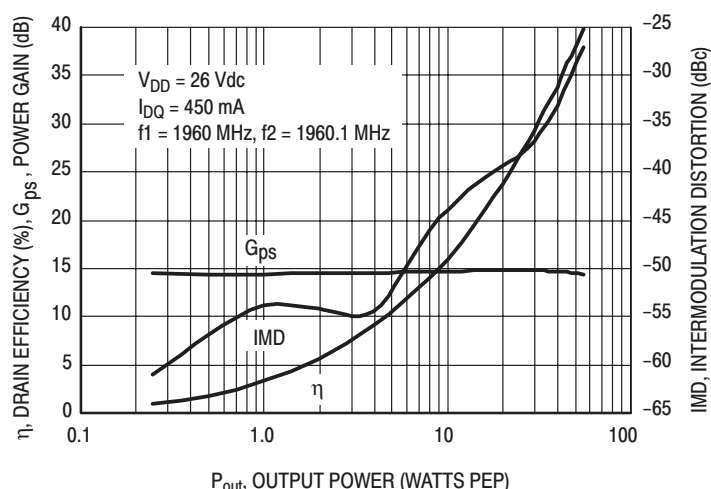


Figure 9. CW Two-Tone Power Gain, IMD and Drain Efficiency versus Output Power

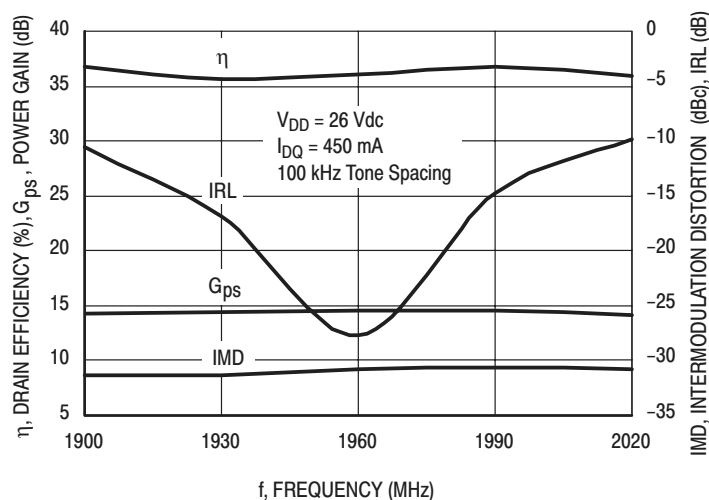


Figure 10. CW Two-Tone Power Gain, Input Return Loss, IMD and Drain Efficiency versus Frequency

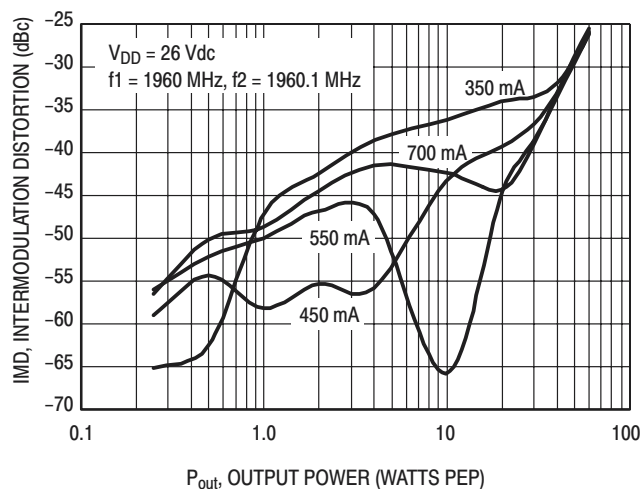


Figure 11. CW Two-Tone Intermodulation Distortion versus Output Power

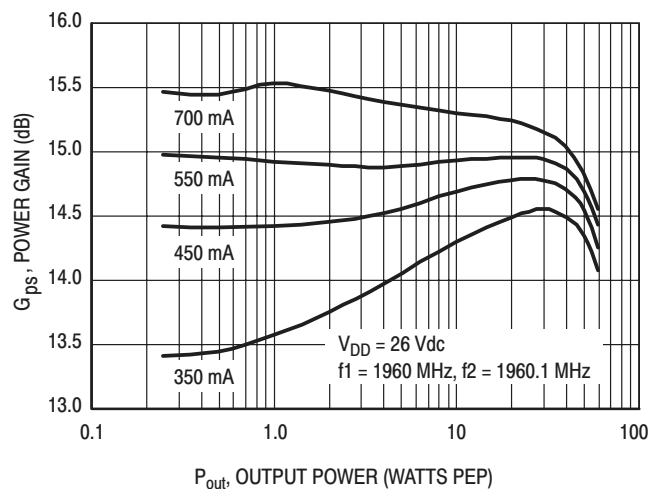


Figure 12. CW Two-Tone Power Gain versus Output Power

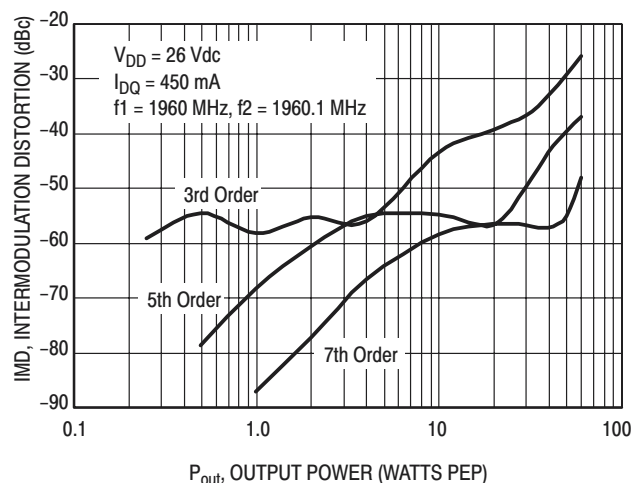


Figure 13. CW Two-Tone Intermodulation Distortion Products versus Output Power

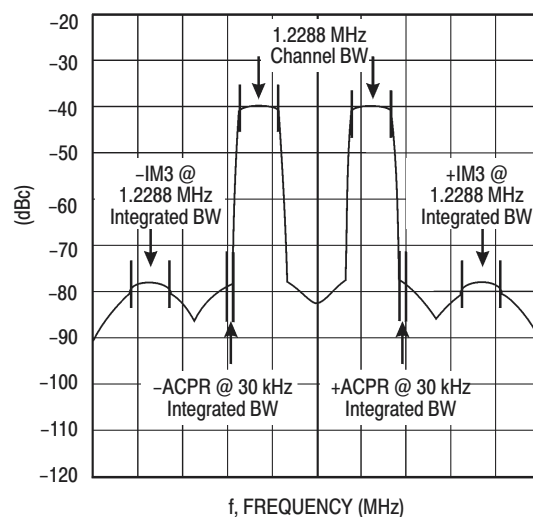
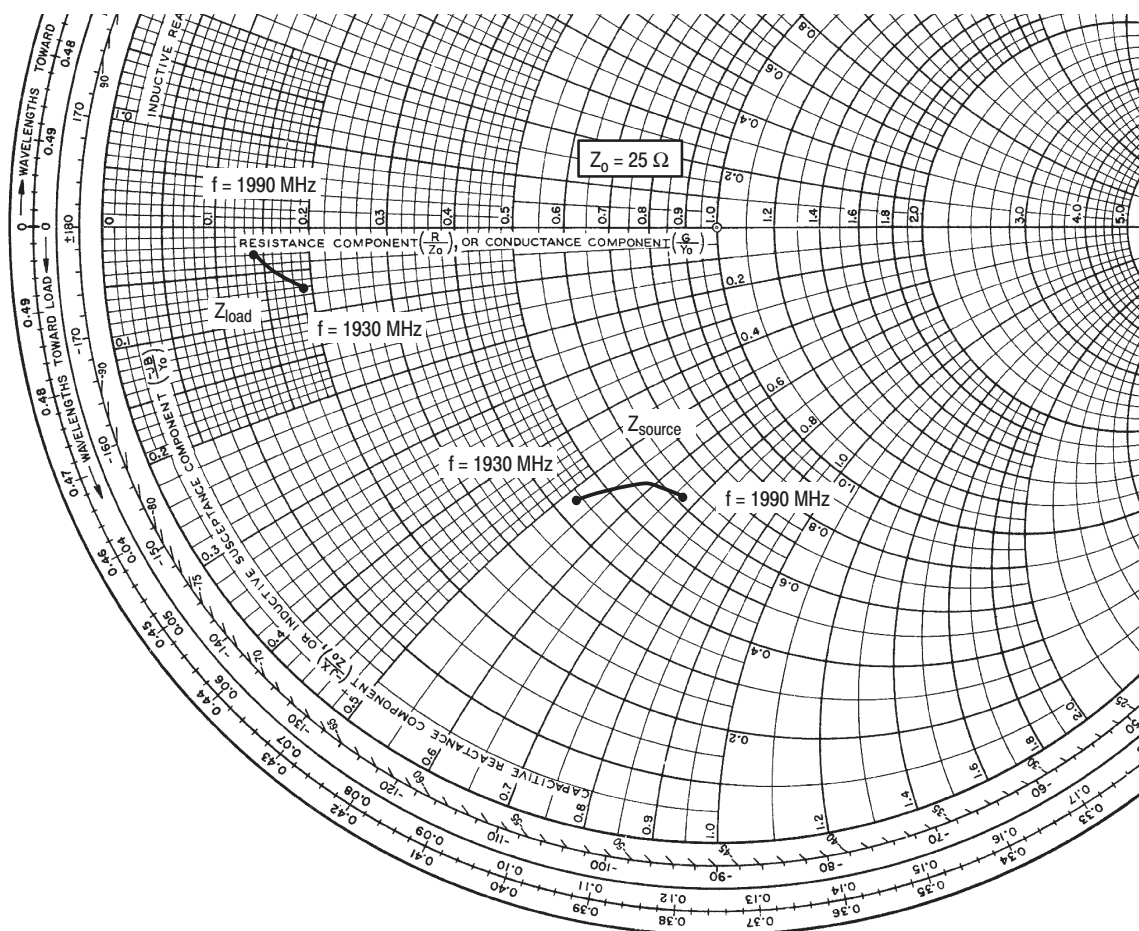


Figure 14. 2-Carrier N-CDMA Spectrum



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 550 \text{ mA}$, $P_{\text{out}} = 9 \text{ W Avg.}$, 2-Carrier N-CDMA

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$15.52 - j16.5$	$4.52 - j1.86$
1960	$14.24 - j14.44$	$3.85 - j1.04$
1990	$11.11 - j13.01$	$3.44 - j0.69$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

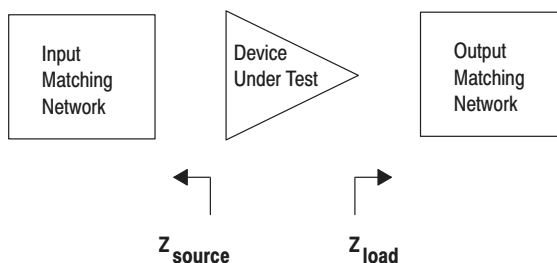


Figure 15. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

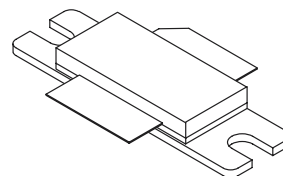
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM and multicarrier amplifier applications.

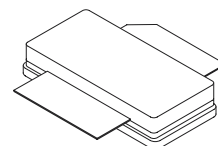
- Typical CDMA Performance: 1960 MHz, 26 Volts
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 7.5 Watts
Power Gain — 12.5 dB
Adjacent Channel Power —
885 kHz: -47 dBc @ 30 kHz BW
1.25 MHz: -55 dBc @ 12.5 kHz BW
2.25 MHz: -55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 60 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

MRF19060
MRF19060R3
MRF19060SR3

1990 MHz, 60 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF19060R3



CASE 465A-06, STYLE 1
NI-780S
MRF19060SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	180 1.03	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	$^\circ\text{C}/\text{W}$

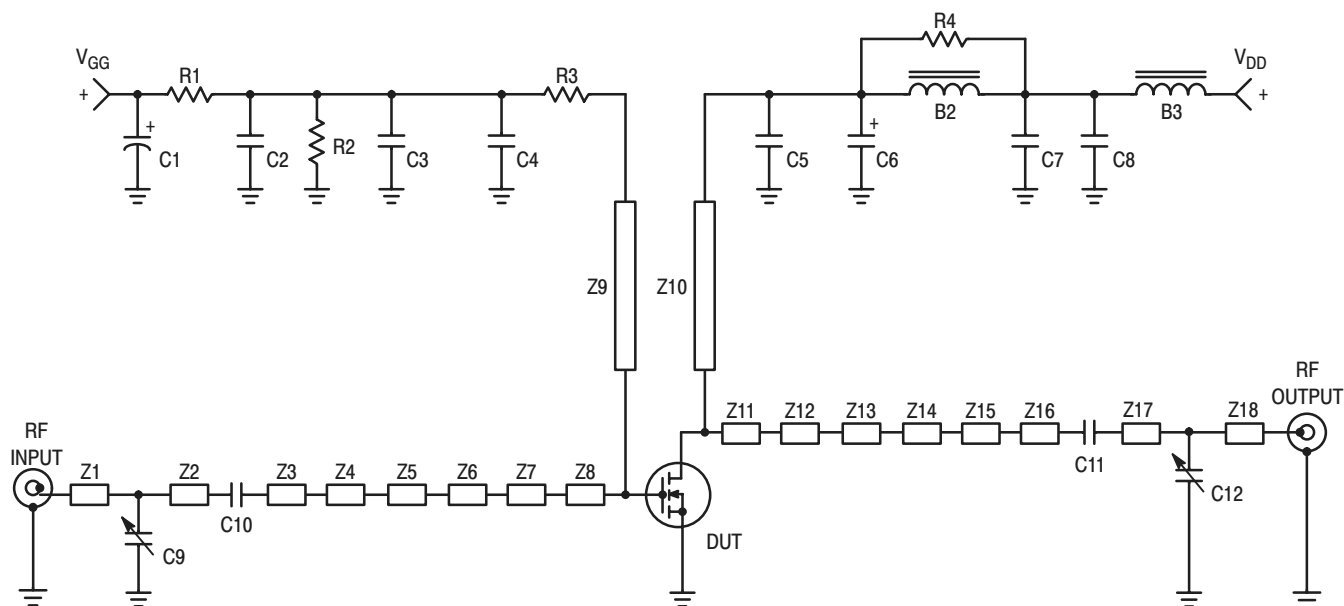
NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 10 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.7	—	S
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2	—	4	V
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 500 mAdc)	V _{GS(Q)}	2.5	3.9	4.5	V
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.27	—	V
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	G _{ps}	11	12.5	—	dB
Two–Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	η	33	36	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–31	–28	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P _{out} , 1 dB Compression Point (V _{DD} = 26 Vdc, P _{out} = 60 W CW, f = 1990 MHz)	P1dB	—	60	—	W
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 500 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.



B2 – B3	Ferrite Beads, Fair Rite, 2743019447	Z4	0.152" x 0.140" Microstrip
C1	10 μ F, 50 V Electrolytic Capacitor, Panasonic #ECEV1HV100R	Z5	0.090" x 0.102" Microstrip
C2, C7	1000 pF Chip Capacitors, B Case, ATC #100B102JCA500X	Z6	0.245" x 0.217" Microstrip
C3, C8	0.10 μ F Chip Capacitors, B Case, Kemet #CDR33BX104AKWS	Z7	0.090" x 0.737" Microstrip
C4	5.1 pF Chip Capacitor, B Case, ATC #100B5R1JCA500X	Z8	0.530" x 0.941" Microstrip
C5	6.2 pF Chip Capacitor, B Case, ATC #100B6R2JCA500X	Z9	1.010" x 0.050" Microstrip
C6	22 μ F, 35 V Tantalum Capacitor, SMT, Sprague	Z10	1.060" x 0.050" Microstrip
C9	0.8 pF – 8.0 pF Variable Capacitor, Johanson Gigatrim	Z11	0.446" x 1.137" Microstrip
C10, C11	10 pF Chip Capacitors, B Case, ATC #100B100JCA500X	Z12	0.152" x 0.567" Microstrip
C12	0.4 pF – 2.5 pF Variable Capacitor, Johanson Gigatrim	Z13	0.183" x 0.220" Microstrip
R1	1 k Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z14	0.100" x 0.338" Microstrip
R2	560 k Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z15	0.480" x 0.142" Microstrip
R3	15 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z16	0.140" x 0.080" Microstrip
R4	10 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z17	0.173" x 0.080" Microstrip
Z1	0.580" x 0.074" Microstrip	Z18	0.420" x 0.080" Microstrip
Z2	0.100" x 0.074" Microstrip	Board	0.030" Glass Teflon [®] Arlon
Z3	0.384" x 0.074" Microstrip		GX-0300-55-22, 2 oz Cu

Figure 1. MRF19060 Test Circuit Schematic

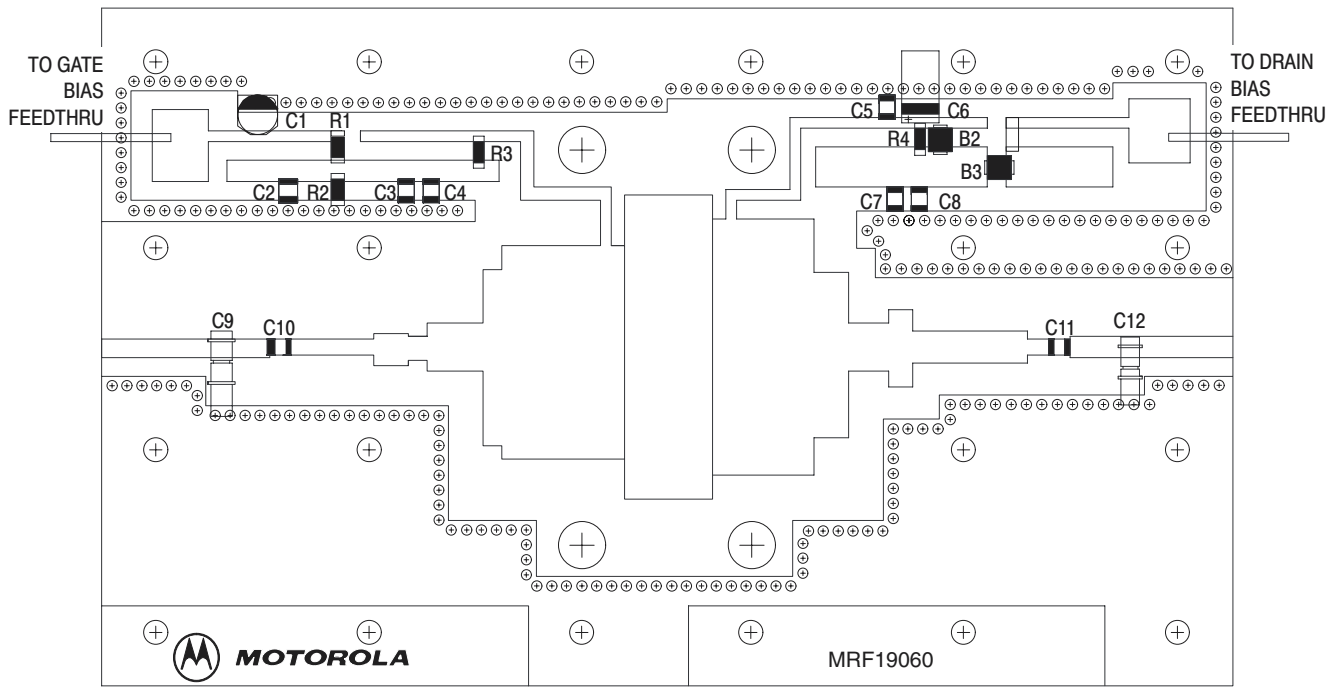


Figure 2. MRF19060 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

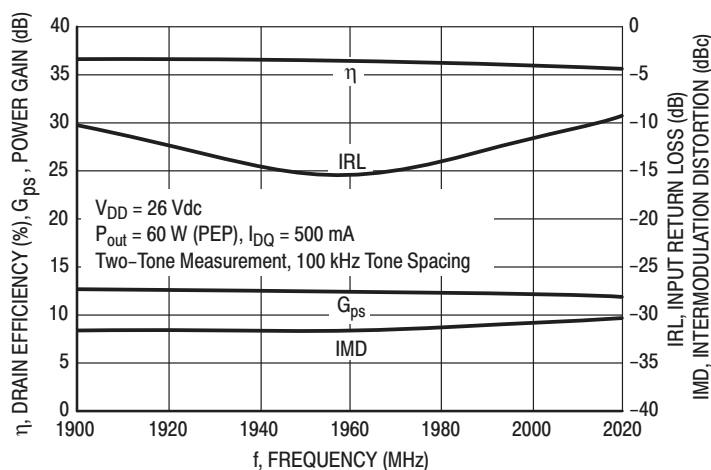


Figure 3. Class AB Broadband Circuit Performance

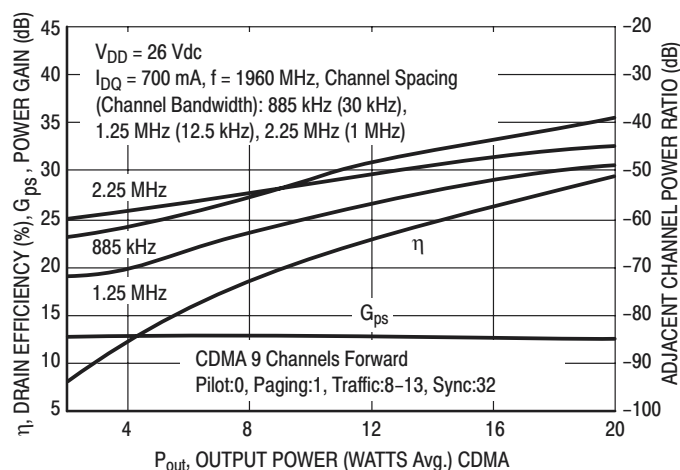


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

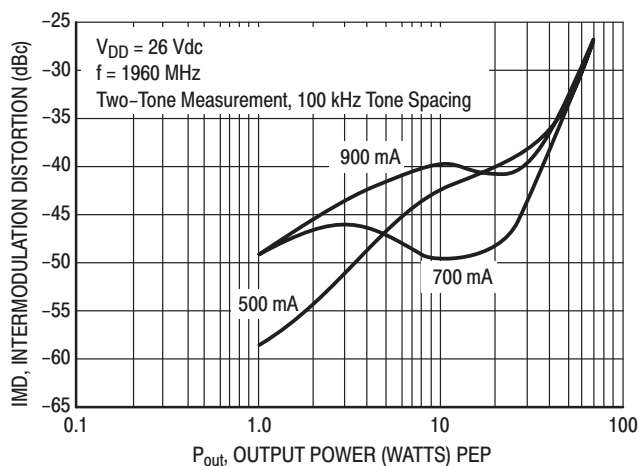


Figure 5. Intermodulation Distortion versus Output Power

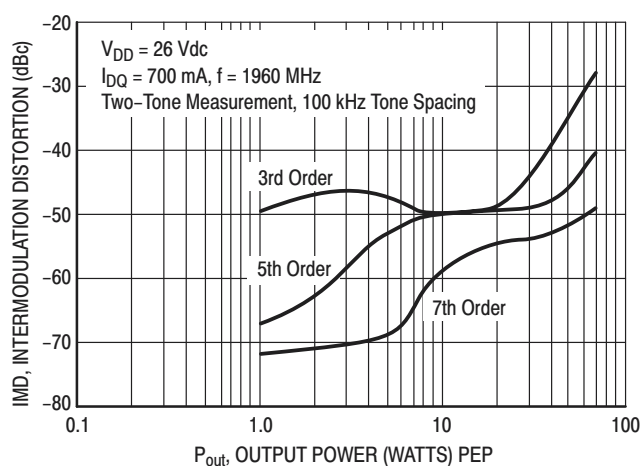


Figure 6. Intermodulation Products versus Output Power

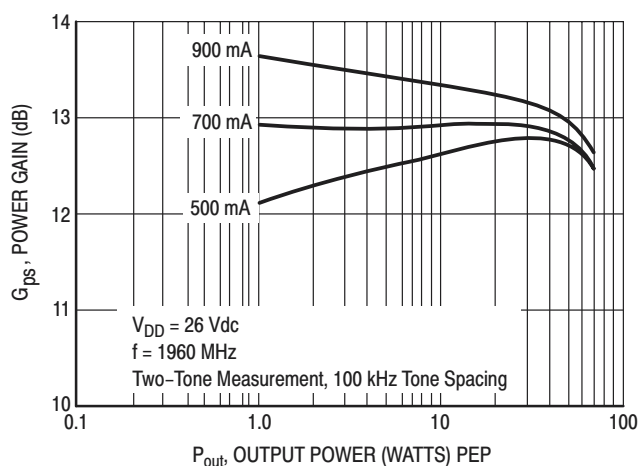


Figure 7. Power Gain versus Output Power

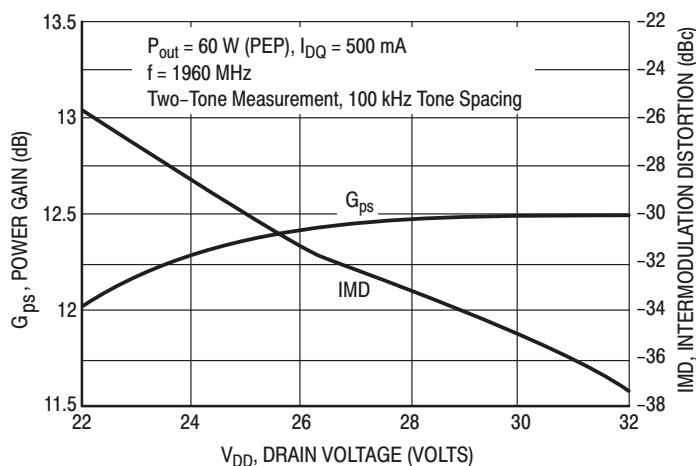
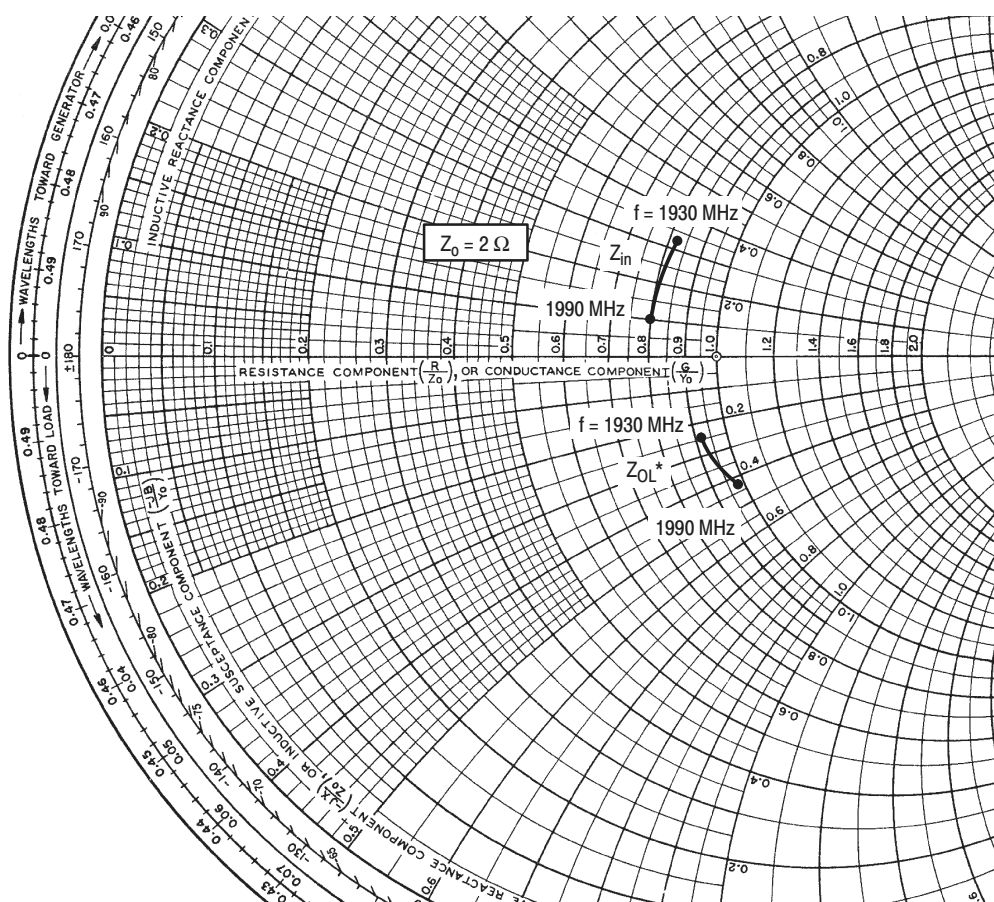


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 60 \text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1930	$1.65 + j0.67$	$1.85 - j0.50$
1960	$1.64 + j0.45$	$1.89 - j0.74$
1990	$1.60 + j0.20$	$1.96 - j0.94$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

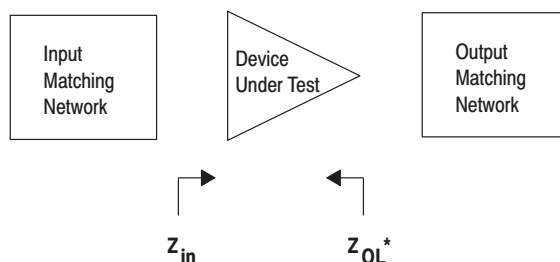


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

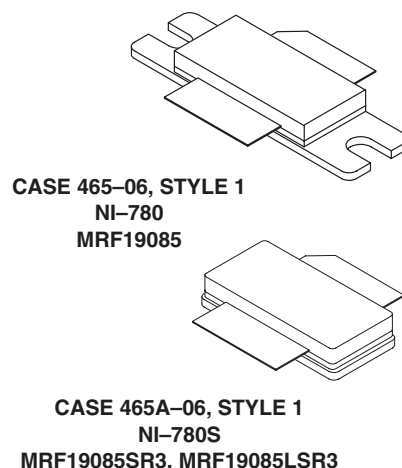
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications.

- Typical 2-Carrier N-CDMA Performance for $V_{DD} = 26$ Volts, $I_{DQ} = 850$ mA, $P_{out} = 18$ Watts Avg., $f_1 = 1960$ MHz, $f_2 = 1962.5$ MHz IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13) 1.2288 MHz Channel Bandwidth Carrier. Adjacent Channels Measured over a 30 kHz Bandwidth at $f_1 - 885$ KHz and $f_2 + 885$ kHz. Distortion Products Measured over 1.2288 MHz Bandwidth at $f_1 - 2.5$ MHz and $f_2 + 2.5$ MHz. Peak/Avg. = 9.8 dB @ 0.01% Probability on CCDF.
Output Power — 18 Watts Avg.
Power Gain — 13.0 dB
Efficiency — 23%
ACPR — -51 dB
IM3 — -36.5 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1.93 GHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

MRF19085
MRF19085R3
MRF19085SR3
MRF19085LSR3

1990 MHz, 90 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	273 1.56	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.79	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS (DC)

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 850 mAdc)	V _{GS(Q)}	2.5	3.5	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.18	0.210	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	6	—	S

DYNAMIC CHARACTERISTICS

Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{rss}	—	3.6	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–Carrier N–CDMA, 1.2288 MHz Channel Bandwidth Carriers.
Peak/Avg. Ratio = 9.8 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 18 W Avg., I _{DQ} = 850 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz)	G _{ps}	12	13	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 18 W Avg., I _{DQ} = 850 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz)	η	21	23	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 18 W Avg., I _{DQ} = 850 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz); IM3 measured over 1.2288 MHz bandwidth @ f ₁ –2.5 MHz and f ₂ = +2.5 MHz)	IMD	—	–36.5	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 26 Vdc, P _{out} = 18 W Avg., I _{DQ} = 850 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz); ACPR measured over 30 kHz bandwidth @ f ₁ –885 MHz and f ₂ = +885 MHz)	ACPR	—	–51	–48	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 18 W Avg., I _{DQ} = 850 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 90 W CW, I _{DQ} = 850 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 850\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	G_{ps}	—	13	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 850\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	η	—	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 850\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	IMD	—	−31	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 850\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	IRL	—	−12	—	dB
P_{out} , 1 dB Compression Point ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 850\text{ mA}$, $f = 1990\text{ MHz}$)	P1dB	—	90	—	W

Freescale Semiconductor, Inc.

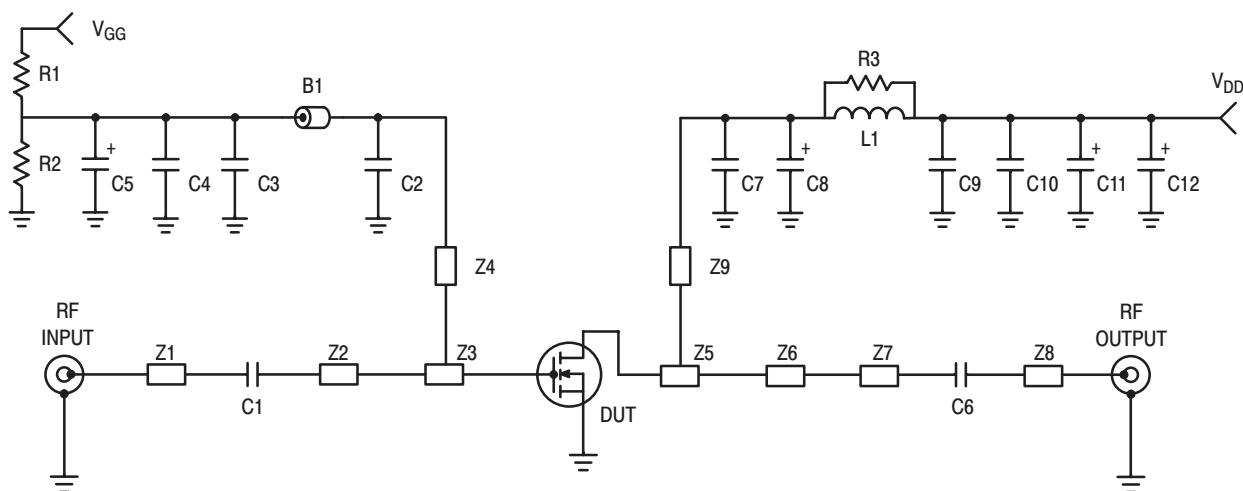


Figure 1. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Schematic

Table 1. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1	Short Ferrite Bead	2743019447	Fair Rite
C1	51 pF Chip Capacitor	100B510JCA500X	ATC
C2, C7	5.1 pF Chip Capacitors	100B5R1JCA500X	ATC
C3, C9	1000 pF Chip Capacitors	100B102JCA500X	ATC
C4, C10	0.1 μ F Chip Capacitors	CDR33BX104AKWS	Kemet
C5	0.1 μ F Tantalum Surface Mount Capacitor	T491C105M050	Kemet
C6	10 pF Chip Capacitor	100B100JCA500X	ATC
C8	10 μ F Tantalum Surface Mount Capacitor	T495X106K035AS4394	Kemet
C11, C12	22 μ F Tantalum Surface Mount Capacitors	T491X226K035AS4394	Kemet
L1	1 Turn, 20 AWG, 0.100" ID		Motorola
N1, N2	Type N Flange Mounts	3052-1648-10	Omni Spectra
R1	1.0 k Ω , 1/8 W Chip Resistor		
R2	220 k Ω , 1/8 W Chip Resistor		
R3	10 Ω , 1/8 W Chip Resistor		
Z1	Microstrip	0.750" x 0.0840"	
Z2	Microstrip	1.090" x 0.0840"	
Z3	Microstrip	0.400" x 1.400"	
Z4	Microstrip	0.520" x 0.050"	
Z5	Microstrip	0.540" x 1.133"	
Z6	Microstrip	0.400" x 0.140"	
Z7	Microstrip	0.555" x 0.0840"	
Z8	Microstrip	0.720" x 0.0840"	
Z9	Microstrip	0.560" x 0.070"	
Board	0.030" Glass Teflon [®]	GX-0300-55-22, $\epsilon_r = 2.55$	Keene
PCB	Etched Circuit Boards	MRF19085 Rev. 4	CMR

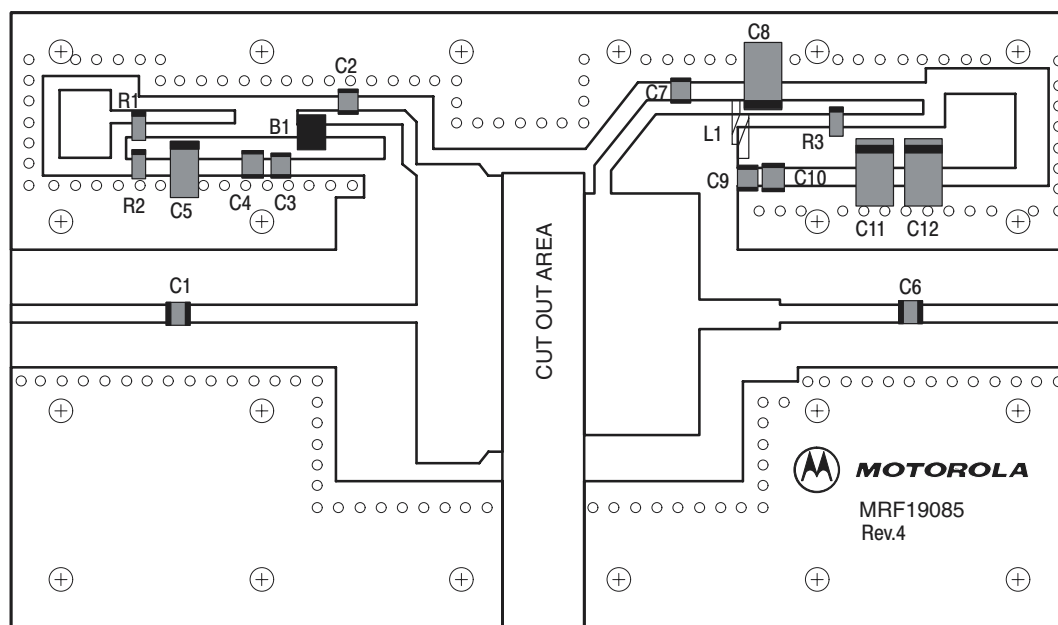


Figure 2. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

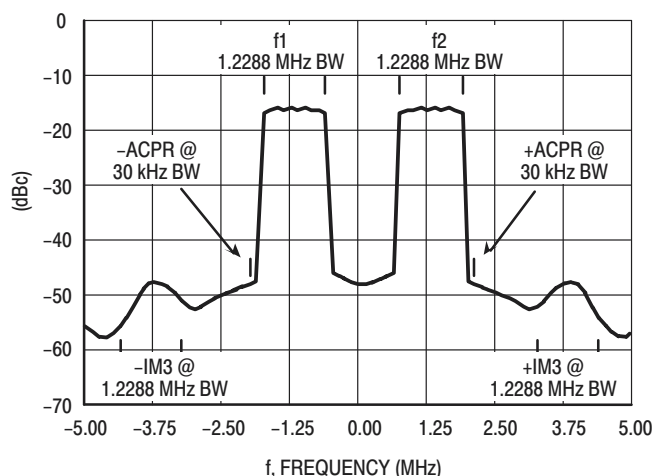


Figure 3. 2-Carrier N-CDMA Spectrum

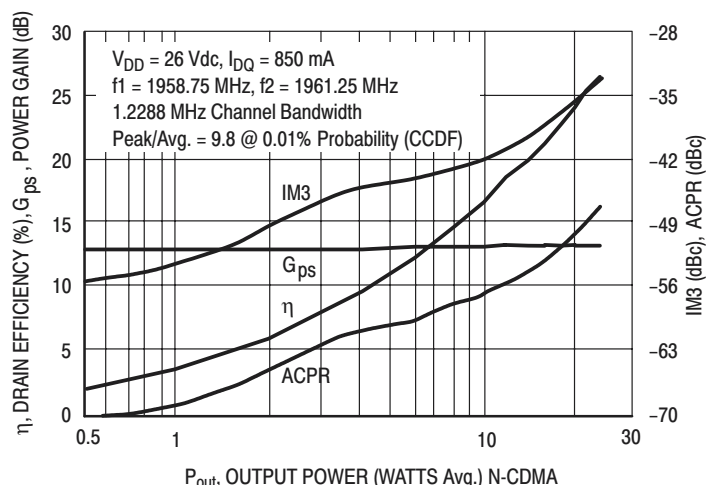


Figure 4. 2-Carrier N-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

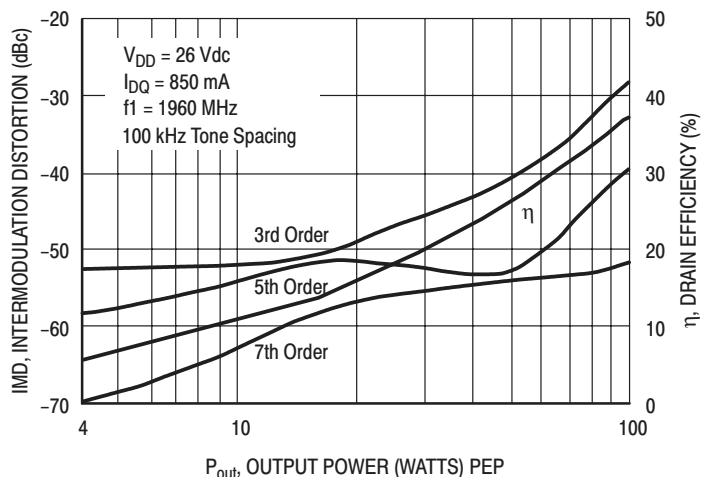


Figure 5. Intermodulation Distortion Products versus Output Power

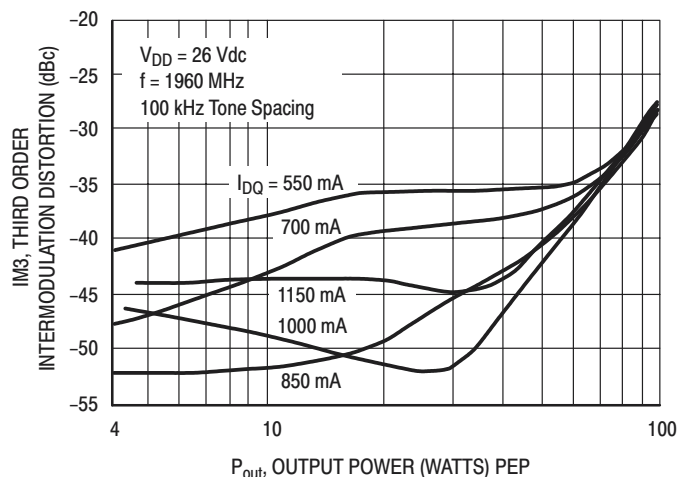


Figure 6. Third Order Intermodulation Distortion versus Output Power and I_{DQ}

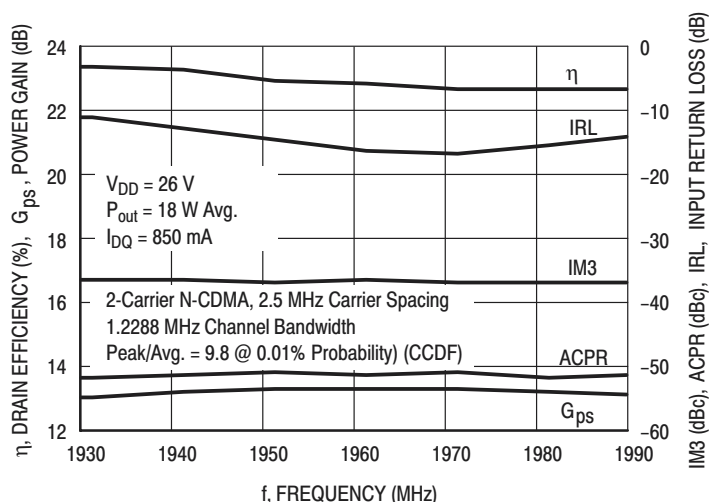


Figure 7. 2-Carrier N-CDMA Broadband Performance

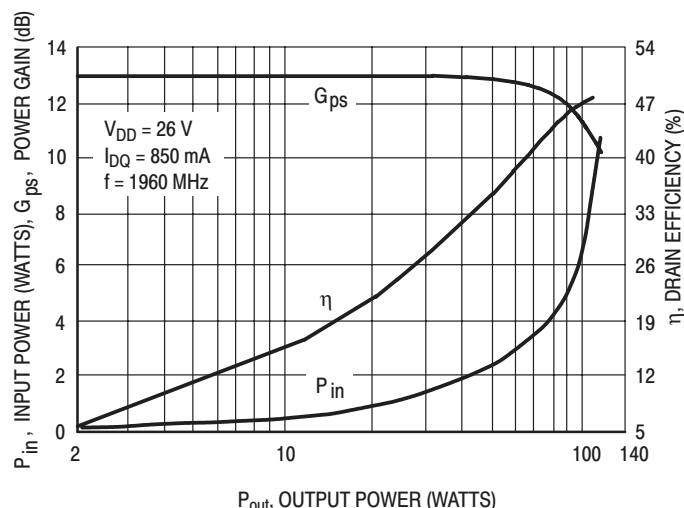


Figure 8. CW Performance

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

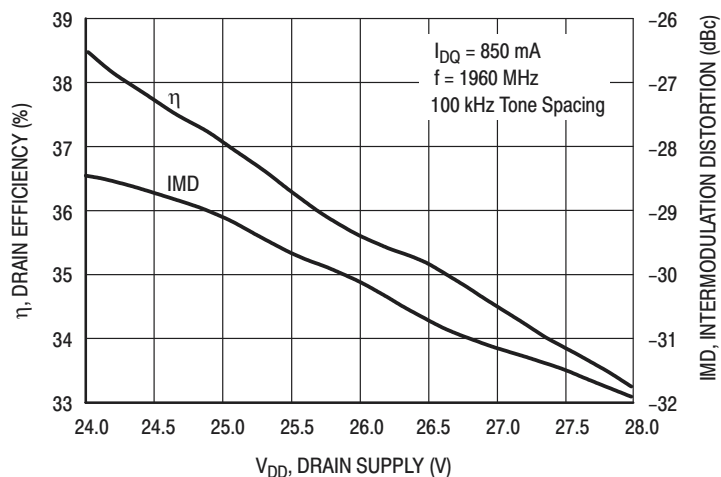


Figure 9. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

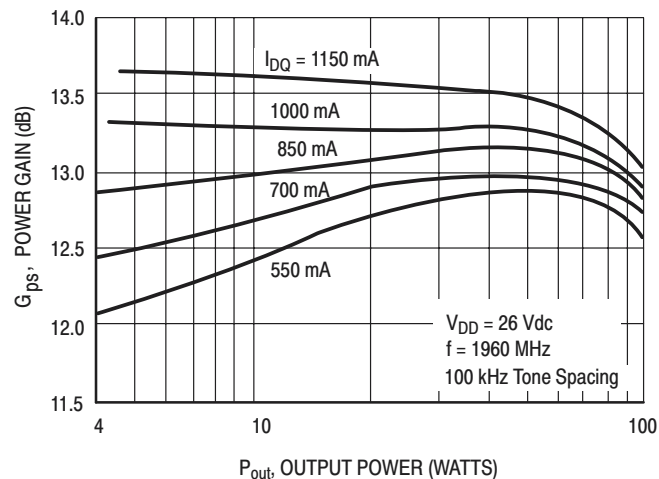


Figure 10. Two-Tone Power Gain versus Output Power

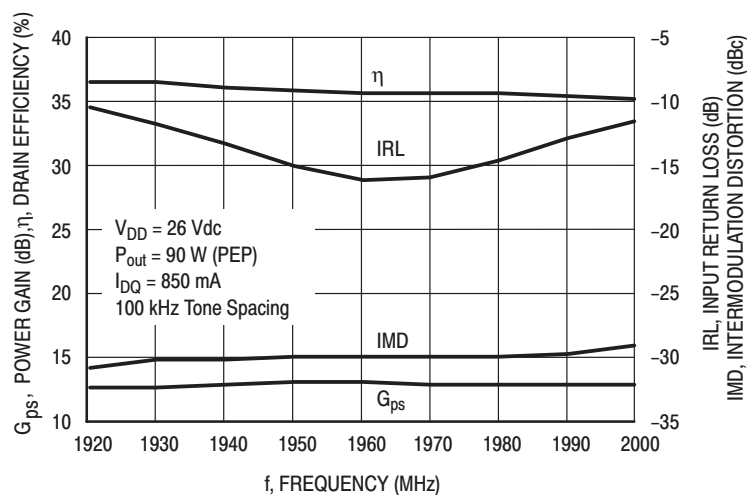
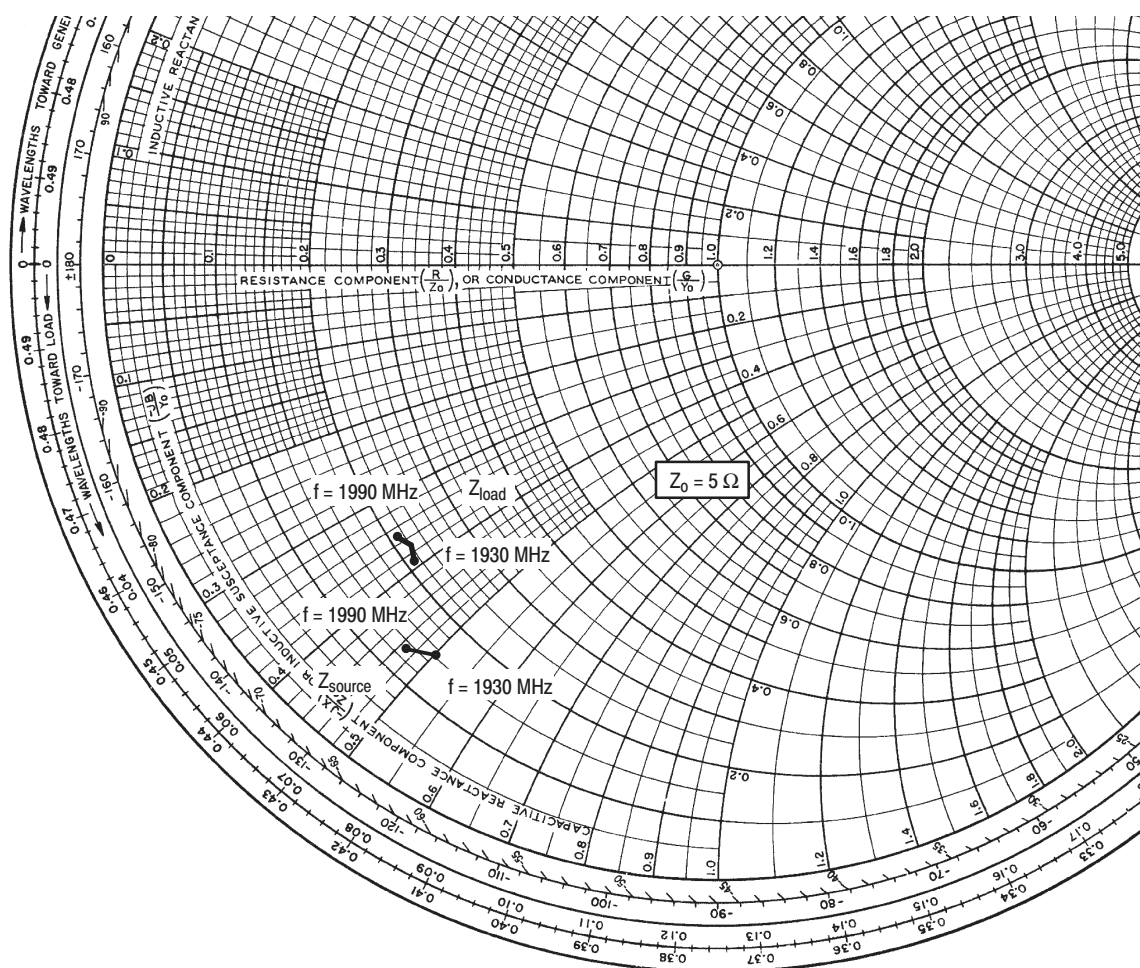


Figure 11. Two-Tone Broadband Performance



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 850 \text{ mA}$, $P_{out} = 18 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$0.75 - j2.50$	$1.05 - j1.95$
1960	$0.70 - j2.40$	$1.10 - j1.85$
1990	$0.65 - j2.35$	$1.05 - j1.75$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

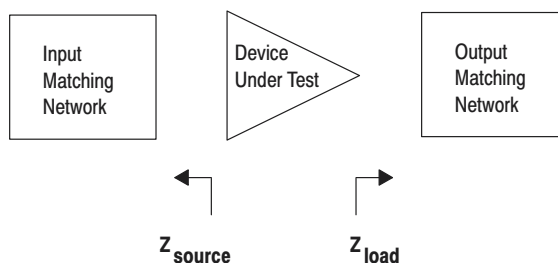


Figure 12. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

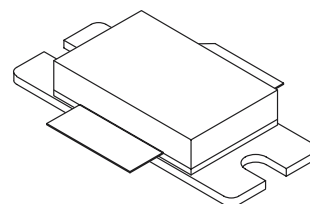
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for Class AB PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM, and multicarrier amplifier applications.

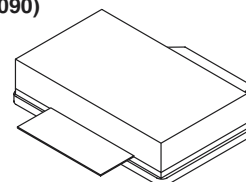
- Typical CDMA Performance: 1990 MHz, 26 Volts
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 9 Watts
Power Gain — 10 dB
Adjacent Channel Power —
885 kHz: -47 dBc @ 30 kHz BW
1.25 MHz: -55 dBc @ 12.5 kHz BW
2.25 MHz: -55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF19090
MRF19090S
MRF19090SR3

1990 MHz, 90 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465B-03, STYLE 1
(NI-880)
(MRF19090)



CASE 465C-02, STYLE 1
(NI-880S)
(MRF19090S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	270 1.54	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

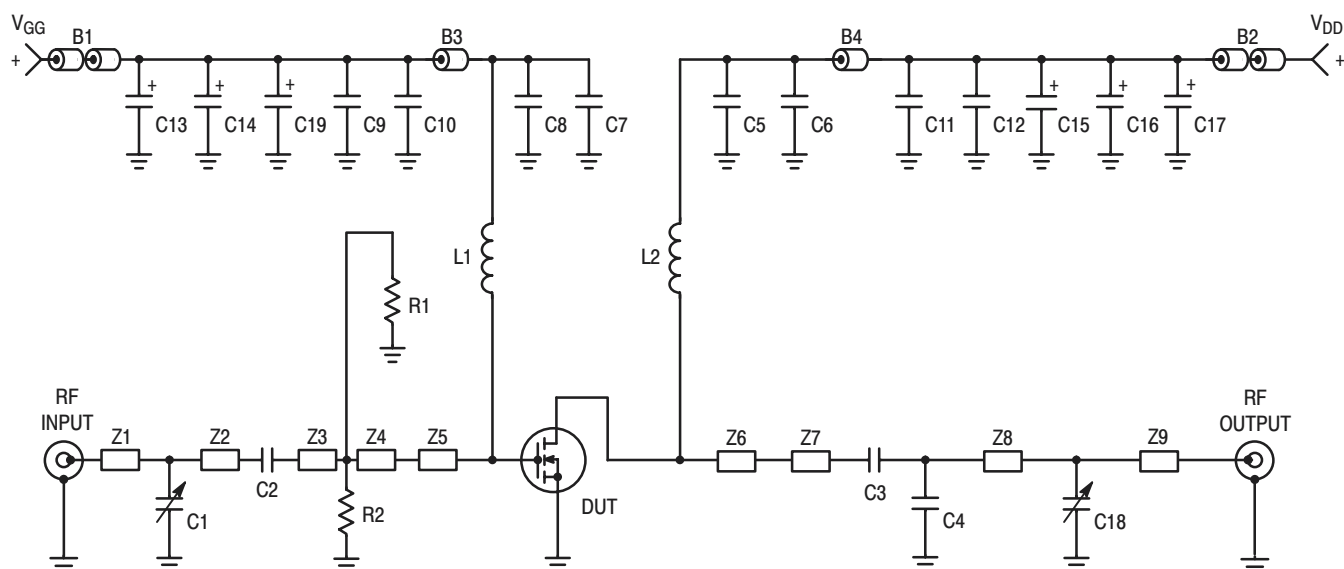
Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μA)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 Adc)	g _{fs}	—	7.2	—	S
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 750 mAdc)	V _{GS(Q)}	2.5	3.8	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.10	—	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 90 W PEP, I _{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	G _{ps}	10	11.5	—	dB
Two–Tone Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 90 W PEP, I _{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	η	33	35	—	%
3rd Order Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 90 W PEP, I _{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	–28	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 90 W PEP, I _{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P _{out} , 1 dB Compression Point (V _{DD} = 26 Vdc, P _{out} = 90 W CW, f = 1990 MHz)	P1dB	—	90	—	W
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 90 W CW, I _{DQ} = 750 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.



B1, B2	2 Ferrite Beads, Round, Ferroxcube #56-590-65-3B	L1, L2	8 Turns, #26 AWG, 0.085" OD, 0.330" Long, Copper Wire
B3, B34	Ferrite Beads, Surface Mount, Ferroxcube	R1, R2	270 Ω , 1/4 W Chip Resistors, Garrett Instruments #RM73B2B271JT
C1, C18	0.4 – 2.5 pF Variable Capacitors, Johanson Gigatrim #27285	Z1	ZO = 50 Ohms
C2, C5, C8	10 pF Chip Capacitors, B Case, ATC #100B100CCA500X	Z2	ZO = 50 Ohms, Lambda = 0.123
C3	12 pF Chip Capacitor, B Case, ATC #100B120CCA500X	Z3	ZO = 15.24 Ohms, Lambda = 0.0762
C4	0.3 pF Chip Capacitor, B Case, ATC #100B0R3CCA500X	Z4	ZO = 10.11 Ohms, Lambda = 0.0392
C6, C7	120 pF Chip Capacitors, B Case, ATC #100B12R1CCA500X	Z5	ZO = 6.34 Ohms, Lambda = 0.0711
C9, C12	0.1 μ F Chip Capacitors, Kemet #CDR33BX104AKWS	Z6	ZO = 5.02 Ohms, Lambda = 0.0476
C10, C11	1000 pF Chip Capacitors, B Case, ATC #100B102JCA50X	Z7	ZO = 5.54 Ohms, Lambda = 0.0972
C13, C17	22 μ F, 35 V Tantalum Chip Capacitors, Kemet #T491X226K035AS4394	Z8	ZO = 50.0 Ohms, Lambda = 0.194
C14, C16	10 μ F, 35 V Tantalum Chip Capacitors, Kemet #T495X106K035AS4394	Z9	ZO = 50.0 Ohms
C15, C19	1 μ F, 35 V Tantalum Chip Capacitors, Kemet #T495X105K035AS4394	Raw PCB Material	0.030" Glass Teflon [®] , ϵ_r = 2.55, 2 oz Copper, 3" x 5" Dimensions

Figure 1. MRF19090 Test Circuit Schematic

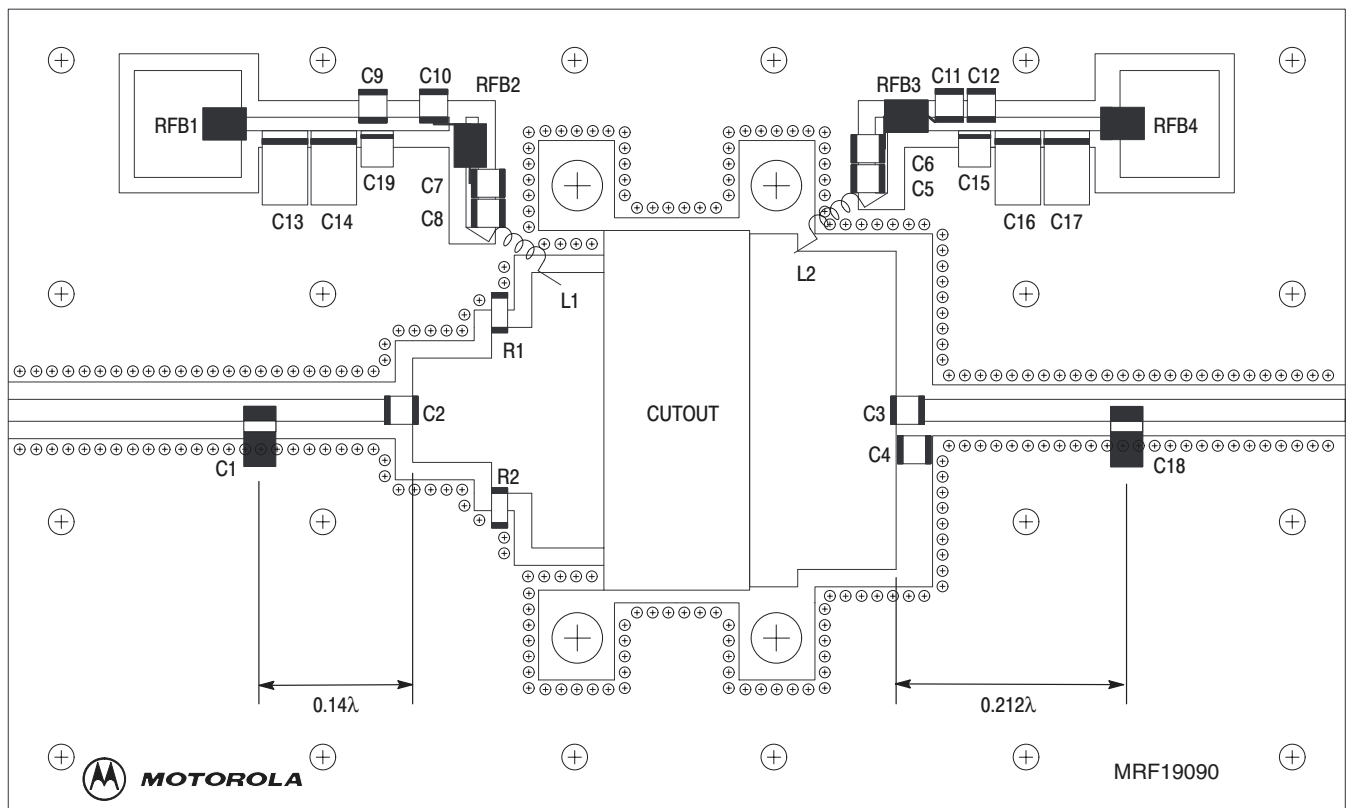


Figure 2. MRF19090 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

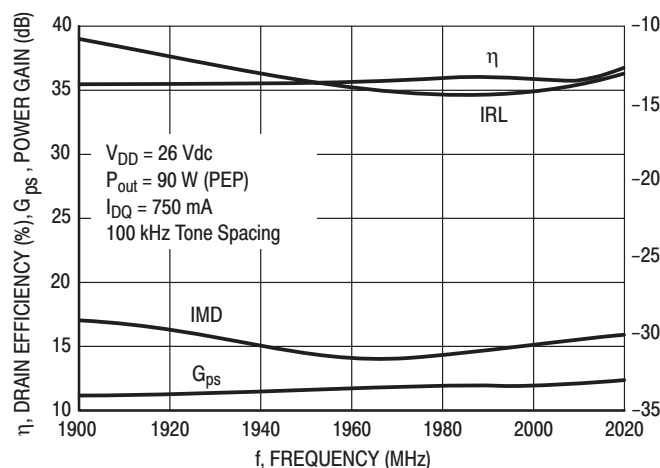


Figure 3. Class AB Performance versus Frequency

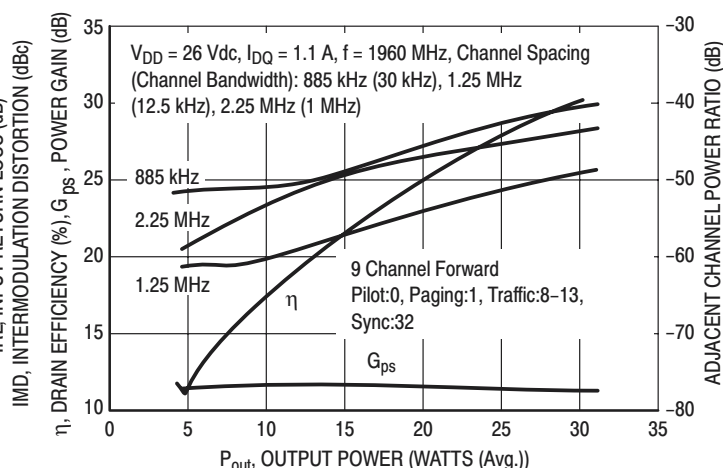


Figure 4. CDMA Performance ACPR, Gain and Drain Efficiency versus Output Power

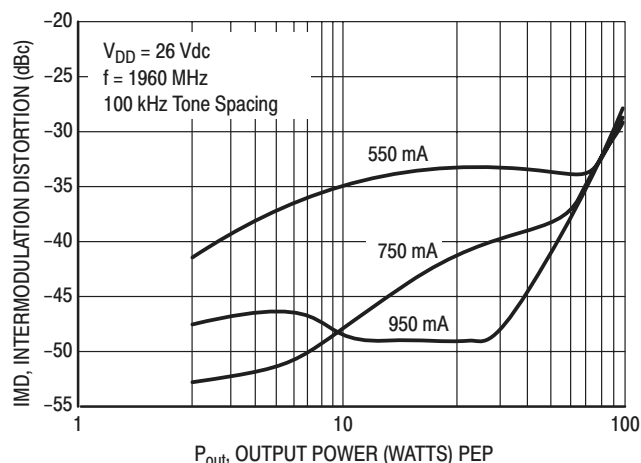


Figure 5. Third Order Intermodulation Distortion versus Output Power

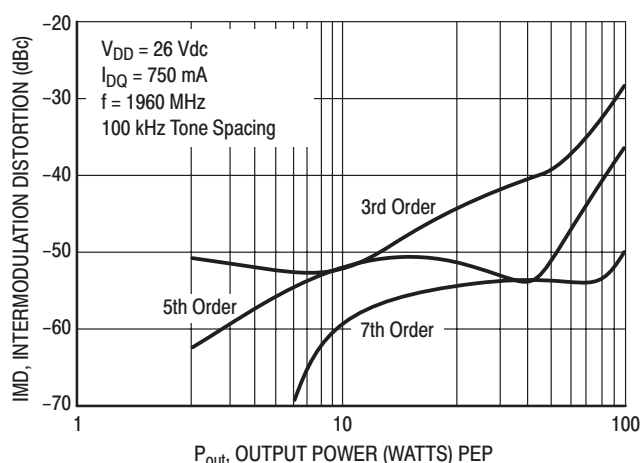


Figure 6. Intermodulation Products versus Output Power

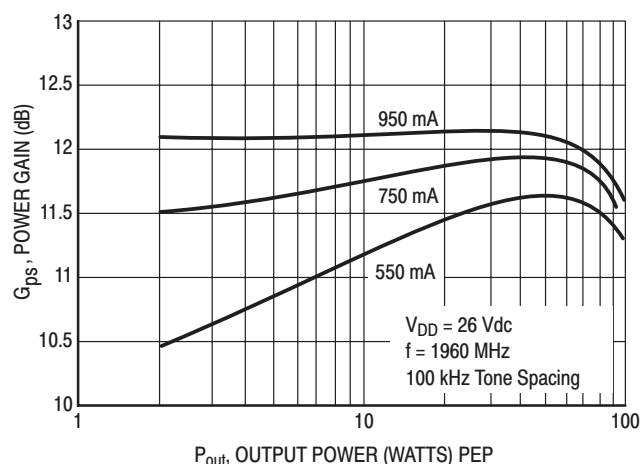


Figure 7. Power Gain versus Output Power

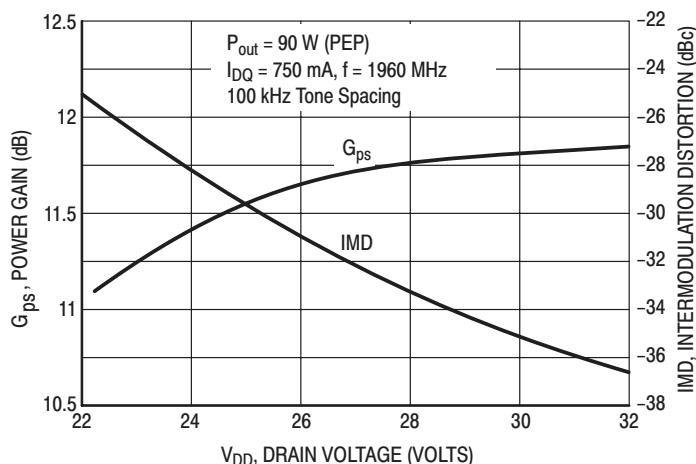
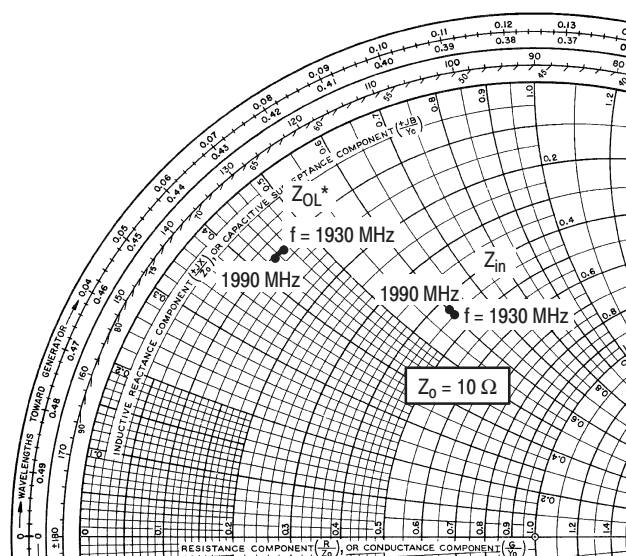


Figure 8. Third Order Intermodulation Distortion and Gain versus Supply Voltage



$V_{DD} = 26\text{ V}$, $I_{DQ} = 750\text{ mA}$, $P_{out} = 90\text{ Watts (PEP)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1930	$4.5 + j6.1$	$1.1 + j4.5$
1960	$4.4 + j6.0$	$1.1 + j4.4$
1990	$4.3 + j6.1$	$1.1 + j4.3$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

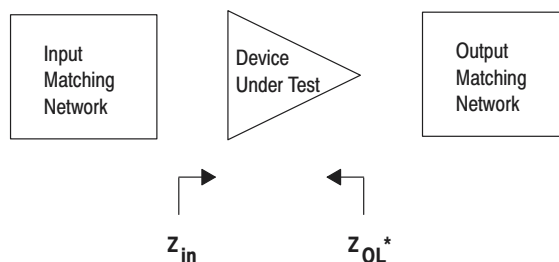


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

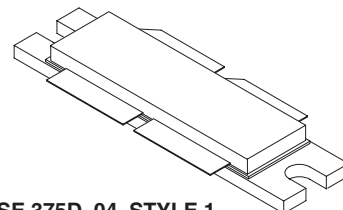
Designed for CDMA base station applications with frequencies from 1930 to 1990 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- CDMA Performance @ 1990 MHz, 26 Volts
 - IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
 - 885 kHz — -47 dBc @ 30 kHz BW
 - 1.25 MHz — -55 dBc @ 12.5 kHz BW
 - 2.25 MHz — -55 dBc @ 1 MHz BW
 - Output Power — 15 Watts (Avg.)
 - Power Gain — 11.7 dB
 - Efficiency — 16%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency, High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1990 MHz, 120 Watts (CW) Output Power
- S-Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

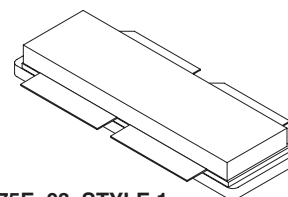
MRF19120

MRF19120S

1990 MHz, 120 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 375D-04, STYLE 1
NI-1230
MRF19120



CASE 375E-03, STYLE 1
NI-1230S
MRF19120S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	389 2.22	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 10 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
ON CHARACTERISTICS (1)					
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.8	—	S
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 200 μA)	V _{GS(th)}	2.5	3	3.8	Vdc
Gate Quiescent Voltage (V _{DS} = 26 V, I _D = 500 mA)	V _{GS(Q)}	3	3.9	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 V, I _D = 2 A)	V _{DS(on)}	—	0.38	0.5	Vdc
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	2.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)					
Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, MRF19120 f1 = 1990.0 MHz, f2 = 1990.1 MHz) MRF19120S	G _{ps}	10.7 10.5	11.7 11.7	— —	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f1 = 1990.0 MHz, f2 = 1990.1 MHz)	η	30	34	—	%
Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, MRF19120 f1 = 1990.0 MHz, f2 = 1990.1 MHz) MRF19120S	IMD	— —	–31 –31	–28 –27	dB
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f1 = 1990.0 MHz, f2 = 1990.1 MHz)	IRL	—	–12	–9	dB
Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G _{ps}	—	11.7	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	—	34	—	%
Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IMD	—	–31	—	dB
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IRL	—	–14	—	dB
Power Output, 1 dB Compression Point (V _{DD} = 26 Vdc, CW, I _{DQ} = 2 × 500 mA, f1 = 1990.0 MHz)	P1dB	—	120	—	Watts
Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 120 W CW, I _{DQ} = 2 × 500 mA, f1 = 1990.0 MHz)	G _{ps}	—	11	—	dB

(1) Each side of device measured separately.

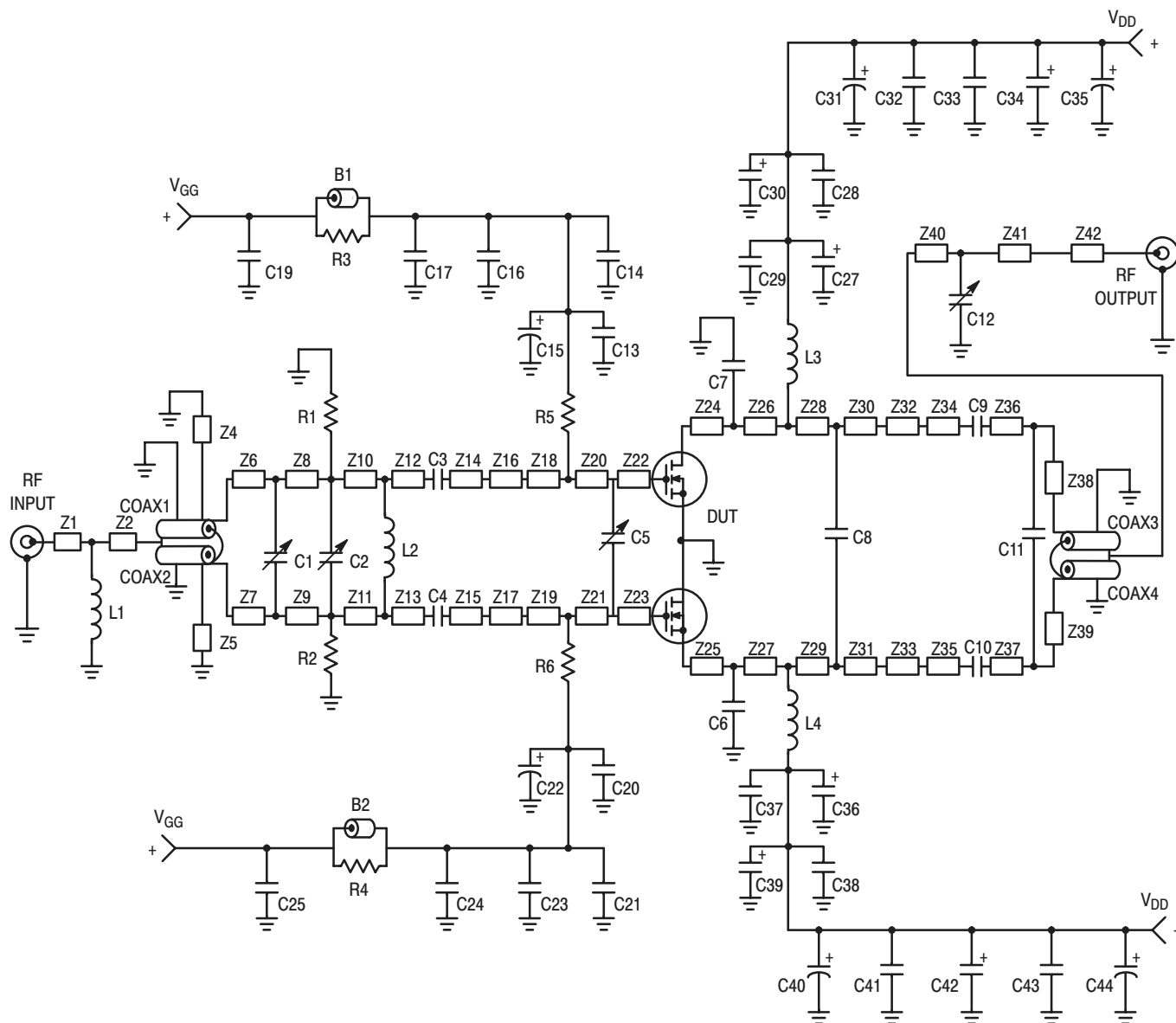
(2) Device measured in push–pull configuration.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) (continued)					
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W CW}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 1990.0\text{ MHz}$)	η	—	45	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 120\text{ W CW}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f = 1990\text{ MHz}$, $VSWR = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(2) Device measured in push–pull configuration.



B1, B2	Ferrite Beads, Fair Rite
C1, C2	0.6 – 4.5 pF Variable Capacitors, Johanson Gigatrim
C3, C4, C9, C10	10 pF Chip Capacitors, B Case, ATC
C5, C12	0.4 – 2.5 pF Variable Capacitors, Johanson Gigatrim
C6, C7	2.0 pF Chip Capacitors, B Case, ATC
C8	1.1 pF Chip Capacitor, B Case, ATC
C11	0.1 pF Chip Capacitor, B Case, ATC
C13, C20, C29, C37	5.1 pF Chip Capacitors, B Case, ATC
C14, C21, C28, C38	91 pF Chip Capacitors, B Case, ATC
C15, C22, C31, C40	100 μ F, 50 V Electrolytic Capacitors, Sprague
C16, C23, C33, C43	0.039 μ F Chip Capacitors, B Case, ATC
C17, C24, C32, C41	1000 pF Chip Capacitors, B Case, ATC
C19, C25	0.020 μ F Chip Capacitors, B Case, ATC
C27, C34, C36, C42	22 μ F, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
C30, C39	1.0 μ F, 35 V Tantalum Surface Mount Chip Capacitors, Kemet
C35, C44	470 μ F, 63 V Electrolytic Capacitors, Sprague
Coax1, Coax2	25 Ω , Semi Rigid Coax, 70 mil OD, 1.05" Long
Coax3, Coax4	50 Ω , Semi Rigid Coax, 85 mil OD, 1.05" Long
L1	5.0 nH, Minispring Inductor, Coilcraft
L2	8.0 nH, Minispring Inductor, Coilcraft
L3, L4	5.60 nH, Microspring Inductors, Coilcraft
R1, R2	1 k Ω , 1/2 W Fixed Metal Film Resistors, Dale
R3, R4	270 Ω , 1/8 W Fixed Film Chip Resistors, Dale
R5, R6	1.0 k Ω , 1/8 W Fixed Film Chip Resistors, Dale
Z1	0.150" x 0.080" Microstrip

Z2	0.320" x 0.080" Microstrip
Z4, Z5	1.050" x 0.080" Microstrip
Z6, Z7	0.120" x 0.080" Microstrip
Z8, Z9	0.140" x 0.080" Microstrip
Z10, Z11	0.610" x 0.080" Microstrip
Z12, Z13	0.135" x 0.080" Microstrip
Z14, Z15	0.130" x 0.080" Microstrip
Z16, Z17	0.300" x 0.350" Microstrip
Z18, Z19	0.150" x 0.500" Microstrip
Z20, Z21	0.075" x 0.500" Microstrip
Z22, Z23	0.330" x 0.500" Microstrip
Z24, Z25	0.100" x 0.550" Microstrip
Z26, Z27	0.175" x 0.550" Microstrip
Z28, Z29	0.045" x 0.550" Microstrip
Z30, Z31	0.190" x 0.325" Microstrip
Z32, Z33	0.080" x 0.325" Microstrip
Z34, Z35	0.515" x 0.080" Microstrip
Z36, Z37	0.020" x 0.080" Microstrip
Z38, Z39	0.565" x 0.080" Microstrip
Z40	0.100" x 0.080" Microstrip
Z41	0.470" x 0.080" Microstrip
Z42	0.100" x 0.080" Microstrip
Board Material	0.03" Teflon [®] , $\epsilon_r = 2.55$ Copper Clad, 2 oz. Cu
Connectors	N-Type Panel Mount, Stripline

Figure 1. 1.93 – 1.99 GHz Broadband Test Circuit Schematic

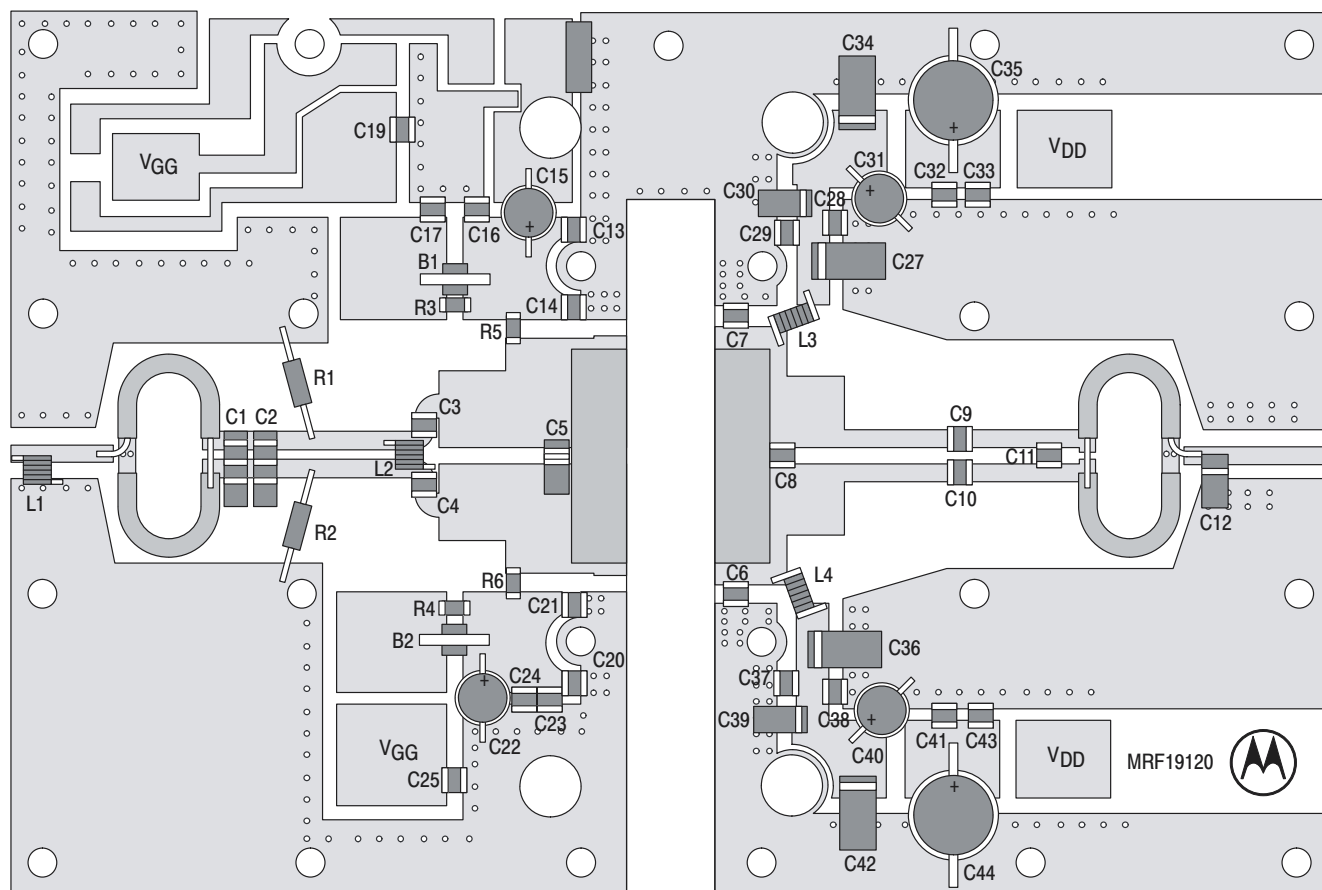


Figure 2. MRF19120 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

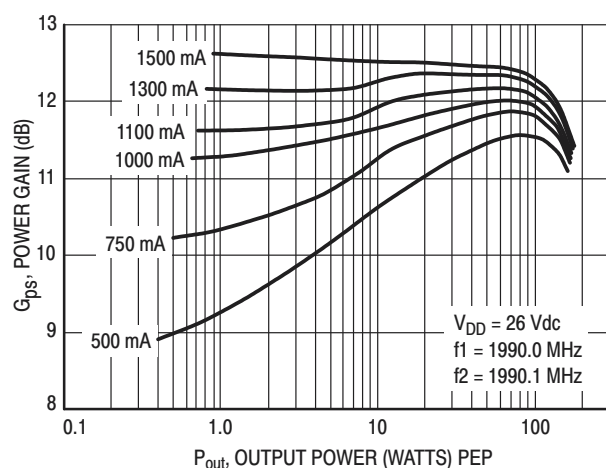


Figure 3. Power Gain versus Output Power

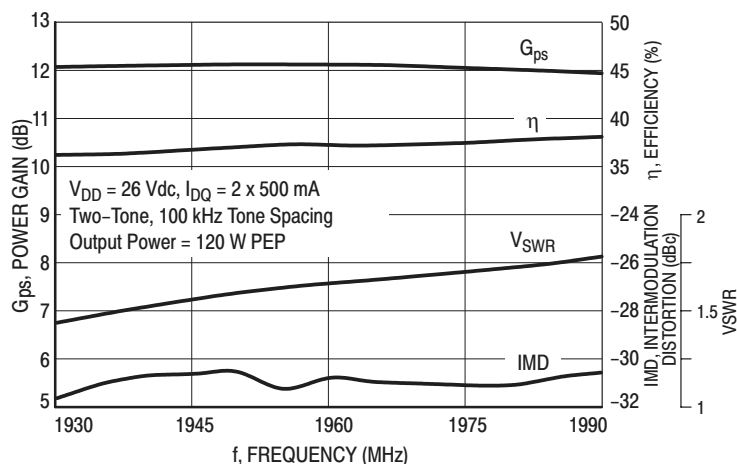


Figure 4. Class AB Broadband Circuit Performance

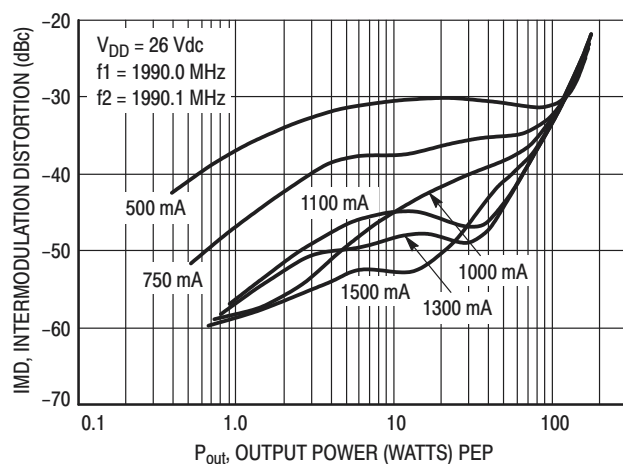


Figure 5. Intermodulation Distortion versus Output Power

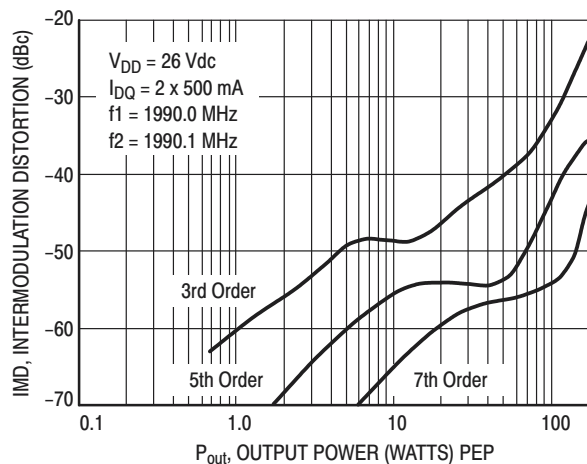


Figure 6. Intermodulation Distortion Products versus Output Power

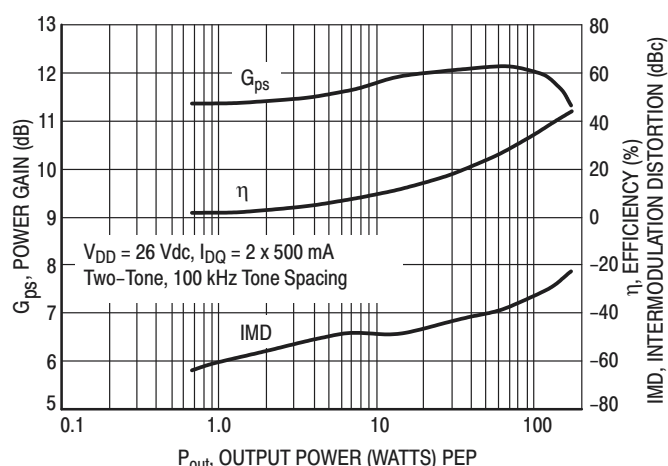


Figure 7. Power Gain, Efficiency, and IMD versus Output Power

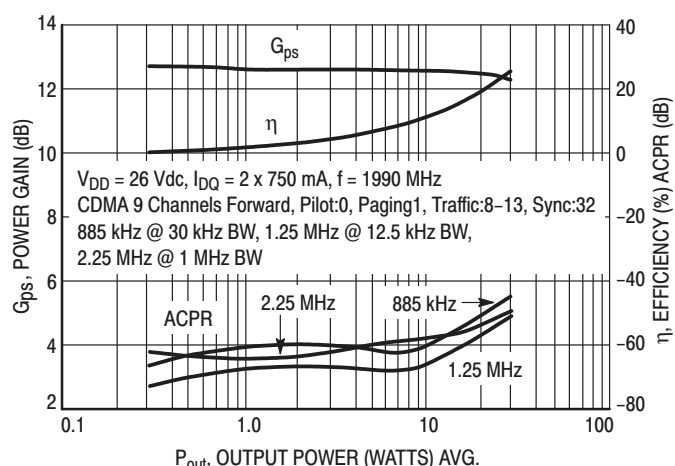
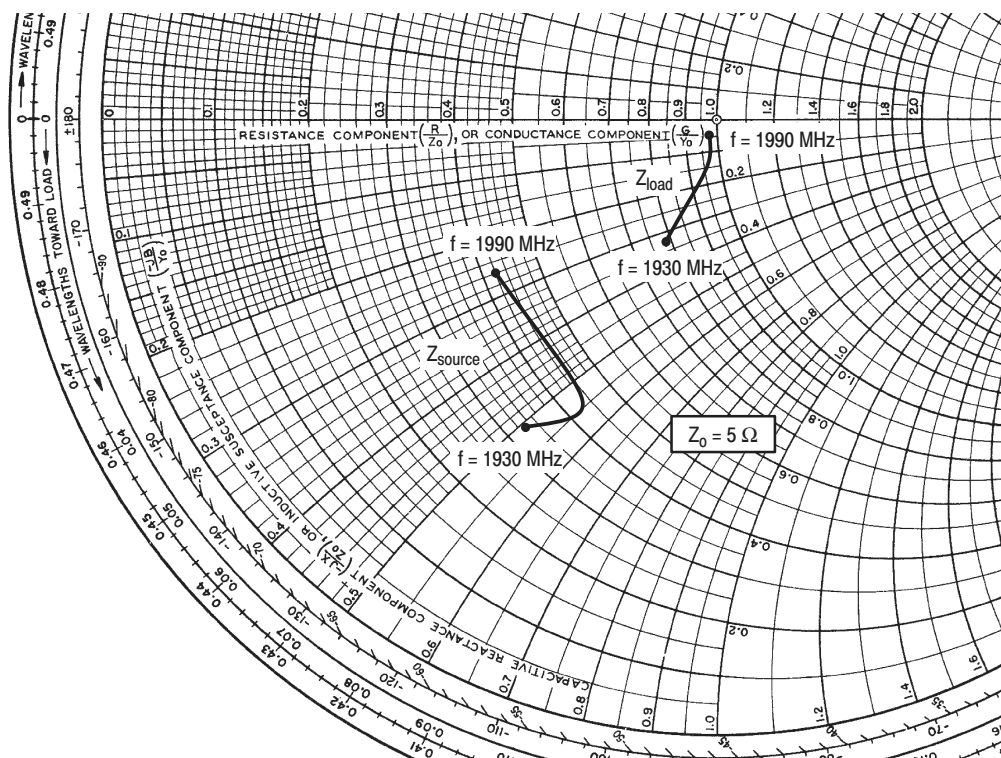


Figure 8. Power Gain, Efficiency, and ACPR versus Output Power



$V_{\text{DD}} = 26 \text{ V}$, $I_{\text{DQ}} = 2 \times 500 \text{ mA}$, $P_{\text{out}} = 120 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$1.64 - j2.6$	$3.9 - j1.7$
1960	$2.10 - j2.8$	$4.8 - j0.8$
1990	$2.10 - j1.4$	$4.9 - j0.3$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

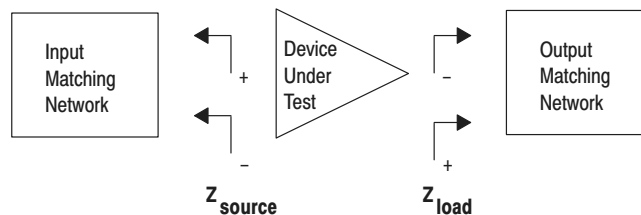


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

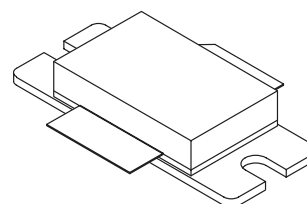
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications.

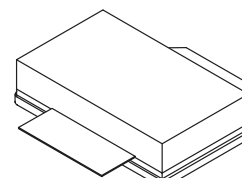
- Typical 2-Carrier N-CDMA Performance for $V_{DD} = 26$ Volts, $I_{DQ} = 1300$ mA, $f_1 = 1958.75$ MHz, $f_2 = 1961.25$ MHz IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13) 1.2288 MHz Channel Bandwidth Carrier. Adjacent Channels Measured over a 30 kHz Bandwidth at $f_1 - 885$ kHz and $f_2 + 885$ kHz. Distortion Products Measured over 1.2288 MHz Bandwidth at $f_1 - 2.5$ MHz and $f_2 + 2.5$ MHz. Peak/Avg. = 9.8 dB @ 0.01% Probability on CCDF.
 Output Power — 24 Watts Avg.
 Power Gain — 13.6 dB
 Efficiency — 22%
 ACPR — -51 dB
 IM3 — -37.0 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1990 MHz, 125 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF19125
MRF19125S
MRF19125SR3

1990 MHz, 125 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465B-03, STYLE 1
NI-880
MRF19125



CASE 465C-02, STYLE 1
NI-880S
MRF19125S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	330 1.89	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.53	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc

ON CHARACTERISTICS

Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 Adc)	g _{fs}	—	9	—	S
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 1300 mAdc)	V _{GS(Q)}	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 3 Adc)	V _{DS(on)}	—	0.185	0.21	Vdc

DYNAMIC CHARACTERISTICS

Reverse Transfer Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	5.4	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture) 2–Carrier N–CDMA, 1.2288 MHz Channel Bandwidth Carriers. Peak/Avg = 9.8 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V _{DD} = 26 Vdc, P _{out} = 24 W Avg, I _{DQ} = 1300 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz)	G _{ps}	12	13.5	—	dB
Drain Efficiency (V _{DD} = 26 Vdc, P _{out} = 24 W Avg, I _{DQ} = 1300 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz)	η	19	22	—	%
Intermodulation Distortion (V _{DD} = 26 Vdc, P _{out} = 24 W Avg, I _{DQ} = 1300 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz; IM3 measured over 1.2288 MHz Bandwidth at f ₁ –2.5 MHz and f ₂ +2.5 MHz)	IMD	—	–37	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 26 Vdc, P _{out} = 24 W Avg, I _{DQ} = 1300 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz; ACPR measured over 30 kHz Bandwidth at f ₁ –885 MHz and f ₂ +885 MHz)	ACPR	—	–51	–47	dBc
Input Return Loss (V _{DD} = 26 Vdc, P _{out} = 24 W Avg, I _{DQ} = 1300 mA, f ₁ = 1930 MHz, f ₂ = 1932.5 MHz and f ₁ = 1987.5 MHz, f ₂ = 1990 MHz)	IRL	—	–13	–9	dB
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 125 W CW, I _{DQ} = 1300 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 125\text{ W PEP}$, $I_{DQ} = 1300\text{ mA}$, $f_1 = 1930\text{ MHz}$, $f_2 = 1990\text{ MHz}$, Tone Spacing = 100 kHz)	G_{ps}	—	13.5	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 125\text{ W PEP}$, $I_{DQ} = 1300\text{ mA}$, $f_1 = 1930\text{ MHz}$, $f_2 = 1990\text{ MHz}$, Tone Spacing = 100 kHz)	η	—	35	—	%
Third Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 125\text{ W PEP}$, $I_{DQ} = 1300\text{ mA}$, $f_1 = 1930\text{ MHz}$, $f_2 = 1990\text{ MHz}$, Tone Spacing = 100 kHz)	IMD	—	-30	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 125\text{ W PEP}$, $I_{DQ} = 1300\text{ mA}$, $f_1 = 1930\text{ MHz}$, $f_2 = 1990\text{ MHz}$, Tone Spacing = 100 kHz)	IRL	—	-13	—	dB
P_{out} , 1 dB Compression Point ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 1300\text{ mA}$, $f = 1990\text{ MHz}$)	P1dB	—	130	—	W

Freescale Semiconductor, Inc.

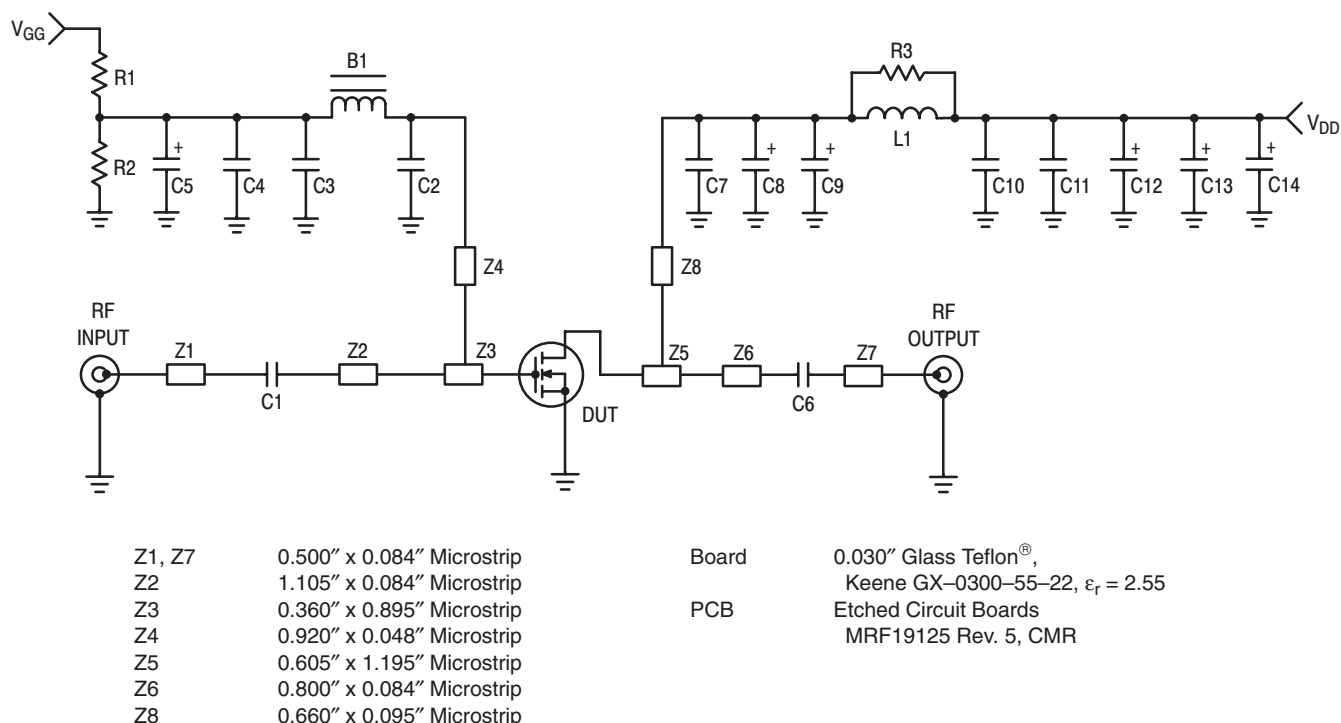


Figure 1. MRF19125 Test Circuit Schematic

Table 1. MRF19125 Test Circuit Component Designations and Values

Designators	Description
B1	Short Ferrite Bead, Fair Rite #2743019447
C1	51 pF Chip Capacitor, ATC #100B510JCA500X
C2, C7	5.1 pF Chip Capacitors, ATC #100B5R1JCA500X
C3, C10	1000 pF Chip Capacitors, ATC #100B102JCA500X
C4, C11	0.1 μ F Chip Capacitors, Kemet #CDR33BX104AKWS
C5	0.1 μ F Tantalum Chip Capacitor, Kemet #T491C105M050
C6	10 pF Chip Capacitor, ATC #100B100JCA500X
C8	10 μ F Tantalum Chip Capacitor, Kemet #T491X106K035AS4394
C9, C12, C13, C14	22 μ F Tantalum Chip Capacitors, Kemet #T491X226K035AS4394
L1	1 Turn, #20 AWG, 0.100" ID, Motorola
N1, N2	Type N Flange Mounts, Omni Spectra #3052-1648-10
R1	1.0 k Ω , 1/8 W Chip Resistor
R2	220 k Ω , 1/8 W Chip Resistor
R3	10 Ω , 1/8 W Chip Resistor

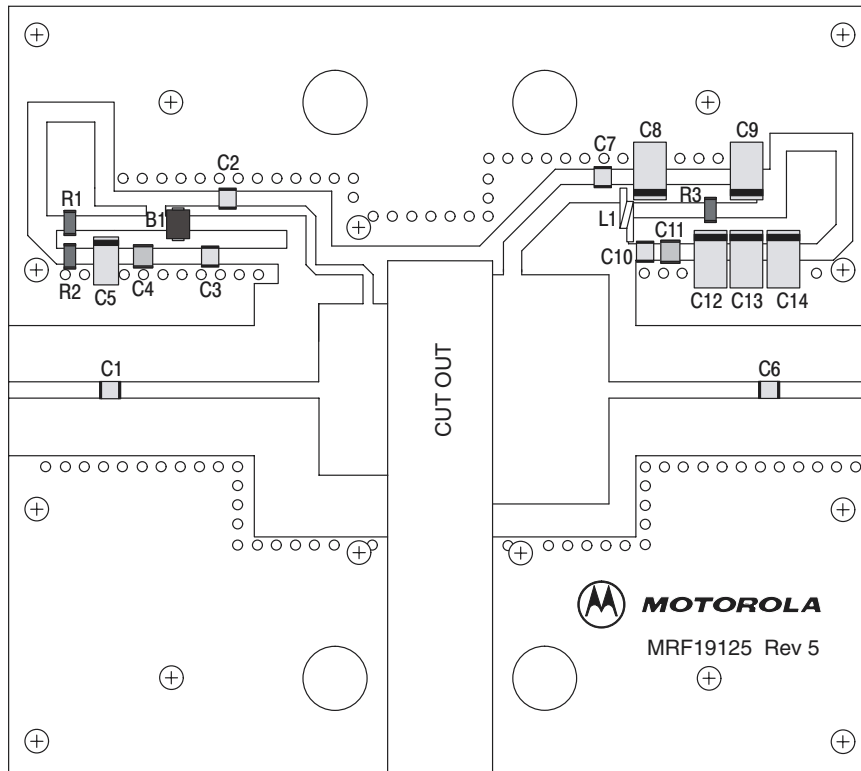


Figure 2. MRF19125 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

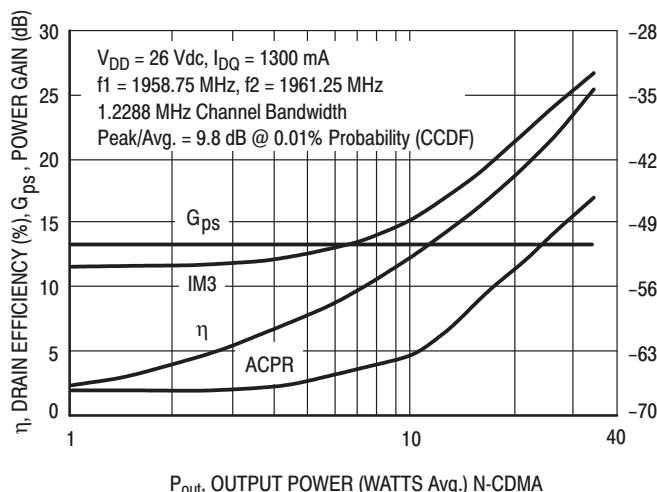


Figure 3. 2-Carrier CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

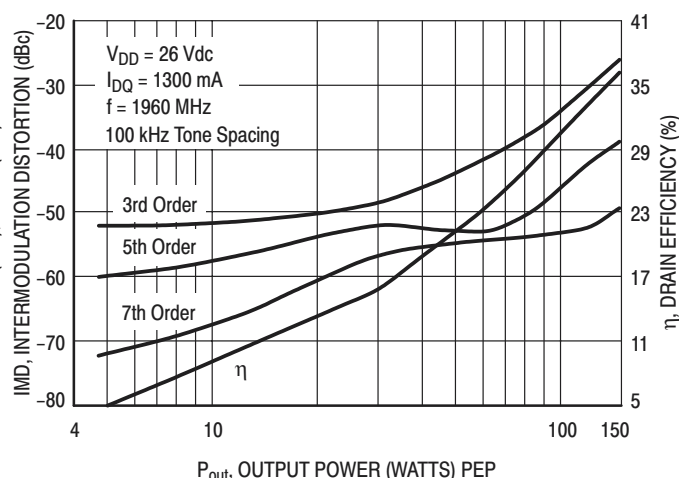


Figure 4. Intermodulation Distortion Products versus Output Power

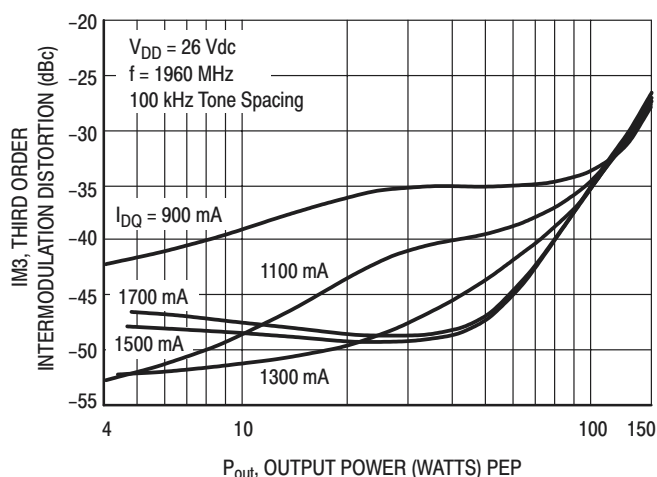


Figure 5. Third Order Intermodulation Distortion versus Output Power

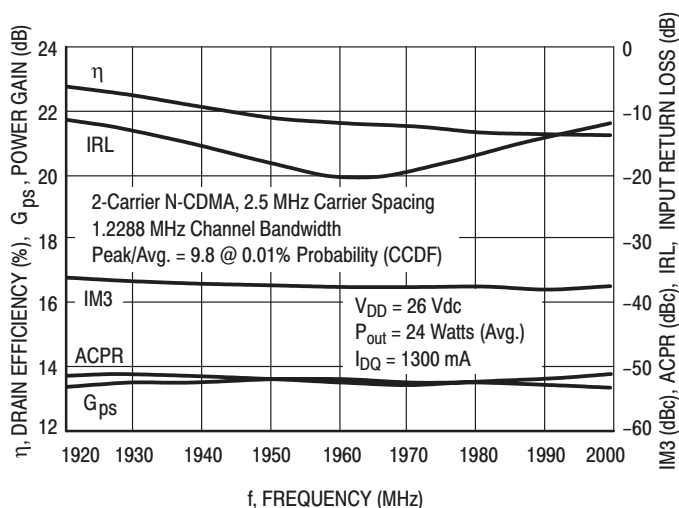


Figure 6. 2-Carrier N-CDMA Broadband Performance

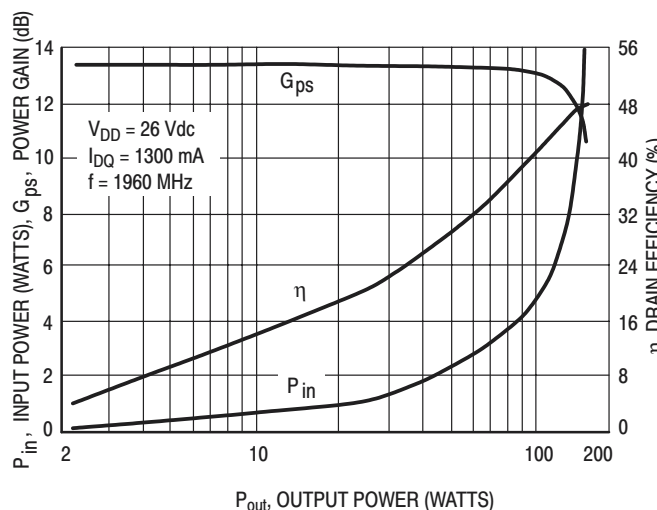


Figure 7. CW Performance

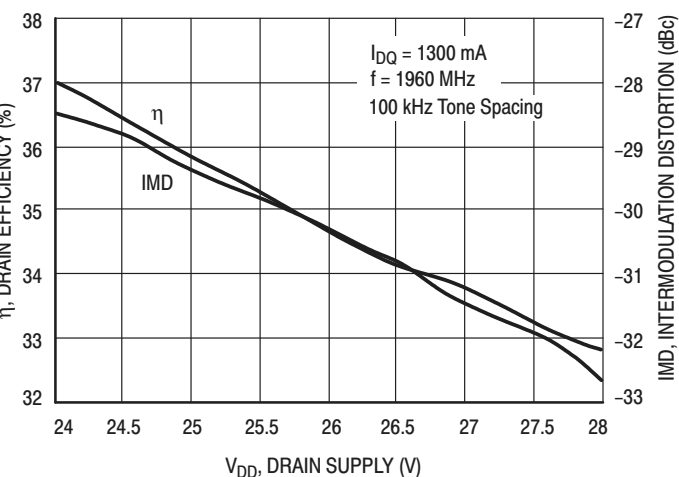


Figure 8. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

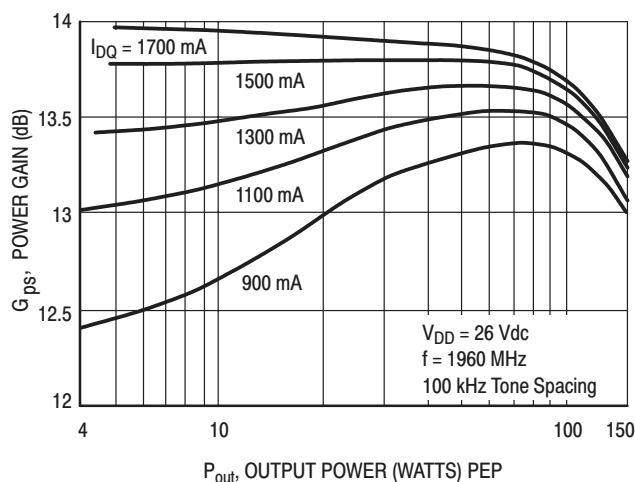


Figure 9. Two-Tone Power Gain versus Output Power

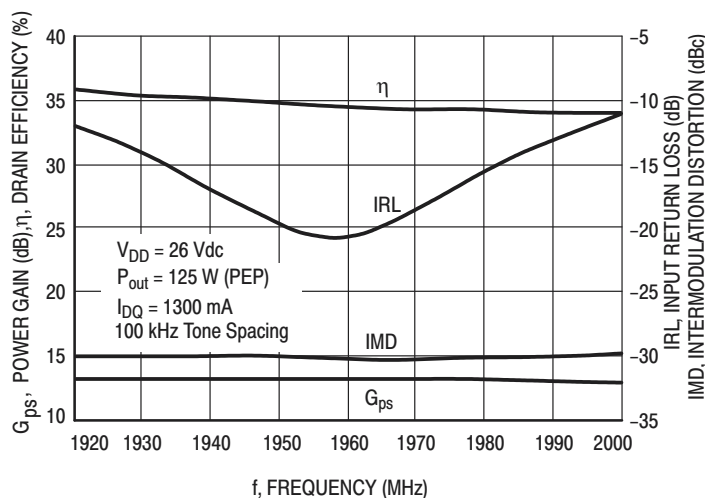


Figure 10. Two-Tone Broadband Performance

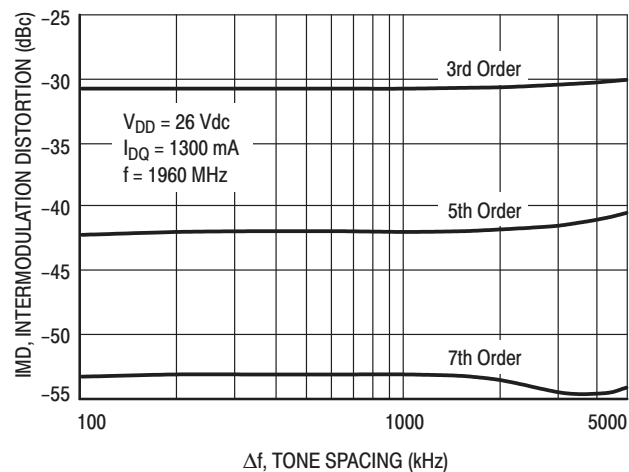


Figure 11. Intermodulation Distortion Products versus Two-Tone Tone Spacing

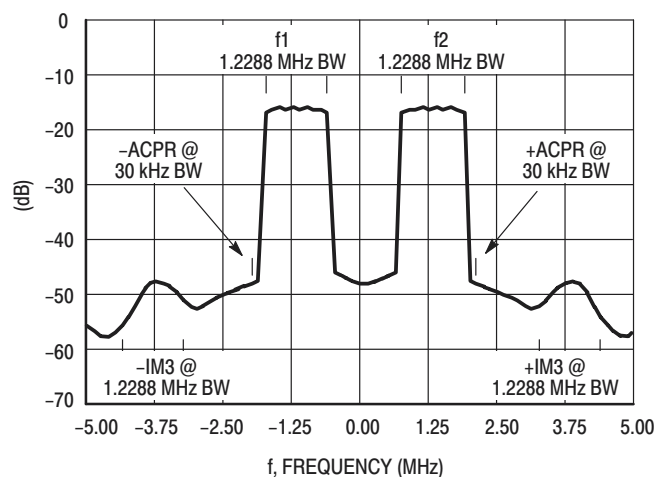
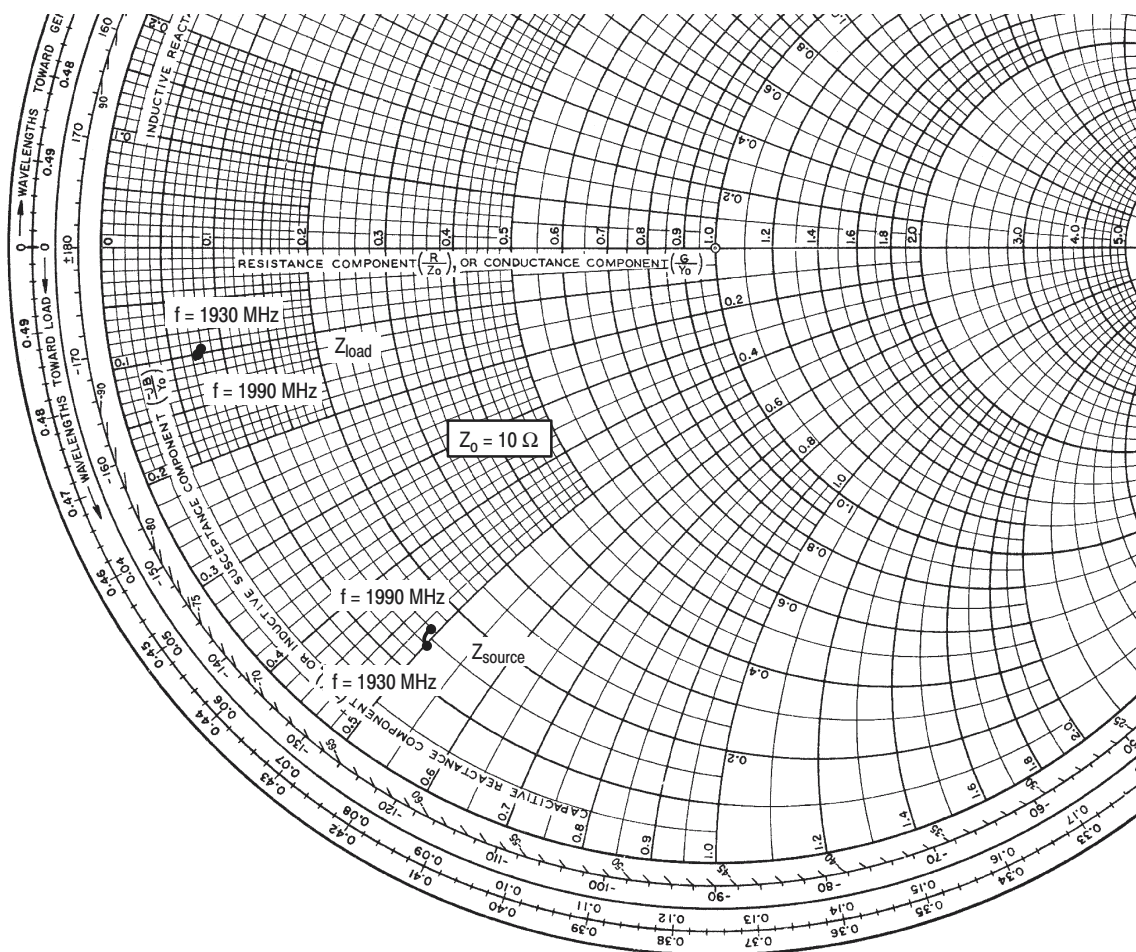


Figure 12. 2-Carrier N-CDMA Spectrum



$V_{DD} = 26\text{ V}$, $I_{DQ} = 1300\text{ mA}$, $P_{out} = 24\text{ W (Avg.)}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$1.43 - j5.01$	$0.75 - j0.93$
1960	$1.51 - j4.88$	$0.71 - j0.89$
1990	$1.56 - j4.93$	$0.68 - j1.02$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

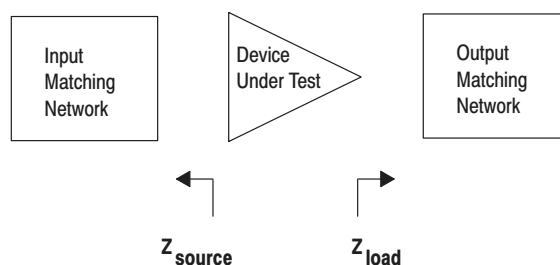


Figure 13. Series Equivalent Input and Output Impedance

The RF MOSFET Line

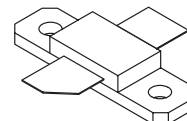
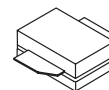
RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF21010R1
MRF21010LSR1

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical W-CDMA Performance: -45 dBc ACPR, 2140 MHz, 28 Volts, 5 MHz Offset/4.096 MHz BW, 15 DTCH
 Output Power — 2.1 Watts
 Power Gain — 13.5 dB
 Efficiency — 21%
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR @ 28 Vdc, 2170 MHz, 10 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 Inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

2170 MHz, 10 W, 28 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs

CASE 360B-05, STYLE 1
NI-360
MRF21010R1

CASE 360C-05, STYLE 1
NI-360S
MRF21010LSR1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	43.75 0.25	W W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.5	$^\circ\text{C/W}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 10 μA)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 50 μA)	V _{GS(th)}	2.5	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 V, I _D = 100 mA)	V _{GS(Q)}	2.5	4	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 V, I _D = 0.5 A)	V _{DS(on)}	—	0.4	0.5	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 1 A)	g _{fs}	—	0.95	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	1	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 10 W PEP, I _{DQ} = 100 mA, f ₁ = 2110 MHz, f ₂ = 2170 MHz, Tone Spacing = 100 KHz)	G _{ps}	12	13.5	—	dB
Two–Tone Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 10 W PEP, I _{DQ} = 100 mA, f ₁ = 2110 MHz, f ₂ = 2170 MHz, Tone Spacing = 100 KHz)	η	31	35	—	%
Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 10 W PEP, I _{DQ} = 100 mA, f ₁ = 2110 MHz, f ₂ = 2170 MHz, Tone Spacing = 100 KHz)	IMD	—	–35	–30	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 10 W PEP, I _{DQ} = 100 mA, f ₁ = 2110 MHz, f ₂ = 2170 MHz, Tone Spacing = 100 KHz)	IRL	—	–12	–10	dB
Output Power, 1 dB Compression Point, CW (V _{DD} = 28 Vdc, I _{DQ} = 100 mA, f = 2170 MHz)	P _{1dB}	—	11	—	W
Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 10 W CW, I _{DQ} = 100 mA, f = 2170 MHz)	G _{ps}	—	12	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 10 W CW, I _{DQ} = 100 mA, f = 2170 MHz)	η	—	42	—	%
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 10 W CW, I _{DQ} = 100 mA, f = 2170 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

Freescale Semiconductor, Inc.

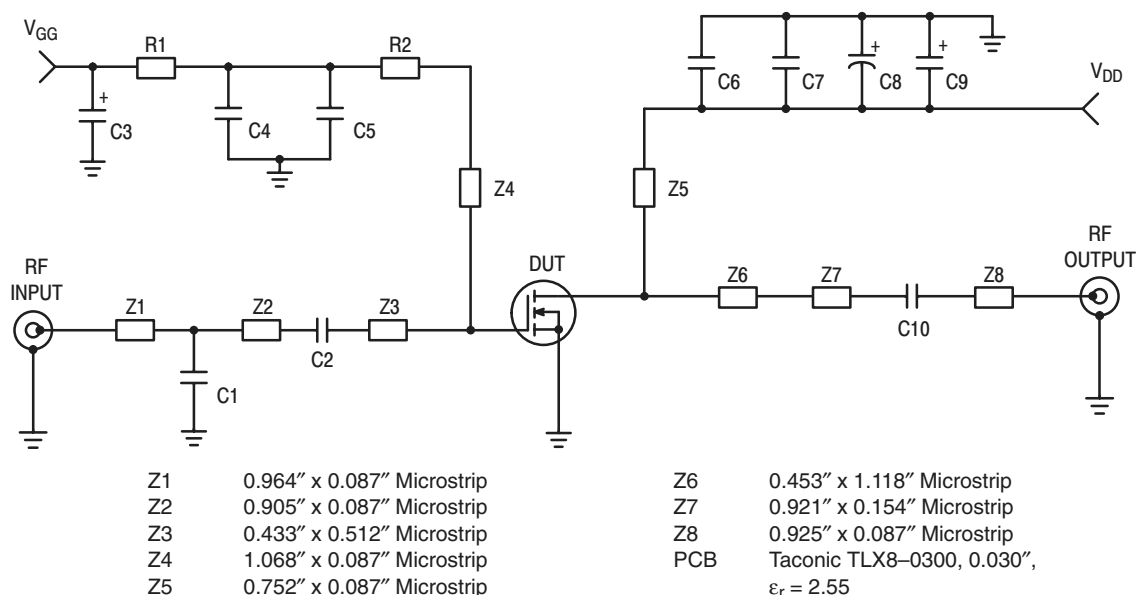


Figure 1. MRF21010 Test Circuit Schematic

Table 1. MRF21010 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1 *	(eared) 2.2 pF Chip Capacitor, B Case	100B2R2BW	ATC
	(earless) 1.8 pF Chip Capacitor, B Case	100B1R8BW	ATC
C2	0.5 pF Chip Capacitor, B Case	100B0R5BW	ATC
C3, C9	10 μ F, 35 V Tantalum Chip Capacitors	293D106X9035D2T	Sprague-Vishay
C4, C7	1 nF Chip Capacitors, B Case	100B102JW	ATC
C5, C6	5.6 pF Chip Capacitors, B Case	100B5R6BW	ATC
C8	470 μ F, 63 V Electrolytic Capacitor		
C10	10 pF Chip Capacitor, B Case	100B100GW	ATC
N1, N2	Type N Connector Flange Mounts	3052-1648-10	Macom
R1	1.0 k Ω Chip Resistor (0805)		
R2	12 Ω Chip Resistor (0805)		

* Piece part depending on eared / earless version of the device.

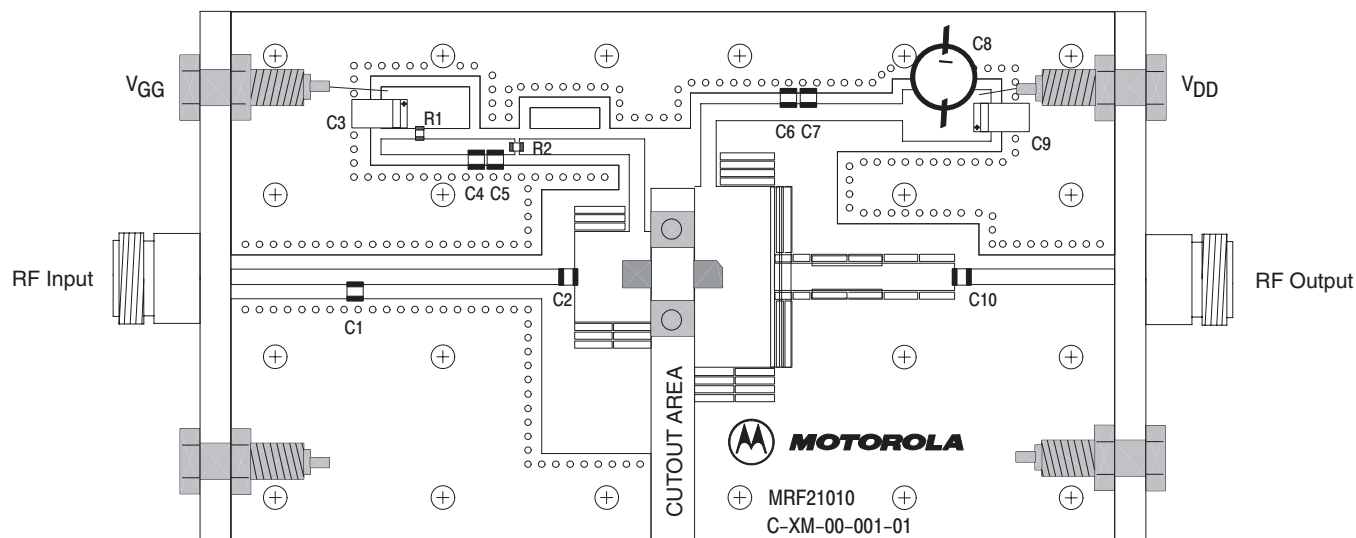


Figure 2. MRF21010 Test Circuit Component Layout

Freescale Semiconductor, Inc.

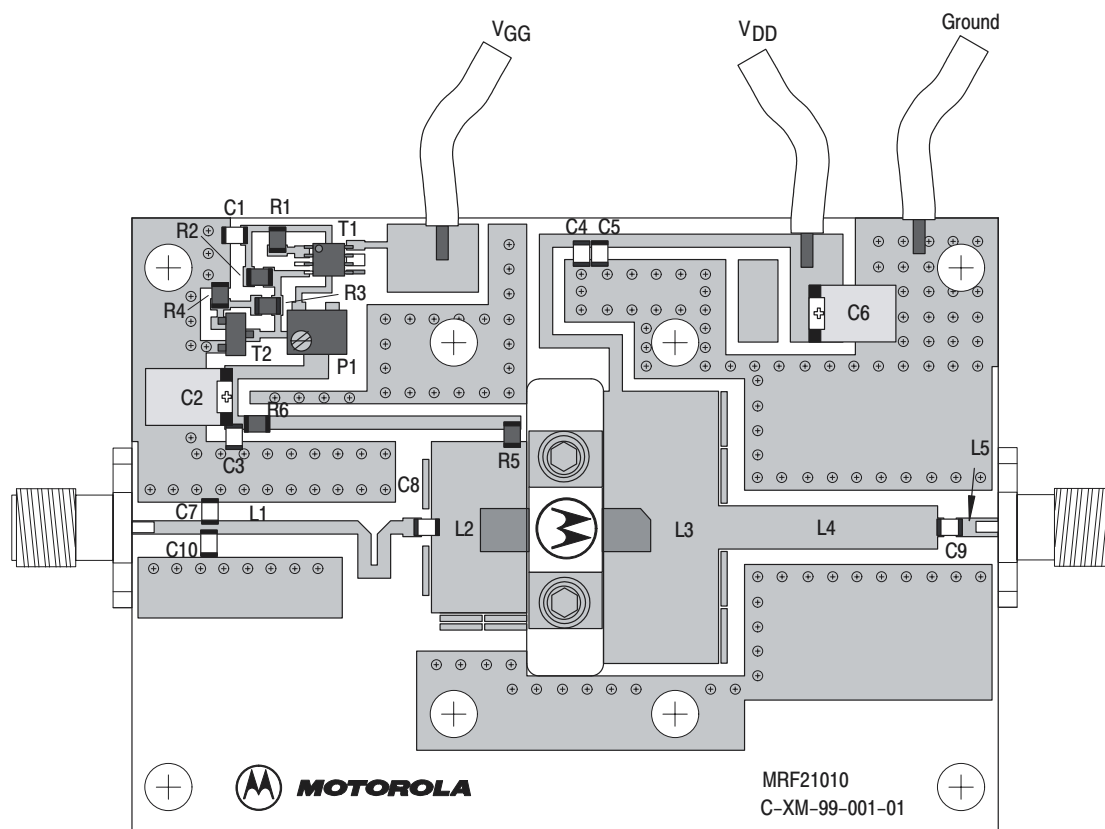


Figure 3. MRF21010 Demonstration Board Component Layout

Table 2. MRF21010 Demonstration Board Component Designations and Values

Designators	Description
C1	1 μ F Chip Capacitor (0805), AVX #08053G105ZATEA
C2, C6	10 μ F, 35 V Tantalum Capacitors, Vishay–Sprague #293D106X9035D
C3, C4	6.8 pF Chip Capacitors, ACCU–P (0805), AVX #08051J6R8CBT
C5	10 nF Chip Capacitor (0805), AVX #08055C103KATDA
C7	1.5 pF Chip Capacitor, ACCU–P (0805), AVX #08051J2R2BBT
C8, C10	0.5 pF Chip Capacitors, ACCU–P (0805), AVX #08051J0R5BBT
C9	10 pF Chip Capacitor, ACCU–P (0805), AVX #08055J100GBT
L1	19 mm $\times$ 1.07 mm
L2	7.7 mm $\times$ 13.8 mm
L3	9.3 mm $\times$ 22 mm
L4	17.7 mm $\times$ 3.5 mm
L5	3.4 mm $\times$ 1.5 mm
R1, R6	10 Ω , 1/8 W Chip Resistors (0805)
R2, R3	1 k Ω , 1/8 W Chip Resistors (0805)
R4	2.2 k Ω , 1/8 W Chip Resistor (0805)
R5	0 Ω , 1/8 W Chip Resistor (0805)
P1	5 k Ω Potentiometer CMS Cermet Multi–Turn, Bourns #3224W
T1	Voltage Regulator, Micro–8, Motorola #LP2951
T2	Bipolar NPN Transistor, SOT–23, Motorola #BC847
PCB	Rogers RO4350, 0.5 mm, $\epsilon_r = 3.53$

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

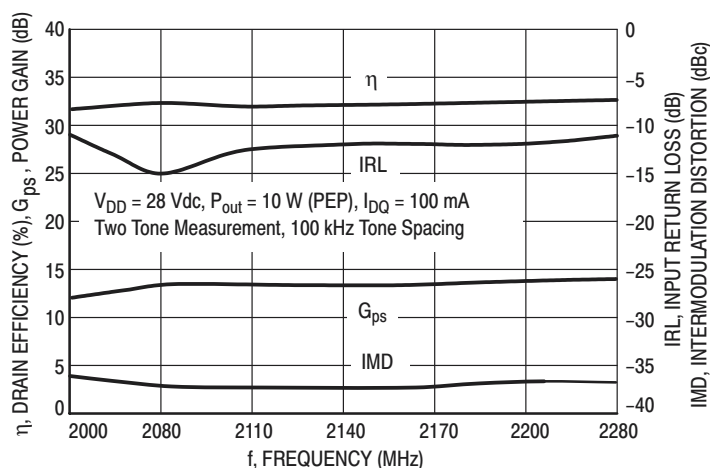


Figure 4. Class AB Broadband Circuit Performance

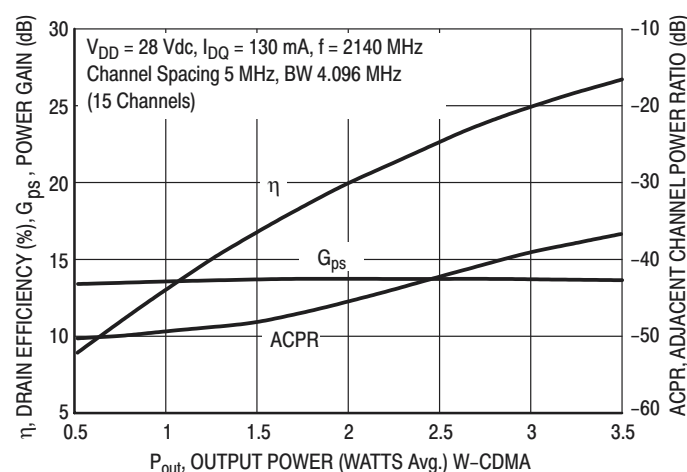


Figure 5. W-CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

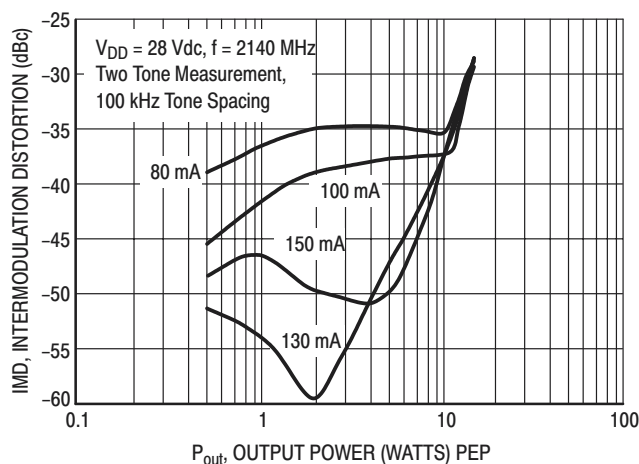


Figure 6. Intermodulation Distortion versus Output Power

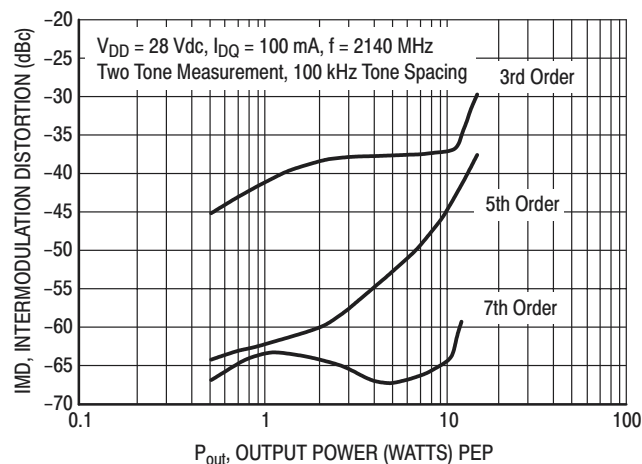


Figure 7. Intermodulation Distortion Products versus Output Power

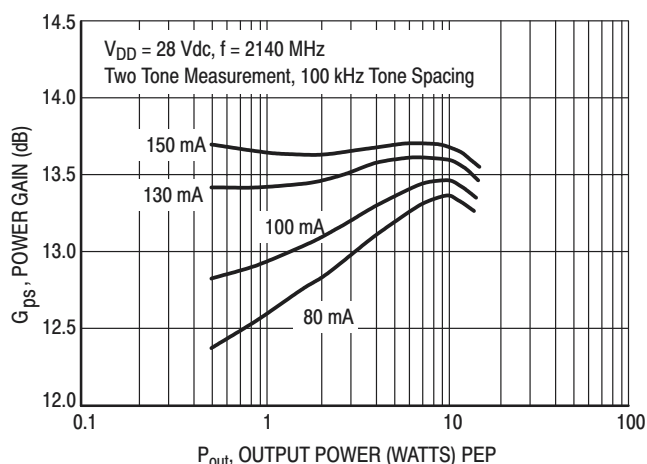


Figure 8. Power Gain versus Output Power

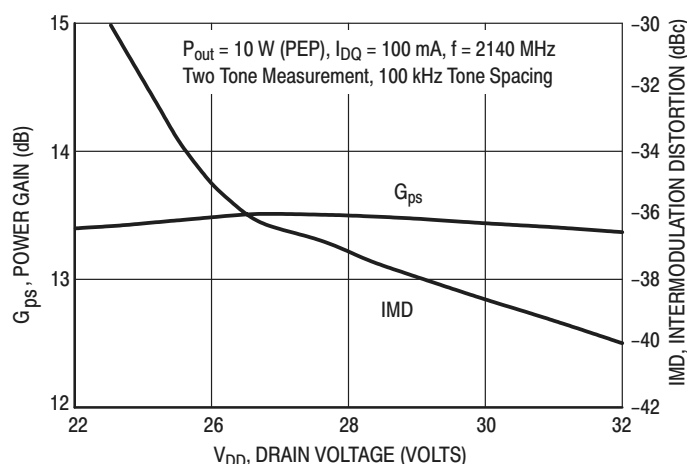
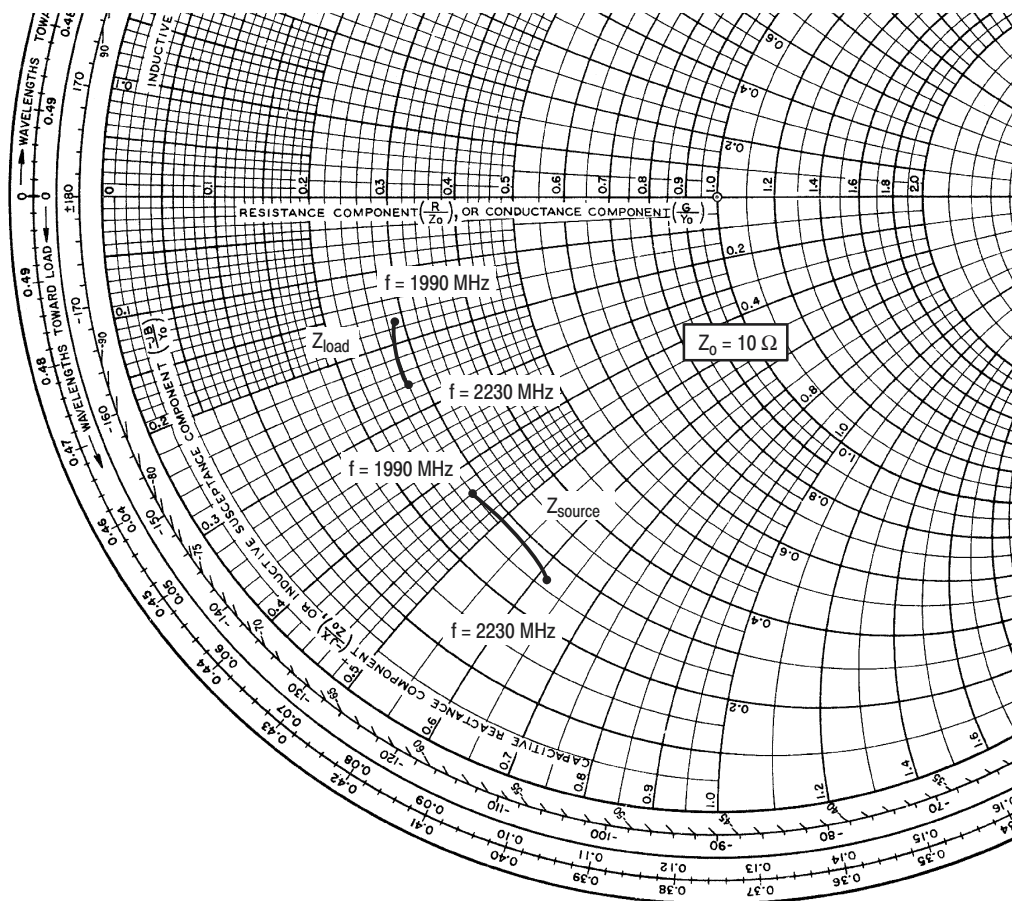


Figure 9. Intermodulation and Gain versus Supply Voltage



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 100 \text{ mA}$, $P_{out} = P_{1dB \text{ CW}}$

f MHz	Z_{source} Ω	Z_{load} Ω
1990	$2.85 - j4.38$	$2.93 - j1.71$
2110	$2.89 - j5.04$	$2.76 - j2.28$
2230	$2.73 - j6.19$	$2.83 - j2.59$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

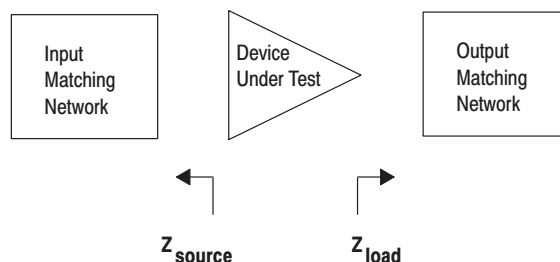


Figure 10. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

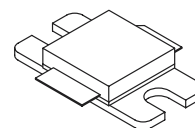
Designed for PCN and PCS base station applications with frequencies from 2.0 to 2.2 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Wideband CDMA Performance: -45 dB ACPR @ 4.096 MHz, 28 Volts
Output Power — 3.5 Watts
Power Gain — 14 dB
Efficiency — 15%
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

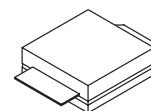
MRF21030R3

MRF21030SR3

2.2 GHz, 30 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-04, STYLE 1
NI-400
MRF21030R3



CASE 465F-04, STYLE 1
NI-400S
MRF21030SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	83.3 0.48	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C/W}$

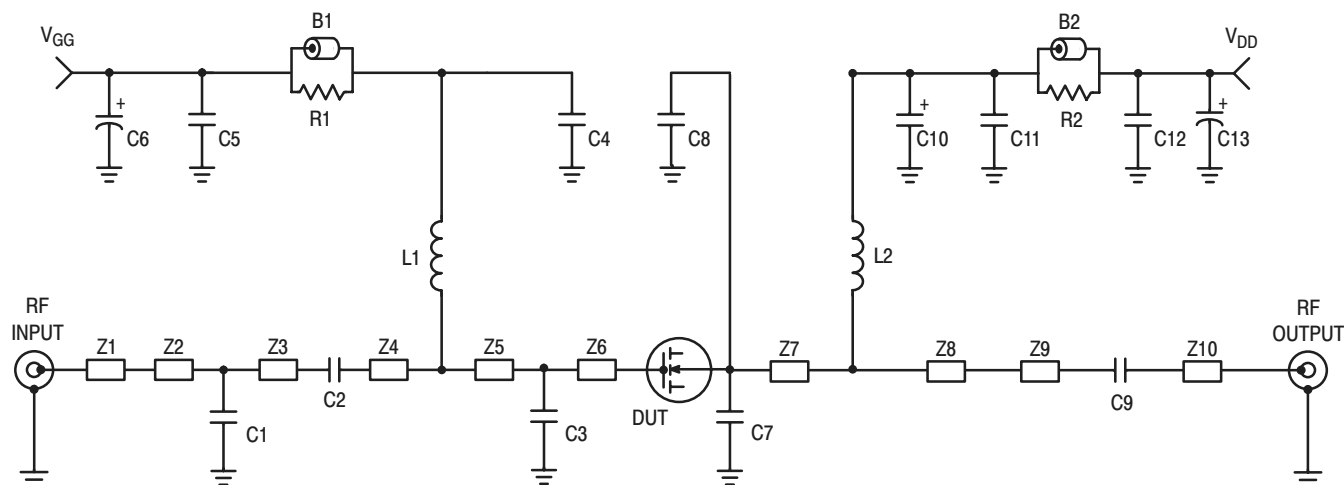
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 20 μA)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 250 mA)	V _{GS(Q)}	2	3.3	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.29	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 1 Adc)	g _{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{iss}	—	98.5	—	pF
Output Capacitance (1) (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{oss}	—	37	—	pF
Reverse Transfer Capacitance (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 2140.0 MHz, f ₂ = 2140.1 MHz)	G _{ps}	—	13	—	dB
Two–Tone Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 2140.0 MHz, f ₂ = 2140.1 MHz)	η	—	33	—	%
3rd Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 2140.0 MHz, f ₂ = 2140.1 MHz)	IMD	—	–30	—	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 2140.0 MHz, f ₂ = 2140.1 MHz)	IRL	—	–13	—	dB
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz and f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	G _{ps}	12	13	—	dB
Two–Tone Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz and f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	η	31	33	—	%
3rd Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz and f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	IMD	—	–30	–27.5	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 30 W PEP, I _{DQ} = 250 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz and f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	IRL	—	–13	–9	dB
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 30 W CW, I _{DQ} = 250 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.



B1, B2	Short Ferrite Beads	Z1	0.153" x 0.087" Microstrip
C1	1 pF Chip Capacitor	Z2	0.509" x 0.156" Microstrip
C2	4.7 pF Chip Capacitor	Z3	0.572" x 0.087" Microstrip
C3	0.5 pF Chip Capacitor	Z4	0.509" x 0.232" Microstrip
C4	3.9 pF Chip Capacitor	Z5	0.277" x 0.143" Microstrip
C5, C12	0.1 μ F Chip Capacitors	Z6	0.200" x 0.305" Microstrip
C6, C13	470 μ F, 63 V Electrolytic Chip Capacitors	Z7	0.200" x 0.511" Microstrip
C7, C8	0.3 pF Chip Capacitors	Z8	0.510" x 0.328" Microstrip
C9	3.6 pF Chip Capacitor	Z9	0.608" x 0.081" Microstrip
C10	22 μ F Tantalum Chip Capacitor	PCB	Taconic TLX8, 30 mils, $\epsilon_r = 2.55$
C11	5.1 pF Chip Capacitor		
L1, L2	12.5 nH Inductors		
R1, R2	12 Ω Chip Resistors (1206)		

Figure 1. MRF21030 Test Circuit Schematic

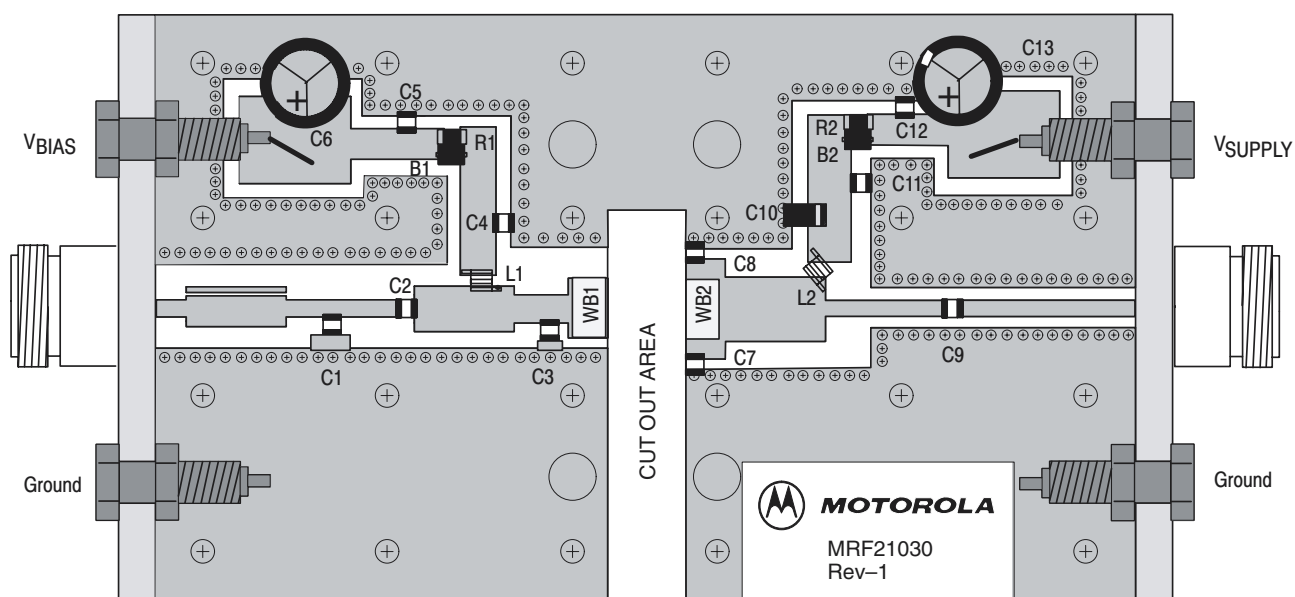


Figure 2. MRF21030 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

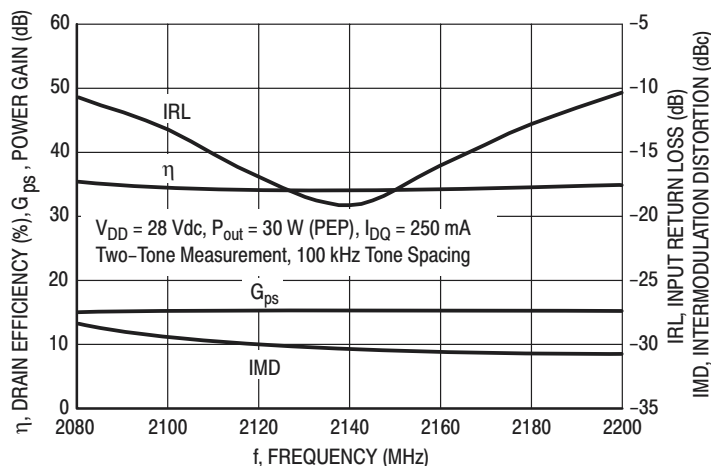


Figure 3. Class AB Broadband Circuit Performance

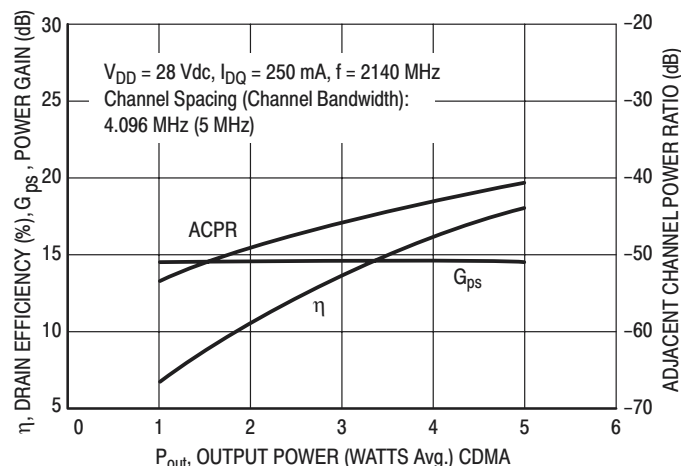


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

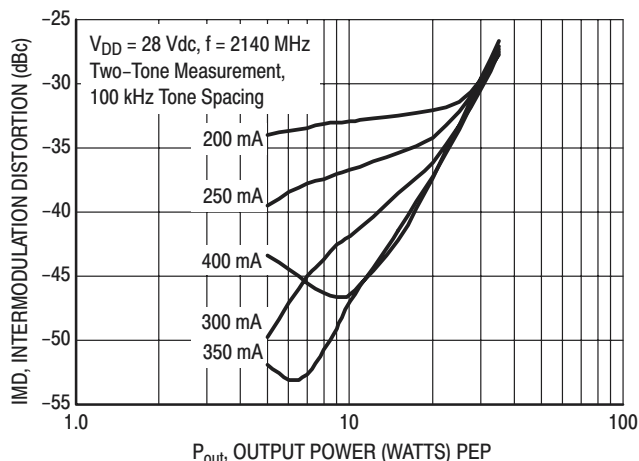


Figure 5. Intermodulation Distortion versus Output Power

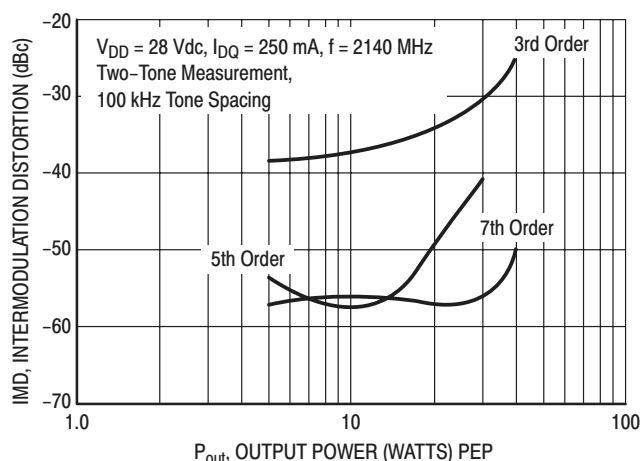


Figure 6. Intermodulation Distortion Products versus Output Power

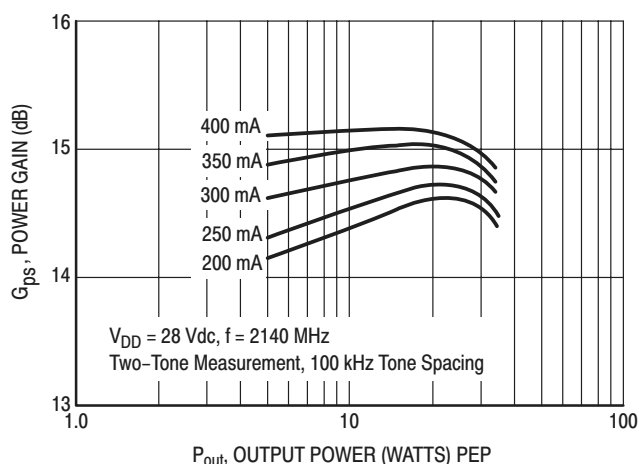


Figure 7. Power Gain versus Output Power

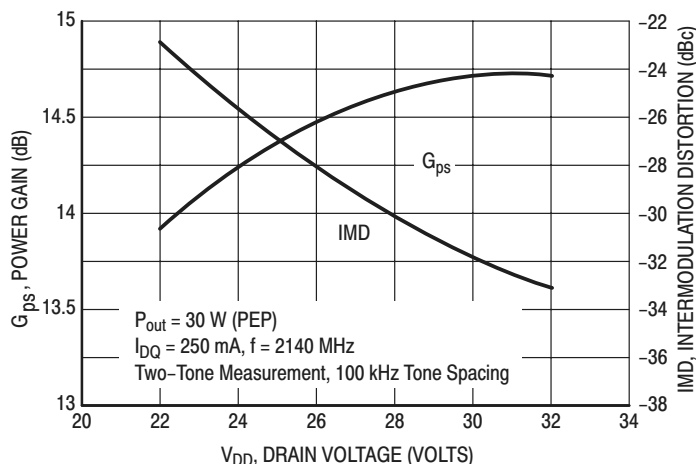
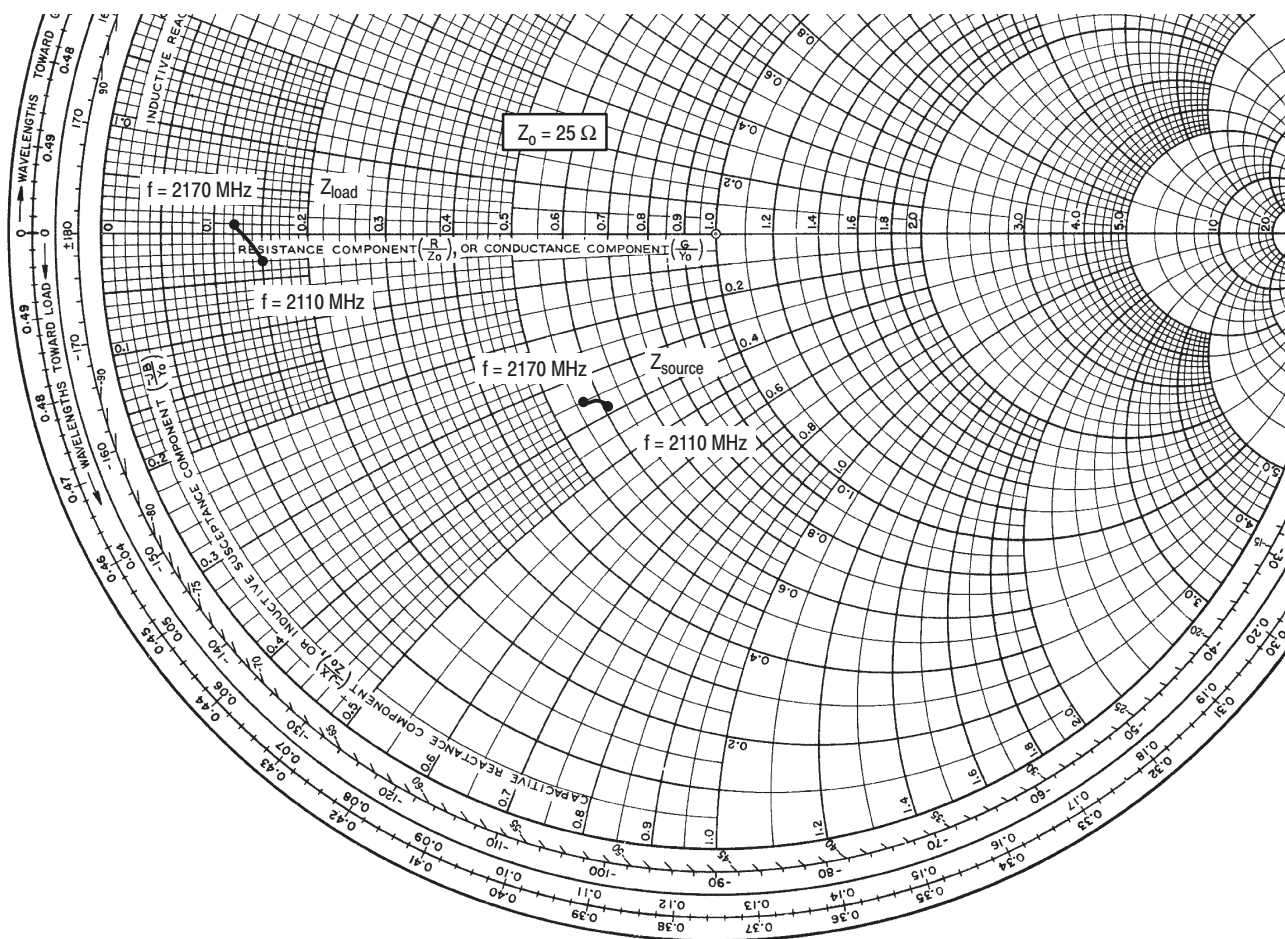


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 30 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
2110	$15.3 - j9.4$	$3.7 - j0.78$
2140	$14.6 - j9.4$	$3.4 - j0.37$
2170	$14.3 - j8.8$	$3.0 + j0.13$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

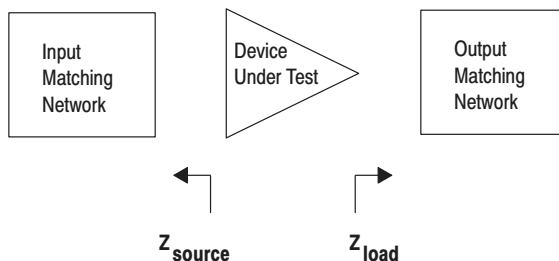


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

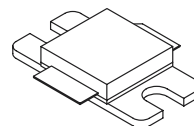
RF Power Field Effect Transistors N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

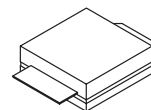
- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 500$ mA, $f_1 = 2135$ MHz, $f_2 = 2145$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels measured over 3.84 MHz Bandwidth at $f_1 - 5$ MHz and $f_2 + 5$ MHz, Distortion Products measured over a 3.84 MHz Bandwidth at $f_1 - 10$ MHz and $f_2 + 10$ MHz, Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.
Output Power — 10 Watts Avg.
Efficiency — 23.5%
Gain — 15 dB
IM3 — -37.5 dBc
ACPR — -41 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2170 MHz, 45 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

MRF21045R3
MRF21045SR3

2170 MHz, 45 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-04, STYLE 1
NI-400
MRF21045R3



CASE 465F-04, STYLE 1
NI-400S
MRF21045SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	105 0.60	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.65	$^\circ\text{C}/\text{W}$

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS (DC)

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 500 mAdc)	V _{GS(Q)}	3	3.9	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.19	0.21	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 1 Adc)	g _{fs}	—	3	—	S

DYNAMIC CHARACTERISTICS (1)

Reverse Transfer Capacitance (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	1.8	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier W–CDMA. Peak/Avg. ratio = 8.3 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 10 W Avg., I _{DQ} = 500 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	G _{ps}	13.5	15	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 10 W Avg., I _{DQ} = 500 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	η	21	23.5	—	%
Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 10 W Avg., I _{DQ} = 500 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured over 3.84 MHz Bandwidth at f ₁ –10 MHz and f ₂ +10 MHz.)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 10 W Avg., I _{DQ} = 500 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured over 3.84 MHz Bandwidth at f ₁ –5 MHz and f ₂ +5 MHz.)	ACPR	—	–41	–38	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 10 W Avg., I _{DQ} = 500 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 45 W CW, I _{DQ} = 500 mA, f = 2170 MHz VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

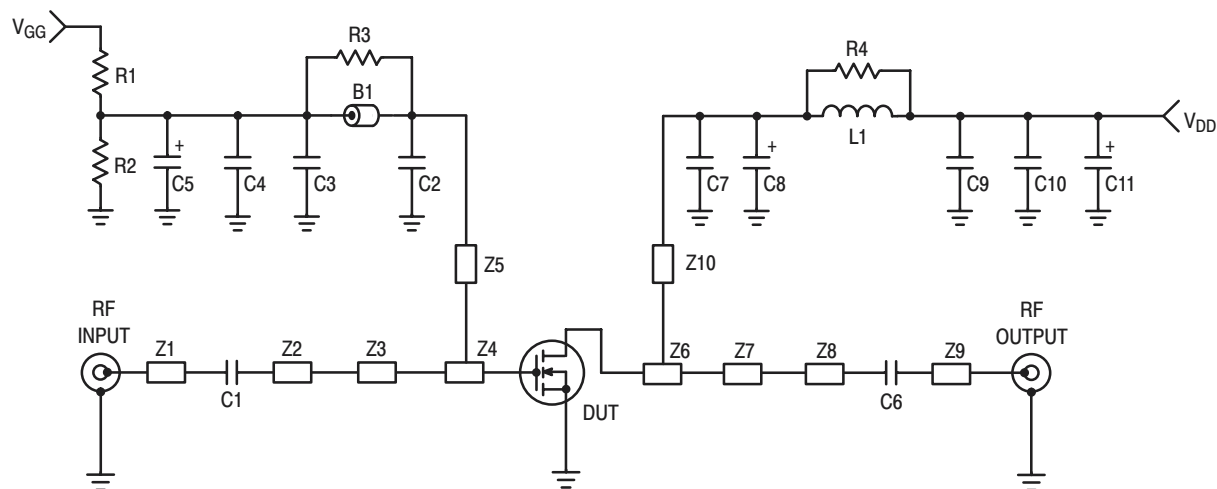
(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) — continued					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	G_{ps}	—	14.9	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	η	—	36	—	%
Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	IMD	—	−30	—	dBc
Two-Tone Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	IRL	—	−12	—	dB
P_{out} , 1 dB Compression Point ($V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 500\text{ mA}$, $f = 2170\text{ MHz}$)	P1dB	—	50	—	W

Freescale Semiconductor, Inc.



Z1, Z9	0.750" x 0.084" Transmission Line
Z2	0.160" x 0.084" Transmission Line
Z3	1.195" x 0.176" Transmission Line
Z4	0.125" x 0.320" Transmission Line
Z5	1.100" x 0.045" Transmission Line
Z6	0.442" x 0.650" Transmission Line
Z7	0.490" x 0.140" Transmission Line
Z8	0.540" x 0.084" Transmission Line
Z10	0.825" x 0.055" Transmission Line

Board	0.030" Glass Teflon®, Keene GX-0300-55-22, $\epsilon_r = 2.55$
PCB	Etched Circuit Boards MRF21045 Rev. 3, CMR

Figure 1. MRF21045 Test Circuit Schematic

Table 1. MRF21045 Component Designations and Values

Designators	Description
B1	Short Ferrite Bead, Fair Rite, #2743019447
C1, C2, C6	43 pF Chip Capacitors, ATC #100B430JCA500X
C7	5.6 pF Chip Capacitor, ATC #100B5R6JCA500X
C3, C9	1000 pF Chip Capacitors, ATC #100B102JCA500X
C4, C10	0.1 μ F Chip Capacitors, Kemet #CDR33BX104AKWS
C5	1.0 μ F Tantalum Chip Capacitor, Kemet #T491C105M050
C8	10 μ F Tantalum Chip Capacitor, Kemet #T495X106K035AS4394
C11	22 μ F Tantalum Chip Capacitor, Kemet #T491X226K035AS4394
L1	1 Turn, #20 AWG, 0.100" ID, Motorola
N1, N2	Type N Flange Mounts, Omni Spectra #3052-1648-10
R1	1.0 k Ω , 1/8 W Chip Resistor
R2	180 k Ω , 1/8 W Chip Resistor
R3, R4	10 Ω , 1/8 W Chip Resistors

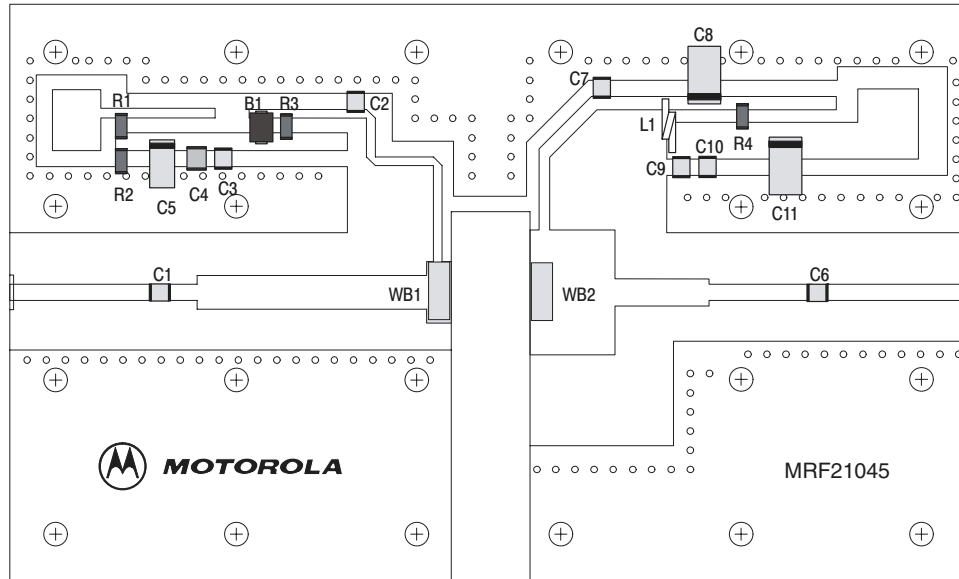


Figure 2. MRF21045 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

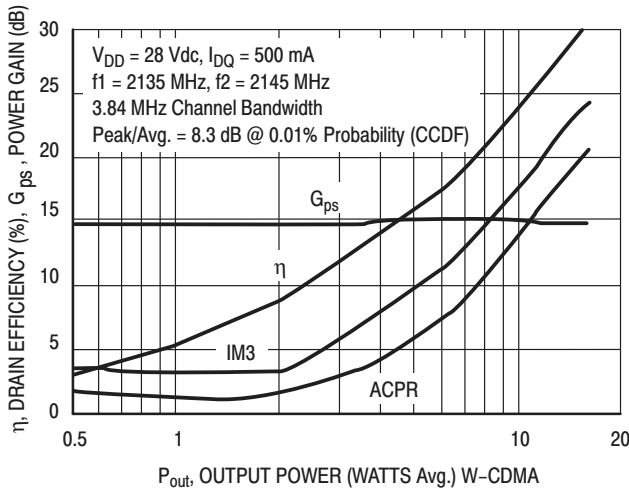


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

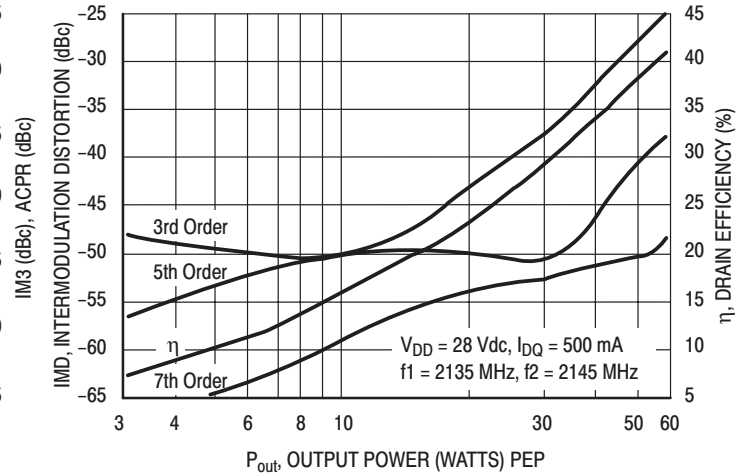


Figure 4. Intermodulation Distortion Products versus Output Power

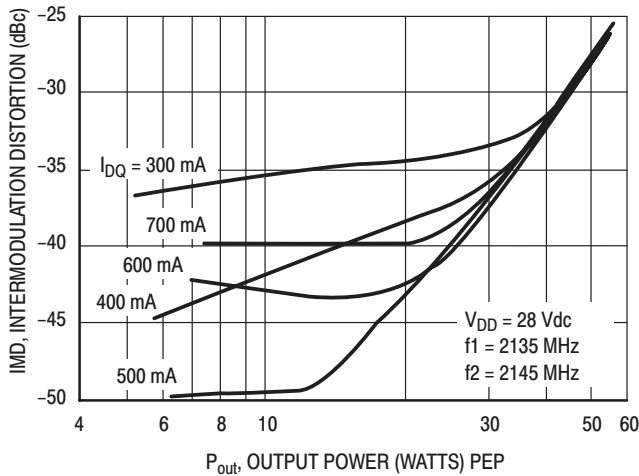


Figure 5. Intermodulation Distortion versus Output Power

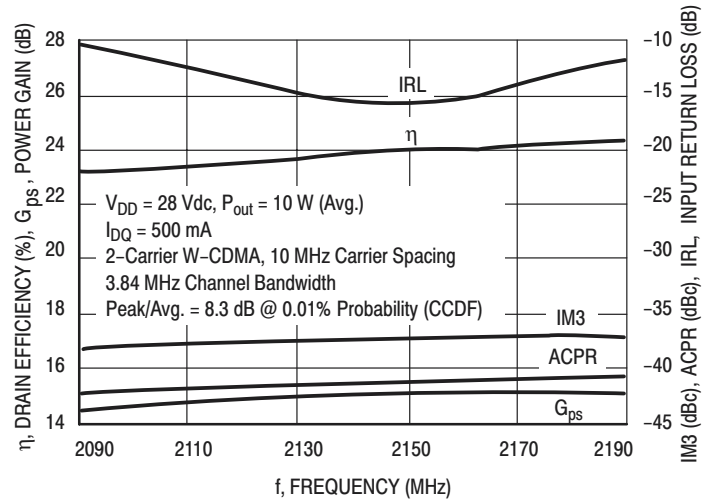


Figure 6. 2-Carrier W-CDMA Broadband Performance

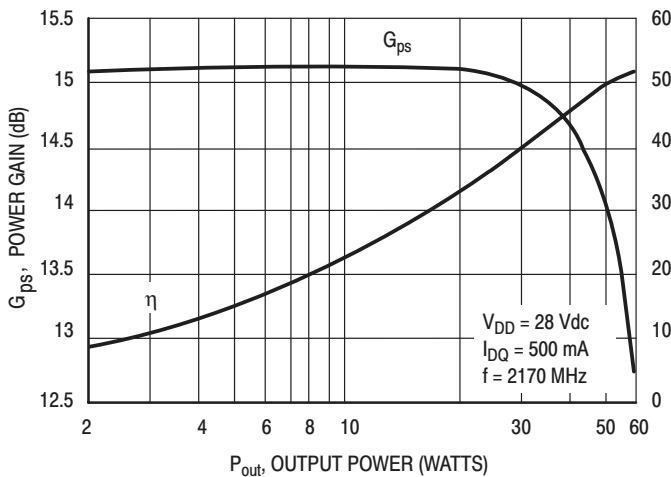


Figure 7. CW Performance

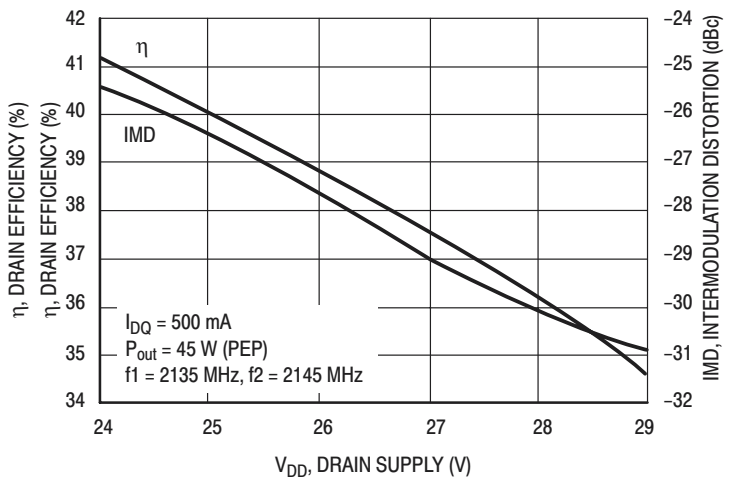


Figure 8. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

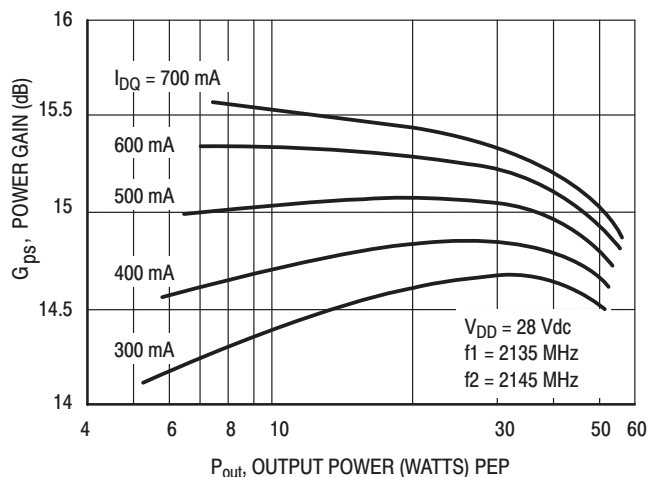


Figure 9. Two-Tone Power Gain versus Output Power

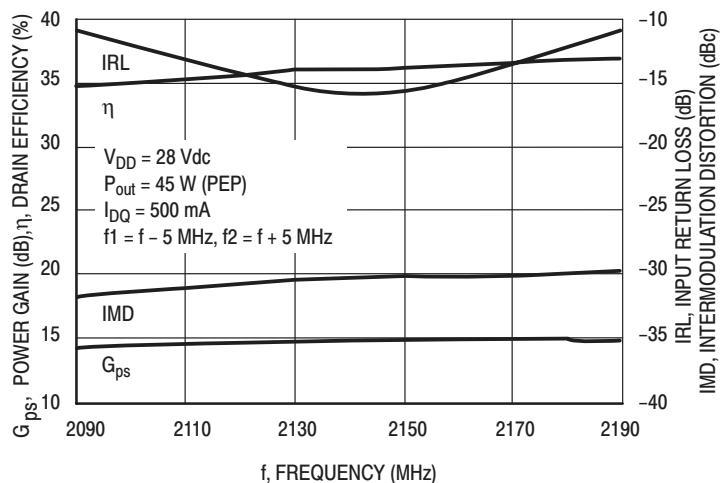


Figure 10. Two-Tone Broadband Performance

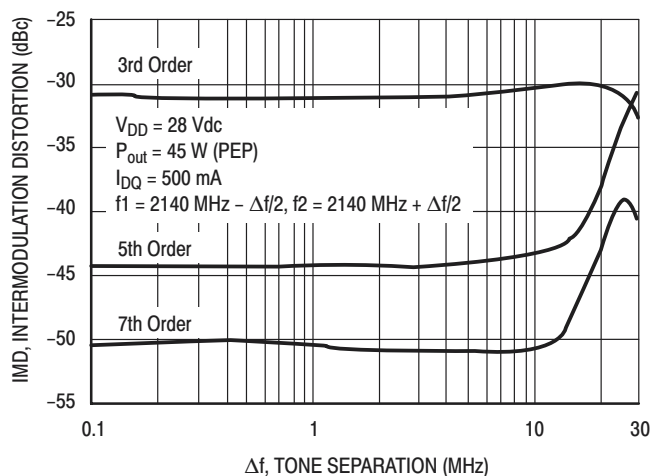


Figure 11. Intermodulation Distortion Products versus Two-Tone Spacing

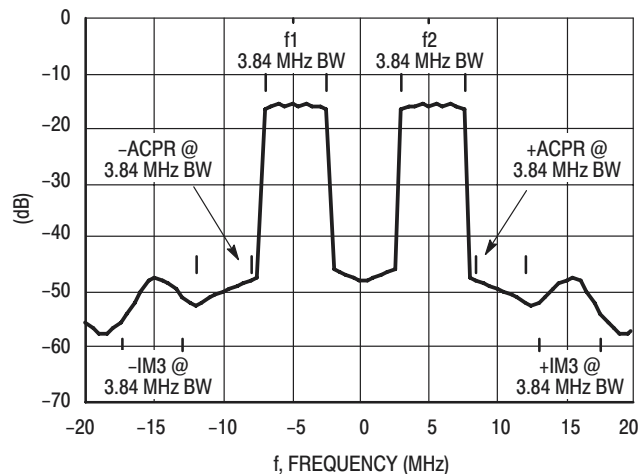
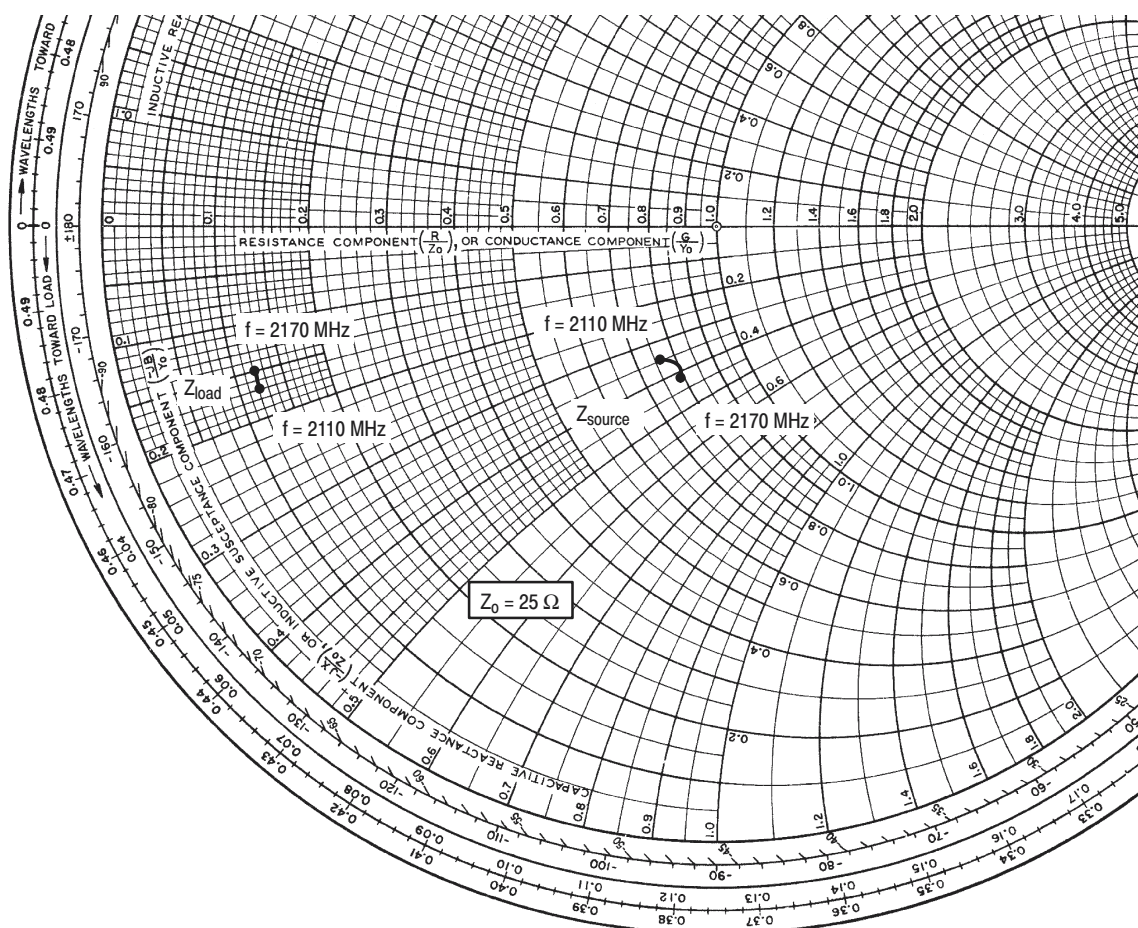


Figure 12. 2-Carrier W-CDMA Spectrum



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 10 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
2110	$18.88 - j8.86$	$3.11 - j4.18$
2140	$19.80 - j9.93$	$3.09 - j3.87$
2170	$19.68 - j10.44$	$3.12 - j3.72$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

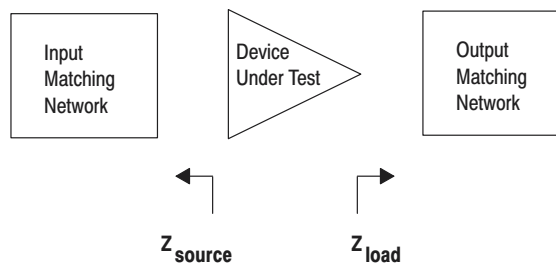


Figure 13. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

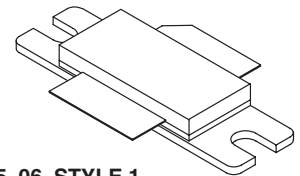
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 2.1 to 2.2 GHz. Suitable for W-CDMA, CDMA, TDMA, GSM and multicarrier amplifier applications.

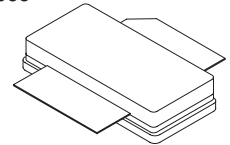
- Typical W-CDMA Performance: 2140 MHz, 28 Volts
5 MHz Offset @ 4.096 MHz BW, 15 DTCH
Output Power — 6.0 Watts
Power Gain — 12.5 dB
Drain Efficiency — 15%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 60 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

MRF21060
MRF21060R3
MRF21060SR3

2170 MHz, 60 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF21060



CASE 465A-06, STYLE 1
NI-780S
MRF21060SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	180 0.98	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

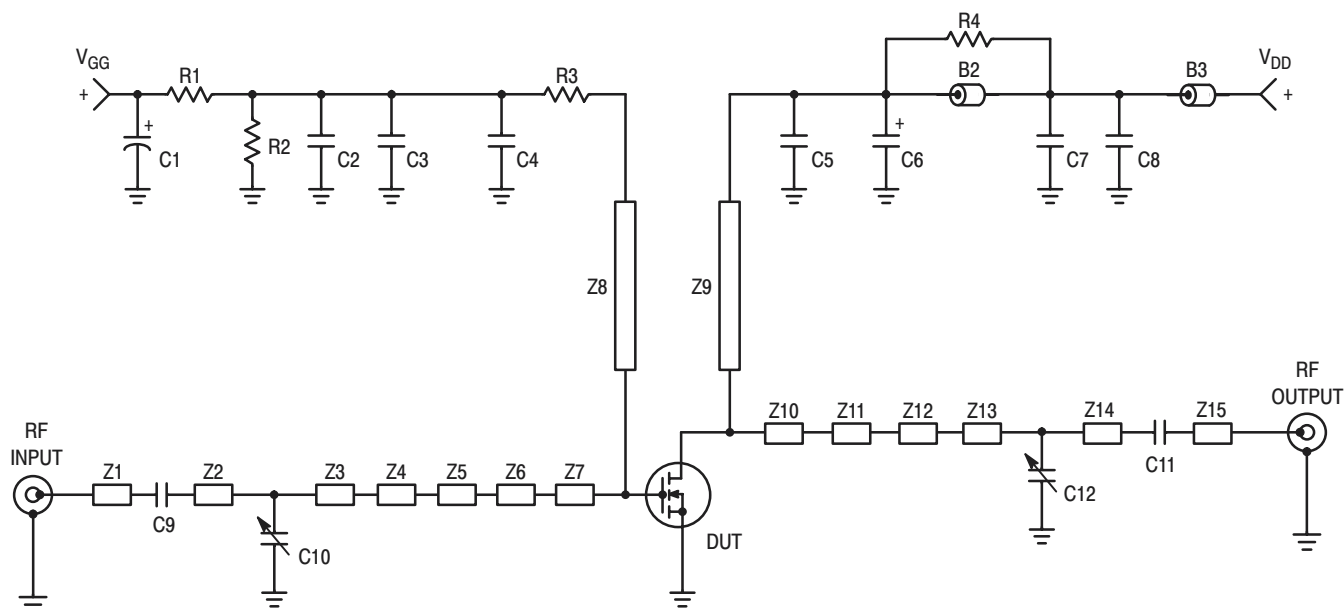
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.02	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 10 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	6	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 500 mAdc)	V _{GS(Q)}	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.27	—	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.7	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	G _{ps}	11	12.5	—	dB
Two–Tone Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	η	31	34	—	%
3rd Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	–28	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 60 W PEP, I _{DQ} = 500 mA, f = 2110 MHz and 2170 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P _{out} , 1 dB Compression Point (V _{DD} = 28 Vdc, P _{out} = 60 W CW, f = 2170 MHz)	P1dB	—	60	—	W
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 60 W CW, I _{DQ} = 500 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B2 – B3	Ferrite Beads, Fair Rite #2743019447	Z3	0.180" x 0.100" Microstrip
C1	10 μ F, 50 V Electrolytic Chip Capacitor, Panasonic #ECEV1HV100R	Z4	0.152" x 0.293" Microstrip
C2, C7	1000 pF Chip Capacitors, ATC #100B102JCA500X	Z5	0.216" x 0.100" Microstrip
C3, C8	0.10 μ F Chip Capacitors, Kemet #CDR33BX104AKWS	Z6	0.114" x 0.410" Microstrip
C4, C5	4.7 pF Chip Capacitors, ATC #100B4R7JCA500X	Z7	0.626" x 0.872" Microstrip
C6	22 μ F, 35 V Tantalum Surface Mount Chip Capacitor, Sprague	Z8	1.050" x 0.050" Microstrip
C9, C11	9.1 pF Chip Capacitors, ATC #100B9R1JCA500X	Z9	0.830" x 0.050" Microstrip
C10	0.8 pF – 8.0 pF Variable Capacitor, Johanson Gigatrim	Z10	0.596" x 1.040" Microstrip
C12	0.4 pF – 4.5 pF Variable Capacitor, Johanson Gigatrim	Z11	0.186" x 0.315" Microstrip
R1	1 k Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z12	0.097" x 0.525" Microstrip
R2	560 k Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z13	0.353" x 0.138" Microstrip
R3	10 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z14	0.112" x 0.080" Microstrip
R4	10 Ω , 1/4 W Fixed Film Chip Resistor, 0.08" x 0.13"	Z15	0.722" x 0.080" Microstrip
Z1	0.743" x 0.080" Microstrip	Board	0.030" Glass Teflon [®] , Arlon
Z2	0.070" x 0.100" Microstrip		GX-0300-55-22, 2 oz Cu

Figure 1. MRF21060 Test Circuit Schematic

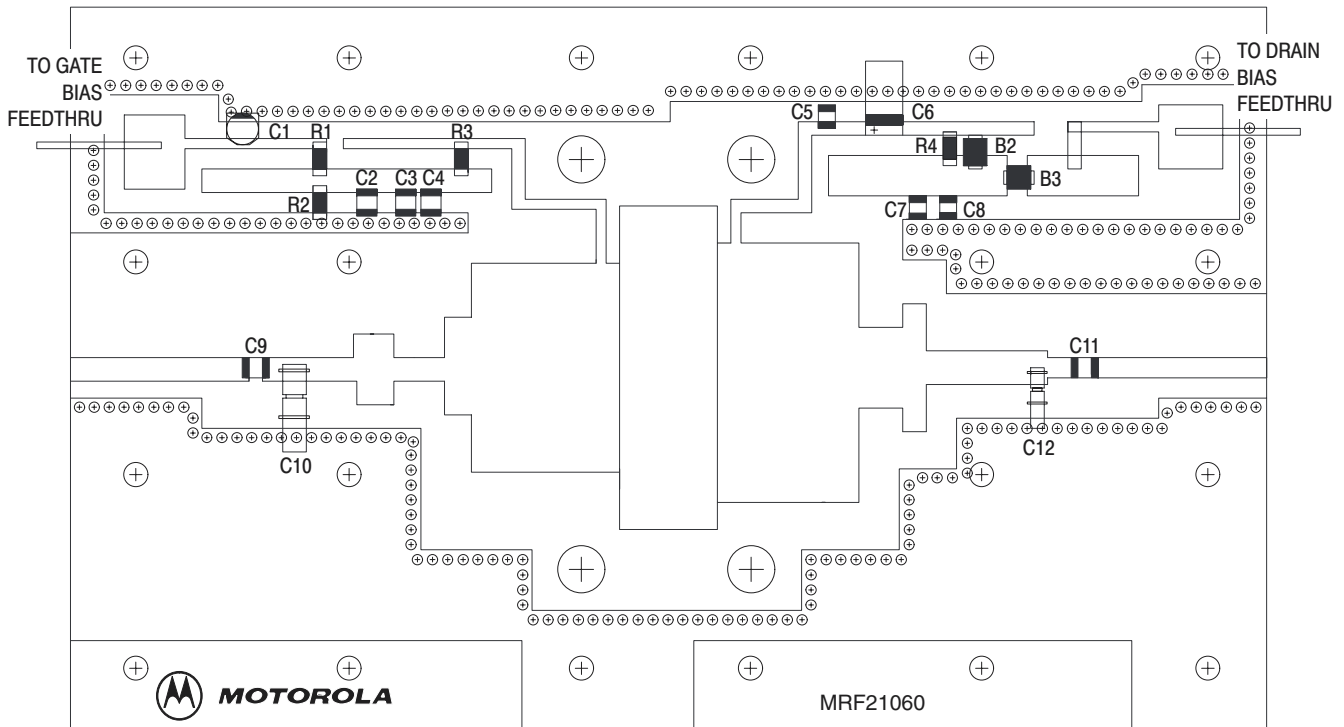


Figure 2. MRF21060 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

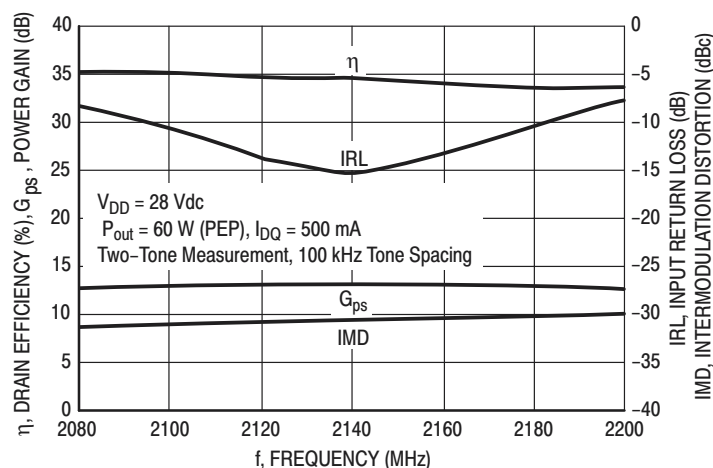


Figure 3. Class AB Broadband Circuit Performance

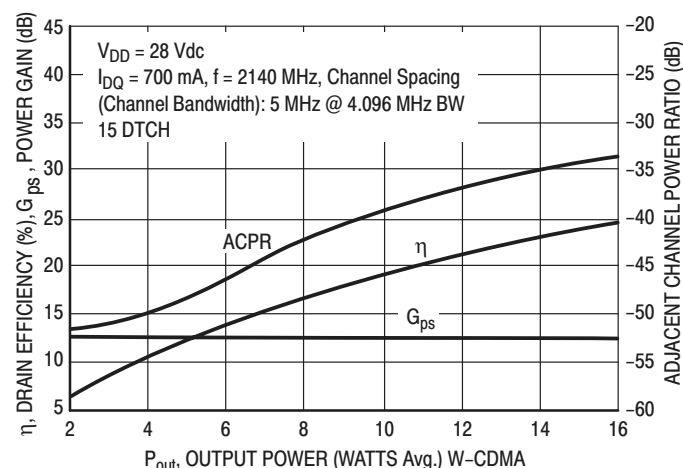


Figure 4. W-CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

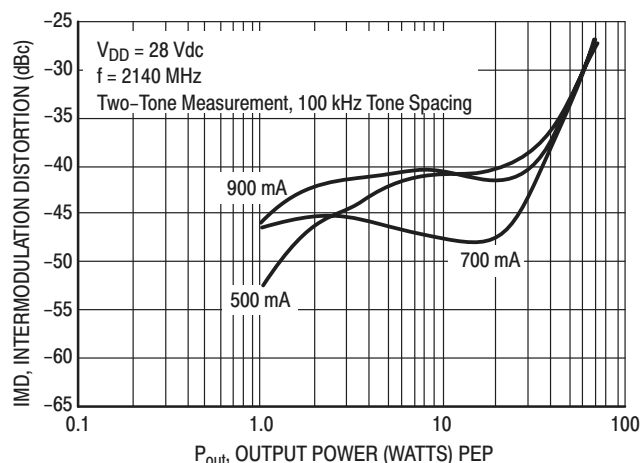


Figure 5. Intermodulation Distortion versus Output Power

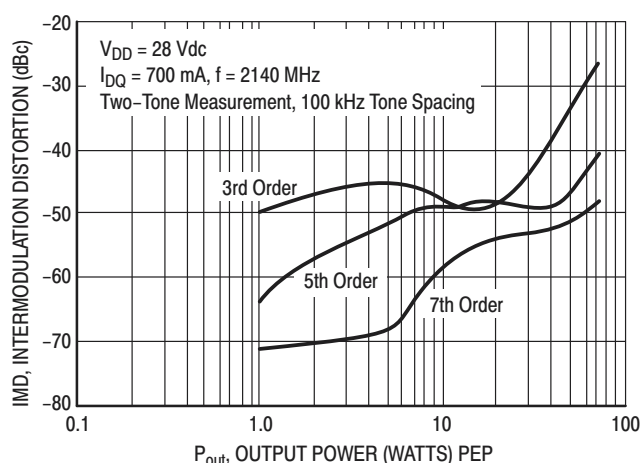


Figure 6. Intermodulation Distortion Products versus Output Power

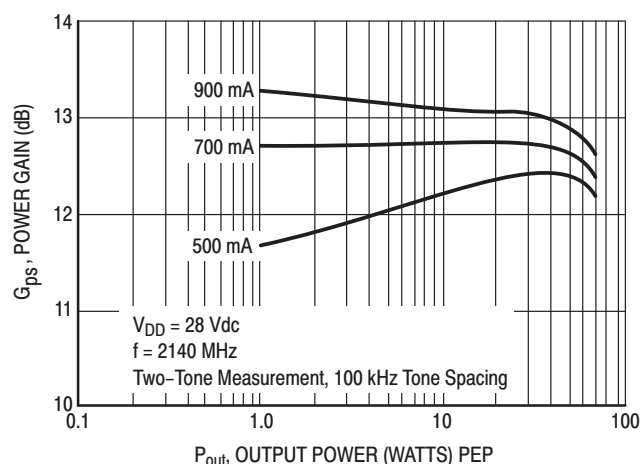


Figure 7. Power Gain versus Output Power

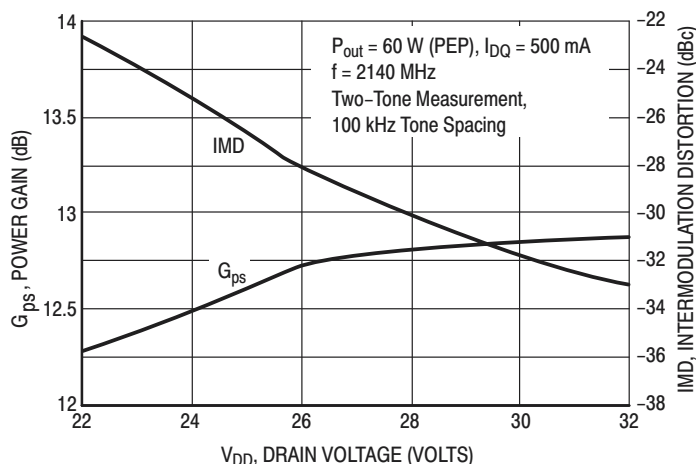
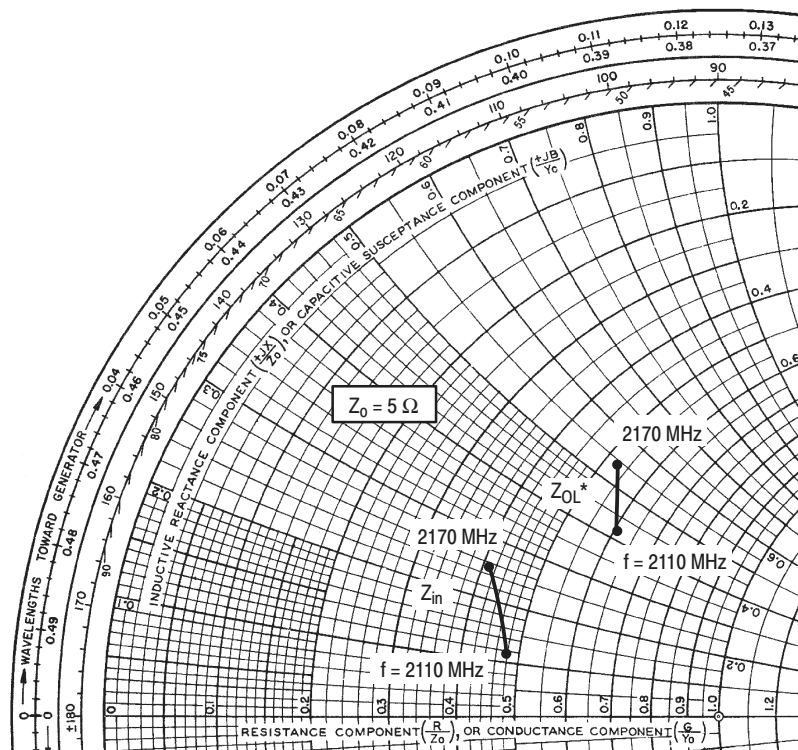


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 60 \text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
2110	$2.40 + j0.55$	$3.07 + j2.05$
2140	$2.26 + j0.87$	$2.89 + j2.38$
2170	$2.08 + j1.23$	$2.66 + j2.71$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

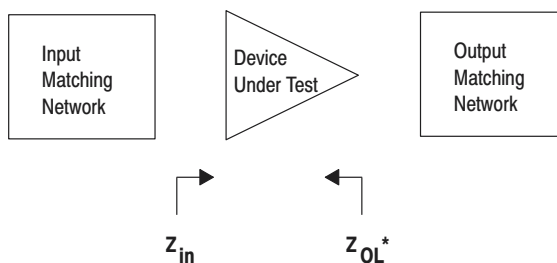


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

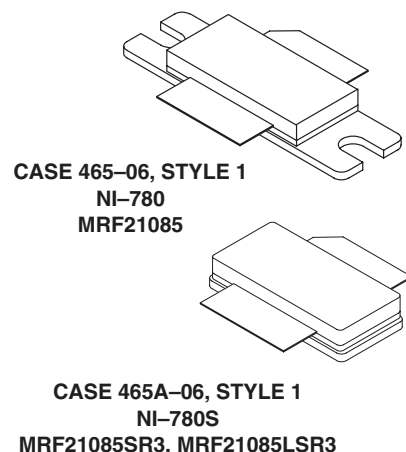
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 1000$ mA, $f_1 = 2135$ MHz, $f_2 = 2145$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ $f_1 - 5$ MHz and $f_2 + 5$ MHz, Distortion Products Measured over a 3.84 MHz BW @ $f_1 - 10$ MHz and $f_2 + 10$ MHz, Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.
Output Power — 19 Watts Avg.
Power Gain — 13.6 dB
Efficiency — 23%
IM3 — -37.5 dBc
ACPR — -41 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2170 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.

MRF21085
MRF21085R3
MRF21085SR3
MRF21085LSR3

2170 MHz, 90 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	224 1.28	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.78	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 µAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	µAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	µAdc

ON CHARACTERISTICS (DC)

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 µAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 1000 mAdc)	V _{GS(Q)}	3	3.9	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.18	0.21	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	6	—	S

DYNAMIC CHARACTERISTICS (1)

Reverse Transfer Capacitance (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1.0 MHz)	C _{rss}	—	3.6	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 1000 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	G _{ps}	12	13.6	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 1000 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	η	20	23	—	%
Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 1000 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured over 3.84 MHz BW at f ₁ –10 MHz and f ₂ +10 MHz referenced to carrier channel power.)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 1000 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured over 3.84 MHz at f ₁ –5 MHz and f ₂ +5 MHz.)	ACPR	—	–41	–38	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 1000 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 90 W CW, I _{DQ} = 1000 mA, f = 2170 MHz VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

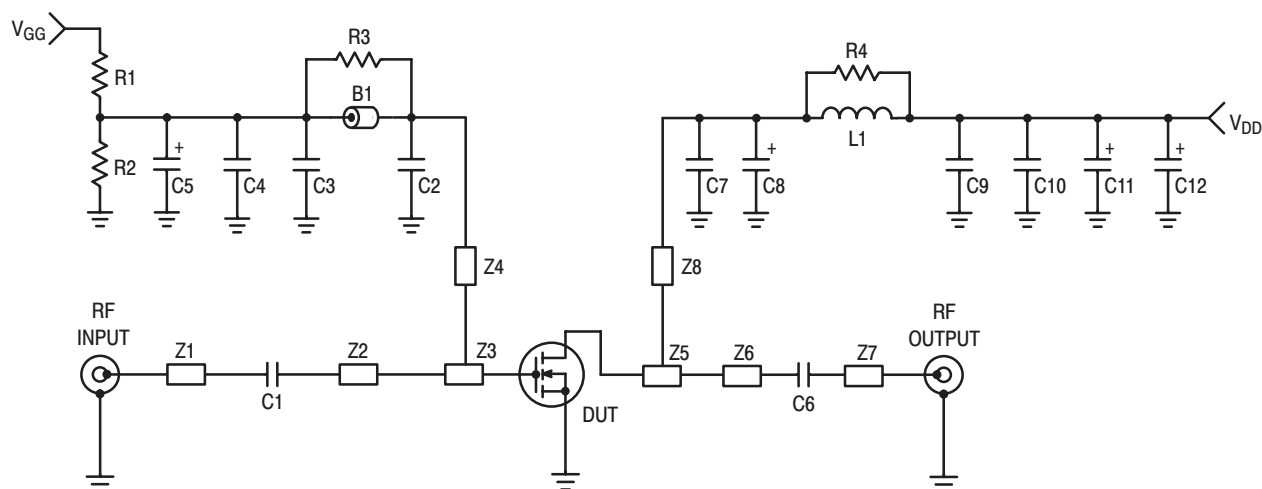
(continued)

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (continued)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 1000\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	G_{ps}	—	13.6	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 1000\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	η	—	36	—	%
Two-Tone Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 1000\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	IMD	—	−31	—	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 1000\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	IRL	—	−12	—	dB
P_{out} , 1 dB Compression Point ($V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1000\text{ mA}$, $f = 2170\text{ MHz}$)	P1dB	—	100	—	W

Freescale Semiconductor, Inc.



Z1	0.750" x 0.084" Microstrip
Z2	1.015" x 0.084" Microstrip
Z3	0.480" x 0.800" Microstrip
Z4	0.750" x 0.050" Microstrip
Z5	0.610" x 0.800" Microstrip
Z6	0.885" x 0.084" Microstrip
Z7	0.720" x 0.084" Microstrip
Z8	0.800" x 0.070" Microstrip

Board	0.030" Glass Teflon®, Keene GX-0300-55-22, $\epsilon_r = 2.55$
PCB	Etched Circuit Boards MRF21085 Rev. 3, CMR

Figure 1. MRF21085 Test Circuit Schematic

Table 1. MRF21085 Test Circuit Component Designations and Values

Designators	Description
B1	Short Ferrite Bead, Fair Rite, #2743019447
C1, C6	43 pF Chip Capacitors, ATC #100B430JCA500X
C2	10 pF Chip Capacitor, ATC #100B100JCA500X
C3, C9	1000 pF Chip Capacitors, ATC #100B102JCA500X
C4, C10	0.1 μ F Chip Capacitors, Kemet #CDR33BX104AKWS
C5	1.0 μ F Tantalum Chip Capacitor, Kemet #T491C105M050
C7	2.7 pF Chip Capacitor, ATC #100B27JCA500X
C8	10 μ F Tantalum Chip Capacitor, Kemet #T495X106K035AS4394
C11, C12	22 μ F Tantalum Chip Capacitors, Kemet #T491X226K035AS4394
L1	1 Turn, #20 AWG, 0.100" ID, Motorola
N1, N2	Type N Flange Mounts, Omni Spectra #3052-1648-10
R1	1.0 k Ω , 1/8 W Chip Resistor
R2	180 k Ω , 1/8 W Chip Resistor
R3, R4	10 Ω , 1/8 W Chip Resistors

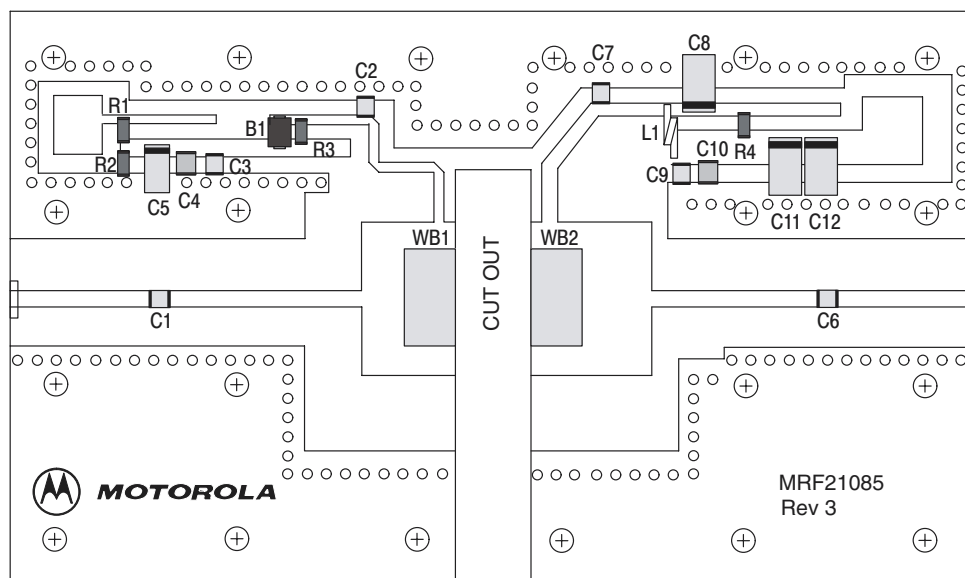


Figure 2. MRF21085 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

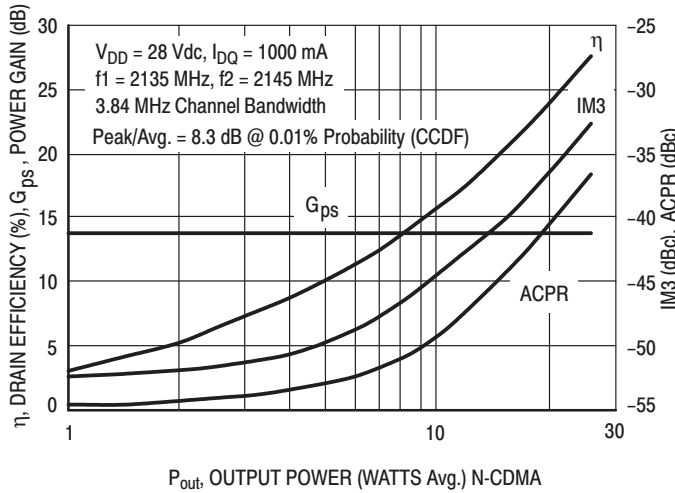


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

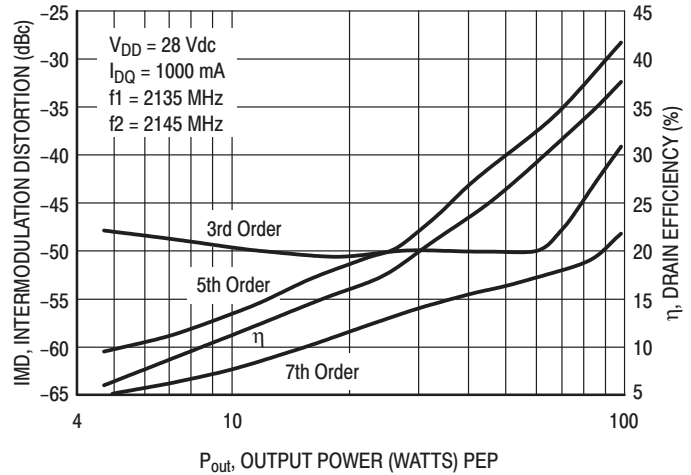


Figure 4. Intermodulation Distortion Products versus Output Power

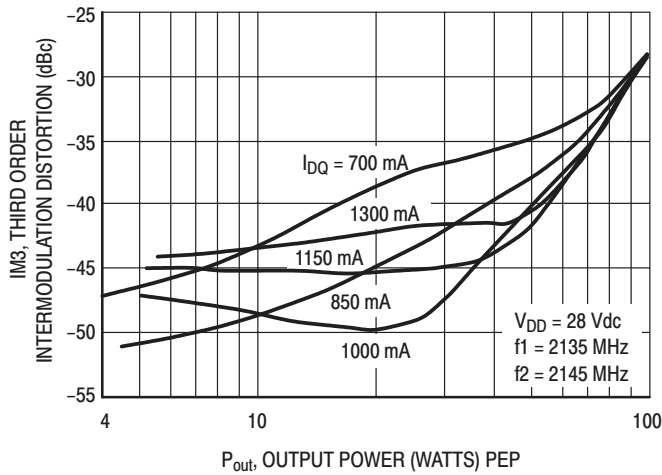


Figure 5. Third Order Intermodulation Distortion versus Output Power

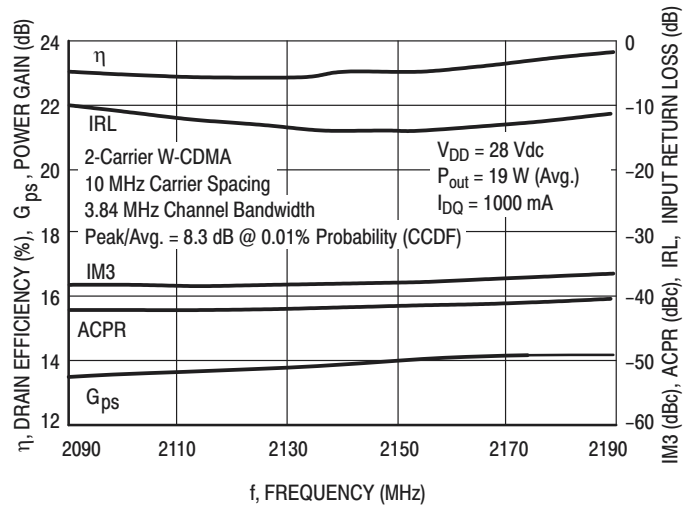


Figure 6. 2-Carrier W-CDMA Broadband Performance

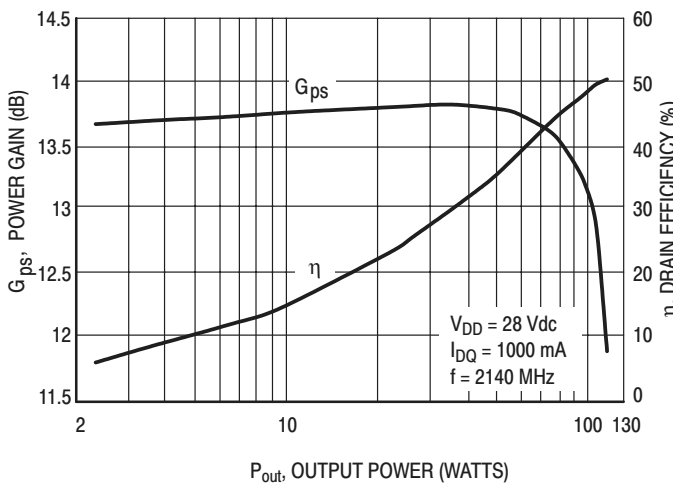


Figure 7. CW Performance

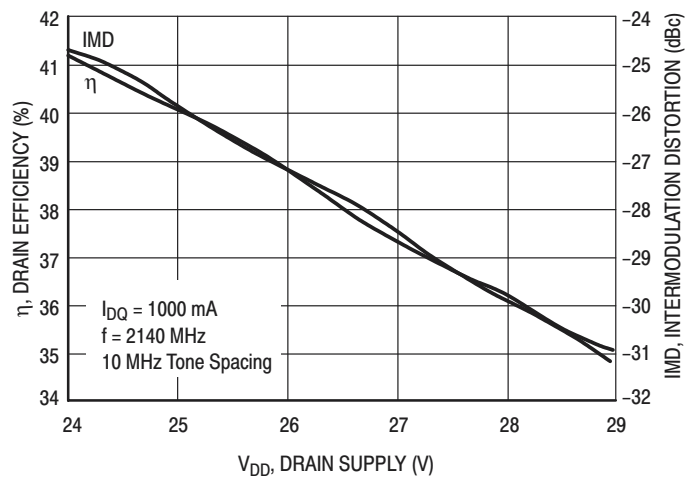


Figure 8. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

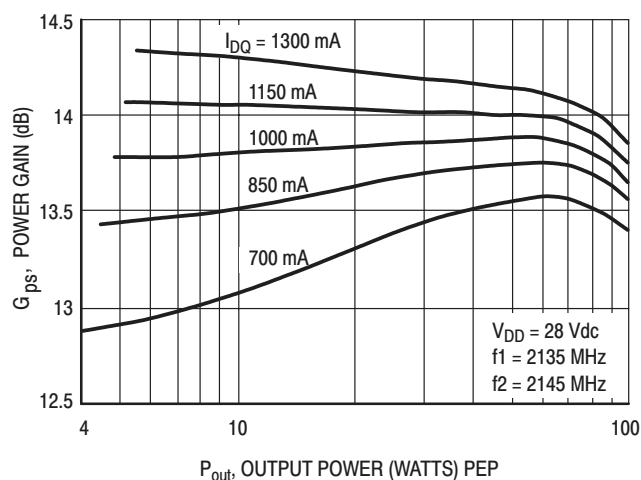


Figure 9. Two-Tone Power Gain versus Output Power

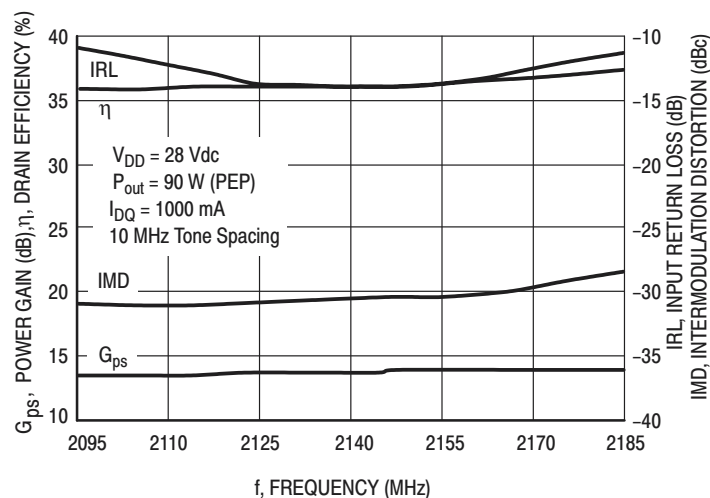


Figure 10. Two-Tone Broadband Performance

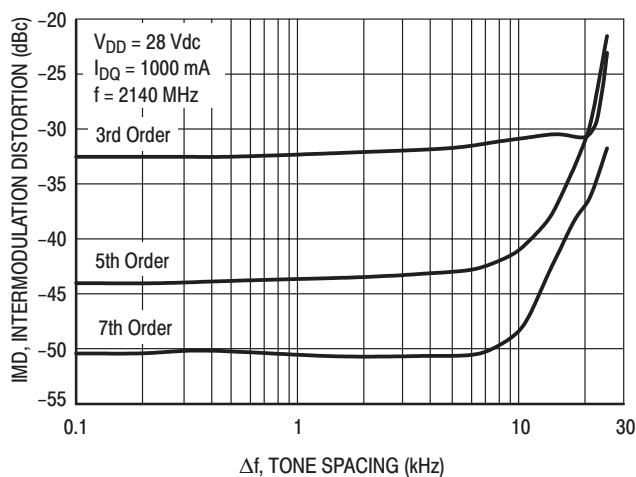


Figure 11. Intermodulation Distortion Products versus Two-Tone Spacing

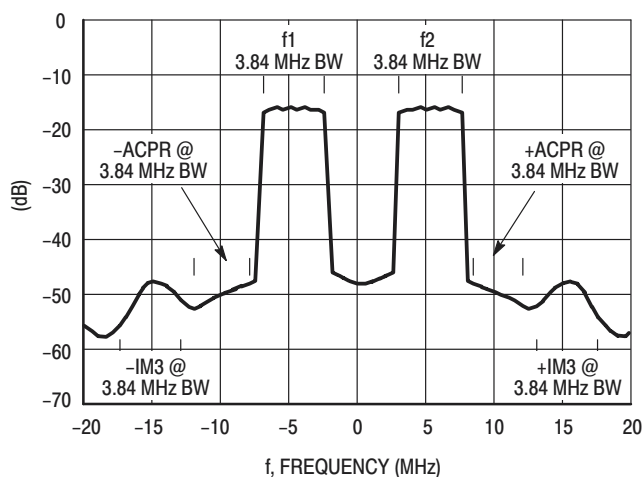
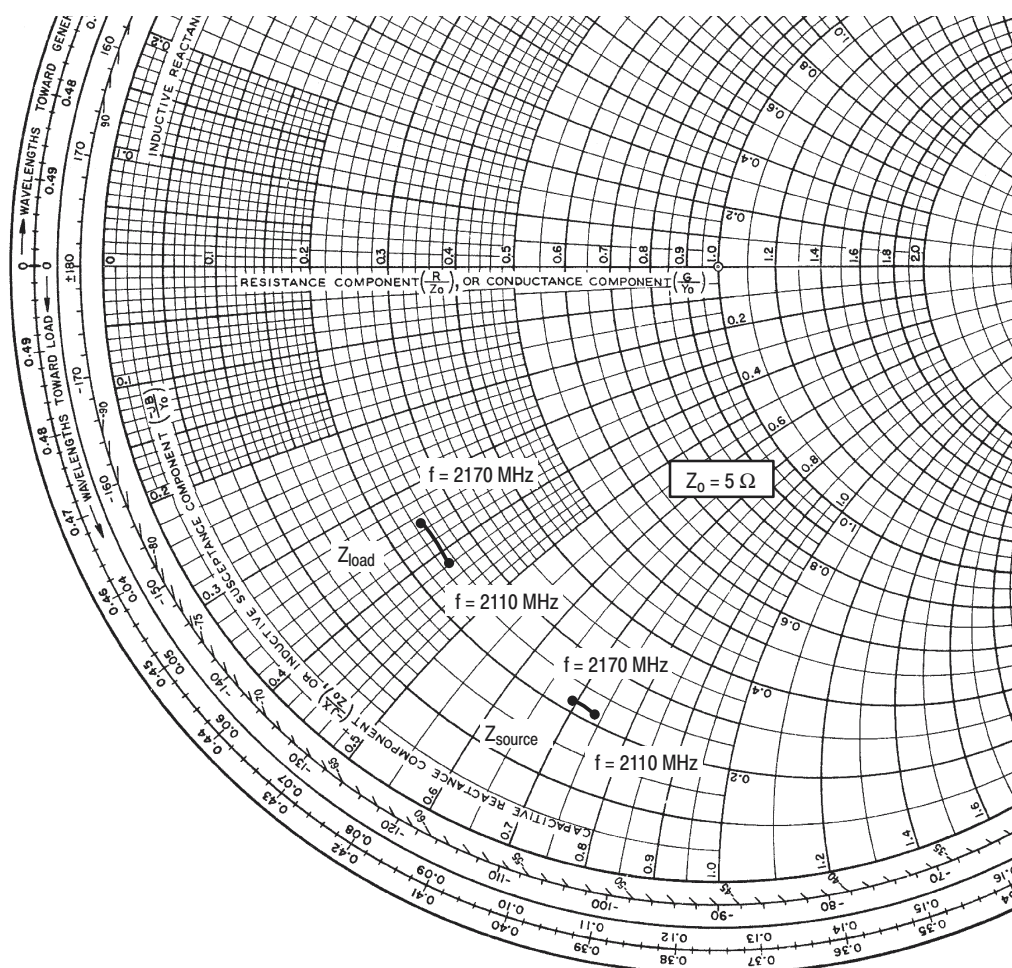


Figure 12. 2-Carrier W-CDMA Spectrum



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 1000 \text{ mA}$, $P_{out} = 19 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
2110	$1.10 - j3.71$	$1.23 - j2.10$
2140	$1.11 - j3.57$	$1.26 - j1.92$
2170	$1.12 - j3.40$	$1.25 - j1.76$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

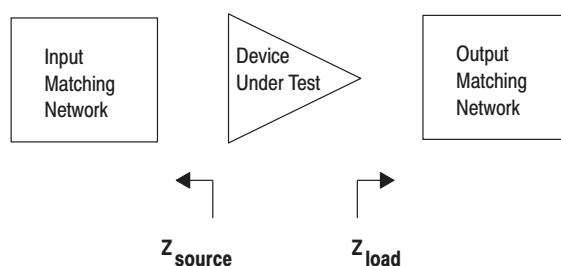


Figure 13. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

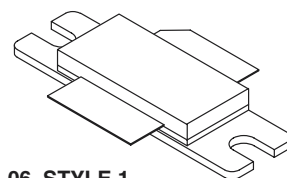
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

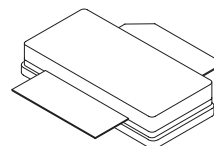
- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 850$ mA, $f_1 = 2135$ MHz, $f_2 = 2145$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ $f_1 - 5$ MHz and $f_2 + 5$ MHz, Distortion Products Measured over a 3.84 MHz BW @ $f_1 - 10$ MHz and $f_2 + 10$ MHz, Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
Output Power — 19 Watts Avg.
Power Gain — 14.5 dB
Efficiency — 26%
IM3 — -37.5 dBc
ACPR — -40.5 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2140 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40 μ " Nominal.
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF5S21090L
MRF5S21090LR3
MRF5S21090LSR3

**2170 MHz, 19 W AVG.,
2 x W-CDMA, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs**



CASE 465-06, STYLE 1
NI-780
MRF5S21090L



CASE 465A-06, STYLE 1
NI-780S
MRF5S21090LSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	224 1.28	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C , 90 W CW Case Temperature 80°C , 19 W CW	$R_{\theta JC}$	0.78 0.80	$^\circ\text{C}/\text{W}$

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C7 (Minimum)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS (DC)

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 μAdc)	V _{GS(th)}	2.5	2.9	3.5	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 850 mAdc)	V _{GS(Q)}	—	3.9	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.25	—	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	5	—	S

DYNAMIC CHARACTERISTICS (1)

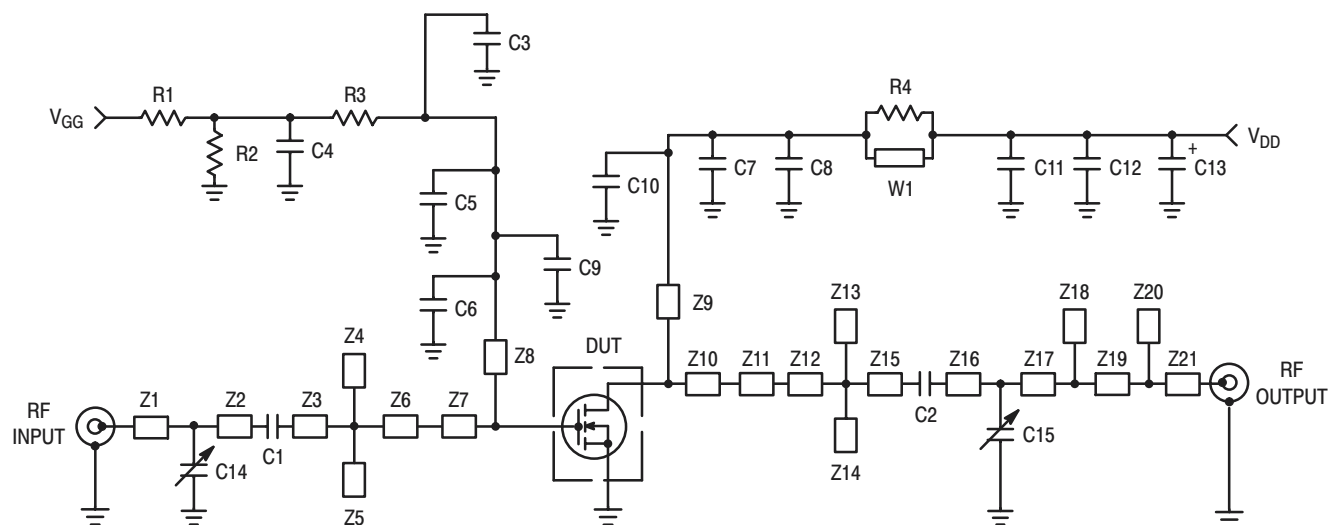
Reverse Transfer Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	1.7	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	G _{ps}	12.5	14.5	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	η	24	26	—	%
3rd Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured over 3.84 MHz BW at f ₁ –10 MHz and f ₂ +10 MHz referenced to carrier channel power.)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured over 3.84 MHz at f ₁ –5 MHz and f ₂ +5 MHz.)	ACPR	—	–40.5	–38	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 19 W Avg., I _{DQ} = 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	IRL	—	–15	–9	dB

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.



Z1	1.0856" x 0.080" Microstrip	Z12	0.609" x 0.220" Microstrip
Z2	0.130" x 0.080" Microstrip	Z13	0.290" x 0.106" Microstrip
Z3	0.230" x 0.080" Microstrip	Z14	0.290" x 0.106" Microstrip
Z4	0.347" x 0.208" Microstrip	Z15	0.080" x 0.025" Microstrip
Z5	0.090" x 0.208" Microstrip	Z16	1.080" x 0.160" Microstrip
Z6	0.650" x 0.176" Taper	Z17	0.180" x 0.080" Microstrip
Z7	0.623" x 0.610" Microstrip	Z18	0.260" x 0.147" Microstrip
Z8	0.044" x 0.881" Microstrip	Z19	0.500" x 0.080" Microstrip
Z9	0.044" x 0.869" Microstrip	Z20	0.199" x 0.147" Microstrip
Z10	1.076" x 0.446" Microstrip	Z21	0.365" x 0.080" Microstrip
Z11	0.320" x 0.393" Microstrip	PCB	Arlon GX0300-55-22, 0.03", $\epsilon_r = 2.55$

Figure 1. MRF5S21090 Test Circuit Schematic

Table 1. MRF5S21090 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1	9.1 pF Chip Capacitor, B Case	100B9R1CP 500X	ATC
C2	8.2 pF Chip Capacitor, B Case	100B8R2CP 500X	ATC
C3	2.0 pF Chip Capacitor, B Case	100B2R0BP 500X	ATC
C4, C12	0.1 μ F Chip Capacitors, B Case	CDR33BX104AKWS	Kemet
C5	5.6 pF Chip Capacitor, B Case	100B5R6CP 500X	ATC
C6	5.1 pF Chip Capacitor, B Case	100B5R1CP 500X	ATC
C7	7.5 pF Chip Capacitor, B Case	100B7R5JP 500X	ATC
C8	1.2 pF Chip Capacitor, B Case	100B1R2BP 500X	ATC
C9, C10	0.56 μ F Chip Capacitors, B Case	700A561MP 150X	ATC
C11	1000 pF Chip Capacitor, B Case	100B102JP 500X	ATC
C13	470 μ F, 35 V Electrolytic Capacitor	95F4579	Newark
C14, C15	0.4 – 2.5 Variable Capacitors, Gigatrim	44F3367	Newark
R1	1 k Ω Chip Resistor	D5534M07B1K00R	Newark
R2	560 k Ω Chip Resistor	CR1206 564JT	Newark
R3, R4	12 Ω Chip Resistors	RM73B2B120JT	Garrett Electronics
W1	Wire Strap		

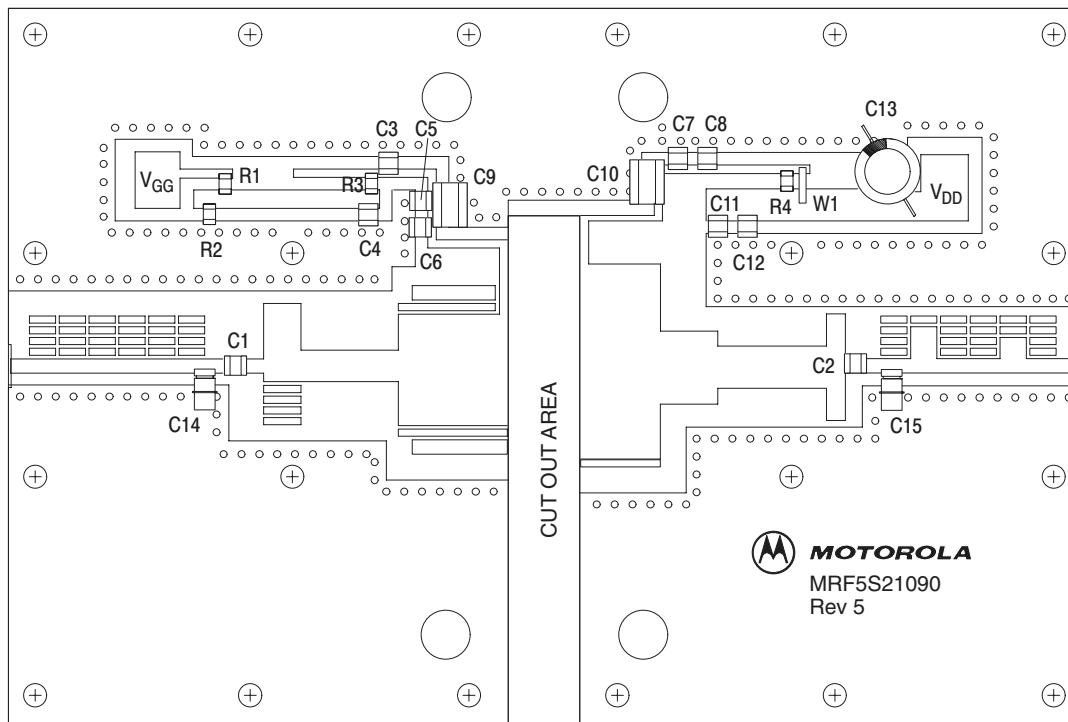


Figure 2. MRF5S21090 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

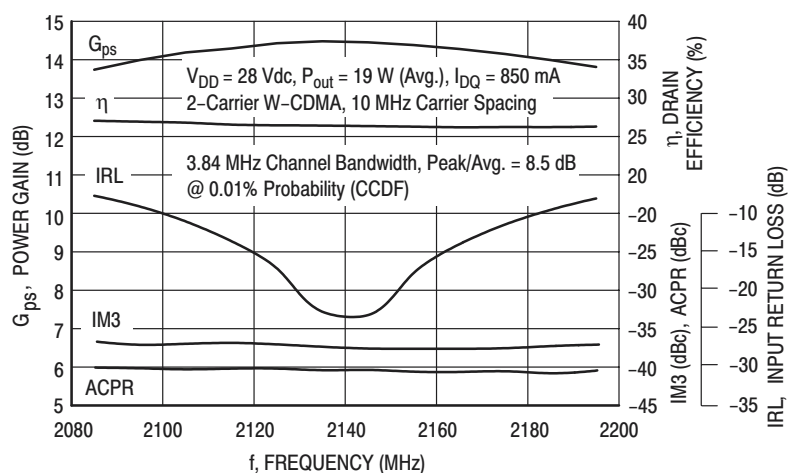


Figure 3. 2-Carrier W-CDMA Broadband Performance

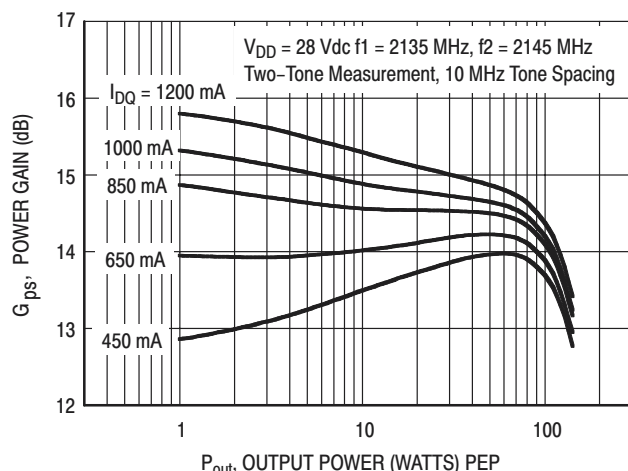


Figure 4. Two-Tone Power Gain versus Output Power

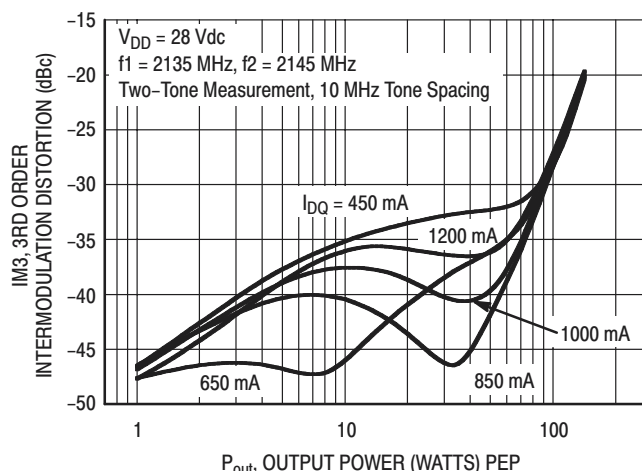


Figure 5. 3rd Order Intermodulation Distortion versus Output Power

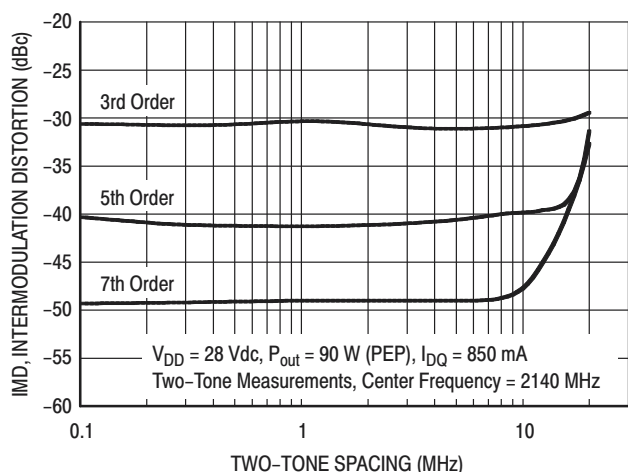


Figure 6. Intermodulation Distortion Products versus Tone Spacing

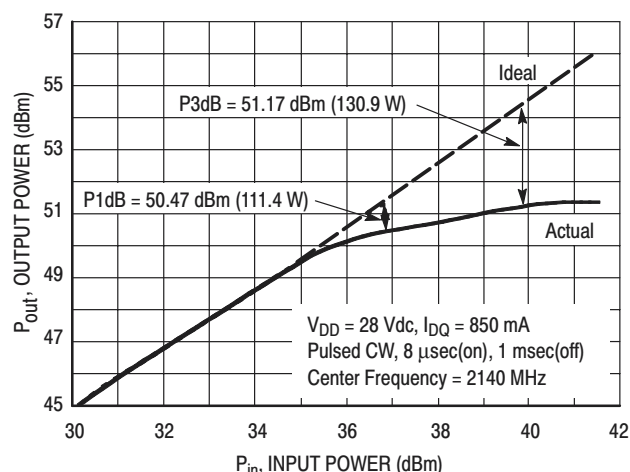


Figure 7. Pulse CW Output Power versus Input Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

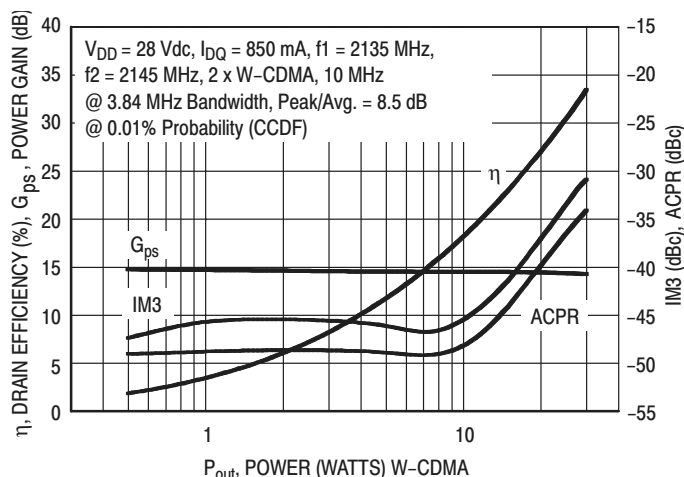


Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

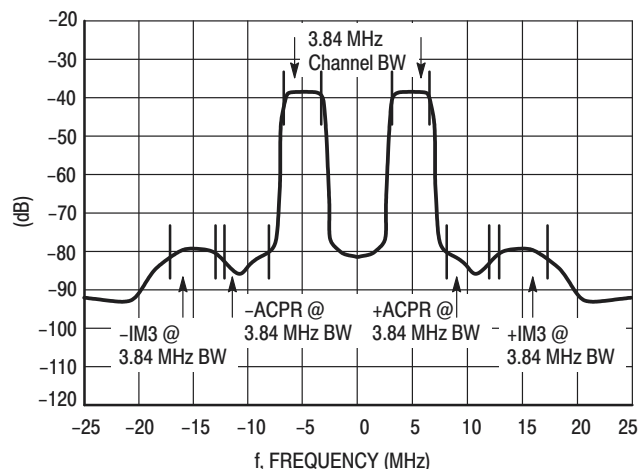


Figure 9. 2-Carrier W-CDMA Spectrum

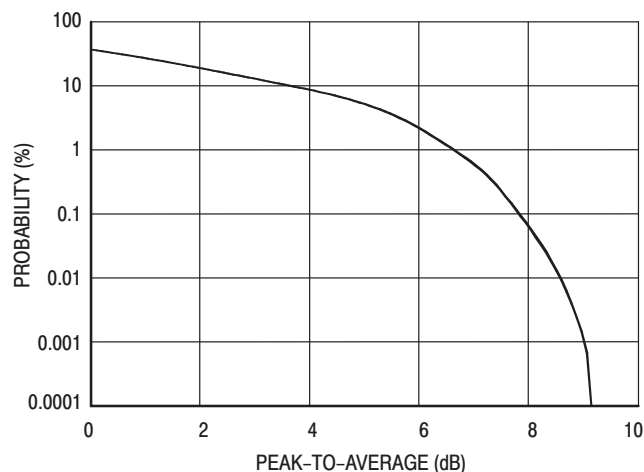
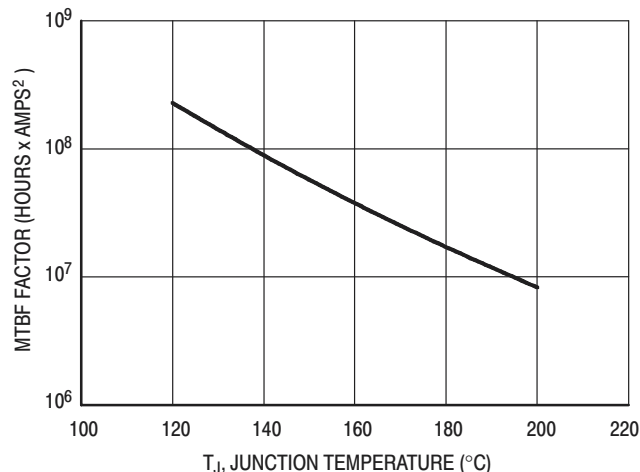
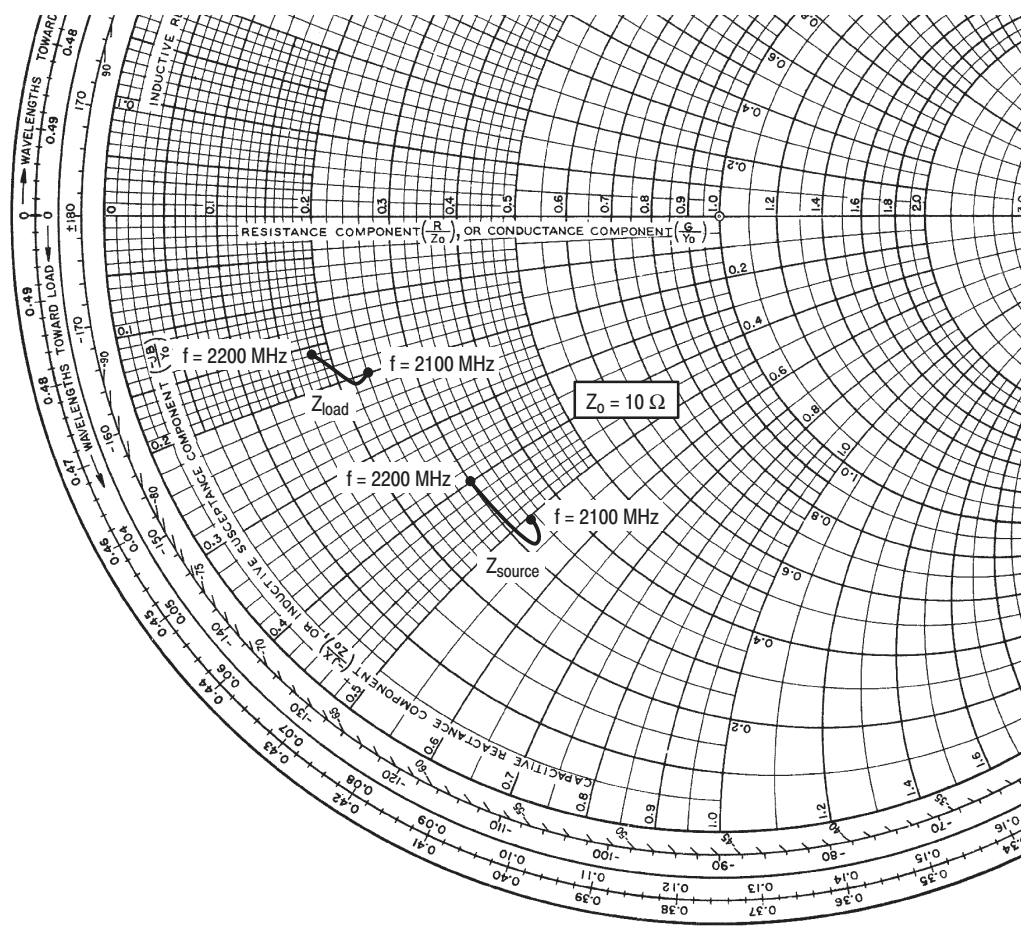


Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single Carrier Test Signal



This above graph displays calculated MTBF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 11. MTBF Factor versus Junction Temperature



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 850 \text{ mA}$, $P_{out} = 19 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
2100	$3.4 - j5.1$	$2.4 - j2.0$
2120	$3.2 - j5.4$	$2.2 - j2.1$
2160	$3.0 - j4.4$	$2.1 - j1.9$
2200	$3.0 - j4.0$	$1.8 - j1.6$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

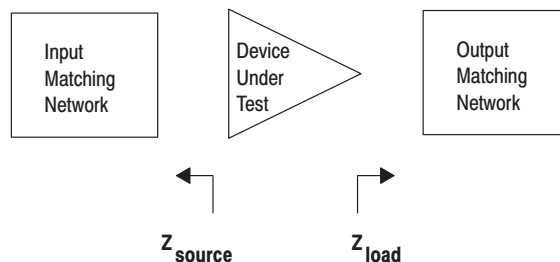


Figure 12. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

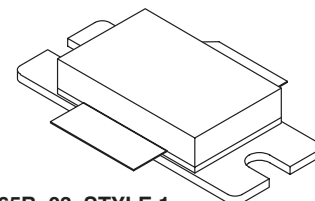
Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

- Typical W-CDMA Performance for 2140 MHz, 28 Volts
4.096 MHz BW @ 5 MHz offset, 1 PERCH 15 DTCH:
Output Power — 11.5 Watts
Efficiency — 16%
Gain — 12.2 dB
ACPR — -45 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2110 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

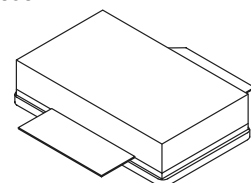
MRF21090

MRF21090S

2170 MHz, 90 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465B-03, STYLE 1
NI-880
MRF21090



CASE 465C-02, STYLE 1
NI-880S
MRF21090S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	270 1.54	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model MRF21090 MRF21090S	2 (Minimum) 1 (Minimum)
Machine Model MRF21090 MRF21090S	M3 (Minimum) M4 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc

ON CHARACTERISTICS

Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 Adc)	g _{fs}	—	7.2	—	S
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 300 μA)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 V, I _D = 750 mA)	V _{GS(Q)}	3	3.8	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 V, I _D = 1 A)	V _{DS(on)}	—	0.1	0.6	Vdc

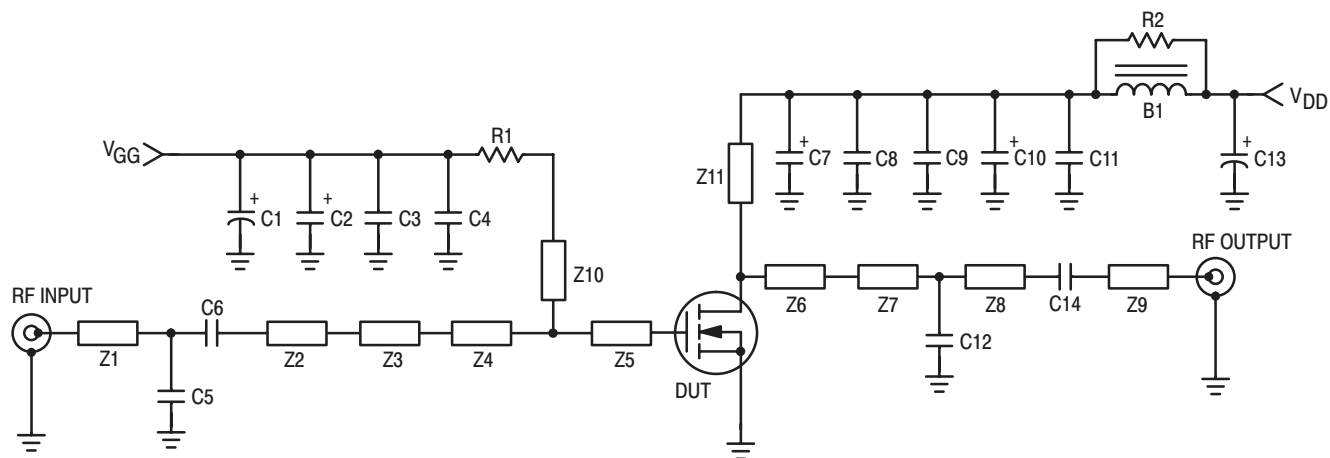
DYNAMIC CHARACTERISTICS

Reverse Transfer Capacitance (1) (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	4.2	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 90 W PEP, I _{DQ} = 750 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz and f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	G _{ps}	10	11.7	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 90 W PEP, I _{DQ} = 750 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz and f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	η	30	33	—	%
Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 90 W PEP, I _{DQ} = 750 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz and f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	IMD	—	–30	–27.5	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 90 W PEP, I _{DQ} = 750 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz and f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	IRL	—	–12	–9.0	dB
Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 75 W CW, I _{DQ} = 750 mA, f = 2170 MHz)	G _{ps}	—	11.7	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 75 W CW, I _{DQ} = 750 mA, f = 2170 MHz)	η	—	41	—	%
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 90 W CW, I _{DQ} = 750 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1	Ferrite Bead, Fair Rite #2743019447	Z7	10.23 x 2.09 mm Microstrip
C1, C13	470 μ F, 50 V Electrolytic Capacitors	Z8	6.03 x 2.09 mm Microstrip
C2, C10	22 μ F, 35 V Tantalum Surface Mount Chip Capacitors, Kemet	Z9	23.98 x 2.09 mm Microstrip
C3, C9	20 nF Chip Capacitors, ATC #100B203MCA500X	Z10	29.82 x 1.15 mm Microstrip
C4, C8	5.1 pF Chip Capacitors, ATC #100B5R1CCA500X	Z11	17.08 x 1.15 mm Microstrip
C5, C12	0.4 – 2.5 pF Variable Capacitors, Johanson Gigatrim	WS1, WS2	Beryllium Copper Wear Blocks 5 mils Thick
C6	10 pF Chip Capacitor, ATC #100B100JCA500X		Brass Banana Jack and Nut
C7	1 μ F, 35 V Tantalum Surface Mount Chip Capacitor, Kemet		Red Banana Jack and Nut
C11	1 nF Chip Capacitor, ATC #100B102JCA500X		Green Banana Jack and Nut
C14	8.2 pF Chip Capacitor, ATC #100B8R2CCA500X		Type N Jack Connectors, 3052–1648–10, Omni Specra
R1	13 Ω , 1/4 W Chip Resistor, Garret Instrument #RM73B2B130JT,		4–40 Head Screws 0.125" Long
R2	12 Ω , 1/4 W Chip Resistor, Garret Instrument #RM73B2B120JT		4–40 Head Screws 0.188" Long
Z1	30.7 x 2.09 mm Microstrip		4–40 Head Screws 0.312" Long
Z2	5.99 x 2.09 mm Microstrip		4–40 Head Screws 0.438" Long
Z3	7.55 x 9.89 mm Microstrip	Endplates Brass	Endplates for Copper Bedstead
Z4	3.77 x 15.71 mm Microstrip	Bedstead	Copper Bedstead/Heatsink
Z5	6.89 x 26.17 mm Microstrip	Insert	Copper Bedstead Insert
Z6	14.93 x 32.05 mm Microstrip	Raw PCB	0.030" Glass Teflon [®] , 2 oz Copper Clad
		RF Circuit	3" x 5" Arion
			3" x 5" Copper Clad PCB Teflon [®] , MRF21090, CMR

Figure 1. MRF21090 Test Circuit Schematic

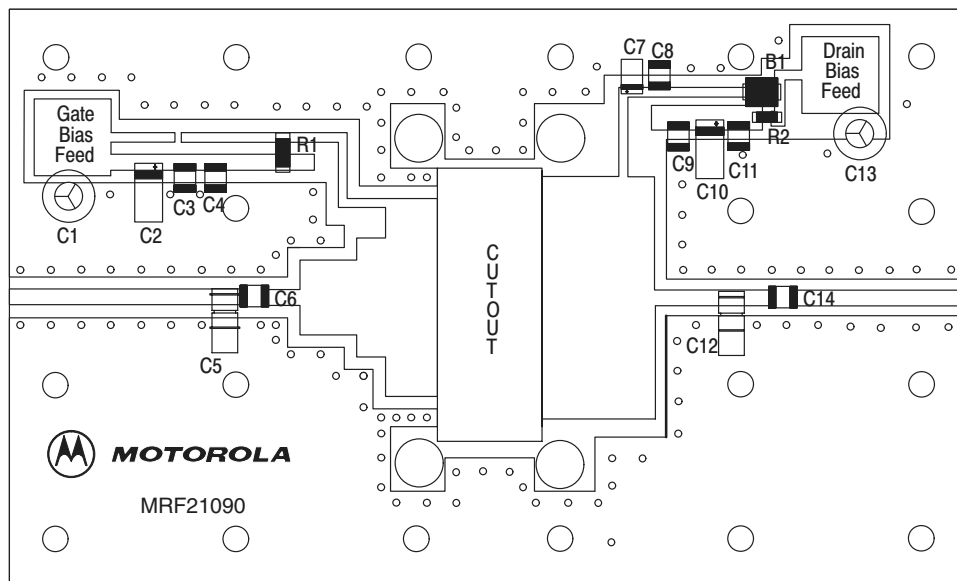


Figure 2. MRF21090 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL PERFORMANCE (IN MOTOROLA TEST FIXTURE)

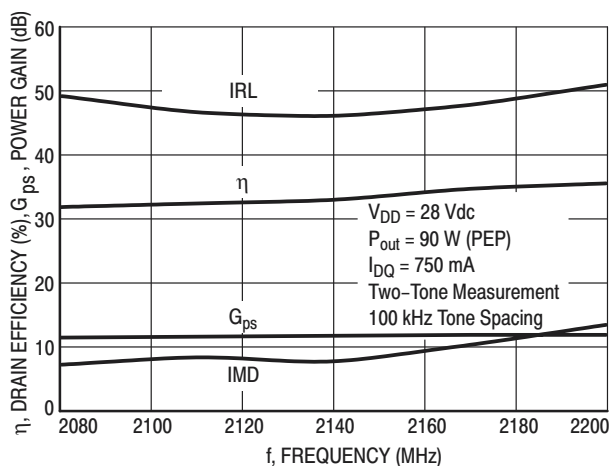


Figure 3. Class AB Broadband Circuit Performance

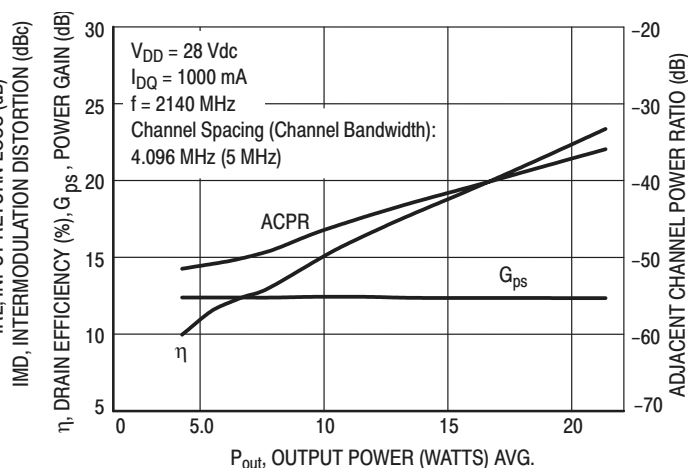


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

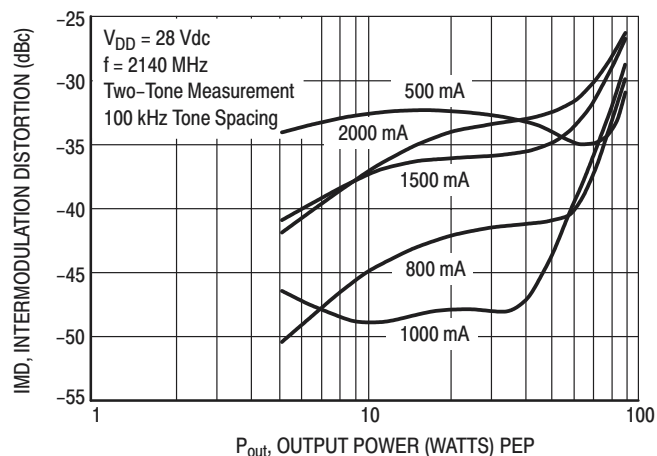


Figure 5. Intermodulation Distortion versus Output Power

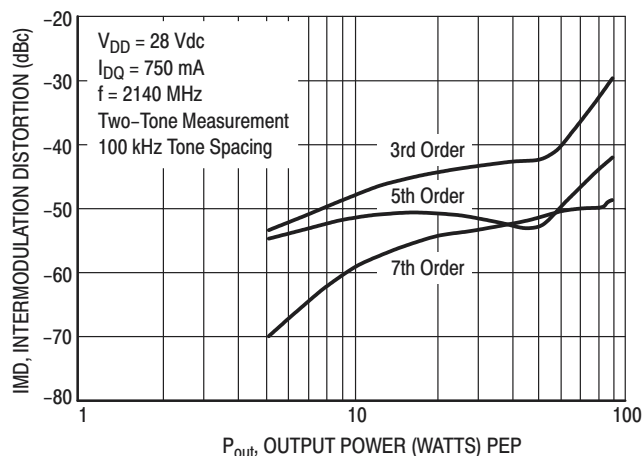


Figure 6. Intermodulation Distortion Products versus Output Power

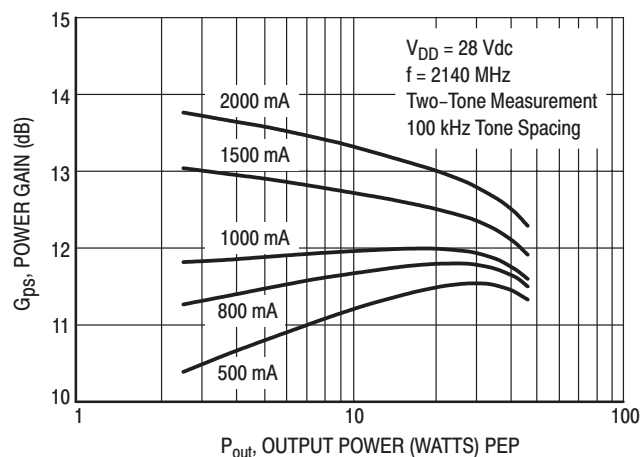


Figure 7. Power Gain versus Output Power

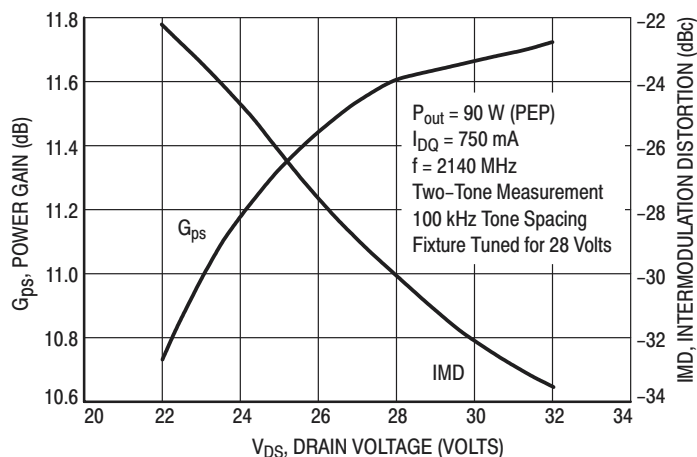
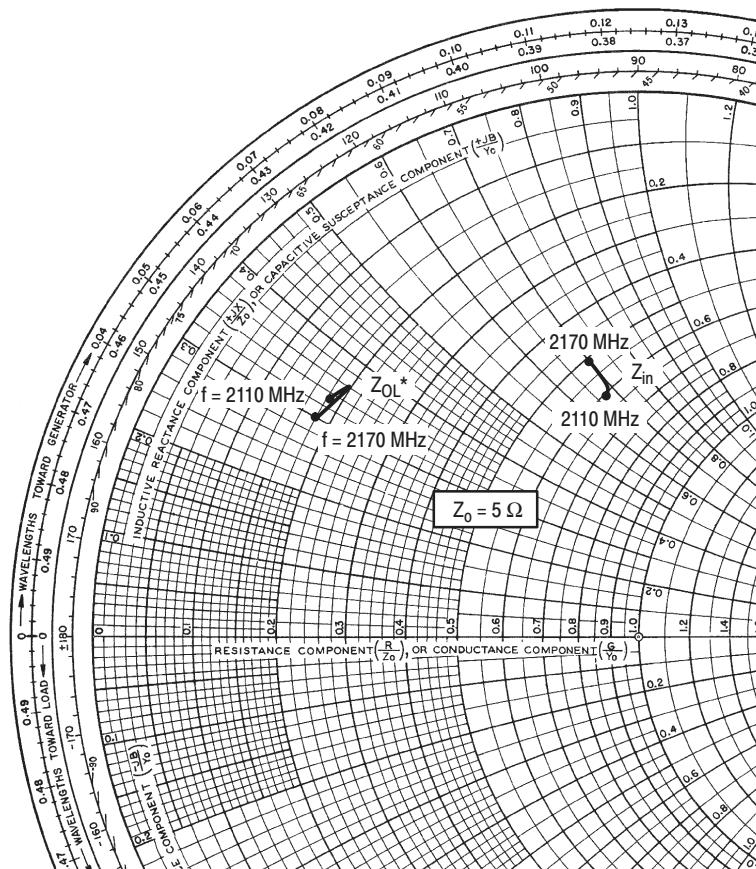


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 750 \text{ mA}$, $P_{out} = 90 \text{ W (PEP)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
2110	$3.03 + j3.40$	$0.92 + j1.67$
2140	$3.02 + j3.46$	$0.97 + j1.80$
2170	$2.60 + j3.50$	$0.90 + j1.52$

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given power, voltage, IMD, bias current and frequency.

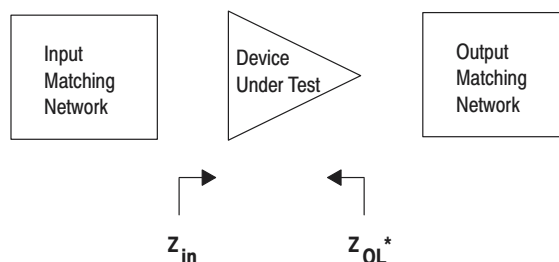


Figure 9. Series Equivalent Input and Output Impedance

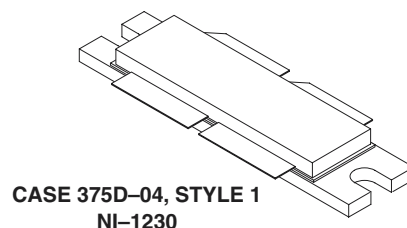
The RF Sub-Micron MOSFET Line **RF Power Field Effect Transistor** N-Channel Enhancement-Mode Lateral MOSFET

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- W-CDMA Performance @ -45 dBc, 5 MHz Offset, 15 DTCH, 1 Perch
Output Power — 14 Watts (Avg.)
Power Gain — 11.5 dB
Efficiency — 16%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2170 MHz, 120 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

MRF21120

**2170 MHz, 120 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFET**



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	389 2.22	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 20 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
ON CHARACTERISTICS (1)					
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.8	—	S
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 200 μA)	V _{GS(th)}	2.5	3	3.8	Vdc
Gate Quiescent Voltage (V _{DS} = 28 V, I _D = 500 mA)	V _{GS(Q)}	3	3.9	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 V, I _D = 2 A)	V _{DS(on)}	—	0.38	0.5	Vdc
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	2.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)					
Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	G _{ps}	10.5	11.4	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	η	30	34.5	—	%
Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	IMD	—	–31	–28	dB
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	IRL	—	–12	–9	dB
Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2140.0 MHz, f ₂ = 2140.1 MHz)	G _{ps}	—	11.5	—	dB
Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz)	G _{ps}	—	11.5	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz)	η	—	34.5	—	%
Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz)	IMD	—	–31	—	dB
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz)	IRL	—	–12	—	dB
Power Output, 1 dB Compression Point (V _{DD} = 28 Vdc, CW, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz)	P1dB	—	120	—	Watts

(1) Each side of device measured separately.

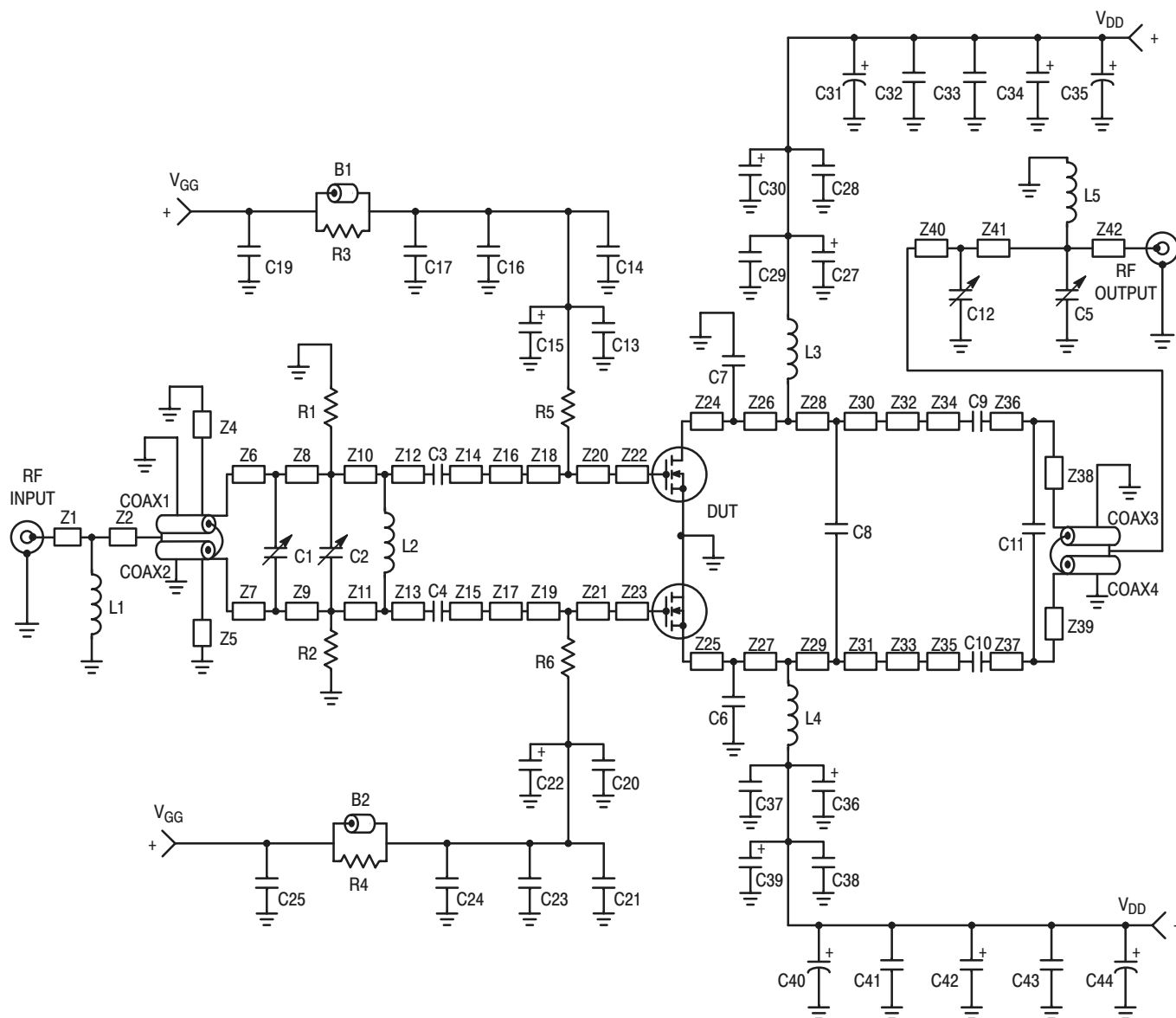
(2) Device measured in push–pull configuration.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) (continued)					
Common–Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\text{ W CW}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 2170.0\text{ MHz}$)	G_{ps}	—	10.5	—	dB
Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\text{ W CW}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f_1 = 2170.0\text{ MHz}$)	η	—	42	—	%
Output Mismatch Stress ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\text{ W CW}$, $I_{DQ} = 2 \times 500\text{ mA}$, $f = 2.17\text{ GHz}$, $VSWR = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(2) Device measured in push–pull configuration.



B1, B2	Ferrite Beads, Fair Rite	Z2	0.320" x 0.080" Microstrip
C1, C2, C12	0.6 – 4.5 pF Variable Capacitors, Johanson Gigatrim	Z4, Z5	1.050" x 0.080" Microstrip
C3, C4, C9, C10	10 pF Chip Capacitors, B Case, ATC	Z6, Z7	0.120" x 0.080" Microstrip
C5	0.4 – 2.5 pF Variable Capacitor, Johanson Gigatrim	Z8, Z9	0.140" x 0.080" Microstrip
C6, C7	2.0 pF Chip Capacitors, B Case, ATC	Z10, Z11	0.610" x 0.080" Microstrip
C8	0.5 pF Chip Capacitor, B Case, ATC	Z12, Z13	0.135" x 0.080" Microstrip
C11	0.2 pF Chip Capacitor, B Case, ATC	Z14, Z15	0.130" x 0.080" Microstrip
C13, C20, C29, C37	5.1 pF Chip Capacitors, B Case, ATC	Z16, Z17	0.300" x 0.350" Microstrip
C14, C21, C28, C38	91 pF Chip Capacitors, B Case, ATC	Z18, Z19	0.150" x 0.500" Microstrip
C15, C22, C27, C34, C36, C42	22 µF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet	Z20, Z21	0.075" x 0.500" Microstrip
C16, C23, C33, C43	0.039 µF Chip Capacitors, B Case, ATC	Z22, Z23	0.330" x 0.500" Microstrip
C17, C24, C32, C41	1000 pF Chip Capacitors, B Case, ATC	Z24, Z25	0.100" x 0.550" Microstrip
C19, C25	0.022 µF Chip Capacitors, B Case, ATC	Z26, Z27	0.175" x 0.550" Microstrip
C30, C39	1.0 µF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet	Z28, Z29	0.045" x 0.550" Microstrip
C31, C40	100 µF, 50 V Electrolytic Capacitors, Sprague	Z30, Z31	0.190" x 0.325" Microstrip
C35, C44	470 µF, 63 V Electrolytic Capacitors, Sprague	Z32, Z33	0.080" x 0.325" Microstrip
Coax1, Coax2	25 Ω Semi Rigid Coax, 70 mil OD, 1.05" Long	Z34, Z35	0.515" x 0.080" Microstrip
Coax3, Coax4	50 Ω Semi Rigid Coax, 85 mil OD, 1.05" Long	Z36, Z37	0.020" x 0.080" Microstrip
L1, L5	5.0 nH Minispring Inductors, Coilcraft	Z38, Z39	0.565" x 0.080" Microstrip
L2	8.0 nH Minispring Inductor, Coilcraft	Z40	0.100" x 0.080" Microstrip
L3, L4	7.15 nH Microspring Inductors, Coilcraft	Z41	0.470" x 0.080" Microstrip
R1, R2	1 kΩ, 1/4 W Fixed Metal Film Resistors, Dale	Z42	0.100" x 0.080" Microstrip
R3, R4	270 Ω, 1/8 W Fixed Film Chip Resistors, Dale	Board Material	0.03" Teflon®, ε _r = 2.55 Copper
R5, R6	1.2 kΩ, 1/8 W Fixed Film Chip Resistors, Dale	Connectors	Clad, 2 oz. Cu
Z1	0.150" x 0.080" Microstrip		N-Type Panel Mount, Stripline

Figure 1. 2.1 – 2.2 GHz Broadband Test Circuit Schematic

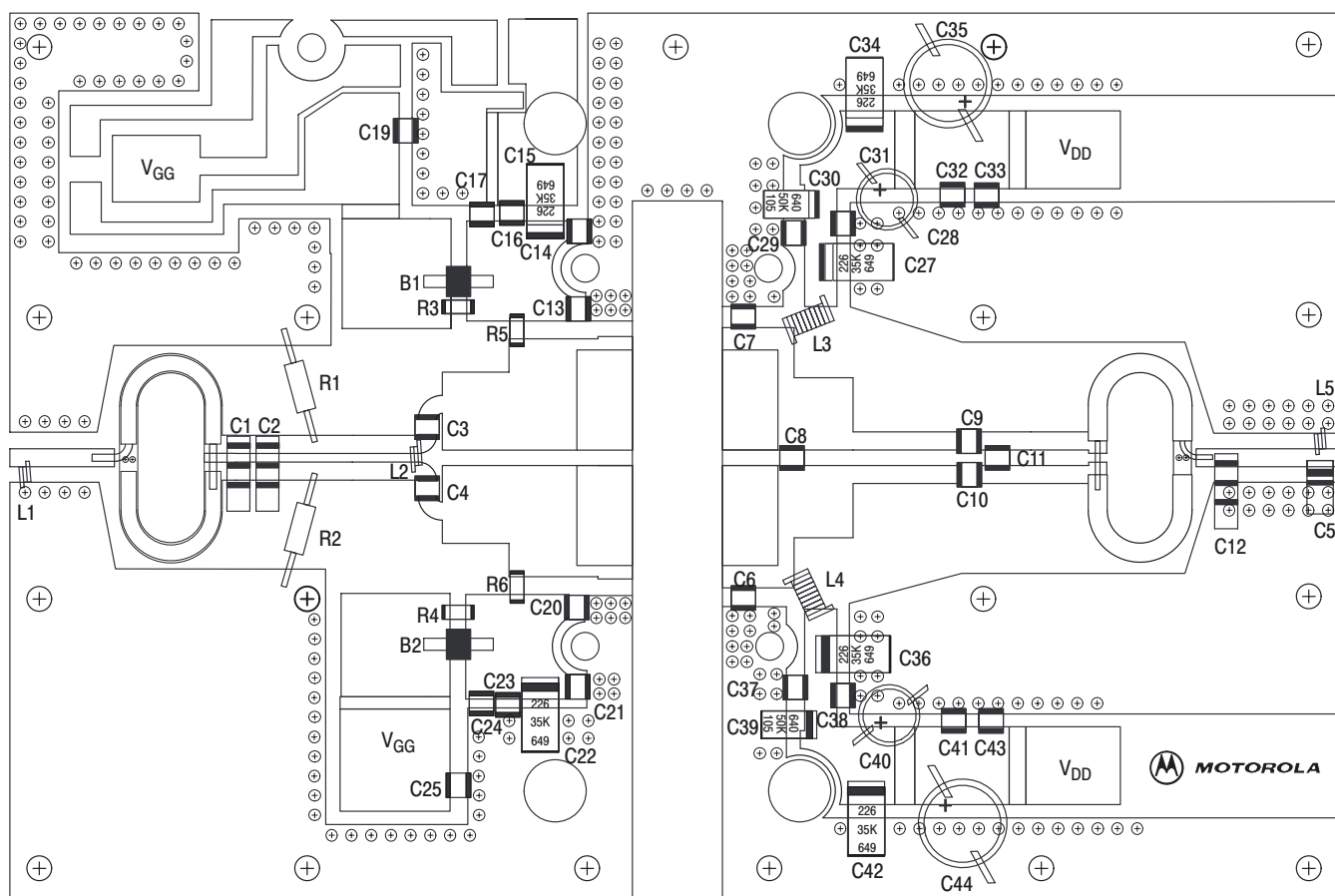


Figure 2.2.1 – 2.2 GHz Broadband Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

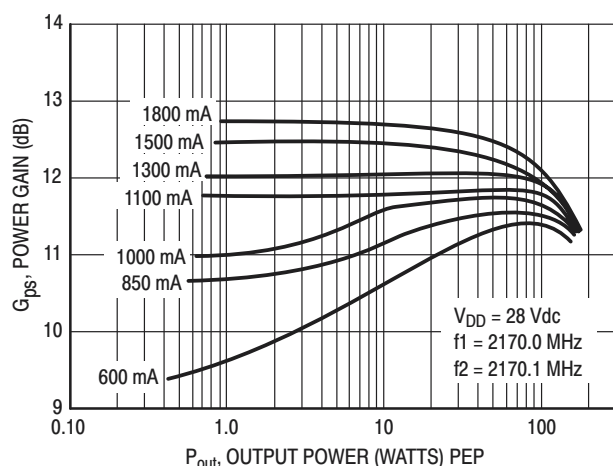


Figure 3. Power Gain versus Output Power

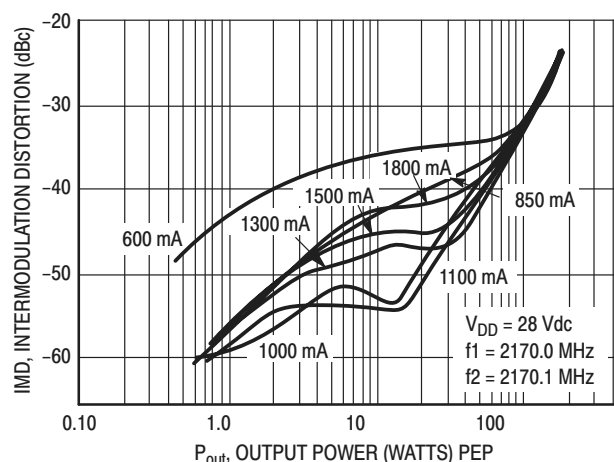


Figure 4. Intermodulation Distortion versus Output Power

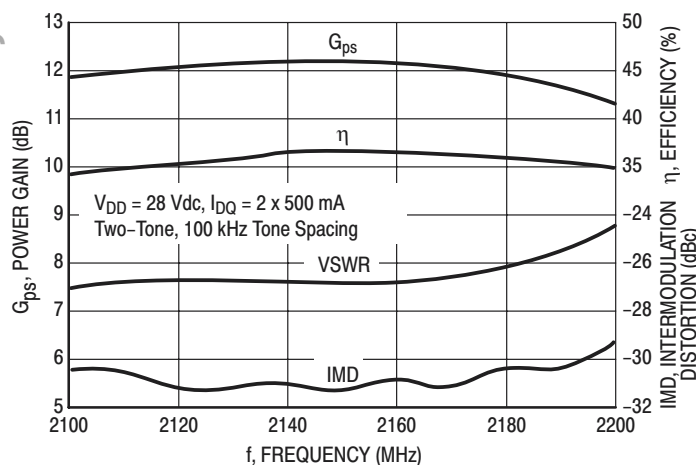


Figure 5. Class AB Broadband Circuit Performance

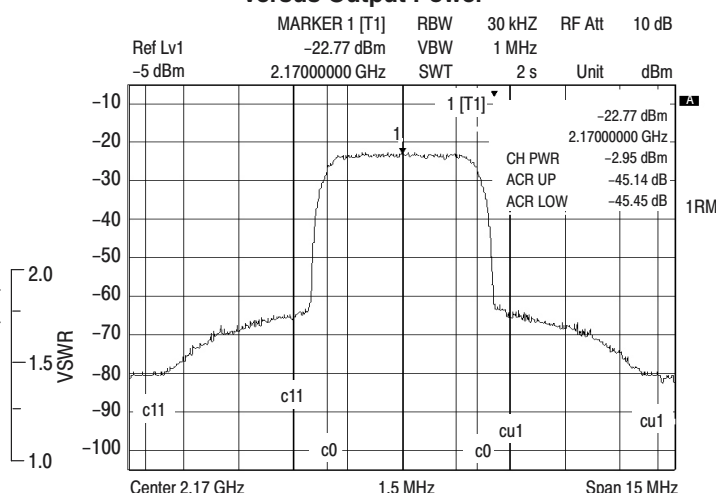


Figure 6. 2.17 GHz W-CDMA Mask at 14 Watts (Avg.), 5 MHz Offset, 15 DTCH, 1 Perch

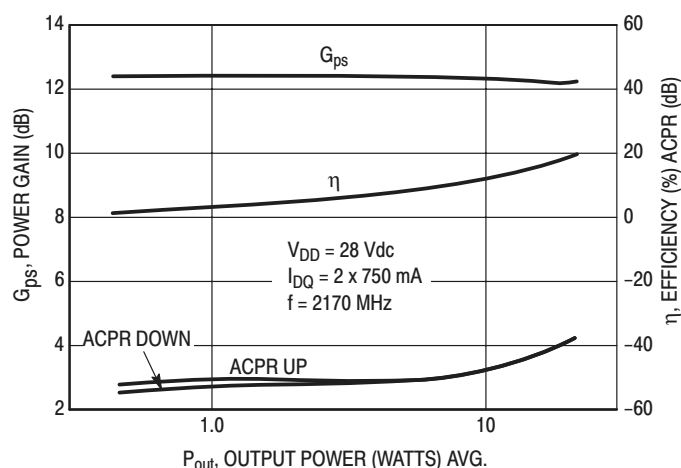


Figure 7. Power Gain, Efficiency, ACPR versus Output Power (W-CDMA)

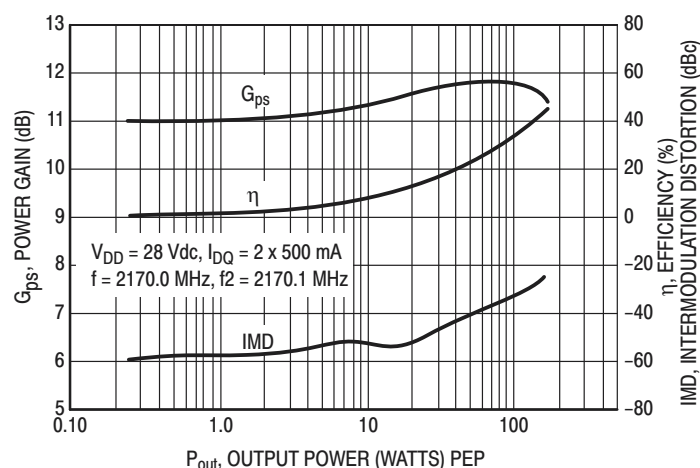
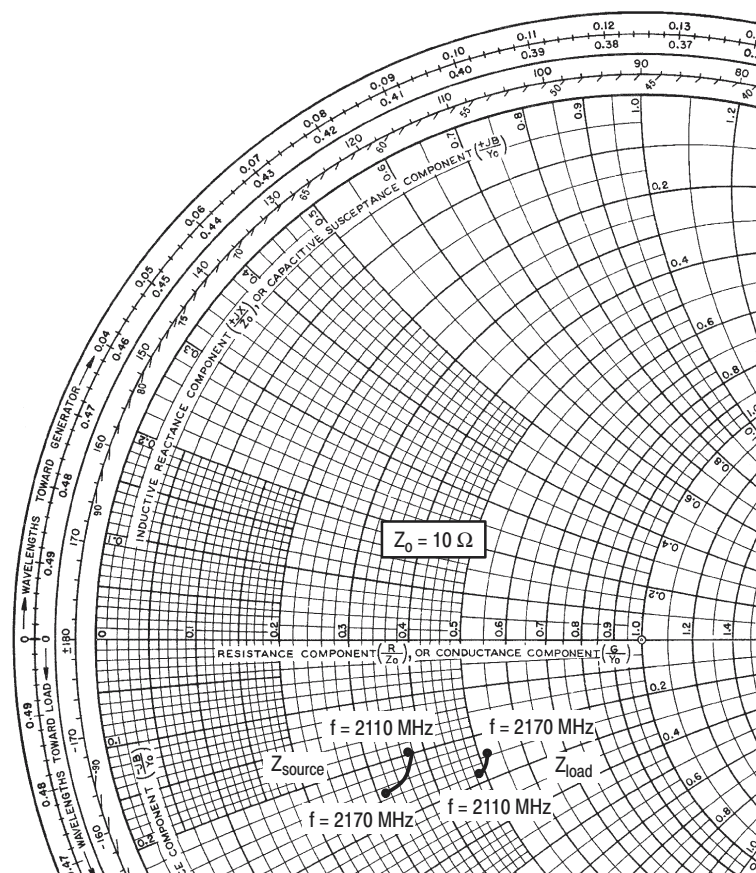


Figure 8. Power Gain, Efficiency, IMD versus Output Power



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 2 \times 500 \text{ mA}$, $P_{out} = 120 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
2110	$3.7 - j2.0$	$4.9 - j2.8$
2140	$3.5 - j2.4$	$5.1 - j2.7$
2170	$3.1 - j2.5$	$5.2 - j2.5$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

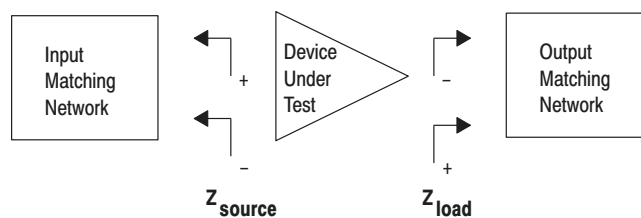


Figure 9. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

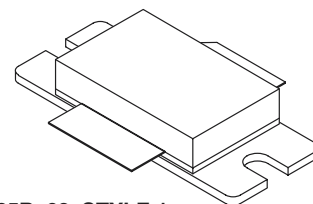
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

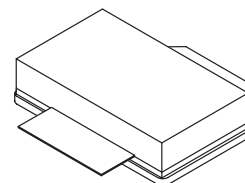
- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 1600$ mA, $f_1 = 2.1125$ GHz, $f_2 = 2.1225$ GHz, Channel bandwidth = 3.84 MHz, adjacent channels at ± 5 MHz, ACPR and IM3 measured in 3.84 MHz bandwidth. Peak/Avg = 8.5 dB @ 0.01% probability on CCDF.
 Output Power — 20 Watts
 Efficiency — 18%
 Gain — 13 dB
 IM3 — -43 dBc
 ACPR — -45 dBc
- 100% Tested under 2-carrier W-CDMA
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2170 MHz, 125 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF21125
MRF21125S
MRF21125SR3

2170 MHz, 125 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465B-03, STYLE 1
NI-880
MRF21125



CASE 465C-02, STYLE 1
NI-880S
MRF21125S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	330 1.89	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.53	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 Adc)	g _{fs}	—	10.8	—	S
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 300 μA)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 V, I _D = 1300 mA)	V _{GS(Q)}	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 V, I _D = 1 A)	V _{DS(on)}	—	0.12	—	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	5.4	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth, IM3 measured in 3.84 MHz Bandwidth. Peak/Avg = 8.5 dB @ 0.01% probability on CCDF.					
Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 20 W Avg, 2–carrier W–CDMA, I _{DQ} = 1600 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	G _{ps}	12	13	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 20 W Avg, 2–carrier W–CDMA, I _{DQ} = 1600 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	η	17	18	—	%
Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 20 W Avg, 2–carrier W–CDMA, I _{DQ} = 1600 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured at f ₁ –10 MHz and f ₂ +10 MHz referenced to carrier channel power.)	IM3	—	–43	–40	dBc
Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 20 W Avg, 2–carrier W–CDMA, I _{DQ} = 1600 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured at f ₁ –5 MHz and f ₂ +5 MHz referenced to carrier channel power.)	ACPR	—	–45	–40	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 20 W Avg, 2–carrier W–CDMA, I _{DQ} = 1600 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	IRL	—	–12	–9.0	dB
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 125 W CW, I _{DQ} = 1600 mA, f = 2170 MHz, VSWR = 5:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

TYPICAL TWO-TONE PERFORMANCE (In Motorola Test Fixture)

Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 125\text{ W PEP}$, $I_{DQ} = 1600\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	G_{ps}	—	12	—	dB
Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 125\text{ W PEP}$, $I_{DQ} = 1600\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	η	—	34	—	%
Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 125\text{ W PEP}$, $I_{DQ} = 1600\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	IMD	—	-30	—	dBc

TYPICAL CW PERFORMANCE

Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 125\text{ W CW}$, $I_{DQ} = 1600\text{ mA}$, $f_1 = 2170.0\text{ MHz}$)	G_{ps}	—	11.5	—	dB
Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 125\text{ W CW}$, $I_{DQ} = 1600\text{ mA}$, $f = 2170.0\text{ MHz}$)	η	—	46	—	%

Freescale Semiconductor, Inc.

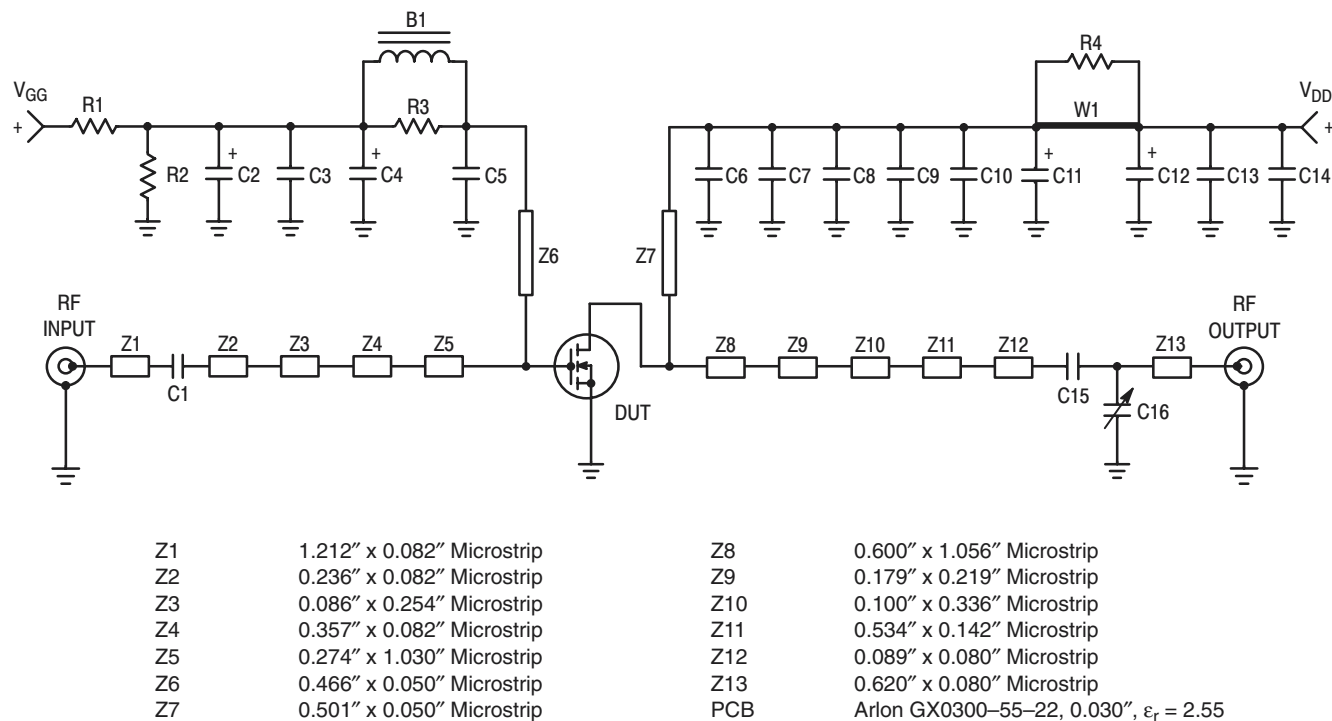


Figure 1. MRF21125 Test Circuit Schematic

Table 1. MRF21125 Test Circuit Component Designations and Values

Designators	Description
B1	Ferrite Bead (Square), Fair Rite #2743019447
C1	9.1 pF Chip Capacitor, B Case, ATC #100B9R1CCA500X
C2, C4, C11, C12	22 μ F, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T491X226K035AS4394
C3, C7	20000 pF Chip Capacitors, B Case, ATC #100B203JCA50X
C5, C14	5.1 pF Chip Capacitors, B Case, ATC #100B5R1CCA500X
C6	100000 pF Chip Capacitor, B Case, ATC #100B104JCA50X
C8	10000 pF Chip Capacitor, B Case, ATC #100B103JCA50X
C9	7.5 pF Chip Capacitor, B Case, ATC #100B7R5CCA500X
C10	1.2 pF Chip Capacitor, B Case, ATC #100B1R2CCA500X
C13	0.1 μ F Chip Capacitor, Kemet #CDR33BX104AKWS
C15	16 pF Chip Capacitor, B Case, ATC #100B160KP500X
C16	0.6 – 4.5 pF Variable Capacitor, Johanson Gigatrim #27271SL
R1	1.0 k Ω , 1/8 W Chip Resistor
R2	560 k Ω , 1/8 W Chip Resistor
R3	4.7 Ω , 1/8 W Chip Resistor
R4	12 Ω , 1/8 W Chip Resistor
W1	Solid Copper Buss Wire, 16 AWG

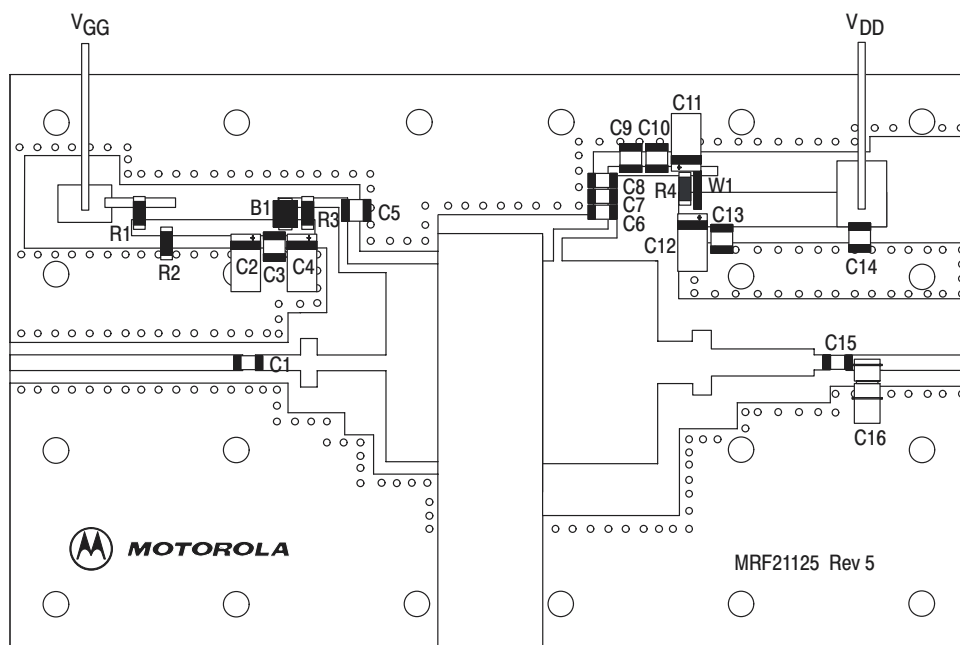


Figure 2. MRF21125 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

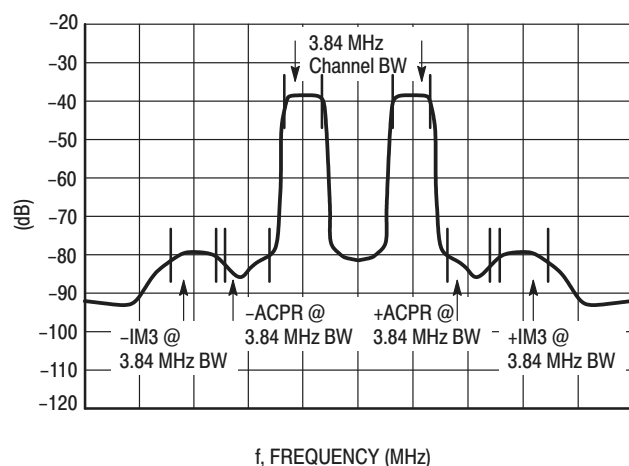


Figure 3. 2-Carrier (10 MHz Spacing) W-CDMA Spectrum

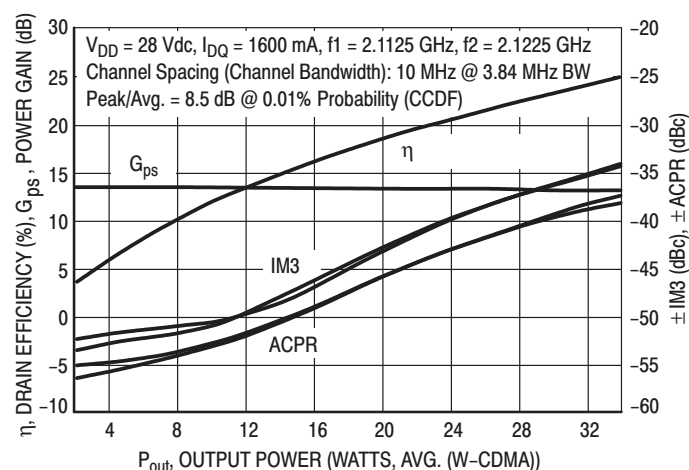


Figure 4. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

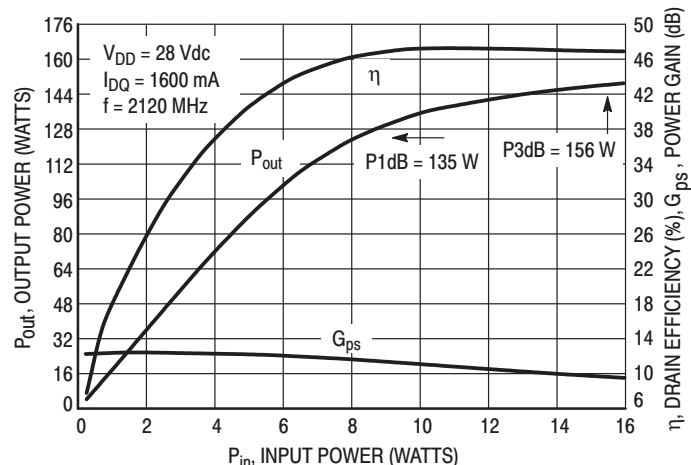


Figure 5. CW Performance

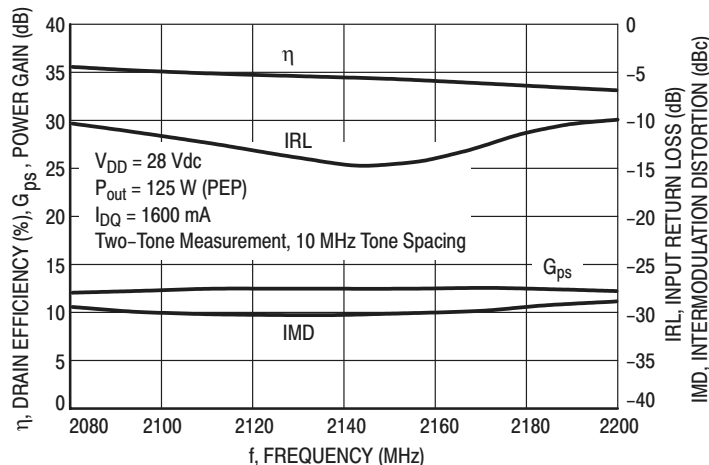


Figure 6. Broadband Linearity Performance

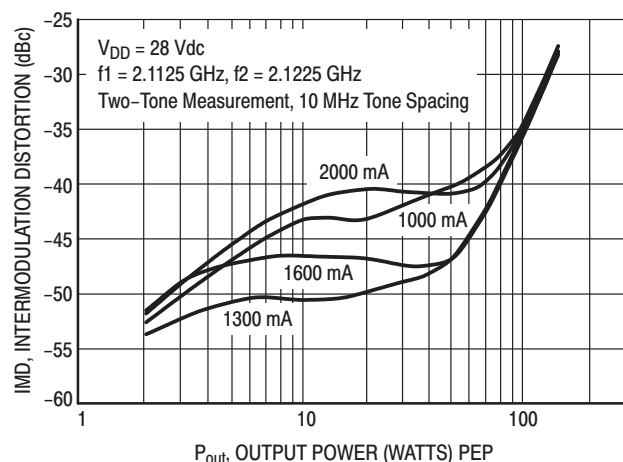


Figure 7. Intermodulation Distortion versus Output Power

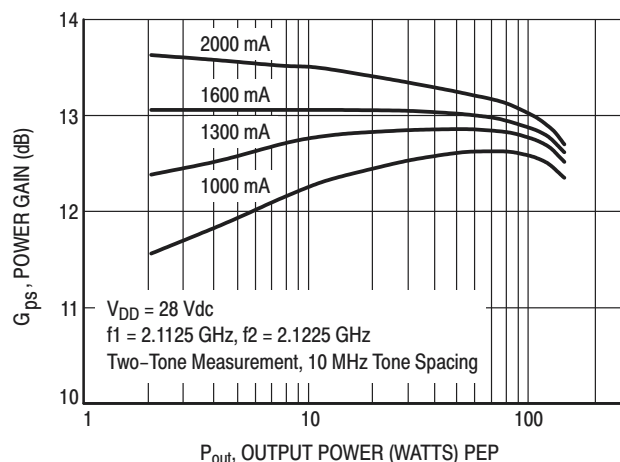
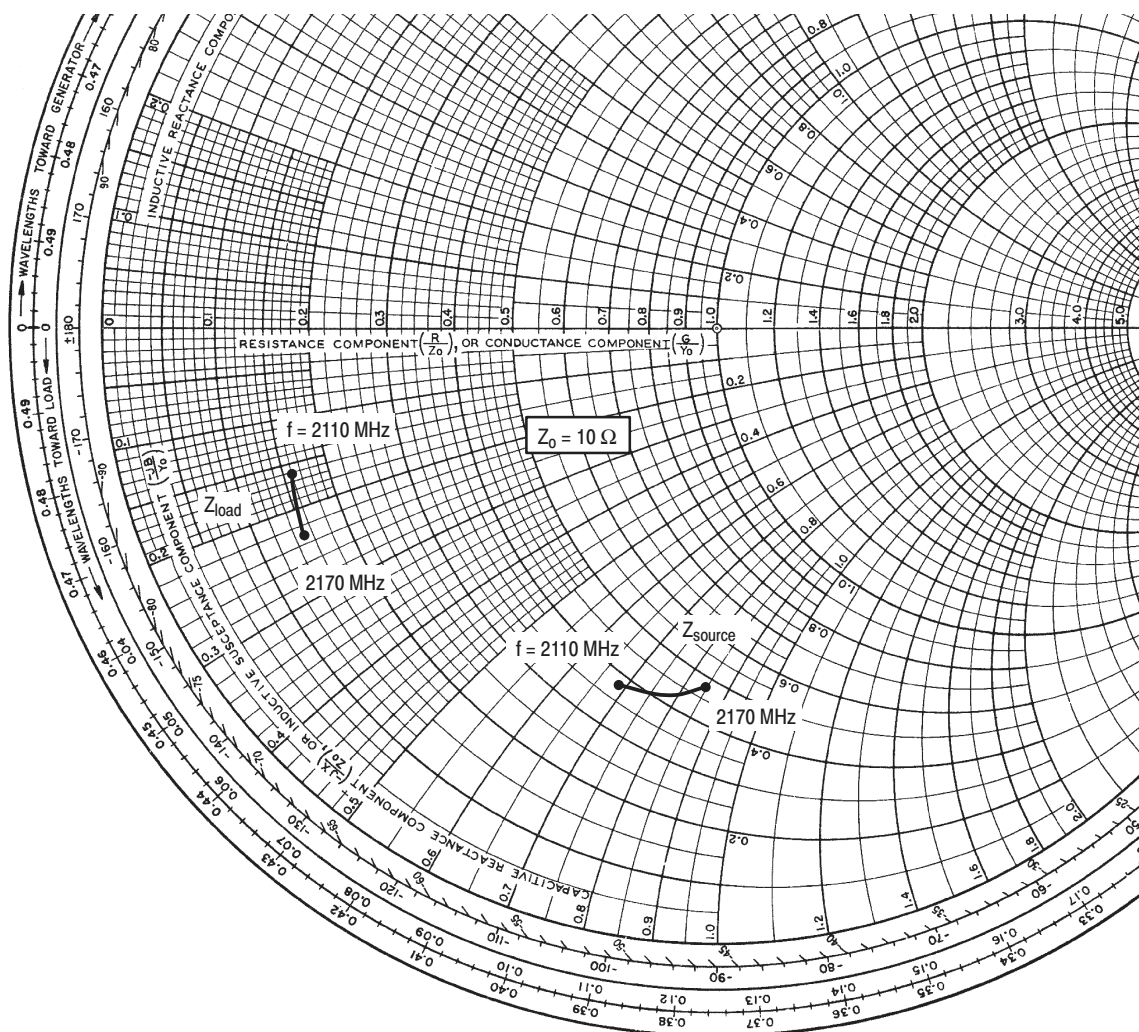


Figure 8. Power Gain versus Output Power



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 1600 \text{ mA}$, $P_{out} = 20 \text{ W (Avg.)}$, 2-Carrier W-CDMA

f MHz	Z_{source} Ω	Z_{load} Ω
2110	$3.81 - j6.86$	$1.56 - j1.58$
2140	$4.33 - j7.90$	$1.53 - j1.90$
2170	$4.84 - j8.46$	$1.48 - j2.26$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

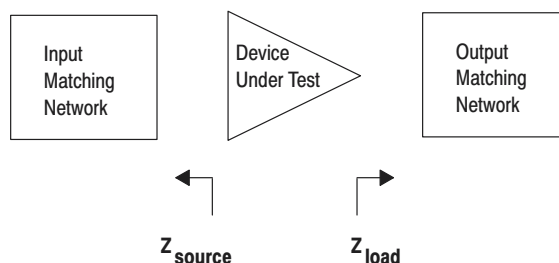


Figure 9. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

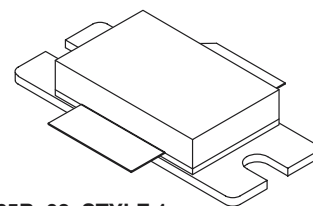
Designed for W-CDMA base station applications at frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 1200$ mA, $f_1 = 2135$ MHz, $f_2 = 2145$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ $f_1 - 5$ MHz and $f_2 + 5$ MHz, Distortion Products Measured over a 3.84 MHz BW @ $f_1 - 10$ MHz and $f_2 + 10$ MHz, Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
 - Output Power — 28 Watts Avg.
 - Power Gain — 13.5 dB
 - Efficiency — 26%
 - IM3 — -37 dBc
 - ACPR — -39 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2140 MHz, 92 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

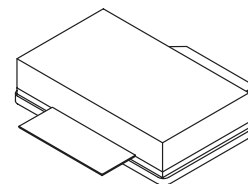
MRF5S21130
MRF5S21130R3
MRF5S21130S
MRF5S21130SR3

**2170 MHz, 28 W AVG.,
2 x W-CDMA, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs**

CASE 465B-03, STYLE 1
NI-880
MRF5S21130



CASE 465C-02, STYLE 1
NI-880S
MRF5S21130S



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	315 2	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$
CW Operation	CW	92	Watts

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C , 92 W CW Case Temperature 80°C , 28 W CW	$R_{\theta JC}$	0.54 0.56	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M4 (Minimum)
Charge Device Model	C7 (Minimum)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2.5	2.7	3.5	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 1200 mAdc)	V _{GS(Q)}	—	3.7	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 3 Adc)	V _{DS(on)}	—	0.26	0.3	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 Adc)	g _{fs}	—	7.5	—	S

DYNAMIC CHARACTERISTICS (1)

Reverse Transfer Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	2.6	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 28 W Avg., I _{DQ} = 1200 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	G _{ps}	12	13.5	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 28 W Avg., I _{DQ} = 1200 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	η	24	26	—	%
Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 28 W Avg., I _{DQ} = 1200 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured over 3.84 MHz BW at f ₁ –10 MHz and f ₂ +10 MHz referenced to carrier channel power.)	IM3		–37	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 28 W Avg., I _{DQ} = 1200 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured over 3.84 MHz at f ₁ –5 MHz and f ₂ +5 MHz.)	ACPR	—	–39	–37	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 28 W Avg., I _{DQ} = 1200 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	IRL	—	–12	–9	dB

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.

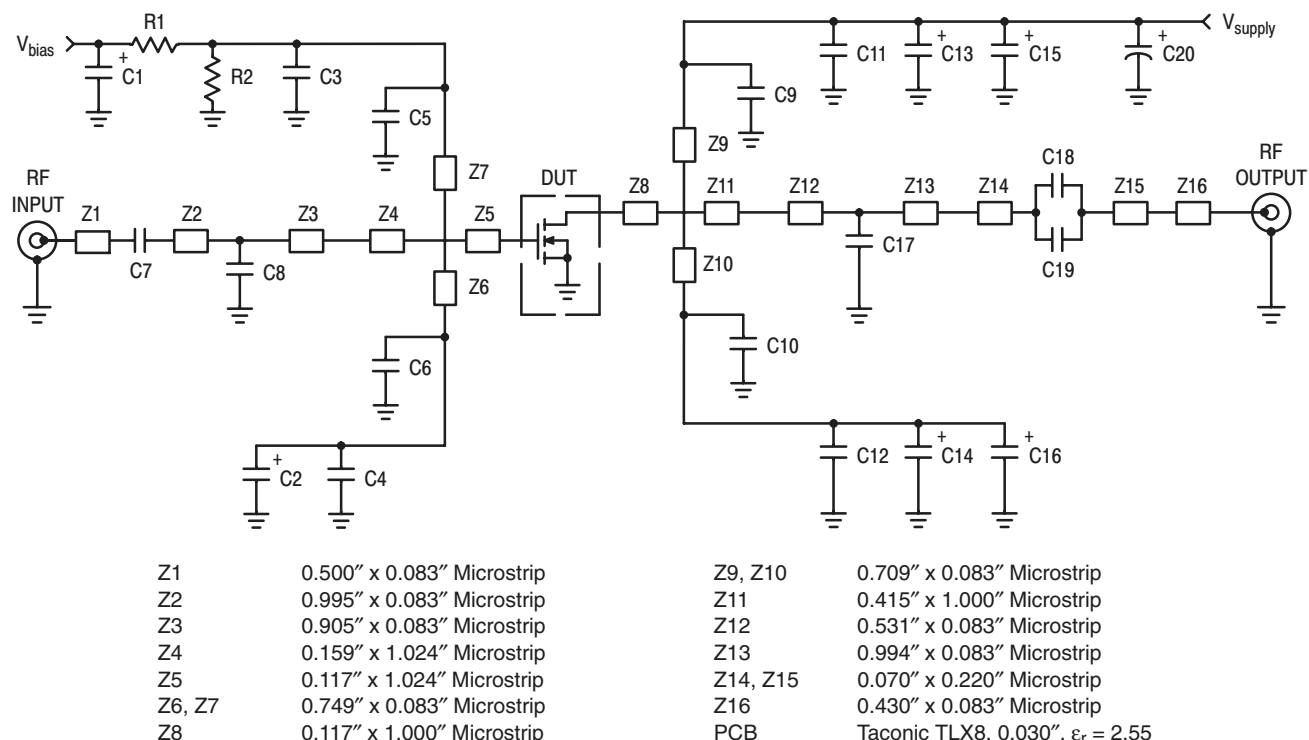


Figure 1. MRF5S21130 Test Circuit Schematic

Table 1. MRF5S21130 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1, C2, C13, C14, C15, C16	10 μ F, 35 V Tantalum Capacitors	293D1106X9035D	Vishay–Sprague
C3, C4, C11, C12	220 nF Chip Capacitors (1812)	1812Y224KXA	Vishay–Vitammon
C5, C6, C7, C9, C10, C18, C19	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C8	0.1 pF 100B Chip Capacitor	100B0R1BW	ATC
C17	0.5 pF 100B Chip Capacitor	100B0R5BW	ATC
C20	220 μ F, 63 V Electrolytic Capacitor, Radial	13668221	Philips
R1, R2	1 k Ω , 1/4 W Chip Resistors		

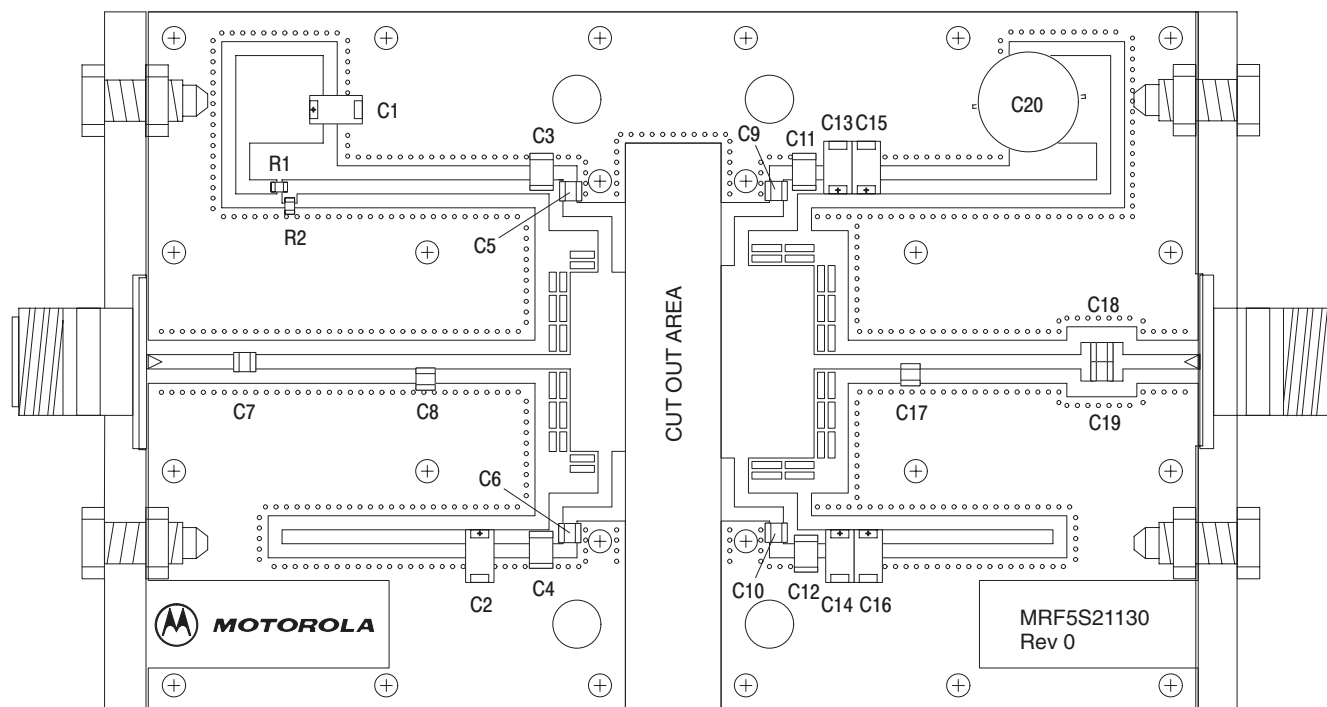


Figure 2. MRF5S21130 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

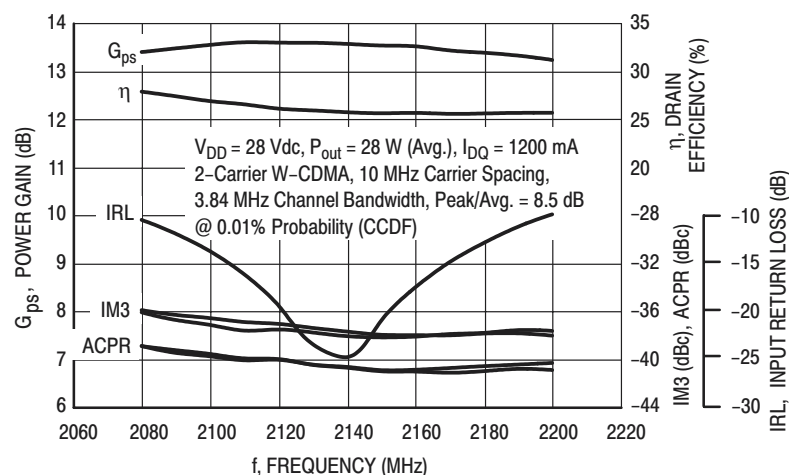


Figure 3. 2-Carrier W-CDMA Broadband Performance

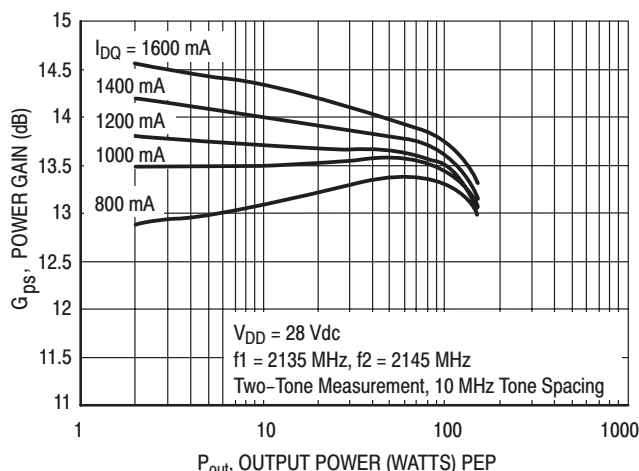


Figure 4. Two-Tone Power Gain versus Output Power

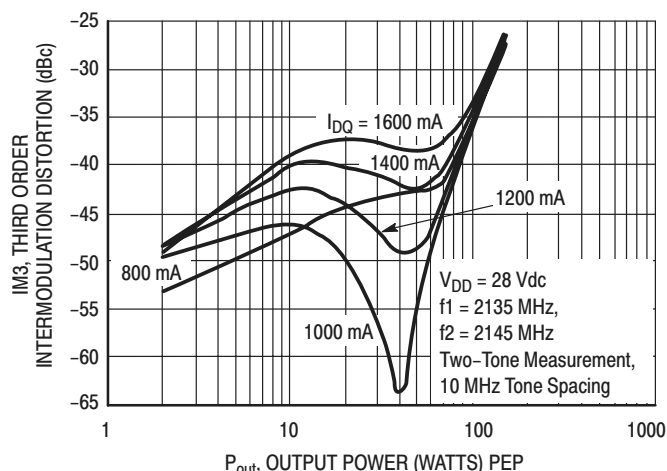


Figure 5. Third Order Intermodulation Distortion versus Output Power

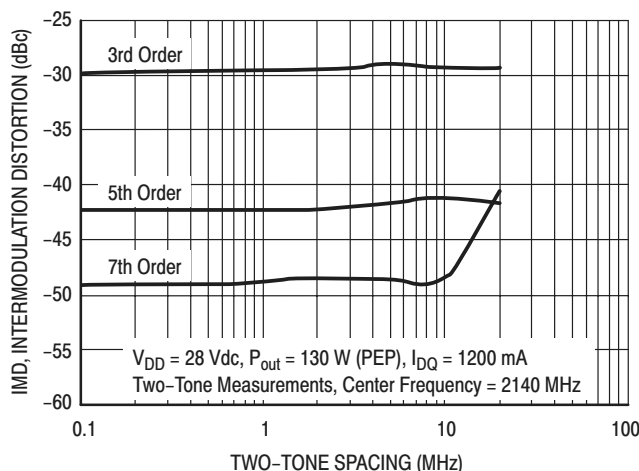


Figure 6. Intermodulation Distortion Products versus Tone Spacing

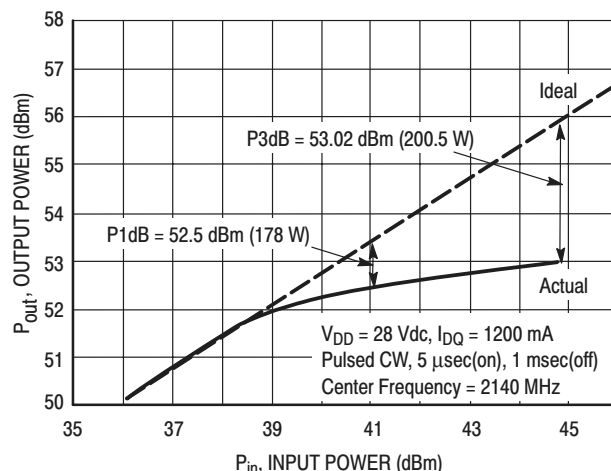


Figure 7. Pulse CW Output Power versus Input Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

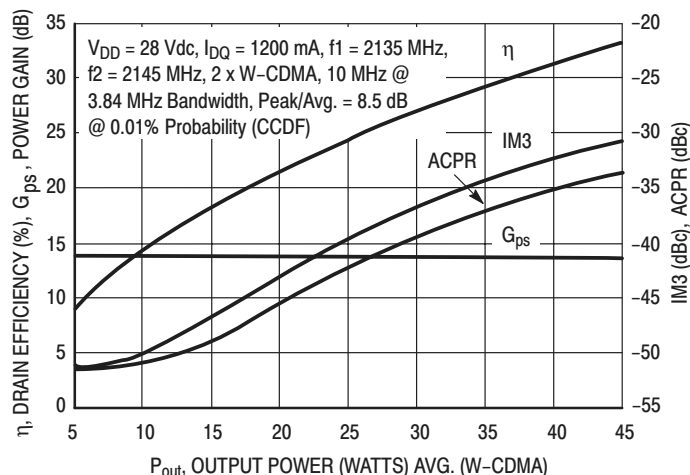


Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

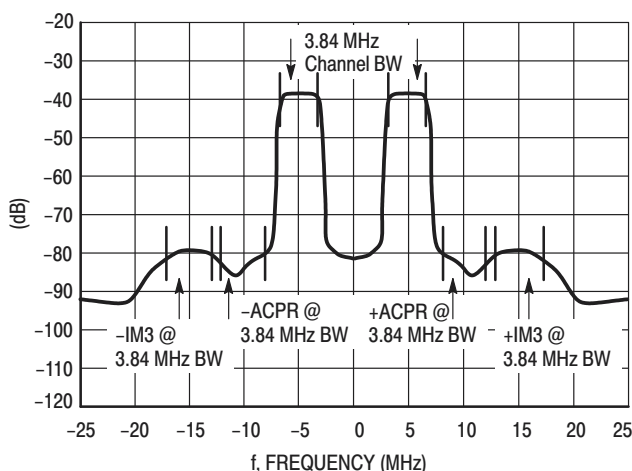


Figure 9. 2-Carrier W-CDMA Spectrum

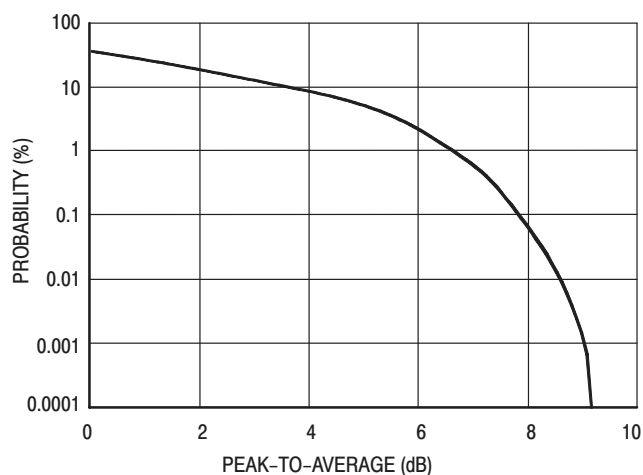
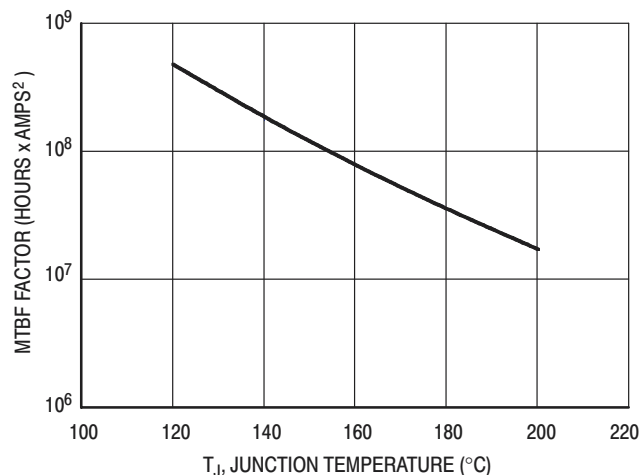
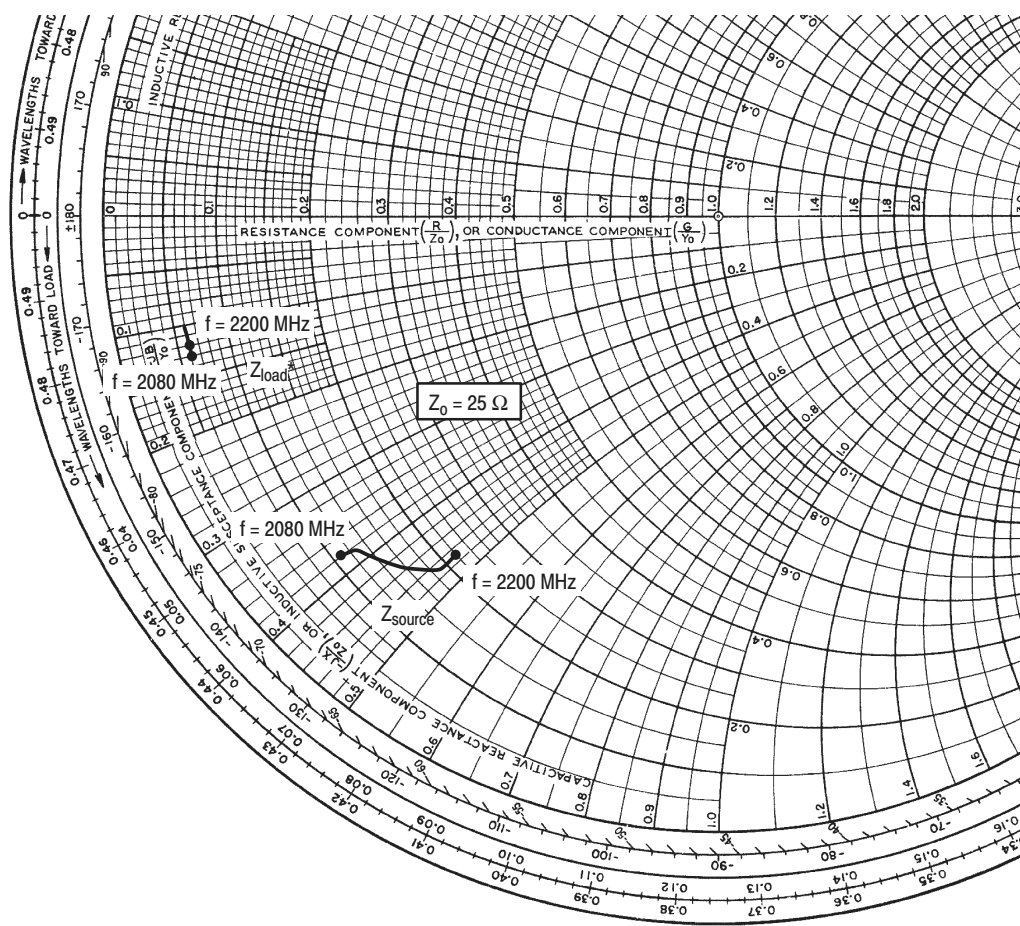


Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single Carrier Test Signal



This above graph displays calculated MTBF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 11. MTBF Factor versus Junction Temperature



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1200 \text{ mA}$, $P_{out} = 28 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
2080	$2.87 - j9.49$	$1.51 - j2.97$
2110	$3.13 - j9.86$	$1.52 - j2.54$
2140	$4.05 - j10.90$	$1.59 - j2.68$
2170	$4.80 - j11.75$	$1.62 - j2.70$
2200	$5.55 - j11.87$	$1.54 - j3.13$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

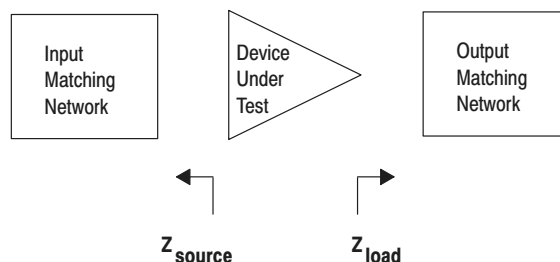


Figure 12. Series Equivalent Input and Output Impedance

The RF MOSFET Line

RF Power Field Effect Transistors

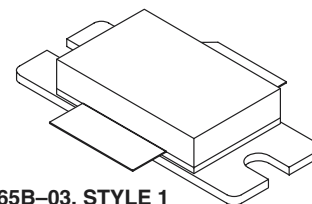
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

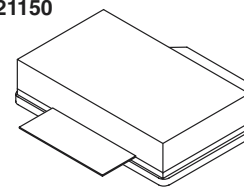
- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 1300$ mA, $f_1 = 2135$ MHz, $f_2 = 2145$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ $f_1 - 5$ MHz and $f_2 + 5$ MHz, Distortion Products Measured over a 3.84 MHz BW @ $f_1 - 10$ MHz and $f_2 + 10$ MHz, Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
 Output Power — 33 Watts Avg.
 Power Gain — 12.5 dB
 Efficiency — 25%
 IM3 — -37 dBc
 ACPR — -39 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2140 MHz, 125 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF5S21150
MRF5S21150R3
MRF5S21150S
MRF5S21150SR3

**2170 MHz, 33 W AVG.,
 2 x W-CDMA, 28 V
 LATERAL N-CHANNEL
 RF POWER MOSFETs**



**CASE 465B-03, STYLE 1
 NI-880
 MRF5S21150**



**CASE 465C-02, STYLE 1
 NI-880S
 MRF5S21150S**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	367 2.1	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$
CW Operation	CW	125	Watts

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C , 125 W CW Case Temperature 80°C , 33 W CW	$R_{\theta JC}$	0.47 0.53	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C7 (Minimum)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μA _{dc}
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μA _{dc}
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μA _{dc}

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 360 μA _{dc})	V _{GS(th)}	2.5	—	3.5	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 1300 mA _{dc})	V _{GS(Q)}	—	3.7	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 3.6 A _{dc})	V _{DS(on)}	—	0.26	0.3	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3.6 A _{dc})	g _{fs}	—	9	—	S

DYNAMIC CHARACTERISTICS (1)

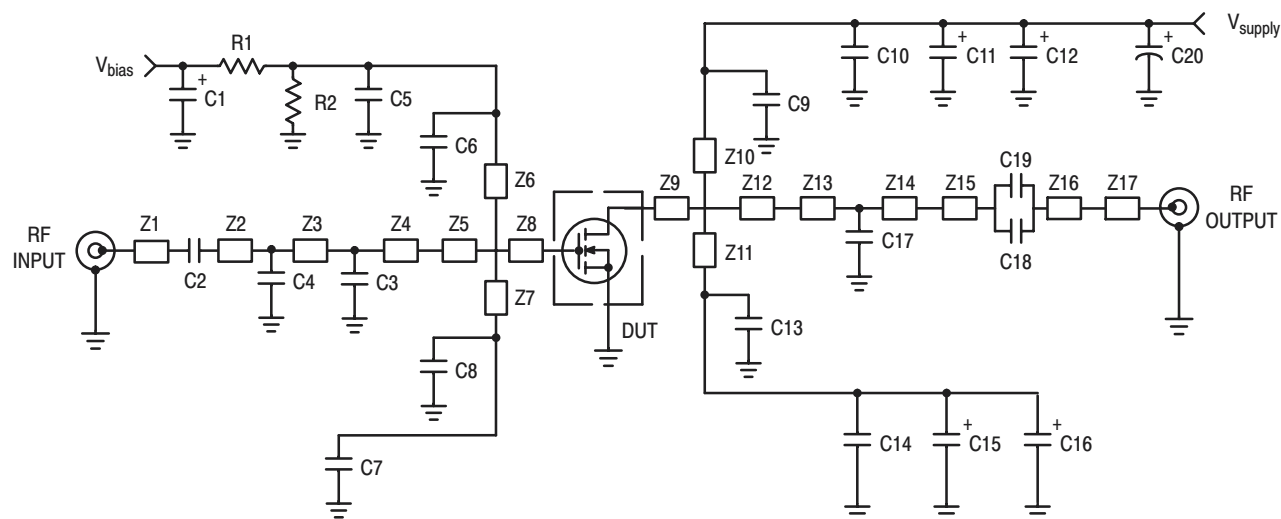
Reverse Transfer Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms) _{ac} @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	3.2	—	pF
--	------------------	---	-----	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	G _{ps}	11	12.5	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	η	23	25	—	%
Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured over 3.84 MHz BW at f ₁ –10 MHz and f ₂ +10 MHz referenced to carrier channel power.)	IM3		–37	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured over 3.84 MHz at f ₁ –5 MHz and f ₂ +5 MHz.)	ACPR	—	–39	–37	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	IRL	—	–12	–9	dB

(1) Part is internally matched both on input and output.

Freescale Semiconductor, Inc.



Z1	0.500" x 0.083" Microstrip	Z10, Z11	0.709" x 0.083" Microstrip
Z2	0.505" x 0.083" Microstrip	Z12	0.415" x 1.100" Microstrip
Z3	0.536" x 0.083" Microstrip	Z13	0.874" x 0.083" Microstrip
Z4	0.776" x 0.083" Microstrip	Z14	1.182" x 0.083" Microstrip
Z5	0.119" x 1.024" Microstrip	Z15, Z16	0.070" x 0.220" Microstrip
Z6, Z7	0.749" x 0.083" Microstrip	Z17	0.430" x 0.083" Microstrip
Z8	0.117" x 1.024" Microstrip	PCB	Taconic TLX8, 0.030", $\epsilon_r = 2.55$
Z9	0.117" x 1.100" Microstrip		

Figure 1. MRF5S21150 Test Circuit Schematic

Table 1. MRF5S21150 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1	22 μ F, 35 V Tantalum Capacitor	TAJE226M035R	AVX
C2, C6, C8, C9, C13, C18, C19	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C3, C4	1.8 pF 100B Chip Capacitors	100B1R8BW	ATC
C5, C7, C10, C14	220 nF Chip Capacitors (1812)	1812Y224KXA	Vishay-Vitramon
C11, C12, C15, C16	10 μ F, 35 V Tantalum Capacitors	293D1106X9035D	Vishay-Sprague
C17	0.3 pF Chip Capacitor	100B0R3BW	ATC
C20	470 μ F, 63 V Electrolytic Capacitor, Radial	13661471	Philips
R1, R2	10 k Ω , 1/4 W Chip Resistors		

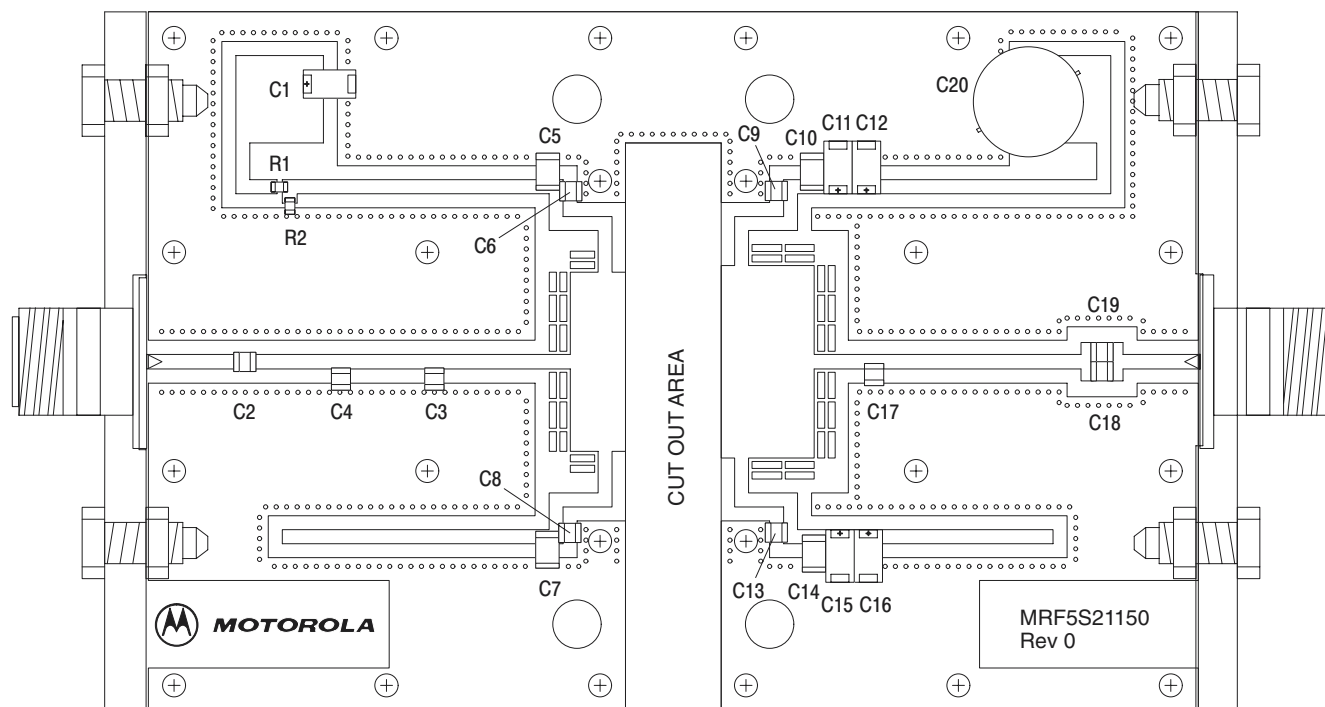


Figure 2. MRF5S21150 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

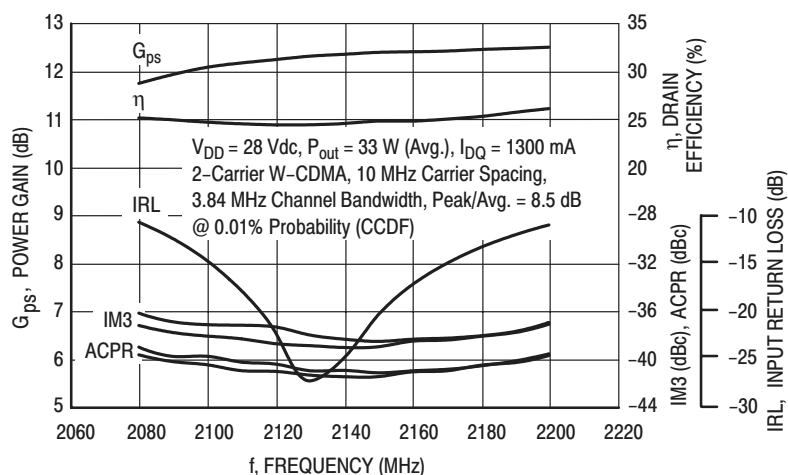


Figure 3. 2-Carrier W-CDMA Broadband Performance

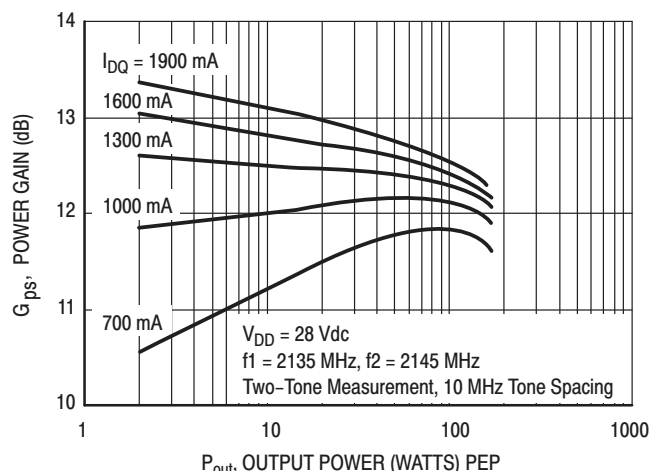


Figure 4. Two-Tone Power Gain versus Output Power

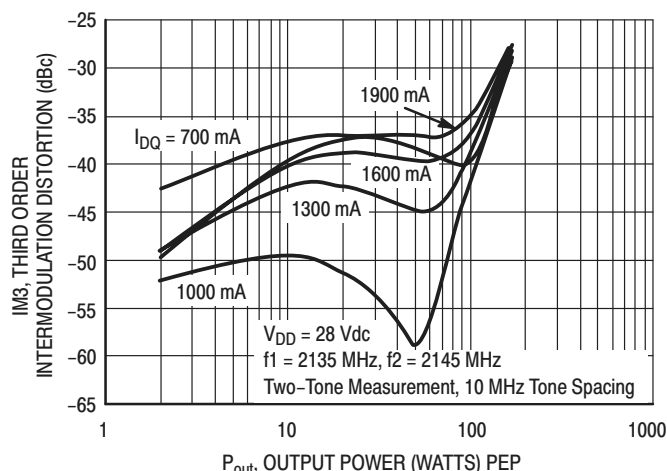


Figure 5. Third Order Intermodulation Distortion versus Output Power

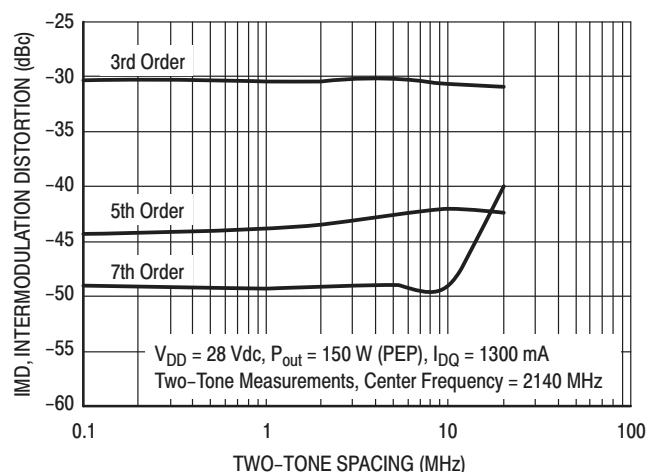


Figure 6. Intermodulation Distortion Products versus Tone Spacing

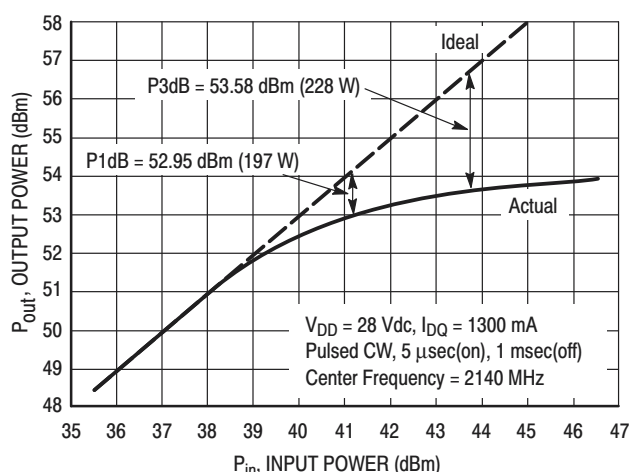


Figure 7. Pulse CW Output Power versus Input Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

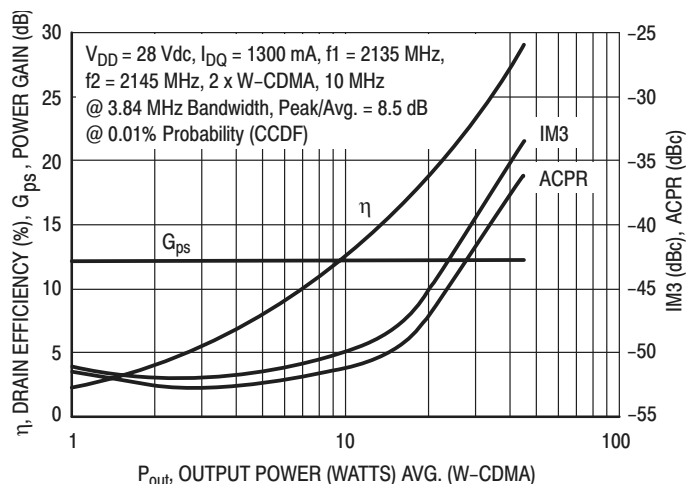


Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

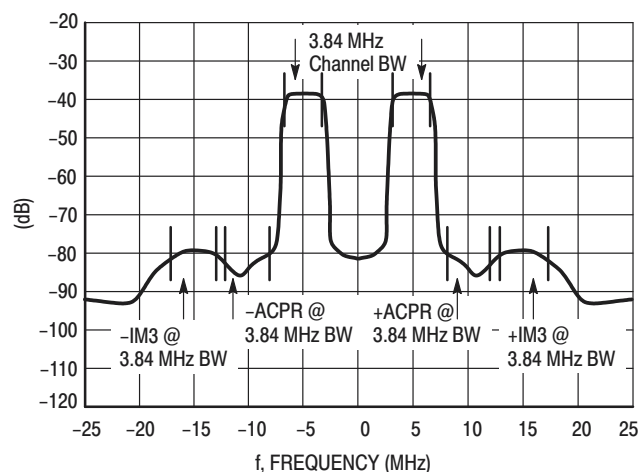


Figure 9. 2-Carrier W-CDMA Spectrum

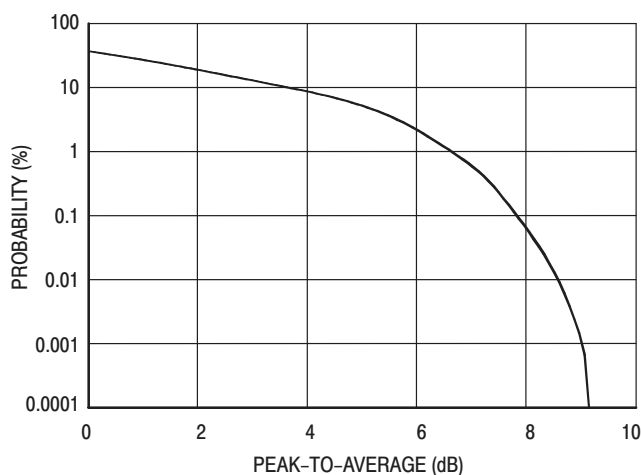
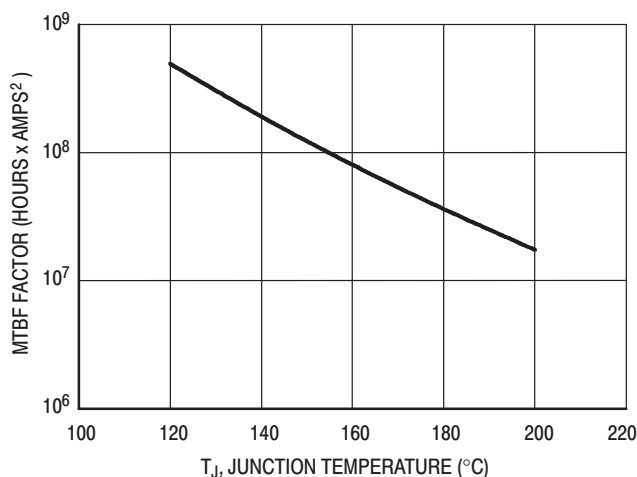
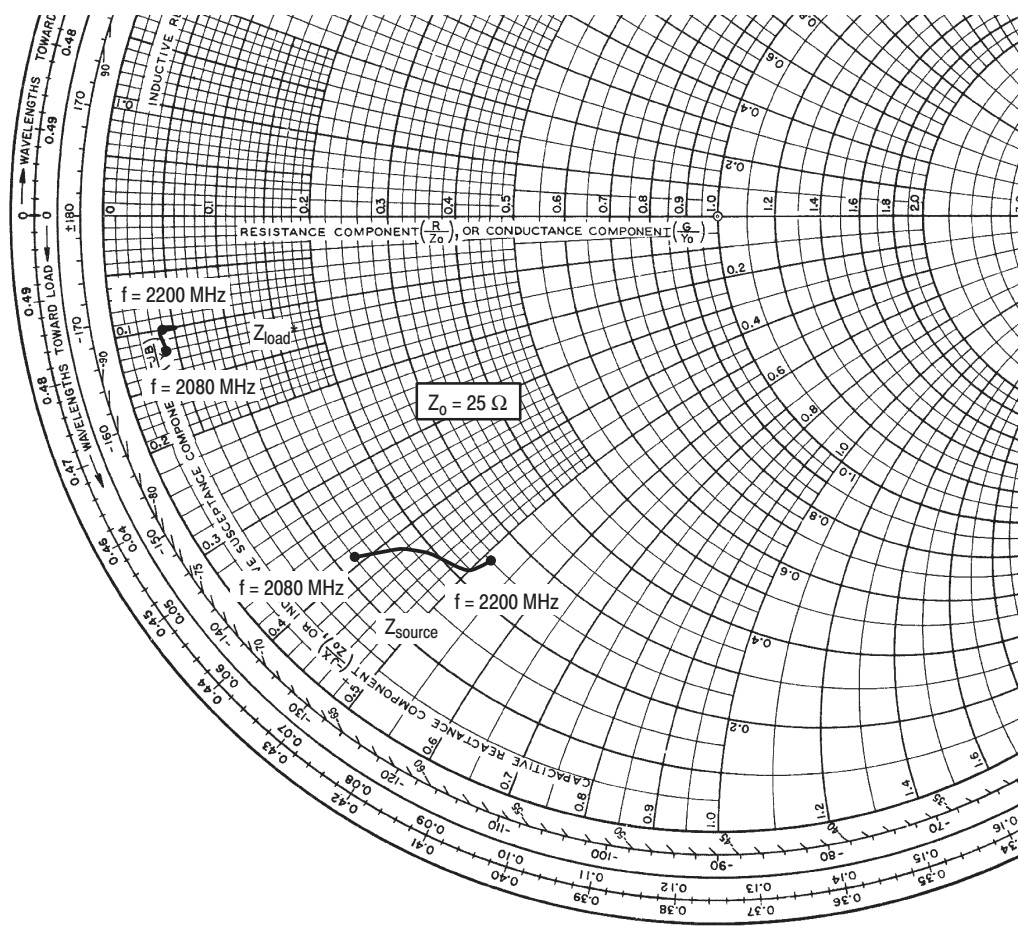


Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single Carrier Test Signal



This above graph displays calculated MTBF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 11. MTBF Factor versus Junction Temperature



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1300 \text{ mA}$, $P_{out} = 33 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
2080	$3.05 - j9.66$	$1.02 - j2.94$
2110	$3.97 - j10.31$	$1.09 - j2.51$
2140	$4.70 - j11.03$	$1.16 - j2.46$
2170	$5.45 - j12.41$	$1.16 - j2.58$
2200	$6.18 - j13.04$	$1.02 - j2.55$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

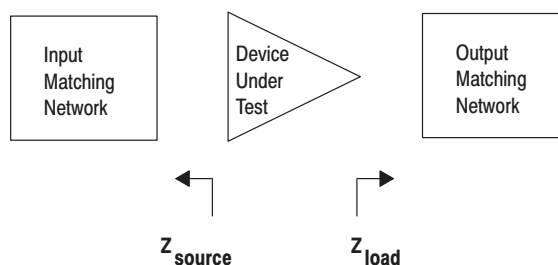


Figure 12. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistor

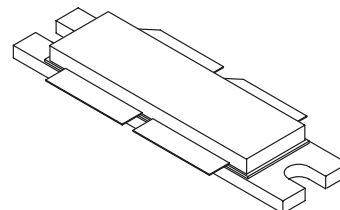
N-Channel Enhancement-Mode Lateral MOSFET

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 2 \times 800$ mA, $f_1 = 2135$ MHz, $f_2 = 2145$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ $f_1 - 5$ MHz and $f_2 + 5$ MHz. Distortion Products Measured over a 3.84 MHz BW @ $f_1 - 10$ MHz and $f_2 + 10$ MHz, Each Carrier Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
Output Power — 38 Watts Avg.
Power Gain — 14 dB
Efficiency — 25.5%
IM3 — 37.5 dBc
ACPR — -41 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2140 MHz, 180 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Qualified Up to a Maximum of 32 V_{DD} Operation

MRF5P21180

**2170 MHz, 38 W AVG.,
2 x W-CDMA, 28 V
LATERAL N-CHANNEL
RF POWER MOSFET**



**CASE 375D-04, STYLE 1
NI-1230**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	437.5 2.5	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C , 180 W CW Case Temperature 80°C , 38 W CW	$R_{\theta JC}$	0.40 0.40	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C7 (Minimum)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS (1)

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 μAdc)	V _{GS(th)}	2.5	2.8	3.5	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 800 mAdc)	V _{GS(Q)}	—	3.6	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.26	0.3	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	5	—	S

DYNAMIC CHARACTERISTICS (1)

Reverse Transfer Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	1.7	—	pF
--	------------------	---	-----	---	----

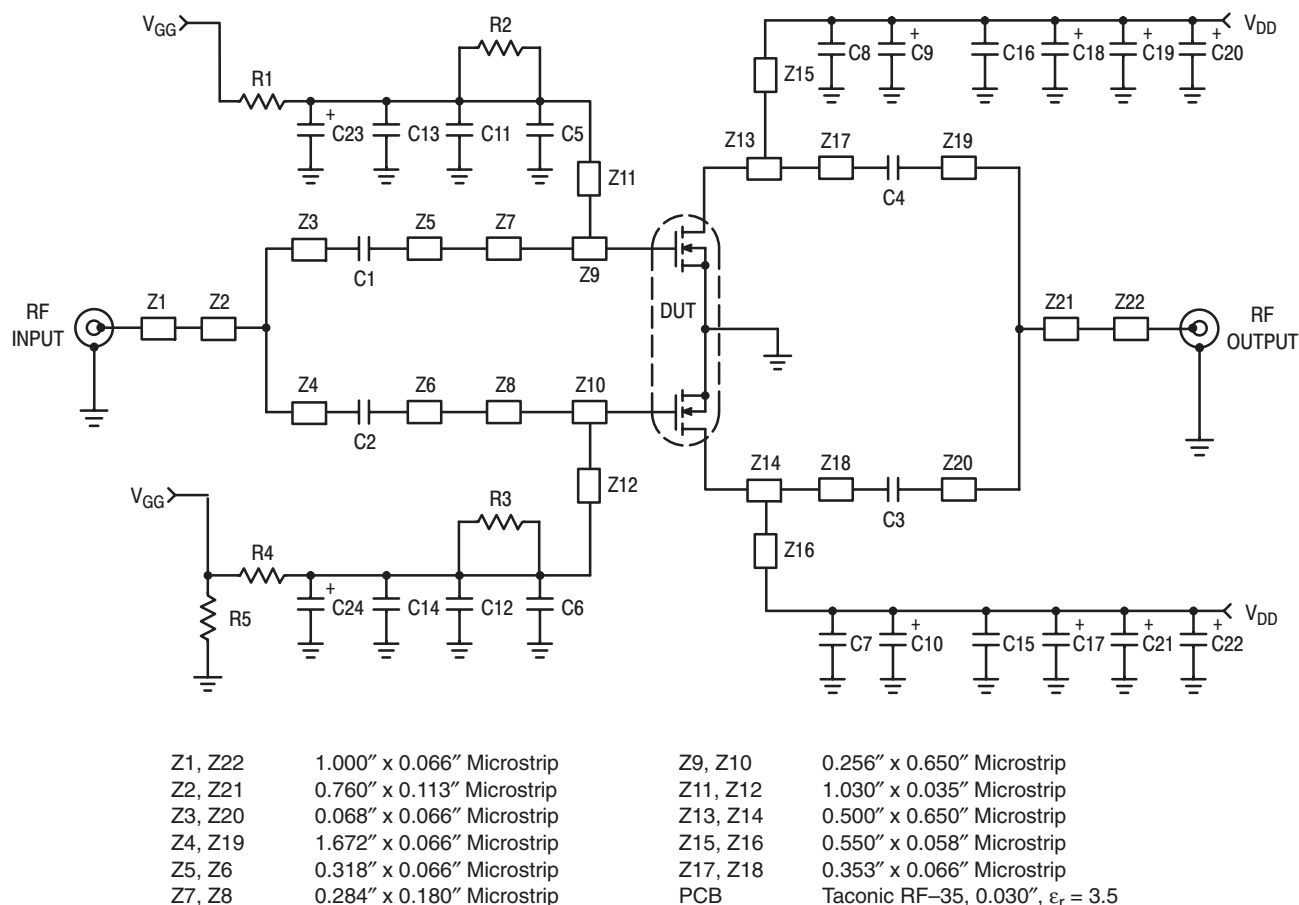
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 800 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	G _{ps}	12.5	14	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 800 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	η	23	25.5	—	%
Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 800 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured over 3.84 MHz BW @ f ₁ –10 MHz and f ₂ +10 MHz referenced to carrier channel power.)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 800 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured over 3.84 MHz BW @ f ₁ –5 MHz and f ₂ +5 MHz.)	ACPR	—	–41	–38	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 800 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	IRL	—	–14	–9	dB

(1) Each side of device measured separately. Part is internally matched both on input and output.

(2) Measurements made with device in push–pull configuration.

Freescale Semiconductor, Inc.



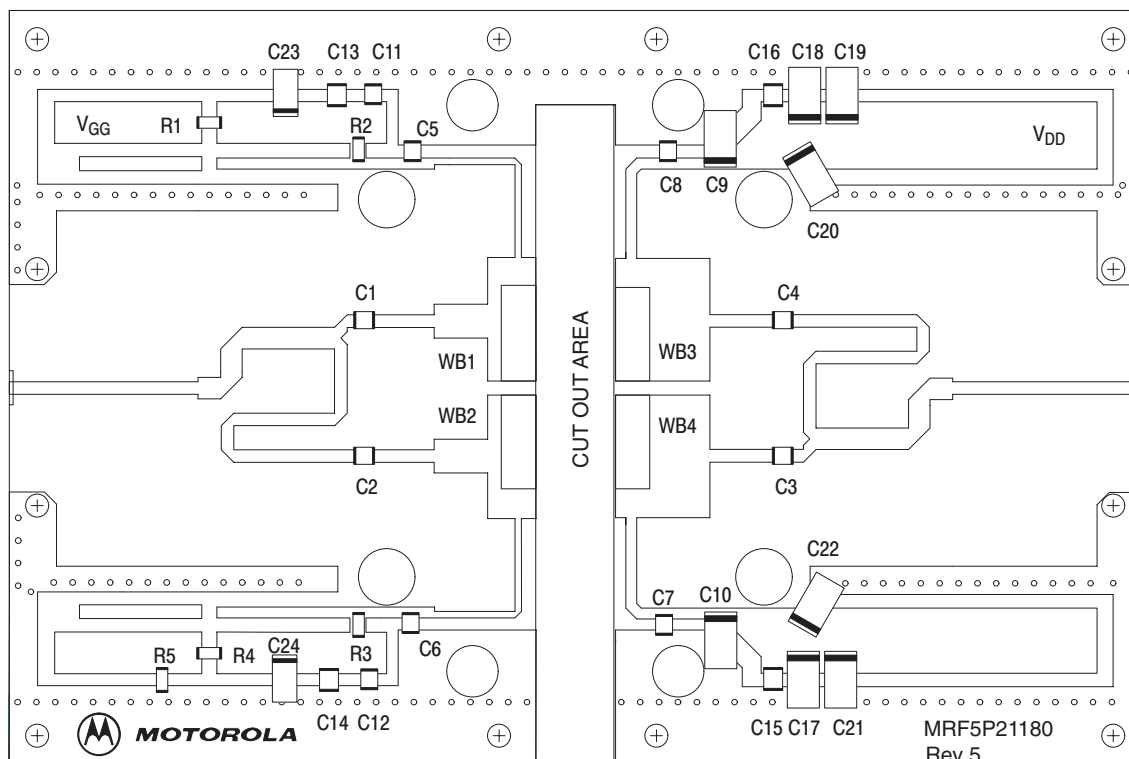


Figure 2. MRF5P21180 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

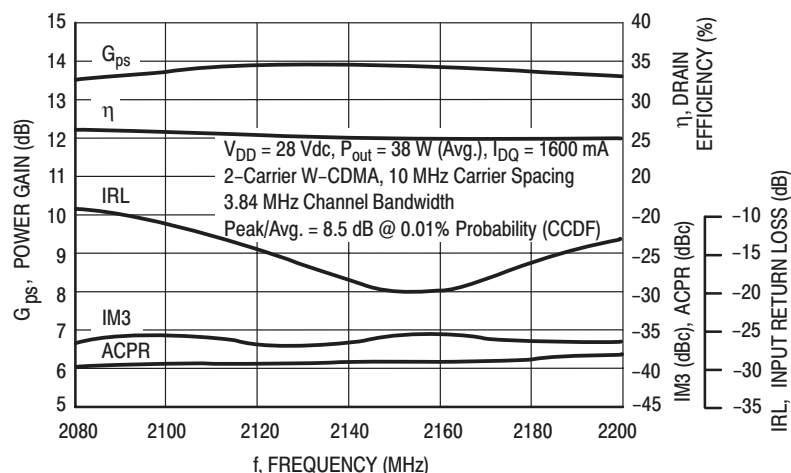


Figure 3. 2-Carrier W-CDMA Broadband Performance

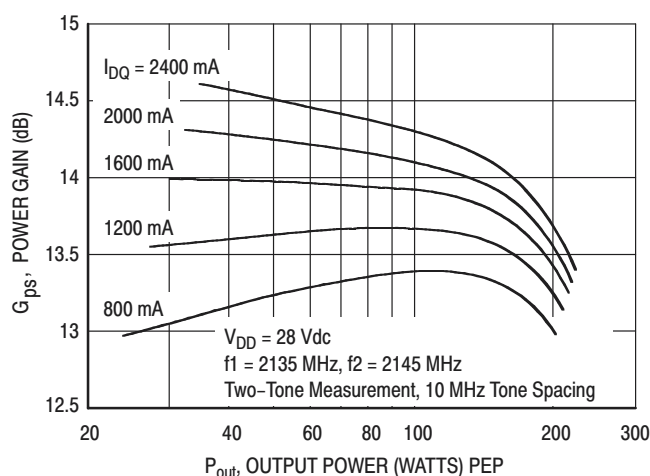


Figure 4. Two-Tone Power Gain versus Output Power

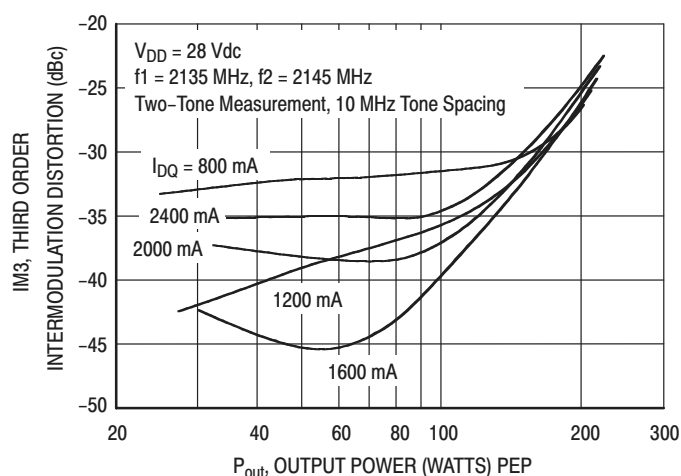


Figure 5. Third Order Intermodulation Distortion versus Output Power

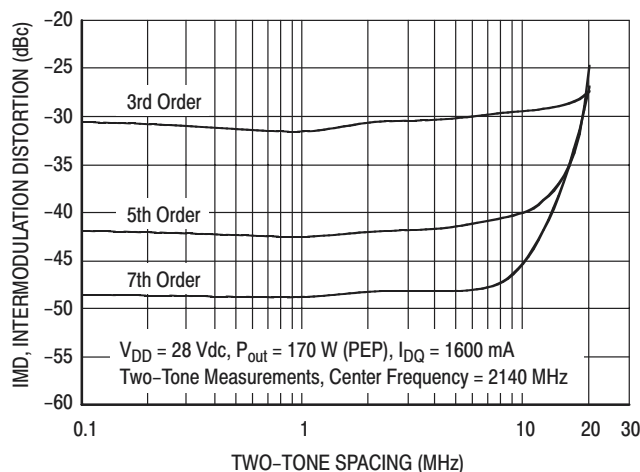


Figure 6. Intermodulation Distortion Products versus Tone Spacing

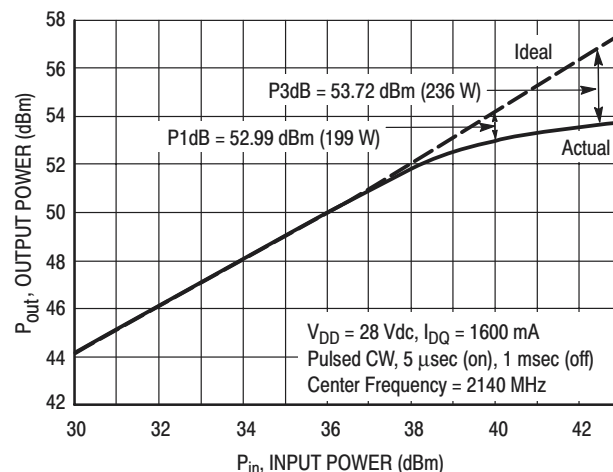


Figure 7. Pulse CW Output Power versus Input Power

Freescale Semiconductor, Inc.

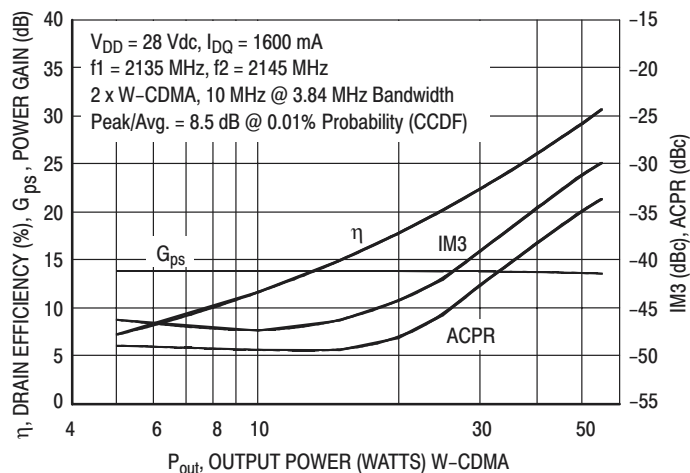


Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

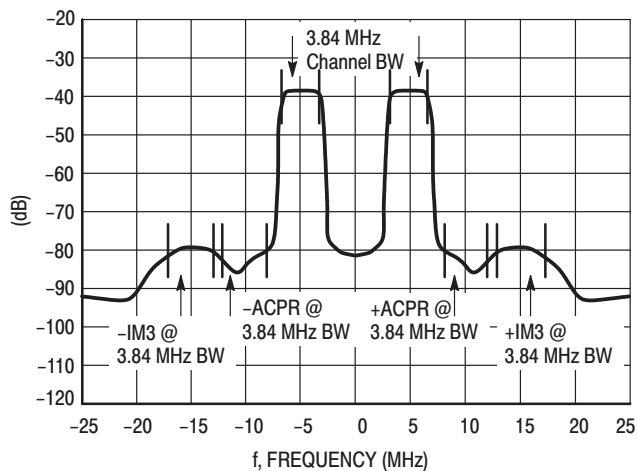


Figure 9. 2-Carrier W-CDMA Spectrum

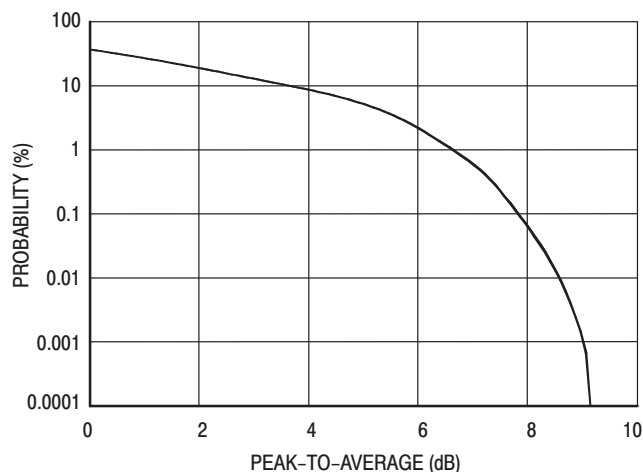
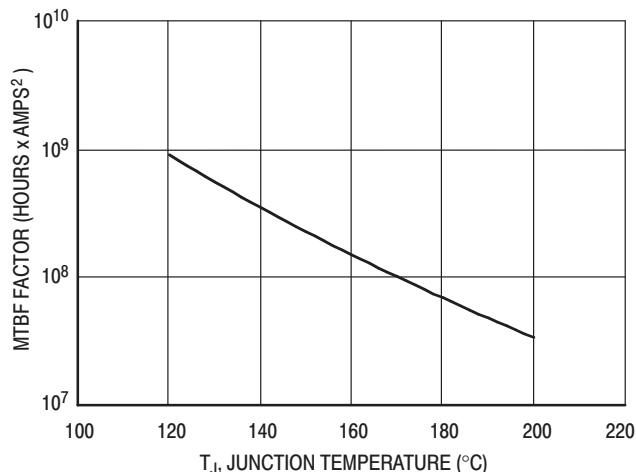
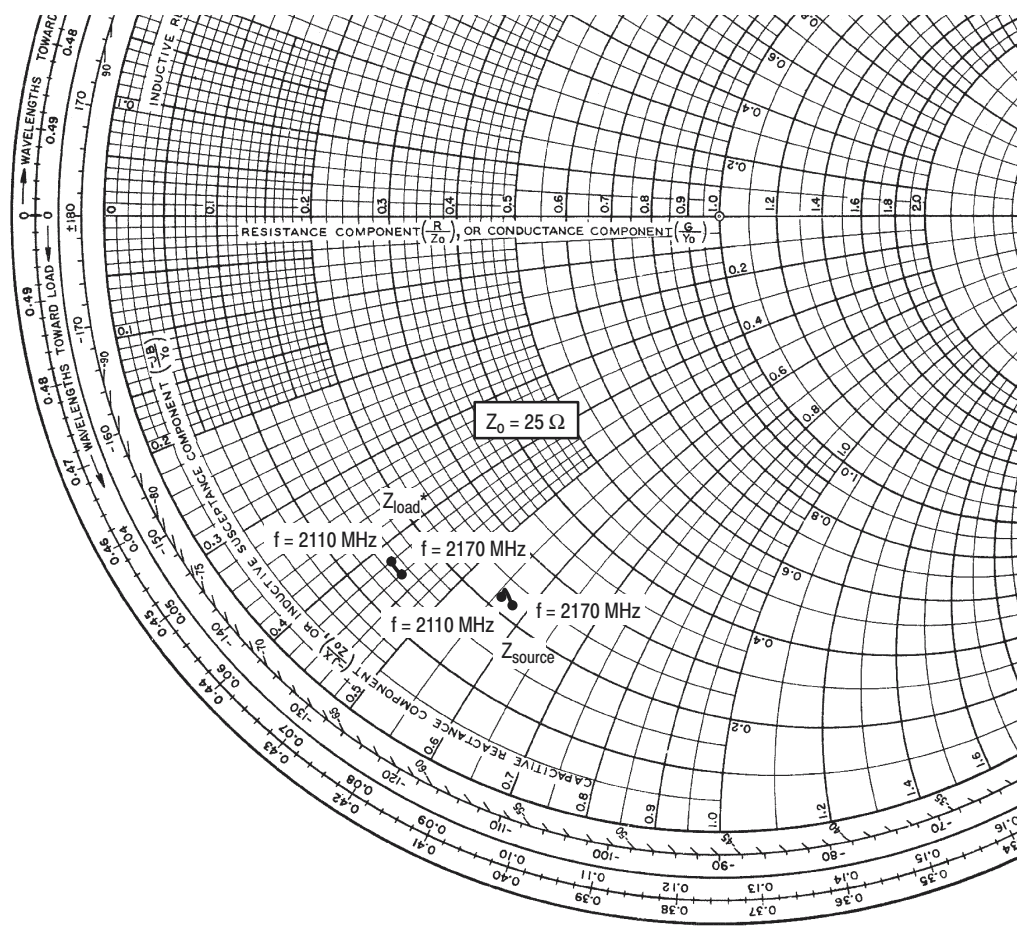


Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single Carrier Test Signal



This above graph displays calculated MTBF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 11. MTBF Factor versus Junction Temperature



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 2 \times 800 \text{ mA}$, $P_{out} = 38 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
2110	$5.39 - j13.89$	$3.69 - j10.51$
2140	$5.66 - j13.99$	$3.81 - j10.66$
2170	$5.53 - j14.51$	$3.79 - j11.05$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

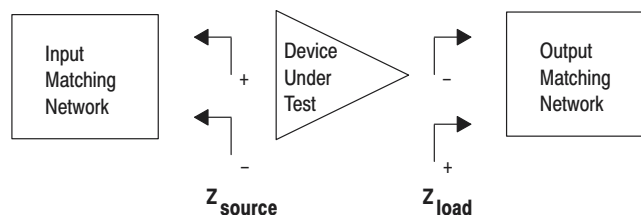


Figure 12. Series Equivalent Input and Output Impedance

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts,
 $I_{DQ} = 2 \times 850$ mA, $f_1 = 2135$ MHz, $f_2 = 2145$ MHz,
Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over
3.84 MHz BW @ $f_1 - 5$ MHz and $f_2 + 5$ MHz. Distortion Products
Measured over a 3.84 MHz BW @ $f_1 - 10$ MHz and $f_2 + 10$ MHz,
Each Carrier Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.
Output Power — 38 Watts (Avg.)
Power Gain — 12.1 dB
Efficiency — 22%
IM3 — 37.5 dBc
ACPR — -41 dBc
- Internally Input and Output Matched, for Ease of Use
- High Gain, High Efficiency, and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2110 MHz, 170 Watts (CW)
Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

MRF21180

MRF21180S

2170 MHz, 170 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs

CASE 375D-04, STYLE 1
NI-1230
MRF21180

CASE 375E-03, STYLE 1
NI-1230S
MRF21180S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	380 2.17	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.46	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 200 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 850 mAdc)	V _{GS(Q)}	3	3.9	5	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.18	0.22	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	6	—	S
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	3.6	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)					
2–Carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers. Each carrier has Peak/Avg. ratio = 8.3 dB @ 0.01% Probability on CCDF.					
Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	G _{ps}	11	12.1	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	η	19	22	—	%
Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured over 3.84 MHz BW @ f ₁ –10 MHz and f ₂ +10 MHz)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured over 3.84 MHz BW @ f ₁ – 5 MHz and f ₂ +5 MHz.)	ACPR	—	–41	–39	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 38 W Avg., I _{DQ} = 2 x 850 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 170 W CW, I _{DQ} = 2 x 850 mA, f = 2170 MHz VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

- (1) Each side of device measured separately. Part is internally matched both on input and output.
 (2) Measurements made with device in push–pull configuration.

(continued)

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) (continued)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 170\text{ W}$, $I_{DQ} = 2 \times 850\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	G_{ps}	—	12	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 170\text{ W}$, $I_{DQ} = 2 \times 850\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	η	—	33	—	%
Two-Tone Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 170\text{ W}$, $I_{DQ} = 2 \times 850\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	IMD	—	-30	—	dBc
Two-Tone Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 170\text{ W}$, $I_{DQ} = 2 \times 850\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2120\text{ MHz}$ and $f_1 = 2160\text{ MHz}$, $f_2 = 2170\text{ MHz}$)	IRL	—	-12	—	dB
P_{out} , 1 dB Compression Point ($V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 2 \times 850\text{ mA}$, $f = 2170\text{ MHz}$)	P1dB	—	180	—	W

(2) Measurements made with device in push-pull configuration.

Freescale Semiconductor, Inc.

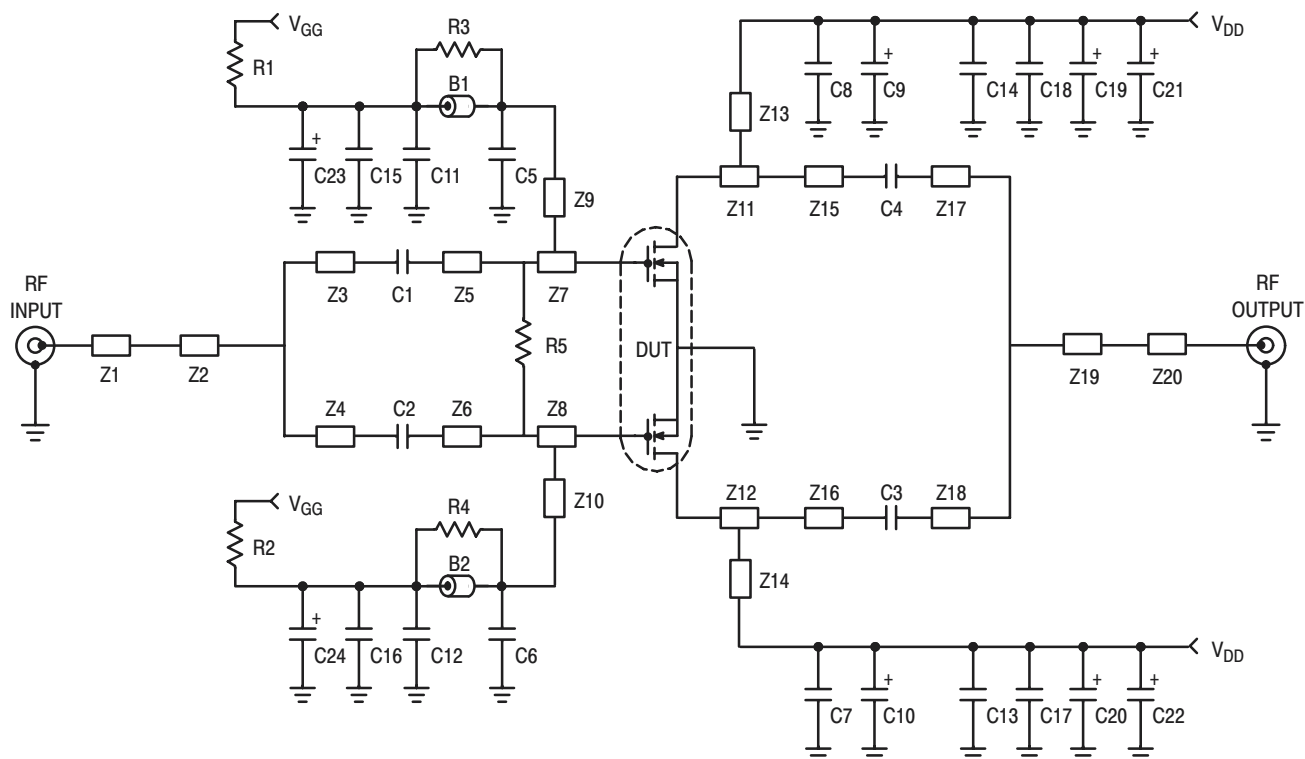


Figure 1. MRF21180 Test Circuit Schematic

Table 1. MRF21180 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1, B2	Short Ferrite Beads	2743019447	Fair Rite
C1, C2, C3, C4	30 pF Chip Capacitors	100B300JCA500X	ATC
C5, C6, C7, C8	5.6 pF Chip Capacitors	100B5R6JCA500X	ATC
C9, C10	10 μ F Tantalum Capacitors	T495X106K035AS4394	Kemet
C11, C12, C13, C14	1000 pF Chip Capacitors	100B102JCA500X	ATC
C15, C16, C17, C18	0.1 μ F Chip Capacitors	CDR33BX104AKWS	Kemet
C19, C20	1.0 μ F Tantalum Capacitors	T491C105M050	Kemet
C21, C22, C23, C24	22 μ F Tantalum Capacitors	T491X226K035AS4394	Kemet
N1, N2	Type N Flange Mounts	3052-1648-10	Omni Spectra
R1, R2, R3, R4	10 Ω , 1/8 W Chip Resistors		
R5	1.0 k Ω , 1/8 W Chip Resistor		
Z1, Z20	Microstrip	0.790" x 0.065"	
Z2, Z19	Microstrip	0.830" x 0.112"	
Z3, Z18	Microstrip	0.145" x 0.065"	
Z4, Z17	Microstrip	1.700" x 0.065"	
Z5, Z6	Microstrip	0.340" x 0.065"	
Z7, Z8	Microstrip	0.455" x 0.600"	
Z9, Z10	Microstrip	0.980" x 0.035"	
Z11, Z12	Microstrip	0.510" x 0.645"	
Z13, Z14	Microstrip	0.770" x 0.058"	
Z15, Z16	Microstrip	0.280" x 0.065"	
WB1, WB2, WB3, WB4	Wear Blocks		
Board	0.030" Glass Teflon®	RF-35, $\epsilon_r = 3.50$	Taconic
PCB	Etched Circuit Boards	MRF21180 Rev. 4	CMR

Freescale Semiconductor, Inc.

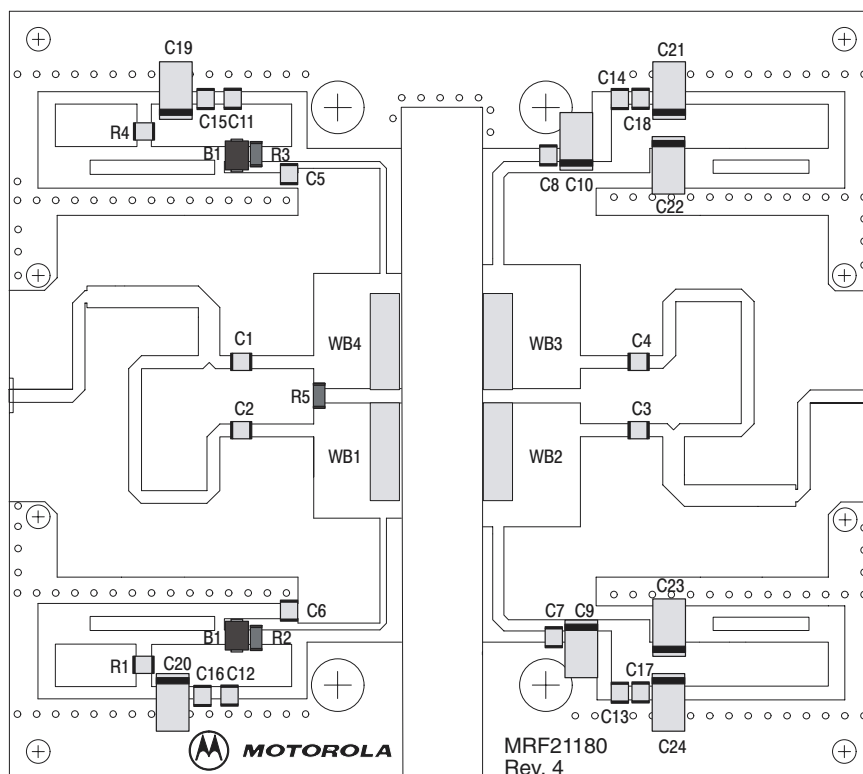


Figure 2. MRF21180 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

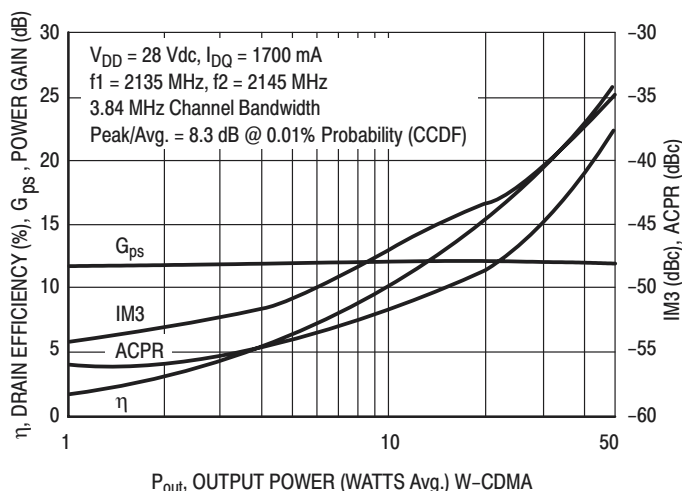


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

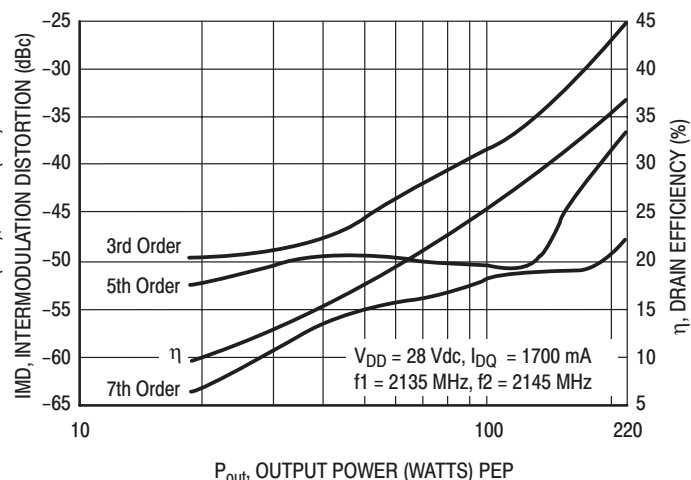


Figure 4. Intermodulation Distortion Products versus Output Power

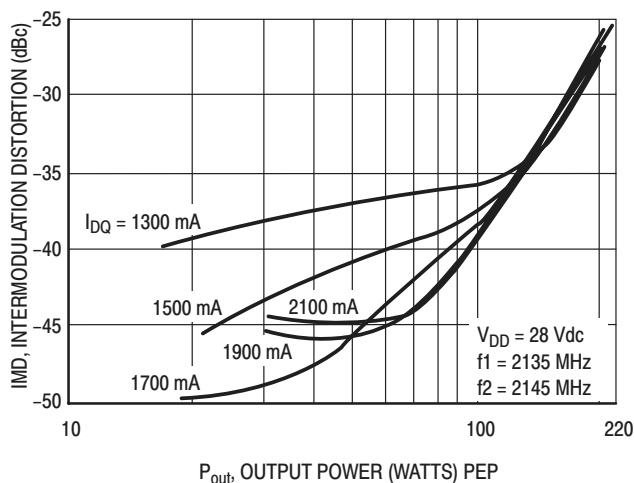


Figure 5. Intermodulation Distortion versus Output Power

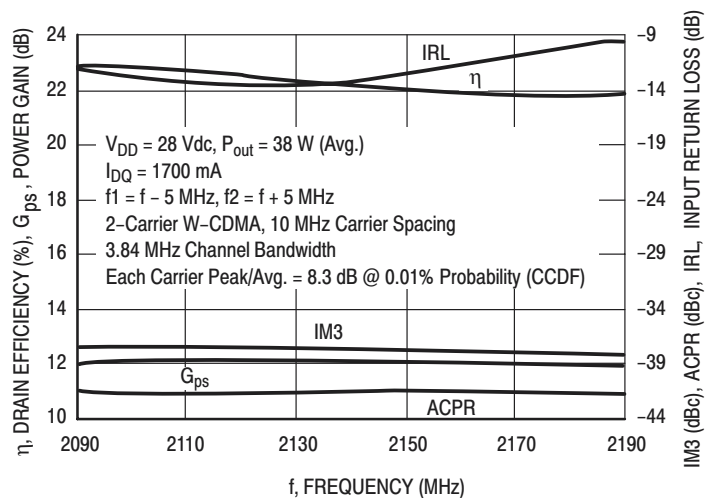


Figure 6. 2-Carrier W-CDMA Broadband Performance

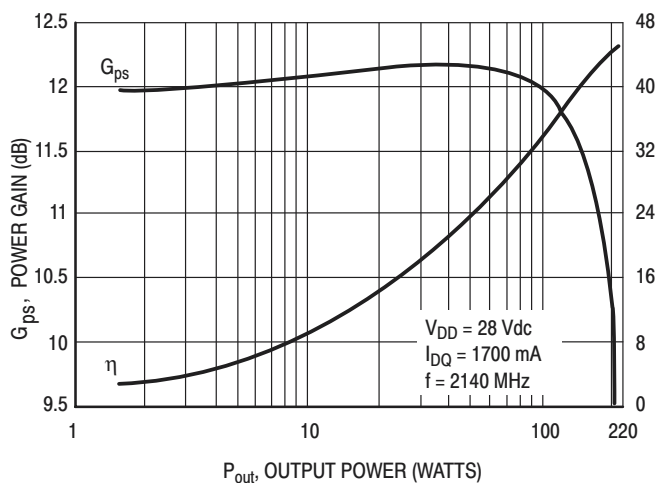


Figure 7. CW Performance

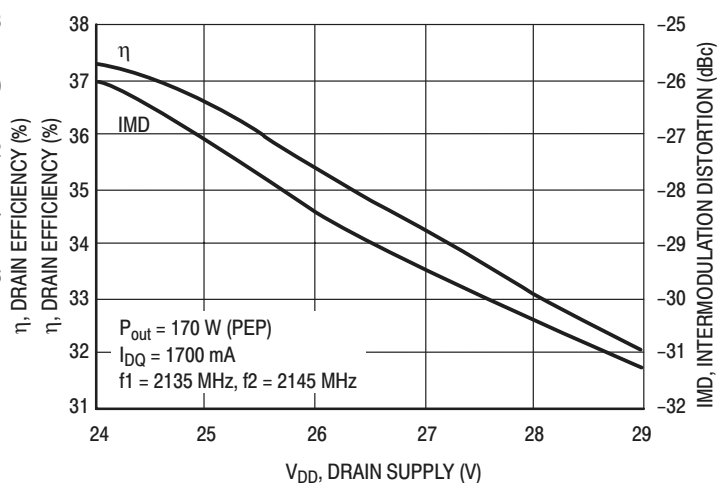


Figure 8. Two-Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

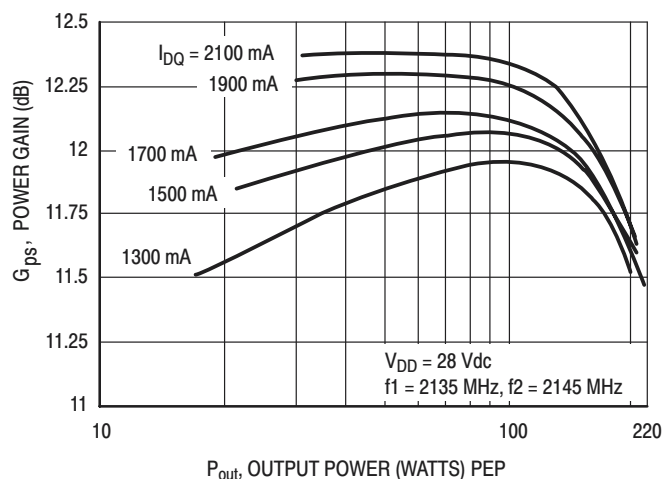


Figure 9. Two-Tone Power Gain versus Output Power

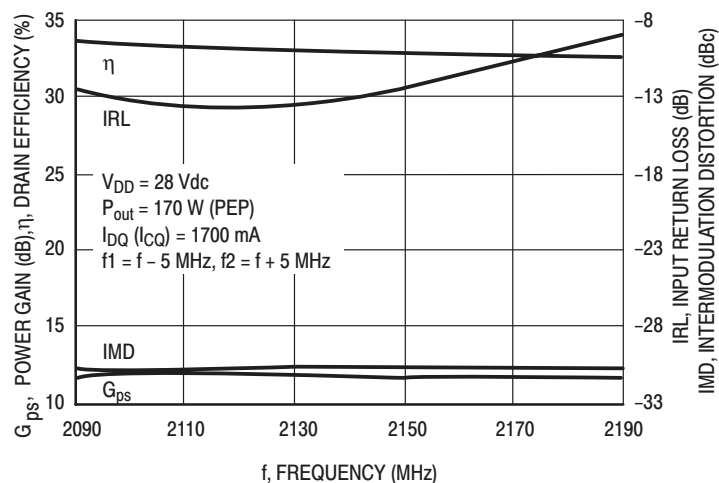


Figure 10. Two-Tone Broadband Performance

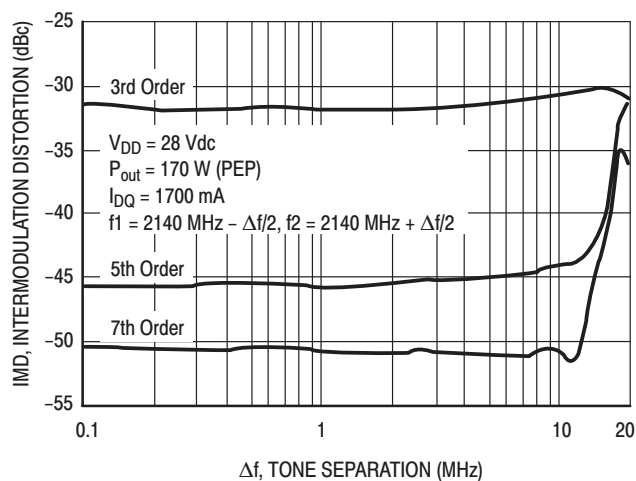


Figure 11. Intermodulation Distortion Products versus Two-Tone Spacing

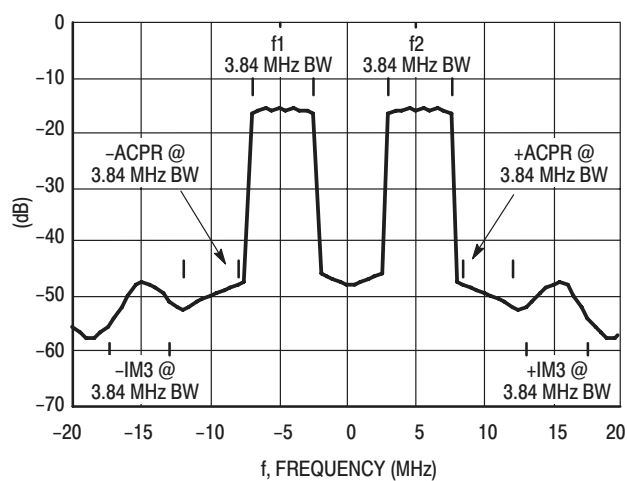
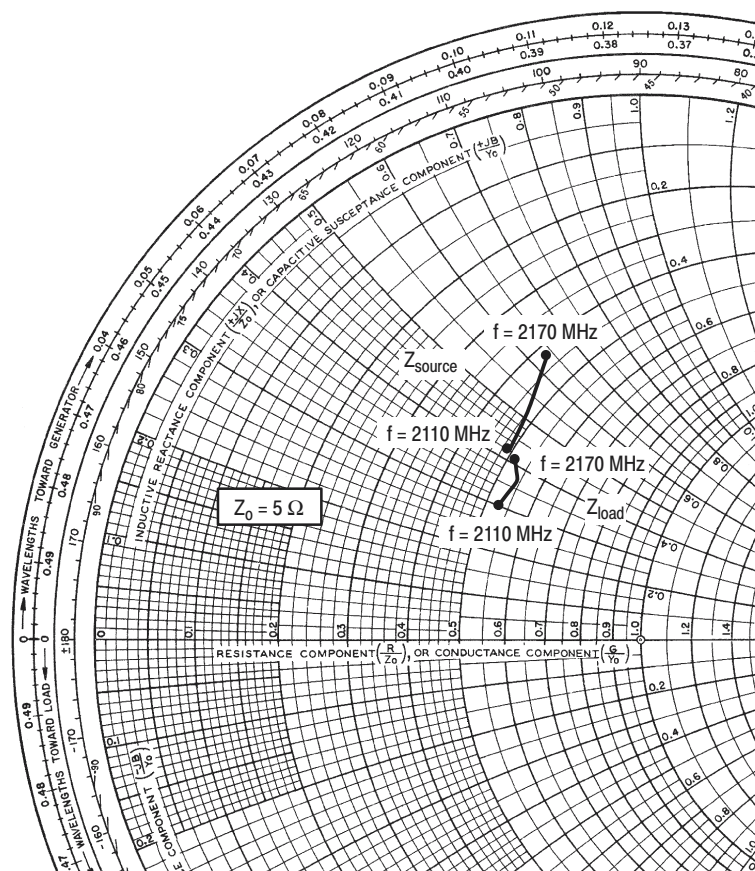


Figure 12. 2-Carrier W-CDMA Spectrum



$V_{DD} = 28$ Vdc, $I_{DQ} = 2 \times 850$ mA, $P_{out} = 38$ W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2110	$2.45 + j2.08$	$2.65 + j1.52$
2140	$2.39 + j2.51$	$2.71 + j1.80$
2170	$2.16 + j3.14$	$2.64 + j2.04$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

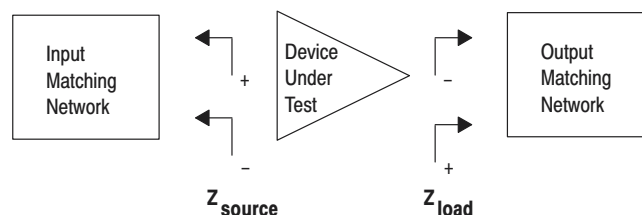


Figure 13. Series Equivalent Input and Output Impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Advance Information

The RF GaAs Line

Gallium Arsenide PHEMT

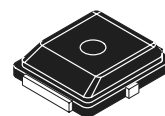
RF Power Field Effect Transistor

Designed for 3.5 GHz WLL/MMDS/BWA or UMTS applications. Characterized from 0.5 to 5.0 GHz. Device is unmatched and is characterized for use in Class AB Customer Premise Equipment (CPE) applications.

- Typical W-CDMA Performance: -42 dBc ACPR, 3.55 GHz, 6 Volts, $I_{DQ} = 180$ mA
 Output Power — 450 mWatts
 Power Gain — 9 dB
 Efficiency — 24%
- 3 Watts P1dB @ 3.55 GHz
- Excellent Phase Linearity and Group Delay Characteristics
- High Gain, High Efficiency and High Linearity
- In Tape and Reel. T1 Suffix = 1000 Units per 12 mm, 7 inch Reel.

MRFG35003M6T1

3.5 GHz, 3 W, 6 V
 POWER FET
 GaAs PHEMT



CASE 466-02, STYLE 1
 PLD-1.5
 PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	8	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	22.7 ⁽²⁾ 0.15 ⁽²⁾	Watts W/ $^\circ\text{C}$
Gate-Source Voltage	V_{GS}	- 5	Vdc
RF Input Power	P_{in}	24	dBm
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Channel Temperature ⁽¹⁾	T_{ch}	175	$^\circ\text{C}$
Operating Case Temperature Range	T_C	- 40 to +85	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.6 ⁽²⁾	$^\circ\text{C/W}$

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	MSL1

(1) For reliable operation, the operating channel temperature should not exceed 150°C .

(2) Simulated.

REV 0

MRFG35003M6T1
 5-444

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Saturated Drain Current (V _{DS} = 3.5 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	2.9	—	Adc
Off State Leakage Current (V _{GS} = -0.4 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	< 1.0	100	μAdc
Off State Drain Current (V _{DS} = 6 Vdc, V _{GS} = -1.9 Vdc)	I _{DSO}	—	0.02	1.0	mAdc
Off State Current (V _{DS} = 20 Vdc, V _{GS} = -2.5 Vdc)	I _{DSX}	—	1.0	15	mAdc
Gate–Source Cut–off Voltage (V _{DS} = 3.5 Vdc, I _{DS} = 15 mA)	V _{GS(th)}	-1.2	-1.0	-0.7	Vdc
Quiescent Gate Voltage (V _{DS} = 6 Vdc, I _{DQ} = 180 mA)	V _{GS(Q)}	-1.1	-0.9	-0.7	Vdc
Power Gain (V _{DD} = 6 Vdc, I _{DQ} = 180 mA, f = 3.55 GHz)	G _{ps}	8	9	—	dB
Output Power, 1 dB Compression Point (V _{DD} = 6 Vdc, I _{DQ} = 180 mA, f = 3.55 GHz)	P1dB	—	3	—	W
Drain Efficiency (V _{DD} = 6 Vdc, I _{DQ} = 180 mA, P _{out} = 450 mW, f = 3.55 GHz. Tune for Maximum P _{out})	η _D	22	24	—	%
Adjacent Channel Power Ratio (V _{DD} = 6 Vdc, P _{out} = 450 mW Avg., I _{DQ} = 180 mA, f = 3.55 GHz, W–CDMA, 8.5 P/A @ 0.01% Probability, 64 CH, 3.84 MCPS)	ACPR	—	-42	-38	dBc

Freescale Semiconductor, Inc.

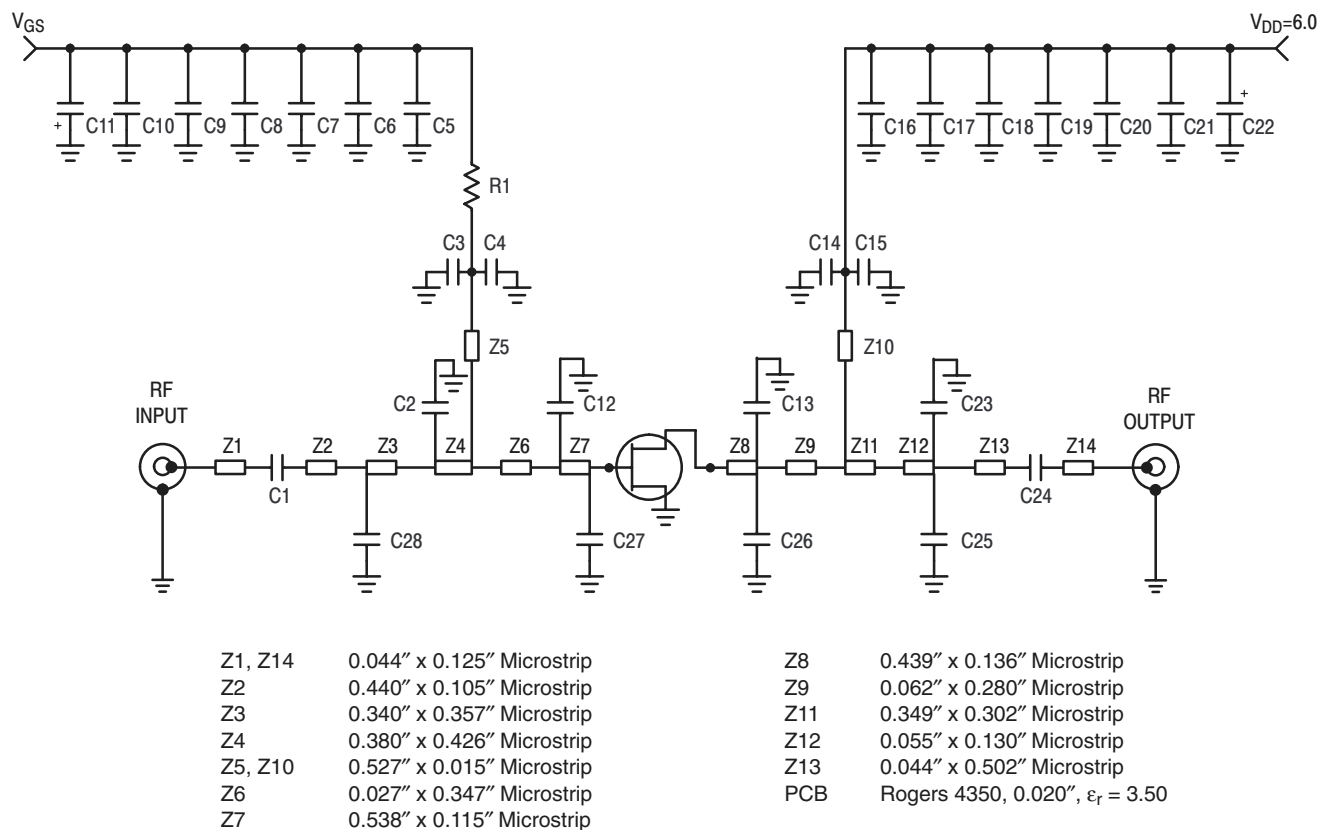


Figure 1. 3.5 GHz Test Circuit Schematic

Table 1. 3.5 GHz Test Circuit Component Designations and Values

Designation	Description
C1	12 pF Chip Capacitor, B Case, ATC
C2	0.1 pF Chip Capacitor (0805), AVX
C3, C4, C14, C15	3.9 pF Chip Capacitors (0805), AVX
C5, C16	10 pF Chip Capacitors, A Case, ATC
C6, C17	100 pF Chip Capacitors, A Case, ATC
C7, C18	100 pF Chip Capacitors, B Case, ATC
C8, C19	1000 pF Chip Capacitors, B Case, ATC
C9, C20	3.9 μ F Chip Capacitors, B Case, ATC
C10, C21	0.1 μ F Chip Capacitors, B Case, ATC
C11, C22	22 μ F, 35 V Tantalum Surface Mount Capacitor, Newark
C12, C13, C26, C27	0.3 pF Chip Capacitors (0805), AVX
C23, C25, C28	1.0 pF Chip Capacitors (0805), AVX
C24	7.5 pF Chip Capacitor, B Case, ATC
R1	50 Ω Chip Resistor, Newark

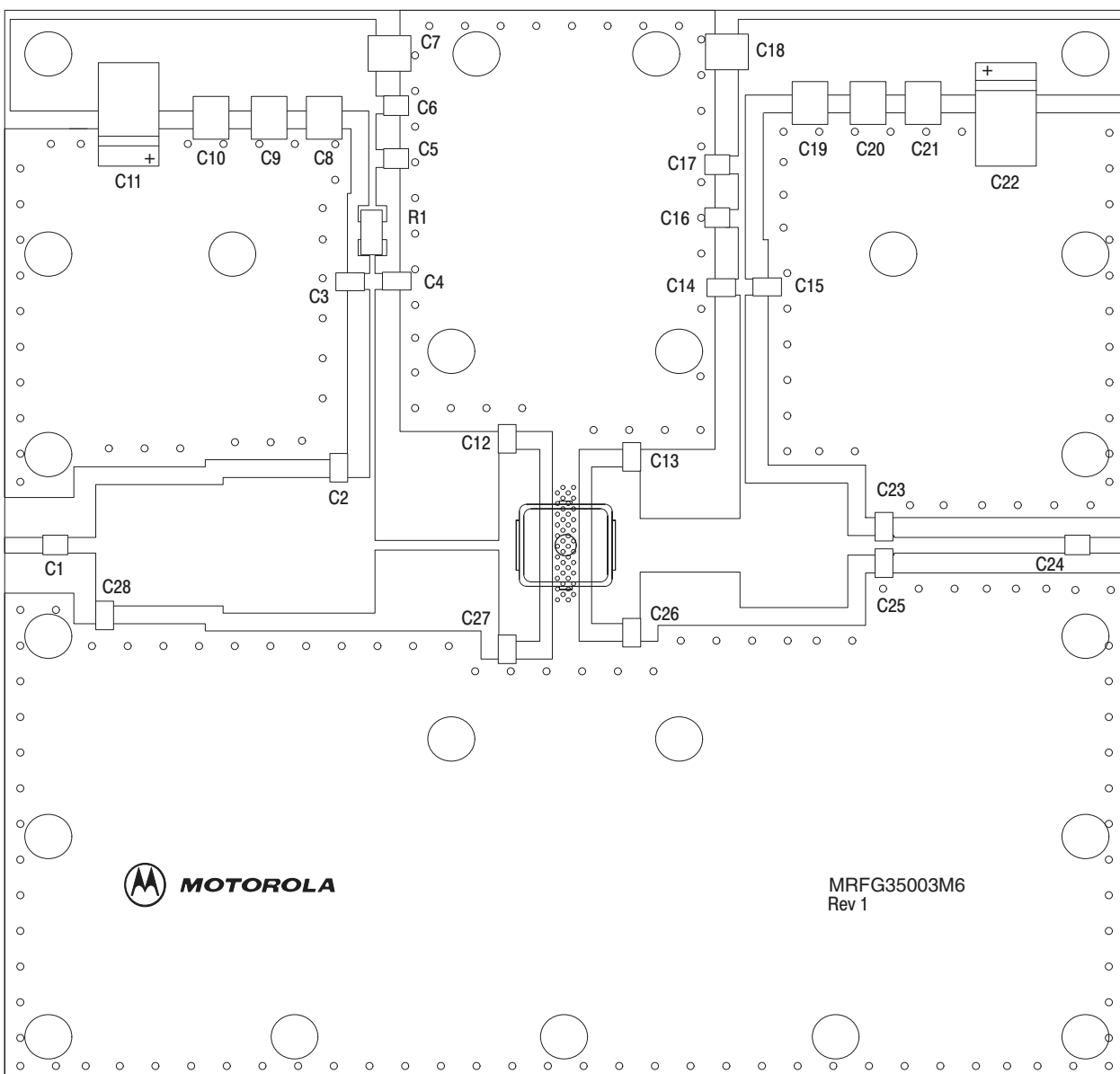


Figure 2. 3.5 GHz Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

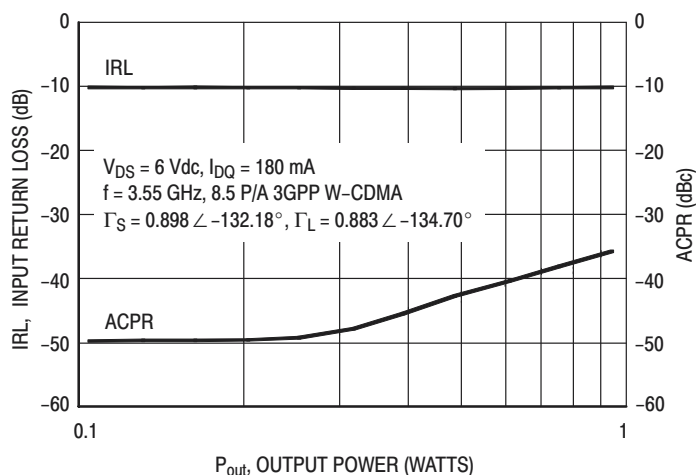


Figure 3. W-CDMA ACPR and Input Return Loss versus Output Power

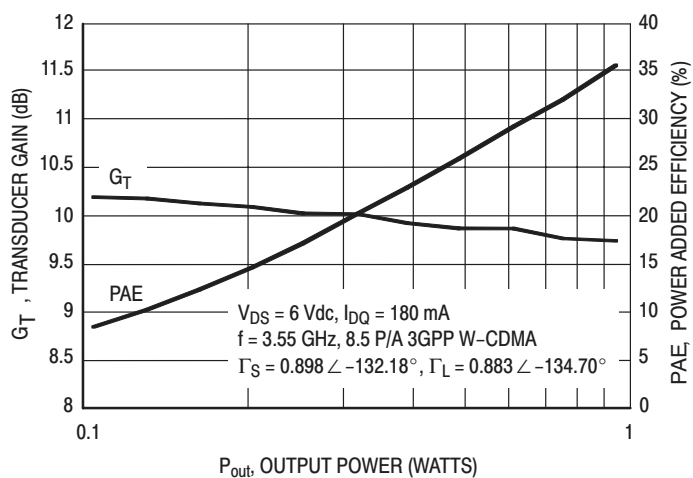


Figure 4. Transducer Gain and Power Added Efficiency versus Output Power

NOTE: All data is referenced to package lead interface. Γ_S and Γ_L are the impedances presented to the DUT. All data is generated from load pull, not from the test circuit shown.

Freescale Semiconductor, Inc.

Table 2. Class AB Common Source S-Parameters at $V_{DS} = 6 \text{ Vdc}$, $I_{DQ} = 180 \text{ mA}$

f GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
0.5	0.954	-176.79	3.859	84.89	0.016	9.07	0.847	178.96
0.55	0.953	-177.98	3.527	83.61	0.016	8.90	0.846	178.38
0.6	0.952	-179.13	3.250	82.29	0.016	8.49	0.846	177.74
0.65	0.952	179.80	3.019	80.95	0.016	8.44	0.845	177.07
0.7	0.952	178.89	2.818	79.74	0.016	8.51	0.844	176.28
0.75	0.951	177.96	2.643	78.49	0.016	8.53	0.844	175.55
0.8	0.952	177.03	2.491	77.11	0.017	8.75	0.843	174.77
0.85	0.952	176.22	2.354	75.85	0.017	8.61	0.842	173.93
0.9	0.951	175.46	2.234	74.67	0.017	8.62	0.842	173.12
0.95	0.951	174.66	2.124	73.38	0.017	8.56	0.841	172.27
1	0.952	173.92	2.025	72.17	0.017	8.48	0.841	171.37
1.05	0.951	173.18	1.934	70.97	0.017	8.47	0.841	170.50
1.1	0.951	172.40	1.851	69.68	0.017	8.93	0.841	169.75
1.15	0.951	171.63	1.774	68.46	0.017	8.90	0.840	168.89
1.2	0.951	170.90	1.704	67.25	0.018	8.79	0.841	168.10
1.25	0.950	170.06	1.638	65.98	0.018	8.80	0.841	167.34
1.3	0.951	169.23	1.576	64.74	0.018	8.44	0.840	166.61
1.35	0.946	168.58	1.518	63.62	0.018	8.76	0.838	166.13
1.4	0.952	167.47	1.463	62.45	0.018	9.00	0.845	165.24
1.45	0.949	166.77	1.411	61.29	0.018	8.57	0.841	164.98
1.5	0.949	163.72	1.360	60.14	0.018	8.15	0.842	166.78
1.55	0.948	162.94	1.317	59.12	0.018	8.28	0.843	166.27
1.6	0.947	162.21	1.276	58.03	0.018	8.51	0.843	165.71
1.65	0.950	161.60	1.237	56.92	0.018	8.31	0.843	165.16
1.7	0.951	160.97	1.201	55.93	0.018	8.40	0.844	164.60
1.75	0.950	160.44	1.167	54.89	0.018	8.35	0.844	164.10
1.8	0.950	159.95	1.135	53.83	0.019	8.44	0.844	163.47
1.85	0.952	159.46	1.105	52.85	0.019	8.61	0.843	162.87
1.9	0.951	159.01	1.076	51.92	0.019	8.34	0.844	162.37
1.95	0.950	158.58	1.049	50.84	0.019	7.93	0.843	161.77
2	0.952	158.25	1.024	49.95	0.019	8.02	0.843	161.24
2.05	0.951	157.84	1.000	49.06	0.019	7.86	0.844	160.75
2.1	0.951	157.48	0.979	48.17	0.019	7.67	0.845	160.26
2.15	0.952	157.17	0.959	47.22	0.019	7.24	0.843	159.69
2.2	0.952	156.89	0.939	46.34	0.020	6.89	0.843	159.08
2.25	0.952	156.63	0.921	45.44	0.020	6.73	0.844	158.58
2.3	0.952	156.35	0.904	44.48	0.020	6.86	0.843	158.07
2.35	0.953	155.98	0.888	43.57	0.020	6.83	0.842	157.42
2.4	0.951	155.66	0.873	42.68	0.020	6.80	0.842	156.97
2.45	0.952	155.28	0.860	41.72	0.020	6.74	0.842	156.47
2.5	0.952	154.86	0.848	40.82	0.020	6.73	0.840	155.83
2.55	0.950	154.44	0.836	39.90	0.021	6.72	0.841	155.29
2.6	0.949	153.93	0.826	38.89	0.021	6.86	0.840	154.74
2.65	0.950	153.36	0.815	37.85	0.021	6.74	0.838	154.18
2.7	0.949	152.82	0.806	36.81	0.022	6.24	0.838	153.62
2.75	0.946	152.08	0.797	35.75	0.022	5.69	0.839	153.16

Freescale Semiconductor, Inc.

Table 2. Class AB Common Source S-Parameters at $V_{DS} = 6 \text{ Vdc}$, $I_{DQ} = 180 \text{ mA}$ (continued)

f GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
2.8	0.946	151.55	0.787	34.63	0.022	4.64	0.836	152.55
2.85	0.946	150.81	0.778	33.54	0.023	3.61	0.836	152.02
2.9	0.945	150.11	0.770	32.46	0.023	2.16	0.837	151.54
2.95	0.945	149.30	0.762	31.37	0.023	1.54	0.835	150.98
3	0.945	148.44	0.754	30.25	0.023	1.03	0.835	150.40
3.05	0.944	147.58	0.747	29.09	0.023	0.48	0.837	149.89
3.1	0.943	146.55	0.739	27.89	0.023	0.15	0.835	149.35
3.15	0.943	145.54	0.732	26.69	0.023	-0.33	0.834	148.72
3.2	0.944	144.52	0.725	25.53	0.023	-0.41	0.836	148.13
3.25	0.941	143.47	0.718	24.33	0.023	-0.52	0.835	147.62
3.3	0.941	142.43	0.711	23.09	0.023	-1.22	0.834	147.01
3.35	0.941	141.33	0.704	21.89	0.023	-1.40	0.834	146.44
3.4	0.940	140.22	0.697	20.67	0.024	-1.31	0.834	145.89
3.45	0.939	139.25	0.689	19.44	0.024	-1.58	0.832	145.40
3.5	0.940	138.09	0.682	18.26	0.024	-1.85	0.833	144.66
3.55	0.940	137.05	0.675	17.08	0.024	-2.29	0.834	144.11
3.6	0.939	136.07	0.668	15.88	0.025	-2.75	0.832	143.59
3.65	0.941	135.06	0.661	14.68	0.025	-3.55	0.831	142.91
3.7	0.939	134.20	0.653	13.50	0.025	-4.69	0.832	142.34
3.75	0.939	133.35	0.646	12.39	0.025	-5.45	0.831	141.92
3.8	0.939	132.47	0.639	11.29	0.025	-6.34	0.830	141.27
3.85	0.940	131.67	0.632	10.20	0.025	-6.85	0.831	140.64
3.9	0.939	130.89	0.625	9.15	0.025	-6.90	0.831	140.02
3.95	0.940	130.26	0.619	8.10	0.025	-6.60	0.830	139.40
4	0.941	129.57	0.613	7.10	0.025	-6.63	0.830	138.76
4.05	0.941	128.98	0.608	6.11	0.026	-6.67	0.831	138.17
4.1	0.942	128.44	0.602	5.10	0.026	-7.00	0.830	137.56
4.15	0.942	128.03	0.598	4.14	0.026	-7.30	0.828	136.87
4.2	0.941	127.57	0.593	3.17	0.027	-7.73	0.828	136.20
4.25	0.940	127.14	0.589	2.15	0.027	-8.12	0.827	135.56
4.3	0.941	126.75	0.585	1.21	0.027	-8.11	0.826	134.85
4.35	0.941	126.39	0.581	0.25	0.027	-8.33	0.826	134.13
4.4	0.939	125.97	0.578	-0.74	0.028	-8.73	0.825	133.44
4.45	0.939	125.64	0.575	-1.67	0.028	-8.92	0.823	132.68
4.5	0.939	125.36	0.573	-2.59	0.029	-9.42	0.823	131.92
4.55	0.938	124.98	0.571	-3.50	0.029	-9.66	0.823	131.23
4.6	0.938	124.55	0.570	-4.53	0.030	-10.28	0.822	130.45
4.65	0.938	124.20	0.571	-5.52	0.030	-10.87	0.821	129.60
4.7	0.937	123.76	0.570	-6.60	0.031	-11.91	0.821	128.79
4.75	0.935	123.17	0.569	-7.76	0.031	-13.22	0.819	127.98
4.8	0.935	122.58	0.569	-8.89	0.031	-14.16	0.817	127.09
4.85	0.934	121.93	0.570	-9.98	0.031	-14.45	0.817	126.23
4.9	0.932	121.14	0.570	-11.17	0.032	-14.82	0.816	125.41
4.95	0.932	120.43	0.571	-12.37	0.032	-14.82	0.815	124.46
5	0.929	119.55	0.573	-13.61	0.032	-14.83	0.815	123.55

The RF GaAs Line

Gallium Arsenide PHEMT

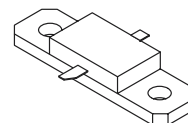
RF Power Field Effect Transistor

MRFG35010

**3.5 GHz, 10 W, 12 V
POWER FET
GaAs PHEMT**

Designed for WLL/MMDS or UMTS driver applications with frequencies from 1.8 to 3.6 GHz. Device is unmatched and is suitable for use in Class AB or Class A linear base station applications.

- Typical W-CDMA Performance: -42 dBc ACPR, 3.55 GHz, 12 Volts, $I_{DQ} = 180$ mA, 5 MHz Offset/3.84 MHz BW, 64 DPCH (8.5 dB P/A @ 0.01% Probability)
Output Power — 1 Watt
Power Gain — 10 dB
Efficiency — 30%
- 10 Watts P1dB @ 3.55 GHz
- Excellent Phase Linearity and Group Delay Characteristics
- High Gain, High Efficiency and High Linearity



**CASE 360D-02, STYLE 1
NI-360HF**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	28.3 0.19	Watts W/ $^\circ\text{C}$
Gate-Source Voltage	V_{GS}	- 5	Vdc
RF Input Power	P_{in}	33	dBm
Storage Temperature Range	T_{stg}	- 65 to +175	$^\circ\text{C}$
Channel Temperature ⁽¹⁾	T_{ch}	175	$^\circ\text{C}$
Operating Case Temperature Range	T_C	- 45 to +90	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Class A Class AB	$R_{\theta JC}$	5.3 4.8	$^\circ\text{C}/\text{W}$

(1) For reliable operation, the operating channel temperature should not exceed 150°C .

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Saturated Drain Current (V _{DS} = 3.5 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	2.9	—	Adc
Off State Leakage Current (V _{GS} = -0.4 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	< 1.0	100	μAdc
Off State Drain Current (V _{DS} = 12 Vdc, V _{GS} = -1.9 Vdc)	I _{DSO}	—	0.09	1.0	mAdc
Off State Current (V _{DS} = 28.5 Vdc, V _{GS} = -2.5 Vdc)	I _{DSX}	—	5.0	15	mAdc
Gate–Source Cut–off Voltage (V _{DS} = 3.5 Vdc, I _{DS} = 15 mA)	V _{GS(th)}	-1.2	-0.8	-0.7	Vdc
Quiescent Gate Voltage (V _{DS} = 12 Vdc, I _D = 180 mA)	V _{GS(Q)}	-1.0	-0.8	-0.5	Vdc
Power Gain (V _{DD} = 12 Vdc, I _{DQ} = 180 mA, f = 3.55 GHz)	G _{ps}	9.0	10	—	dB
Output Power, 1 dB Compression Point (V _{DD} = 12 Vdc, I _{DQ} = 180 mA, f = 3.55 GHz)	P1dB	—	10	—	W
Drain Efficiency (V _{DD} = 12 Vdc, I _{DQ} = 180 mA, P _{out} = 1.0 W Avg., f = 3.55 GHz)	η _D	23	30	—	%
Adjacent Channel Power Ratio (V _{DD} = 12 Vdc, P _{out} = 1.0 W Avg., I _{DQ} = 180 mA, f = 3.55 GHz, W–CDMA, 8.5 P/A @ 0.01% Probability, 64 CH, 3.84 MCPS)	ACPR	—	-42	-40	dBc

Freescale Semiconductor, Inc.

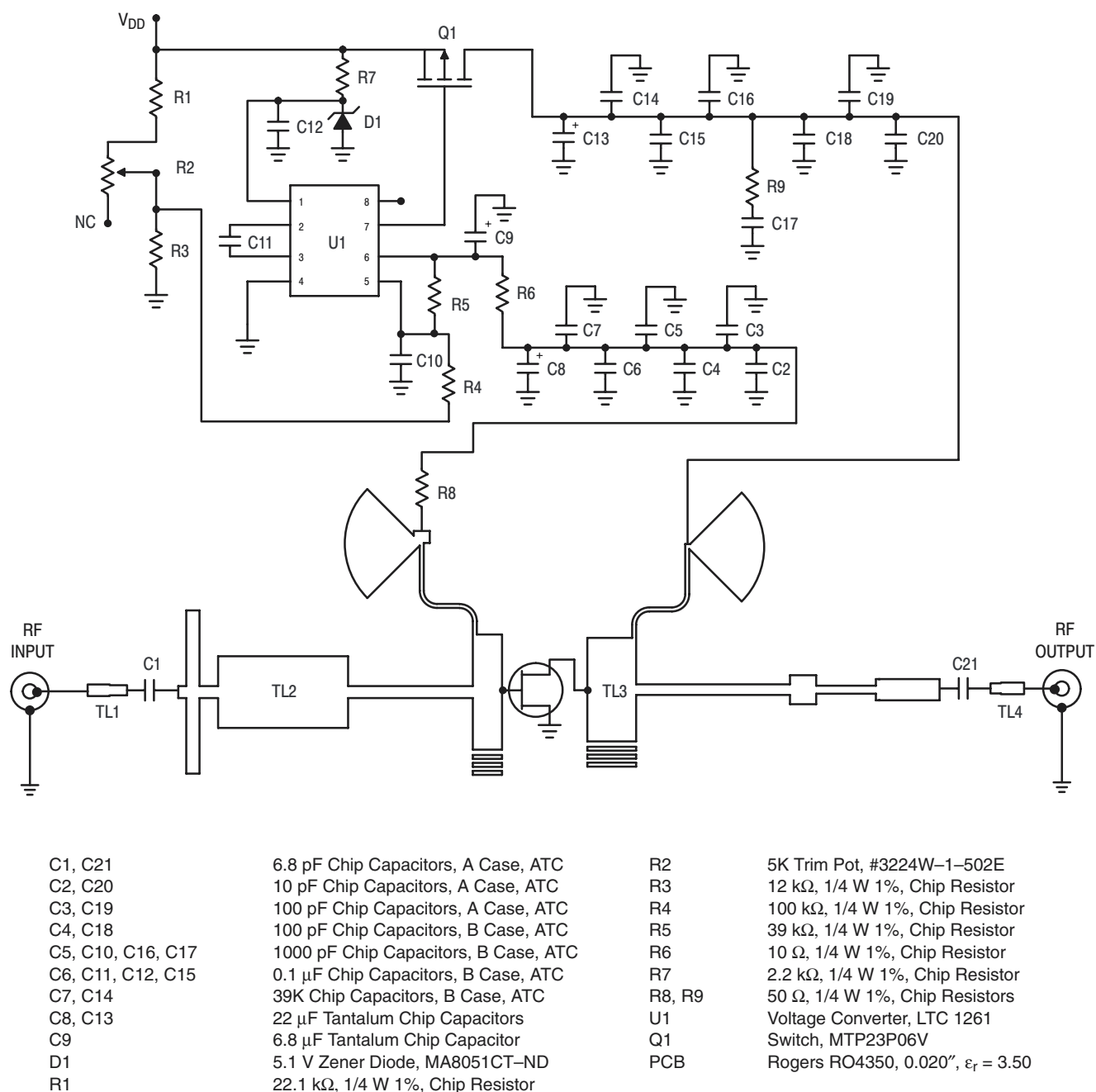


Figure 1. 3.4 – 3.6 GHz Single Supply Bias Sequencing Test Circuit Schematic

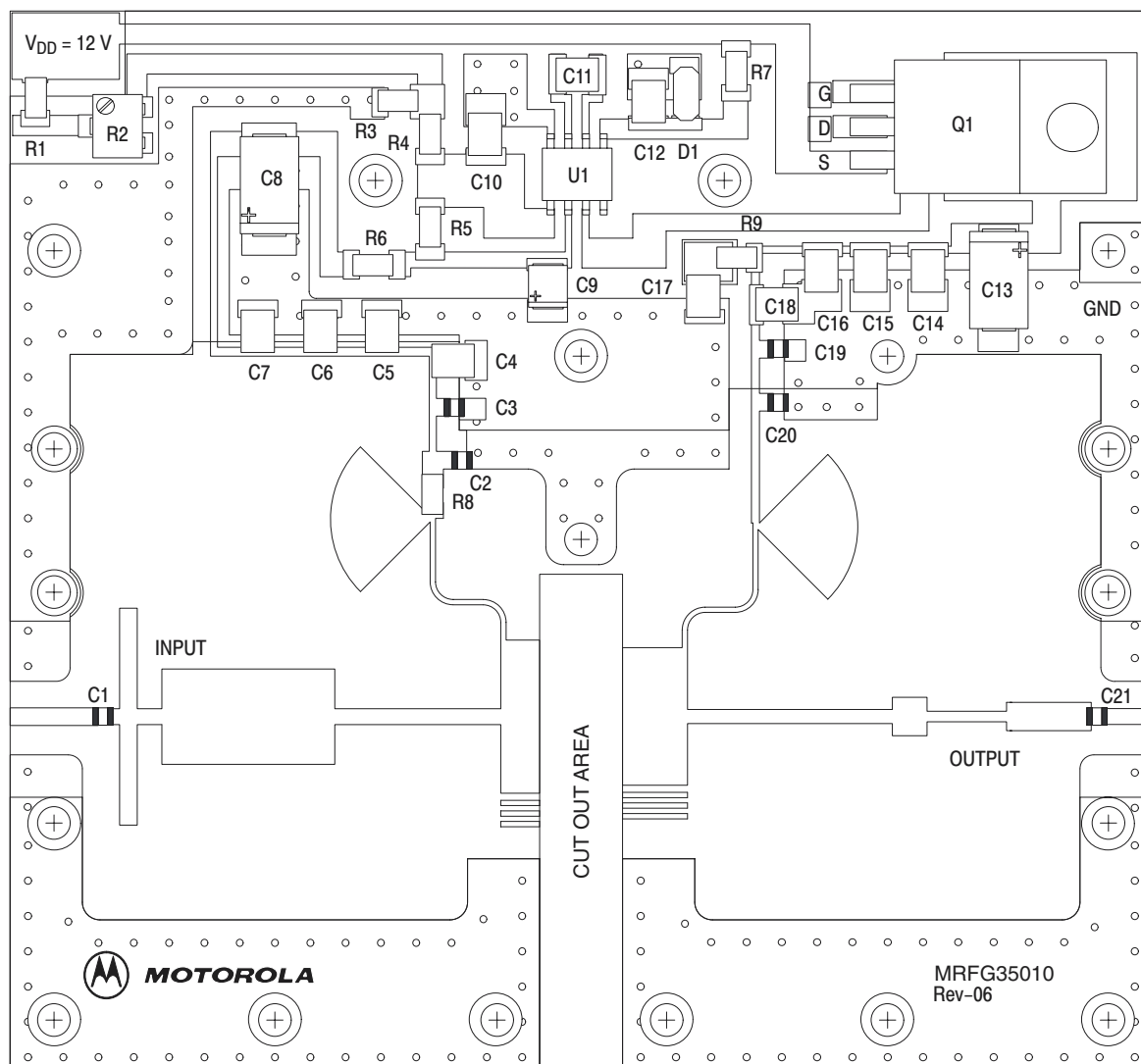


Figure 2. 3.4 – 3.6 GHz Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

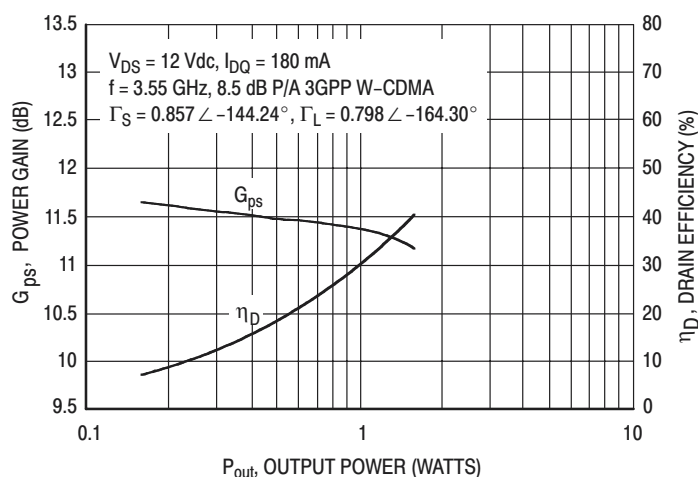


Figure 3. Power Gain and Drain Efficiency versus Output Power

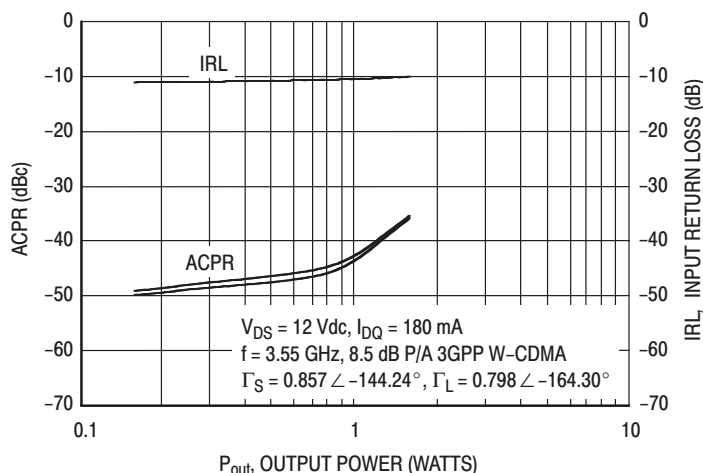


Figure 4. W-CDMA ACPR and Input Return Loss versus Output Power

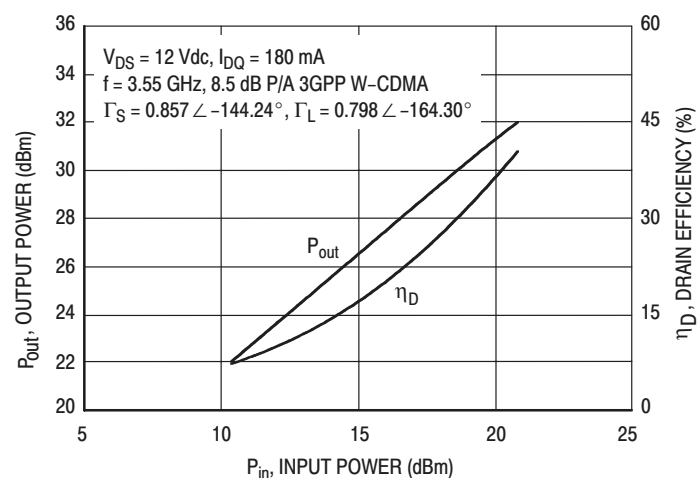
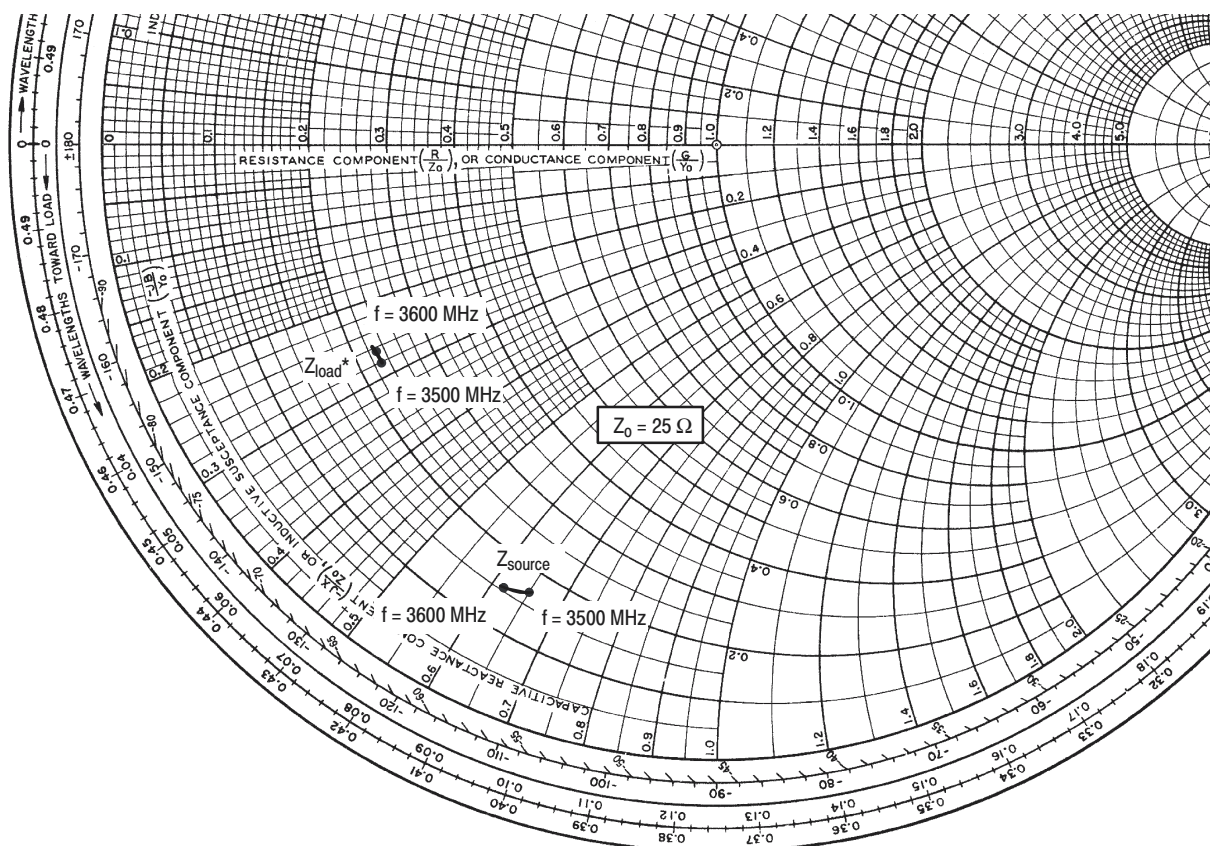


Figure 5. W-CDMA Output Power and Drain Efficiency versus Input Power

NOTE: All data is referenced to package lead interface. Γ_S and Γ_L are the impedances presented to the DUT. All data is generated from load pull, not from the test circuit shown.



$V_{DD} = 12 \text{ V}$, $I_{DQ} = 180 \text{ mA}$, $P_{\text{out}} = 1 \text{ W}$

f MHz	Z_{source} Ω	Z_{load} Ω
3500	$4.3 - j16.3$	$5.7 - j7.0$
3550	$4.2 - j16.0$	$5.7 - j6.8$
3600	$4.1 - j15.8$	$5.7 - j6.6$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

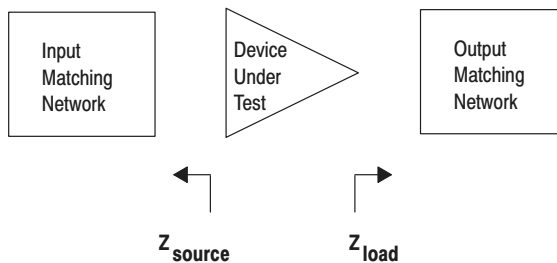


Figure 6. Series Equivalent Input and Output Impedance

Freescale Semiconductor, Inc.

Table 1. Class A Common Source S-Parameters at $V_{DS} = 12 \text{ Vdc}$, $I_{DQ} = 1000 \text{ mA}$

f GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
0.50	0.956	-177.95	5.591	79.60	0.007	15.64	0.741	179.71
0.60	0.957	-179.86	4.668	76.30	0.007	23.81	0.739	179.15
0.70	0.956	178.44	4.007	73.21	0.008	23.84	0.736	178.75
0.80	0.956	177.05	3.520	70.18	0.008	26.09	0.736	178.29
0.90	0.954	175.83	3.138	67.20	0.009	30.55	0.735	177.85
1.00	0.955	174.61	2.842	64.30	0.010	28.91	0.735	177.42
1.10	0.954	173.42	2.604	61.65	0.009	31.64	0.734	176.95
1.20	0.952	172.29	2.402	58.87	0.011	31.90	0.735	176.52
1.30	0.952	171.25	2.236	56.13	0.011	36.06	0.735	175.97
1.40	0.950	170.02	2.098	53.34	0.011	33.99	0.736	175.52
1.50	0.950	168.36	2.054	50.41	0.011	32.65	0.725	174.86
1.60	0.948	167.24	1.944	47.63	0.012	32.47	0.725	174.31
1.70	0.946	166.01	1.850	44.77	0.013	37.07	0.725	173.70
1.80	0.944	164.67	1.769	42.06	0.014	34.40	0.725	172.90
1.90	0.943	163.59	1.698	39.29	0.015	35.71	0.725	172.32
2.00	0.942	162.31	1.638	36.53	0.015	37.47	0.724	171.58
2.10	0.940	161.09	1.580	33.69	0.016	35.82	0.724	170.75
2.20	0.938	159.66	1.532	30.84	0.017	35.69	0.722	169.89
2.30	0.937	158.30	1.491	28.03	0.017	35.43	0.721	169.04
2.40	0.935	156.86	1.454	25.19	0.019	34.19	0.720	168.15
2.50	0.934	155.35	1.422	22.38	0.020	34.10	0.718	167.32
2.60	0.932	153.83	1.396	19.54	0.021	35.51	0.718	166.38
2.70	0.928	152.26	1.375	16.68	0.022	33.15	0.716	165.61
2.80	0.926	150.58	1.356	13.80	0.023	30.84	0.714	164.67
2.90	0.923	148.97	1.342	10.91	0.025	31.00	0.711	163.77
3.00	0.920	147.18	1.332	7.87	0.027	29.11	0.708	162.89
3.10	0.917	145.27	1.328	4.88	0.028	28.98	0.704	161.96
3.20	0.913	143.23	1.326	1.73	0.030	27.36	0.699	161.08
3.30	0.908	141.12	1.329	-1.48	0.032	25.93	0.694	160.09
3.40	0.903	138.91	1.335	-4.80	0.034	24.33	0.687	159.09
3.50	0.897	136.46	1.346	-8.26	0.036	22.30	0.679	158.02
3.60	0.893	133.77	1.360	-11.89	0.039	19.80	0.670	156.93
3.70	0.884	130.86	1.375	-15.61	0.042	17.46	0.659	155.90
3.80	0.875	127.58	1.393	-19.50	0.045	15.22	0.648	154.96
3.90	0.866	124.06	1.417	-23.55	0.048	13.31	0.636	154.06
4.00	0.851	120.13	1.443	-27.75	0.052	10.27	0.626	153.16
4.10	0.833	115.98	1.472	-32.06	0.056	7.36	0.618	152.14
4.20	0.814	111.48	1.505	-36.63	0.060	4.18	0.609	151.13
4.30	0.793	106.69	1.541	-41.44	0.065	1.13	0.602	149.84
4.40	0.771	101.44	1.581	-46.57	0.071	-3.19	0.592	148.47
4.50	0.748	95.69	1.622	-51.82	0.076	-7.50	0.582	147.06
4.60	0.723	89.38	1.668	-57.33	0.082	-11.79	0.575	145.72
4.70	0.697	82.41	1.721	-63.32	0.089	-16.57	0.568	144.03
4.80	0.672	74.51	1.771	-69.70	0.096	-22.28	0.559	142.02
4.90	0.647	65.82	1.818	-76.56	0.103	-28.04	0.549	139.82
5.00	0.622	56.14	1.860	-83.67	0.110	-33.91	0.539	137.39

Freescale Semiconductor, Inc.

Table 2. Class AB Common Source S-Parameters at $V_{DS} = 12 \text{ Vdc}$, $I_{DQ} = 180 \text{ mA}$

f GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
0.50	0.936	-175.05	5.292	80.70	0.014	3.73	0.735	-178.66
0.60	0.936	-177.28	4.422	77.20	0.014	3.63	0.735	-179.61
0.70	0.935	-179.21	3.803	74.02	0.015	3.78	0.735	179.80
0.80	0.935	179.21	3.341	70.87	0.014	7.22	0.736	179.20
0.90	0.935	177.77	2.983	67.85	0.014	5.83	0.738	178.58
1.00	0.934	176.46	2.701	64.80	0.015	7.03	0.738	178.09
1.10	0.934	175.26	2.473	62.00	0.015	7.15	0.738	177.54
1.20	0.933	174.05	2.284	59.24	0.014	6.85	0.739	177.01
1.30	0.933	172.86	2.124	56.47	0.015	6.90	0.740	176.42
1.40	0.933	171.71	1.991	53.70	0.015	8.93	0.739	175.92
1.50	0.929	170.06	1.948	50.73	0.016	7.81	0.730	175.22
1.60	0.930	168.89	1.845	47.88	0.016	8.58	0.731	174.51
1.70	0.927	167.73	1.757	44.99	0.016	8.16	0.731	173.88
1.80	0.926	166.37	1.678	42.32	0.016	10.00	0.730	173.09
1.90	0.925	165.33	1.610	39.48	0.017	9.25	0.732	172.45
2.00	0.923	164.05	1.551	36.70	0.018	11.89	0.731	171.71
2.10	0.921	162.82	1.498	33.90	0.018	10.06	0.731	170.85
2.20	0.920	161.49	1.451	31.07	0.018	10.11	0.730	170.01
2.30	0.918	160.17	1.411	28.22	0.019	10.86	0.729	169.14
2.40	0.916	158.74	1.376	25.43	0.020	9.05	0.728	168.25
2.50	0.916	157.35	1.347	22.58	0.020	8.57	0.727	167.43
2.60	0.913	155.97	1.321	19.80	0.021	9.64	0.727	166.51
2.70	0.912	154.45	1.300	16.98	0.022	10.23	0.725	165.61
2.80	0.909	152.83	1.280	14.05	0.023	9.68	0.723	164.76
2.90	0.907	151.25	1.268	11.14	0.024	10.24	0.719	163.70
3.00	0.904	149.54	1.257	8.18	0.026	7.35	0.717	162.83
3.10	0.901	147.76	1.253	5.20	0.026	9.11	0.714	161.86
3.20	0.896	145.88	1.253	2.11	0.028	6.33	0.709	160.85
3.30	0.893	143.83	1.255	-1.10	0.030	7.09	0.704	159.82
3.40	0.887	141.78	1.260	-4.43	0.031	5.16	0.697	158.76
3.50	0.882	139.43	1.268	-7.81	0.033	4.74	0.690	157.60
3.60	0.876	136.99	1.281	-11.29	0.035	4.34	0.682	156.46
3.70	0.870	134.24	1.295	-14.96	0.038	1.64	0.672	155.26
3.80	0.863	131.29	1.311	-18.72	0.040	0.43	0.660	154.16
3.90	0.853	127.96	1.334	-22.68	0.042	-2.33	0.650	153.12
4.00	0.840	124.33	1.354	-26.85	0.046	-4.01	0.639	152.16
4.10	0.825	120.40	1.386	-31.01	0.049	-6.67	0.632	150.97
4.20	0.807	116.26	1.414	-35.40	0.053	-9.06	0.624	149.72
4.30	0.787	111.78	1.453	-40.01	0.057	-11.29	0.617	148.33
4.40	0.767	106.97	1.492	-44.83	0.061	-14.79	0.608	146.78
4.50	0.745	101.74	1.537	-49.99	0.066	-18.66	0.599	145.00
4.60	0.721	95.90	1.579	-55.50	0.071	-22.20	0.589	143.33
4.70	0.697	89.39	1.633	-61.25	0.077	-26.02	0.580	141.41
4.80	0.674	82.09	1.685	-67.46	0.084	-30.63	0.569	139.21
4.90	0.647	73.93	1.740	-74.01	0.090	-35.78	0.557	136.94
5.00	0.622	64.84	1.790	-81.02	0.097	-41.70	0.545	134.20

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Advance Information

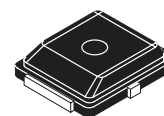
The RF GaAs Line **Gallium Arsenide PHEMT** **RF Power Field Effect Transistor**

Designed for WLL/MMDS/BWA or UMTS driver applications with frequencies from 1.8 to 3.6 GHz. Device is unmatched and is suitable for use in Class AB linear base station applications.

- Typical W-CDMA Performance: -42 dBc ACPR, 3.55 GHz, 12 Volts, $I_{DQ} = 180$ mA, 5 MHz Offset/3.84 MHz BW, 64 DPCH (8.5 dB P/A @ 0.01% Probability)
 Output Power — 900 mW
 Power Gain — 10 dB
 Efficiency — 28%
- 9 Watts P1dB @ 3.55 GHz
- Excellent Phase Linearity and Group Delay Characteristics
- High Gain, High Efficiency and High Linearity
- In Tape and Reel. T1 Suffix = 1000 Units per 12 mm, 7 inch Reel.

MRFG35010MT1

3.5 GHz, 9 W, 12 V
POWER FET
GaAs PHEMT



CASE 466-02, STYLE 1
PLD-1.5
PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	22.7 ⁽²⁾ 0.15 ⁽²⁾	Watts W/ $^\circ\text{C}$
Gate-Source Voltage	V_{GS}	- 5	Vdc
RF Input Power	P_{in}	33	dBm
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Channel Temperature ⁽¹⁾	T_{ch}	175	$^\circ\text{C}$
Operating Case Temperature Range	T_C	- 40 to +85	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.6 ⁽²⁾	$^\circ\text{C/W}$

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	MSL1

(1) For reliable operation, the operating channel temperature should not exceed 150°C .

(2) Simulated.

REV 0

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Saturated Drain Current (V _{DS} = 3.5 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	2.9	—	Adc
Off State Leakage Current (V _{GS} = -0.4 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	< 1.0	100	μAdc
Off State Drain Current (V _{DS} = 12 Vdc, V _{GS} = -1.9 Vdc)	I _{DSO}	—	0.1	1.0	mAdc
Off State Current (V _{DS} = 28.5 Vdc, V _{GS} = -2.5 Vdc)	I _{DSX}	—	2.0	15	mAdc
Gate-Source Cut-off Voltage (V _{DS} = 3.5 Vdc, I _{DS} = 15 mA)	V _{GS(th)}	-1.2	-1.0	-0.7	Vdc
Quiescent Gate Voltage (V _{DS} = 12 Vdc, I _{DQ} = 180 mA)	V _{GS(Q)}	-1.2	-0.95	-0.7	Vdc
Power Gain (V _{DD} = 12 Vdc, I _{DQ} = 180 mA, f = 3.55 GHz)	G _{ps}	9.0	10	—	dB
Output Power, 1 dB Compression Point (V _{DD} = 12 Vdc, I _{DQ} = 180 mA, f = 3.55 GHz)	P1dB	—	9	—	W
Drain Efficiency (V _{DD} = 12 Vdc, I _{DQ} = 180 mA, P _{out} = 900 mW Avg., f = 3.55 GHz)	η _D	23	28	—	%
Adjacent Channel Power Ratio (V _{DD} = 12 Vdc, P _{out} = 900 mW Avg., I _{DQ} = 180 mA, f = 3.55 GHz, W-CDMA, 8.5 P/A @ 0.01% Probability, 64 CH, 3.84 MCPS)	ACPR	—	-43	-40	dBc

Freescale Semiconductor, Inc.

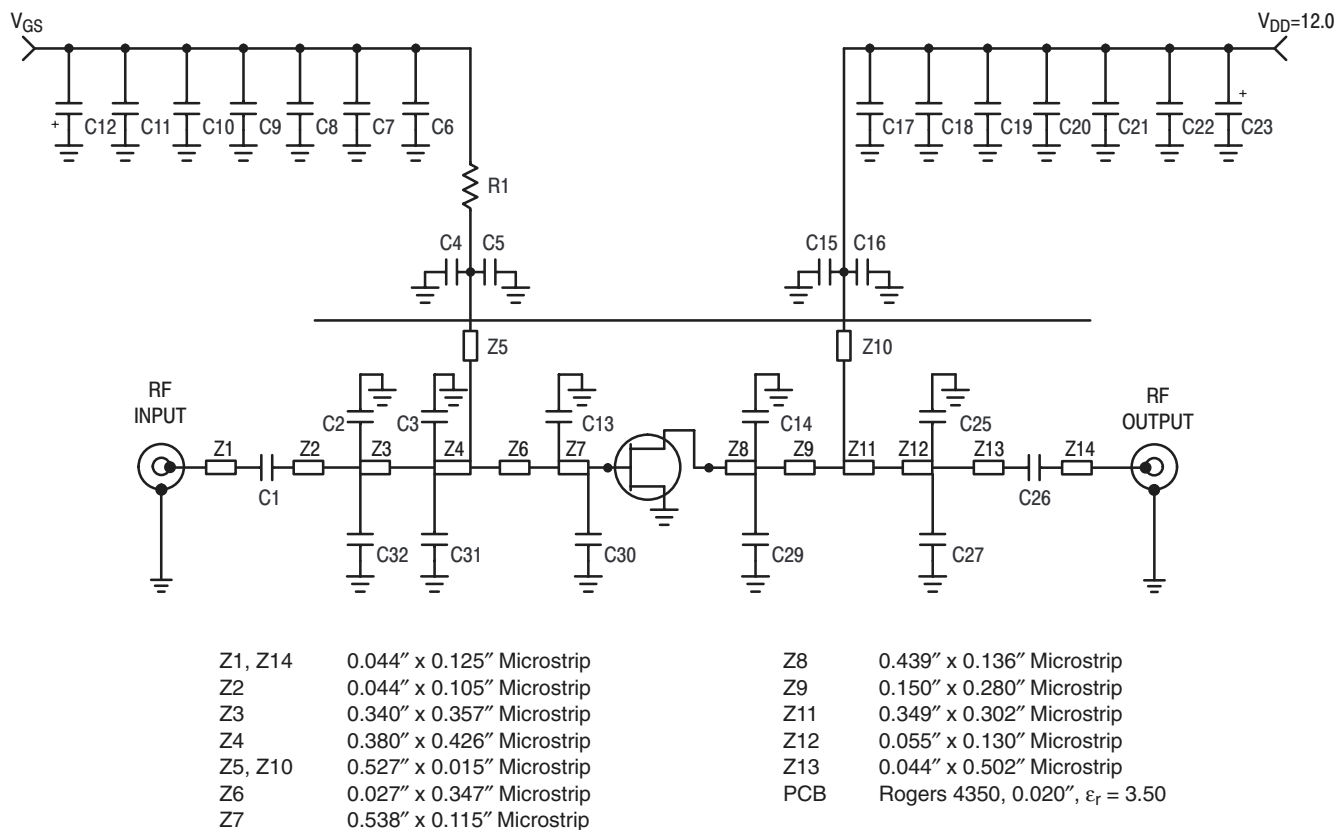


Figure 1. 3.5 GHz Test Circuit Schematic

Table 1. 3.5 GHz Test Circuit Component Designations and Values

Designation	Description
C1, C26	7.5 pF Chip Capacitors, B Case, ATC
C2, C14	0.4 pF Chip Capacitors (0805), AVX
C3, C13, C30	0.2 pF Chip Capacitors (0805), AVX
C4, C5, C15, C16	3.9 pF Chip Capacitors, AVX
C6, C17	10 pF Chip Capacitors, A Case, ATC
C7, C18	100 pF Chip Capacitors, A Case, ATC
C8, C19	100 pF Chip Capacitors, B Case, ATC
C9, C20	1000 pF Chip Capacitors, B Case, ATC
C10, C21	0.1 μ F Chip Capacitors, B Case, ATC
C11, C22	3.9 μ F Chip Capacitors, B Case, ATC
C12, C23	22 μ F, 35 V Tantalum Surface Mount Capacitors, Newark
C25, C27	1.0 pF Chip Capacitors (0805), AVX
C29	0.7 pF Chip Capacitor (0805), AVX
R1	50 Ω Chip Resistor, Newark

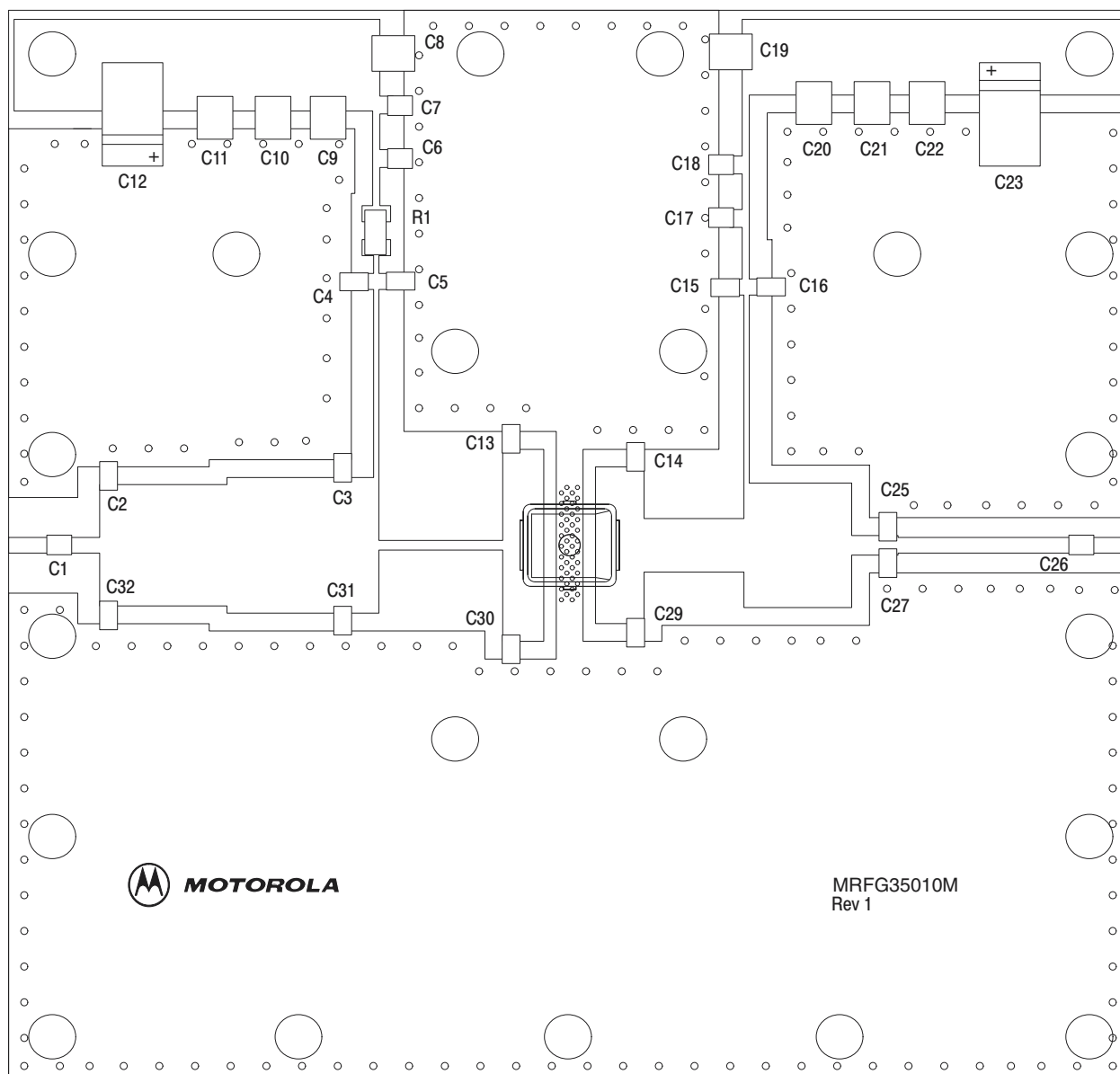


Figure 2. 3.5 GHz Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

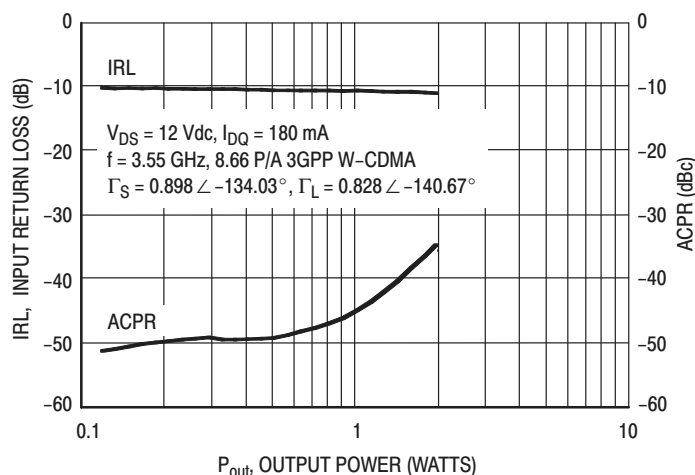


Figure 3. W-CDMA ACPR and Input Return Loss versus Output Power

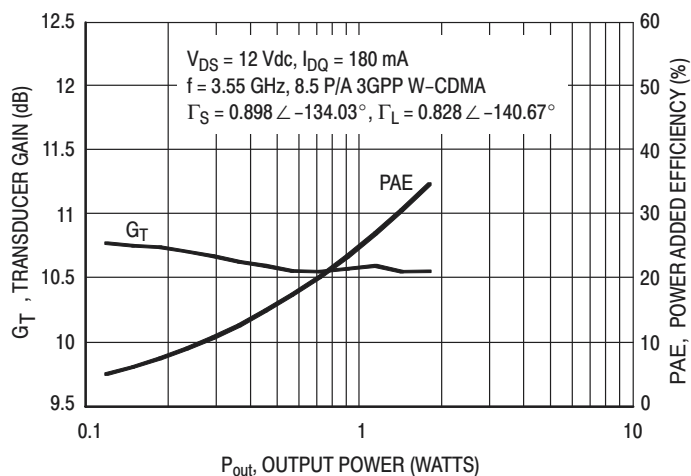


Figure 4. Transducer Gain and Power Added Efficiency versus Output Power

NOTE: All data is referenced to package lead interface. Γ_S and Γ_L are the impedances presented to the DUT. All data is generated from load pull, not from the test circuit shown.

Freescale Semiconductor, Inc.

Table 2. Class AB Common Source S-Parameters at $V_{DS} = 12 \text{ Vdc}$, $I_{DQ} = 180 \text{ mA}$

f GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
0.5	0.946	-177.11	4.710	82.28	0.016	8.19	0.759	-179.39
0.55	0.945	-178.28	4.303	80.79	0.016	7.57	0.758	-179.99
0.6	0.944	-179.44	3.963	79.23	0.016	7.60	0.758	179.39
0.65	0.945	179.50	3.674	77.69	0.016	7.44	0.758	178.74
0.7	0.945	178.60	3.427	76.28	0.016	7.44	0.757	177.98
0.75	0.944	177.66	3.211	74.83	0.016	7.21	0.757	177.28
0.8	0.945	176.74	3.023	73.24	0.017	7.65	0.756	176.57
0.85	0.945	175.95	2.853	71.74	0.017	7.16	0.756	175.75
0.9	0.944	175.17	2.705	70.36	0.017	7.34	0.756	174.99
0.95	0.945	174.36	2.570	68.88	0.017	7.31	0.755	174.18
1	0.945	173.63	2.447	67.47	0.017	7.08	0.755	173.33
1.05	0.944	172.90	2.337	66.06	0.017	7.29	0.756	172.51
1.1	0.944	172.09	2.234	64.52	0.017	7.56	0.756	171.82
1.15	0.944	171.29	2.139	63.11	0.017	7.46	0.756	171.01
1.2	0.944	170.57	2.052	61.73	0.017	7.43	0.757	170.22
1.25	0.943	169.71	1.971	60.26	0.017	7.47	0.757	169.52
1.3	0.944	168.85	1.894	58.81	0.017	7.28	0.757	168.83
1.35	0.940	168.20	1.823	57.49	0.017	7.56	0.755	168.39
1.4	0.946	167.07	1.754	56.13	0.017	7.92	0.762	167.55
1.45	0.943	166.35	1.691	54.75	0.018	7.59	0.759	167.32
1.5	0.944	163.30	1.626	53.36	0.017	7.06	0.762	169.20
1.55	0.943	162.54	1.573	52.16	0.017	7.24	0.763	168.75
1.6	0.942	161.81	1.523	50.87	0.017	7.48	0.764	168.22
1.65	0.945	161.17	1.474	49.56	0.018	7.46	0.765	167.71
1.7	0.946	160.55	1.429	48.35	0.017	7.46	0.766	167.18
1.75	0.945	160.01	1.387	47.14	0.018	7.84	0.767	166.73
1.8	0.945	159.48	1.348	45.88	0.018	7.89	0.767	166.15
1.85	0.947	159.00	1.310	44.70	0.018	7.97	0.768	165.58
1.9	0.946	158.52	1.274	43.55	0.018	7.87	0.770	165.10
1.95	0.945	158.06	1.240	42.30	0.018	7.89	0.769	164.54
2	0.948	157.71	1.209	41.23	0.018	7.61	0.771	164.05
2.05	0.947	157.30	1.179	40.16	0.018	7.78	0.772	163.59
2.1	0.947	156.92	1.152	39.09	0.018	7.65	0.773	163.12
2.15	0.948	156.58	1.127	37.97	0.018	7.40	0.773	162.56
2.2	0.948	156.32	1.102	36.90	0.019	7.22	0.773	162.01
2.25	0.948	156.04	1.079	35.82	0.019	6.98	0.775	161.53
2.3	0.949	155.73	1.058	34.70	0.019	7.24	0.775	161.05
2.35	0.949	155.33	1.037	33.62	0.019	7.52	0.775	160.43
2.4	0.948	154.99	1.019	32.54	0.019	7.60	0.776	159.99
2.45	0.948	154.57	1.002	31.44	0.019	7.49	0.777	159.53
2.5	0.948	154.13	0.986	30.35	0.019	7.69	0.776	158.91
2.55	0.946	153.68	0.971	29.28	0.019	8.05	0.777	158.40
2.6	0.946	153.15	0.957	28.12	0.020	8.01	0.777	157.88
2.65	0.946	152.54	0.943	26.91	0.020	8.01	0.776	157.34
2.7	0.945	151.98	0.930	25.73	0.020	7.82	0.777	156.80
2.75	0.943	151.22	0.918	24.52	0.021	7.27	0.778	156.36

Freescale Semiconductor, Inc.

Table 2. Class AB Common Source S-Parameters at $V_{DS} = 12$ Vdc, $I_{DQ} = 180$ mA (continued)

f GHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
2.8	0.943	150.66	0.906	23.27	0.021	6.42	0.776	155.80
2.85	0.943	149.88	0.894	22.02	0.022	5.21	0.777	155.28
2.9	0.942	149.16	0.883	20.80	0.021	4.17	0.778	154.81
2.95	0.942	148.32	0.872	19.56	0.021	4.03	0.778	154.25
3	0.943	147.41	0.862	18.28	0.021	3.53	0.778	153.67
3.05	0.942	146.51	0.853	16.96	0.022	3.11	0.780	153.18
3.1	0.940	145.45	0.842	15.64	0.022	2.65	0.780	152.64
3.15	0.940	144.41	0.833	14.29	0.022	2.43	0.779	152.04
3.2	0.941	143.33	0.823	13.00	0.022	2.48	0.782	151.43
3.25	0.938	142.25	0.814	11.67	0.022	2.48	0.781	150.92
3.3	0.939	141.15	0.804	10.32	0.022	2.08	0.781	150.33
3.35	0.939	140.02	0.795	8.97	0.022	1.99	0.782	149.74
3.4	0.938	138.89	0.785	7.61	0.022	2.11	0.783	149.19
3.45	0.938	137.88	0.776	6.26	0.023	2.05	0.782	148.72
3.5	0.939	136.68	0.767	4.96	0.023	1.79	0.783	147.97
3.55	0.938	135.63	0.757	3.67	0.023	1.56	0.785	147.40
3.6	0.938	134.63	0.748	2.34	0.024	1.02	0.783	146.88
3.65	0.939	133.60	0.739	1.04	0.024	0.44	0.783	146.20
3.7	0.938	132.68	0.729	-0.25	0.024	-0.54	0.785	145.61
3.75	0.937	131.84	0.720	-1.47	0.024	-1.30	0.785	145.17
3.8	0.937	130.92	0.711	-2.69	0.024	-1.98	0.785	144.52
3.85	0.938	130.07	0.702	-3.89	0.024	-2.38	0.786	143.87
3.9	0.938	129.29	0.694	-5.07	0.024	-2.22	0.787	143.24
3.95	0.939	128.60	0.686	-6.23	0.024	-2.00	0.787	142.61
4	0.939	127.88	0.678	-7.34	0.025	-1.80	0.788	141.94
4.05	0.939	127.23	0.671	-8.46	0.025	-2.04	0.789	141.34
4.1	0.941	126.66	0.664	-9.57	0.025	-2.17	0.789	140.69
4.15	0.941	126.23	0.658	-10.65	0.025	-2.15	0.788	140.01
4.2	0.940	125.73	0.651	-11.72	0.026	-2.48	0.789	139.31
4.25	0.939	125.28	0.645	-12.82	0.026	-2.81	0.789	138.65
4.3	0.940	124.85	0.640	-13.86	0.026	-2.79	0.788	137.91
4.35	0.940	124.45	0.635	-14.92	0.027	-2.73	0.789	137.16
4.4	0.939	124.01	0.630	-16.00	0.027	-3.22	0.789	136.45
4.45	0.939	123.63	0.627	-17.01	0.028	-3.26	0.788	135.67
4.5	0.939	123.27	0.623	-18.03	0.028	-3.64	0.788	134.88
4.55	0.937	122.84	0.620	-19.03	0.029	-3.74	0.789	134.16
4.6	0.937	122.32	0.619	-20.17	0.029	-4.57	0.788	133.36
4.65	0.937	121.88	0.618	-21.26	0.030	-5.02	0.788	132.50
4.7	0.936	121.36	0.617	-22.45	0.030	-6.01	0.788	131.67
4.75	0.935	120.72	0.615	-23.68	0.031	-7.22	0.787	130.83
4.8	0.935	120.04	0.614	-24.90	0.031	-7.64	0.786	129.91
4.85	0.934	119.35	0.613	-26.12	0.031	-8.05	0.786	129.03
4.9	0.932	118.49	0.613	-27.41	0.031	-8.39	0.786	128.20
4.95	0.931	117.69	0.614	-28.72	0.032	-8.32	0.785	127.24
5	0.929	116.74	0.614	-30.05	0.033	-8.48	0.786	126.32

Chapter Six

Motorola RF Amplifier ICs and Modules – Data Sheets

Device Number	Page Number
Amplifier ICs and Modules	
MHL9236	6–3
MHL9236M	6–3
MHL9318	6–6
MHL9838	6–9
MHL18336	6–12
MHL18926	6–13
MHL19338	6–14
MHL19926	6–15
MHL19936	6–16
MHL21336	6–19
MHPA19010	6–22
MHPA21010	6–25
MHVIC910HR2	6–28
MHVIC915R2	6–35
MW4IC915MBR1	6–43
MW4IC915GMBR1	6–43
MWIC930R1	6–53
MWIC930GR1	6–53
General Purpose Linear Amplifier Modules	
MHW1345	6–61

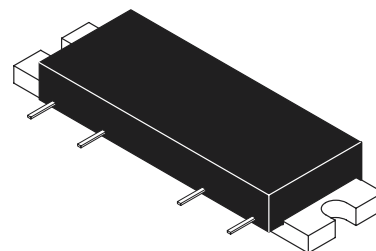
The RF Line Cellular Band RF Linear LDMOS Amplifiers

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA, CDMA or QPSK.

- Third Order Intercept: 47 dBm Typ
- Power Gain: 30.5 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA, CDMA, QPSK or Analog Systems

**MHL9236
MHL9236M**

**800–960 MHz
2.5 W, 30.5 dB
RF LINEAR LDMOS AMPLIFIERS**



CASE 301AP-02, STYLES 1, 2

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	30	Vdc
RF Input Power	P _{in}	+10	dBm
Storage Temperature Range	T _{stg}	–40 to +100	°C
Operating Case Temperature Range	T _C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 Vdc, T_C = 25°C; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I _{DD}	—	550	620	mA
Power Gain (f = 880 MHz)	G _p	29.5	30.5	31.5	dB
Gain Flatness (f = 800–960 MHz)	G _F	—	0.1	0.3	dB
Power Output @ 1 dB Comp. (f = 880 MHz)	P _{out} 1 dB	33.0	34.0	—	dBm
Input VSWR (f = 800–960 MHz)	VSWR _{in}	—	1.2:1	1.5:1	
Output VSWR (f = 800–960 MHz)	VSWR _{out}	—	1.2:1	1.5:1	
Third Order Intercept (f ₁ = 879 MHz, f ₂ = 884 MHz)	ITO	46.0	47.0	—	dBm
Noise Figure (f = 800–960 MHz)	NF	—	3.5	4.5	dB

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

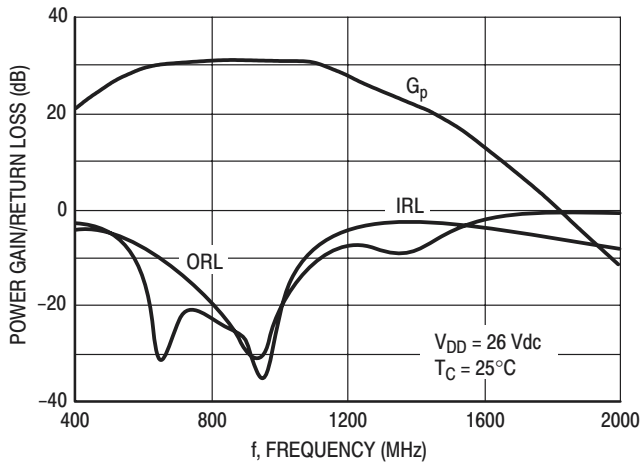


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

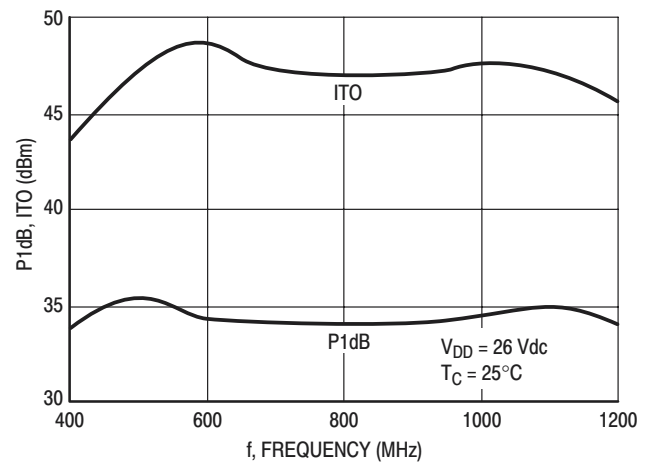


Figure 2. P1dB, ITO versus Frequency

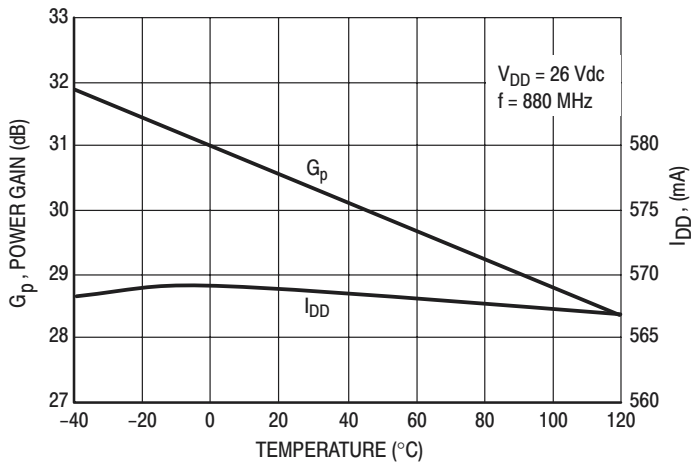


Figure 3. Power Gain, I_{DD} versus Temperature

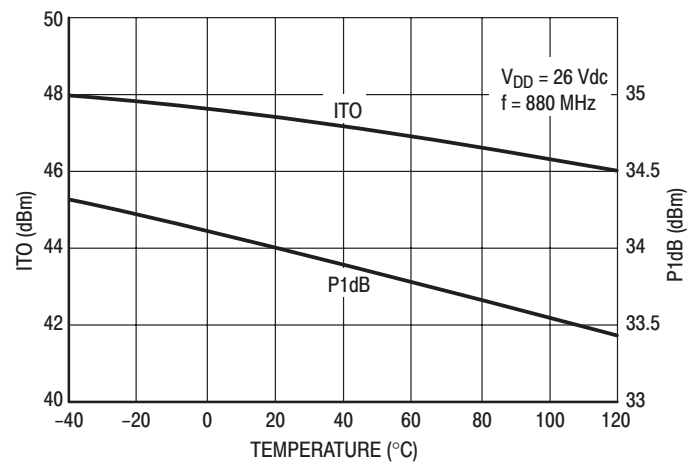


Figure 4. ITO, P1dB versus Temperature

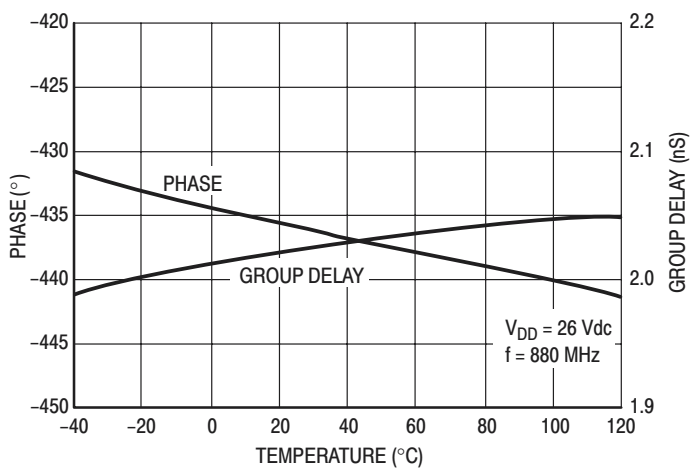


Figure 5. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Temperature

⁽¹⁾In Production Test Fixture

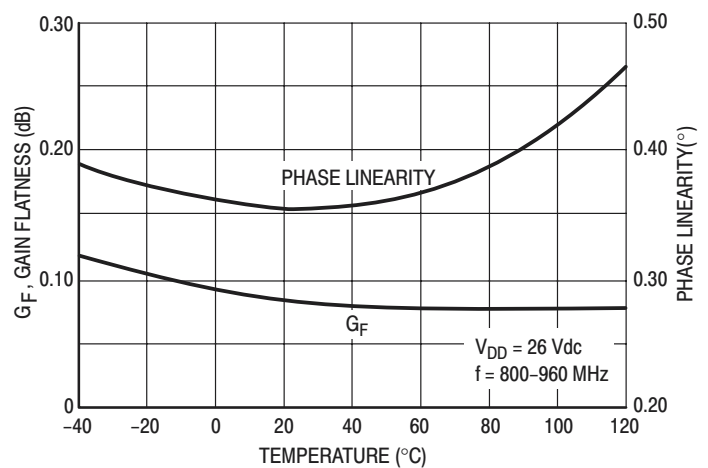


Figure 6. Gain Flatness, Phase Linearity versus Temperature

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

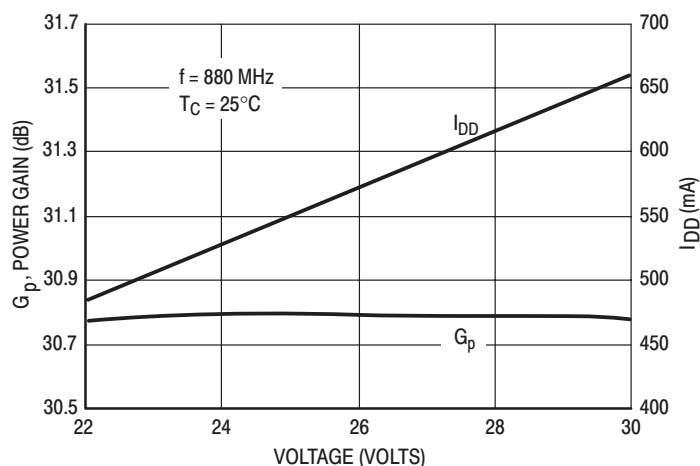


Figure 7. Power Gain, I_{DD} versus Voltage

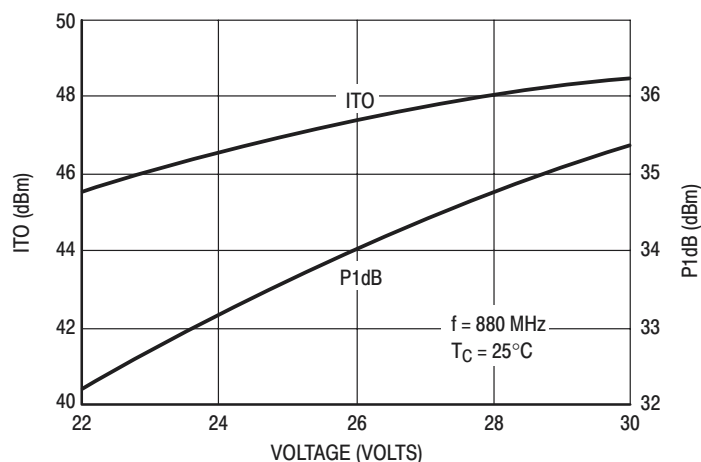


Figure 8. ITO, P1dB versus Voltage

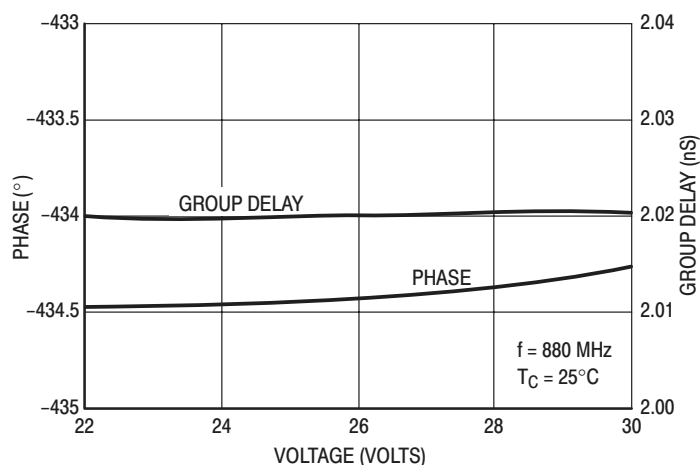


Figure 9. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Voltage

⁽¹⁾In Production Test Fixture

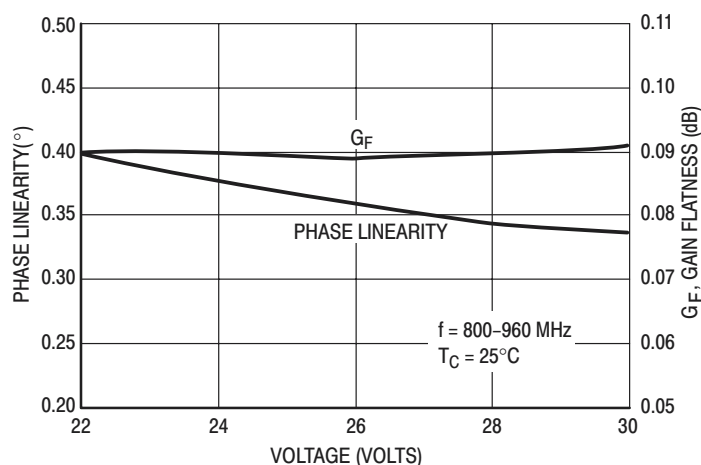


Figure 10. Phase Linearity, Gain Flatness versus Voltage

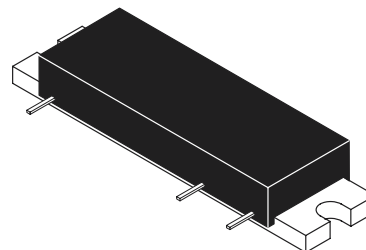
The RF Line Cellular Band RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 49 dBm Typ
- Power Gain: 17.5 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA and CDMA Multi-Carrier Applications

MHL9318

**3.0 W, 17.5 dB
860–900 MHz
RF LINEAR LDMOS AMPLIFIER**



CASE 301AS-01, STYLE 1

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+20	dBm
Storage Temperature Range	T_{stg}	–40 to +100	$^\circ\text{C}$
Operating Case Temperature Range	T_C	–20 to +100	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{DD} = 28 \text{ Vdc}$, $T_C = 25^\circ\text{C}$; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{DD}	—	500	560	mA
Power Gain (f = 880 MHz)	G_p	17	17.5	18.5	dB
Gain Flatness (f = 860–900 MHz)	G_F	—	0.1	0.2	dB
Power Output @ 1 dB Comp. (f = 880 MHz)	$P_{out \text{ 1 dB}}$	—	35.5	—	dBm
Input VSWR (f = 860–900 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR (f = 860–900 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)	ITO	47	49	—	dBm
Noise Figure (f = 960 MHz)	NF	—	3	4.5	dB

Freescale Semiconductor, Inc.

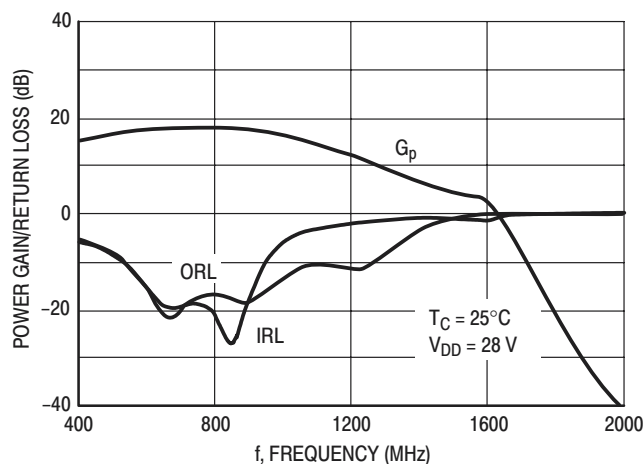


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

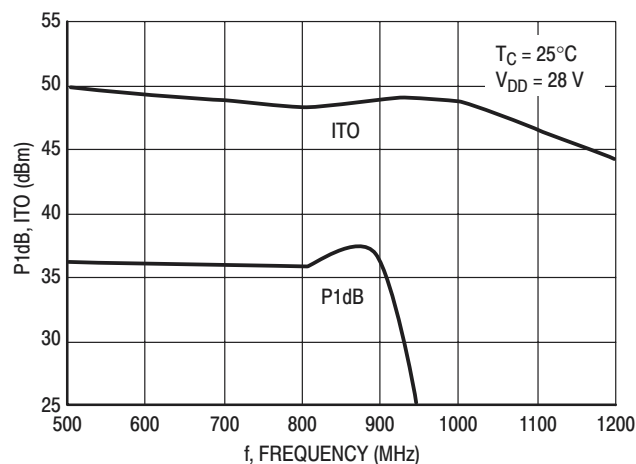


Figure 2. P1dB, ITO versus Frequency

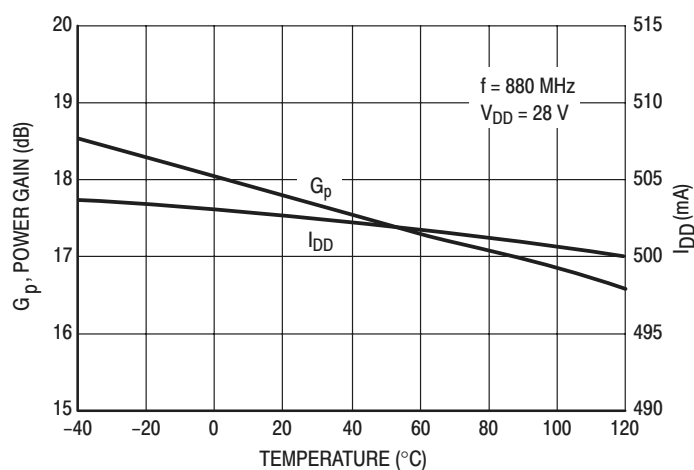


Figure 3. Power Gain, I_{DD} versus Temperature

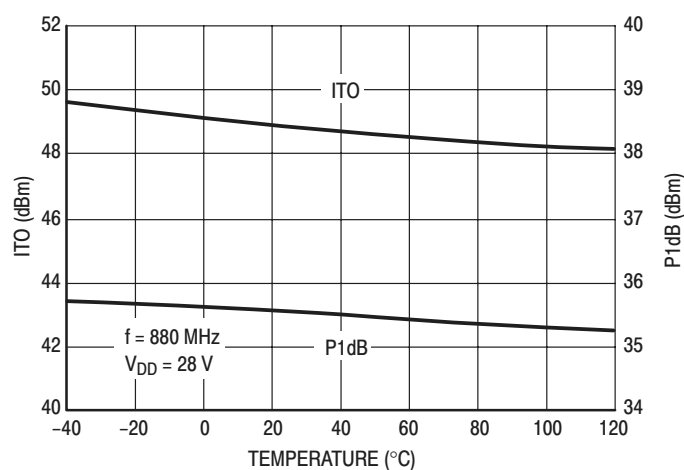


Figure 4. ITO, P1dB versus Temperature

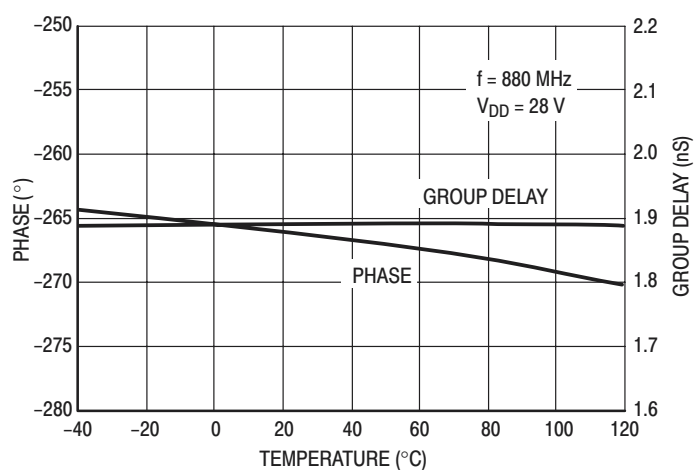


Figure 5. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Temperature
(¹)In Production Test Fixture

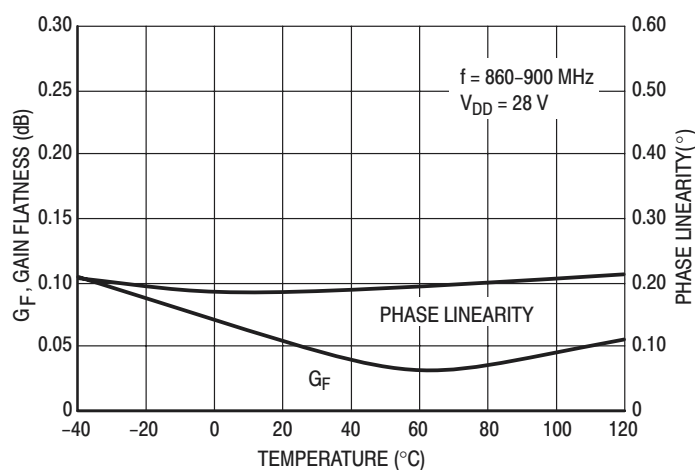


Figure 6. Gain Flatness, Phase Linearity versus Temperature

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

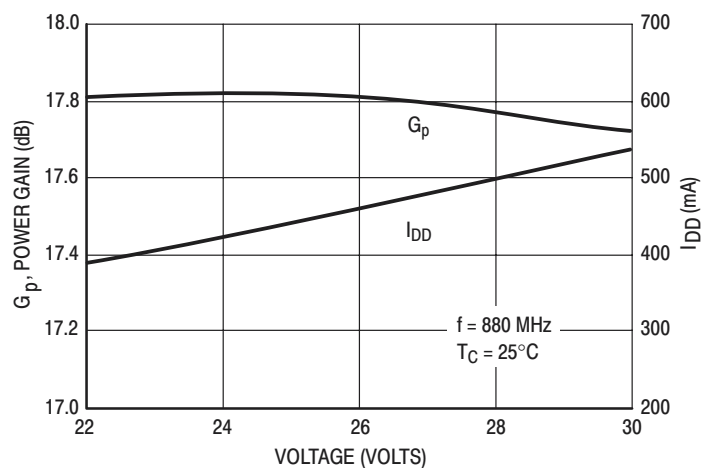


Figure 7. Power Gain, I_{DD} versus Voltage

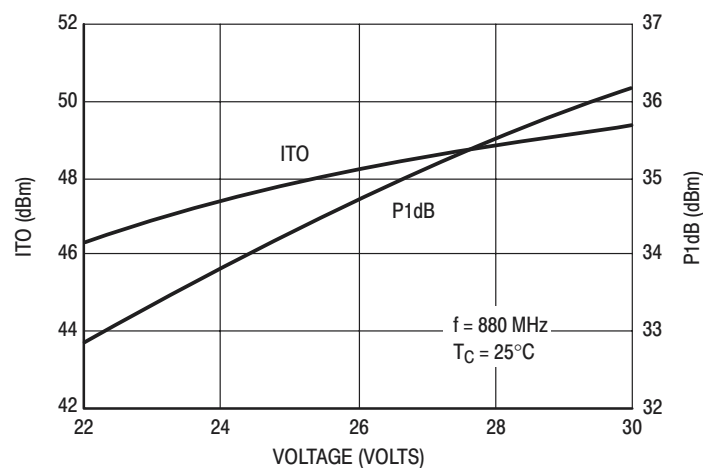


Figure 8. ITO, P1dB versus Voltage

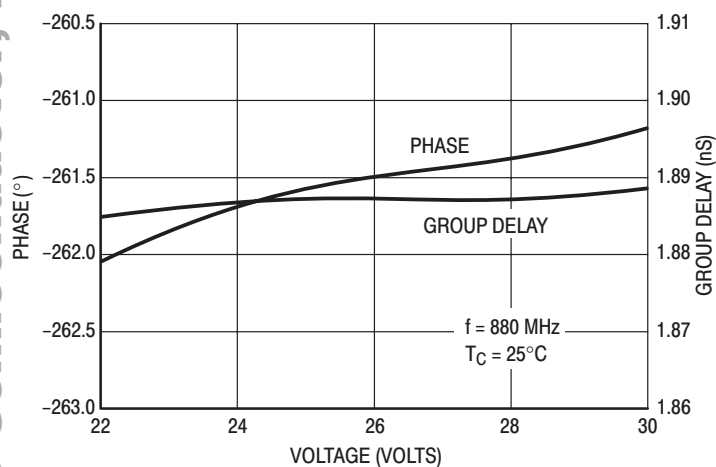


Figure 9. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Voltage
(¹)In Production Test Fixture

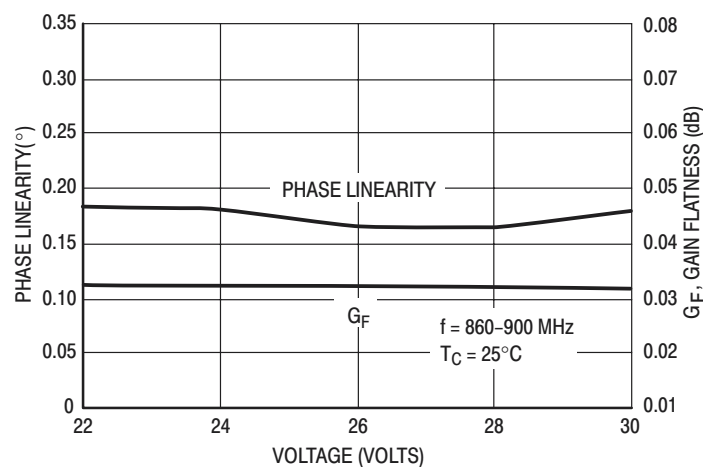


Figure 10. Phase Linearity, Gain Flatness versus Voltage

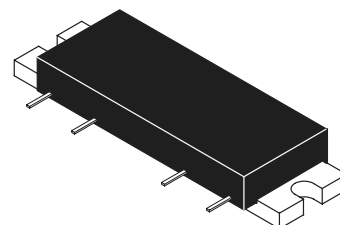
The RF Line Cellular Band RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 50 dBm Typ
- Power Gain: 31 dB Typ (@ $f = 880$ MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA and CDMA Multi-Carrier Applications

MHL9838

**800–925 MHz
8.0 W, 31 dB
RF LINEAR LDMOS AMPLIFIER**



CASE 301AP-02, STYLE 1

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+6	dBm
Storage Temperature Range	T_{stg}	–40 to +100	$^\circ\text{C}$
Operating Case Temperature Range	T_C	–20 to +100	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{DD} = 28$ Vdc, $T_C = 25^\circ\text{C}$; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{DD}	—	770	800	mA
Power Gain (f = 880 MHz)	G_p	30	31	32	dB
Gain Flatness (f = 800–925 MHz)	G_F	—	0.1	0.3	dB
Power Output @ 1 dB Comp. (f = 880 MHz)	$P_{out\ 1\ dB}$	—	39	—	dBm
Input VSWR (f = 800–925 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR (f = 800–925 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)	ITO	49	50	—	dBm
Noise Figure (f = 925 MHz)	NF	—	3.7	4.5	dB

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

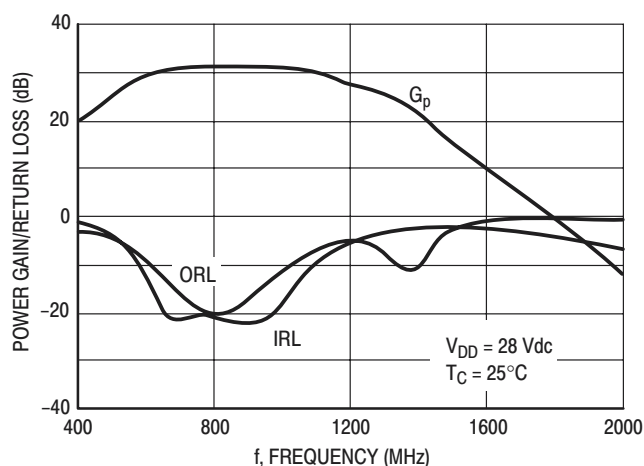


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

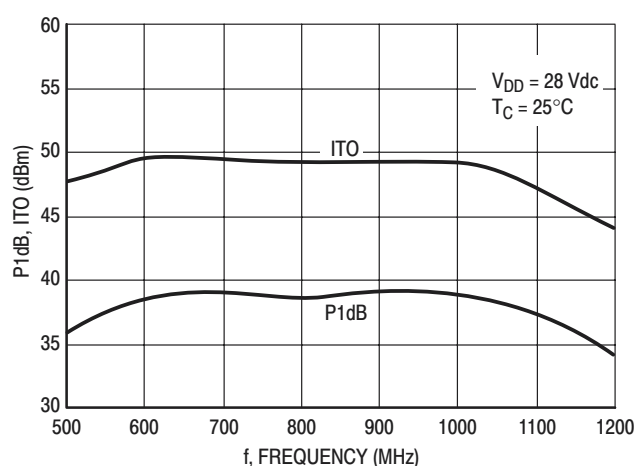


Figure 2. P1dB, ITO versus Frequency

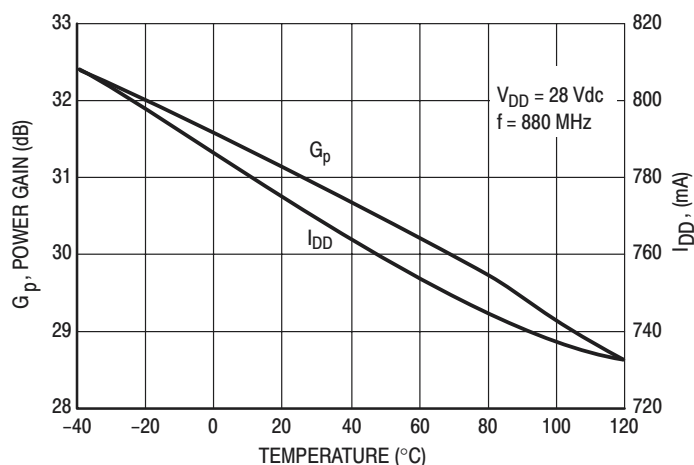


Figure 3. Power Gain, I_{DD} versus Temperature

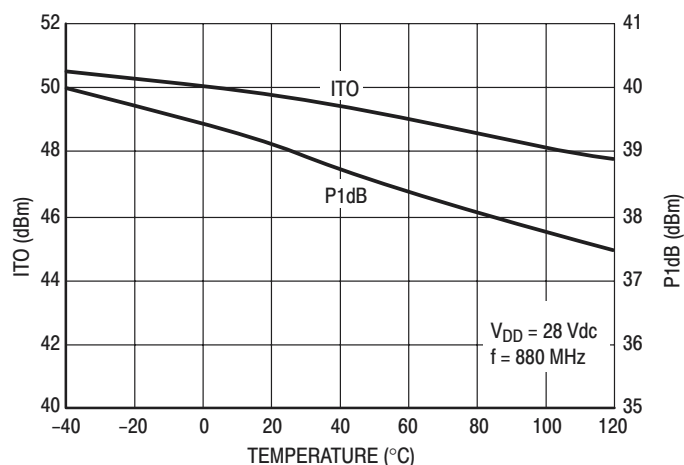


Figure 4. ITO, P1dB versus Temperature

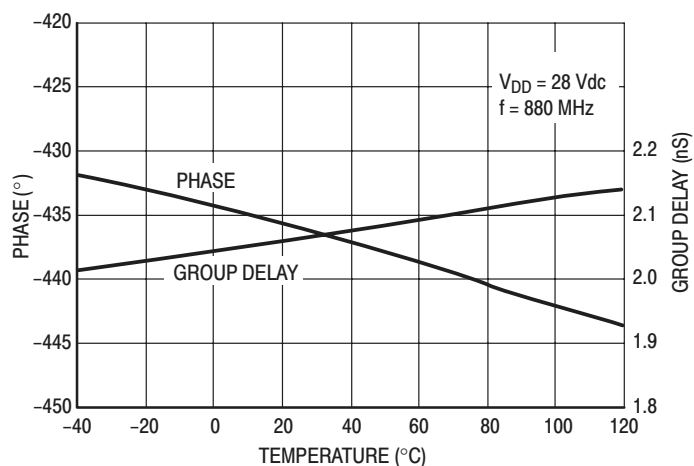


Figure 5. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Temperature

⁽¹⁾In Production Test Fixture

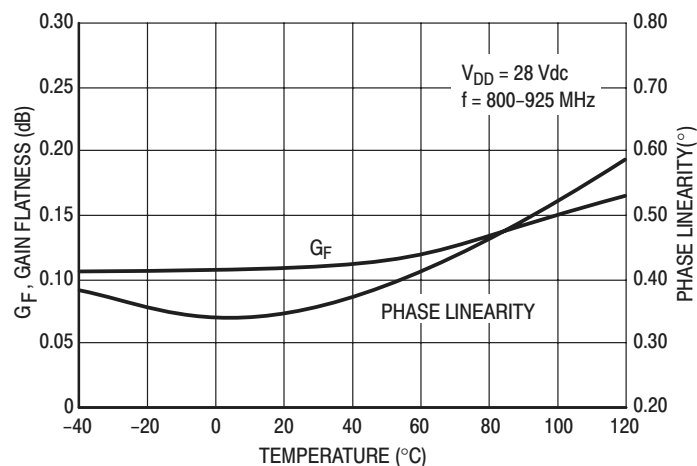


Figure 6. Gain Flatness, Phase Linearity versus Temperature

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

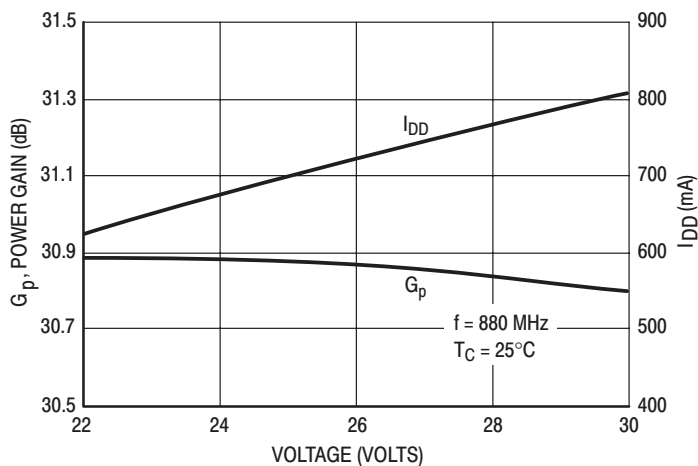


Figure 7. Power Gain, I_{DD} versus Voltage

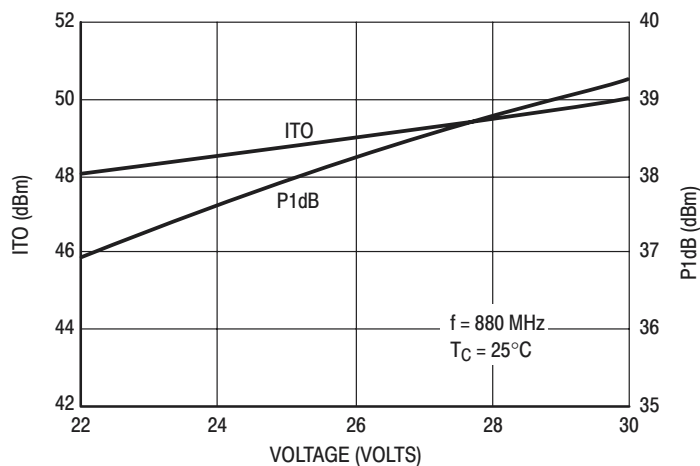


Figure 8. ITO, P1dB versus Voltage

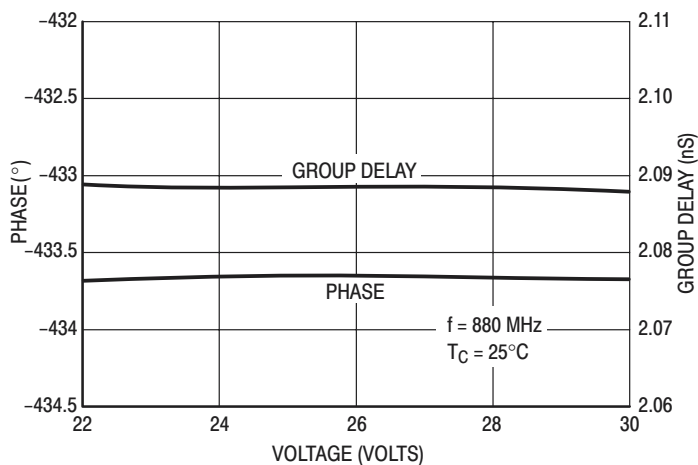


Figure 9. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Voltage

⁽¹⁾In Production Test Fixture

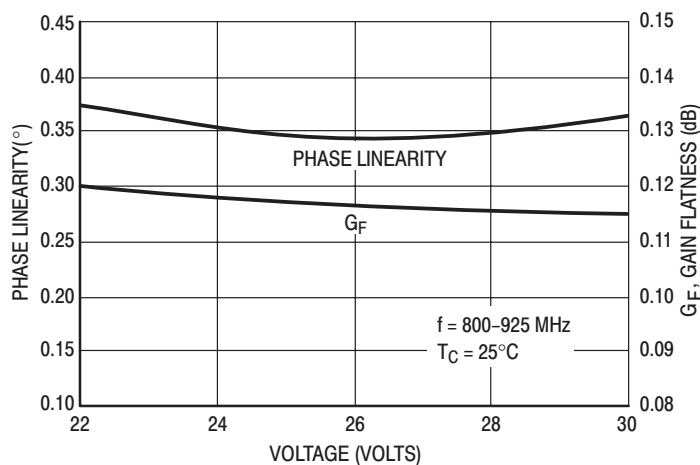


Figure 10. Phase Linearity, Gain Flatness versus Voltage

The RF Line

PCS Band

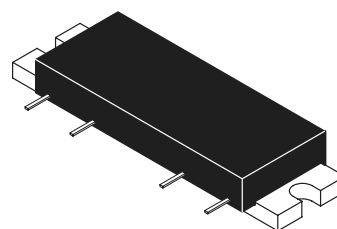
RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 46 dBm Typ
- Power Gain: 30 dB Typ (@ f = 1850 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

MHL18336

1800–1900 MHz
4 W, 30 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AP-02, STYLE 1

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+10	dBm
Storage Temperature Range	T_{stg}	-40 to +100	$^\circ\text{C}$
Operating Case Temperature Range	T_C	-20 to +100	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{DD} = 26\text{ Vdc}$, $T_C = 25^\circ\text{C}$; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{DD}	—	500	525	mA
Power Gain (f = 1850 MHz)	G_p	29	30	31	dB
Gain Flatness (f = 1800–1900 MHz)	G_F	—	0.2	0.4	dB
Power Output @ 1 dB Comp. (f = 1850 MHz)	$P_{out\ 1\ dB}$	35	36	—	dBm
Input VSWR (f = 1800–1900 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 1847 MHz, f2 = 1852 MHz)	ITO	45	46	—	dBm
Noise Figure (f = 1850 MHz)	NF	—	4.2	4.5	dB

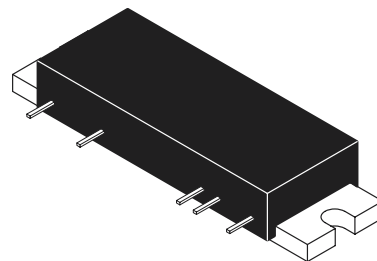
The RF Line PCS Band RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 Ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA, EDGE and CDMA.

- Third Order Intercept Point: 50 dBm Typ
- Power Gain: 28.6 dB Typ (@ f = 1842 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Application

MHL18926

**1805–1880 MHz, 10 W, 28.6 dB
RF LINEAR LDMOS AMPLIFIER**



CASE 301AY-01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	30	Vdc
RF Input Power	P _{in}	+7	dBm
Storage Temperature Range	T _{stg}	–40 to +100	°C
Operating Case Temperature Range	T _C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C; V_{DD} = 26 Vdc; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I _{DD}	—	1.1	1.15	A
Power Gain (f = 1842 MHz)	G _p	27.6	28.6	29.6	dB
Gain Flatness (f = 1805–1880 MHz)	G _F	—	0.3	0.5	dB
Power Output @ 1 dB Compression (f = 1842 MHz)	P1 dB	39	40	—	dBm
Input VSWR (f = 1805–1880 MHz)	VSWR _{in}	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 1839 MHz, f2 = 1844 MHz)	ITO	49.5	50	—	dBm
Noise Figure (f = 1880 MHz)	NF	—	4.2	5	dB

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

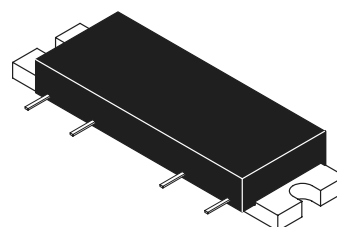
The RF Line PCS Band RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 46 dBm Typ
- Power Gain: 30 dB Typ (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

MHL19338

**1900–2000 MHz
4.0 W, 30 dB
RF LINEAR LDMOS AMPLIFIER**



CASE 301AP-02, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	30	Vdc
RF Input Power	P _{in}	+10	dBm
Storage Temperature Range	T _{stg}	–40 to +100	°C
Operating Case Temperature Range	T _C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 28 Vdc, T_C = 25°C; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I _{DD}	—	500	525	mA
Power Gain (f = 1960 MHz)	G _p	29	30	31	dB
Gain Flatness (f = 1900–2000 MHz)	G _F	—	0.1	0.4	dB
Power Output @ 1 dB Comp. (f = 1950 MHz)	P _{out} 1 dB	35	36	—	dBm
Input VSWR (f = 1900–2000 MHz)	VSWR _{in}	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 1950 MHz, f2 = 1955 MHz)	ITO	45	46	—	dBm
Noise Figure (f = 2000 MHz)	NF	—	4.2	4.5	dB

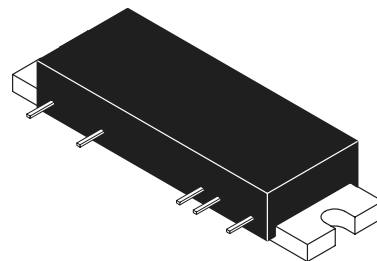
The RF Line PCS Band RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 Ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA, EDGE and CDMA.

- Third Order Intercept Point: 50 dBm Typ
- Power Gain: 29.4 dB Typ (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Application

MHL19926

**1930–1990 MHz, 10 W, 29.4 dB
RF LINEAR LDMOS AMPLIFIER**



CASE 301AY-01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	30	Vdc
RF Input Power	P _{in}	+7	dBm
Storage Temperature Range	T _{stg}	–40 to +100	°C
Operating Case Temperature Range	T _C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C; V_{DD} = 26 Vdc; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I _{DD}	—	1	1.05	A
Power Gain (f = 1960 MHz)	G _p	28.4	29.4	30.4	dB
Gain Flatness (f = 1930–1990 MHz)	G _F	—	0.3	0.5	dB
Power Output @ 1 dB Compression (f = 1960 MHz)	P1 dB	39	40	—	dBm
Input VSWR (f = 1930–1990 MHz)	VSWR _{in}	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 1957 MHz, f2 = 1962 MHz)	ITO	49.5	50	—	dBm
Noise Figure (f = 1990 MHz)	NF	—	4.2	5	dB

NOTE – CAUTION – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

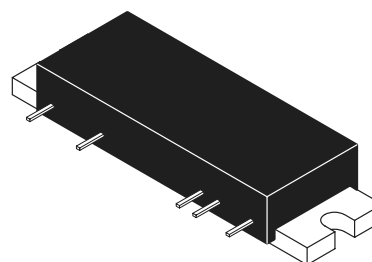
The RF Line PCS Band RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 49.5 dBm Typ
- Power Gain: 29 dB Typ (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

MHL19936

**1900–2000 MHz
12 W, 29 dB
RF LINEAR LDMOS AMPLIFIER**



CASE 301AY-01, STYLE 1

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+10	dBm
Storage Temperature Range	T_{stg}	–40 to +100	$^\circ\text{C}$
Operating Case Temperature Range	T_C	–20 to +100	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{DD} = 26\text{ Vdc}$, $T_C = 25^\circ\text{C}$; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{DD}	—	1.4	1.45	A
Power Gain (f = 1960 MHz)	G_p	28	29	30	dB
Gain Flatness (f = 1900–2000 MHz)	G_F	—	0.2	0.4	dB
Power Output @ 1 dB Comp. (f = 1950 MHz)	P_{1dB}	40	41	—	dBm
Input VSWR (f = 1900–2000 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 1950 MHz, f2 = 1955 MHz)	ITO	49	49.5	—	dBm
Noise Figure (f = 2000 MHz)	NF	—	4.2	4.5	dB

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

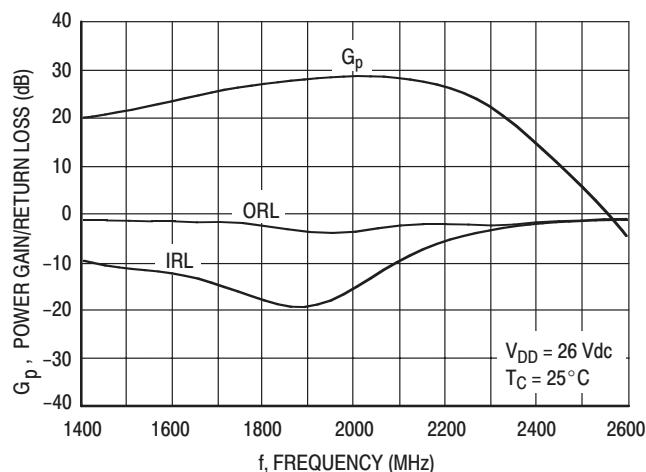


Figure 11. Power Gain, Input Return Loss, Output Return Loss versus Frequency

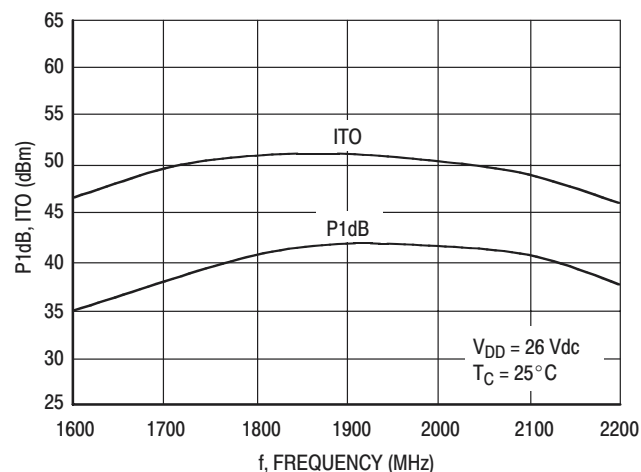


Figure 12. P1dB, ITO versus Frequency

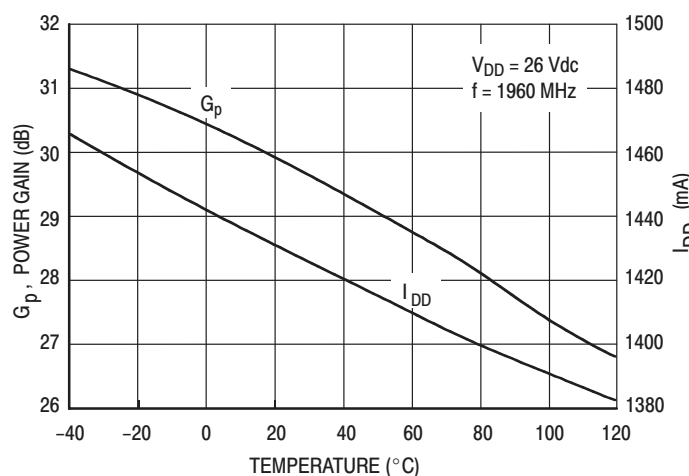


Figure 13. Power Gain, I_{DD} versus Temperature

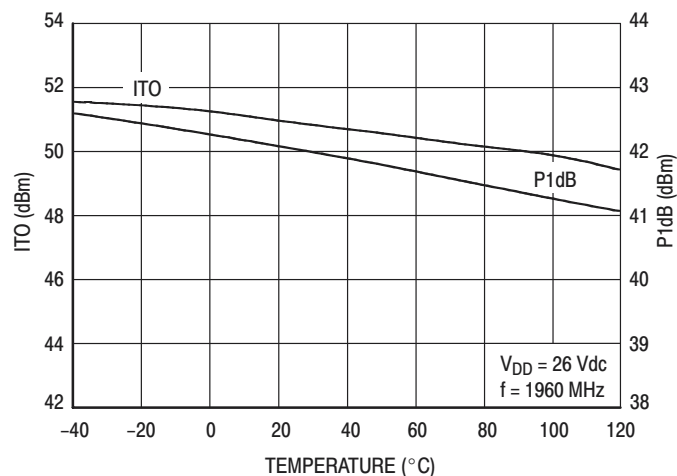


Figure 14. ITO, P1dB versus Temperature

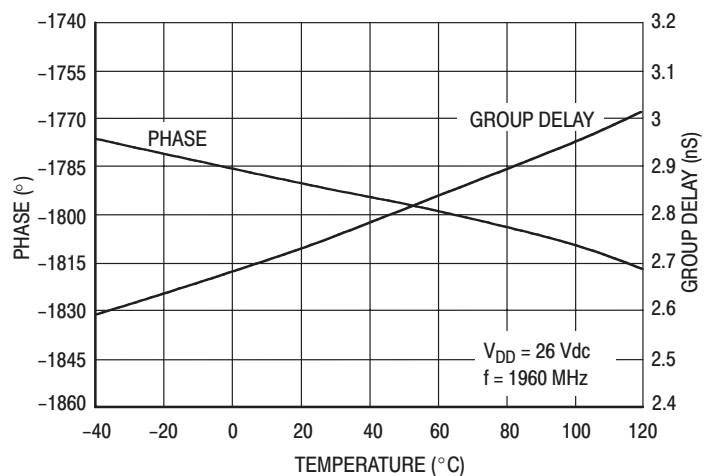


Figure 15. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Temperature
(¹)In Production Test Fixture

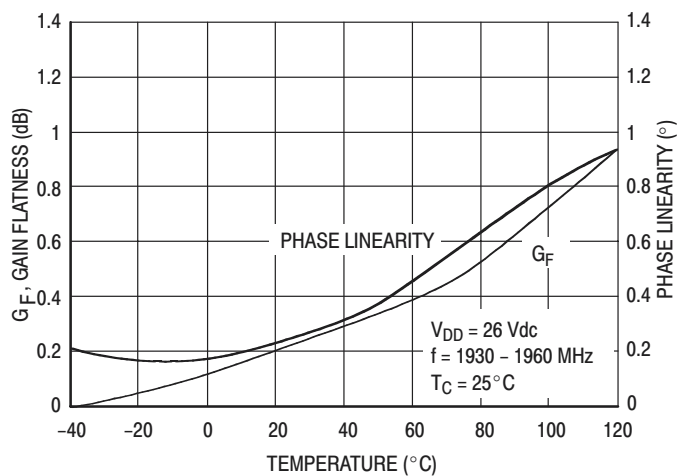


Figure 16. Gain Flatness, Phase Linearity versus Temperature

Freescale Semiconductor, Inc.

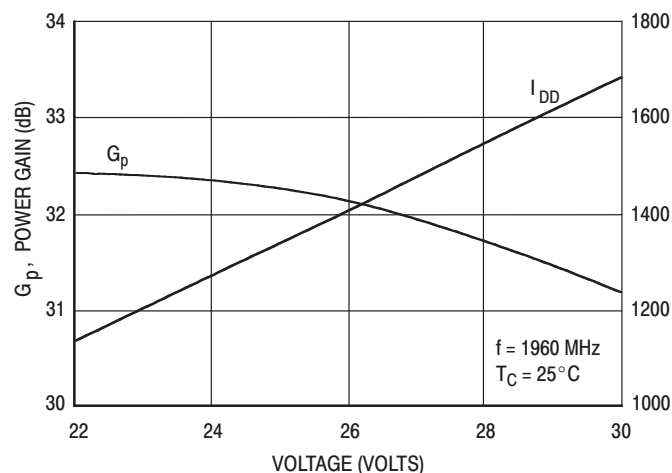


Figure 17. Power Gain, I_{DD} versus Voltage

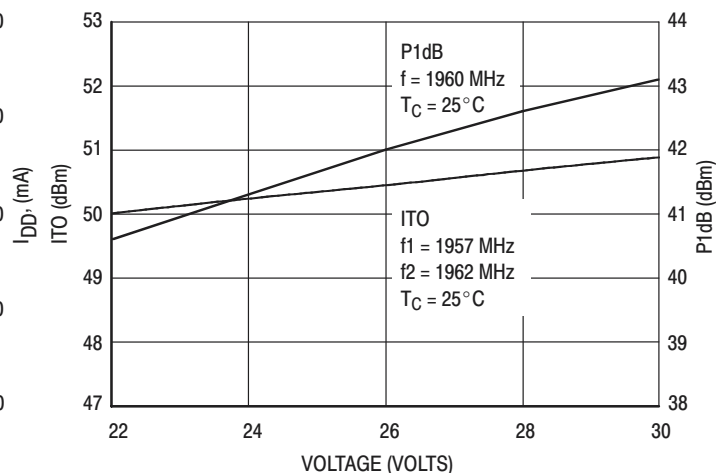


Figure 18. ITO, P1dB versus Voltage

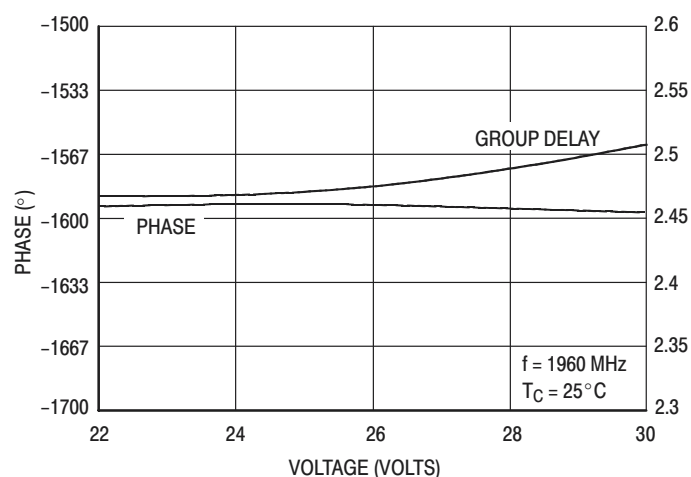


Figure 19. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Voltage

⁽¹⁾In Production Test Fixture

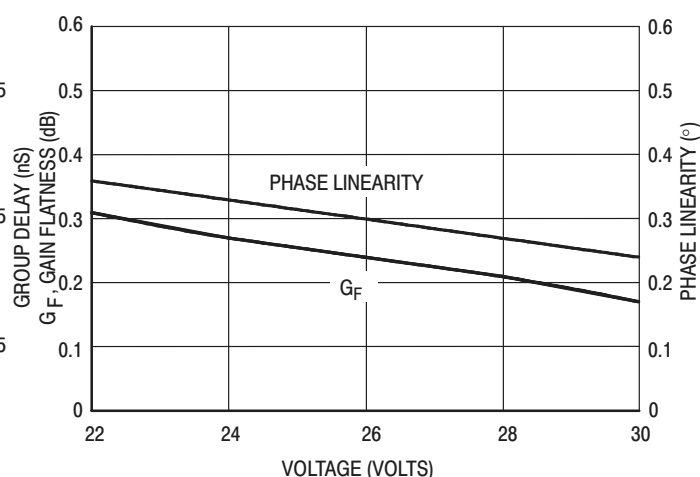


Figure 20. Phase Linearity, Gain Flatness versus Voltage

The RF Line

3G Band

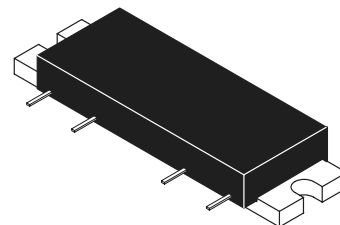
RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the 3G frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital CDMA modulation systems.

- Third Order Intercept: 45 dBm Typ
- Power Gain: 31 dB Typ (@ f = 2140 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

MHL21336

2110–2170 MHz
3.0 W, 31 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AP-02, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	30	Vdc
RF Input Power	P _{in}	+5	dBm
Storage Temperature Range	T _{stg}	–40 to +100	°C
Operating Case Temperature Range	T _C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 Vdc, T_C = 25°C; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I _{DD}	—	500	525	mA
Power Gain (f = 2140 MHz)	G _p	30	31	32	dB
Gain Flatness (f = 2110–2170 MHz)	G _F	—	0.15	0.4	dB
Power Output @ 1 dB Comp. (f = 2140 MHz)	P _{out} 1 dB	34	35	—	dBm
Input VSWR (f = 2110–2170 MHz)	VSWR _{in}	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 2137 MHz, f2 = 2142 MHz)	ITO	44	45	—	dBm
Noise Figure (f = 2170 MHz)	NF	—	4.5	5	dB

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

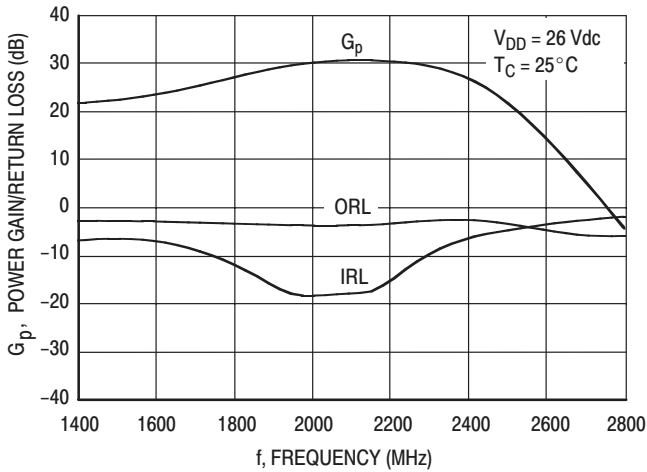


Figure 21. Power Gain, Input Return Loss, Output Return Loss versus Frequency

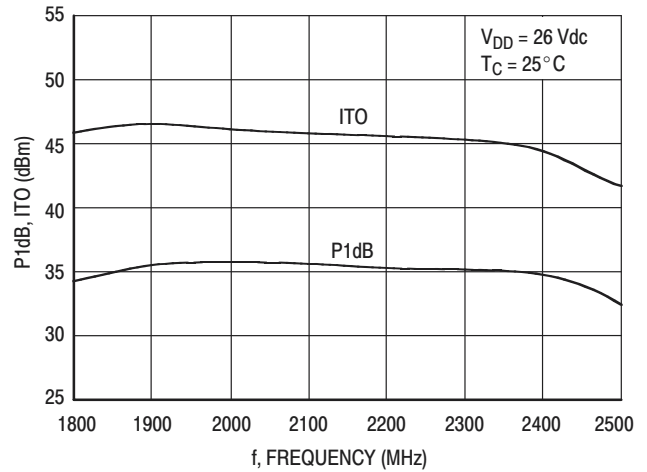


Figure 22. P1dB, ITO versus Frequency

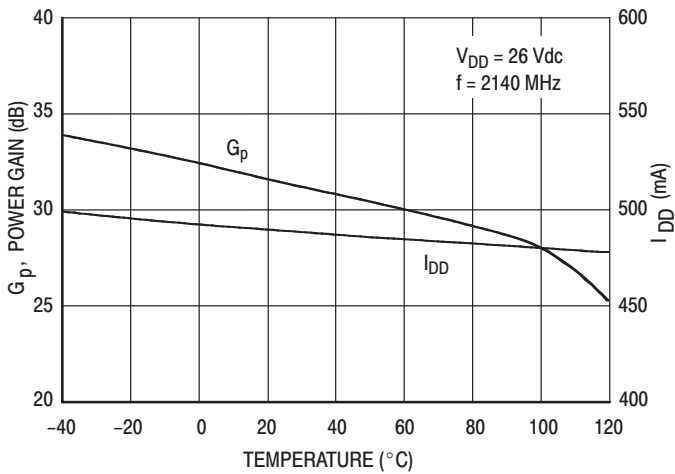


Figure 23. Power Gain, I_{DD} versus Temperature

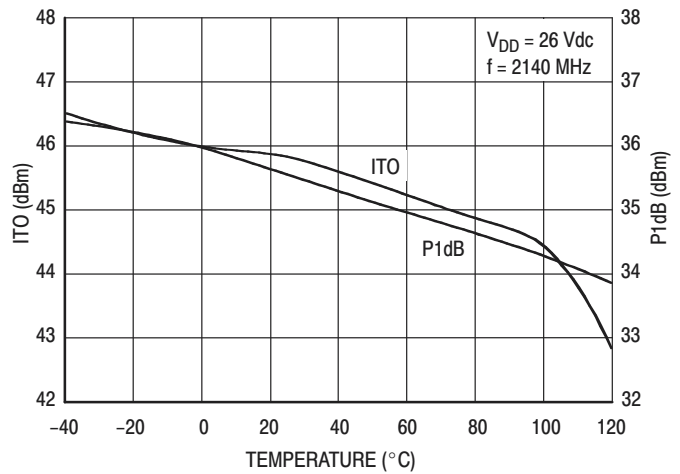


Figure 24. ITO, P1dB versus Temperature

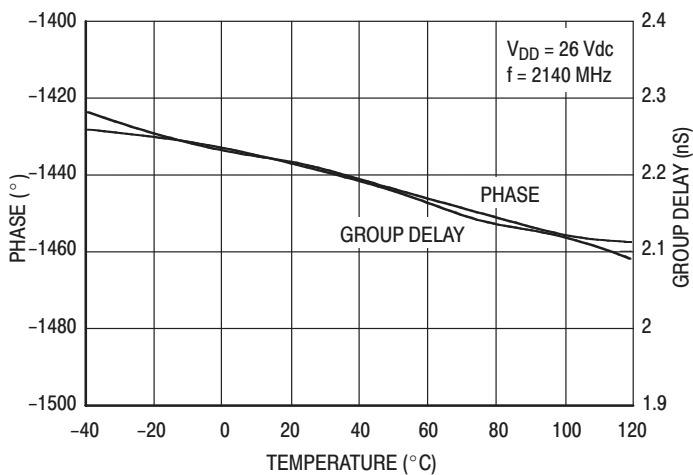


Figure 25. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Temperature

⁽¹⁾In Production Test Fixture

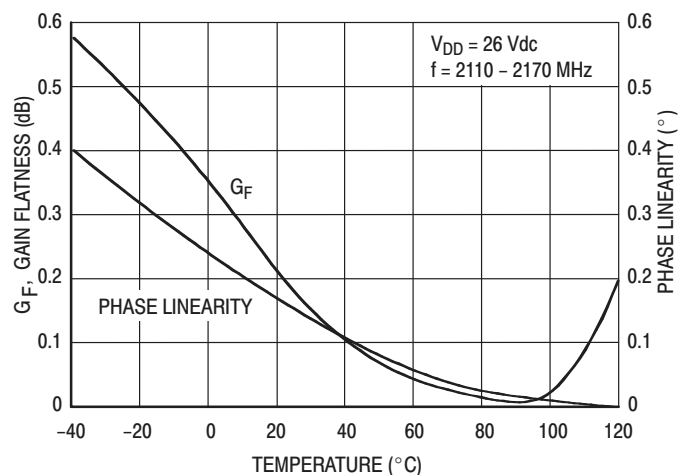


Figure 26. Gain Flatness, Phase Linearity versus Temperature

Freescale Semiconductor, Inc.

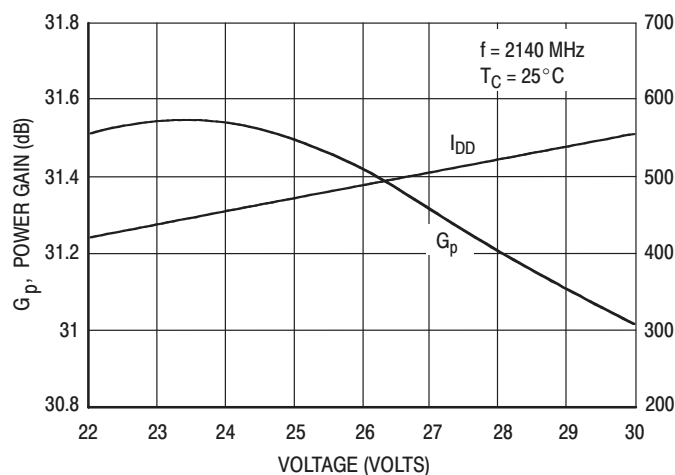


Figure 27. Power Gain, I_{DD} versus Voltage

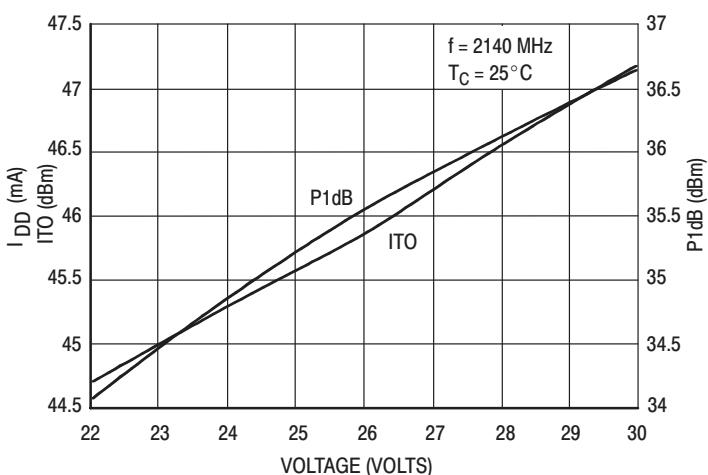


Figure 28. ITO, P1dB versus Voltage

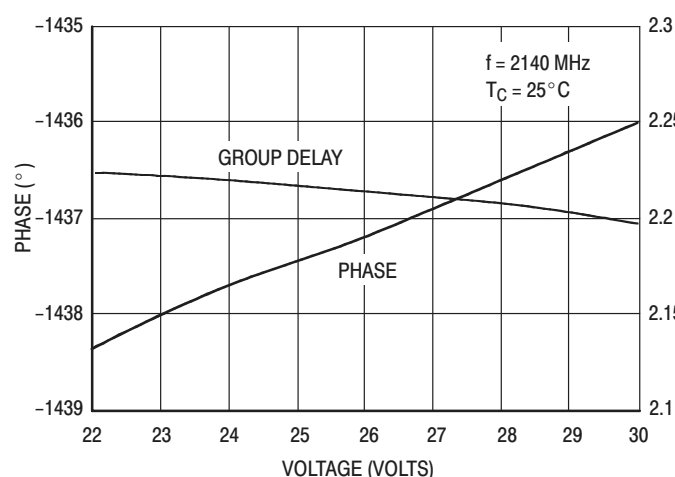


Figure 29. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Voltage

⁽¹⁾In Production Test Fixture

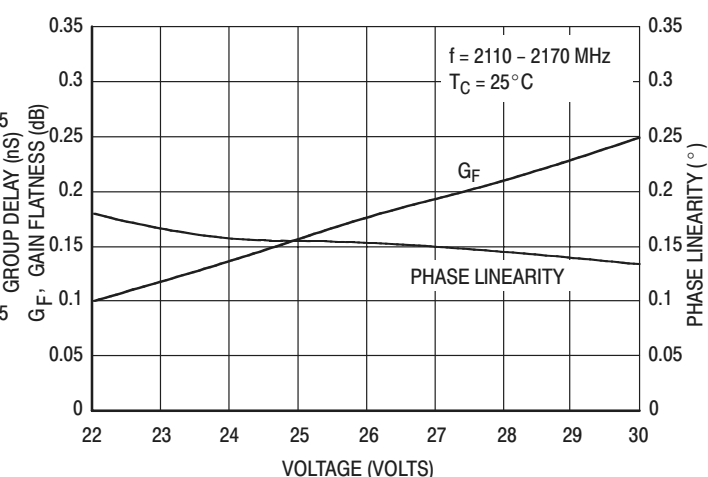


Figure 30. Phase Linearity, Gain Flatness versus Voltage

The RF Line

PCS Band

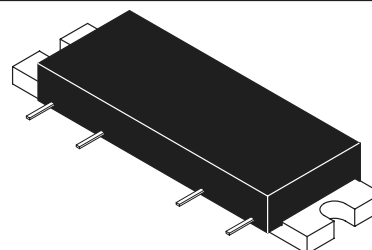
RF Linear LDMOS Amplifier

Designed for Class AB amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Typical CDMA Performance: 1960 MHz, 28 Volts
IS-95 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
- Adjacent Channel Power: -51 dBc @ 30 dBm, 885 kHz Channel Spacing
- Power Gain: 24.5 dB Min (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- 0.2 dB Typical Gain Flatness
- Ideal for Feedforward Base Station Applications

MHPA19010

1930–1990 MHz
10 W, 24.5 dB
RF HIGH POWER LDMOS AMPLIFIER



CASE 301AP-02, STYLE 3

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power (Single Carrier CW)	P_{in}	+20	dBm
Storage Temperature Range	T_{stg}	-40 to +100	$^\circ\text{C}$
Operating Case Temperature Range	T_C	-20 to +100	$^\circ\text{C}$
Quiescent Bias Current	I_{DQ}	750	mA

ELECTRICAL CHARACTERISTICS ($V_{DD} = 28\text{ Vdc}$, $V_{BIAS} \cong 8\text{ V}$ Set for Supply Current of 600 mA, $T_C = 25^\circ\text{C}$, 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{DD}	—	600	—	mA
Power Gain (f = 1960 MHz)	G_p	24.5	25	—	dB
Gain Flatness (f = 1930–1990 MHz)	G_F	—	0.2	0.5	dB
Power Output @ 1 dB Comp. (f = 1960 MHz)	P_{1dB}	—	41.5	—	dBm
Input VSWR (f = 1930–1990 MHz)	$VSWR_{in}$	—	1.5:1	2:1	
Noise Figure (f = 1960 MHz)	NF	—	8	10	dB
Adjacent Channel Power Rejection @ 30 dBm, 1.23 MHz BW, 885 kHz Channel Spacing	ACPR	—	-58	-51	dBc

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

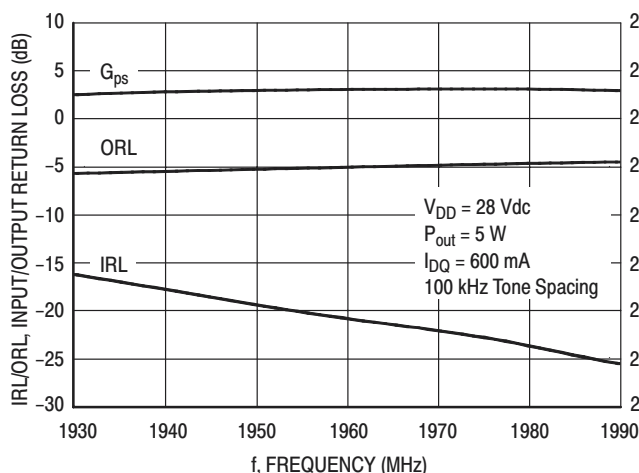


Figure 31. Two-Tone Power Gain, Input Return Loss and Output Return Loss versus Frequency

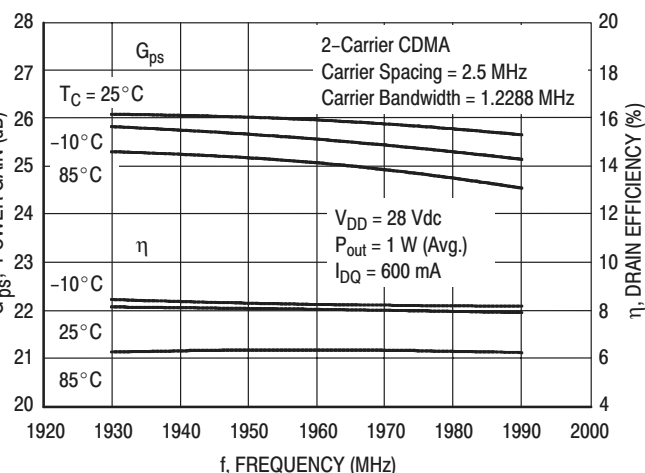


Figure 32. 2-Carrier CDMA Power Gain and Efficiency versus Frequency

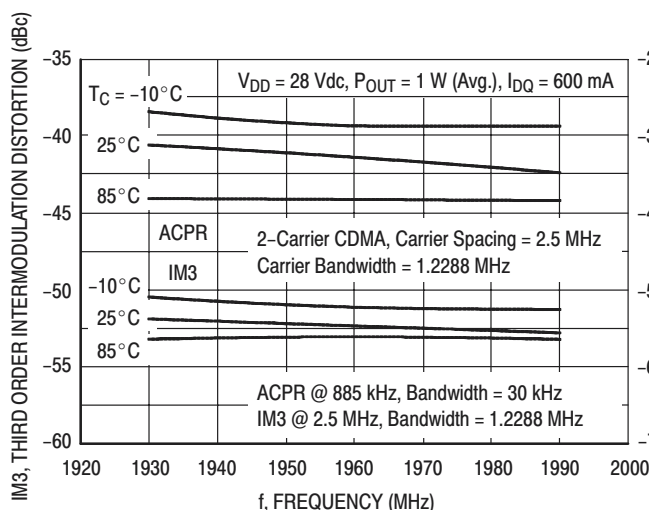


Figure 33. 2-Carrier CDMA IM3 and ACPR versus Frequency

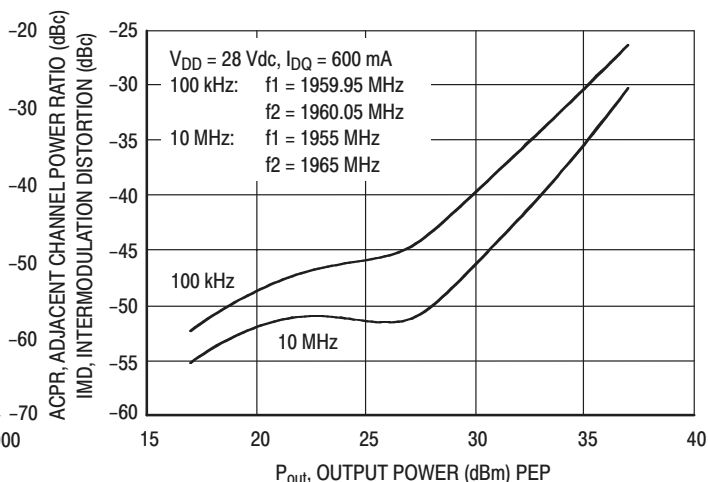


Figure 34. Two-Tone CDMA IMD versus Output Power

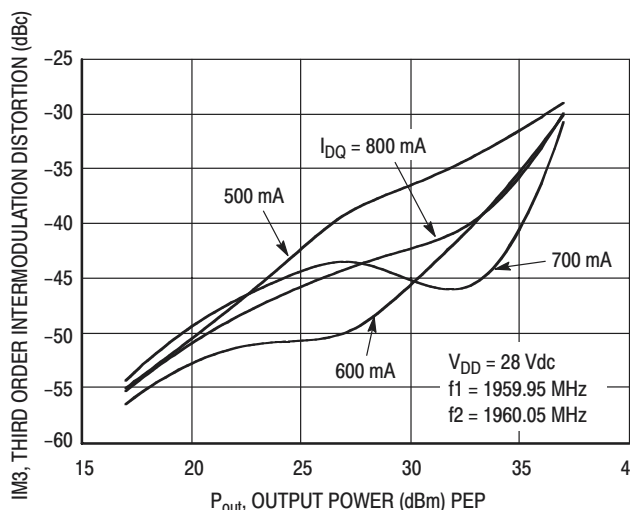


Figure 35. Third Order Intermodulation Distortion versus Output Power

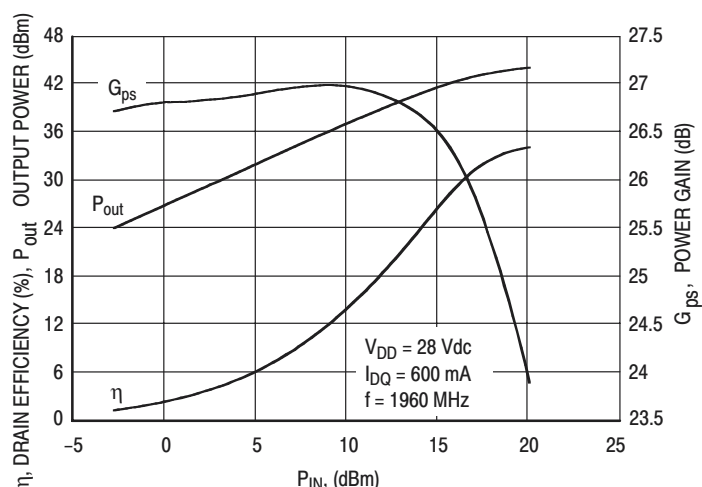


Figure 36. CW Output Power, Efficiency and Gain versus Input Power

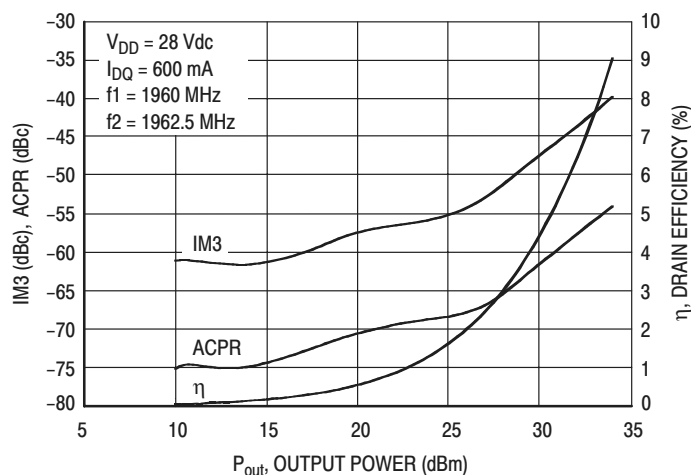


Figure 37. 2-Carrier CDMA ACPR, IM3 and Efficiency versus Output Power

NOTE: V_{DD} (Pin 3) should always be applied before V_{BIAS} (Pin 2).

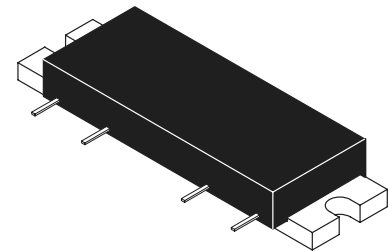
The RF Line UMTS Band RF Linear LDMOS Amplifier

Designed for Class AB amplifier applications in 50 ohm systems operating in the UMTS frequency band. A silicon FET design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems.

- Typical W-CDMA Performance for $V_{DD} = 28$ Volts, $V_{bias} = 8$ Volts, $I_{DQ} = 550$ mA, Channel Bandwidth = 3.84 MHz, Adjacent Channels at ± 5 MHz, ACPR Measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF, 3GPP Test Model 1, 64 DTCH.
- Adjacent Channel Power: -50 dBc @ 30 dBm, 5 MHz Channel Spacing
- Power Gain: 23.7 dB Min (@ $f = 2140$ MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- 0.2 dB Typical Gain Flatness
- Ideal for Feedforward Base Station Applications

MHPA21010

**2110–2170 MHz
10 W, 23.7 dB
RF HIGH POWER LDMOS AMPLIFIER**



CASE 301AP-02, STYLE 3

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power (Single Carrier CW)	P_{in}	+20	dBm
Storage Temperature Range	T_{stg}	-40 to $+100$	$^\circ\text{C}$
Operating Case Temperature Range	T_C	-20 to $+100$	$^\circ\text{C}$
Quiescent Bias Current	I_{DQ}	750	mA

ELECTRICAL CHARACTERISTICS ($V_{DD} = 28$ Vdc, $V_{BIAS} \cong 8$ V Set for Supply Current of 550 mA, $T_C = 25^\circ\text{C}$, 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{DD}	—	550	—	mA
Power Gain ($f = 2140$ MHz)	G_p	23.7	25	—	dB
Gain Flatness ($f = 2110$ – 2170 MHz)	G_F	—	0.2	0.6	dB
Power Output @ 1 dB Comp. ($f = 2140$ MHz)	P_{1dB}	—	41.5	—	dBm
Input VSWR ($f = 2110$ – 2170 MHz)	$VSWR_{in}$	—	1.5:1	2:1	
Noise Figure ($f = 2140$ MHz)	NF	—	—	10	dB
Adjacent Channel Power Rejection @ 30 dBm Avg., 3.84 MHz BW, 5 MHz Channel Spacing	ACPR	—	-55	-50	dBc

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

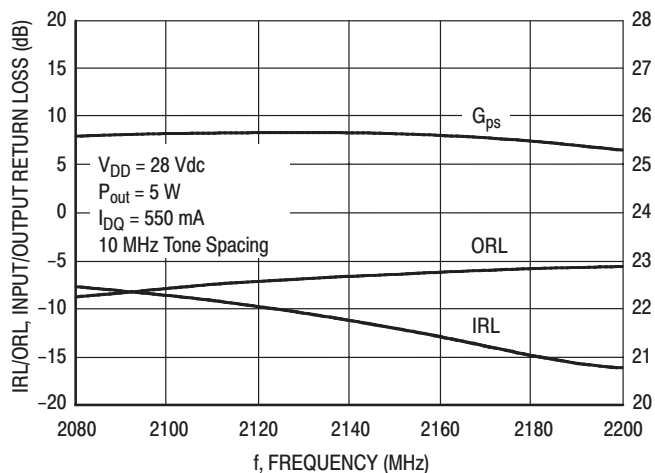


Figure 38. Two-Tone Power Gain, Input Return Loss and Output Return Loss versus Frequency

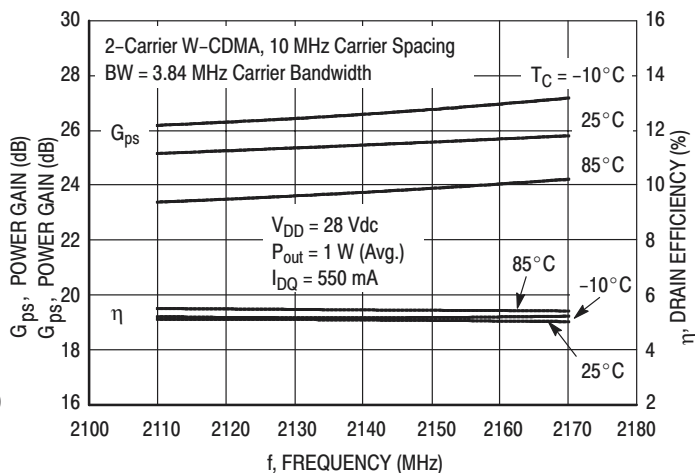


Figure 39. 2-Carrier W-CDMA Power Gain and Efficiency versus Frequency

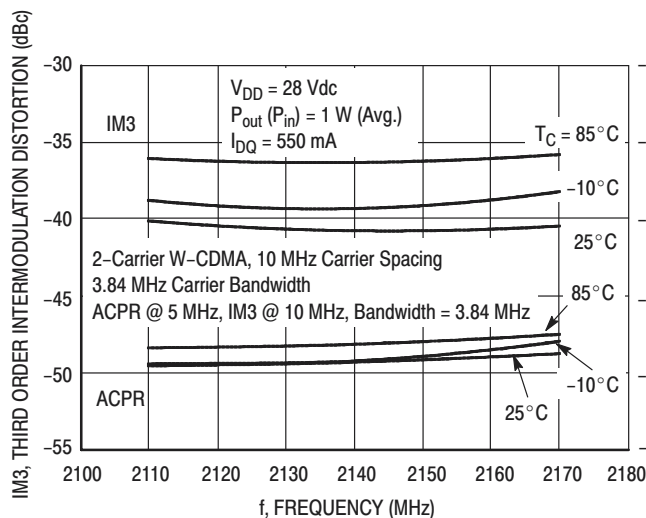


Figure 40. 2-Carrier W-CDMA IM3 and ACPR versus Frequency

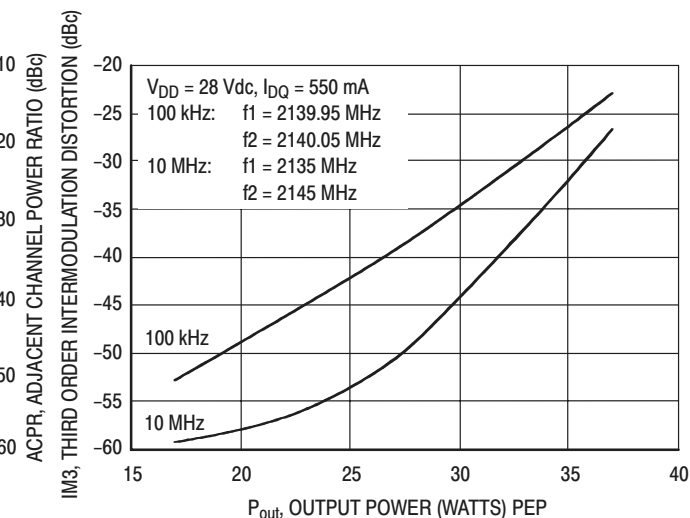


Figure 41. Two-Tone W-CDMA IM3 versus Output Power

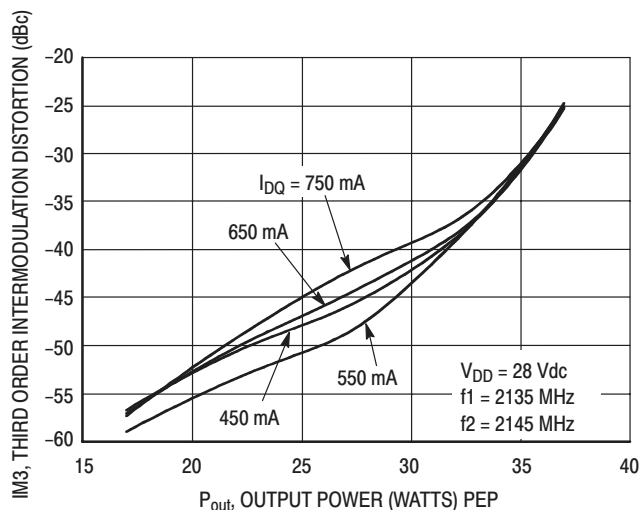


Figure 42. Third Order Intermodulation Distortion versus Output Power

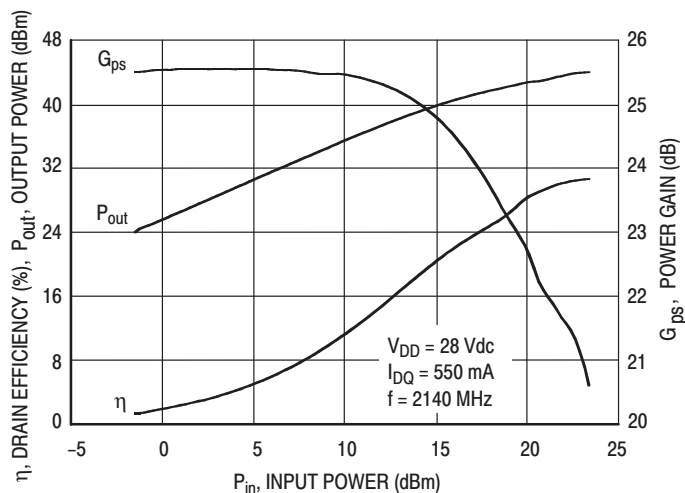


Figure 43. CW Output Power, Efficiency and Gain versus Input Power

Freescale Semiconductor, Inc.

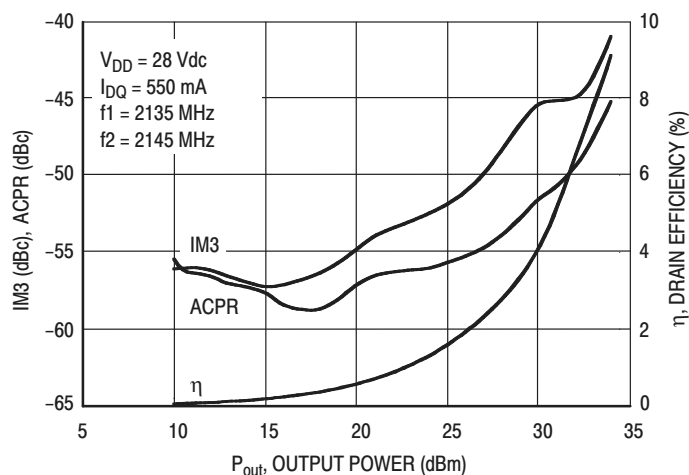


Figure 44. 2-Carrier W-CDMA ACPR, IM3 and Efficiency versus Output Power

NOTE: V_{DD} (Pin 3) should always be applied before V_{BIAS} (Pin 2).

The RF Line

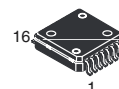
921 MHz - 960 MHz SiFET RF Integrated Power Amplifier

The MHVIC910HR2 integrated circuit is designed for GSM base stations, uses Motorola's newest High Voltage (26 Volts) LDMOS IC technology, and contains a three-stage amplifier. Target applications include macrocell (driver function) and microcell base stations (final stage). The device is packaged in a PFP-16 Power Flat Pack package which gives excellent thermal performances through a solderable backside contact.

- Typical GSM Performance @ Full Frequency Band (921 – 960 MHz), 26 Volts
Output Power – 40 dBm (CW) @ P1dB
Power Gain – 39 dB @ P1dB
Efficiency – 48% @ P1dB
- Integrated ESD Protection
- Usable Frequency Range – 921 to 960 MHz
- Available in Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

MHVIC910HR2

960 MHz, 10 W, 26 V
GSM CELLULAR
RF LDMOS INTEGRATED CIRCUIT



CASE 978-03
(PFP-16)

MAXIMUM RATINGS

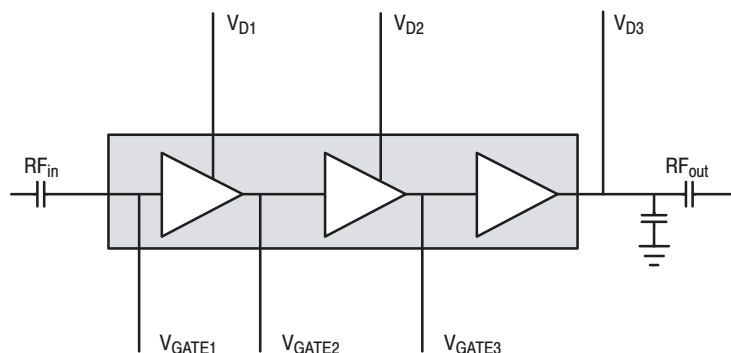
Rating	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	28	Vdc
Gate Supply Voltage	V_{GS}	6	Vdc
RF Input Power	P_{in}	5	dBm
Case Operating Temperature	T_C	– 30 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Operating Channel Temperature	T_{ch}	150	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	0 (Minimum)
Machine Model	M2 (Minimum)

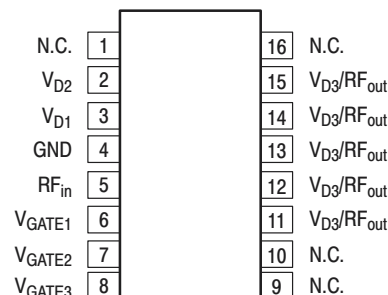
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.9	°C/W



Functional Block Diagram

PIN CONNECTIONS



(Top View)

NOTE: MHVIC910HR2 Moisture Sensitivity Level (MSL) = 3.

REV 3

MHVIC910HR2
6-28

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

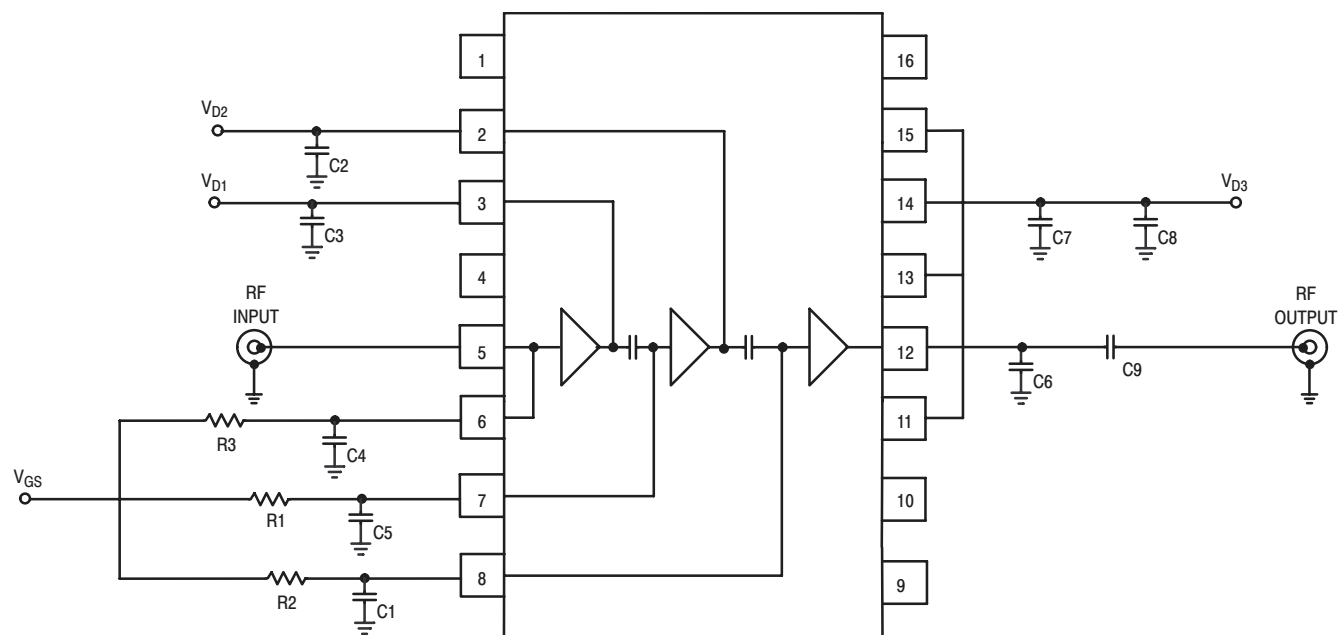
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	26	Vdc
3rd Stage Quiescent Current	I_{DQ3}	150	mA
2nd Stage Quiescent Current	I_{DQ2}	50	mA
1st Stage Quiescent Current	I_{DQ1}	25	mA

ELECTRICAL CHARACTERISTICS ($V_{DD} = 26$ V, V_{GS} set for $I_{DQ3} = 150$ mA, $T_A = 25^\circ\text{C}$ matched to a 50 Ω system, frequency range 921 – 960 MHz, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	f_{RF}	921	—	960	MHz
Output Power @ 1 dB Compression Point	P @ 1dB	39	40	—	dBm
Power Gain @ P1dB	G @ 1dB	38	39	—	dB
Power Added Efficiency @ 1 dB Compression Point	PAE @ 1dB	43	48	—	%
Input Return Loss @ P1dB	IRL @ 1dB	—	–15	–10	dB
Gain Flatness @ 40 dBm Variation ($T_C = -30$ to $+85^\circ\text{C}$ @ 40 dBm)	G_F G_V	— —	.5 5	— —	dB dB
Load Stability ($V_{DS} = 24$ V to 28 V, $P_{out} = \text{P1dB Down to } 0$ dBm, All Phase Angles)	VSWR	10:1	—	—	—
Ruggedness ($V_{DS} = 26$ V, $P_{out} = 42$ dBm, Load VSWR = 10:1, All Phase Angles)	Ψ	No Damage After Test			

Freescale Semiconductor, Inc.



C1, C2, C3, C4, C5, C8	1 μ F Surface Mount Chip Capacitors	J1, J2	Header (Break-away), HDR2X10STIMCSAFU
C6	4.7 pF AVX Chip Capacitor, ACCU-P (08051J4R7BBT)	J3, J4	SMA Connector 2052-1618-02 (Threaded)
C7	47 pF AVX Chip Capacitor, ACCU-P (08055K470JBTTR)	R1, R2, R3	100 Ω Chip Resistors (0402)
C9	33 pF AVX Chip Capacitor, ACCU-P (08053J330JBT)	PCB	Rogers 04350, 20 mils

Figure 1. 921-960 MHz Demo Board Schematic

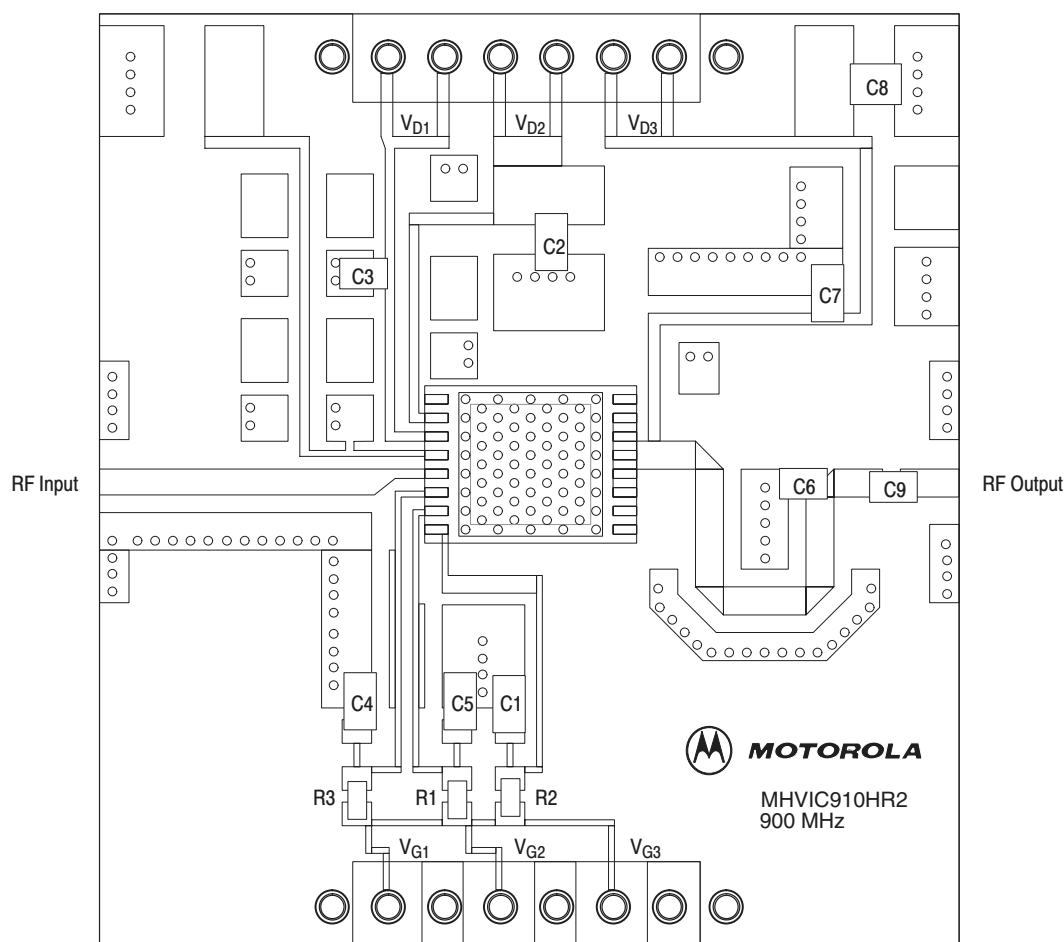


Figure 2. 921-960 MHz Demo Board Component Layout

Freescale Semiconductor, Inc.

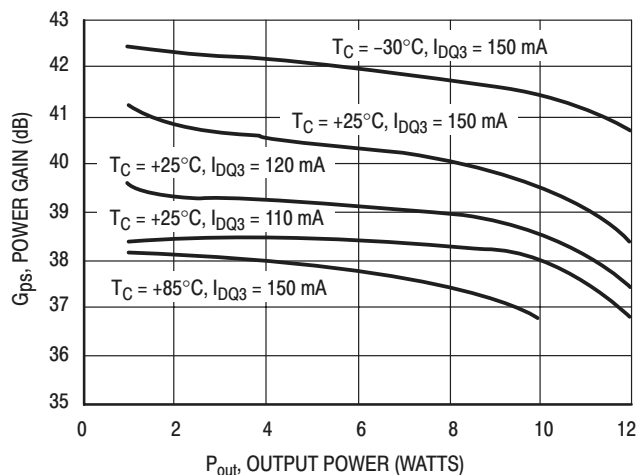


Figure 3. Power Gain versus Output Power

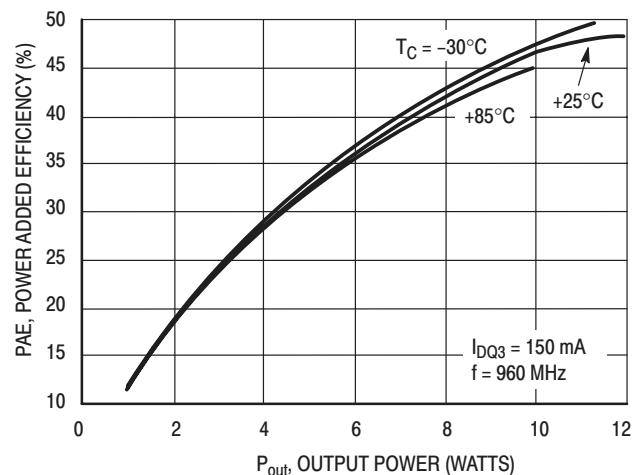


Figure 4. Power Added Efficiency versus Output Power

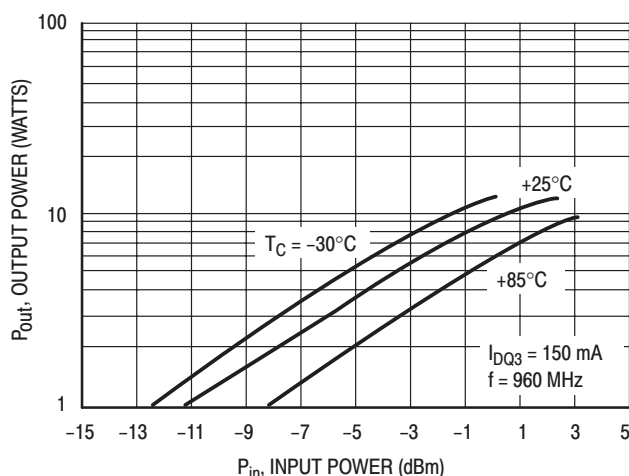


Figure 5. Output Power versus Input Power

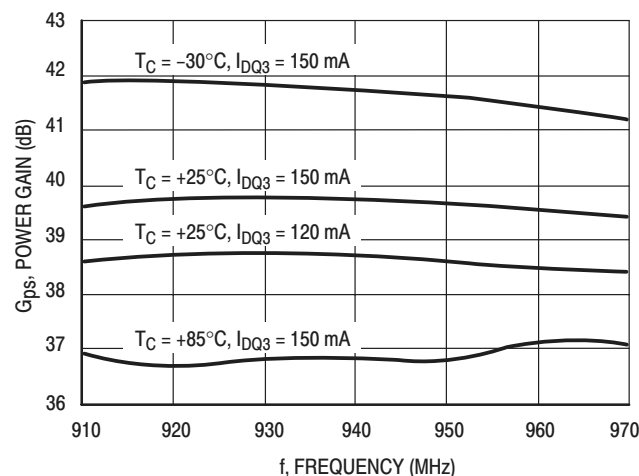


Figure 6. Power Gain versus Frequency
P_{out} = 10 W

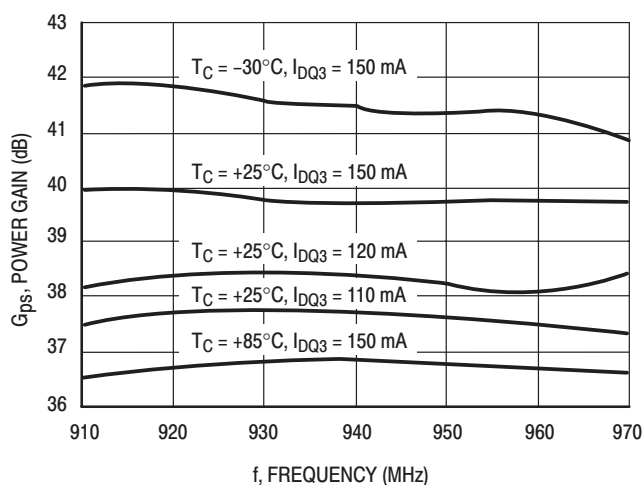


Figure 7. Power Gain versus Frequency
P_{out} = P1dB

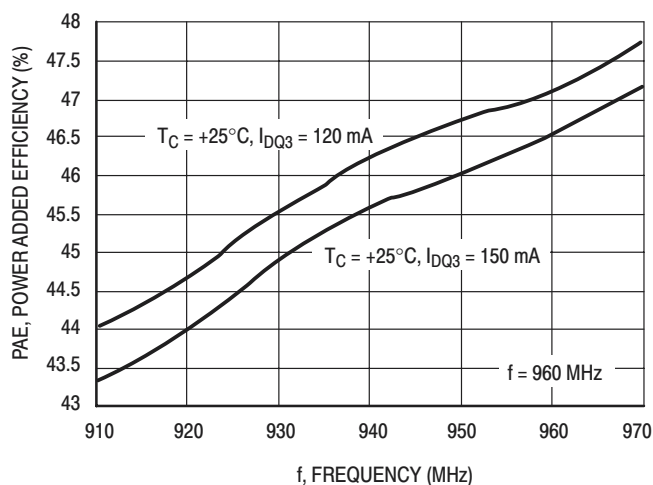


Figure 8. Power Added Efficiency versus Frequency
P_{out} = 10 W

Freescale Semiconductor, Inc.

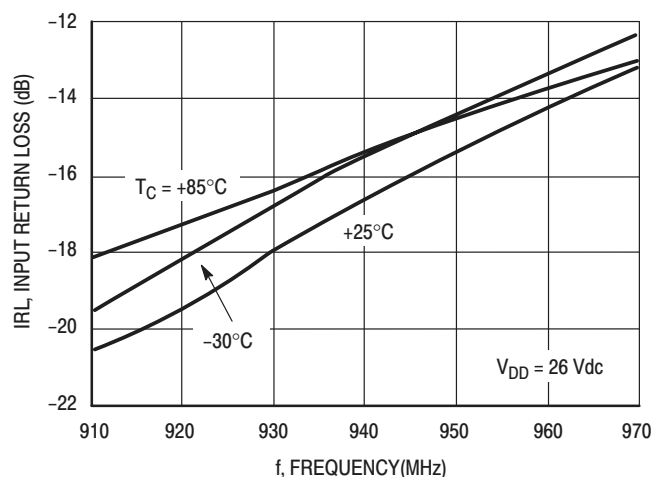


Figure 9. Input Return Loss versus Frequency
 $P_{out} = 10\text{ W}$

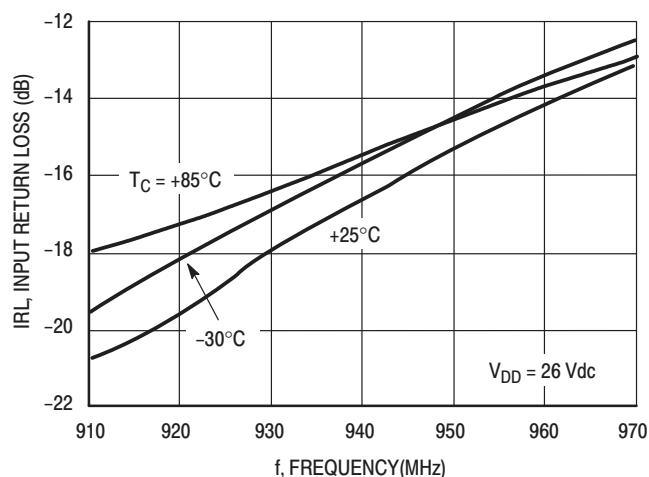


Figure 10. Input Return Loss versus Frequency
 $P_{out} = P_{1dB}$

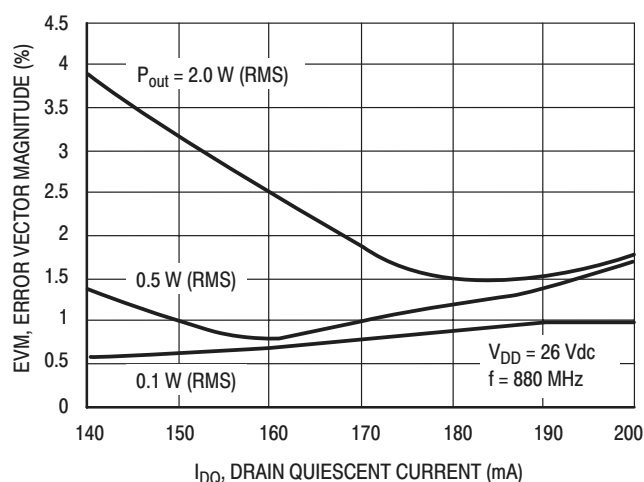


Figure 11. Error Vector Magnitude versus I_{DQ} Total

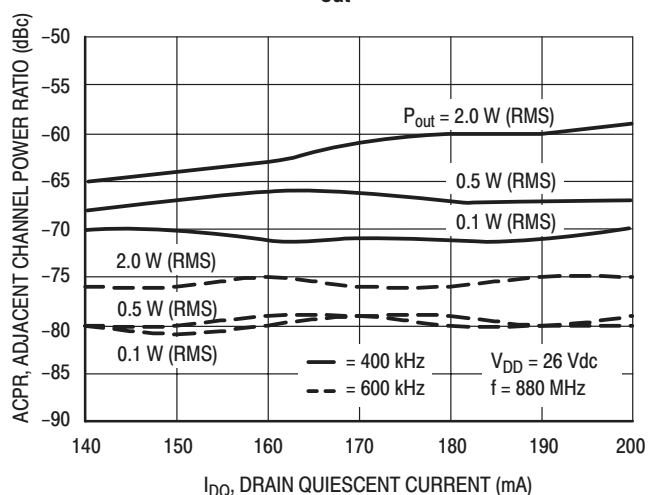


Figure 12. Adjacent Channel Power Ratio versus I_{DQ} Total

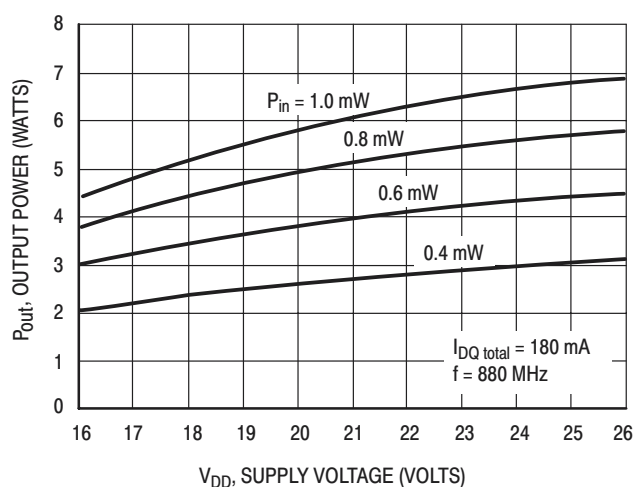


Figure 13. Output Power versus Supply Voltage

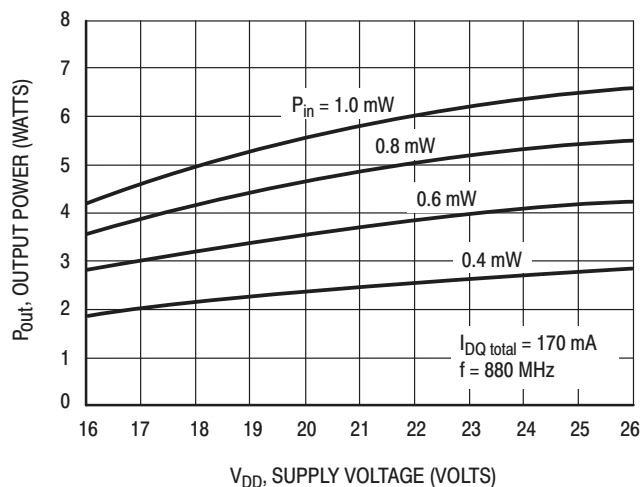


Figure 14. Output Power versus Supply Voltage

Freescale Semiconductor, Inc.

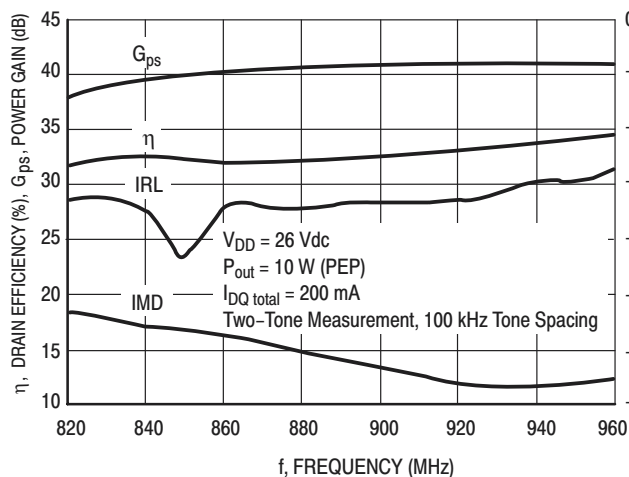


Figure 15. Two-Tone Broadband Performance

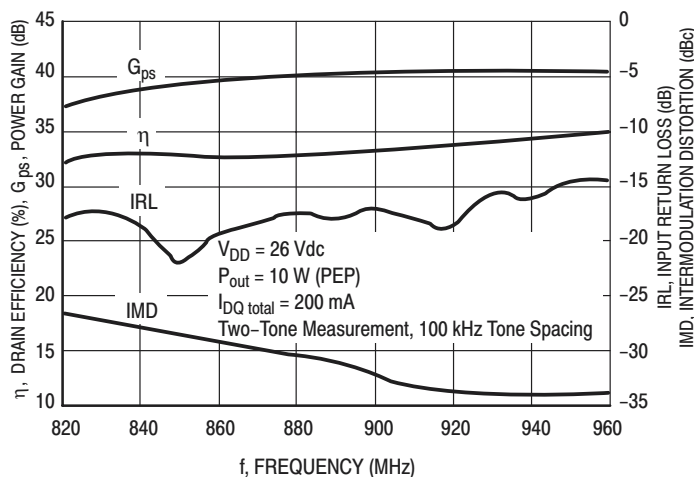


Figure 16. Two-Tone Broadband Performance

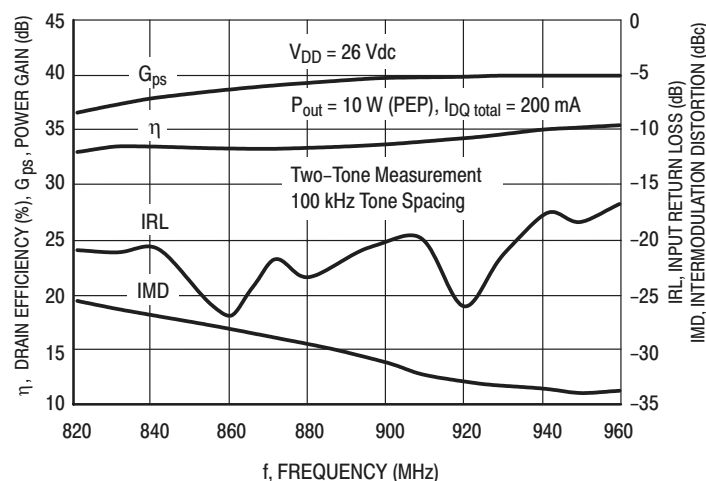


Figure 17. Two-Tone Broadband Performance

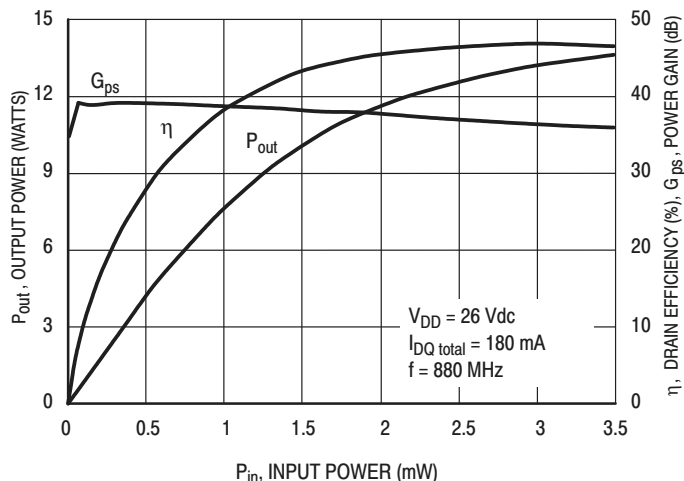


Figure 18. CW Performance @ 880 MHz

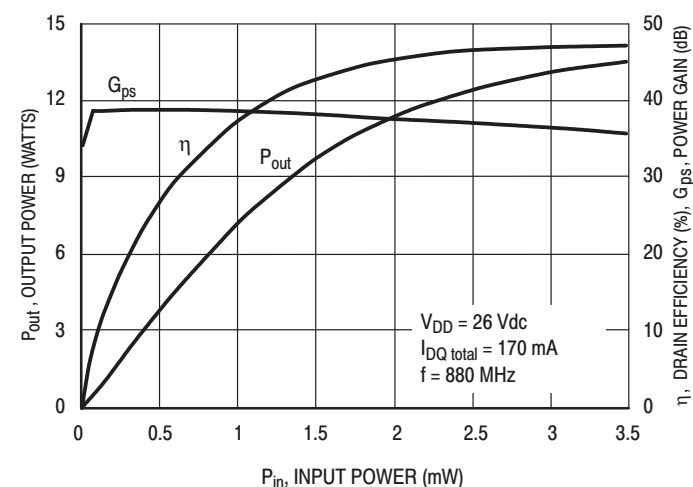


Figure 19. CW Performance @ 880 MHz

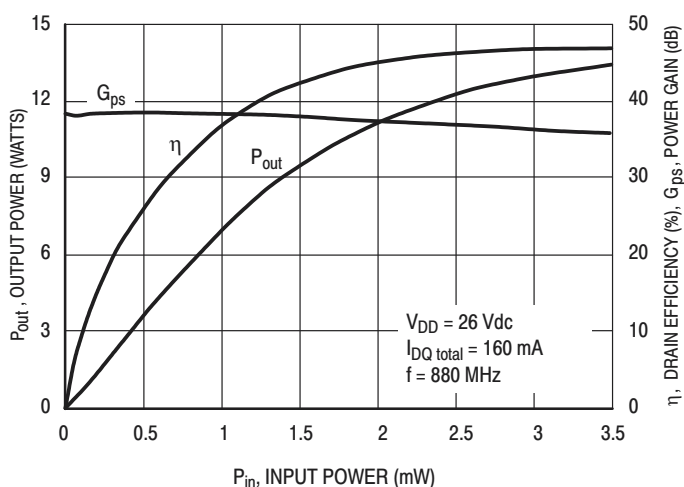


Figure 20. CW Performance @ 880 MHz

Freescale Semiconductor, Inc.

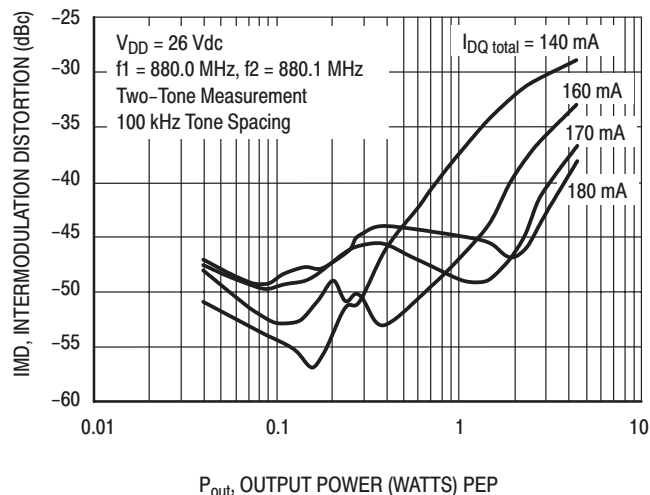
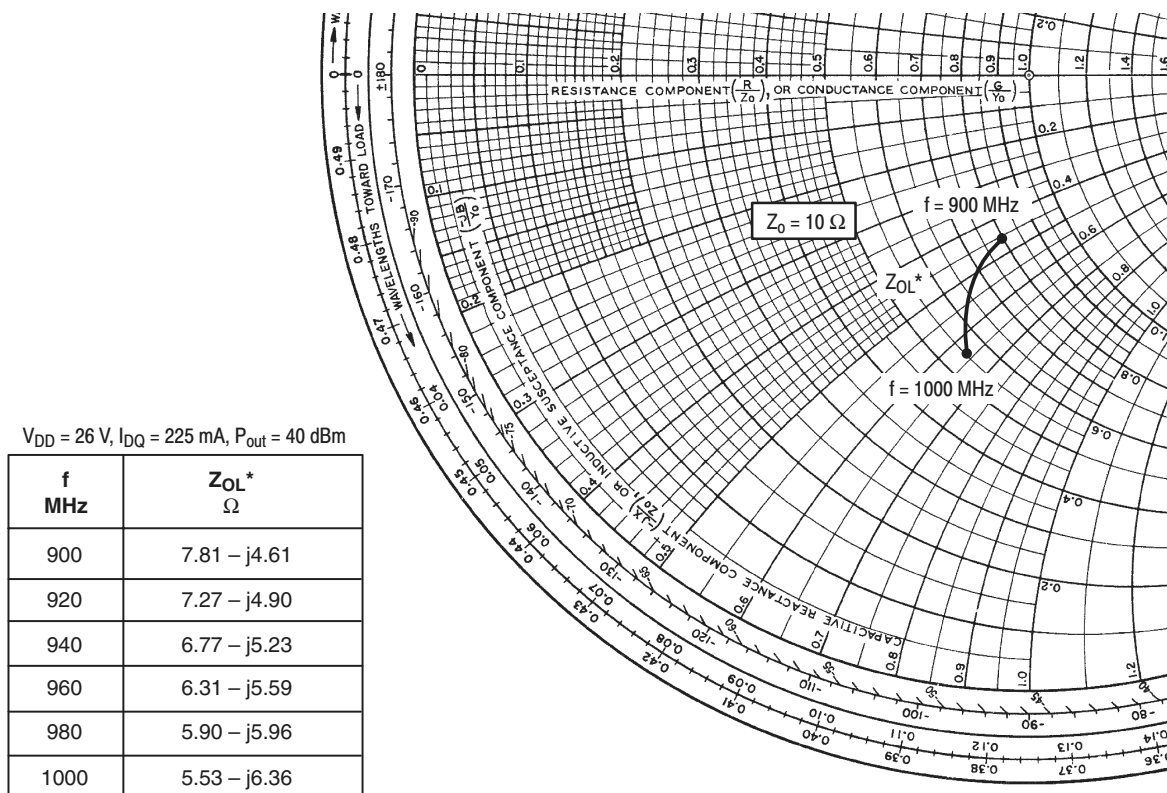


Figure 21. Intermodulation Distortion versus Output Power



Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, and drain efficiency.

Figure 22. Large Signal Impedance

The RF Line

746-960 MHz RF LDMOS Wideband Integrated Power Amplifier

The MHVIC915R2 wideband integrated circuit is designed for CDMA and GSM/GSM EDGE applications. It uses Motorola's newest high voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On Chip integral matching circuitry makes it usable from 746 to 960 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, and CDMA. The device is packaged in a PFP-16 flat pack package that provides excellent thermal performance through a solderable backside contact.

- Typical CDMA Performance: 869-894 MHz, 27 Volts, $I_{DQ1} = 80$ mA, $I_{DQ2} = 120$ mA, 1-Carrier N-CDMA, IS-95 CDMA 9-Channel Forward

Driver Application

Output Power — 23 dBm
Power Gain — 31 dB
Adjacent Channel Power Ratio —
-60 dBc @ 750 kHz in a 30 kHz BW
-66 dBc @ 1.98 MHz in a 30 kHz BW

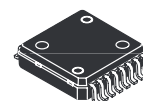
Output Application

Output Power — 34 dBm
PAE = 21%
Adjacent Channel Power Ratio —
-50 dBc @ 750 kHz in a 30 kHz BW

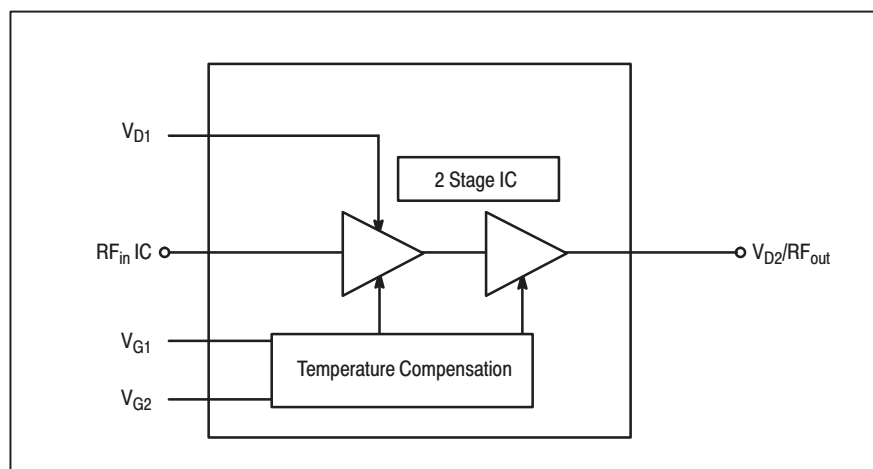
- Typical GSM Performance: 921-960 MHz, 26 Volts
Output Power — 15 W P1dB
Power Gain — 30 dB @ P1dB
Drain Efficiency = 56% @ P1dB
- On-Chip Matching (50 Ohm Input, >9 Ohm Output)
- Integrated Temperature Compensation Capability
- Usable for SCPA and MCPA Architecture
- Integrated ESD Protection
- Available in Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

MHVIC915R2

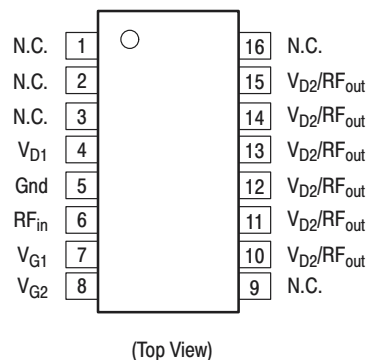
CDMA, GSM/GSM EDGE
746-960 MHz, 15 W, 27 V
RF LDMOS WIDEBAND
INTEGRATED AMPLIFIER



CASE 978-03
PFP-16
PLASTIC



PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Driver Application ($P_{out} = 0.2$ W CW)	Stage 1, 27 Vdc, $I_{DQ} = 80$ mA Stage 2, 27 Vdc, $I_{DQ} = 120$ mA	5.07	
Output Application ($P_{out} = 2.5$ W CW)	Stage 1, 27 Vdc, $I_{DQ} = 80$ mA Stage 2, 27 Vdc, $I_{DQ} = 120$ mA	3.73	
GSM Application ($P_{out} = 15$ W CW)	Stage 1, 26 Vdc, $I_{DQ} = 50$ mA Stage 2, 26 Vdc, $I_{DQ} = 140$ mA	3.41	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)
Charge Device Model	C4 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22–A113	3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

CDMA FUNCTIONAL TESTS (In Motorola CDMA Test Fixture, 50 ohm system) $V_{DS} = 27$ V, $I_{DQ1} = 80$ mA, $I_{DQ2} = 120$ mA, 880 MHz, 1–Carrier N–CDMA, IS–95 CDMA 9–Channel Forward

Common–Source Amplifier Power Gain ($P_{out} = 23$ dBm)	G_{ps}	29	31	—	dB
Power Added Efficiency ($P_{out} = 34$ dBm)	η	—	21	—	%
Input Return Loss ($P_{out} = 23$ dBm)	IRL	—	–12	–9	dB
Adjacent Channel Power Ratio ($P_{out} = 23$ dBm) @ 750 kHz offset in 30 kHz BW	ACPR	—	–60	–55	dBc
Adjacent Channel Power Ratio ($P_{out} = 34$ dBm) @ 750 kHz offset in 30 kHz BW	ACPR	—	–50	—	dBc
Gain Flatness @ $P_{out} = 23$ dBm (865 MHz to 895 MHz)	G_F	—	0.2	0.4	dB

(continued)

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

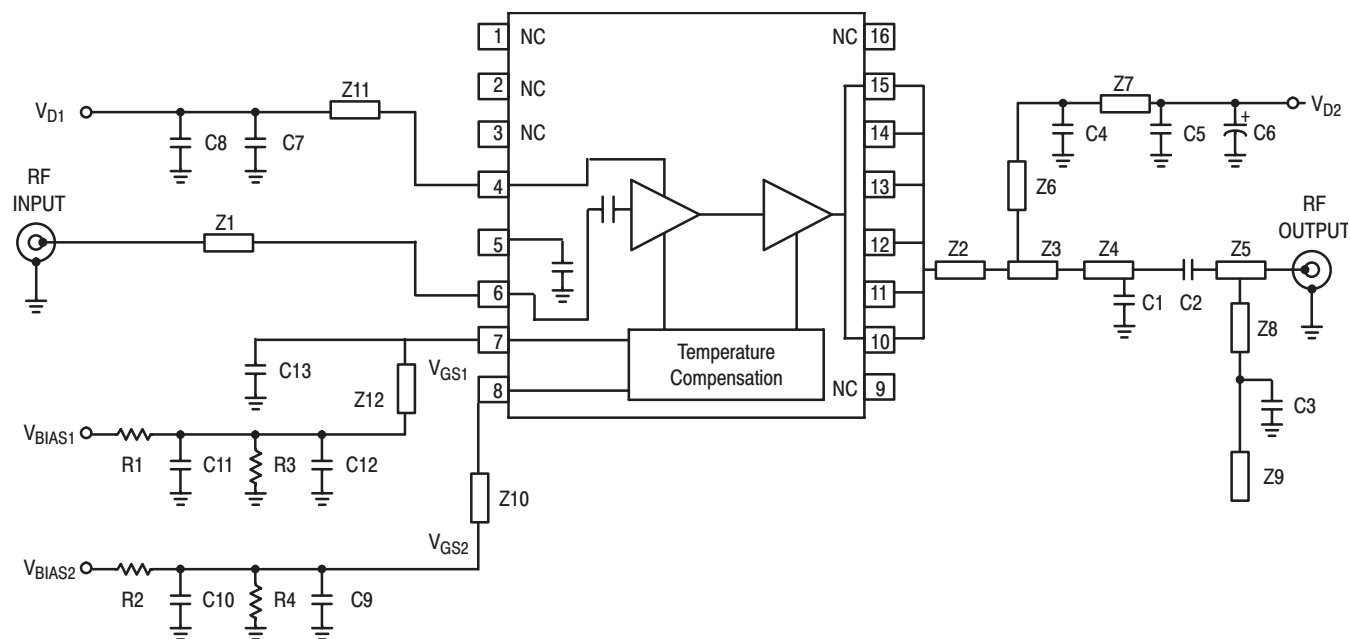
PERFORMANCE TESTS (In Motorola Test Fixture, 50 ohm system) $V_{DS} = 27\text{ V}$, $I_{DQ1} = 80\text{ mA}$, $I_{DQ2} = 120\text{ mA}$, 865–895 MHz

Rating	Symbol	Min	Typ	Max	Unit
Quiescent Current Accuracy over Temperature (–10 to 85°C) at Nominal Value	ΔI_{qt}	—	± 5	—	%
Gain Flatness @ $P_{out} = 23\text{ dBm}$ (800 MHz to 960 MHz)	G_F	—	0.20	—	dB
Deviation from Linear Phase @ $P_{out} = 23\text{ dBm}$	$\emptyset$	—	± 0.2	—	$^\circ$
Group Delay @ $P_{out} = 23\text{ dBm}$	Delay	—	2.2	—	ns
Insertion Phase Window @ $P_{out} = 23\text{ dBm}$ (part to part)	$\Delta\emptyset$	—	± 10	—	$^\circ$

GSM FUNCTIONAL TESTS (In Motorola GSM Test Fixture, 50 ohm system) $V_{DS} = 26\text{ V}$, $I_{DQ1} = 50\text{ mA}$, $I_{DQ2} = 140\text{ mA}$, 921–960 MHz, CW

Rating	Symbol	Min	Typ	Max	Unit
Output Power at 1dB Compression Point	P1dB	—	15	—	Watts
Common–Source Amplifier Power Gain @ P1dB	Gain	—	30	—	dB
Drain Efficiency @ P1dB	η	—	56	—	%
Input return Loss @ P1dB	IRL	—	–16	—	dB
EVM @ 5 W	—	—	0.9	—	%
Third Order Intermodulation Distortion (15 W PEP, 2 Tone 100 kHz spacing)	IMD3	—	–30	—	dBc
Drain Efficiency (15 W PEP, 2 Tone 100 kHz spacing)	η	—	35	—	%

Freescale Semiconductor, Inc.



Z1	0.0438" x 0.400" 50 Ω Microstrip	Z7	0.0504" x 0.480" Microstrip
Z2	0.1709" x 0.1004" Microstrip (not including IC pad length)	Z8	0.0252" x 0.843" Microstrip
Z3	0.1222" x 0.1944" Microstrip	Z9	0.0252" x 0.167" Microstrip
Z4	0.0836" x 0.3561" Microstrip	Z10	0.040" x 0.850" Microstrip
Z5	0.0438" x 0.2725" Microstrip	Z11	0.025" x 0.400" Microstrip
Z6	0.0504" x 0.3378" Microstrip	Z12	0.020" x 0.710" Microstrip
		PCB	Rogers 4350, 0.020", $\epsilon_r = 3.50$

Figure 1. MHVIC915 746–960 MHz Test Circuit Schematic

Table 1. MHVIC915 746–960 MHz Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1, C2	4.7 pF High Q Capacitors (0603)	ATC600S4R7CW	ATC
C3, C4	47 pF NPO Capacitors (0805)	GRM40–001COG470J050BD	Murata
C5, C8, C10, C11	1 μ F X7R Chip Capacitors (1214)	GRM42–2X7R105K050AL	Murata
C6	10 μ F, 50 V Electrolytic Capacitor	ECEV1HA100SP	Panasonic
C7, C9, C12	0.01 μ F X7R Chip Capacitors (0805)	GRM40X7R103J050BD	Murata
C13	8.2 pF NPO Chip Capacitor (0805)	GRM40–001COG8R2C050BD	Murata
R1, R2	1 k Ω Chip Resistors (0603)	RM73B2AT102J	KOA Speer
R3, R4	100 k Ω Chip Resistors (0603)	RM73B2AT104J	KOA Speer

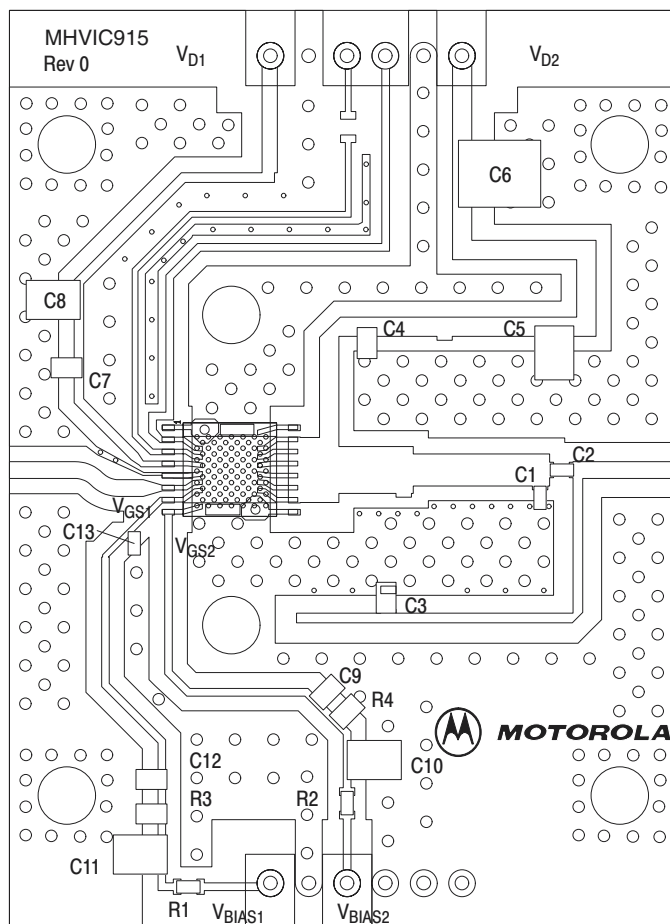


Figure 2. MHVIC915 746–960 MHz Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS (MOTOROLA TEST FIXTURE, 50 OHM SYSTEM)

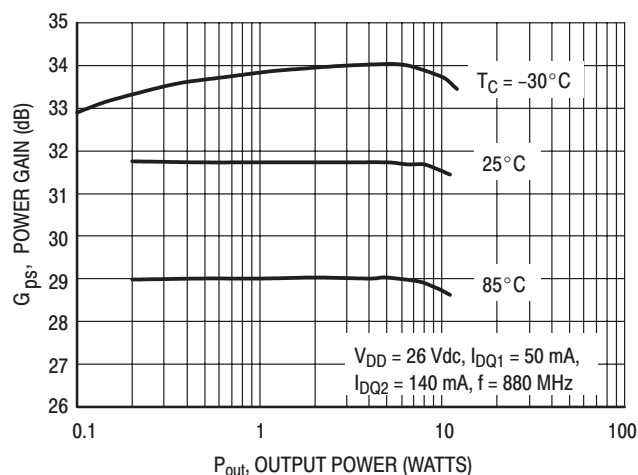


Figure 3. Power Gain versus Output Power

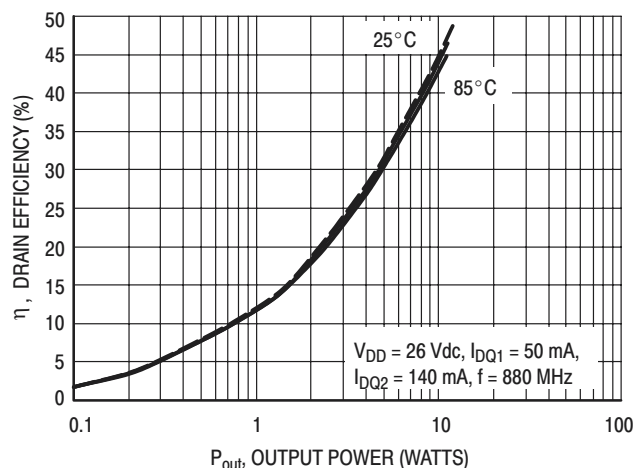


Figure 4. Drain Efficiency versus Output Power

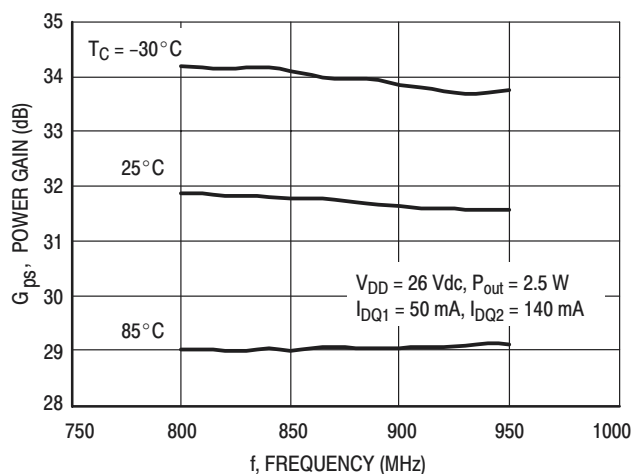


Figure 5. Power Gain versus Frequency

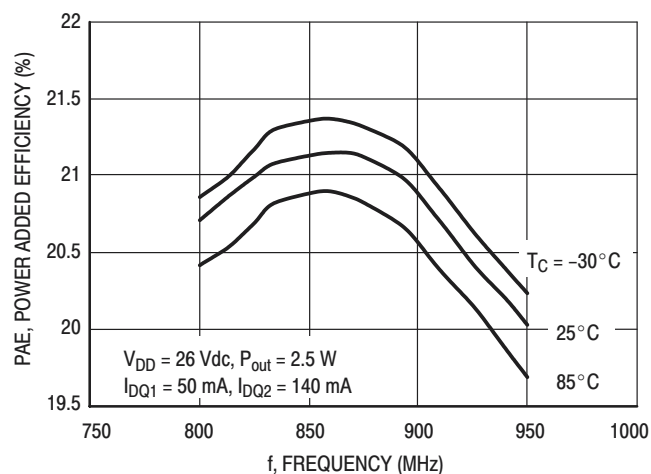


Figure 6. Power Added Efficiency versus Frequency

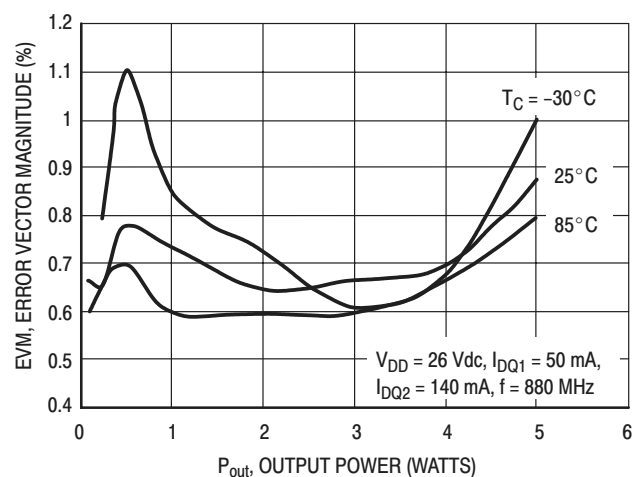


Figure 7. Error Vector Magnitude versus Output Power

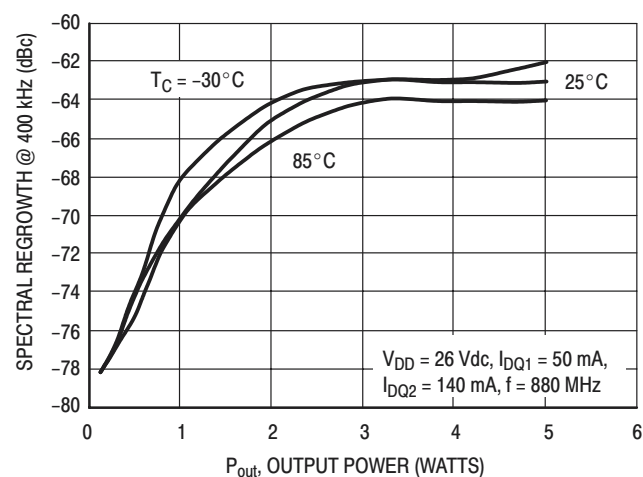


Figure 8. Spectral Regrowth @ 400 kHz versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS (MOTOROLA TEST FIXTURE, 50 OHM SYSTEM)

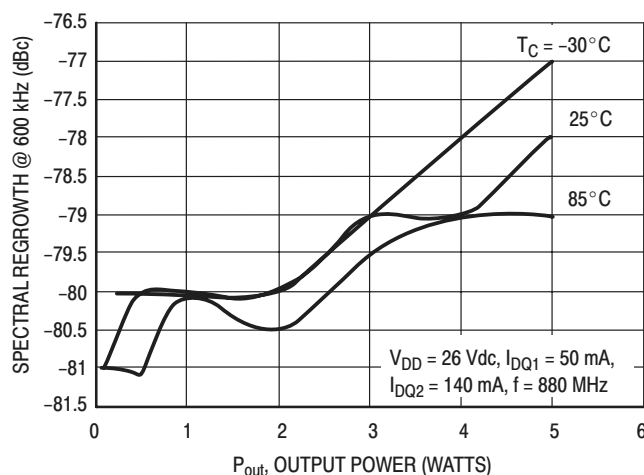


Figure 9. Spectral Regrowth @ 600 kHz versus Output Power

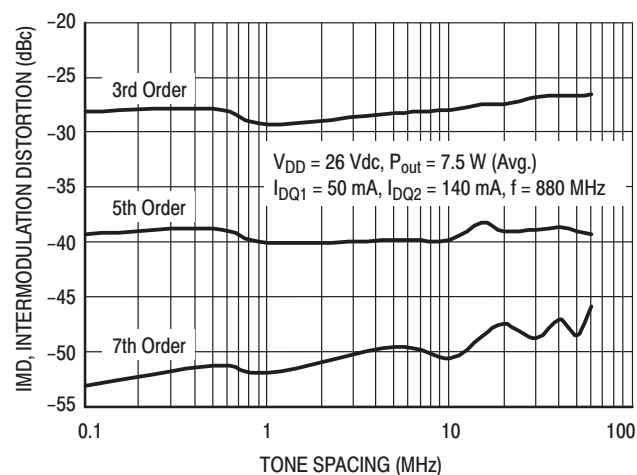


Figure 10. Two-Tone Broadband Performance

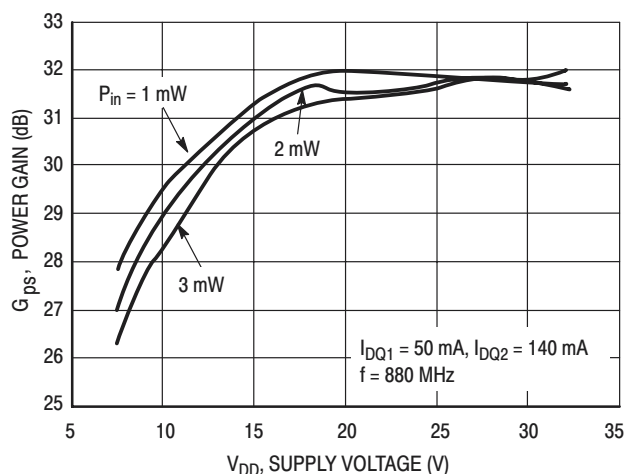


Figure 11. Power Gain versus Supply Voltage

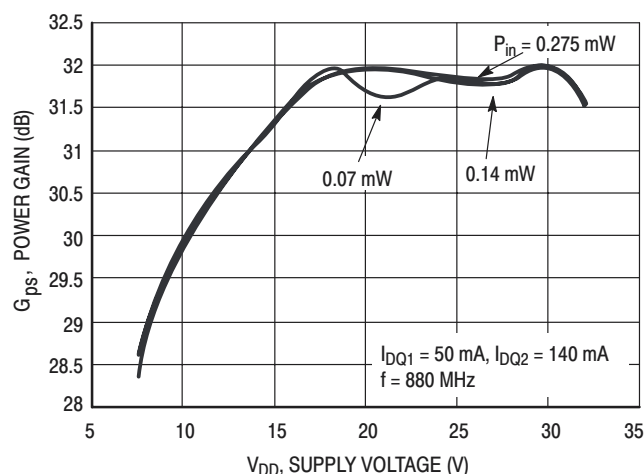


Figure 12. Power Gain versus Supply Voltage

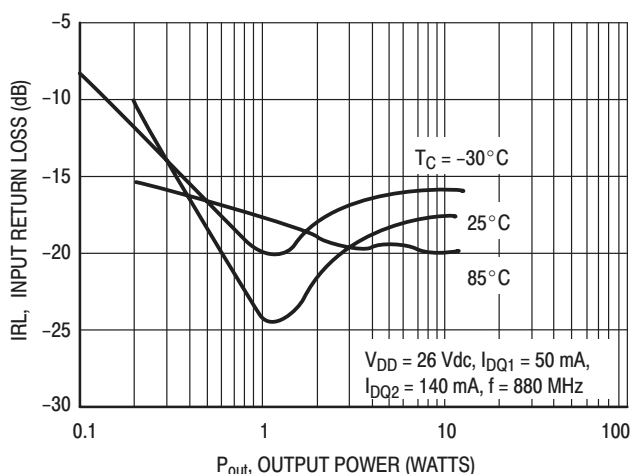


Figure 13. Input Return Loss versus Output Power

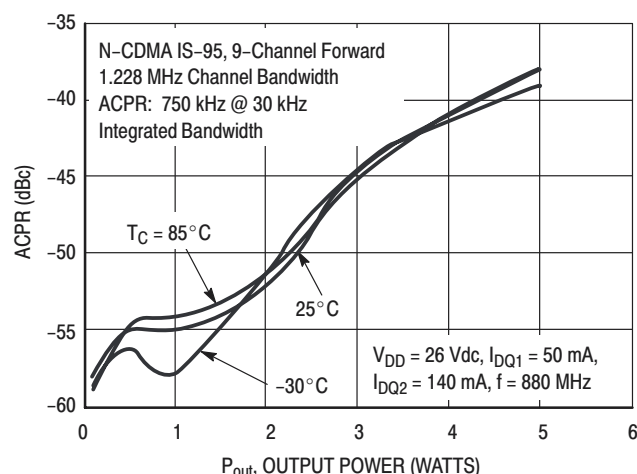
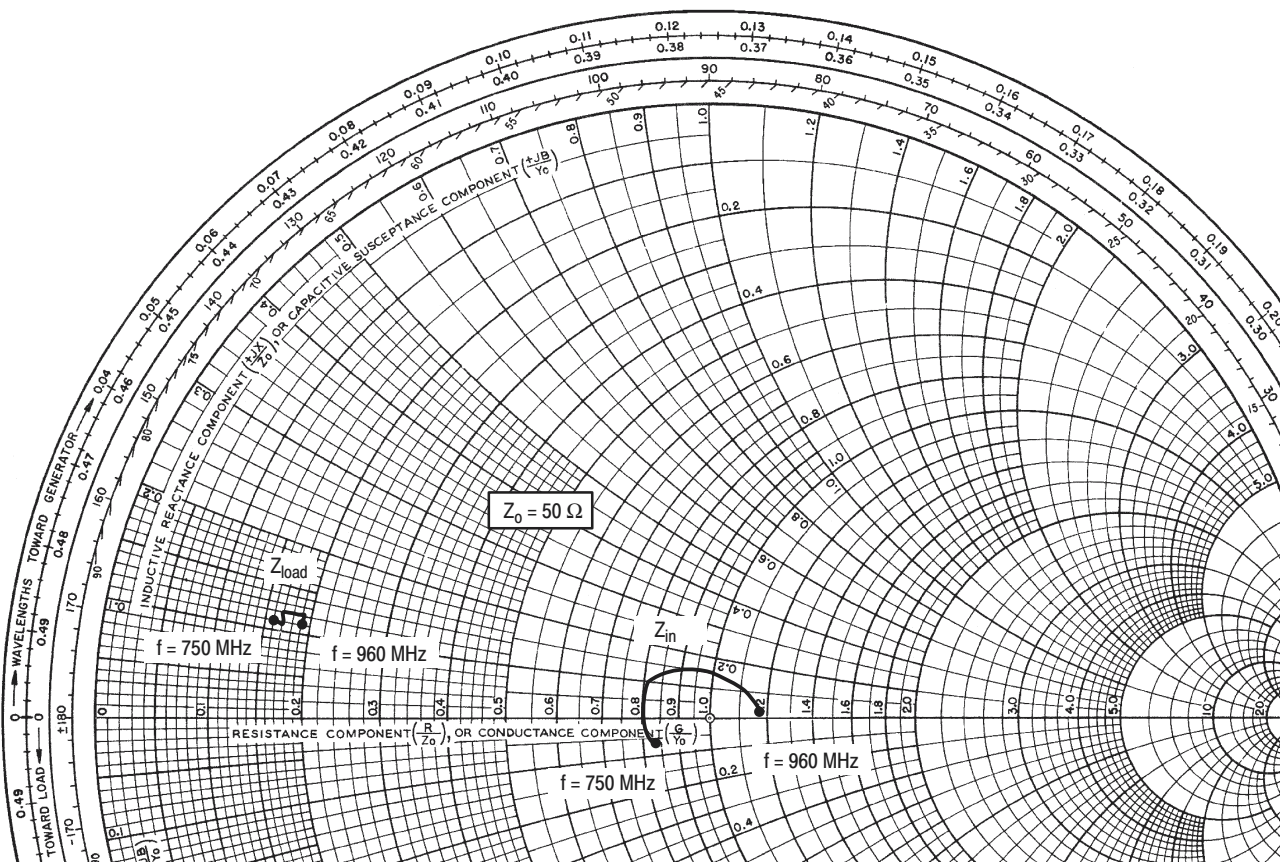


Figure 14. Adjacent Channel Power Ratio versus Output Power



$V_{DD} = 26 \text{ Vdc}$, $I_{DQ1} = 50 \text{ mA}$, $I_{DQ2} = 140 \text{ mA}$, $P_{out} = 1.25 \text{ W CW}$

f MHz	Z_{in} Ω	Z_{load} Ω
750	$42.11 - j2.79$	$8.24 + j5.33$
765	$40.86 - j1.37$	$8.31 + j5.56$
780	$40.09 + j0.06$	$8.39 + j5.82$
795	$39.77 + j1.52$	$8.50 + j5.95$
810	$39.89 + j3.01$	$8.62 + j6.02$
825	$40.49 + j4.39$	$8.82 + j6.12$
840	$41.48 + j5.70$	$8.94 + j6.19$
855	$42.89 + j6.73$	$9.12 + j6.17$
870	$43.51 + j7.03$	$9.16 + j6.12$
885	$46.81 + j7.87$	$9.33 + j6.09$
900	$49.21 + j7.74$	$9.38 + j5.95$
915	$51.79 + j7.02$	$9.50 + j5.85$
930	$54.48 + j5.65$	$9.47 + j5.73$
945	$57.05 + j3.61$	$9.54 + j5.63$
960	$59.16 + j0.75$	$9.42 + j5.45$

Z_{in} = Device input impedance as measured from RF input to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

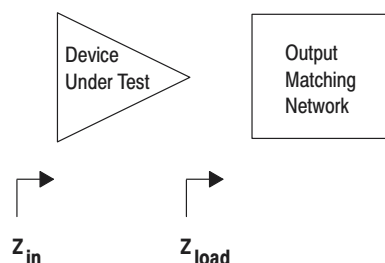


Figure 15. Series Equivalent Input and Output Impedance

The RF Line

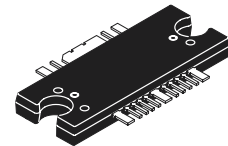
RF LDMOS Wideband Integrated Power Amplifiers

The MW4IC915MB/GMB wideband integrated circuit is designed for GSM and GSM EDGE base station applications. It uses Motorola's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On Chip design makes it usable from 750 to 1000 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, N-CDMA and W-CDMA.

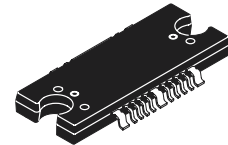
- Typical GSM/GSM EDGE Performances: 26 Volts, $I_{DQ1} = 60$ mA, $I_{DQ2} = 240$ mA, 869–894 MHz and 921–960 MHz
Output Power — 3 Watts Avg.
Power Gain — 31 dB
Efficiency — 19%
Spectral Regrowth @ 400 kHz Offset = –65 dBc
Spectral Regrowth @ 600 kHz Offset = –83 dBc
EVM — 1.5%
- Typical Performance: 860–960 MHz, 26 Volts
Output Power — 15 Watts CW
Power Gain — 30 dB
Efficiency — 44%
- On Chip Matching (50 Ohm Input, >3 Ohm Output)
- Integrated Temperature Compensation Capability with Enable/Disable Function
- Integrated ESD Protection
- Capable of Handling 5:1 VSWR, @ 26 Vdc, $f = 921$ MHz,
 $P_{out} = 15$ W CW, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA
- Can Be Bolted or Soldered through a Hole in the Circuit Board for Maximum Thermal Performance
- Also Available in Gull Wing for Surface Mount
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MW4IC915MBR1 MW4IC915GMBR1

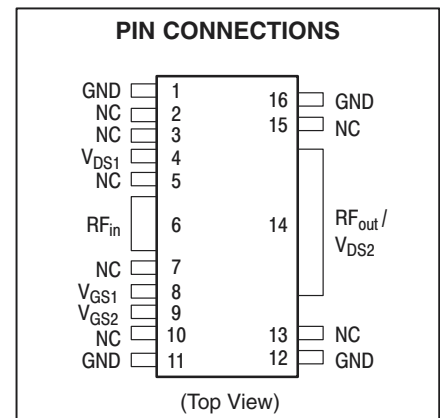
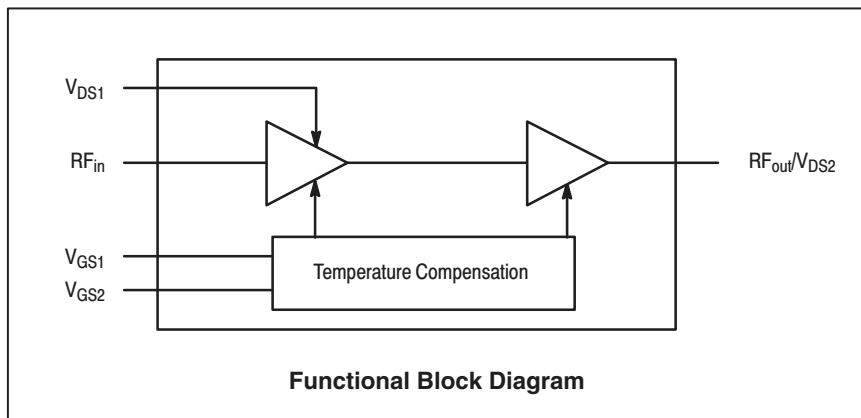
**GSM/GSM EDGE,
N-CDMA, W-CDMA
860 – 960 MHz, 15 W, 26 V
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS**



**CASE 1329–08
TO–272 WIDE BODY MULTI–LEAD
PLASTIC
MW4IC915MBR1**



**CASE 1329A–02
TO–272 WIDE BODY MULTI–LEAD
GULL WING
PLASTIC
MW4IC915GMBR1**



Freescale Semiconductor, Inc.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5. +15	Vdc
Storage Temperature Range	T_{stg}	–65 to +175	°C
Operating Junction Temperature	T_J	175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
GSM Application ($P_{out} = 15$ W CW)	Stage 1, 26 Vdc, $I_{DQ} = 60$ mA Stage 2, 26 Vdc, $I_{DQ} = 240$ mA	1.48	
GSM EDGE Application ($P_{out} = 7.5$ W CW)	Stage 1, 26 Vdc, $I_{DQ} = 60$ mA Stage 2, 26 Vdc, $I_{DQ} = 240$ mA	1.59	
CDMA Application ($P_{out} = 3.75$ W CW)	Stage 1, 26 Vdc, $I_{DQ} = 60$ mA Stage 2, 26 Vdc, $I_{DQ} = 240$ mA	1.63	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C2 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22–A113	3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

TWO–TONE FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Two–Tone Common–Source Amplifier Power Gain ($V_{DS} = 26$ Vdc, $P_{out} = 15$ W PEP, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f_1 = 869$ MHz, $f_2 = 869.1$ MHz and $f_1 = 960$ MHz and $f_2 = 960.1$ MHz)	G_{ps}	29	31	—	dB
Drain Efficiency ($V_{DS} = 26$ Vdc, $P_{out} = 15$ W PEP, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f_1 = 869$ MHz, $f_2 = 869.1$ MHz and $f_1 = 960$ MHz and $f_2 = 960.1$ MHz)	η	29	31	—	%
Third Order Intermodulation Distortion ($V_{DS} = 26$ Vdc, $P_{out} = 15$ W PEP, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f_1 = 869$ MHz, $f_2 = 869.1$ MHz and $f_1 = 960$ MHz and $f_2 = 960.1$ MHz)	IMD3	—	–40	–29	dBc
Input Return Loss ($V_{DS} = 26$ Vdc, $P_{out} = 15$ W PEP, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f_1 = 869$ MHz, $f_2 = 869.1$ MHz and $f_1 = 960$ MHz and $f_2 = 960.1$ MHz)	IRL	—	–15	–10	dB

(continued)

Freescale Semiconductor, Inc.

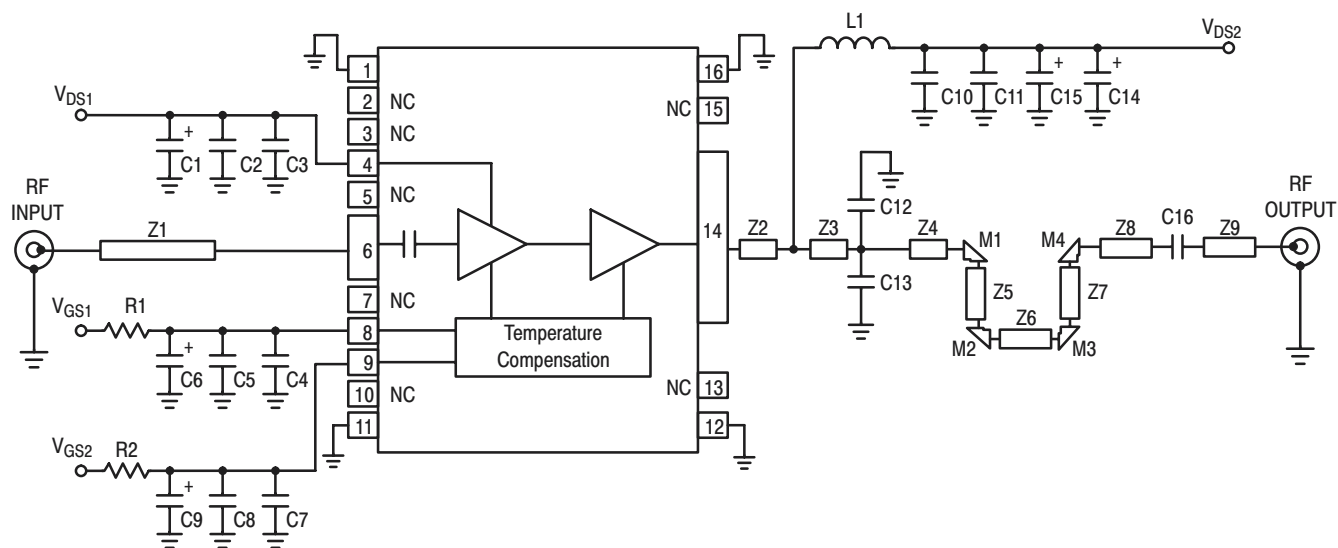
ELECTRICAL CHARACTERISTICS – continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
PERFORMANCE TESTS (In Motorola Reference Board) $V_{DS} = 26\text{ V}$, $I_{DQ1} = 60\text{ mA}$, $I_{DQ2} = 240\text{ mA}$					
Quiescent Current Accuracy over Temperature (-10 to 85°C) at Nominal Value	ΔI_{QT}	—	± 5	—	%
Gain Flatness in 40 MHz Bandwidth @ $P_{out} = 3\text{ W CW}$ (Characterize from 869–894 MHz and 920–960 MHz)	G_F	—	0.2	—	dB
Deviation from Linear Phase in 40 MHz Bandwidth @ $P_{out} = 3\text{ W CW}$ (Characterize from 869–894 MHz and 920–960 MHz)	Φ	—	± 0.6	—	$^\circ$
Delay @ $P_{out} = 3\text{ W CW}$	Delay	—	2.5	—	ns
Insertion Phase Window @ $P_{out} = 3\text{ W CW}$	$\Phi\Delta$	—	± 15	—	$^\circ$

TYPICAL PERFORMANCE GSM/GSM EDGE (In Motorola Reference Board) $V_{DS} = 26\text{ V}$, $I_{DQ1} = 60\text{ mA}$, $I_{DQ2} = 240\text{ mA}$, 869–894 MHz and 921–960 MHz

Output Power at 1dB Compression Point	P1dB	—	20	—	Watts
Common–Source Amplifier Power Gain ($P_{out} = 15\text{ W CW}$)	G_{ps}	—	30	—	dB
Drain Efficiency ($P_{out} = 15\text{ W CW}$)	η	—	44	—	%
Input Return Loss ($P_{out} = 15\text{ W CW}$)	IRL	—	–15	—	dB
Error Vector Magnitude ($P_{out} = 3\text{ W Avg.}$ including 0.6% rms source EVM)	EVM	—	1.5	—	%
Spectral Regrowth at 400 kHz Offset ($P_{out} = 3\text{ W Avg.}$)	SR1	—	–65	—	dBc
Spectral Regrowth at 600 kHz Offset ($P_{out} = 3\text{ W Avg.}$)	SR2	—	–83	—	dBc

Freescale Semiconductor, Inc.



Z1	0.086" , 50 Ω Microstrip	Z6	0.157" x 0.283" Microstrip
Z2	0.133" x 0.236" Microstrip	Z7	0.429" x 0.283" Microstrip
Z3	0.435" x 0.283" Microstrip	Z8	0.394" x 0.088" Microstrip
Z4	0.171" x 0.283" Microstrip	Z9	0.181" x 0.088" Microstrip
Z5	0.429" x 0.283" Microstrip	PCB	Taconic TLX8, 0.030", $\epsilon_r = 2.55$

Figure 1. Two-Tone 860–960 MHz Test Fixture Schematic

Table 1. Two-Tone 860–960 MHz Test Fixture Component Designations and Values

Designators	Description
C1, C6, C9, C14	22 μ F, 35 V Tantalum Chip Capacitors, AVX #TAJE226M035R
C2, C5, C8, C11	1000 pF Chip Capacitors, B Case, ATC #100B102JCA500X
C3, C4, C7, C10, C16	22 pF Chip Capacitors, B Case, ATC #100B220JCA500X
C12, C13	10 pF Chip Capacitors, B Case, ATC #100B100JCA500X
C15	10 μ F Tantalum Chip Capacitor, Kemet #T491X226K035AS4394
R1, R2	10 k Ω , 1/4 W Chip Resistor (1206)
L1	12.5 nH Inductor
M1, M2, M3, M4	0.283", 90° Mitered Microstrip Bends

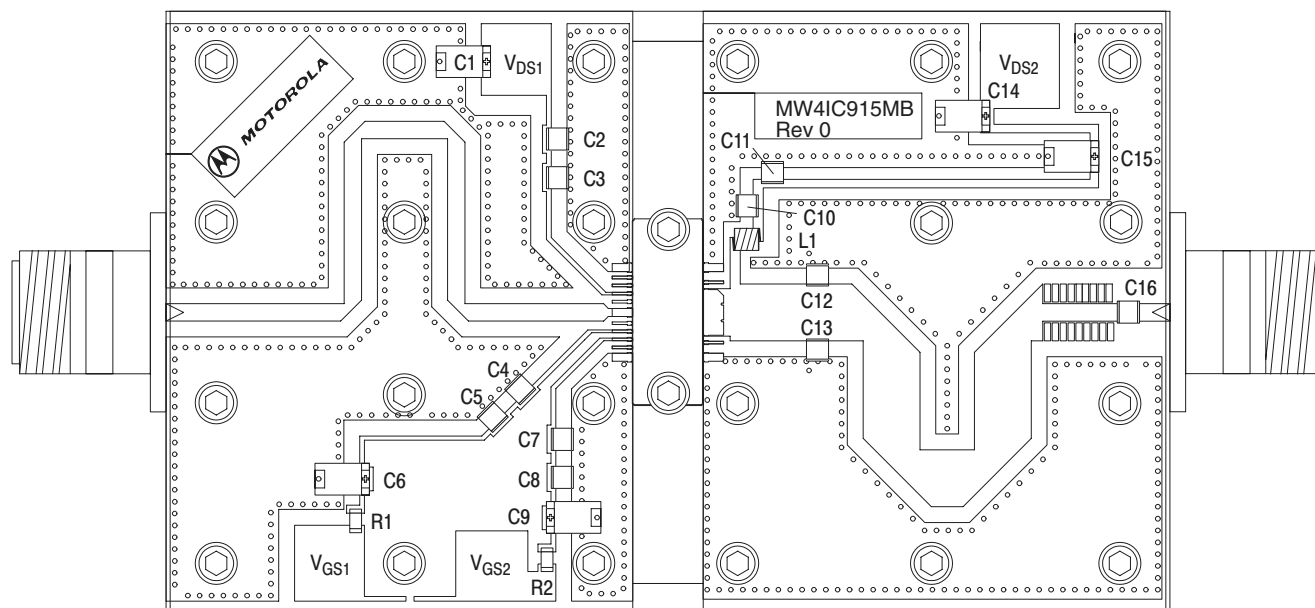
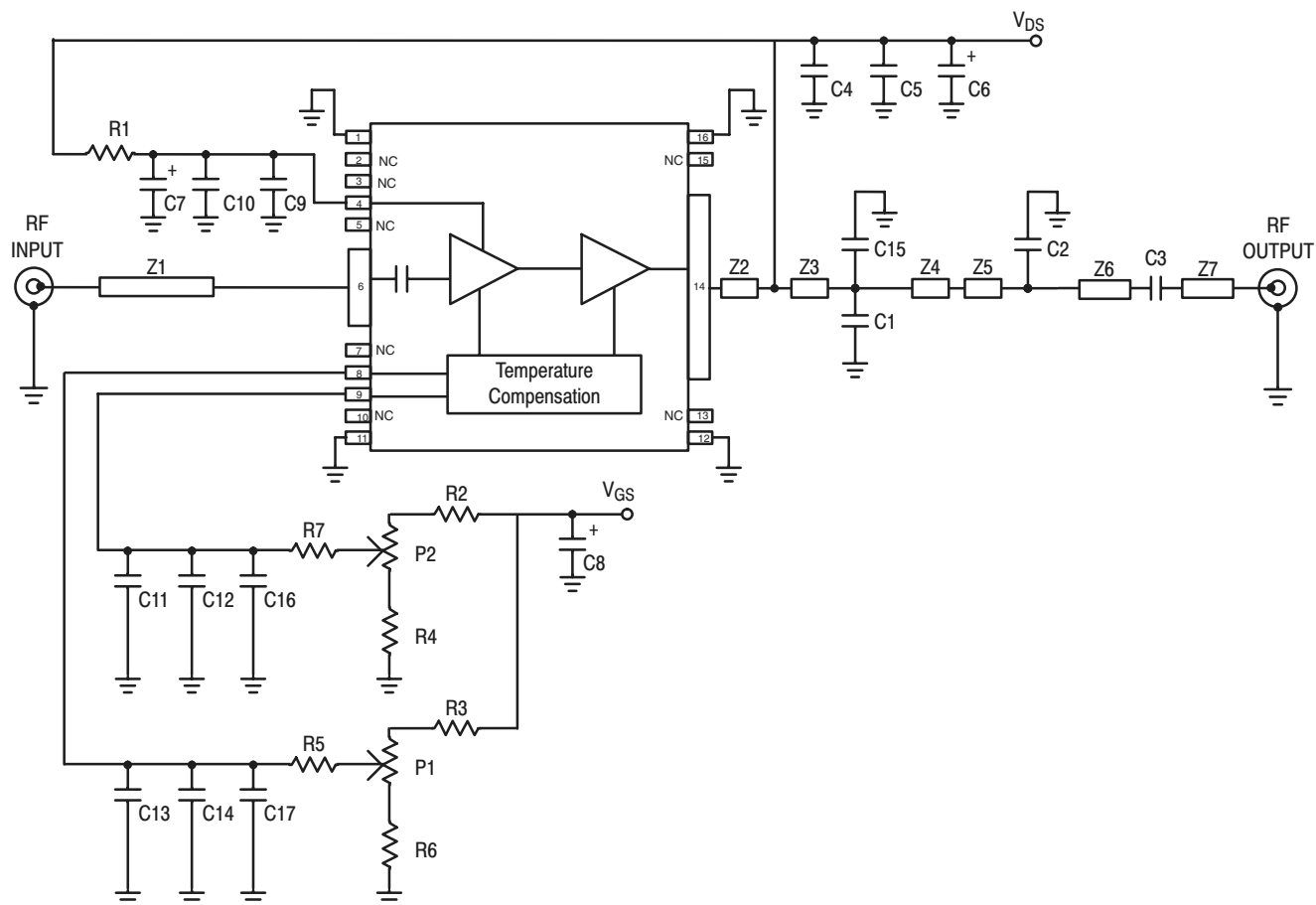


Figure 2. Two-Tone 860–960 MHz Test Fixture Component Layout



Z1	0.681" x 0.039", 50 Ω Microstrip	Z5	0.566" x 0.043" Microstrip
Z2	0.157" x 0.228" Microstrip	Z6	0.165" x 0.043" Microstrip
Z3	0.468" x 0.157" Microstrip	Z7	0.078" x 0.043" Microstrip
Z4	0.220" x 0.157" Microstrip	PCB	Taconic RF35, 0.02", $\epsilon_r = 3.5$

Figure 3. 860-960 MHz Reference Board Schematic

Table 2. 860-960 MHz Reference Board Component Designations and Values

Designators	Description
C1, C15	10 pF Chip Capacitors (0805), ACCU-P AVX #08051J100GBT
C2	5.6 pF Chip Capacitor (0805), ACCU-P AVX #08051J5R6BBT
C3, C4, C9, C11, C13	33 pF Chip Capacitors (0805), ACCU-P AVX #08051J330GB
C5, C10, C12, C14	10 nF Chip Capacitors (0805), AVX #08055C103KAT
C6, C7, C8	22 μ F, 35 V Tantalum Capacitors, AVX #TAJE226M035R
C16, C17	100 nF Chip Capacitors (0805), AVX #08055C104KAT
P1, P2	5 k Ω Potentiometer CMS Cermet Multi-turn, Bourns #3224W
R1, R2, R3, R4, R5	0 Ω , 1/8 W Chip Resistors (0805)
R6, R7	10 k Ω , 1/4 W Chip Resistors (1206)

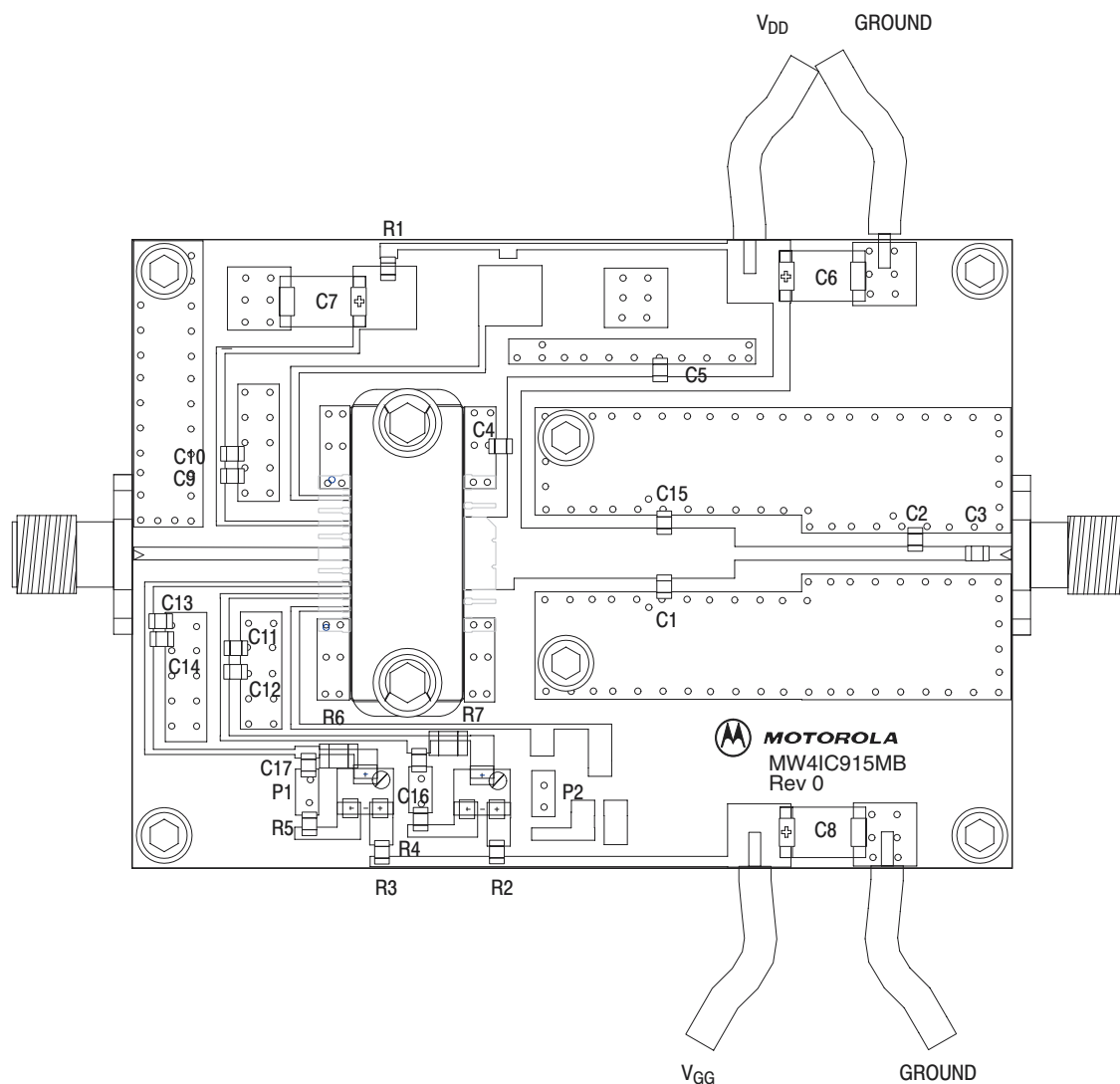


Figure 4. 860–960 MHz Reference Board Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS (MOTOROLA TEST FIXTURE, 50 OHM SYSTEM)

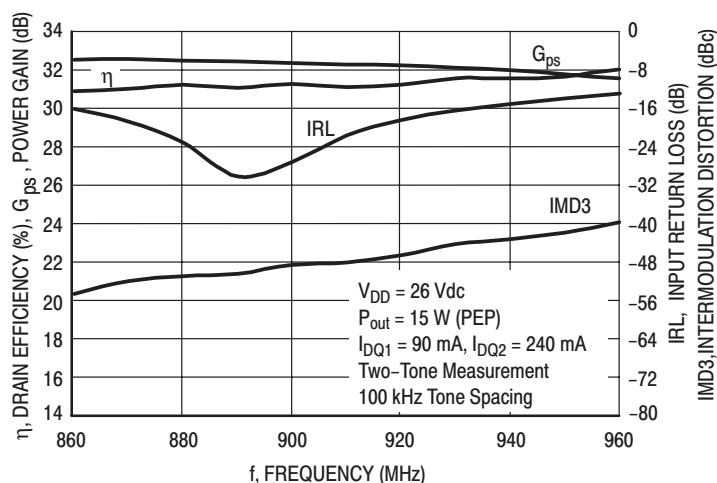


Figure 5. Two-Tone Wideband Circuit Performance

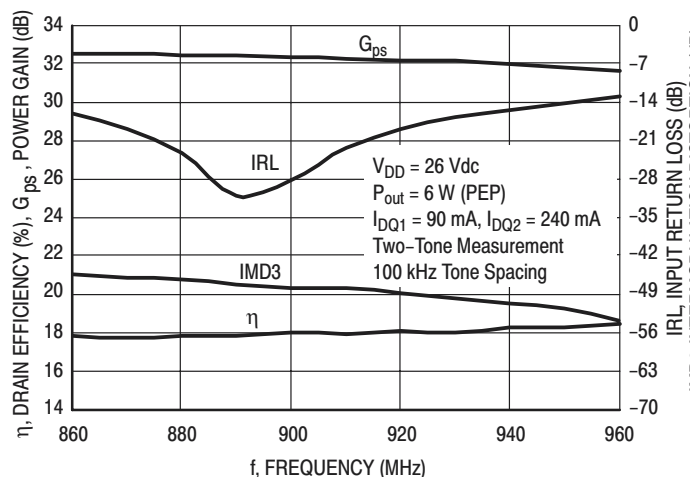


Figure 6. Two-Tone Wideband Circuit Performance

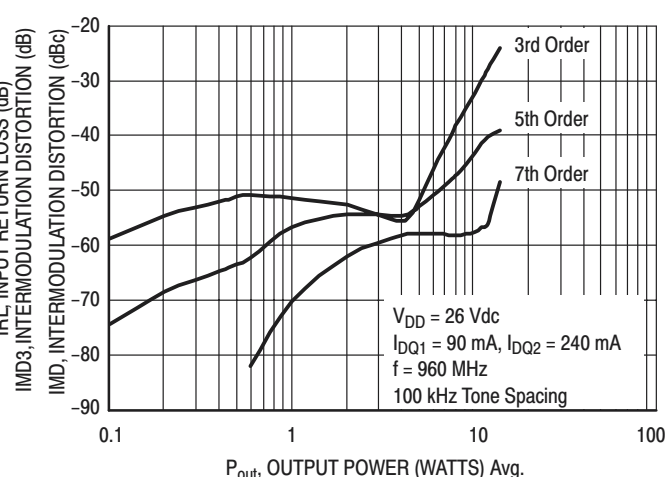


Figure 7. Intermodulation Distortion Products versus Output Power

TYPICAL CHARACTERISTICS (MOTOROLA REFERENCE BOARD)

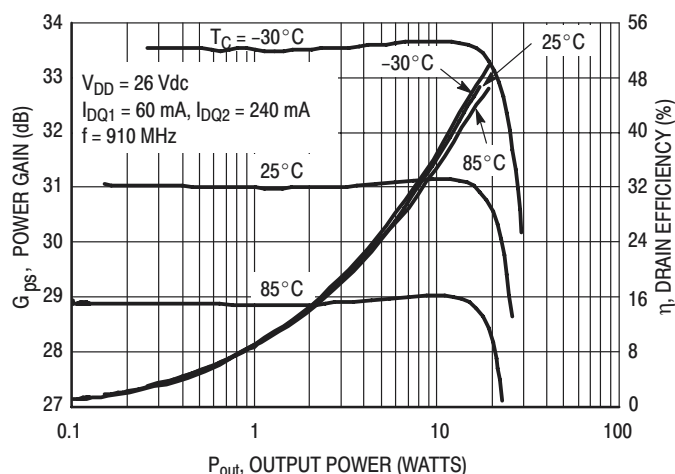


Figure 8. Power Gain and Efficiency versus Output Power

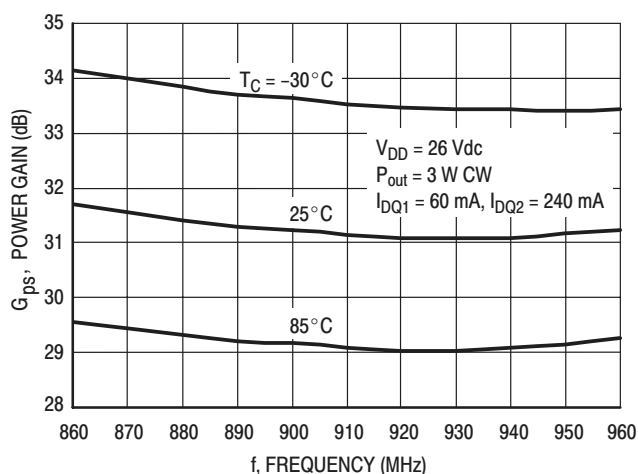


Figure 9. Power Gain versus Frequency

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS (MOTOROLA REFERENCE BOARD) – CONTINUED

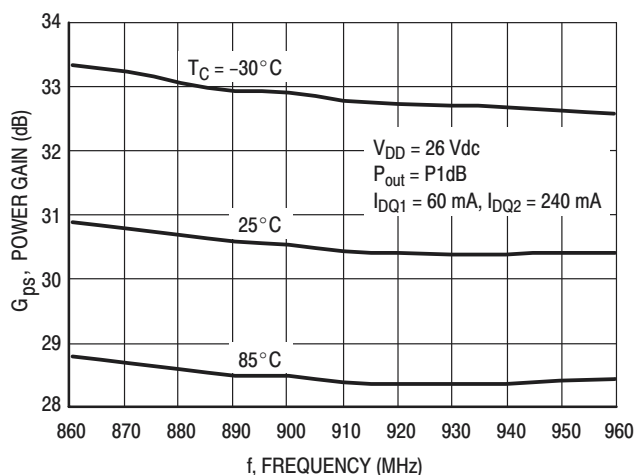


Figure 10. Power Gain versus Frequency

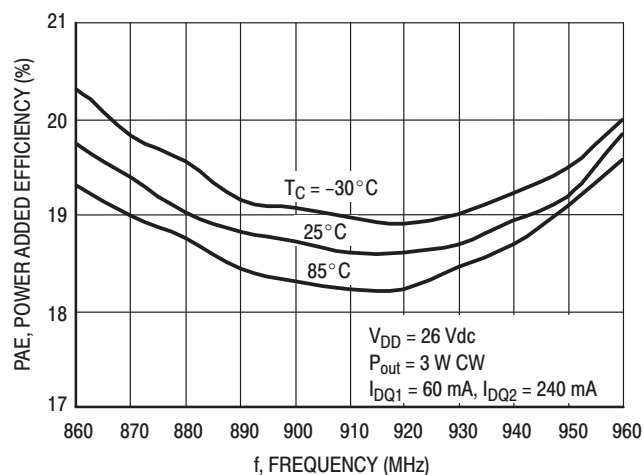


Figure 11. Power Added Efficiency versus Frequency

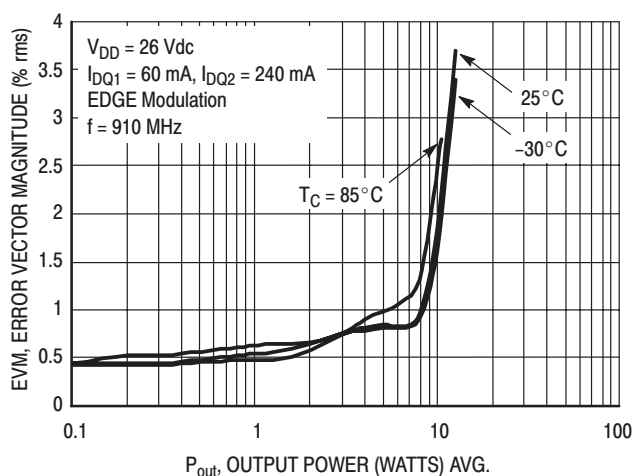


Figure 12. Error Vector Magnitude versus Output Power

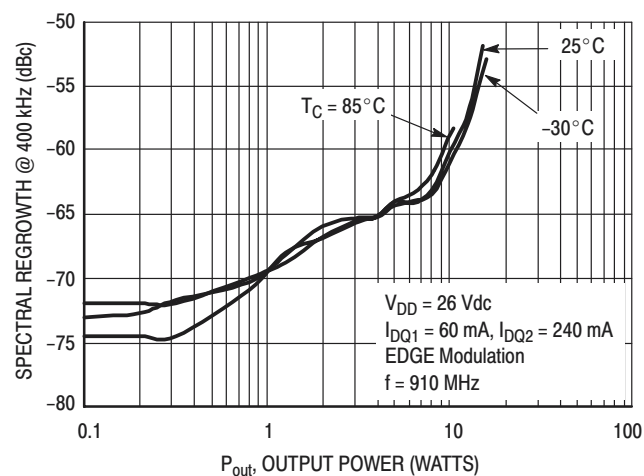


Figure 13. Spectral Regrowth at 400 kHz versus Output Power

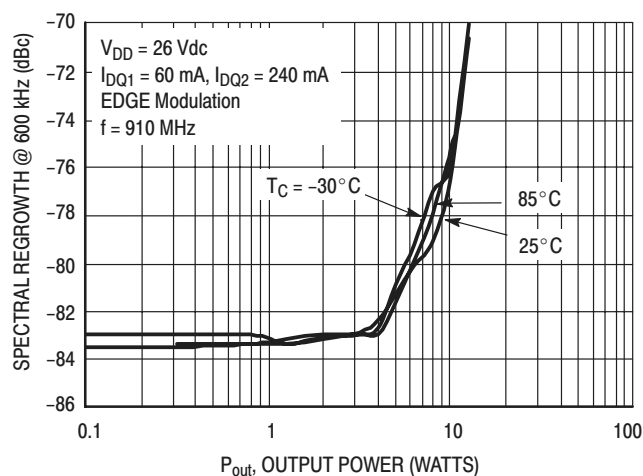
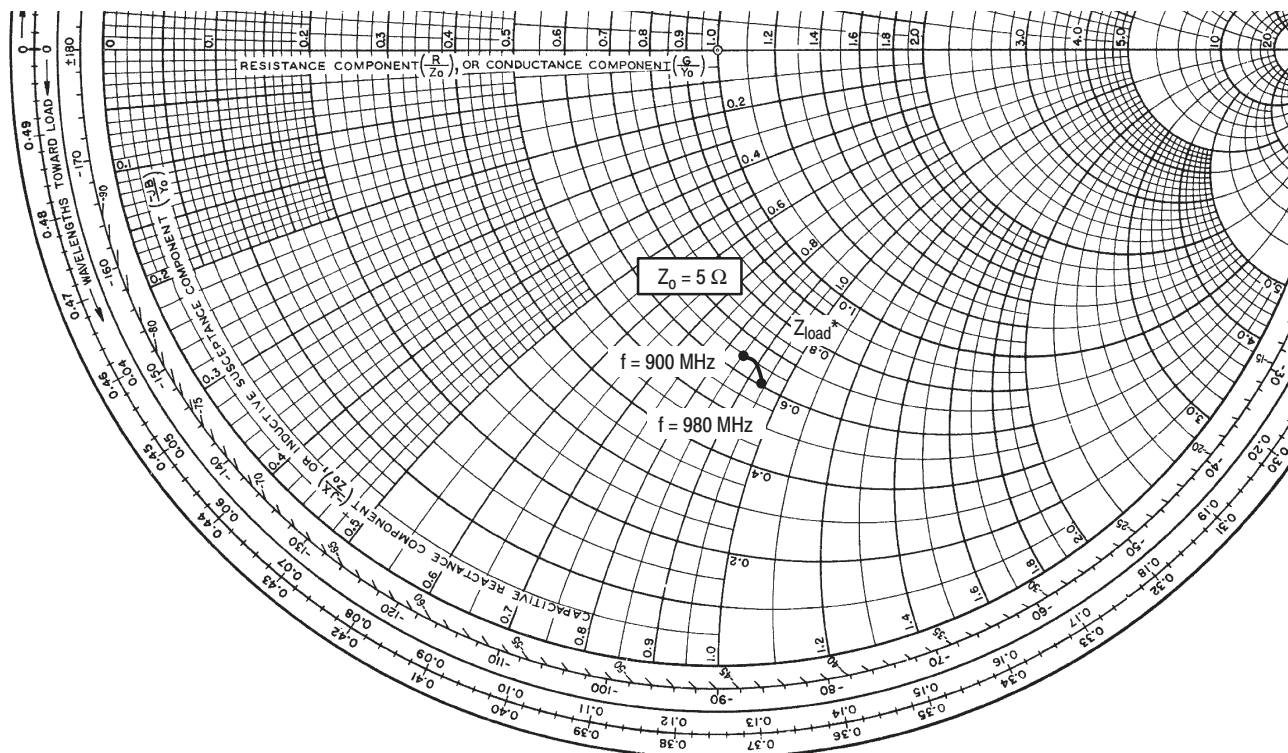


Figure 14. Spectral Regrowth at 600 kHz versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ1} = 60 \text{ mA}$, $I_{DQ2} = 240 \text{ mA}$, $P_{out} = P_{1dB}$

f MHz	Z_{load} Ω
900	$3.23 - j4.30$
910	$3.24 - j4.36$
920	$3.25 - j4.42$
930	$3.25 - j4.47$
940	$3.23 - j4.52$
950	$3.21 - j4.56$
960	$3.16 - j4.60$
970	$3.11 - j4.65$
980	$3.04 - j4.70$

Z_{load} = Test circuit impedance as measured from drain to ground.

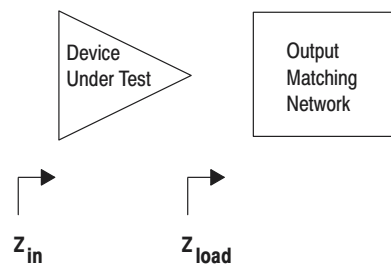


Figure 15. Series Equivalent Output Impedance

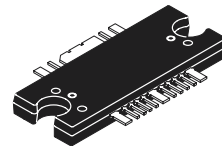
The RF Line RF LDMOS Integrated Power Amplifiers

The MWIC930 wideband integrated circuit is designed for CDMA and GSM/GSM EDGE applications. It uses Motorola's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On Chip integral matching circuitry makes it usable from 746 to 960 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, N-CDMA and W-CDMA.

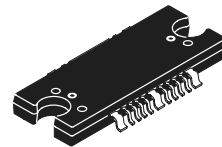
- Typical CDMA Performance: 27 Volts, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, 2-Carrier N-CDMA, IS -95, 869-894 MHz, 1.2288 MHz Channel Bandwidth, IM3 Measured in 1.2288 Integrated Bandwidth, ACPR Measured in 30 kHz Integrated Bandwidth, 2.5 MHz Carrier Spacing
Output Power — 5 Watts (Avg.)
Power Gain — 31 dB
Efficiency — 21%
Adjacent Channel Power — -52 dBc
IRL — -14 dB
- Typical Performance @ P1dB: 921-960 MHz, 26 Volts
Output Power — 30 Watts P1dB
Power Gain — 30 dB
Efficiency — 45%
- On Chip Matching (50 Ohm Input, >4 Ohm Output)
- Integrated Temperature Compensation Capability
- Integrated ESD Protection
- Usable for SCPA and MCPA Architecture
- Capable of Handling 5:1 VSWR, @ 26 Vdc, $f = 921$ MHz, $P_{out} = 30$ W CW, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA
- Can Be Bolted or Soldered through a Hole in the Circuit Board for Maximum Thermal Performance
- Also Available in Gull Wing for Surface Mount
- Available in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MWIC930R1 MWIC930GR1

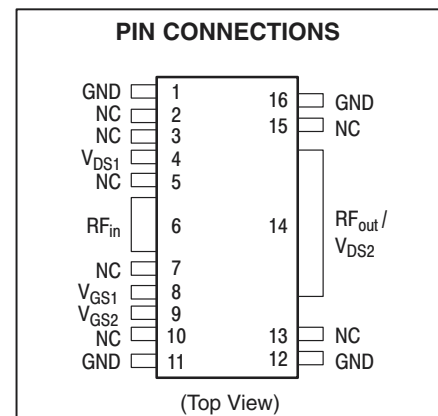
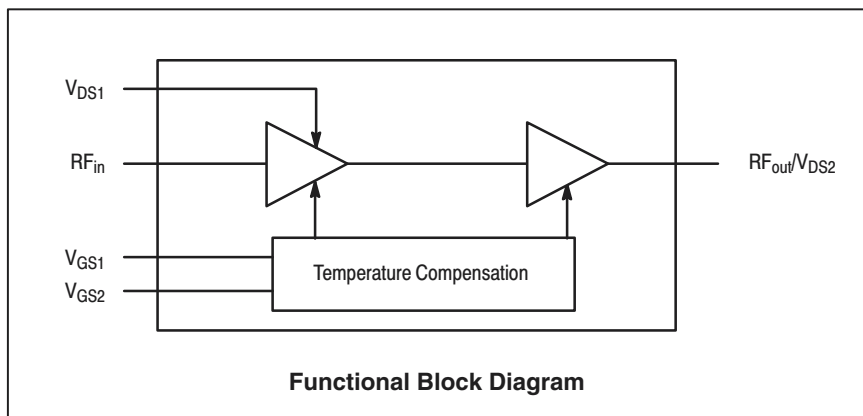
**N-CDMA, W-CDMA,
GSM/GSM EDGE, 746 – 960 MHz,
30 W, 26–28 V RF LDMOS
INTEGRATED POWER AMPLIFIERS**



**CASE 1329-08
TO-272 WIDE BODY MULTI-LEAD
PLASTIC
MWIC930R1**



**CASE 1329A-02
TO-272 WIDE BODY MULTI-LEAD
GULL WING
PLASTIC
MWIC930GR1**



REV 0

MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

**For More Information On This Product,
Go to: www.freescale.com**

MWIC930R1 MWIC930GR1

6-53

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Storage Temperature Range	T_{stg}	–65 to +175	°C
Operating Junction Temperature	T_J	175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
GSM Application ($P_{out} = 30$ W CW)	Stage 1, 27 Vdc, $I_{DQ} = 90$ mA Stage 2, 27 Vdc, $I_{DQ} = 240$ mA	1.22	
GSM EDGE Application ($P_{out} = 15$ W CW)	Stage 1, 27 Vdc, $I_{DQ} = 90$ mA Stage 2, 27 Vdc, $I_{DQ} = 240$ mA	1.39	
CDMA Application ($P_{out} = 5$ W CW)	Stage 1, 27 Vdc, $I_{DQ} = 90$ mA Stage 2, 27 Vdc, $I_{DQ} = 240$ mA	1.50	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C2 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22–A113	3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

CDMA FUNCTIONAL TESTS (In Motorola CDMA Test Fixture, 50 ohm system) 1–Carrier N–CDMA, 869–894 MHz, IS–95 CDMA Pilot, Sync, Paging, Traffic Codes 8 through 13.

Common–Source Amplifier Power Gain ($V_{DD} = 27$ Vdc, $P_{out} = 5$ W Avg., 1–Carrier N–CDMA, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f = 869$ – 894 MHz)	G_{ps}	28	31	—	dB
Drain Efficiency ($V_{DD} = 27$ Vdc, $P_{out} = 5$ W Avg., 1–Carrier N–CDMA, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f = 869$ – 894 MHz)	η	18	21	—	%
Adjacent Channel Power Ratio ($V_{DD} = 27$ Vdc, $P_{out} = 5$ W Avg., 1–Carrier N–CDMA, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f = 869$ – 894 MHz)	ACPR	—	–52	–48	dBc
Input Return Loss ($V_{DD} = 27$ Vdc, $P_{out} = 5$ W Avg., 1–Carrier N–CDMA, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f = 880$ MHz)	IRL	—	–12	–9	dB

(continued)

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

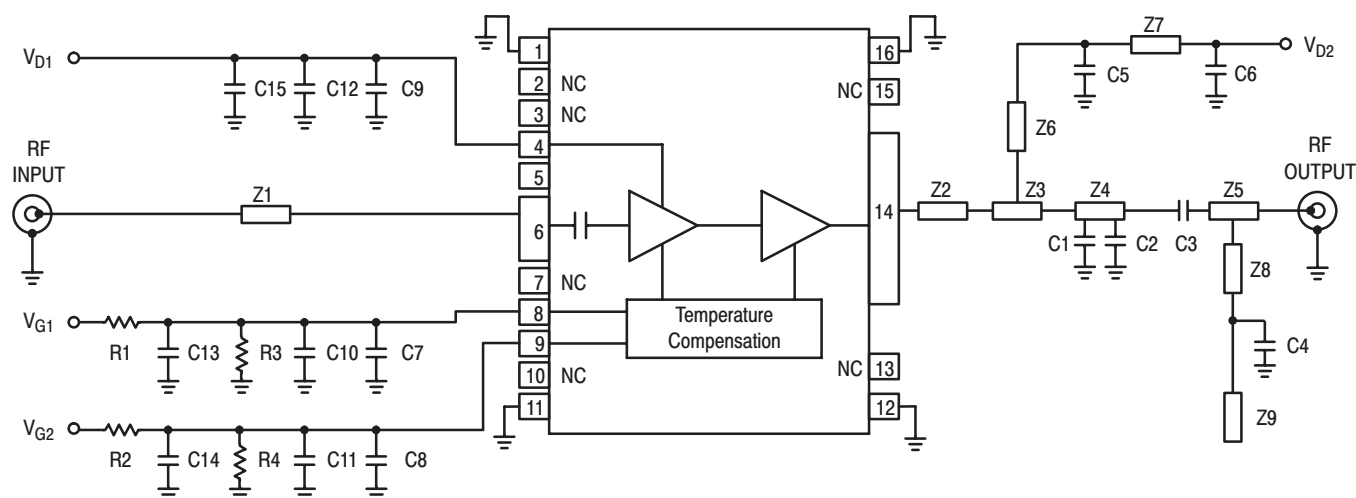
PERFORMANCE TESTS (In Motorola Test Fixture) V_{DS} = 26 V, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA

Quiescent Current Accuracy over Temperature (–10 to 85°C) at Nominal Value	ΔI_{QT}	—	±5	—	%
Gain Flatness in 80 MHz Bandwidth @ P _{out} = 5 W CW (Characterize from 840–920 MHz)	G _F	—	0.3	—	dB
Deviation from Linear Phase in 80 MHz Bandwidth @ P _{out} = 5 W CW (Characterize from 840–920 MHz)	Φ	—	0.6	—	°
Delay @ P _{out} = 5 W CW	Delay	—	3	—	ns
Insertion Phase Window @ P _{out} = 5 W CW	ΦΔ	—	±15	—	°

GSM/GSM EDGE FUNCTIONAL TESTS (In Motorola GSM Test Fixture) V_{DS} = 27 V, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, 921–960 MHz, CW

Output Power at 1dB Compression Point	P1dB	—	30	—	Watts
Common–Source Amplifier Power Gain @ P1dB	G _{ps}	—	30	—	dB
Drain Efficiency @ P1dB	η	—	45	—	%
Input Return Loss @ P1dB	IRL	—	–12	—	dB
Third Order Intermodulation Distortion (15 W, 2–Tone 100 kHz Spacing)	IMD3	—	–30	—	dBc
Third Order Intermodulation Distortion (1 W, 2–Tone 100 kHz Tone Spacing)	IMD3 backoff	—	–45	—	dBc
Gain Flatness 921–960 MHz @ P _{out} = 5 W CW	G _F	—	0.3	—	dB
Deviation from Linear Phase 921–960 MHz @ P _{out} = 5 W CW	Φ	—	0.6	—	°

Freescale Semiconductor, Inc.



Z1	0.0438" x 0.970" 50 Ω Microstrip (not including lead pad)	Z5	0.0438" x 0.2009" Microstrip
Z2	0.234" x 0.1183" Microstrip (including lead pad)	Z6	0.0504" x 0.528" Microstrip
Z3	0.1575" x 0.0938" Microstrip	Z7	0.0504" x 0.150" Microstrip
Z4	0.08425" x 0.584" Microstrip	Z8	0.0254" x 0.880" Microstrip
		Z9	0.0254" x 0.250" Microstrip
		PCB	Rogers 4350, 0.020", $\epsilon_r = 3.50$

Figure 1. 746–960 MHz Test Fixture Schematic

Table 1. 746–960 MHz Test Fixture Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
*C1	15 pF High Q Capacitor	ATC600S150JW	ATC
*C2	6.8 pF High Q Capacitor – GSM Fixture 8.2 pF High Q Capacitor – CDMA Fixture	ATC600S6R8CW ATC600S8R2CW	ATC
*C3	5.6 pF High Q Capacitor	ATC600S5R6CW	ATC
*C4, C5, C7, C8, C9	47 pF High Q Capacitors	ATC600S470JW	ATC
C6, C13, C14, C15	1 μ F Chip Capacitors	GRM42–2X7R105K050AL	Murata
C10, C11, C12	10 nF Chip Capacitors	C0603C103J5R	Kemet
R1, R2	1 k Ω , 1/8 W Chip Resistors	RM73B2AT102J	KOA Speer
R3, R4	1 M Ω , 1/4 W Chip Resistors	RM73B2BT105J	KOA Speer

* For output matching and bypass purposes, it is strongly recommended to use these exact capacitors.

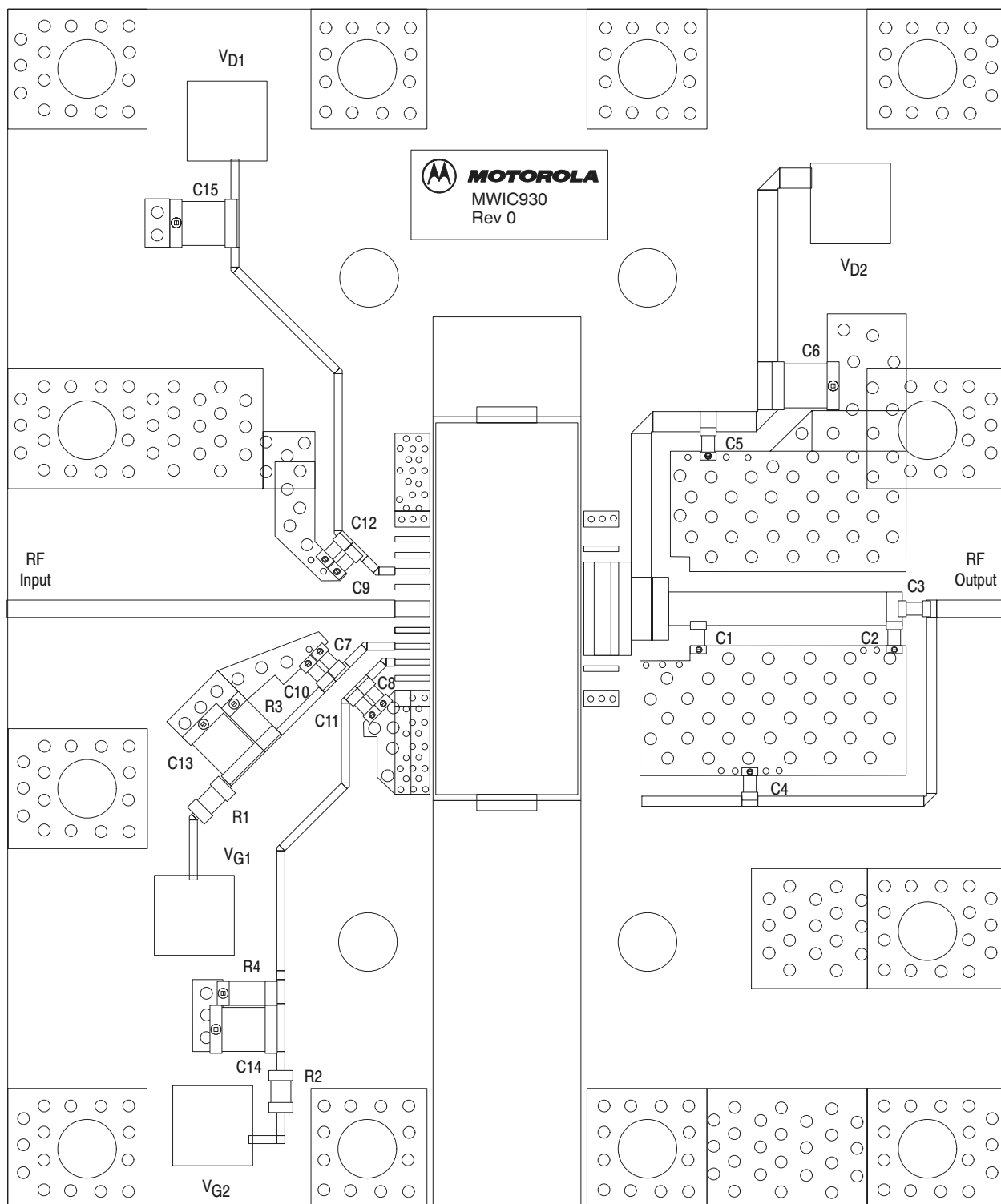


Figure 2. 746–960 MHz Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

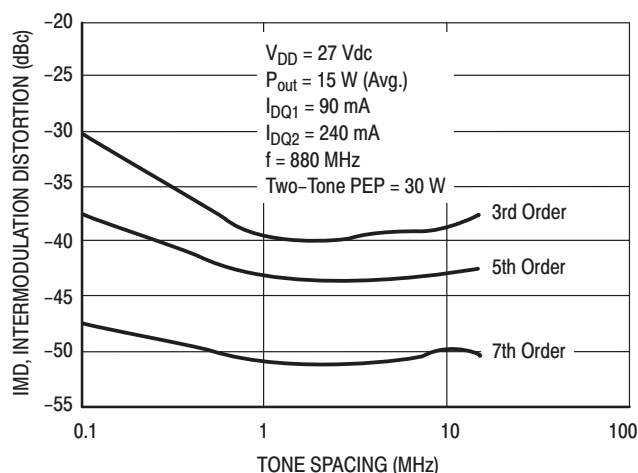


Figure 3. Two-Tone Broadband Performance

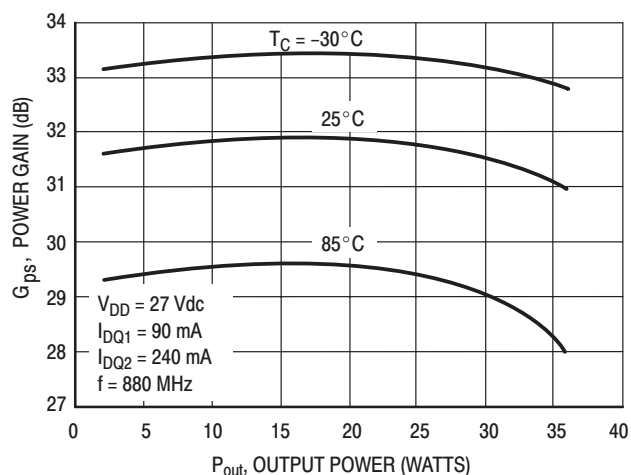


Figure 4. Power Gain versus Output Power

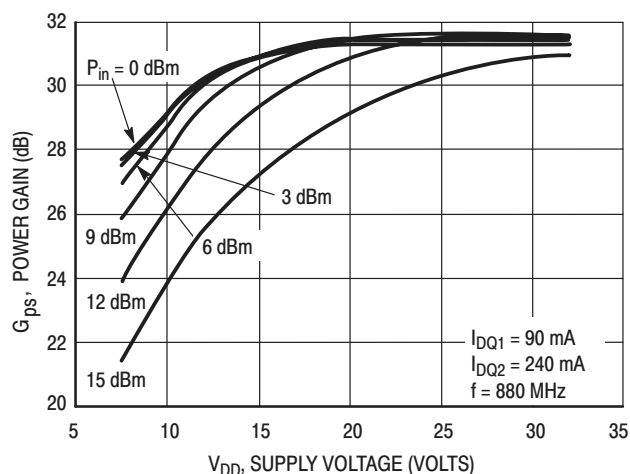


Figure 5. Power Gain versus Supply Voltage

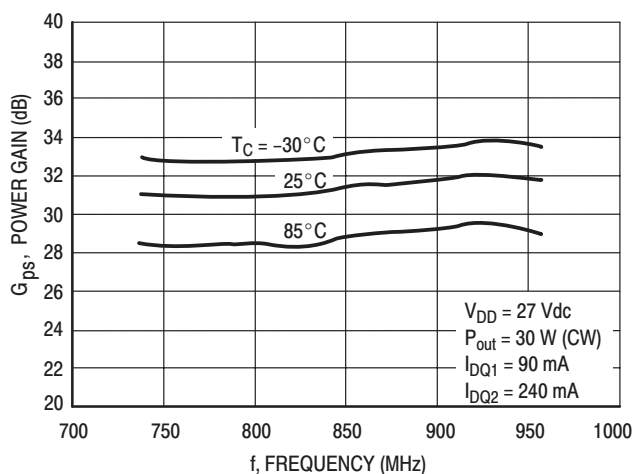


Figure 6. Power Gain versus Frequency

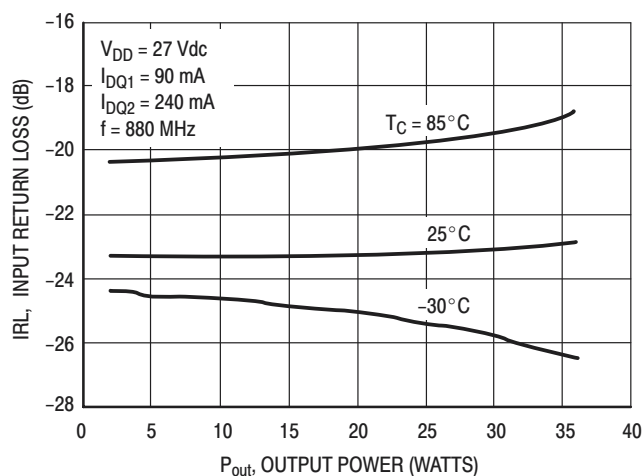


Figure 7. Input Return Loss versus Output Power

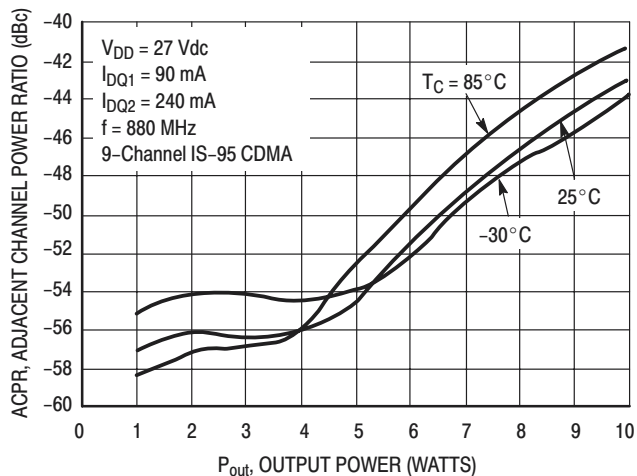


Figure 8. Adjacent Channel Power Ratio versus Output Power

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

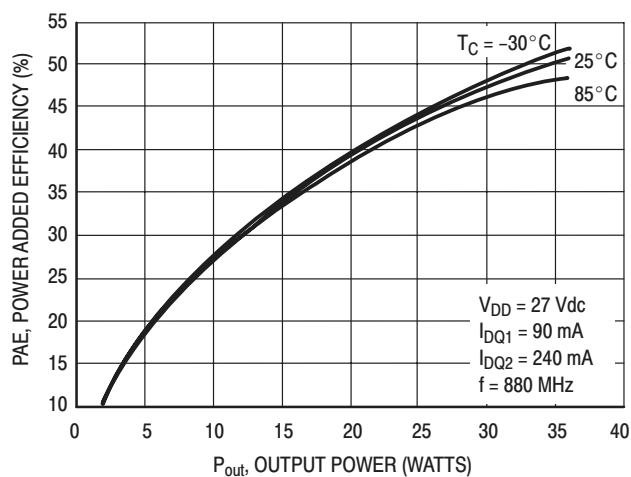


Figure 9. Power Added Efficiency versus Output Power

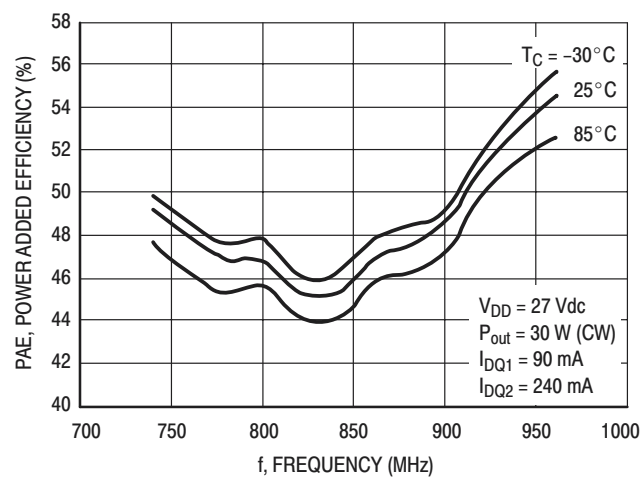
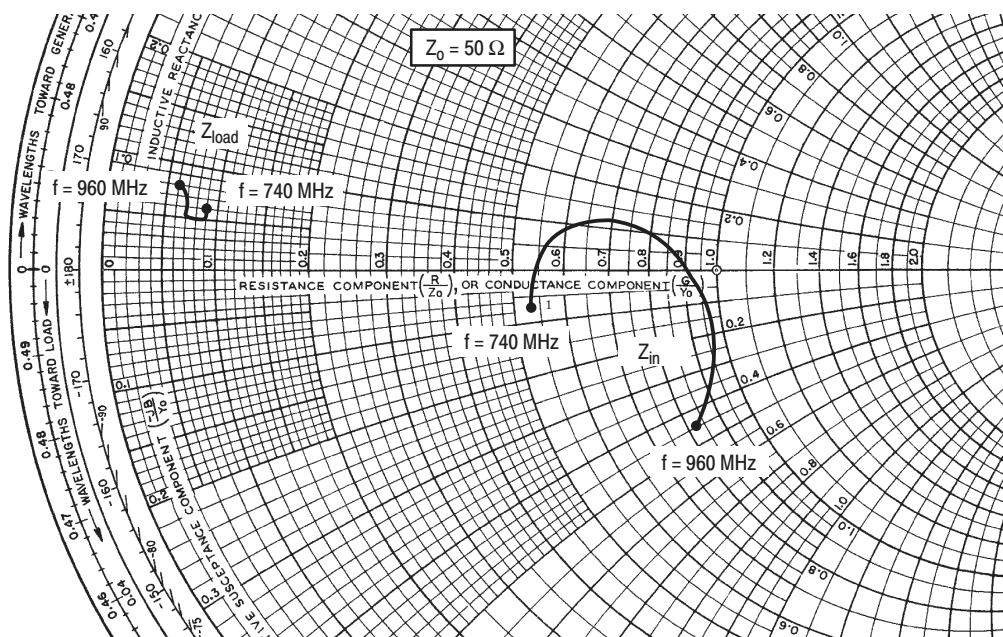


Figure 10. Power Added Efficiency versus Frequency



$V_{DD} = 27 \text{ Vdc}$, $I_{DQ1} = 90 \text{ mA}$, $I_{DQ2} = 240 \text{ mA}$, $P_{out} = 5 \text{ W Avg.}$

f MHz	Z_{in} Ω	Z_{load} Ω
740	$26.61 - j3.68$	$4.28 + j2.99$
760	$26.88 - j0.53$	$4.37 + j2.91$
780	$28.22 + j2.21$	$4.39 + j2.79$
800	$30.57 + j4.31$	$4.34 + j2.64$
820	$33.79 + j5.53$	$4.21 + j2.54$
840	$37.83 + j5.30$	$4.06 + j2.52$
860	$41.92 + j3.42$	$3.90 + j2.58$
880	$45.58 - j0.40$	$3.73 + j2.70$
900	$47.77 - j5.84$	$3.59 + j2.93$
920	$47.83 - j12.15$	$3.43 + j3.17$
940	$45.55 - j18.05$	$3.28 + j3.44$
960	$41.58 - j22.64$	$3.13 + j3.75$

Z_{in} = Device input impedance as measured from RF input to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

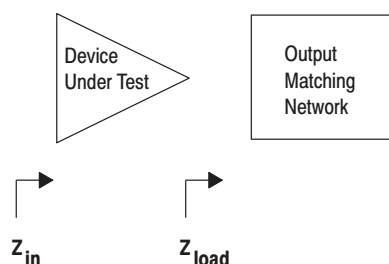


Figure 11. Series Equivalent Input and Output Impedance

The RF Line

General Purpose Linear Amplifier Module

Features

- 34.5 dB Typical Gain @ 100 MHz
- Silicon Bipolar Technology
- Class A Operation
- Typical ITO = +44 dBm @ 200 MHz
- Unconditionally Stable Under All Load Conditions

Applications

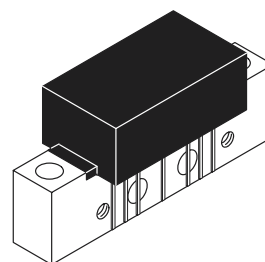
- Driver Amplifier in 50 Ohm Systems Requiring High Linearity
- Instrumentation Amplifiers
- Return Path Amplifier on CATV Systems Operating in the 10 to 200 MHz Frequency Range
- Possible Replacement for CA2830C

Description

- 24 Vdc Supply, 10 to 200 MHz, General Purpose Linear Amplifier Module

MHW1345

10–200 MHz
34.5 dB
800 mW
**GENERAL PURPOSE
LINEAR AMPLIFIER MODULE**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, $V_{CC} = 24\text{ V}$, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	200	MHz
Gain Flatness ($f = 10\text{--}200\text{ MHz}$)	G_F	—	± 0.5	± 1	dB
Power Gain ($f = 100\text{ MHz}$)	G_p	33.5	34.5	35.5	dB
Noise Figure, Broadband ($f = 200\text{ MHz}$)	NF	—	3.8	4.5	dB
Power Output — 1 dB Compression ($f = 10\text{--}200\text{ MHz}$)	P_{1dB}	630	800	—	mW
Power Output — 1 dB Compression ($f = 10\text{--}200\text{ MHz}$, $V_{CC} = 28\text{ V}$)	P_{1dB}	1000	1260	—	mW
Third Order Intercept (See Figure 2, $f_1 = 200\text{ MHz}$)	ITO	43	44	—	dBm
Input/Output VSWR ($f = 10\text{--}200\text{ MHz}$)	VSWR	—	1.5:1	2:1	—
Second Harmonic Distortion (Tone at 100 mW, $f_{2H} = 150\text{ MHz}$)	d_{so}	—	–60	–50	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 2) ($f = 10\text{--}200\text{ MHz}$ @ –32 dB IMD)	PEP	600	800	—	mW
Supply Current	I_{CC}	270	310	330	mA

REV 0

Freescale Semiconductor, Inc.

Biased at 24 Volts

T = 25°C Z_o = 50Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
10	-19.3	45.5	34.6	-0.6	-47.0	2.3	-14.5	76.8
50	-15.6	35.0	34.2	-56.7	-47.5	-30.3	-12.6	45.0
100	-13.2	34.4	33.9	-114	-47.9	-62.9	-10.8	10.7
200	-11.1	30.1	33.5	134	-48.3	-128	-14.9	-42.6

Magnitude in dB, Phase Angle in degrees.

Table 1. S-Parameters

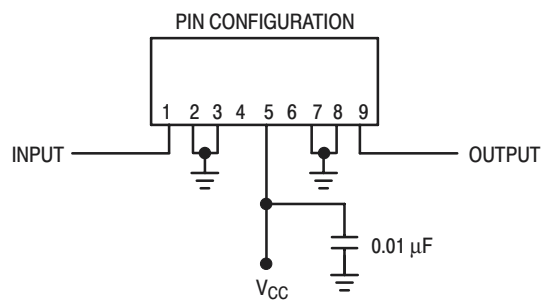
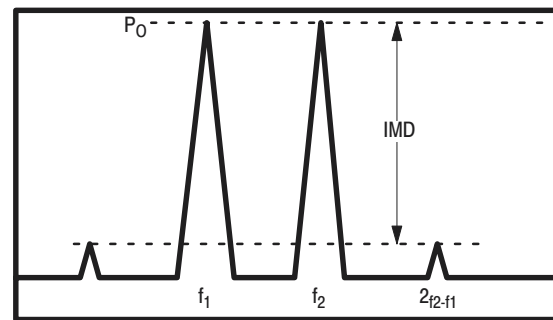


Figure 12. External Connections



$$ITO = P_0 + \frac{IMD}{2} @ IMD > 60dB$$

$$PEP = 4X P_0 @ IMD = -32dB$$

Figure 13. Intermodulation Test

Chapter Seven

Motorola RF CATV Distribution Amplifier
Modules – Data Sheets

Device Number	Page Number	Device Number	Page Number
MHW1223LA	7-3	MHW8185L	7-44
MHW1224LA	7-5	MHW8202B	7-46
MHW1244	7-7	MHW8205	7-48
MHW1253LA	7-9	MHW8205L	7-50
MHW1254L	7-11	MHW8222B	7-52
MHW1254LA	7-12	MHW8242A	7-54
MHW1303LA	7-14	MHW8272A	7-55
MHW1304LA	7-16	MHW9146	7-56
MHW1353LA	7-18	MHW9182B	7-58
MHW1354LA	7-20	MHW9186	7-59
MHW6342T	7-22	MHW9187	7-61
MHW7182B	7-24	MHW9188	7-63
MHW7185C	7-26	MHW9189	7-65
MHW7185CL	7-28	MHW9206	7-67
MHW7205C	7-30	MHW9227	7-69
MHW7205CL	7-32	MHW9236	7-71
MHW7222B	7-34	MHW9242A	7-73
MHW7242A	7-36	MHW9247	7-75
MHW7272A	7-38	MHW9267	7-77
MHW7292A	7-39	MHW9276	7-79
MHW8182B	7-40	MMG1001R2	7-81
MHW8185	7-42	MMG2001R2	7-86

The RF Line CATV Amplifier Module

Features

- Specified for 6- and 10-Channel Loading
- Excellent Distortion Performance
- Low Power Consumption
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

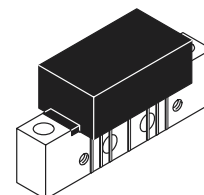
- CATV Systems Operating in the 5 to 200 MHz Frequency Range
- Specified for Use as a Return Path Amplifier for Low-, Mid- and High-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 200 MHz, CATV Reverse Amplifier

MHW1223LA

**5–200 MHz, 22.7 dB
10-CHANNEL
CATV LOW CURRENT AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth All	BW	5	—	200	MHz
Power Gain (f = 5 MHz)	G_p	22.1	22.7	23.5	dB
Slope (5–200 MHz)	S	– 0.2	—	0.7	dB
Gain Flatness (Peak To Valley) (5–200 MHz)	G_F	—	—	0.4	dB
Return Loss — Input/Output (@ f = 5–150 MHz) (@ f = 150–200 MHz)	IRL/ORL	20 18	— —	— —	dB
Composite Second Order ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CSO_6	—	– 73	– 68	
10-Channel FLAT	CSO_{10}	—	– 72	– 65	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	XMD_6	—	–69	–65	
10-Channel FLAT	XMD_{10}	—	–63	–60	
Composite Triple Beat ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CTB_6	—	–78	–75	
10-Channel FLAT	CTB_{10}	—	–69	–66	
Noise Figure ($f = 5$ –200 MHz)	NF	—	6.3	7	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line CATV Amplifier Module

Features

- Specified for 6- and 10-Channel Loading
- Excellent Distortion Performance
- Low Power Consumption
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

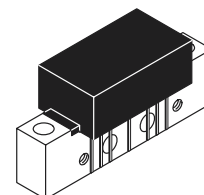
- CATV Systems Operating in the 5 to 65 MHz Frequency Range
- Specified for Use as a Return Path Amplifier for Low-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 65 MHz, CATV Reverse Amplifier

MHW1224LA

**5–65 MHz, 22.7 dB
10-CHANNEL
CATV LOW CURRENT AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth All	BW	5	—	65	MHz
Power Gain ($f = 5$ MHz)	G_p	22.1	22.7	23.2	dB
Slope (5–65 MHz)	S	– 0.2	—	0.5	dB
Gain Flatness (Peak To Valley) (5–65 MHz)	G_F	—	—	0.4	dB
Return Loss — Input/Output (@ $f = 5$ –65 MHz)	IRL/ORL	20	—	—	dB
Composite Second Order ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CSO_6	—	– 73	– 68	
10-Channel FLAT	CSO_{10}	—	– 72	– 65	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	XMD_6	—	–69	–65	
10-Channel FLAT	XMD_{10}	—	–63	–60	
Composite Triple Beat ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CTB_6	—	–78	–75	
10-Channel FLAT	CTB_{10}	—	–69	–66	
Noise Figure ($f = 5$ –65 MHz)	NF	—	6.3	7	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line CATV Amplifier Module

Features

- Specified for 12-, 22- and 26-Channel Loading
- Excellent Distortion Performance
- Superior Gain, Return Loss and DC Current Stability over Temperature
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

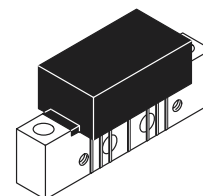
- CATV Systems Operating in the 5 to 200 MHz Frequency Range
- Designed for Broadband Applications Requiring Low Distortion Characteristics
- Specified for Use as a Return Path Amplifier for Low-, Mid- and High-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 200 MHz, CATV Reverse Amplifier

MHW1244

**5–200 MHz, 24.0 dB
26–CHANNEL
CATV HIGH–SPLIT
REVERSE AMPLIFIER**



CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^{\circ}\text{C}$, 75 Ω system)

Characteristic	Symbol	MHW1244	Units
Power Gain @ 10 MHz	G_p	24.0 ± 0.5	dB
Frequency Range (Response/Return Loss) (1)	BW	5.0–200	MHz
Cable Slope Equivalent (5.0–200 MHz)	S	–0.2 Min/+0.8 Max	dB
Gain Flatness (5.0–200 MHz)	G_F	± 0.2 Max	dB
Input/Output Return Loss (5.0–200 MHz) (1)	IRL/ORL	18.0 Min	dB
Cross Modulation Distortion @ +50 dBmV per ch. 12-Channel FLAT (5.0–120 MHz)	XMD_{12}	–66 Typ	dBc
22-Channel FLAT (5.0–175 MHz) (2) (3)	XMD_{22}	–61 Max	dBc
26-Channel FLAT (5.0–200 MHz)	XMD_{26}	–61 Typ	dBc

NOTES:

- Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
- Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22-channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7–Channels
2–6	55.25–83.25 MHz	5–Channels
A–7	121.25–175.25 MHz	10–Channels
- Video carriers used for 12-Channel typical performances are T7–6; For 26-Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22-Channel carriers listed above.

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system)

Characteristic	Symbol	MHW1244	Units
Composite Triple Beat Distortion @ +50 dBmV per ch. 22-Channel FLAT (5.0–175 MHz) (2) 26-Channel FLAT (5.0–200 MHz) (3)	CTB ₂₂ CTB ₂₆	–68 Max –67.5 Typ	dBc dBc
Individual Triple Beat Distortion @ +50 dBmV per ch. Mid-Split (5.0–120 MHz) T11, T12 and CH2 @ 123.25 MHz High-Split (5.0–175 MHz) T13, CH2 and CH5 @ 175.5 MHz	TB ₃ TB ₃	–87 Typ –84 Typ	dBc dBc
Second Order Distortion @ +50 dBmV per ch. High-Split (5.0–175 MHz) CH2, CHA @ 176.5 MHz	IMD	–72 Max	dBc
Noise Figure High-Split (5.0–175 MHz) (2)	NF	5.0 Max	dB
DC Current	I _{DC}	210 Typ/240 Max	mAdc

NOTES:

- Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
- Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22-channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7-Channels
2–6	55.25–83.25 MHz	5-Channels
A–7	121.25–175.25 MHz	10-Channels
- Video carriers used for 12-Channel typical performances are T7–6; For 26-Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22-Channel carriers listed above.

The RF Line CATV Amplifier Module

Features

- Specified for 6- and 10-Channel Loading
- Excellent Distortion Performance
- Low Power Consumption
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

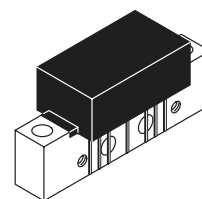
- CATV Systems Operating in the 5 to 200 MHz Frequency Range
- Specified for Use as a Return Path Amplifier for Low-, Mid- and High-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 200 MHz, CATV Reverse Amplifier

MHW1253LA

**5–200 MHz, 25.5 dB
10-CHANNEL
CATV LOW CURRENT AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth All	BW	5	—	200	MHz
Power Gain (f = 5 MHz)	G_p	25	25.5	26	dB
Slope (5–200 MHz)	S	– 0.2	—	0.7	dB
Gain Flatness (Peak To Valley) (5–200 MHz)	G_F	—	—	0.4	dB
Return Loss — Input/Output (@ f = 5–150 MHz) (@ f = 150–200 MHz)	IRL/ORL	20 18	— —	— —	dB
Composite Second Order ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CSO_6	—	– 73	– 68	
10-Channel FLAT	CSO_{10}	—	– 71	– 66	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	XMD_6	—	–69	–65	
10-Channel FLAT	XMD_{10}	—	–64	–61	
Composite Triple Beat ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CTB_6	—	–78	–75	
10-Channel FLAT	CTB_{10}	—	–69	–66	
Noise Figure ($f = 5$ –200 MHz)	NF	—	5.8	6.5	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line CATV Amplifier Module

Features

- Specified for 4-Channel Loading
- Superior Gain, Return Loss and DC Current Stability over Temperature
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

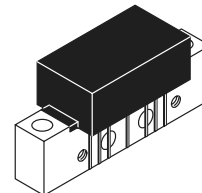
- CATV Systems Operating in the 5 to 50 MHz Frequency Range
- Specified for Use as a Return Path Amplifier for Low-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 50 MHz, CATV Reverse Amplifier

MHW1254L

**50 MHz, 25 dB
4-CHANNEL
CATV LOW CURRENT AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{IN}	+70	dBmV
Operating Case Temperature Range	T_C	- 20 to +100	°C
Storage Temperature Range	T_{stg}	- 40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 ohm system, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Bandwidth	BW	5.0	50	MHz
Power Gain (f = 5.0 MHz)	G_p	24.3	25.8	dB
Return Loss (@ f = 5.0-50 MHz)	RL	20	—	dB
Second Order Distortion ($V_{out} = +50$ dBmV/ch)	IMD	—	-70	dBc
Cross Modulation ($V_{out} = +50$ dBmV/ch)	XMD_4	—	-62	dBc
Triple Beat Distortion ($V_{out} = +50$ dBmV/ch)	TB_3	—	-70	dBc
Noise Figure (f = 50 MHz)	NF	—	4.5	dB
DC Current	IDC	100	135	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 6- and 10-Channel Loading
- Excellent Distortion Performance
- Low Power Consumption
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

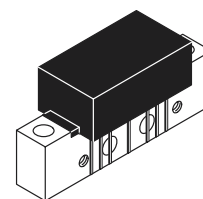
- CATV Systems Operating in the 5 to 65 MHz Frequency Range
- Specified for Use as a Return Path Amplifier for Low-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 65 MHz, CATV Reverse Amplifier

MHW1254LA

5–65 MHz, 25.5 dB
10-CHANNEL
CATV LOW CURRENT AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth All	BW	5	—	65	MHz
Power Gain (f = 5 MHz)	G_p	25	25.5	26	dB
Slope (5–65 MHz)	S	– 0.2	—	0.5	dB
Gain Flatness (Peak To Valley) (5–65 MHz)	G_F	—	—	0.4	dB
Return Loss — Input/Output (@ f = 5–65 MHz)	IRL/ORL	20	—	—	dB
Composite Second Order ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CSO_6	—	– 73	– 68	
10-Channel FLAT	CSO_{10}	—	– 71	– 66	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
	6-Channel FLAT	—	–69	–65	
	10-Channel FLAT	—	–64	–61	
Composite Triple Beat ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
	6-Channel FLAT	—	–78	–75	
	10-Channel FLAT	—	–69	–66	
Noise Figure ($f = 5$ –65 MHz)	NF	—	5.8	6.5	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 6- and 10-Channel Loading
- Excellent Distortion Performance
- Low Power Consumption
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

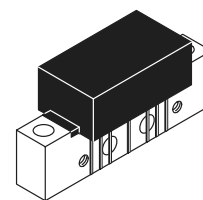
- CATV Systems Operating in the 5 to 200 MHz Frequency Range
- Specified for Use as a Return Path Amplifier for Low-, Mid- and High-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 200 MHz, CATV Reverse Amplifier

MHW1303LA

5–200 MHz, 30.8 dB
10-CHANNEL
CATV LOW CURRENT AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth All	BW	5	—	200	MHz
Power Gain (f = 5 MHz)	G_p	30	30.8	31.2	dB
Slope (5–200 MHz)	S	0	—	1.0	dB
Gain Flatness (Peak To Valley) (5–200 MHz)	G_F	—	—	0.7	dB
Return Loss — Input/Output (@ f = 5–65 MHz) (@ f = 65–200 MHz)	IRL/ORL	20 18	— —	— —	dB
Composite Second Order ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CSO_6	—	– 73	– 68	
10-Channel FLAT	CSO_{10}	—	– 70	– 65	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
	6-Channel FLAT	—	–67	–64	
	10-Channel FLAT	—	–61	–58	
Composite Triple Beat ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
	6-Channel FLAT	—	–76	–74	
	10-Channel FLAT	—	–67	–64	
Noise Figure ($f = 5$ –200 MHz)	NF	—	5	5.7	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 6- and 10-Channel Loading
- Excellent Distortion Performance
- Low Power Consumption
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

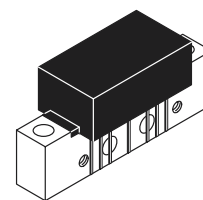
- CATV Systems Operating in the 5 to 65 MHz Frequency Range
- Specified for Use as a Return Path Amplifier for Low-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 65 MHz, CATV Reverse Amplifier

MHW1304LA

5–65 MHz, 30.8 dB
10-CHANNEL
CATV LOW CURRENT AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth All	BW	5	—	65	MHz
Power Gain (f = 5 MHz)	G_p	30	30.8	31.2	dB
Slope (5–65 MHz)	S	– 0.2	—	0.5	dB
Gain Flatness (Peak To Valley) (5–65 MHz)	G_F	—	—	0.5	dB
Return Loss — Input/Output (@ f = 5–65 MHz)	IRL/ORL	20	—	—	dB
Composite Second Order ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CSO_6	—	– 73	– 68	
10-Channel FLAT	CSO_{10}	—	– 70	– 65	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +50$ dBmV per Ch., Worst Case)	6-Channel FLAT	—	–67	–64	dBc
	10-Channel FLAT	—	–61	–58	
Composite Triple Beat ($V_{out} = +50$ dBmV per Ch., Worst Case)	6-Channel FLAT	—	–76	–74	dBc
	10-Channel FLAT	—	–67	–64	
Noise Figure ($f = 5$ –65 MHz)	NF	—	5	5.7	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 6- and 10-Channel Loading
- Excellent Distortion Performance
- Low Power Consumption
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

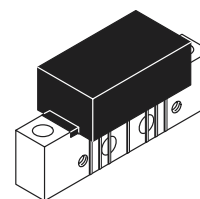
- CATV Systems Operating in the 5 to 150 MHz Frequency Range
- Specified for Use as a Return Path Amplifier for Low-, Mid- and High-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 150 MHz, CATV Reverse Amplifier

MHW1353LA

5–150 MHz, 35.2 dB
10-CHANNEL
CATV LOW CURRENT AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth All	BW	5	—	150	MHz
Power Gain (f = 5 MHz)	G_p	34.5	35.2	35.7	dB
Slope (5–150 MHz)	S	0	—	1	dB
Gain Flatness (Peak To Valley) (5–150 MHz)	G_F	—	—	0.7	dB
Return Loss — Input/Output (@ f = 5–65 MHz) (@ f = 65–150 MHz)	IRL/ORL	20 18	— —	— —	dB
Composite Second Order ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CSO_6	—	– 73	– 68	
10-Channel FLAT	CSO_{10}	—	– 69	– 65	

REV 1

MHW1353LA
7–18

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	XMD_6	—	–66	–63	
10-Channel FLAT	XMD_{10}	—	–60	–57	
Composite Triple Beat ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CTB_6	—	–75	–73	
10-Channel FLAT	CTB_{10}	—	–65	–62	
Noise Figure ($f = 5$ –150 MHz)	NF	—	4.4	5.4	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 6- and 10-Channel Loading
- Excellent Distortion Performance
- Low Power Consumption
- Capable of Handling Multiple Channels in the Return Path with Good Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

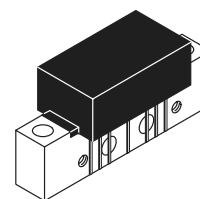
- CATV Systems Operating in the 5 to 65 MHz Frequency Range
- Specified for Use as a Return Path Amplifier for Low-Split 2-Way Cable TV Systems

Description

- 24 Vdc Supply, 5 to 65 MHz, CATV Reverse Amplifier

MHW1354LA

5–65 MHz, 35.2 dB
10-CHANNEL
CATV LOW CURRENT AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+60	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth All	BW	5	—	65	MHz
Power Gain (f = 5 MHz)	G_p	34.5	35.2	35.7	dB
Slope (5–65 MHz)	S	– 0.2	—	0.5	dB
Gain Flatness (Peak To Valley) (5–65 MHz)	G_F	—	—	0.5	dB
Return Loss — Input/Output (@ f = 5–65 MHz)	IRL/ORL	20	—	—	dB
Composite Second Order ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CSO_6	—	– 73	– 68	
10-Channel FLAT	CSO_{10}	—	– 69	– 65	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = 30^\circ\text{C}$, 75 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	XMD_6	—	–66	–63	
10-Channel FLAT	XMD_{10}	—	–60	–57	
Composite Triple Beat ($V_{out} = +50$ dBmV per Ch., Worst Case)					dBc
6-Channel FLAT	CTB_6	—	–75	–73	
10-Channel FLAT	CTB_{10}	—	–65	–62	
Noise Figure ($f = 5$ –65 MHz)	NF	—	4.4	5.4	dB
DC Current	I_{DC}	85	95	110	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77-Channel Loading
- Excellent Distortion Performance
- Superior Gain, Return Loss and DC Current Stability over Temperature
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

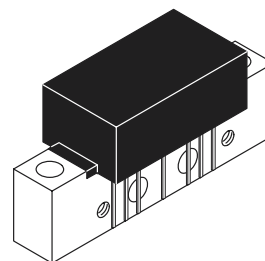
- CATV Systems Operating in the 40 to 550 MHz Frequency Range
- Single Module High Gain Line Amplifier in Cable TV Distribution System

Description

- 24 Vdc Supply, 40 to 550 MHz, CATV Forward Amplifier

MHW6342T

550 MHz
35.2 dB GAIN
77-CHANNEL
CATV AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^{\circ}\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	550	MHz
Power Gain 50 MHz 550 MHz	G_p	33.5 34.5	34.5 35.2	35.5 —	dB
Slope	S	0	0.7	2	dB
Gain Flatness (Peak To Valley)	G_F	—	0.3	0.8	dB
Return Loss — Input/Output ($Z_0 = 75$ Ohms) 40–550 MHz 450–550 MHz	IRL/ORL	18 16	— —	— —	dB
Second Order Intermodulation Distortion ($V_{out} = +46$ dBmV per ch., Ch 2, M13, M22) ($V_{out} = +44$ dBmV per ch., Ch 2, M30, M39)	IMD	— —	-80 -74	— —	dBc
Cross Modulation Distortion ($V_{out} = +46$ dBmV per ch.) ($V_{out} = +44$ dBmV per ch.) 60-Channel FLAT 77-Channel FLAT	XMD ₆₀ XMD ₇₇	— —	-62 -63	— -57	dBc

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24 \text{ Vdc}$, $T_C = +30^\circ\text{C}$, 75Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Composite Triple Beat ($V_{out} = +46 \text{ dBmV per ch.}$) 60-Channel FLAT ($V_{out} = +44 \text{ dBmV per ch.}$) 77-Channel FLAT	CTB ₆₀ CTB ₇₇	— —	−64 −63	— −57	dBc
Composite Second Order ($V_{out} = +46 \text{ dBmV/ch, 60-Channel FLAT}$) ($V_{out} = +44 \text{ dBmV/ch, 77-Channel FLAT}$)	CSO ₆₀ CSO ₇₇	— —	−70 −65	— −57	dBc
Noise Figure 550 MHz	NF	—	5.5	6.5	dB
DC Current	I _{DC}	—	310	340	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77- and 110-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

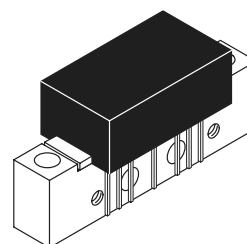
- CATV Systems Operating in the 40 to 750 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 750 MHz, CATV Forward Amplifier

MHW7182B

750 MHz
19 dB GAIN
110-CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	750	MHz
Power Gain 50 MHz 750 MHz	G_p	18 18.2	18.5 19	19 20	dB
Slope 40-750 MHz	S	0	0.4	1	dB
Gain Flatness (40-750 MHz, Peak to Valley)	G_F	—	0.3	0.6	dB
Return Loss — Input/Output ($Z_0 = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	20 —	— —	— 0.005	dB dB/MHz
Composite Second Order ($V_{out} = +40$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	CSO ₁₁₀ CSO ₇₇	— —	-70 -70	-63 -64	dBc

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion @ Ch 2 ($V_{out} = +40$ dBmV/ch., FM = 55 MHz) 110–Channel FLAT ($V_{out} = +44$ dBmV/ch., FM = 55 MHz) 77–Channel FLAT		XMD ₁₁₀	—	–66	–64	dBc
		XMD ₇₇	—	–61	–59	
Composite Triple Beat ($V_{out} = +40$ dBmV/ch., Worst Case) 110–Channel FLAT ($V_{out} = +44$ dBmV/ch., Worst Case) 77–Channel FLAT		CTB ₁₁₀	—	–68	–66	dBc
		CTB ₇₇	—	–66	–64	
Noise Figure	50 MHz	NF	—	4.0	5.0	dB
	550 MHz		—	4.5	—	
	750 MHz		—	5.0	6.5	
DC Current ($V_{DC} = 24$ V, $T_C = 30^\circ\text{C}$)		I _{DC}	180	220	240	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77- and 110-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

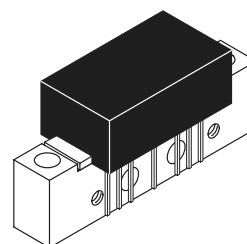
- CATV Systems Operating in the 40 to 750 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 750 MHz, CATV Forward Power Doubler Amplifier

MHW7185C

750 MHz
19.4 dB GAIN
110-CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	750	MHz
Power Gain 50 MHz 750 MHz	G_p	18.3 19	18.8 19.4	19.3 20	dB
Slope 40-750 MHz	S	0	0.4	1.0	dB
Gain Flatness (40-750 MHz, Peak to Valley)	G_F	—	0.3	0.6	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	19 —	— —	— 0.006	dB dB/MHz
Composite Second Order ($V_{out} = +44$ dBmV/ch., Worst Case) 110-Channel FLAT 77-Channel FLAT	CSO_{110} CSO_{77}	— —	-72 -80	-64 -68	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +44$ dBmV/ch., FM = 55 MHz) 110-Channel FLAT 77-Channel FLAT	XMD_{110} XMD_{77}	— —	-66 -70	-63 -68	dBc

REV 7

MHW7185C
7-26

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Triple Beat ($V_{out} = +44$ dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–64	–62	dBc
	77–Channel FLAT	CTB_{77}	—	–71	–69	
Noise Figure	50 MHz	NF	—	5.0	6.0	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	7.5	
DC Current ($V_{DC} = 24$ V, $T_C = 30^\circ\text{C}$)		I_{DC}	365	400	435	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77- and 110-Channel Loading
- Lower DC Current Requirements
- Excellent Distortion Performance
- Excellent DC Current Stability over Temperature
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

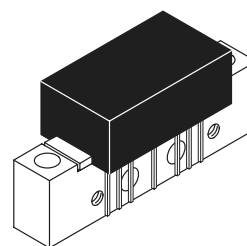
- CATV Systems Operating in the 40 to 750 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Amplifier Requiring Lower Power Dissipation While Maintaining Excellent Output Performance

Description

- 24 Vdc Supply, 40 to 750 MHz, CATV Forward Power Doubler Amplifier

MHW7185CL

750 MHz
19.2 dB GAIN
110-CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	750	MHz
Power Gain 50 MHz 750 MHz	G_p	18 18.7	18.5 19.2	19 19.7	dB
Slope 40–750 MHz	S	0.3	0.6	1.3	dB
Gain Flatness (40–750 MHz, Peak to Valley)	G_F	—	0.3	0.6	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order ($V_{out} = +44$ dBmV/ch., Worst Case) 110-Channel FLAT 77-Channel FLAT	CSO_{110} CSO_{77}	— —	-70 -83	-64 -68	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +44$ dBmV/ch., FM = 55 MHz) 110-Channel FLAT 77-Channel FLAT	XMD_{110} XMD_{77}	— —	-66 -69	-63 -67	dBc

REV 2

MHW7185CL
7-28

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Triple Beat ($V_{out} = +44$ dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–63.5	–61	dBc
	77–Channel FLAT	CTB_{77}	—	–70	–68	
Noise Figure	50 MHz	NF	—	5.3	6.2	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.5	7.5	
DC Current ($V_{DC} = 24$ V, $T_C = -20$ to $+100^\circ\text{C}$)		I_{DC}	345	370	385	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77- and 110-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

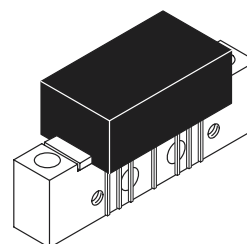
- CATV Systems Operating in the 40 to 750 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 750 MHz, CATV Forward Power Doubler Amplifier

MHW7205C

750 MHz
20.2 dB GAIN
110-CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	750	MHz
Power Gain 50 MHz 750 MHz	G_p	19.3 20	19.8 20.2	20.3 21	dB
Slope 40–750 MHz	S	0	0.4	1.0	dB
Gain Flatness (40–750 MHz, Peak to Valley)	G_F	—	0.3	0.6	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	19 —	— —	— 0.006	dB dB/MHz
Composite Second Order ($V_{out} = +44$ dBmV/ch., Worst Case) 110-Channel FLAT 77-Channel FLAT	CSO_{110} CSO_{77}	— —	-70 -80	-63 -68	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +44$ dBmV/ch., FM = 55 MHz) 110-Channel FLAT 77-Channel FLAT	XMD_{110} XMD_{77}	— —	-67 -70	-62 -68	dBc

REV 7

MHW7205C
7-30

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Triple Beat ($V_{out} = +44$ dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–63	–61	dBc
	77–Channel FLAT	CTB_{77}	—	–71	–69	
Noise Figure	50 MHz	NF	—	5.0	6.0	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	7.5	
DC Current ($V_{DC} = 24$ V, $T_C = 30^\circ\text{C}$)		I_{DC}	365	400	435	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77- and 110-Channel Loading
- Lower DC Current Requirements
- Excellent Distortion Performance
- Excellent DC Current Stability over Temperature
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

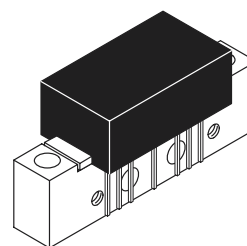
- CATV Systems Operating in the 40 to 750 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Amplifier Requiring Lower Power Dissipation While Maintaining Excellent Output Performance

Description

- 24 Vdc Supply, 40 to 750 MHz, CATV Forward Power Doubler Amplifier

MHW7205CL

750 MHz
20 dB GAIN
110-CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	750	MHz
Power Gain 50 MHz 750 MHz	G_p	19 19.7	19.5 20	20 21.2	dB
Slope 40–750 MHz	S	0.2	0.5	1.7	dB
Gain Flatness (40–750 MHz, Peak to Valley)	G_F	—	0.3	0.8	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order ($V_{out} = +44$ dBmV/ch., Worst Case) 110-Channel FLAT 77-Channel FLAT	CSO_{110} CSO_{77}	— —	-69 -80	-63 -67	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +44$ dBmV/ch., FM = 55 MHz) 110-Channel FLAT 77-Channel FLAT	XMD_{110} XMD_{77}	— —	-65 -69	-62 -66	dBc

REV 2

MHW7205CL
7-32

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Triple Beat ($V_{out} = +44$ dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–63	–61	dBc
	77–Channel FLAT	CTB_{77}	—	–70	–68	
Noise Figure	50 MHz	NF	—	5.0	6.2	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	7.5	
DC Current ($V_{DC} = 24$ V, $T_C = -20$ to $+100^\circ\text{C}$)		I_{DC}	345	365	385	mA

The RF Line

CATV Amplifier Module

Features

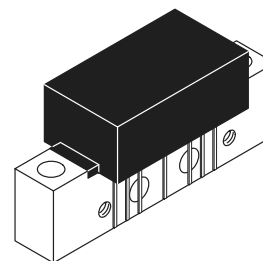
- Specified for 77- and 110-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

- CATV Systems Operating in the 40 to 750 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 750 MHz, CATV Forward Amplifier

MHW7222B
**750 MHz
22.7 dB GAIN
110-CHANNEL
CATV AMPLIFIER**

CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	750	MHz
Power Gain $f = 50$ MHz $f = 750$ MHz	G_p	21.4 22.2	21.9 22.7	22.4 23.2	dB
Slope ($f = 40$ –750 MHz)	S	0.2	0.7	1.2	—
Gain Flatness (Peak To Valley) ($f = 40$ –750 MHz)	G_F	—	0.4	0.6	—
Input/Output Return Loss @ $f = 40$ MHz	IRL/ORL	20	25	—	dB
Derate Return Loss @ $f > 40$ MHz	RLD	—	—	0.006	dB/MHz
Composite Second Order ($V_{out} = +40$ dBmV/ch; 110 Channels) ($V_{out} = +44$ dBmV/ch; 77 Channels)	CSO_{110} CSO_{77}	— —	-67 -67	-60 -60	dBc

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +40$ dBmV/ch, 110–Channel @ $F_m = 55.25$ MHz) ($V_{out} = +44$ dBmV/ch, 77–Channel @ $F_m = 55.25$ MHz)	XMD ₁₁₀ XMD ₇₇	— —	–63 –59	–60 –56	dBc
Composite Triple Beat ($V_{out} = +40$ dBmV/ch, 110–Channels, Worst Case) ($V_{out} = +44$ dBmV/ch, 77–Channels, Worst Case)	CTB ₁₁₀ CTB ₇₇	— —	–64 –65	–61 –62	dBc
Noise Figure f = 50 MHz f = 750 MHz	NF	— —	3.7 5	4.5 6.5	dB
DC Current	I _{DC}	180	220	240	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77- and 110-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

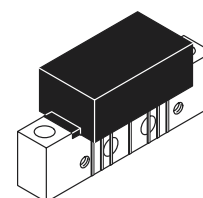
- CATV Systems Operating in the 40 to 750 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 750 MHz, CATV Forward Amplifier

MHW7242A

750 MHz
24.7 dB GAIN
110-CHANNEL
CATV AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	750	MHz
Power Gain	G_p	23.2	24	24.8	dB
		24	24.7	26	
Slope	S	0	0.6	1.5	dB
Gain Flatness (40–750 MHz, Peak To Valley)	G_F	—	0.4	0.6	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms)	IRL/ORL	20	—	—	dB
		—	—	0.007	dB/MHz
Composite Second Order					dBc
($V_{out} = +40$ dBmV/ch., Worst Case)	CSO_{110}	—	-69	-62	
($V_{out} = +44$ dBmV/ch., Worst Case)	CSO_{77}	—	-78	—	

REV 3

MHW7242A
 7-36

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion @ Ch 2 ($V_{out} = +40$ dBmV/ch., FM = 55 MHz) ($V_{out} = +44$ dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–63	–61	dBc
	77–Channel FLAT	XMD_{77}	—	–58	—	
Composite Triple Beat ($V_{out} = +40$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–67	–63	dBc
	77–Channel FLAT	CTB_{77}	—	–64	—	
Noise Figure	50 MHz	NF	—	4.8	5.5	dB
	750 MHz		—	5.5	7	
DC Current		I_{DC}	280	318	350	mA

The RF Line

CATV Amplifier Module

MHW7272A

Features

- Specified for 110-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

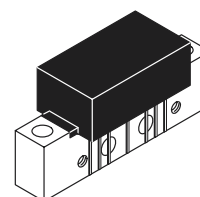
Applications

- CATV Systems Operating in the 40 to 750 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 750 MHz, CATV Forward Amplifier

750 MHz
27.7 dB GAIN
110-CHANNEL
CATV AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	750	MHz
Power Gain 50 MHz 750 MHz	G_p	26.2 27	27.2 27.7	27.8 29	dB
Slope 40-750 MHz	S	0	0.7	1.5	dB
Gain Flatness (40-750 MHz, Peak to Valley)	G_F	—	0.4	0.8	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order ($V_{out} = +40$ dBmV/ch., Worst Case) 110-Channel FLAT	CSO_{110}	—	-70	-64	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +40$ dBmV/ch., FM = 55 MHz) 110-Channel FLAT	XMD_{110}	—	-63	-60	dBc
Composite Triple Beat ($V_{out} = +40$ dBmV/ch., Worst Case) 110-Channel FLAT	CTB_{110}	—	-68	-64	dBc
Noise Figure 50 MHz 750 MHz	NF	— —	— 5.5	5.5 6.5	dB
DC Current ($V_{DC} = 24$ V, $T_C = 30^\circ\text{C}$)	I_{DC}	280	310	350	mA

The RF Line CATV Amplifier Module

Features

- Specified for 110-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

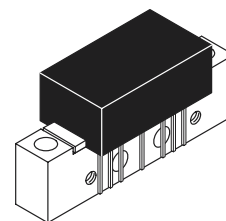
- CATV Systems Operating in the 40 to 770 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 770 MHz, CATV Forward Amplifier

MHW7292A

**770 MHz, 29.8 dB GAIN
110-CHANNEL
CATV AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	770	MHz
Power Gain 50 MHz 770 MHz	G_p	28.2 29	29 29.8	29.8 31	dB
Slope 40-770 MHz	S	0	0.7	2	dB
Gain Flatness (40-750 MHz, Peak to Valley)	G_F	—	0.4	0.8	dB
Return Loss — Input/Output ($Z_0 = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order ($V_{out} = +40$ dBmV/ch., Worst Case) 110-Channel FLAT	CSO_{110}	—	-70	-60	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +40$ dBmV/ch., FM = 55 MHz) 110-Channel FLAT	XMD_{110}	—	-62	-60	dBc
Composite Triple Beat ($V_{out} = +40$ dBmV/ch., Worst Case) 110-Channel FLAT	CTB_{110}	—	-62	-60	dBc
Noise Figure 50 MHz 770 MHz	NF	— —	— 5.5	5.5 6.5	dB
DC Current ($V_{DC} = 24$ V, $T_C = 30^\circ\text{C}$)	I_{DC}	280	310	350	mA

REV 1

The RF Line

CATV Amplifier Module

Features

- Specified for 77-, 110- and 128-Channel Loading
- Excellent Distortion Performance
- Superior Gain, Return Loss and DC Current Stability over Temperature
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

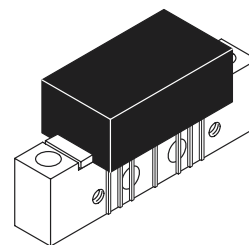
- CATV Systems Operating in the 40 to 860 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 860 MHz, CATV Forward Amplifier

MHW8182B

860 MHz
19.1 dB GAIN
128-CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G _p	18 18.2	18.5 19.1	19 20.5	dB
Slope	40–860 MHz	S	0	0.7	2.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		G _F	—	0.3	0.6	dB
Return Loss — Input/Output (Z ₀ = 75 Ohms) @ 40 MHz @ f > 40 MHz (Derate)		IRL/ORL	20 —	— —	— 0.005	dB dB/MHz
Composite Second Order (V _{out} = +38 dBmV/ch., Worst Case) 128–Channel FLAT (V _{out} = +40 dBmV/ch., Worst Case) 110–Channel FLAT (V _{out} = +44 dBmV/ch., Worst Case) 77–Channel FLAT		CSO ₁₂₈ CSO ₁₁₀ CSO ₇₇	— — —	–71 –70 –70	–64 –63 –64	dBc

REV 2

MHW8182B
7-40

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion @ Ch 2						dBc
($V_{out} = +38$ dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	–68	–65	
($V_{out} = +40$ dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–66	–64	
($V_{out} = +44$ dBmV/ch., FM = 55 MHz)	77–Channel FLAT	XMD_{77}	—	–61	–59	
Composite Triple Beat						dBc
($V_{out} = +38$ dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	–69	–66	
($V_{out} = +40$ dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–68	–66	
($V_{out} = +44$ dBmV/ch., Worst Case)	77–Channel FLAT	CTB_{77}	—	–66	–64	
Noise Figure	50 MHz	NF	—	4.0	5.0	dB
	550 MHz		—	4.5	—	
	750 MHz		—	5.0	6.5	
	860 MHz		—	5.5	7.5	
DC Current ($V_{DC} = 24$ V, $T_C = 30^\circ\text{C}$)		I_{DC}	180	220	240	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77–, 110– and 128–Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

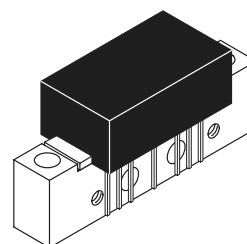
- CATV Systems Operating in the 40 to 860 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 860 MHz, CATV Forward Power Doubler Amplifier

MHW8185

860 MHz
19.4 dB GAIN
128–CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G _p	18.3 19	18.8 19.4	19.3 20.5	dB
Slope	40–860 MHz	S	0	.5	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		G _F	—	0.3	1.0	dB
Return Loss — Input/Output (Z _o = 75 Ohms) 						

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24 \text{ Vdc}$, $T_C = +30^\circ\text{C}$, 75Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Triple Beat ($V_{out} = +40 \text{ dBmV/ch.}$, Worst Case) ($V_{out} = +44 \text{ dBmV/ch.}$, Worst Case)	128–Channel FLAT	CTB_{128}	—	–67	–64	dBc
	110–Channel FLAT	CTB_{110}	—	–64	–62	
	77–Channel FLAT	CTB_{77}	—	–71	–69	
Noise Figure	50 MHz	NF	—	5.0	6.0	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	—	
	860 MHz		—	7.0	8.0	
DC Current ($V_{DC} = 24 \text{ V}$, $T_C = 30^\circ\text{C}$)		I_{DC}	365	400	435	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77-, 110- and 128-Channel Loading
- Lower DC Current Requirements
- Excellent Distortion Performance
- Excellent DC Current Stability over Temperature
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

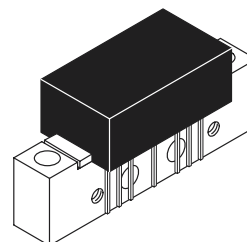
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Amplifiers Requiring Lower Power Dissipation While Maintaining Excellent Output Performance

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV Forward Power Doubler Amplifier

MHW8185L

870 MHz
19.4 dB GAIN
128-CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^{\circ}\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain	G_p	18	18.5	19	dB
50 MHz		19	19.4	20.5	
Slope	S	0.4	0.9	1.4	dB
40–870 MHz					
Gain Flatness (40–870 MHz, Peak-to-Valley)	G_F	—	0.3	0.8	dB
Return Loss — Input/Output ($Z_0 = 75$ Ohms)	IRL/ORL				
@ 40 MHz		20	—	—	dB
@ $f > 40$ MHz (Derate)		—	—	0.007	dB/MHz
Composite Second Order					dBc
($V_{out} = +40$ dBmV/ch., Worst Case) 128-Channel FLAT	CSO_{128}	—	-69	-62	
($V_{out} = +44$ dBmV/ch., Worst Case) 110-Channel FLAT	CSO_{110}	—	-70	-64	
($V_{out} = +44$ dBmV/ch., Worst Case) 77-Channel FLAT	CSO_{77}	—	-85	-68	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion @ Ch 2 ($V_{out} = +40$ dBmV/ch., FM = 55 MHz) ($V_{out} = +44$ dBmV/ch., FM = 55 MHz) ($V_{out} = +44$ dBmV/ch., FM = 55 MHz)	128-Channel FLAT	XMD_{128}	—	-72	-64	dBc
	110-Channel FLAT	XMD_{110}	—	-66	-63	
	77-Channel FLAT	XMD_{77}	—	-69	-67	
Composite Triple Beat ($V_{out} = +40$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	128-Channel FLAT	CTB_{128}	—	-66	-63	dBc
	110-Channel FLAT	CTB_{110}	—	-63	-61	
	77-Channel FLAT	CTB_{77}	—	-70	-68	
Noise Figure	50 MHz	NF	—	5.3	6.2	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.6	—	
	870 MHz		—	7.8	8.5	
DC Current ($V_{DC} = 24$ V, $T_C = -20$ to $+100^\circ\text{C}$)		I_{DC}	345	365	385	mA

The RF Line

CATV Amplifier Module

MHW8202B

Features

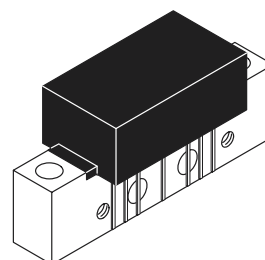
- Specified for 77–, 110– and 128–Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV Forward Amplifier

870 MHz
20.9 dB GAIN
128–CHANNEL
CATV AMPLIFIER

CASE 1302–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^{\circ}\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain $f = 50$ MHz $f = 870$ MHz	G_p	19.8 20.3	20.4 20.9	20.8 21.8	dB
Slope ($f = 40$ –870 MHz)	S	—	0.5	1.2	dB
Gain Flatness (Peak To Valley) ($f = 40$ –870 MHz)	G_F	—	0.4	0.6	dB
Input/Output Return Loss @ $f = 40$ MHz	IRL/ORL	20	21	—	dB
Derate Return Loss @ $f > 40$ MHz	RLD	—	—	0.005	dB/MHz
Composite Second Order ($V_{out} = +38$ dBmV/ch; 128–Channels, Worst Case) ($V_{out} = +40$ dBmV/ch; 110–Channels, Worst Case) ($V_{out} = +44$ dBmV/ch; 77–Channels, Worst Case)	CSO_{128} CSO_{110} CSO_{77}	— — —	–71 –70 –75	–66 –65 –70	dBc

REV 1

MHW8202B
7–46
For More Information On This Product,
Go to: www.freescale.com
MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +38$ dBmV/ch, 128-Channels, Worst Case) ($V_{out} = +40$ dBmV/ch, 110-Channels, Worst Case) ($V_{out} = +44$ dBmV/ch, 77-Channels, Worst Case)	XMD ₁₂₈ XMD ₁₁₀ XMD ₇₇	— — —	−67 −65 −58	−62 −61 −57	dBc
Composite Triple Beat ($V_{out} = +38$ dBmV/ch, 128-Channels, Worst Case) ($V_{out} = +40$ dBmV/ch, 110-Channels, Worst Case) ($V_{out} = +44$ dBmV/ch, 77-Channels, Worst Case)	CTB ₁₂₈ CTB ₁₁₀ CTB ₇₇	— — —	−67 −66 −65	−63 −63 −63	dBc
Noise Figure f = 50 MHz f = 750 MHz f = 870 MHz	NF	— — —	3.8 5.0 5.6	5.0 6.5 7.0	dB
DC Current	I _{DC}	180	220	240	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77-, 110- and 128-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

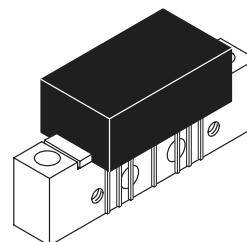
- CATV Systems Operating in the 40 to 860 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems

Description

- 24 Vdc Supply, 40 to 860 MHz, CATV Forward Power Doubler Amplifier

MHW8205

860 MHz
20.2 dB GAIN
128-CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	860	MHz
Power Gain	G_p	19.3	19.8	20.3	dB
		20	20.2	21.5	
Slope	S	0	.4	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)	G_F	—	0.3	1.0	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms)	IRL/ORL				
@ 40 MHz		19	—	—	dB
@ $f > 40$ MHz (Derate)		—	—	0.006	dB/MHz
Composite Second Order					dBc
($V_{out} = +40$ dBmV/ch., Worst Case) 128-Channel FLAT	CSO_{128}	—	-69	-60	
($V_{out} = +44$ dBmV/ch., Worst Case) 110-Channel FLAT	CSO_{110}	—	-70	-63	
77-Channel FLAT	CSO_{77}	—	-80	-68	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion @ Ch 2 ($V_{out} = +40$ dBmV/ch., FM = 55 MHz) ($V_{out} = +44$ dBmV/ch., FM = 55 MHz)	128-Channel FLAT	XMD_{128}	—	-72	-64	dBc
	110-Channel FLAT	XMD_{110}	—	-67	-62	
	77-Channel FLAT	XMD_{77}	—	-71	-68	
Composite Triple Beat ($V_{out} = +40$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	128-Channel FLAT	CTB_{128}	—	-66	-63	dBc
	110-Channel FLAT	CTB_{110}	—	-63	-61	
	77-Channel FLAT	CTB_{77}	—	-71	-69	
Noise Figure	50 MHz	NF	—	5.0	6.0	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	—	
	860 MHz		—	7.0	8.0	
DC Current ($V_{DC} = 24$ V, $T_C = 30^\circ\text{C}$)		I_{DC}	365	400	435	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77–, 110– and 128–Channel Loading
- Lower DC Current Requirements
- Excellent Distortion Performance
- Excellent DC Current Stability over Temperature
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

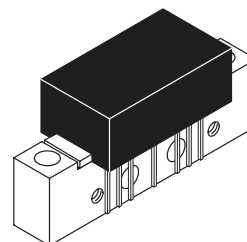
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Amplifiers Requiring Lower Power Dissipation While Maintaining Excellent Output Performance

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV Forward Power Doubler Amplifier

MHW8205L

870 MHz
20.4 dB GAIN
128–CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 50 MHz 870 MHz	G_p	19 19.8	19.5 20.4	20 21.3	dB
Slope 40–870 MHz	S	0.2	0.8	1.7	dB
Gain Flatness (40–870 MHz, Peak to Valley)	G_F	—	0.5	1.0	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order ($V_{out} = +40$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	CSO ₁₂₈ CSO ₁₁₀ CSO ₇₇	— — —	–69 –70 –80	–60 –63 –67	dBc

REV 2

MHW8205L
7–50

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion @ Ch 2 ($V_{out} = +40$ dBmV/ch., FM = 55 MHz) ($V_{out} = +44$ dBmV/ch., FM = 55 MHz)	128-Channel FLAT	XMD_{128}	—	−72	−64	dBc
	110-Channel FLAT	XMD_{110}	—	−65	−62	
	77-Channel FLAT	XMD_{77}	—	−69	−66	
Composite Triple Beat ($V_{out} = +40$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	128-Channel FLAT	CTB_{128}	—	−66	−63	dBc
	110-Channel FLAT	CTB_{110}	—	−63	−61	
	77-Channel FLAT	CTB_{77}	—	−70	−68	
Noise Figure	50 MHz	NF	—	5.0	6.2	dB
	550 MHz		—	5.8	—	
	750 MHz		—	6.2	—	
	870 MHz		—	7.7	8.5	
DC Current ($V_{DC} = 24$ V, $T_C = -20^\circ\text{C}$ to $+100^\circ\text{C}$)		I_{DC}	345	365	385	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77-, 110- and 128-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

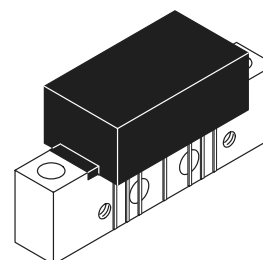
- CATV Systems Operating in the 40 to 860 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 860 MHz, CATV Forward Amplifier

MHW8222B

860 MHz
22.7 dB GAIN
128-CHANNEL
CATV AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	860	MHz
Power Gain f = 50 MHz f = 860 MHz	G_p	21.4 21.8	21.9 22.7	22.4 24	dB
Slope (f = 40–860 MHz)	S	0.1	0.8	1.5	—
Gain Flatness (Peak To Valley) (f = 40–860 MHz)	G_F	—	0.4	0.6	—
Input/Output Return Loss @ f = 40 MHz	IRL/ORL	20	24	—	dB
Derate Return Loss @ f > 40 MHz	RLD	—	—	0.009	dB/MHz
Composite Second Order ($V_{out} = +38$ dBmV/ch; 128 Channels) ($V_{out} = +40$ dBmV/ch; 110 Channels) ($V_{out} = +44$ dBmV/ch; 77 Channels)	CSO_{128} CSO_{110} CSO_{77}	— — —	-68 -64 -65	-60 -61 -62	dBc

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 24 \text{ Vdc}$, $T_C = +30^\circ\text{C}$, 75Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion ($V_{out} = +38 \text{ dBmV/ch}$, 128-Channel @ $F_m = 55.25 \text{ MHz}$) ($V_{out} = +40 \text{ dBmV/ch}$, 110-Channel @ $F_m = 55.25 \text{ MHz}$) ($V_{out} = +44 \text{ dBmV/ch}$, 77-Channel @ $F_m = 55.25 \text{ MHz}$)	XMD ₁₂₈ XMD ₁₁₀ XMD ₇₇	— — —	—65 —63 —59	—63 —60 —56	dBc
Composite Triple Beat ($V_{out} = +38 \text{ dBmV/ch}$, 128-Channels, Worst Case) ($V_{out} = +40 \text{ dBmV/ch}$, 110-Channels, Worst Case) ($V_{out} = +44 \text{ dBmV/ch}$, 77-Channels, Worst Case)	CTB ₁₂₈ CTB ₁₁₀ CTB ₇₇	— — —	—66 —64 —65	—64 —61 —62	dBc
Noise Figure f = 50 MHz f = 750 MHz f = 860 MHz	NF	— — —	3.7 5 5.6	4.5 6.5 7	dB
DC Current	I _{DC}	180	220	240	mA

The RF Line

CATV Amplifier Module

Features

- Specified for 77- and 128-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

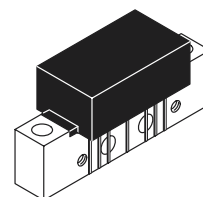
- CATV Systems Operating in the 40 to 860 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 860 MHz, CATV Forward Amplifier

MHW8242A

860 MHz
25 dB GAIN
128-CHANNEL
CATV AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	860	MHz
Power Gain	G_p	23.2	24	24.8	dB
		24	25	26	
Slope	S	0	0.8	1.8	dB
Gain Flatness (40–860 MHz, Peak To Valley)	G_F	—	0.4	0.8	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms)	IRL/ORL	20	—	—	dB
		—	—	0.007	dB/MHz
Composite Second Order					dBc
($V_{out} = +38$ dBmV/ch., Worst Case)	CSO_{128}	—	-69	-62	
($V_{out} = +44$ dBmV/ch., Worst Case)	CSO_{77}	—	-78	—	
Cross Modulation Distortion @ Ch 2	XMD_{128}	—	-65	-62	dBc
($V_{out} = +38$ dBmV/ch., FM = 55 MHz)	XMD_{77}	—	-58	—	
($V_{out} = +44$ dBmV/ch., FM = 55 MHz)					
Composite Triple Beat	CTB_{128}	—	-68	-64	dBc
($V_{out} = +38$ dBmV/ch., Worst Case)	CTB_{77}	—	-64	—	
($V_{out} = +44$ dBmV/ch., Worst Case)					
Noise Figure	NF	—	4.8	5.5	dB
		—	5.8	7.5	
DC Current	I_{DC}	280	318	350	mA

REV 4

MHW8242A
7-54

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

The RF Line CATV Amplifier Module

Features

- Specified for 128-Channel Loading
- Excellent Distortion Performance
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

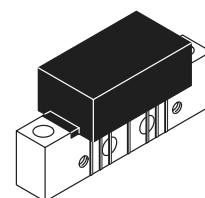
- CATV Systems Operating in the 40 to 860 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 860 MHz, CATV Forward Amplifier

MHW8272A

**860 MHz
27.7 dB GAIN
128-CHANNEL
CATV AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	860	MHz
Power Gain 50 MHz 860 MHz	G_p	26.2 27	27.2 27.7	27.8 29.5	dB
Slope 40-860 MHz	S	0	0.6	2	dB
Gain Flatness (40-860 MHz, Peak to Valley)	G_F	—	0.4	0.8	dB
Return Loss — Input/Output ($Z_0 = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order ($V_{out} = +38$ dBmV/ch., Worst Case) 128-Channel FLAT	CSO_{128}	—	-69	-64	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +38$ dBmV/ch., FM = 55 MHz) 128-Channel FLAT	XMD_{128}	—	-65	-62	dBc
Composite Triple Beat ($V_{out} = +38$ dBmV/ch., Worst Case) 128-Channel FLAT	CTB_{128}	—	-69	-64	dBc
Noise Figure 50 MHz 860 MHz	NF	— —	— 6.0	5.5 7.0	dB
DC Current ($V_{DC} = 24$ V, $T_C = 30^\circ\text{C}$)	I_{DC}	280	310	350	mA

The RF Line

Gallium Arsenide

CATV Amplifier Module

MHW9146

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

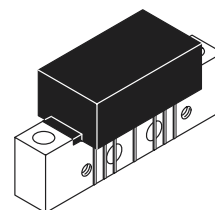
Applications

- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Output Stage Amplifier on Applications Requiring Low Power Dissipation and High Output Performance
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV GaAs Forward Amplifier Module

870 MHz
14.3 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER MODULE


CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	200	200	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 870 MHz	G_p	13.8	14.3	14.8	dB
Slope 40-870 MHz	S	0	0.4	1.0	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	G_F	—	—	0.5	dB
Return Loss — Input ($Z_o = 75$ Ohms)	IRL	20 18	— —	— —	dB
Return Loss — Output ($Z_o = 75$ Ohms)	ORL	20 18	— —	— —	dB

REV 1

 MHW9146
 7-56

For More Information On This Product,
Go to: www.freescale.com

 MOTOROLA WIRELESS
 RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Second Order ($V_{out} = +48$ dBmV/ch., Worst Case) ($V_{out} = +46$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	79–Channel FLAT	CSO_{79}	—	–68	–64	dBc
	112–Channel FLAT	CSO_{112}	—	–63	–60	
	132–Channel FLAT	CSO_{132}	—	–63	–60	
Cross Modulation Distortion @ Ch 2 ($V_{out} = +48$ dBmV/ch., FM = 55.25 MHz) ($V_{out} = +46$ dBmV/ch., FM = 55.25 MHz) ($V_{out} = +44$ dBmV/ch., FM = 55.25 MHz)	79–Channel FLAT	XMD_{79}	—	–60	–55	dBc
	112–Channel FLAT	XMD_{112}	—	–60	–55	
	132–Channel FLAT	XMD_{132}	—	–60	–55	
Composite Triple Beat ($V_{out} = +48$ dBmV/ch., Worst Case) ($V_{out} = +46$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	79–Channel FLAT	CTB_{79}	—	–64	–60	dBc
	112–Channel FLAT	CTB_{112}	—	–64	–60	
	132–Channel FLAT	CTB_{132}	—	–64	–60	
Noise Figure	50 MHz	NF	—	4.4	5.5	dB
	550 MHz		—	3.8	—	
	750 MHz		—	4.0	—	
	870 MHz		—	4.3	5.5	
DC Current ($V_{DC} = 24$ V, $T_C = 45^\circ\text{C}$)		I_{DC}	230	245	260	mA

NOTE: This device requires an external 0.01 μF DC blocking capacitor connected to the output pin (Pin 9) as indicated in Figure 1.

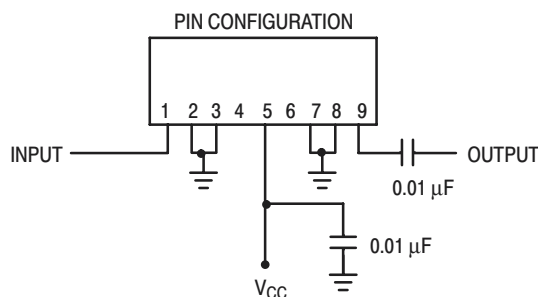


Figure 14. External Connections

The RF Line

CATV Amplifier Module

MHW9182B

Features

- Specified for 110- and 152-Channel Loading
- Excellent Distortion Performance
- Superior Gain, Return Loss and DC Current Stability over Temperature
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

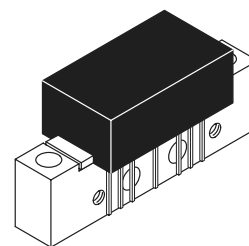
Applications

- CATV Systems Operating in the 40 to 1000 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 1000 MHz, CATV Forward Amplifier

1000 MHz
19.4 dB GAIN
152-CHANNEL
CATV AMPLIFIER



CASE 714Y-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	1000	MHz
Power Gain 50 MHz 1000 MHz	G_p	18 18.7	18.5 19.4	19 20.7	dB
Slope 40–1000 MHz	S	0.4	0.9	1.4	dB
Gain Flatness (40–1000 MHz, Peak to Valley)	G_F	—	0.4	0.8	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms) @ 40 MHz @ $f > 40$ MHz (Derate)	IRL/ORL	20 —	— —	— 0.006	dB dB/MHz
Composite Second Order ($V_{out} = +40$ dBmV/ch., Worst Case) ($V_{out} = +38$ dBmV/ch., Worst Case)	CSO ₁₁₀ CSO ₁₅₂	— —	70 -69	-63 -63	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +40$ dBmV/ch., FM = 55 MHz) ($V_{out} = +38$ dBmV/ch., FM = 55 MHz)	XMD ₁₁₀ XMD ₁₅₂	— —	-66 -65	-64 -61	dBc
Composite Triple Beat ($V_{out} = +40$ dBmV/ch., Worst Case) ($V_{out} = +38$ dBmV/ch., Worst Case)	CTB ₁₁₀ CTB ₁₅₂	— —	-68 -64	-66 -61	dBc
Noise Figure 50 MHz 550 MHz 860 MHz 1000 MHz	NF	— — — —	4.0 4.5 5.5 6.0	5.0 — — 7.5	dB
DC Current ($V_{DC} = 24$ V, $T_C = 30^\circ\text{C}$)	I_{DC}	180	210	240	mA

REV 2

MHW9182B
7-58

For More Information On This Product,
Go to: www.freescale.com

MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

The RF Line

Gallium Arsenide

CATV Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

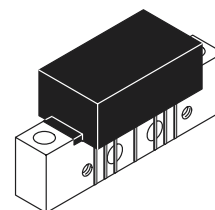
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Output Stage Amplifier on Applications Requiring Low Power Dissipation and High Output Performance
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV GaAs Forward Amplifier

MHW9186

870 MHz
18.5 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	300	300	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain	G_p	17.5	18	18.5	dB
		18	18.5	19.5	
Slope	S	0.2	0.6	1.2	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	G_F	—	0.3	0.8	dB
Return Loss — Input ($Z_0 = 75$ Ohms)	IRL	20	—	—	dB
		19	—	—	
		18	—	—	
Return Loss — Output ($Z_0 = 75$ Ohms)	ORL	20	—	—	dB
		19	—	—	
		18	—	—	

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Second Order ($V_{out} = +44$ dBmV/ch., Worst Case) ($V_{out} = +46$ dBmV/ch., Worst Case) ($V_{out} = +48$ dBmV/ch., Worst Case)	132–Channel FLAT	CSO_{132}	—	–67	–60	dBc
	112–Channel FLAT	CSO_{112}	—	–65	–61	
	79–Channel FLAT	CSO_{79}	—	–72	–64	
Cross Modulation Distortion @ Ch 2 ($V_{out} = +44$ dBmV/ch., FM = 55 MHz) ($V_{out} = +46$ dBmV/ch., FM = 55 MHz) ($V_{out} = +48$ dBmV/ch., FM = 55 MHz)	132–Channel FLAT	XMD_{132}	—	–58	–52	dBc
	112–Channel FLAT	XMD_{112}	—	–58	–52	
	79–Channel FLAT	XMD_{79}	—	–58	–52	
Composite Triple Beat ($V_{out} = +44$ dBmV/ch., Worst Case) ($V_{out} = +46$ dBmV/ch., Worst Case) ($V_{out} = +48$ dBmV/ch., Worst Case)	132–Channel FLAT	CTB_{132}	—	–62	–58	dBc
	112–Channel FLAT	CTB_{112}	—	–61	–58	
	79–Channel FLAT	CTB_{79}	—	–64	–60	
Noise Figure	50 MHz	NF	—	4	5.0	dB
	870 MHz		—	3.7	5.0	
DC Current ($V_{DC} = 24$ V, $T_C = -20^\circ$ to $+100^\circ\text{C}$)		I_{DC}	230	250	265	mA

The RF Line

Gallium Arsenide

CATV Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Higher Output Capability
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

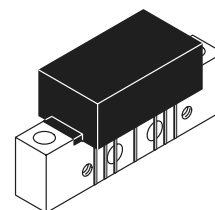
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV GaAs Forward Power Doubler Amplifier

MHW9187

**870 MHz
20 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	200	200	V
Human Body Model per Mil. Std. 1686	0.7	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 870 MHz	G_p	19.4	20	20.6	dB
Slope 40-870 MHz	S	0	0.5	1.0	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	G_F	—	—	0.5	dB
Return Loss — Input ($Z_o = 75$ Ohms)	IRL	20 18 16	— — —	— — —	dB
Return Loss — Output ($Z_o = 75$ Ohms)	ORL	20 18	— —	— —	dB

REV 2

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24 \text{ Vdc}$, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Composite Second Order					dBc
($V_{out} = +48 \text{ dBmV/ch.}$, Worst Case) 132–Channel FLAT	CSO_{132}	—	–64	–62	
($V_{out} = +48 \text{ dBmV/ch.}$, Worst Case) 112–Channel FLAT	CSO_{112}	—	–66	–64	
($V_{out} = +48 \text{ dBmV/ch.}$, Worst Case) 79–Channel FLAT	CSO_{79}	—	–70	–68	
($V_{out} = +56 \text{ dBmV @ 870 Mhz Equiv}$) 112–Channel, 12db Tilt	CSO_{112}	—	–65	–63	
($V_{out} = +56 \text{ dBmV @ 870 Mhz Equiv}$) 112–Channel, 13.5db Tilt	CSO_{112}	—	–64	–62	
($V_{out} = +56 \text{ dBmV @ 870 Mhz Equiv}$) 112–Channel, 17db Tilt	CSO_{112}	—	–63	–61	
($V_{out} = +58 \text{ dBmV @ 870 Mhz Equiv}$) 79–Channel, 12db Tilt	CSO_{79}	—	–69	–67	
($V_{out} = +58 \text{ dBmV @ 870 Mhz Equiv}$) 79–Channel, 13.5db Tilt	CSO_{79}	—	–74	–72	
($V_{out} = +58 \text{ dBmV @ 870 Mhz Equiv}$) 79–Channel, 17db Tilt	CSO_{79}	—	–73	–71	
Cross Modulation Distortion @ Ch 2					dBc
($V_{out} = +48 \text{ dBmV/ch.}$, FM = 55 MHz) 132–Channel FLAT	XMD_{132}	—	–57	–55	
($V_{out} = +48 \text{ dBmV/ch.}$, FM = 55 MHz) 112–Channel FLAT	XMD_{112}	—	–59	–57	
($V_{out} = +48 \text{ dBmV/ch.}$, FM = 55 MHz) 79–Channel FLAT	XMD_{79}	—	–62	–60	
($V_{out} = +56 \text{ dBmV @ 870 Mhz Equiv}$) 112–Channel, 12db Tilt	XMD_{112}	—	–53	–51	
($V_{out} = +56 \text{ dBmV @ 870 Mhz Equiv}$) 112–Channel, 13.5db Tilt	XMD_{112}	—	–55	–53	
($V_{out} = +56 \text{ dBmV @ 870 Mhz Equiv}$) 112–Channel, 17db Tilt	XMD_{112}	—	–58	–56	
($V_{out} = +58 \text{ dBmV @ 870 Mhz Equiv}$) 79–Channel, 12db Tilt	XMD_{79}	—	–60	–47	
($V_{out} = +58 \text{ dBmV @ 870 Mhz Equiv}$) 79–Channel, 13.5db Tilt	XMD_{79}	—	–62	–60	
($V_{out} = +58 \text{ dBmV @ 870 Mhz Equiv}$) 79–Channel, 17db Tilt	XMD_{79}	—	–67	–65	
Composite Triple Beat					dBc
($V_{out} = +48 \text{ dBmV/ch.}$, Worst Case) 132–Channel FLAT	CTB_{132}	—	–60	–56	
($V_{out} = +48 \text{ dBmV/ch.}$, Worst Case) 112–Channel FLAT	CTB_{112}	—	–64	–60	
($V_{out} = +48 \text{ dBmV/ch.}$, Worst Case) 79–Channel FLAT	CTB_{79}	—	–68	–66	
($V_{out} = +56 \text{ dBmV @ 870 Mhz Equiv}$) 112–Channel, 12db Tilt	CTB_{112}	—	–60	–58	
($V_{out} = +56 \text{ dBmV @ 870 Mhz Equiv}$) 112–Channel, 13.5db Tilt	CTB_{112}	—	–61	–59	
($V_{out} = +56 \text{ dBmV @ 870 Mhz Equiv}$) 112–Channel, 17db Tilt	CTB_{112}	—	–64	–62	
($V_{out} = +58 \text{ dBmV @ 870 Mhz Equiv}$) 79–Channel, 12db Tilt	CTB_{79}	—	–66	–64	
($V_{out} = +58 \text{ dBmV @ 870 Mhz Equiv}$) 79–Channel, 13.5db Tilt	CTB_{79}	—	–71	–69	
($V_{out} = +58 \text{ dBmV @ 870 Mhz Equiv}$) 79–Channel, 17db Tilt	CTB_{79}	—	–74	–72	
Noise Figure					dB
50 MHz	NF	—	4.0	4.5	
550 MHz		—	3.5	4.5	
750 MHz		—	3.5	4.5	
870 MHz		—	4.0	4.5	
DC Current ($V_{DC} = 24 \text{ V}$, $T_C = 45^\circ\text{C}$)	I_{DC}	410	425	440	mA

The RF Line

Gallium Arsenide

CATV Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Higher Output Capability
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

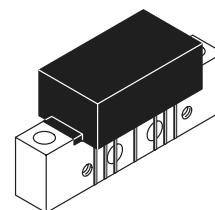
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV GaAs Forward Power Doubler Amplifier

MHW9188

**870 MHz
20.3 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+75	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	300	300	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 870 MHz	G_p	19.7	20.3	20.9	dB
Slope 40-870 MHz	S	0	0.5	1.0	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	G_F	—	—	0.5	dB
Return Loss — Input ($Z_o = 75$ Ohms)	IRL	20 18 16	— — —	— — —	dB
Return Loss — Output ($Z_o = 75$ Ohms)	ORL	20 18	— —	— —	dB

REV 1

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Composite Second Order					dBc
($V_{out} = +48$ dBmV/ch., Worst Case) 132–Channel FLAT	CSO_{132}	—	–64	–62	
($V_{out} = +48$ dBmV/ch., Worst Case) 112–Channel FLAT	CSO_{112}	—	–66	–64	
($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CSO_{79}	—	–70	–68	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 12 dB Tilt	CSO_{112}	—	–65	–63	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 13.5 dB Tilt	CSO_{112}	—	–64	–62	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 17 dB Tilt	CSO_{112}	—	–63	–61	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 12 dB Tilt	CSO_{79}	—	–69	–67	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 13.5 dB Tilt	CSO_{79}	—	–74	–72	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 17 dB Tilt	CSO_{79}	—	–73	–71	
Cross Modulation Distortion @ Ch 2					dBc
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 132–Channel FLAT	XMD_{132}	—	–57	–55	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 112–Channel FLAT	XMD_{112}	—	–59	–57	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 79–Channel FLAT	XMD_{79}	—	–62	–60	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 12 dB Tilt	XMD_{112}	—	–53	–51	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 13.5 dB Tilt	XMD_{112}	—	–55	–53	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 17 dB Tilt	XMD_{112}	—	–58	–56	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 12 dB Tilt	XMD_{79}	—	–60	–47	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 13.5 dB Tilt	XMD_{79}	—	–62	–60	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 17 dB Tilt	XMD_{79}	—	–67	–65	
Composite Triple Beat					dBc
($V_{out} = +48$ dBmV/ch., Worst Case) 132–Channel FLAT	CTB_{132}	—	–58	–56	
($V_{out} = +48$ dBmV/ch., Worst Case) 112–Channel FLAT	CTB_{112}	—	–62	–60	
($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CTB_{79}	—	–68	–66	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 12 dB Tilt	CTB_{112}	—	–60	–58	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 13.5 dB Tilt	CTB_{112}	—	–61	–59	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 17 dB Tilt	CTB_{112}	—	–64	–62	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 12 dB Tilt	CTB_{79}	—	–66	–64	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 13.5 dB Tilt	CTB_{79}	—	–71	–69	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 17 dB Tilt	CTB_{79}	—	–74	–72	
Noise Figure					dB
50 MHz	NF	—	4.0	4.5	
550 MHz		—	4.0	4.5	
750 MHz		—	4.0	4.5	
870 MHz		—	4.0	4.5	
DC Current ($V_{DC} = 24$ V, $T_C = 45^\circ\text{C}$)	I_{DC}	410	425	440	mA

The RF Line

Gallium Arsenide

CATV Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Mirror Image of MHW9188
- Excellent Distortion Performance
- Higher Output Capability
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

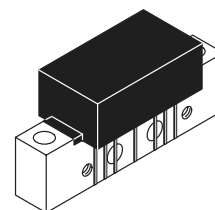
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV GaAs Forward Mirror Power Doubler Amplifier

MHW9189

**870 MHz
20.3 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER**



CASE 1302-01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+75	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	300	300	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 870 MHz	G_p	19.7	20.3	20.9	dB
Slope 40-870 MHz	S	0	0.5	1.0	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	G_F	—	—	0.5	dB
Return Loss — Input ($Z_o = 75$ Ohms)	IRL	20 18 16	— — —	— — —	dB
Return Loss — Output ($Z_o = 75$ Ohms)	ORL	20 18	— —	— —	dB

REV 1

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Second Order						dBc
($V_{out} = +48$ dBmV/ch., Worst Case)	132–Channel FLAT	CSO_{132}	—	–64	–62	
($V_{out} = +48$ dBmV/ch., Worst Case)	112–Channel FLAT	CSO_{112}	—	–66	–64	
($V_{out} = +48$ dBmV/ch., Worst Case)	79–Channel FLAT	CSO_{79}	—	–70	–68	
($V_{out} = +56$ dBmV @ 870 MHz Equiv)	112–Channel, 12 dB Tilt	CSO_{112}	—	–65	–63	
($V_{out} = +56$ dBmV @ 870 MHz Equiv)	112–Channel, 13.5 dB Tilt	CSO_{112}	—	–64	–62	
($V_{out} = +56$ dBmV @ 870 MHz Equiv)	112–Channel, 17 dB Tilt	CSO_{112}	—	–63	–61	
($V_{out} = +58$ dBmV @ 870 MHz Equiv)	79–Channel, 12 dB Tilt	CSO_{79}	—	–69	–67	
($V_{out} = +58$ dBmV @ 870 MHz Equiv)	79–Channel, 13.5 dB Tilt	CSO_{79}	—	–74	–72	
($V_{out} = +58$ dBmV @ 870 MHz Equiv)	79–Channel, 17 dB Tilt	CSO_{79}	—	–73	–71	
Cross Modulation Distortion @ Ch 2						dBc
($V_{out} = +48$ dBmV/ch., FM = 55 MHz)	132–Channel FLAT	XMD_{132}	—	–57	–55	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz)	112–Channel FLAT	XMD_{112}	—	–59	–57	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz)	79–Channel FLAT	XMD_{79}	—	–62	–60	
($V_{out} = +56$ dBmV @ 870 MHz Equiv)	112–Channel, 12 dB Tilt	XMD_{112}	—	–53	–51	
($V_{out} = +56$ dBmV @ 870 MHz Equiv)	112–Channel, 13.5 dB Tilt	XMD_{112}	—	–55	–53	
($V_{out} = +56$ dBmV @ 870 MHz Equiv)	112–Channel, 17 dB Tilt	XMD_{112}	—	–58	–56	
($V_{out} = +58$ dBmV @ 870 MHz Equiv)	79–Channel, 12 dB Tilt	XMD_{79}	—	–60	–47	
($V_{out} = +58$ dBmV @ 870 MHz Equiv)	79–Channel, 13.5 dB Tilt	XMD_{79}	—	–62	–60	
($V_{out} = +58$ dBmV @ 870 MHz Equiv)	79–Channel, 17 dB Tilt	XMD_{79}	—	–67	–65	
Composite Triple Beat						dBc
($V_{out} = +48$ dBmV/ch., Worst Case)	132–Channel FLAT	CTB_{132}	—	–58	–56	
($V_{out} = +48$ dBmV/ch., Worst Case)	112–Channel FLAT	CTB_{112}	—	–62	–60	
($V_{out} = +48$ dBmV/ch., Worst Case)	79–Channel FLAT	CTB_{79}	—	–68	–66	
($V_{out} = +56$ dBmV @ 870 MHz Equiv)	112–Channel, 12 dB Tilt	CTB_{112}	—	–60	–58	
($V_{out} = +56$ dBmV @ 870 MHz Equiv)	112–Channel, 13.5 dB Tilt	CTB_{112}	—	–61	–59	
($V_{out} = +56$ dBmV @ 870 MHz Equiv)	112–Channel, 17 dB Tilt	CTB_{112}	—	–64	–62	
($V_{out} = +58$ dBmV @ 870 MHz Equiv)	79–Channel, 12 dB Tilt	CTB_{79}	—	–66	–64	
($V_{out} = +58$ dBmV @ 870 MHz Equiv)	79–Channel, 13.5 dB Tilt	CTB_{79}	—	–71	–69	
($V_{out} = +58$ dBmV @ 870 MHz Equiv)	79–Channel, 17 dB Tilt	CTB_{79}	—	–74	–72	
Noise Figure						dB
	50 MHz	NF	—	4.0	4.5	
	550 MHz		—	4.0	4.5	
	750 MHz		—	4.0	4.5	
	870 MHz		—	4.0	4.5	
DC Current ($V_{DC} = 24$ V, $T_C = 45^\circ\text{C}$)		I_{DC}	410	425	440	mA

The RF Line

Gallium Arsenide

CATV Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

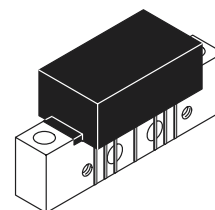
- CATV Systems Operating in the 47 to 870 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Output Stage Amplifier on Applications Requiring Low Power Dissipation and High Output Performance
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 47 to 870 MHz, CATV GaAs Forward Amplifier

MHW9206

**870 MHz
20.2 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	300	300	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	47	—	870	MHz
Power Gain 870 MHz	G_p	19.6	20.2	20.8	dB
Slope 47-870 MHz	S	0.4	0.8	1.4	dB
Gain Flatness (47-870 MHz, Peak-to-Valley)	G_F	—	—	0.5	dB
Return Loss — Input/Output ($Z_0 = 75$ Ohms)	IRL/ORL	20 19 18	— — —	— — —	dB
Composite Second Order ($V_{out} = +48$ dBmV/ch., Worst Case) ($V_{out} = +46$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	CSO ₇₉ CSO ₁₁₂ CSO ₁₃₂	— — —	-66 -62 -63	-63 -59 -59	dBc

REV 1

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24 \text{ Vdc}$, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion @ Ch 2						dBc
($V_{out} = +48 \text{ dBmV/ch.}$, FM = 55.25 MHz)	79–Channel FLAT	XMD_{79}	—	–55	–51	
($V_{out} = +46 \text{ dBmV/ch.}$, FM = 55.25 MHz)	112–Channel FLAT	XMD_{112}	—	–55	–51	
($V_{out} = +44 \text{ dBmV/ch.}$, FM = 55.25 MHz)	132–Channel FLAT	XMD_{132}	—	–57	–51	
Composite Triple Beat						dBc
($V_{out} = +48 \text{ dBmV/ch.}$, Worst Case)	79–Channel FLAT	CTB_{79}	—	–62	–60	
($V_{out} = +46 \text{ dBmV/ch.}$, Worst Case)	112–Channel FLAT	CTB_{112}	—	–60	–57	
($V_{out} = +44 \text{ dBmV/ch.}$, Worst Case)	132–Channel FLAT	CTB_{132}	—	–60	–57	
Noise Figure	50 MHz	NF	—	3.8	4.5	dB
	870 MHz		—	4	4.5	
DC Current ($V_{DC} = 24 \text{ V}$, $T_C = 45^\circ\text{C}$)		I_{DC}	230	245	260	mA

The RF Line

Gallium Arsenide

CATV Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Higher Output Capability
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

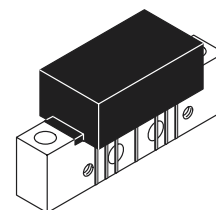
- CATV Systems Operating in the 47 to 870 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 47 to 870 MHz, CATV GaAs Forward Power Doubler Amplifier

MHW9227

**870 MHz
22.1 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER MODULE**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	200	200	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	47	—	870	MHz
Power Gain 870 MHz	G_p	21.5	22.1	22.7	dB
Slope 47-870 MHz	S	0	0.5	1.0	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	—	—	—	0.7	dB
Return Loss — Input/Output ($Z_o = 75$ Ohms)	IRL	20 18 16	— — —	— — —	dB
		47-500 MHz			
		501-750 MHz			
		751-870 MHz			

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Composite Second Order					dBc
($V_{out} = +48$ dBmV/ch., Worst Case) 132–Channel FLAT	CSO_{132}	—	–64	–62	
($V_{out} = +48$ dBmV/ch., Worst Case) 112–Channel FLAT	CSO_{112}	—	–66	–64	
($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CSO_{79}	—	–70	–68	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 12 dB Tilt	CSO_{112}	—	–65	–63	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 13.5 dB Tilt	CSO_{112}	—	–64	–62	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 17 dB Tilt	CSO_{112}	—	–63	–61	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 12 dB Tilt	CSO_{79}	—	–69	–67	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 13.5 dB Tilt	CSO_{79}	—	–74	–72	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 17 dB Tilt	CSO_{79}	—	–73	–71	
Cross Modulation Distortion @ Ch 2					dBc
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 132–Channel FLAT	XMD_{132}	—	–57	–55	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 112–Channel FLAT	XMD_{112}	—	–59	–57	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 79–Channel FLAT	XMD_{79}	—	–62	–60	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 12 dB Tilt	XMD_{112}	—	–53	–51	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 13.5 dB Tilt	XMD_{112}	—	–55	–53	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 17 dB Tilt	XMD_{112}	—	–58	–56	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 12 dB Tilt	XMD_{79}	—	–60	–47	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 13.5 dB Tilt	XMD_{79}	—	–62	–60	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 17 dB Tilt	XMD_{79}	—	–67	–65	
Composite Triple Beat					dBc
($V_{out} = +48$ dBmV/ch., Worst Case) 132–Channel FLAT	CTB_{132}	—	–58	–56	
($V_{out} = +48$ dBmV/ch., Worst Case) 112–Channel FLAT	CTB_{112}	—	–62	–60	
($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CTB_{79}	—	–66	–64	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 12 dB Tilt	CTB_{112}	—	–57	–55	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 13.5 dB Tilt	CTB_{112}	—	–58	–56	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 17 dB Tilt	CTB_{112}	—	–60	–58	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 12 dB Tilt	CTB_{79}	—	–63	–61	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 13.5 dB Tilt	CTB_{79}	—	–65	–63	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 17 dB Tilt	CTB_{79}	—	–69	–67	
Noise Figure					dB
50 MHz	NF	—	4.0	4.5	
550 MHz		—	4.0	4.5	
750 MHz		—	4.0	4.5	
870 MHz		—	4.0	4.5	
DC Current ($V_{DC} = 24$ V, $T_C = 45^\circ\text{C}$)	I_{DC}	410	425	440	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Advance Information

The RF Line

Gallium Arsenide CATV Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Integrated ESD Protection Diodes
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

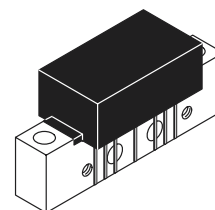
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV GaAs Forward Amplifier Module

MHW9236

870 MHz
23.6 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER MODULE



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	200	200	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 870 MHz	G_p	23	23.6	24.3	dB
Slope 40-870 MHz	S	0	0.4	1.0	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	G_F	—	—	0.8	dB
Return Loss — Input ($Z_0 = 75$ Ohms)	IRL	20 18	— —	— —	dB
		40-500 MHz $f > 501$ MHz			

REV 1

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Return Loss — Output ($Z_0 = 75$ Ohms)	40–300 MHz 301–750 MHz $f > 750$ MHz	ORL	20 19 16	— — —	— — —	dB
Composite Second Order ($V_{out} = +48$ dBmV/ch., Worst Case) ($V_{out} = +46$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	79–Channel FLAT 112–Channel FLAT 132–Channel FLAT	CSO ₇₉ CSO ₁₁₂ CSO ₁₃₂	— — —	–66 –64 –64	–63 –60 –60	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +48$ dBmV/ch., FM = 55.25 MHz) ($V_{out} = +46$ dBmV/ch., FM = 55.25 MHz) ($V_{out} = +44$ dBmV/ch., FM = 55.25 MHz)	79–Channel FLAT 112–Channel FLAT 132–Channel FLAT	XMD ₇₉ XMD ₁₁₂ XMD ₁₃₂	— — —	–57 –57 –57	–53 –53 –53	dBc
Composite Triple Beat ($V_{out} = +48$ dBmV/ch., Worst Case) ($V_{out} = +46$ dBmV/ch., Worst Case) ($V_{out} = +44$ dBmV/ch., Worst Case)	79–Channel FLAT 112–Channel FLAT 132–Channel FLAT	CTB ₇₉ CTB ₁₁₂ CTB ₁₃₂	— — —	–66 –66 –68	–60 –60 –60	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 870 MHz	NF	— — — —	5.0 5.0 5.0 5.3	6.0 — — 6.0	dB
DC Current ($V_{DC} = 24$ V, $T_C = 45^\circ\text{C}$)		I_{DC}	240	255	270	mA

The RF Line CATV Amplifier Module

Features

- Specified for 77-, 110-, 128- and 152-Channel Loading
- Excellent Distortion Performance
- Superior Gain, Return Loss and DC Current Stability over Temperature
- Silicon Bipolar Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

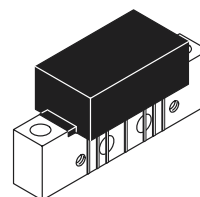
- CATV Systems Operating in the 40 to 1000 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications
- Output Stage Amplifier on Applications Requiring Low Power Dissipation

Description

- 24 Vdc Supply, 40 to 1000 MHz, CATV Forward Amplifier

MHW9242A

**1000 MHz
24 dB GAIN
152-CHANNEL
CATV AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	1000	MHz
Power Gain	G_p	23.2	—	24.8	dB
		24	—	26	
Slope	S	0	—	2.5	dB
Gain Flatness (40–1000 MHz, Peak-to-Valley)	G_F	—	—	1.0	dB
Return Loss — Input/Output ($Z_0 = 75$ Ohms)	IRL/ORL	20	—	—	dB
		—	—	0.01	dB/MHz
Composite Second Order					dBc
($V_{out} = +38$ dBmV/ch; Worst Case)	CSO_{152}	—	-66	-61	
($V_{out} = +38$ dBmV/ch; Worst Case)	CSO_{128}	—	-69	—	
($V_{out} = +40$ dBmV/ch; Worst Case)	CSO_{110}	—	-69	—	
($V_{out} = +44$ dBmV/ch; Worst Case)	CSO_{77}	—	-78	—	
Cross Modulation Distortion @ Ch 2					dBc
($V_{out} = +38$ dBmV/ch., FM = 55 MHz)	XMD_{152}	—	-62	-59	
($V_{out} = +38$ dBmV/ch, FM = 55.25 MHz)	XMD_{128}	—	-65	—	
($V_{out} = +40$ dBmV/ch, FM = 55.25 MHz)	XMD_{110}	—	-63	—	
($V_{out} = +44$ dBmV/ch, FM = 55.25 MHz)	XMD_{77}	—	-58	—	

REV 2

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Composite Triple Beat ($V_{out} = +38$ dBmV/ch., Worst Case) ($V_{out} = +38$ dBmV/ch, Worst Case) ($V_{out} = +40$ dBmV/ch, Worst Case) ($V_{out} = +44$ dBmV/ch, Worst Case)	152–Channel FLAT	CTB_{152}	—	–64	–58	dBc
	128–Channel FLAT	CTB_{128}	—	–68	—	
	110–Channel FLAT	CTB_{110}	—	–67	—	
	77–Channel FLAT	CTB_{77}	—	–64	—	
Noise Figure	$f = 50$ MHz	NF	—	4.8	5.5	dB
	$f = 750$ MHz		—	5.5	7.0	
	$f = 860$ MHz		—	5.8	7.5	
	$f = 1000$ MHz		—	—	8.0	
DC Current		I_{DC}	280	318	350	mA

The RF Line

Gallium Arsenide

CATV Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Higher Output Capability
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

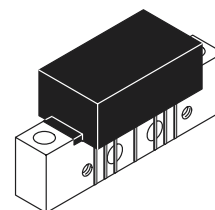
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV GaAs Forward Power Doubler Amplifier

MHW9247

**870 MHz
24.9 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	300	300	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 870 MHz	G_p	24.4	24.9	25.4	dB
Slope 40-870 MHz	S	0	0.5	1.0	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	G_F	—	—	0.5	dB
Return Loss — Input ($Z_o = 75$ Ohms)	IRL	20 18 16	— — —	— — —	dB
Return Loss — Output ($Z_o = 75$ Ohms)	ORL	20 18	— —	— —	dB

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Composite Second Order					dBc
($V_{out} = +48$ dBmV/ch., Worst Case) 132–Channel FLAT	CSO_{132}	—	–64	–62	
($V_{out} = +48$ dBmV/ch., Worst Case) 112–Channel FLAT	CSO_{112}	—	–66	–64	
($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CSO_{79}	—	–70	–68	
($V_{out} = +56$ dBmV @ 870 Mhz Equiv) 112–Channel, 12db Tilt	CSO_{112}	—	–66	–64	
($V_{out} = +56$ dBmV @ 870 Mhz Equiv) 112–Channel, 13.5db Tilt	CSO_{112}	—	–67	–65	
($V_{out} = +56$ dBmV @ 870 Mhz Equiv) 112–Channel, 17db Tilt	CSO_{112}	—	–68	–66	
($V_{out} = +58$ dBmV @ 870 Mhz Equiv) 79–Channel, 12db Tilt	CSO_{79}	—	–71	–69	
($V_{out} = +58$ dBmV @ 870 Mhz Equiv) 79–Channel, 13.5db Tilt	CSO_{79}	—	–74	–72	
($V_{out} = +58$ dBmV @ 870 Mhz Equiv) 79–Channel, 17db Tilt	CSO_{79}	—	–74	–72	
Cross Modulation Distortion @ Ch 2					dBc
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 132–Channel FLAT	XMD_{132}	—	–56	–54	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 112–Channel FLAT	XMD_{112}	—	–58	–56	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 79–Channel FLAT	XMD_{79}	—	–60	–58	
($V_{out} = +56$ dBmV @ 870 Mhz Equiv) 112–Channel, 12db Tilt	XMD_{112}	—	–53	–51	
($V_{out} = +56$ dBmV @ 870 Mhz Equiv) 112–Channel, 13.5db Tilt	XMD_{112}	—	–54	–52	
($V_{out} = +56$ dBmV @ 870 Mhz Equiv) 112–Channel, 17db Tilt	XMD_{112}	—	–55	–53	
($V_{out} = +58$ dBmV @ 870 Mhz Equiv) 79–Channel, 12db Tilt	XMD_{79}	—	–55	–53	
($V_{out} = +58$ dBmV @ 870 Mhz Equiv) 79–Channel, 13.5db Tilt	XMD_{79}	—	–58	–56	
($V_{out} = +58$ dBmV @ 870 Mhz Equiv) 79–Channel, 17db Tilt	XMD_{79}	—	–61	–59	
Composite Triple Beat					dBc
($V_{out} = +48$ dBmV/ch., Worst Case) 132–Channel FLAT	CTB_{132}	—	–58	–56	
($V_{out} = +48$ dBmV/ch., Worst Case) 112–Channel FLAT	CTB_{112}	—	–61	–59	
($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CTB_{79}	—	–68	–66	
($V_{out} = +56$ dBmV @ 870 Mhz Equiv) 112–Channel, 12db Tilt	CTB_{112}	—	–58	–56	
($V_{out} = +56$ dBmV @ 870 Mhz Equiv) 112–Channel, 13.5db Tilt	CTB_{112}	—	–59	–57	
($V_{out} = +56$ dBmV @ 870 Mhz Equiv) 112–Channel, 17db Tilt	CTB_{112}	—	–61	–59	
($V_{out} = +58$ dBmV @ 870 Mhz Equiv) 79–Channel, 12db Tilt	CTB_{79}	—	–64	–62	
($V_{out} = +58$ dBmV @ 870 Mhz Equiv) 79–Channel, 13.5db Tilt	CTB_{79}	—	–67	–65	
($V_{out} = +58$ dBmV @ 870 Mhz Equiv) 79–Channel, 17db Tilt	CTB_{79}	—	–69	–67	
Noise Figure					dB
50 MHz	NF	—	5.5	7.0	
550 MHz		—	5.5	7.0	
750 MHz		—	5.8	7.0	
870 MHz		—	6.0	7.0	
DC Current ($V_{DC} = 24$ V, $T_C = 45^\circ\text{C}$)	I_{DC}	420	440	460	mA

The RF Line

Gallium Arsenide

CATV Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Higher Output Capability
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

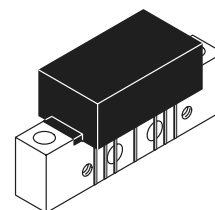
- CATV Systems Operating in the 47 to 870 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 47 to 870 MHz, CATV GaAs Forward Power Doubler Amplifier Module

MHW9267

**870 MHz
27.6 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER MODULE**



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	200	200	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 870 MHz	G_p	27	27.6	28.2	dB
Slope 47-870 MHz	S	0	0.7	1.4	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	G_F	—	—	0.5	dB
Return Loss — Input ($Z_0 = 75$ Ohms)	IRL	20 18 16	— — —	— — —	dB
		47-500 MHz 501-750 MHz 751-870 MHz			

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = +45°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Return Loss — Output (Z ₀ = 75 Ohms)	ORL	20 18	— —	— —	dB
47–160 MHz f > 160 MHz					
Composite Second Order					dBc
(V _{out} = +48 dBmV/ch., Worst Case) 132–Channel FLAT	CSO ₁₃₂	—	–62	–60	
(V _{out} = +48 dBmV/ch., Worst Case) 112–Channel FLAT	CSO ₁₁₂	—	–64	–62	
(V _{out} = +48 dBmV/ch., Worst Case) 79–Channel FLAT	CSO ₇₉	—	–68	–66	
(V _{out} = +56 dBmV @ 870 MHz Equiv) 112–Channel, 12db Tilt	CSO ₁₁₂	—	–64	–62	
(V _{out} = +56 dBmV @ 870 MHz Equiv) 112–Channel, 13.5db Tilt	CSO ₁₁₂	—	–65	–63	
(V _{out} = +56 dBmV @ 870 MHz Equiv) 112–Channel, 17db Tilt	CSO ₁₁₂	—	–66	–64	
(V _{out} = +58 dBmV @ 870 MHz Equiv) 79–Channel, 12db Tilt	CSO ₇₉	—	–69	–67	
(V _{out} = +58 dBmV @ 870 MHz Equiv) 79–Channel, 13.5db Tilt	CSO ₇₉	—	–71	–69	
(V _{out} = +58 dBmV @ 870 MHz Equiv) 79–Channel, 17db Tilt	CSO ₇₉	—	–72	–70	
Cross Modulation Distortion @ Ch 2					dBc
(V _{out} = +48 dBmV/ch., FM = 55 MHz) 132–Channel FLAT	XMD ₁₃₂	—	–56	–54	
(V _{out} = +48 dBmV/ch., FM = 55 MHz) 112–Channel FLAT	XMD ₁₁₂	—	–58	–56	
(V _{out} = +48 dBmV/ch., FM = 55 MHz) 79–Channel FLAT	XMD ₇₉	—	–60	–58	
(V _{out} = +56 dBmV @ 870 MHz Equiv) 112–Channel, 12db Tilt	XMD ₁₁₂	—	–52	–50	
(V _{out} = +56 dBmV @ 870 MHz Equiv) 112–Channel, 13.5db Tilt	XMD ₁₁₂	—	–53	–51	
(V _{out} = +56 dBmV @ 870 MHz Equiv) 112–Channel, 17db Tilt	XMD ₁₁₂	—	–55	–53	
(V _{out} = +58 dBmV @ 870 MHz Equiv) 79–Channel, 12db Tilt	XMD ₇₉	—	–55	–52	
(V _{out} = +58 dBmV @ 870 MHz Equiv) 79–Channel, 13.5db Tilt	XMD ₇₉	—	–58	–56	
(V _{out} = +58 dBmV @ 870 MHz Equiv) 79–Channel, 17db Tilt	XMD ₇₉	—	–61	–59	
Composite Triple Beat					dBc
(V _{out} = +48 dBmV/ch., Worst Case) 132–Channel FLAT	CTB ₁₃₂	—	–58	–56	
(V _{out} = +48 dBmV/ch., Worst Case) 112–Channel FLAT	CTB ₁₁₂	—	–61	–59	
(V _{out} = +48 dBmV/ch., Worst Case) 79–Channel FLAT	CTB ₇₉	—	–66	–64	
(V _{out} = +56 dBmV @ 870 MHz Equiv) 112–Channel, 12db Tilt	CTB ₁₁₂	—	–58	–56	
(V _{out} = +56 dBmV @ 870 MHz Equiv) 112–Channel, 13.5db Tilt	CTB ₁₁₂	—	–59	–57	
(V _{out} = +56 dBmV @ 870 MHz Equiv) 112–Channel, 17db Tilt	CTB ₁₁₂	—	–61	–59	
(V _{out} = +58 dBmV @ 870 MHz Equiv) 79–Channel, 12db Tilt	CTB ₇₉	—	–62	–60	
(V _{out} = +58 dBmV @ 870 MHz Equiv) 79–Channel, 13.5db Tilt	CTB ₇₉	—	–64	–62	
(V _{out} = +58 dBmV @ 870 MHz Equiv) 79–Channel, 17db Tilt	CTB ₇₉	—	–67	–65	
Noise Figure	NF	— — — —	5.5 5.5 5.8 6.0	7.0 7.0 7.0 7.0	dB
50 MHz 550 MHz 750 MHz 870 MHz					
DC Current (V _{DC} = 24 V, T _C = 45°C)	I _{DC}	410	440	460	mA

The RF Line

Gallium Arsenide

CATV Amplifier Module

Features

- 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Integrated ESD Protection Diodes
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions

Applications

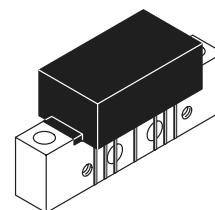
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV GaAs Forward Amplifier Module

MHW9276

870 MHz
27.9 dB GAIN
132-CHANNEL
GaAs CATV AMPLIFIER MODULE



CASE 1302-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ESD MAXIMUM RATINGS

Rating	Input Value	Output Value	Unit
Surge Voltage per IEC 1000-4-5	200	200	V
Human Body Model per Mil. Std. 1686	2	2	kV

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 870 MHz	G_p	27	27.9	28.5	dB
Slope 40-870 MHz	S	0.4	0.95	1.4	dB
Gain Flatness (40-870 MHz, Peak-to-Valley)	G_F	—	—	0.8	dB

Freescale Semiconductor, Inc.

ELECTRICAL CHARACTERISTICS – continued (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Return Loss (Z ₀ = 75 Ohms) 40–200 MHz 201–600 MHz 601–870 MHz	IRL	20 19 18	— — —	— — —	dB
Output Return Loss (Z ₀ = 75 Ohms) 40–200 MHz 201–600 MHz 601–870 MHz	ORL	20 18 18	— — —	— — —	dB
Composite Second Order (V _{out} = +44 dBmV/ch., Worst Case) (V _{out} = +44 dBmV/ch., Worst Case) (V _{out} = +44 dBmV/ch., Worst Case) 79–Channel FLAT 112–Channel FLAT 132–Channel FLAT	CSO ₇₉ CSO ₁₁₂ CSO ₁₃₂	— — —	–70 –66 –66	–64 –62 –60	dBc
Cross Modulation Distortion @ Ch 2 (V _{out} = +44 dBmV/ch., FM = 55.25 MHz) (V _{out} = +44 dBmV/ch., FM = 55.25 MHz) (V _{out} = +44 dBmV/ch., FM = 55.25 MHz) 79–Channel FLAT 112–Channel FLAT 132–Channel FLAT	XMD ₇₉ XMD ₁₁₂ XMD ₁₃₂	— — —	–60 –60 –60	–53 –53 –53	dBc
Composite Triple Beat (V _{out} = +44 dBmV/ch., Worst Case) (V _{out} = +44 dBmV/ch., Worst Case) (V _{out} = +44 dBmV/ch., Worst Case) 79–Channel FLAT 112–Channel FLAT 132–Channel FLAT	CTB ₇₉ CTB ₁₁₂ CTB ₁₃₂	— — —	–71 –68 –66	–65 –61 –60	dBc
Noise Figure 50 MHz 550 MHz 750 MHz 870 MHz	NF	— — — —	5.0 5.0 5.0 5.0	5.5 — — 6.5	dB
DC Current (V _{DC} = 24 V, T _C = 45°C)	I _{DC}	235	250	265	mA

The RF Line

Gallium Arsenide

CATV Integrated Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

Applications

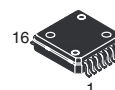
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Output Stage Amplifier on Applications Requiring Low Power Dissipation and High Output Performance
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV Integrated Forward Amplifier Module

MMG1001R2

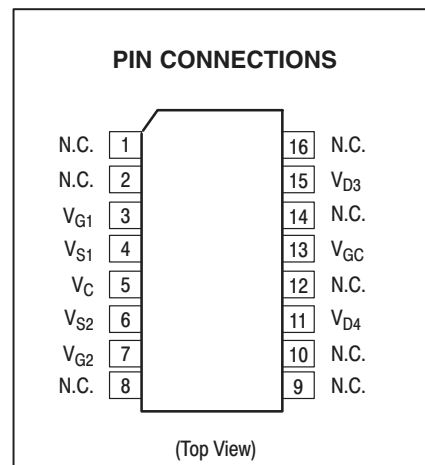
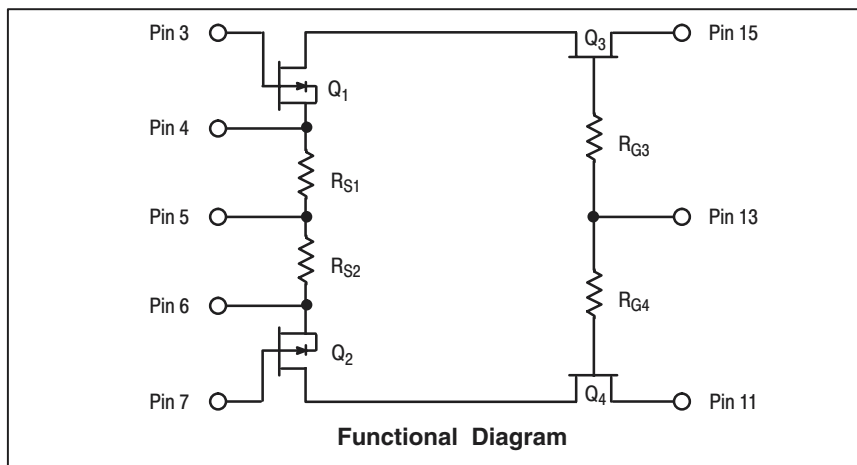
**870 MHz
18.5 dB GAIN
132-CHANNEL
CATV INTEGRATED AMPLIFIER
MODULE**



**CASE 978-03
PFP-16**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C



NOTE: MMG1001R2 Moisture Sensitivity Level (MSL) = 3.

Freescale Semiconductor, Inc.

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (minimum)
Machine Model	M1 (minimum)
Charge Device Model	C5 (minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.6	°C/W

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain 50 MHz 870 MHz	G_p	— —	18 19	— —	dB
Slope 40–870 MHz	S	—	0.6	—	dB
Gain Flatness (40–870 MHz, Peak to Valley)	G_F	—	0.5	—	dB
Input Return Loss ($Z_0 = 75$ Ohms) f = 40–160 MHz f = 161–450 MHz f = 451–870 MHz	IRL	— — —	21 19 22	— — —	dB
Output Return Loss ($Z_0 = 75$ Ohms) f = 40–400 MHz f = 401–870 MHz	ORL	— —	22 17	— —	dB
Composite Second Order ($V_{out} = +44$ dBmV/ch., Worst Case) 132–Channel FLAT ($V_{out} = +46$ dBmV/ch., Worst Case) 112–Channel FLAT ($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CSO_{132} CSO_{112} CSO_{79}	— — —	–65 –65 –71	–58 –59 –62	dBc
Cross Modulation Distortion @ Ch 2 ($V_{out} = +44$ dBmV/ch., FM = 55 MHz) 132–Channel FLAT ($V_{out} = +46$ dBmV/ch., FM = 55 MHz) 112–Channel FLAT ($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 79–Channel FLAT	XMD_{132} XMD_{112} XMD_{79}	— — —	–64 –63 –62	–52 –52 –52	dBc
Composite Triple Beat ($V_{out} = +44$ dBmV/ch., Worst Case) 132–Channel FLAT ($V_{out} = +46$ dBmV/ch., Worst Case) 112–Channel FLAT ($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CTB_{132} CTB_{112} CTB_{79}	— — —	–63 –64 –65	–56 –56 –58	dBc
Noise Figure 50 MHz 870 MHz	NF	— —	4 4	5.0 5.0	dB
DC Current ($V_{DC} = 24$ V, $T_C = -20^\circ$ to $+100^\circ\text{C}$)	I_{DC}	230	250	265	mA

Freescale Semiconductor, Inc.

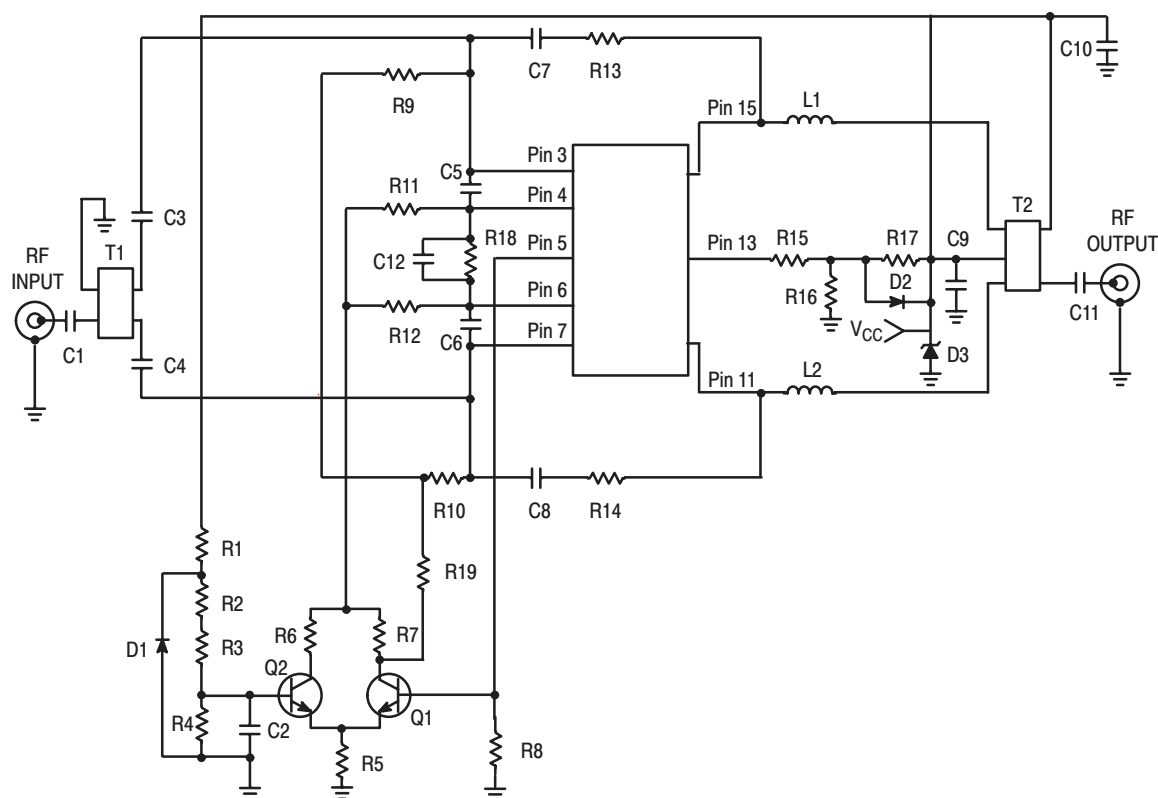


Figure 1. MMG1001R2 50–870 MHz Test Circuit Schematic

Table 1. MMG1001R2 50–870 MHz Test Circuit Component Designations and Values

Designation	Description
C1, C7, C8, C11	220 pF Chip Capacitors (0603)
C2, C3, C4, C9, C10	0.01 μ F Chip Capacitors (0603)
C5, C6	1.8 pF Chip Capacitors (0603)
C12	5.6 pF Chip Capacitor (0603)
D1	5.1 V Zener Diode, On/MM3Z5V1T1
D2	27 V Zener Diode, On/MM3Z27VT1
D3	Transient Voltage Suppressor, On/1.5k27A/1.5SMC27AT3
L1, L2	22 nH Chip Inductors (0603)
Q1, Q2	Dual Transistors Package, On/MBT3904DW1T1
R1	2.2 k Ω , 1/4 W Chip Resistor (1206)
R2	560 Ω Chip Resistor (0603)
R3	82 Ω Chip Resistor (0603)
R4, R5	820 Ω Chip Resistors (0603)
R6	120 Ω Chip Resistor (0603)
R7	1.5 k Ω Chip Resistor (0603)
R8	12 Ω , 1 W Chip Resistor (2512)
R9, R10, R15	470 Ω Chip Resistors (0603)
R11, R12	18 Ω Chip Resistors (0603)
R13, R14	910 Ω Chip Resistors (0603)
R16	2 k Ω Chip Resistor (0603)
R17	6.2 k Ω Chip Resistor (0603)
R18	5.6 Ω Chip Resistor (0603)
R19	0 Ω Chip Resistor (0603)
T1	Input Transformer, Mot/77PC016E068
T2	Output Transformer, Mot/77PC016E061
PCB	FR4, 62 mil, $\epsilon_r = 4.81$

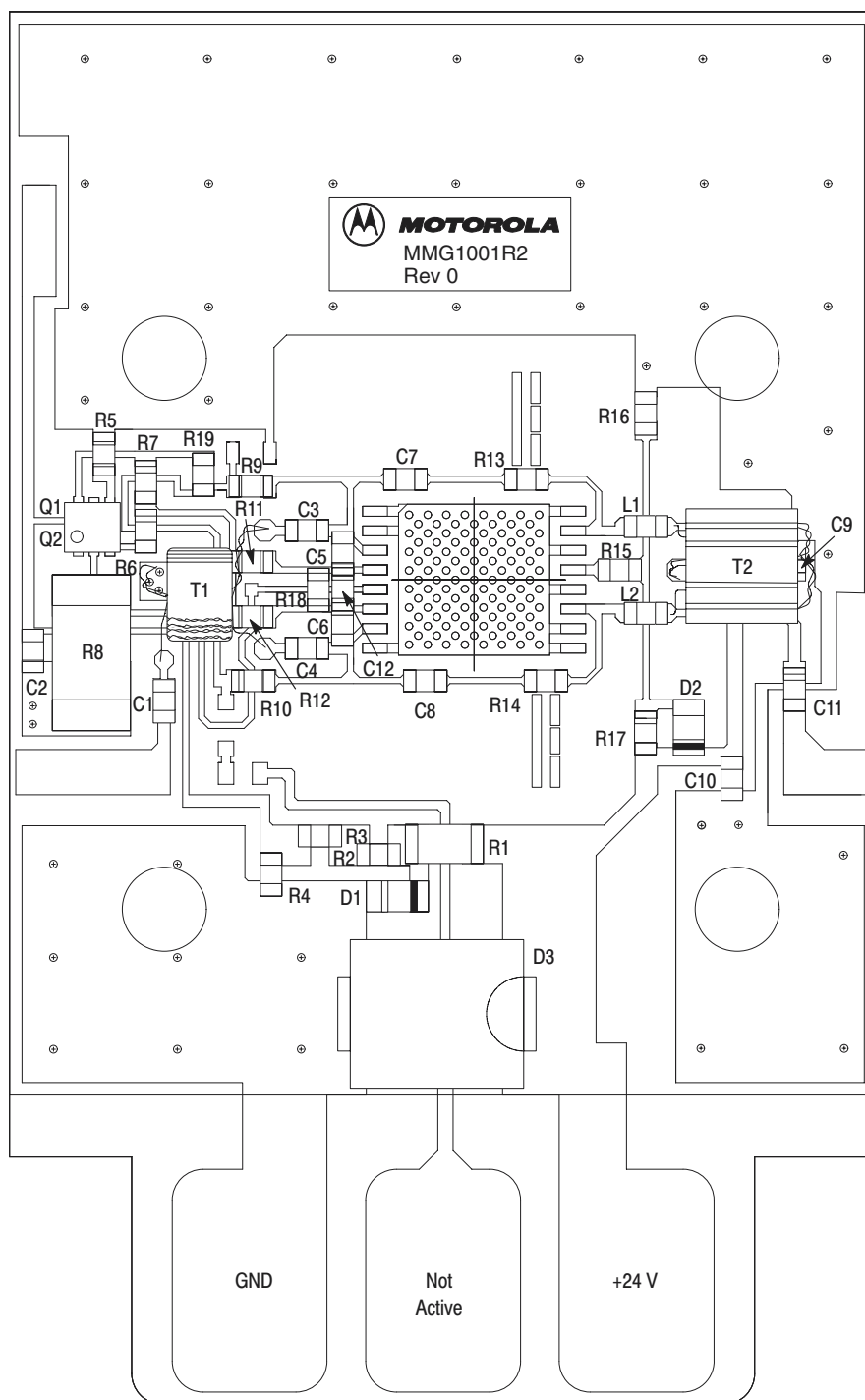


Figure 2. MMG1001R2 50–870 MHz Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

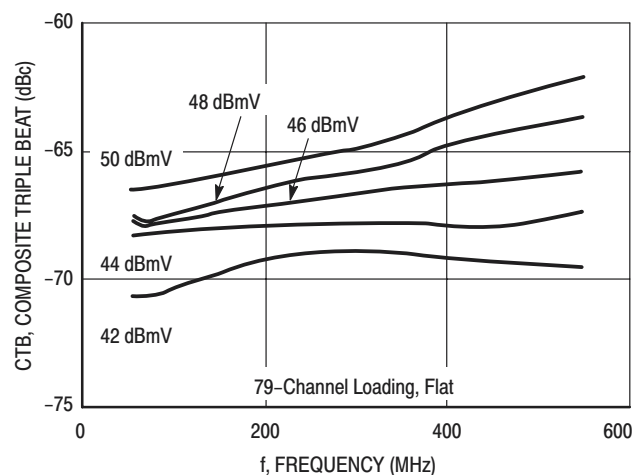


Figure 3. Composite Triple Beat versus Frequency

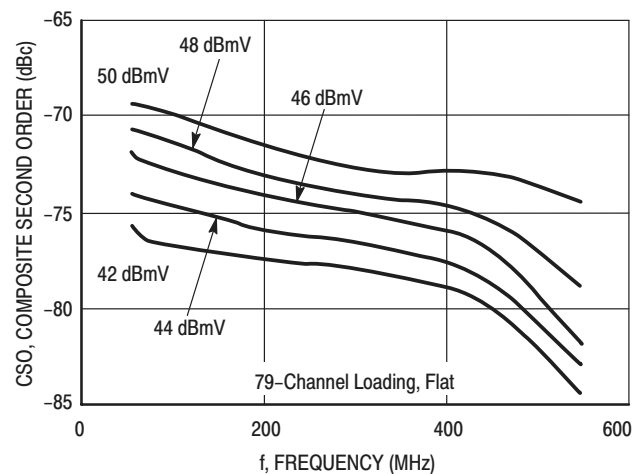


Figure 4. Composite Second Order versus Frequency

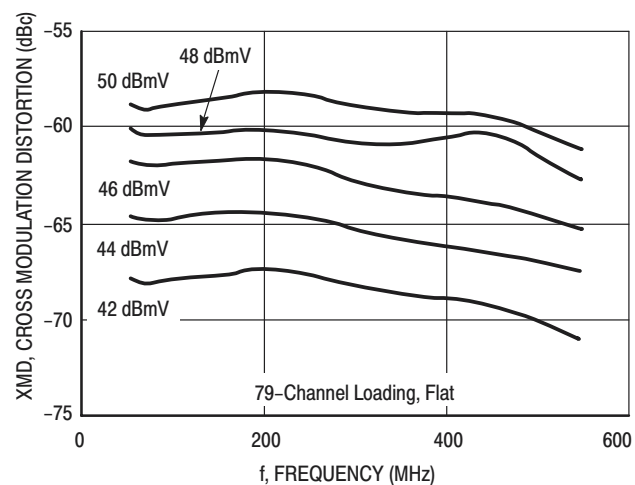


Figure 5. Cross Modulation Distortion versus Frequency

The RF Line

Gallium Arsenide

CATV Integrated Amplifier Module

Features

- Specified for 79–, 112– and 132–Channel Loading
- Excellent Distortion Performance
- Higher Output Capability
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

Applications

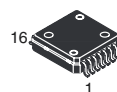
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Output Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply, 40 to 870 MHz, CATV Integrated Forward Power Doubler Amplifier Module

MMG2001R2

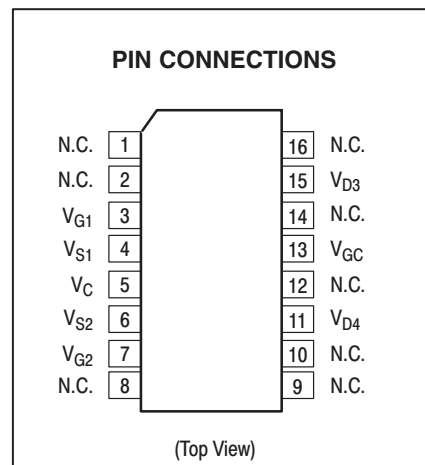
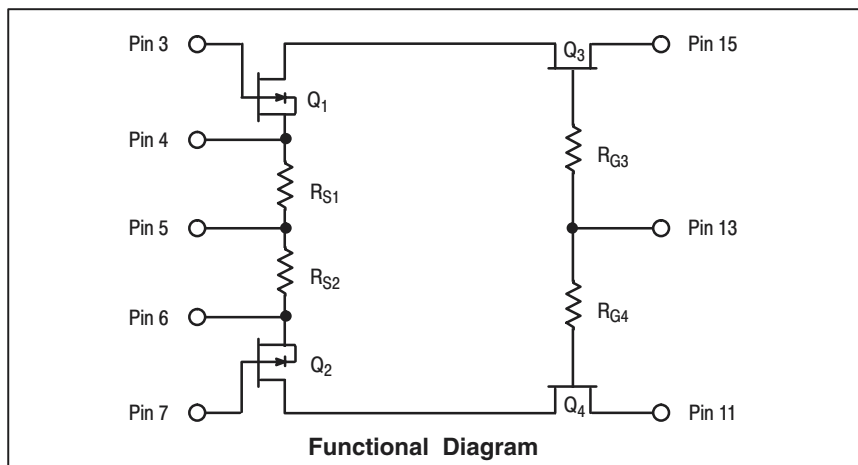
870 MHz
19.5 dB GAIN
132–CHANNEL
CATV INTEGRATED AMPLIFIER
MODULE



CASE 978–03
PFP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+26	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C



NOTE: MMG2001R2 Moisture Sensitivity Level (MSL) = 3.

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (minimum)
Machine Model	M1 (minimum)
Charge Device Model	C5 (minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.7	°C/W

ELECTRICAL CHARACTERISTICS ($V_{CC} = 24$ Vdc, $T_C = +45^\circ\text{C}$, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain	G_p	—	19	—	dB
40 MHz		—	21	—	
870 MHz		—	—	—	
Slope	S	—	0.8	—	dB
Gain Flatness (40–870 MHz, Peak to Valley)	G_F	—	0.5	—	dB
Input Return Loss ($Z_0 = 75$ Ohms)	IRL	—	21	—	dB
f = 40–160 MHz		—	19	—	
f = 161–450 MHz		—	22	—	
f = 451–870 MHz		—	—	—	
Output Return Loss ($Z_0 = 75$ Ohms)	ORL	—	22	—	dB
f = 40–400 MHz		—	17	—	
f = 401–870 MHz		—	—	—	
Composite Second Order					dBc
($V_{out} = +48$ dBmV/ch., Worst Case) 132–Channel FLAT	CSO_{132}	—	–68	–60	
($V_{out} = +48$ dBmV/ch., Worst Case) 112–Channel FLAT	CSO_{112}	—	–70	–62	
($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CSO_{79}	—	–74	–66	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 12 dB Tilt	CSO_{112}	—	–63	—	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 13.5 dB Tilt	CSO_{112}	—	–62	—	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 17 dB Tilt	CSO_{112}	—	–61	—	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 12 dB Tilt	CSO_{79}	—	–67	—	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 13.5 dB Tilt	CSO_{79}	—	–72	—	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 17 dB Tilt	CSO_{79}	—	–71	—	
Cross Modulation Distortion @ Ch 2					dBc
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 132–Channel FLAT	XMD_{132}	—	–55	–53	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 112–Channel FLAT	XMD_{112}	—	–57	–55	
($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 79–Channel FLAT	XMD_{79}	—	–60	–58	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 12 dB Tilt	XMD_{112}	—	–51	—	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 13.5 dB Tilt	XMD_{112}	—	–53	—	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 17 dB Tilt	XMD_{112}	—	–56	—	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 12 dB Tilt	XMD_{79}	—	–58	—	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 13.5 dB Tilt	XMD_{79}	—	–60	—	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 17 dB Tilt	XMD_{79}	—	–65	—	
Composite Triple Beat					dBc
($V_{out} = +48$ dBmV/ch., Worst Case) 132–Channel FLAT	CTB_{132}	—	–56	–54	
($V_{out} = +48$ dBmV/ch., Worst Case) 112–Channel FLAT	CTB_{112}	—	–60	–58	
($V_{out} = +48$ dBmV/ch., Worst Case) 79–Channel FLAT	CTB_{79}	—	–66	–64	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 12 dB Tilt	CTB_{112}	—	–58	—	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 13.5 dB Tilt	CTB_{112}	—	–59	—	
($V_{out} = +56$ dBmV @ 870 MHz Equiv) 112–Channel, 17 dB Tilt	CTB_{112}	—	–62	—	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 12 dB Tilt	CTB_{79}	—	–64	—	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 13.5 dB Tilt	CTB_{79}	—	–69	—	
($V_{out} = +58$ dBmV @ 870 MHz Equiv) 79–Channel, 17 dB Tilt	CTB_{79}	—	–72	—	
Noise Figure	NF	—	4.0	4.5	dB
50 MHz		—	4.0	4.5	
550 MHz		—	4.0	4.5	
750 MHz		—	4.0	4.5	
870 MHz		—	4.0	4.5	
DC Current ($V_{DC} = 24$ V, $T_C = 45^\circ\text{C}$)	I_{DC}	410	425	440	mA

Freescale Semiconductor, Inc.

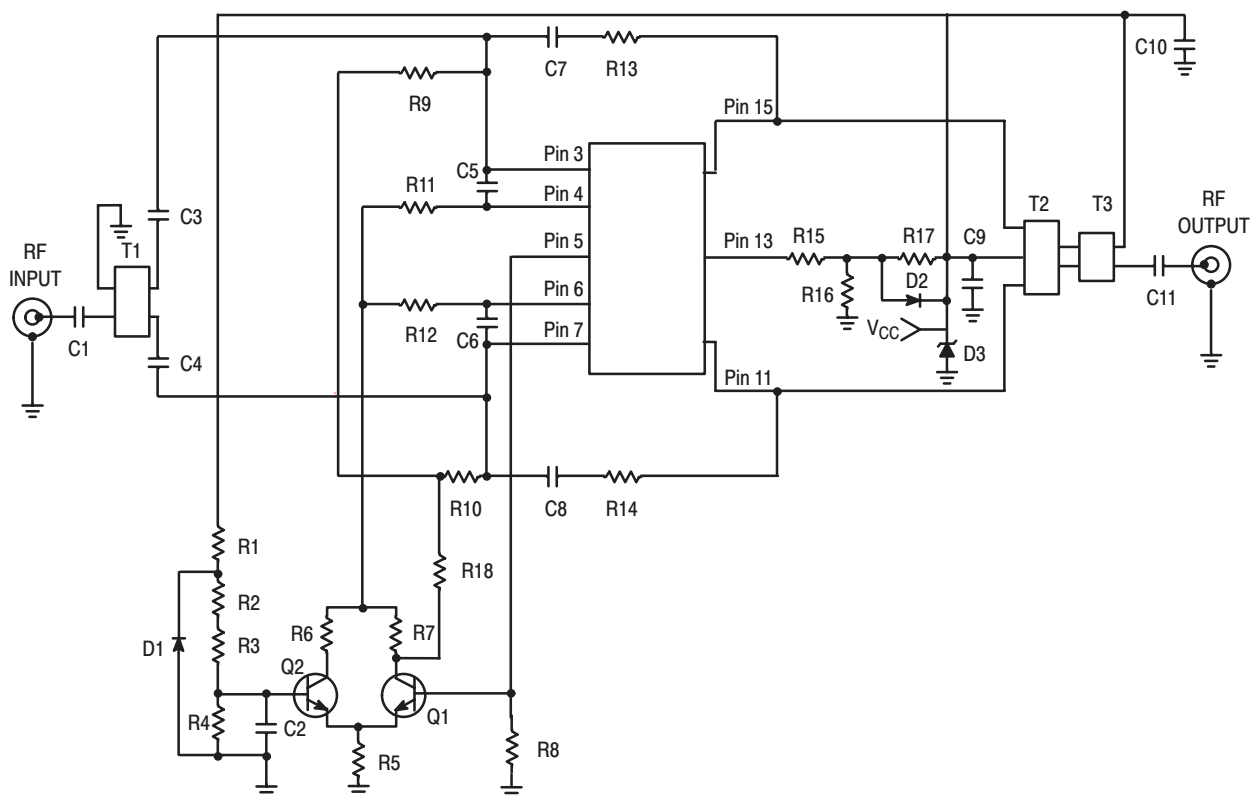


Figure 1. MMG2001R2 50–870 MHz Test Circuit Schematic

Table 1. MMG2001R2 50–870 MHz Test Circuit Component Designations and Values

Designation	Description
C1, C7, C8, C11	220 pF Chip Capacitors (0603)
C2, C3, C4, C9, C10	0.01 μ F Chip Capacitors (0603)
C5, C6	1.8 pF Chip Capacitors (0603)
D1	5.1 V Zener Diode, On/MM3Z5V1T1
D2	27 V Zener Diode, On/MM3Z27VT1
D3	Transient Voltage Suppressor, On/1.5k27A/1.5SMC27AT3
Q1, Q2	Dual Transistors Package, On/MBT3904DW1T1
R1	2.2 k Ω , 1/4 W Chip Resistor (1206)
R2	680 Ω Chip Resistor (0603)
R3	180 Ω Chip Resistor (0603)
R4	1600 Ω Chip Resistor (0603)
R5	820 Ω Chip Resistor (0603)
R6	120 Ω Chip Resistor (0603)
R7	1.5 k Ω Chip Resistor (0603)
R8	8 Ω , 1 W Chip Resistor (2512)
R9, R10, R15	470 Ω Chip Resistors (0603)
R11, R12	18 Ω Chip Resistors (0603)
R13, R14	680 Ω Chip Resistors (0603)
R16	2.4 k Ω Chip Resistor (0603)
R17	6.2 k Ω Chip Resistor (0603)
R18	0 Ω Chip Resistor (0603)
T1	Input Transformer, Mot/77PC016E080
T2	Output Transformer, Mot/77PC016E071
T3	Output Transformer, Mot/77PC016E072
PCB	FR4, 62 mil, $\epsilon_r = 4.81$

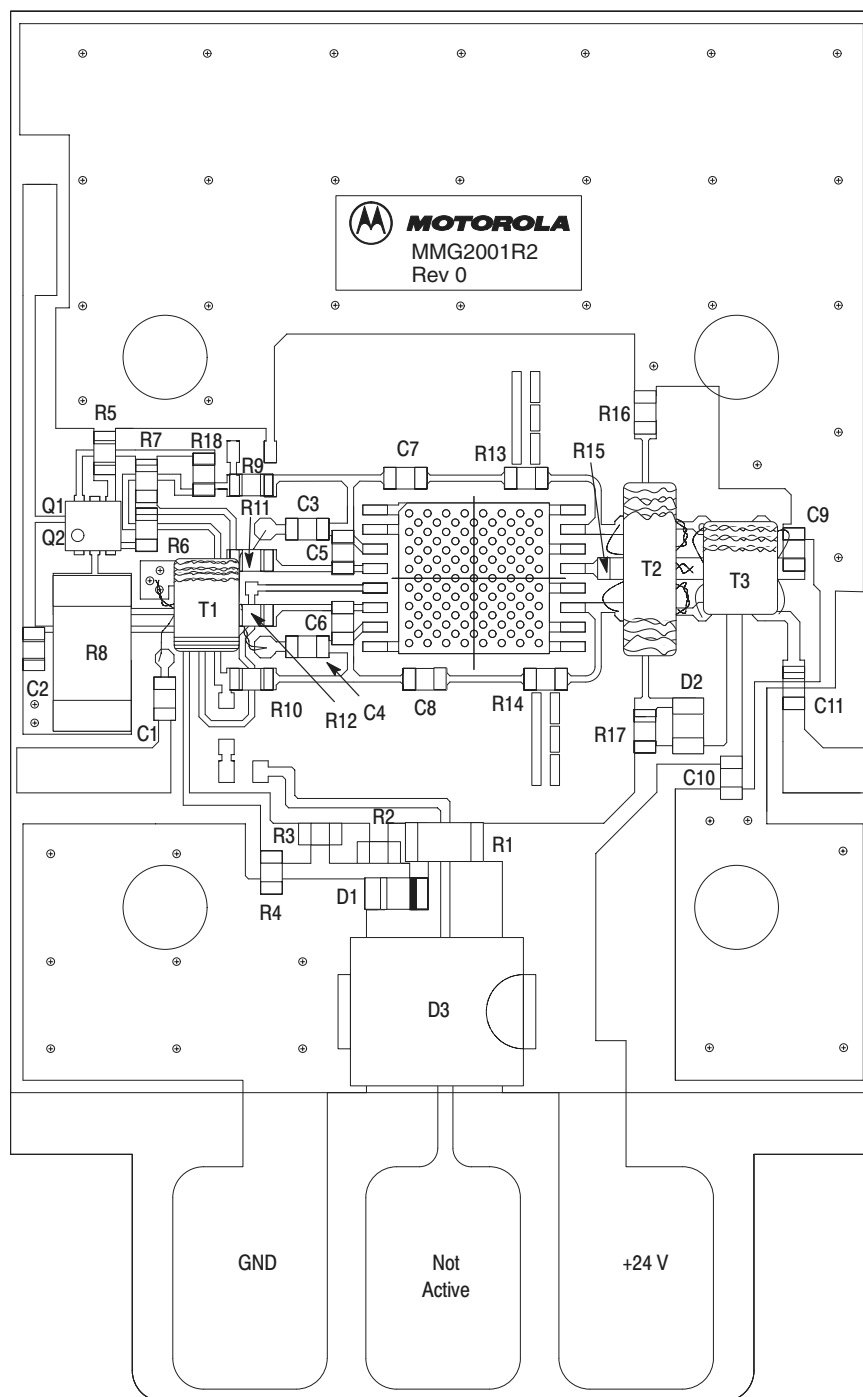


Figure 2. MMG2001R2 50–870 MHz Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

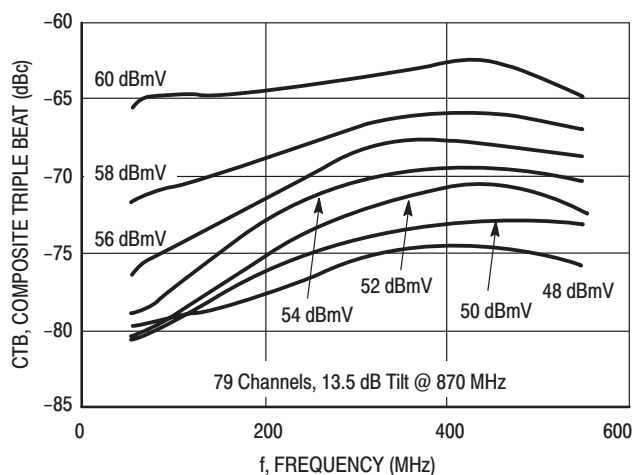


Figure 3. Composite Triple Beat versus Frequency

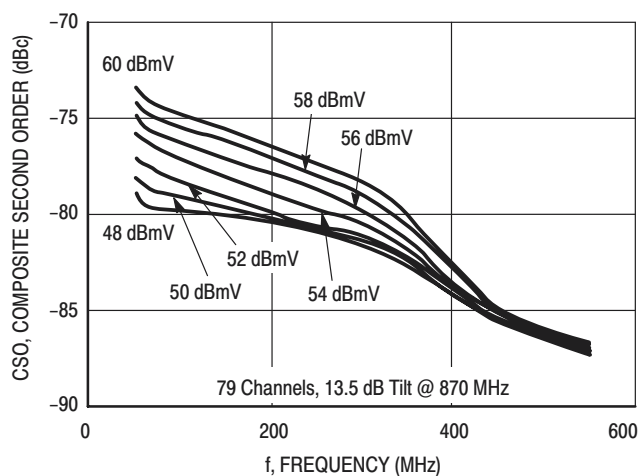


Figure 4. Composite Second Order versus Frequency

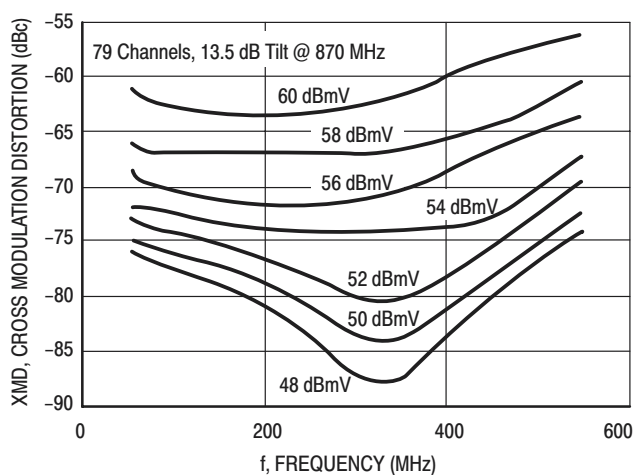


Figure 5. Cross Modulation Distortion versus Frequency

Chapter Eight

Tape and Reel Specifications

Motorola offers the convenience of Tape and Reel packaging for our growing family of standard integrated circuit products. Reels are available to support the requirements of both first and second generation pick-and-place equipment. The packaging fully conforms to the latest EIA-481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel-back cover tape.

Table of Contents

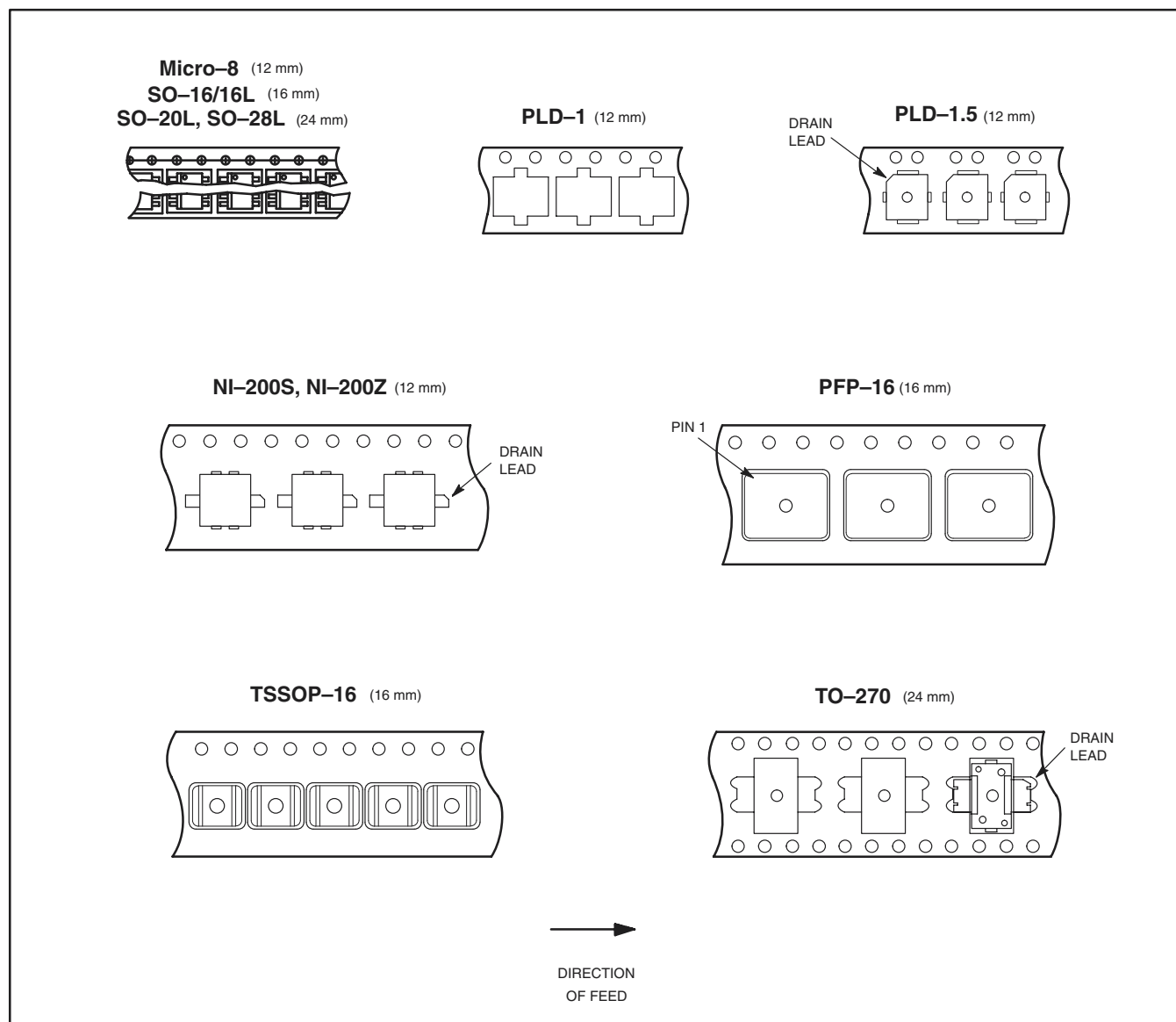
	Page
Tape and Reel Specifications	8-2
Embossed Tape and Reel Ordering Information ..	8-4
Embossed Tape and Reel Data for Discretes	8-5

RF and IF Tape and Reel Specifications

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the “peel-back” cover tape.

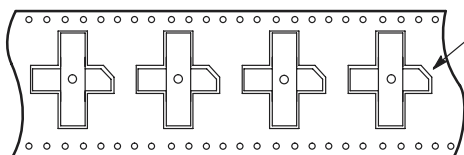
- Two Reel Sizes Available (7” and 13”)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, -1, -2
- SOT-363 in 8 mm Tape
- Micro-8, QFN-32, PLD-1, PLD-1.5, NI-200S, NI-200Z in 12 mm Tape
- SO-16/16L, TSSOP-16 in 16 mm Tape
- SO-20L, SO-28L, TO-270 in 24 mm Tape
- NI-360, NI-360S, NI-400, NI-400S, NI-600 in 32 mm Tape
- TO-272, TO-272 Dual Lead, TO-272 Split Lead, TO-272 Split Lead-Straight Lead Version, TO-272 Straight Lead, TO-272 Wide Body Multi Lead and TO-272 Wide Body Multi Lead Gull Wing in 44 mm Tape
- NI-780, NI-780S, NI-880, NI-880S in 56 mm Tape

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

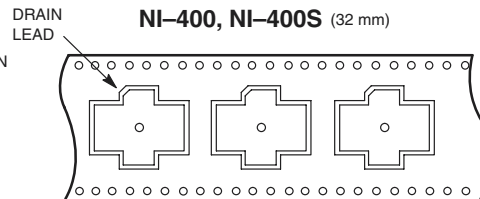


Freescale Semiconductor, Inc.

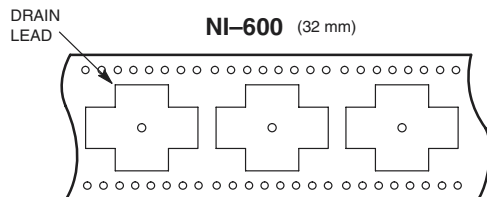
NI-360, NI-360S (32 mm)



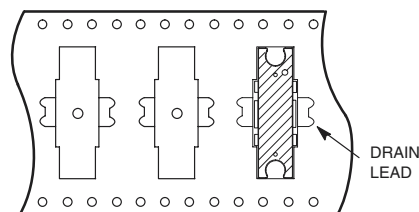
NI-400, NI-400S (32 mm)



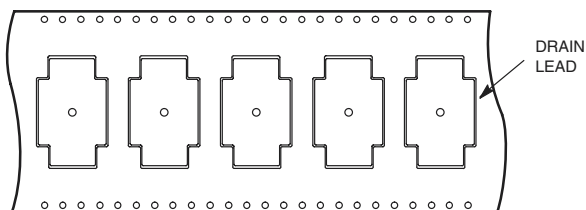
NI-600 (32 mm)



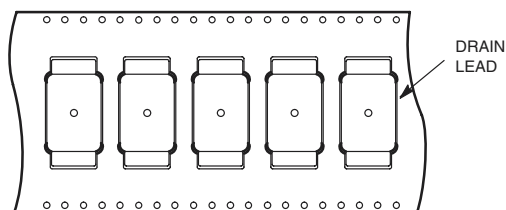
TO-272, TO-272 Dual Lead, TO-272 Split Lead, TO-272 Split Lead-Straight Lead Version, TO-272 Straight Lead (44 mm)



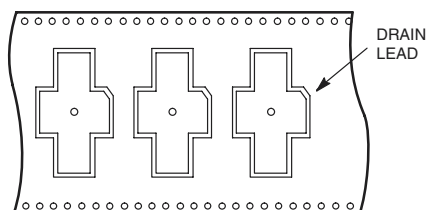
TO-272 Wide Body Multi Lead (44 mm)



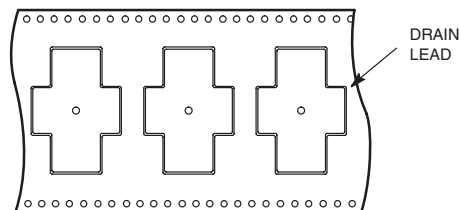
TO-272 Wide Body Multi Lead Gull Wing (44 mm)



NI-780, NI-780S (56 mm)



NI-880, NI-880S (56 mm)



Freescale Semiconductor, Inc.

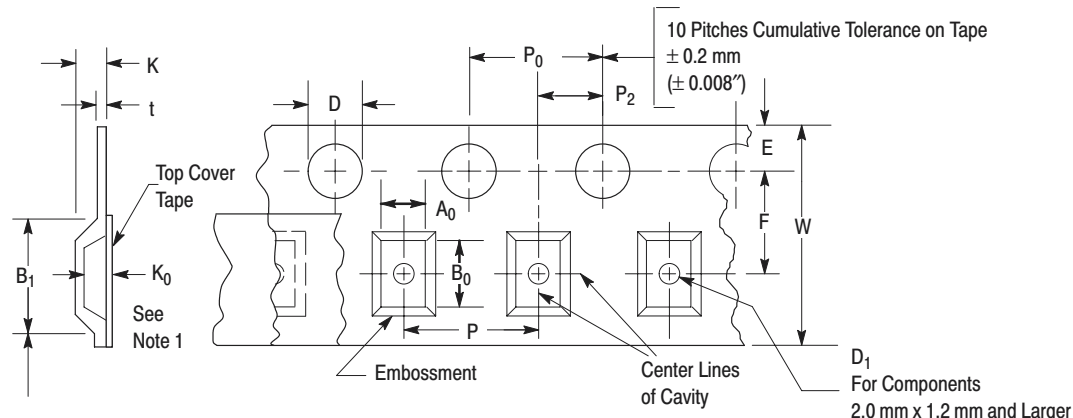
RF and IF EMBOSSED TAPE AND REEL ORDERING INFORMATION

Package	Tape Width (mm)	Pitch mm (inch)	Reel Size mm (inch)	Devices Per Reel and Minimum Order Quantity	Device Suffix
Micro-8	12	8.0 ± 0.1 (.315 ± .003)	330 (13)	2,500	R2
NI-200S (458B)	12	12.0 ± 0.1 (.471 ± .004)	178 (7)	500	R1
NI-200Z (458C)	12	12.0 ± 0.1 (.471 ± .004)	178 (7)	500	R1
NI-360 (360B)	32	24.0 ± 0.1 (.945 ± .004)	330 (13)	500	R1
NI-360S (360C)	32	24.0 ± 0.1 (.945 ± .004)	330 (13)	500	R1
NI-400 (465E)	32	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI-400S (465F)	32	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI-600 (465D)	32	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI-780 (465)	56	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI-780S (465A)	56	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI-880 (465B)	56	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
NI-880S (465C)	56	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3
PLD-1	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
PLD-1.5	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
PFP-16	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,500	R2
QFN-24	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	2,500	R2
QFN-32 (5x5 mm)	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	2,500	R2
SO-16/16L	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
SO-20L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SO-28L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SOT-363	8	4.0 ± 0.1 (.157 ± .004)	178 (7)	3,000	T1
TO-270 (1265)	24	16.0 ± 0.1 (.631 ± .004)	330 (13)	500	R1
TO-272 (1264), TO-272 Straight Lead (1264A)	44	16.0 ± 0.1 (.631 ± .004)	330 (13)	500	T1
TO-272 Split Lead (1366), TO-272 Split Lead–Straight Lead Version (1366A)	44	20.0 ± 0.1 (.787 ± .004)	330 (13)	500	T1
TO-272 Dual Lead (1337)	44	16.0 ± 0.1 (.631 ± .004)	330 (13)	500	R1
TO-272 Wide Body Multi Lead (1329)	44	20.0 ± 0.1 (.788 ± .004)	330 (13)	500	R1
TO-272 Wide Body Multi Lead Gull Wing (1329A)	44	16.0 ± 0.1 (.631 ± .004)	330 (13)	500	R1
TSSOP-16	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2

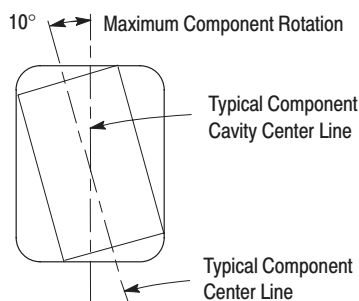
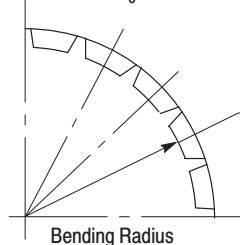
Freescale Semiconductor, Inc.

EMBOSSED TAPE AND REEL DATA FOR DISCRETES

CARRIER TAPE SPECIFICATIONS



For Machine Reference Only
Including Draft and RADII
Concentric Around B_0



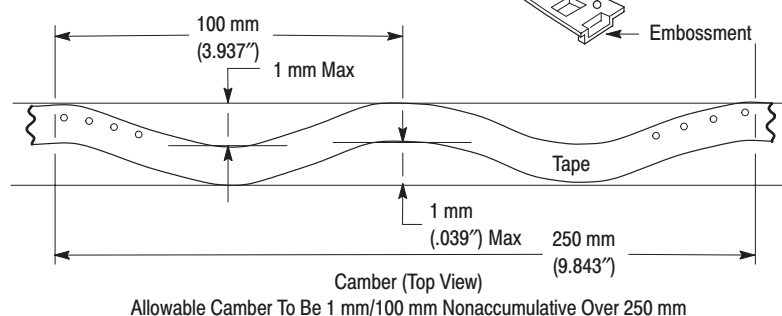
User Direction of Feed

Bar Code Label

* Top Cover Tape
Thickness (t_1)
0.10 mm
(.004") Max.

Embossed Carrier

Embossment



Freescale Semiconductor, Inc.

DIMENSIONS

Tape Size	B ₁ Max	D	D ₁	E ₁	F	K	P ₀	P ₂	R Min	t Max	W Max		
12 mm	8.2 mm (.323")	1.5±0.1 mm -0.0 (.059±.004" -0.0)	1.5 mm Min (.060")	1.75±0.1 mm (.069±.004")	5.5±0.05 mm (.217±.002")	6.4 mm Max (.252")	4.0±0.1 mm (.157±.004")	2.0±0.1 mm (.079±.004")	30 mm (1.18")	0.4 mm (.016")	12±.30 mm (.470±.012")		
16 mm	12.1 mm (.476")				7.5±0.10 mm (.295±.004")	7.9 mm Max (.311")					16.3 mm (.642")		
24 mm	20.1 mm (.791")				11.5±0.1 mm (.453±.004")	11.9 mm Max (.468")					24.3 mm (.957")		
32 mm	23.0 mm (.906")	1.5 mm Min (.059")	1.5 mm Min (.059")	1.75±0.1 mm (.069±.004")	14.2±0.1 mm (.559 ±.004")	4.6 mm (.181") NI-360/S	4.0±0.1 mm (.157±.004")	2.0±0.1 mm (.079±.004")	50 mm (1.969")	0.6 mm (.024")	32.2 mm (1.272")		
44 mm	35.0 mm (1.378")					4.3 mm (.169") NI-400/S						15.9 mm Max (.625")	44±.30 mm (1.732±.012")
						5.34 mm (.210") NI-600/S							
					11.5±0.1 mm (.453±.004")	3.20 mm (.126")					20.0±0.1 mm (.788±.004")		
20.2±0.15 mm (0.796±.006") TO-272 WB	2.92 mm (.115")				16.0±0.1 mm (.630±.004")								
24.0 mm (.946") TO-272 Wide Body Multi Lead						20.2±0.15 mm (0.796±.006")						3.20 mm (.126")	
23.77 mm (.936") TO-272 WB Multi Lead Gull Wing													
56 mm	34.7 mm (1.366")	26.2 ±0.15 mm (1.031±.006")	4.5 mm (0.177") NI-780/S	4.0±0.1 mm (.157±.004")	56±.30 mm (2.205±.012")								
						5.23 mm (0.206") NI-880/S							

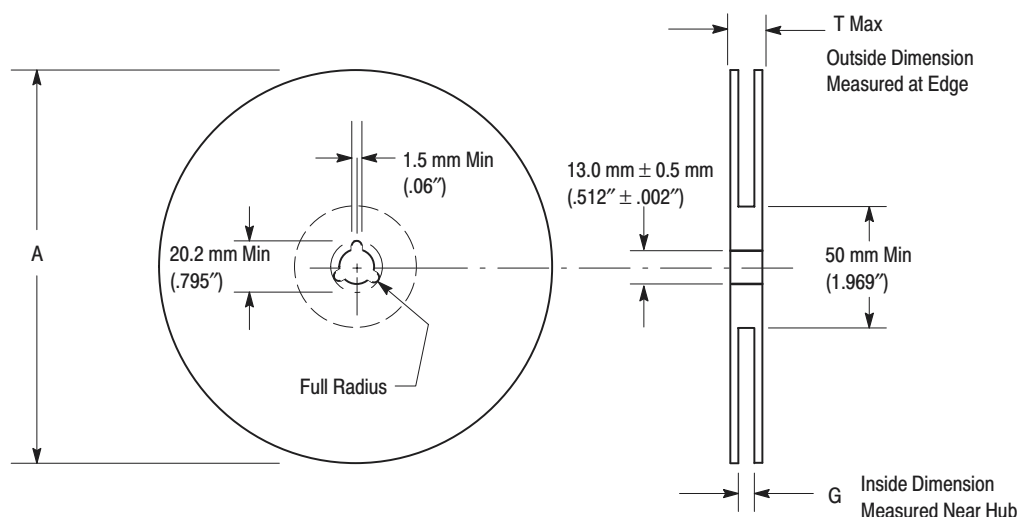
Metric dimensions govern — English are in parentheses for reference only.

NOTE 1: A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within .05 mm min. to .50 mm max., the component cannot rotate more than 10° within the determined cavity.

NOTE 3: Pitch information is contained in the Embossed Tape and Reel Ordering Information on pg. 8–4.

Freescale Semiconductor, Inc.

EMBOSED TAPE AND REEL DATA FOR DISCRETES



Size	A Max	G	T Max
12 mm	330 mm (12.992")	12.4 mm + 2.0 mm, -0.0 (.49" + .079", -0.00)	18.4 mm (.72")
16 mm	360 mm (14.173")	16.4 mm + 2.0 mm, -0.0 (.646" + .078", -0.00)	22.4 mm (.882")
24 mm	360 mm (14.173")	24.4 mm + 2.0 mm, -0.0 (.961" + .070", -0.00)	30.4 mm (1.197")
32 mm	360 mm (14.163")	32.4 mm + 2.0 mm, -0.0 (1.276" + 0.79", -0.00)	38.4 mm (1.512")
44 mm	330 mm (12.992")	44.4 mm + 2.0 mm, -0.0 (1.748" + 0.79", -0.00)	50.4 mm (1.984")
44 mm TO-272 Wide Body Multi Lead	330 mm (12.992")	45.3 mm + 0.5 mm, -0.0 (1.785" + 0.02", -0.00)	50.4 mm (1.984")
44 mm TO-272 Wide Body Multi Lead Gull Wing	330 mm (12.992")	45.3 mm + 0.5 mm, -0.0 (1.785" + 0.02", -0.00)	50.4 mm (1.984")
56 mm	330 mm (12.992")	56.4 mm + 2.0 mm, -0.0 (2.220" + 0.79", -0.00)	62 mm (2.441")

Reel Dimensions

Metric Dimensions Govern — English are in parentheses for reference only

Freescale Semiconductor, Inc.

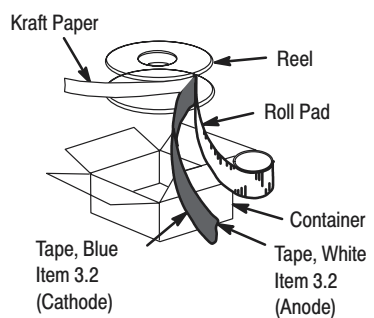


Figure 1. Reel Packing

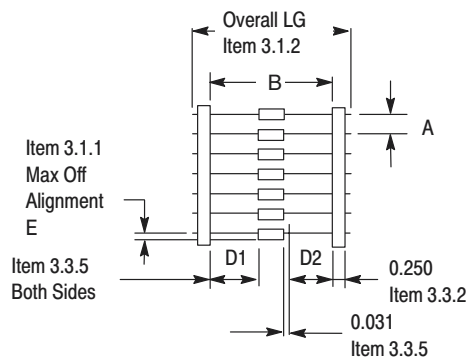


Figure 2. Component Spacing

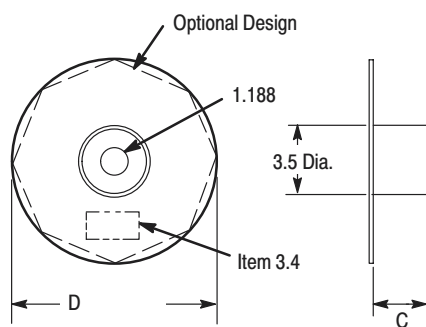


Figure 3. Reel Dimensions

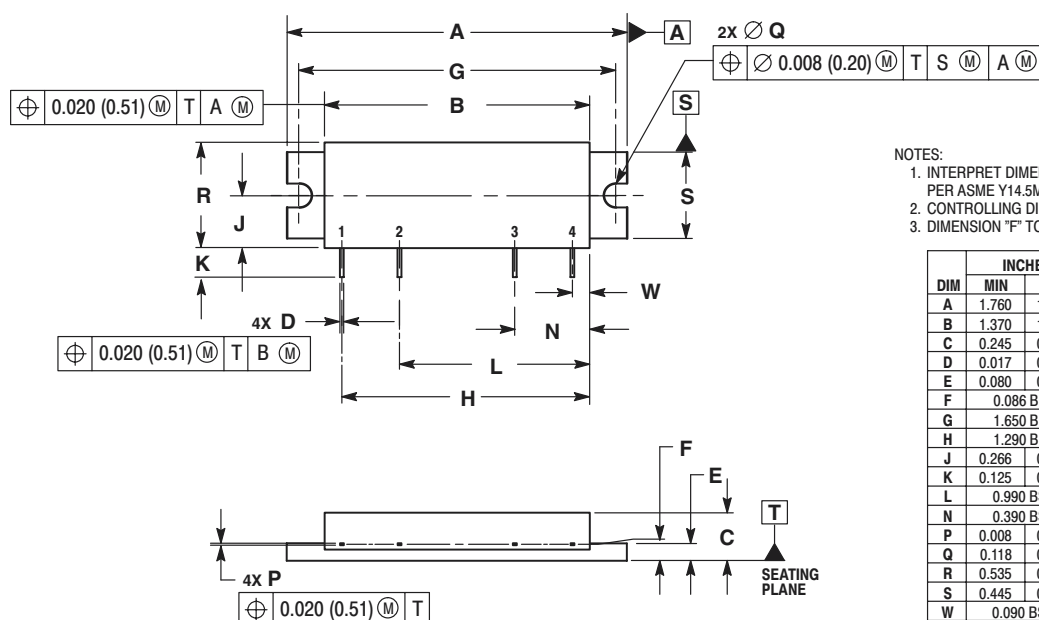
Chapter Nine

Packaging Information

The packaging availability for each device type is indicated on the individual data sheets and in the Selector Guide. All of the outline dimensions for the packages are given in this section.

Table of Contents	
	Page
Case Dimensions	9-2

Case Dimensions

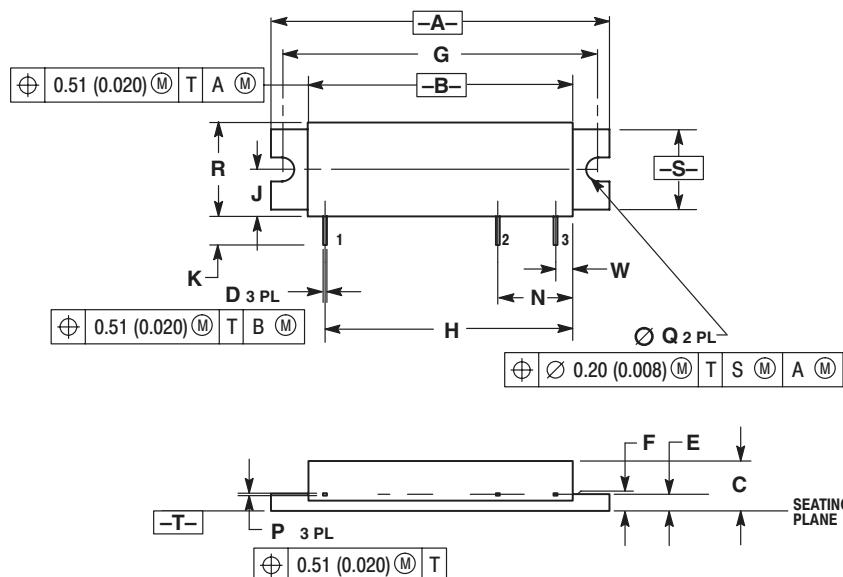


- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "F" TO CENTER OF LEADS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
L	0.990 BSC		25.15 BSC	
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

- STYLE 1: PIN 1. RF INPUT
2. VDD1
3. VDD2
4. RF OUTPUT
CASE: GROUND
- STYLE 2: PIN 1. RF OUTPUT
2. VDD2
3. VDD1
4. RF INPUT
CASE: GROUND
- STYLE 3: PIN 1. RF INPUT
2. VBIAS
3. VDD
4. RF OUTPUT
CASE: GROUND

CASE 301AP-02
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION F TO CENTER OF LEADS.

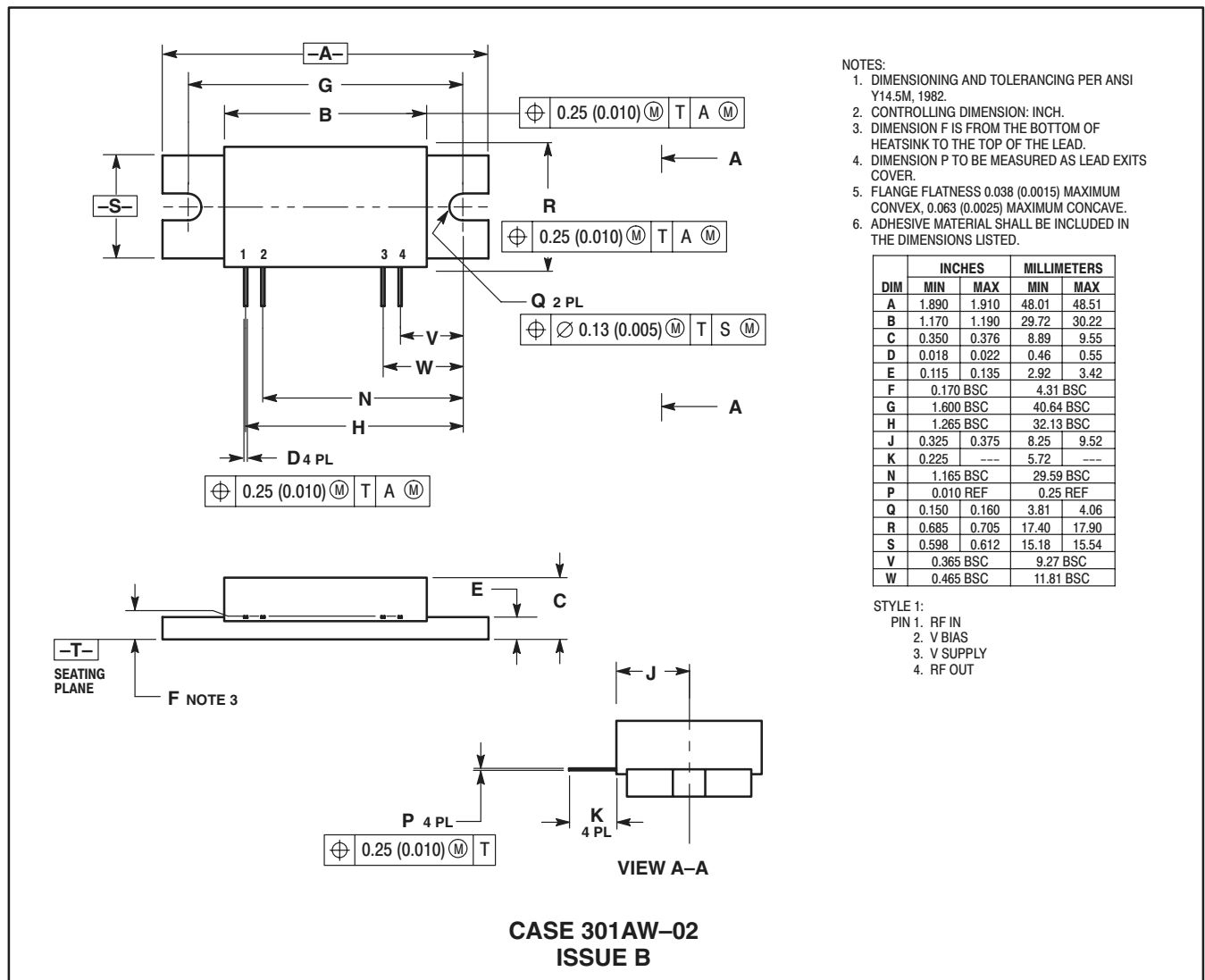
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

- STYLE 1: PIN 1. RF INPUT
2. VDD
3. RF OUTPUT
CASE: GROUND

CASE 301AS-01
ISSUE A

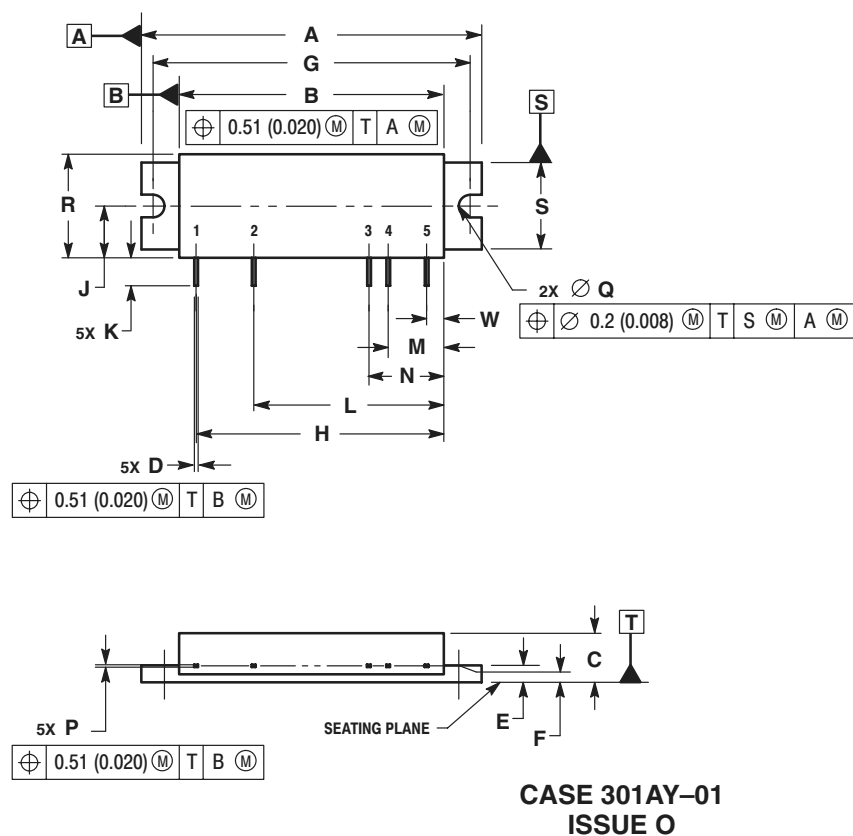
Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



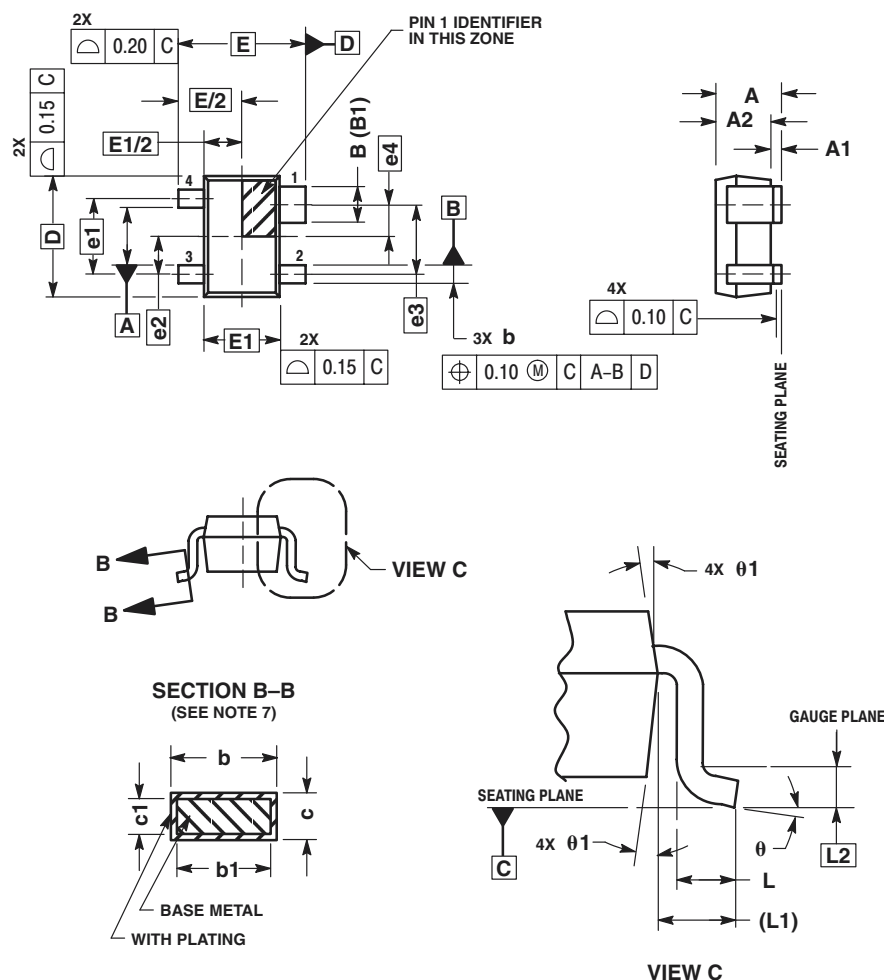
- NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
 3. DIMENSION F TO CENTER LINE OF LEADS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	44.7	45.21	1.760	1.780
B	34.8	35.31	1.370	1.390
C	6.22	6.73	0.245	0.265
D	0.43	0.58	0.017	0.023
E	2.03	2.54	0.080	0.100
F	2.18 BSC		0.086 BSC	
G	41.91 BSC		1.650 BSC	
H	32.77 BSC		1.290 BSC	
J	6.76	7.11	0.266	0.280
K	3.18	4.19	0.125	0.165
L	25.15 BSC		0.990 BSC	
M	7.37 BSC		0.290 BSC	
N	9.91 BSC		0.390 BSC	
P	0.2	0.33	0.008	0.013
Q	3	3.35	0.118	0.132
R	13.59	14.1	0.535	0.555
S	11.3	11.81	0.445	0.465
W	2.29 BSC		0.090 BSC	

STYLE 1:
 PIN 1. RF INPUT
 2. VDD1
 3. VDD2
 4. VDD3
 5. RF OUTPUT
 CASE: GROUND

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



NOTES:

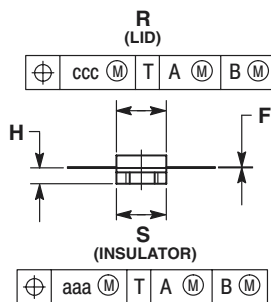
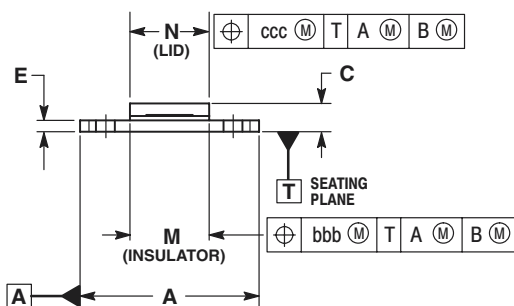
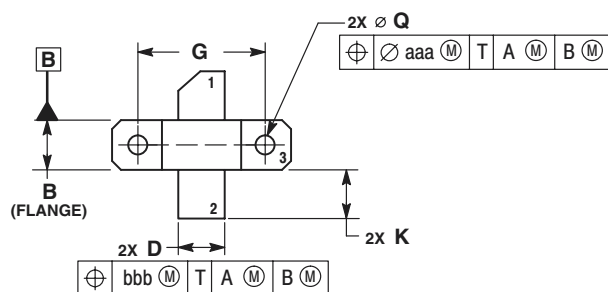
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm PER SIDE.
4. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF PLASTIC BODY.
5. DATUMS A, B AND D TO BE DETERMINED 0.10mm FROM THE LEAD TIP.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08mm AND 0.15mm FROM THE LEAD TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	---	1.10
A1	0.00	0.10
A2	0.80	1.00
b	0.25	0.40
b1	0.25	0.35
B	0.55	0.70
B1	0.55	0.65
c	0.10	0.25
c1	0.08	0.20
D	2.00 BSC	
E	2.10 BSC	
E1	1.25 BSC	
e1	1.30 BSC	
e2	0.65 BSC	
e3	1.15 BSC	
e4	0.50 BSC	
L	0.26	0.46
L1	0.425 REF	
L2	0.15 BSC	
θ	0°	8°
θ1	4°	10°

**CASE 318M-01
ISSUE O
SOT-343**

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)

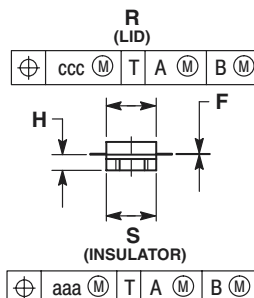
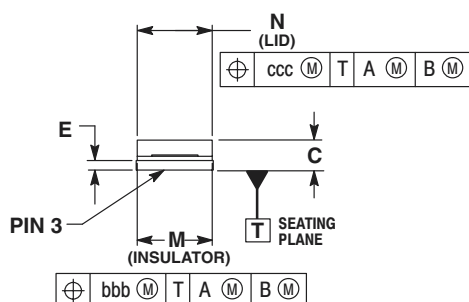
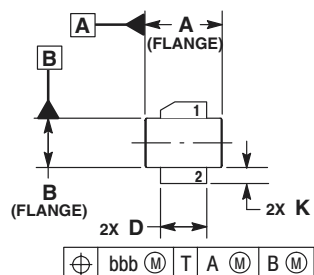


- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.795	0.805	20.19	20.45
B	0.225	0.235	5.72	5.97
C	0.125	0.175	3.18	4.45
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.10	0.15
G	0.562 BSC		14.28 BSC	
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
Q	0.125	0.135	3.18	3.43
R	0.227	0.233	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

- STYLE 1:
- PIN 1. DRAIN
 - GATE
 - SOURCE

**CASE 360B-05
ISSUE F
NI-360**



- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

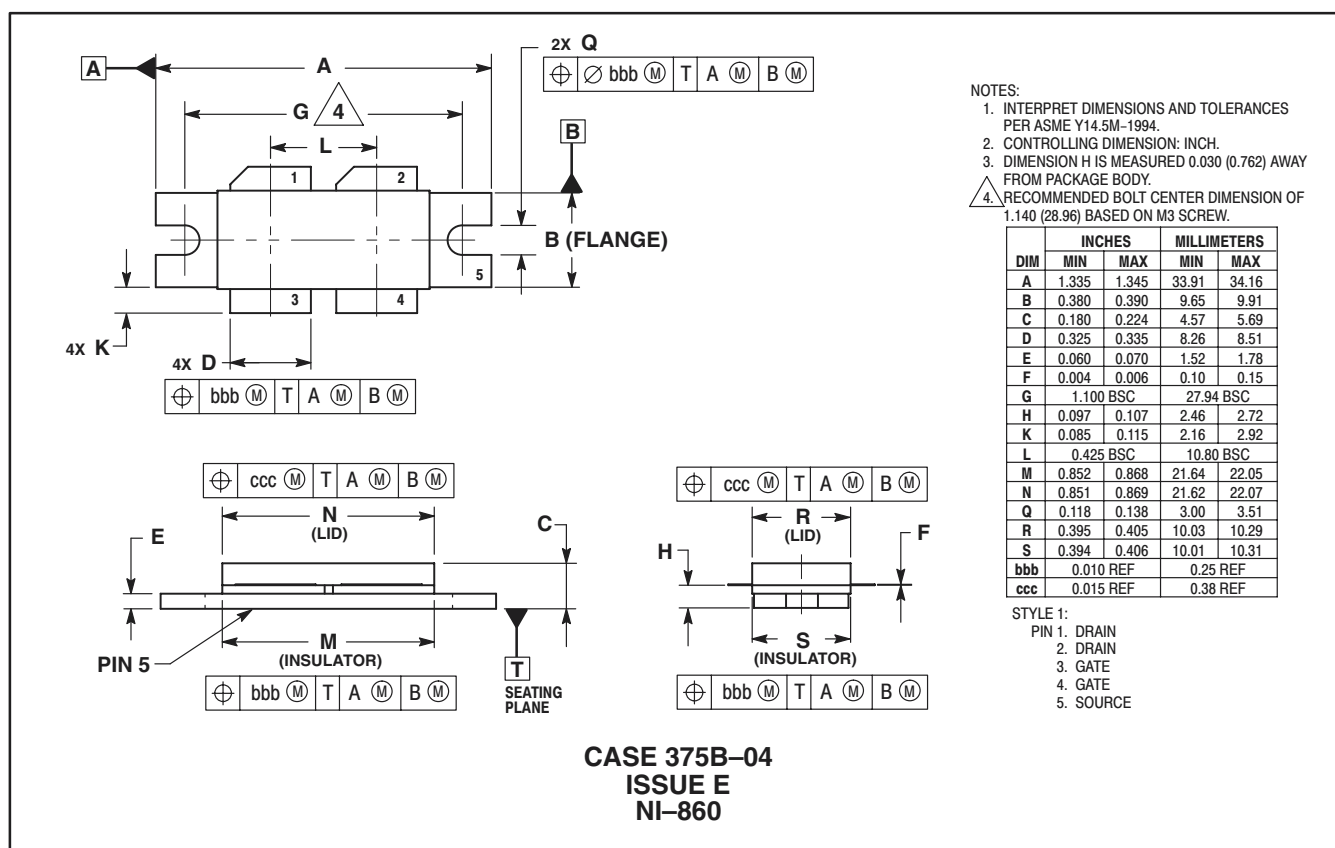
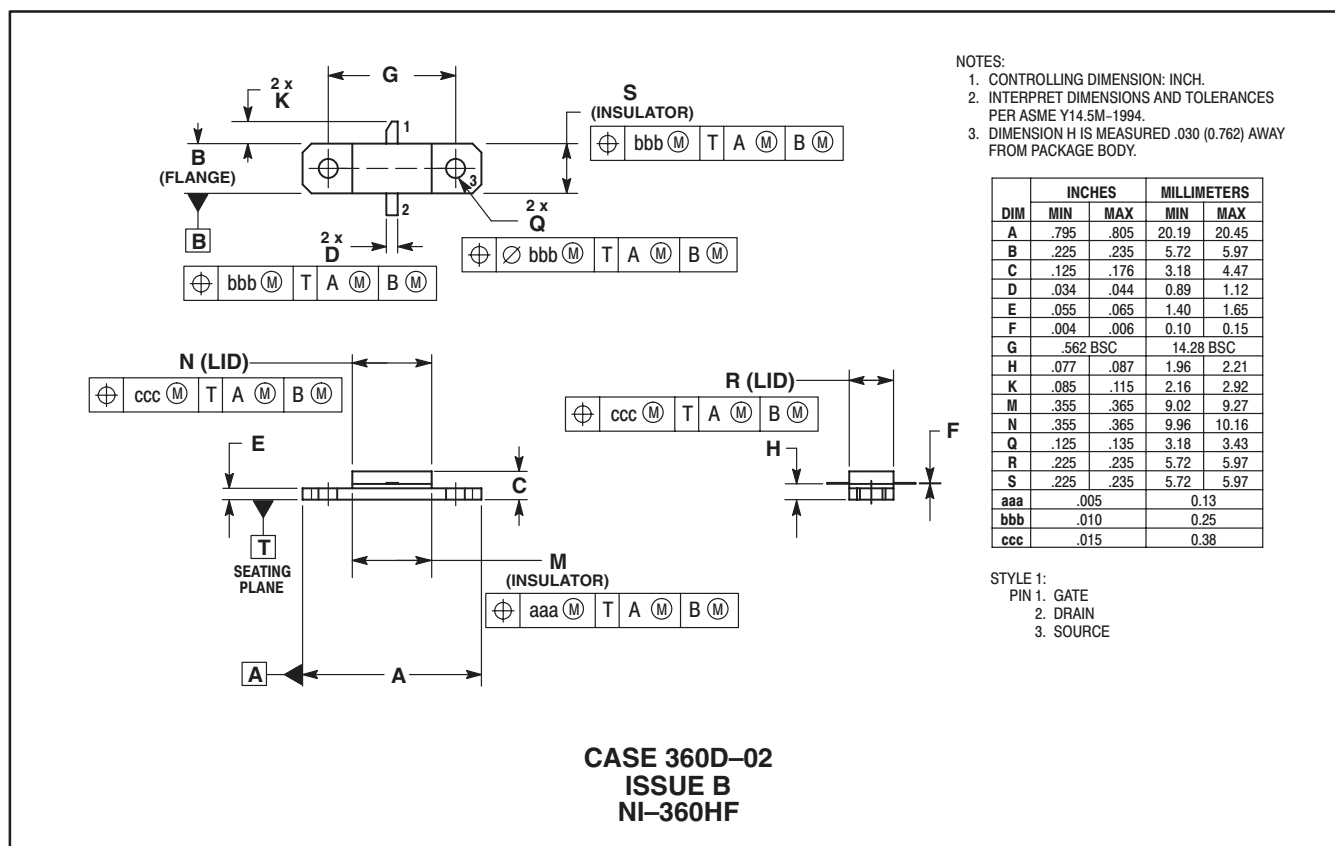
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.375	0.385	9.53	9.78
B	0.225	0.235	5.72	5.97
C	0.105	0.155	2.67	3.94
D	0.210	0.220	5.33	5.59
E	0.035	0.045	0.89	1.14
F	0.004	0.006	0.10	0.15
H	0.057	0.067	1.45	1.70
K	0.085	0.115	2.16	2.92
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
R	0.227	0.23	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

- STYLE 1:
- PIN 1. DRAIN
 - GATE
 - SOURCE

**CASE 360C-05
ISSUE D
NI-360S**

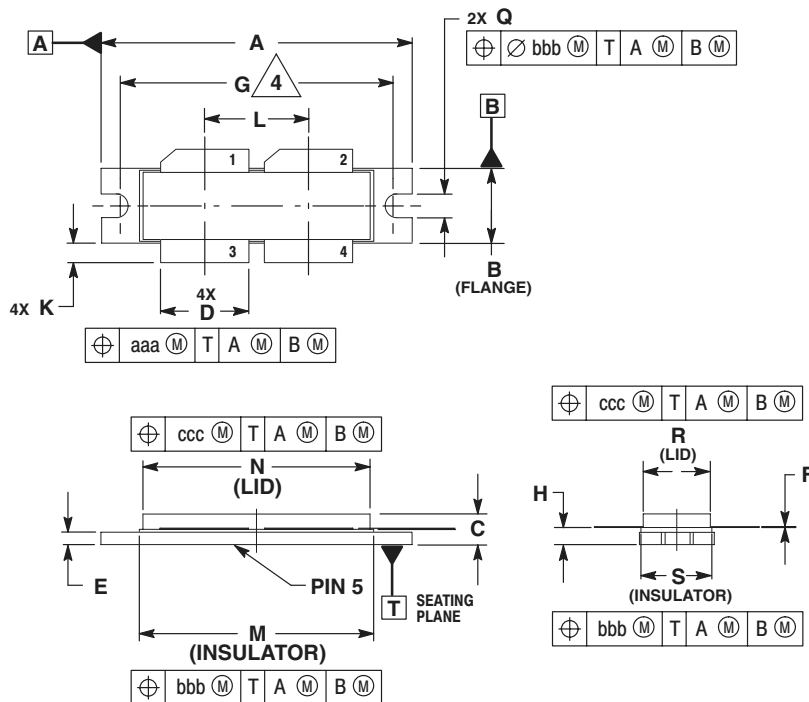
Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)

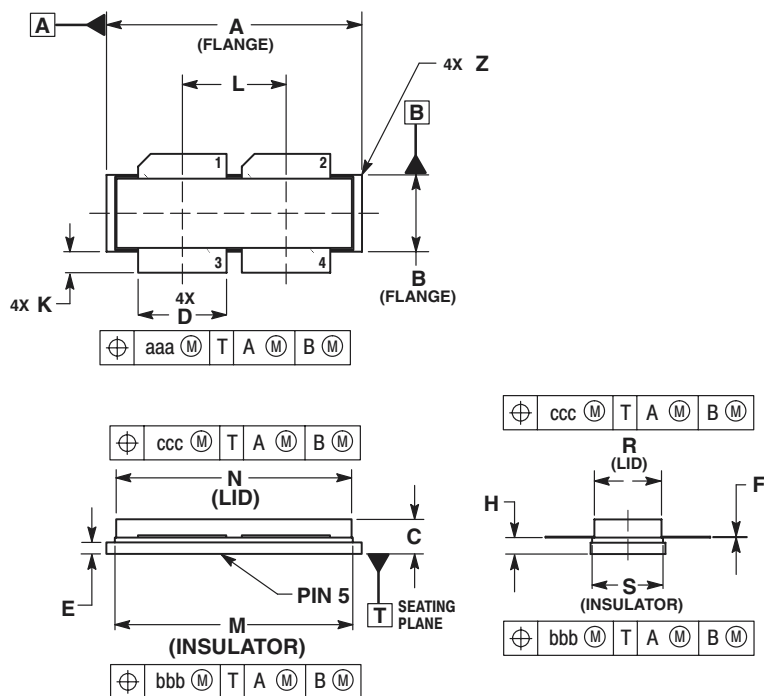


- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
 4. RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.28
B	0.395	0.405	10.03	10.29
C	0.150	0.200	3.81	5.08
D	0.455	0.465	11.56	11.81
E	0.062	0.066	1.57	1.68
F	0.004	0.007	0.10	0.18
G	1.400 BSC		35.56 BSC	
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.219	1.241	30.96	31.52
N	1.218	1.242	30.94	31.55
Q	0.120	0.130	3.05	3.30
R	0.355	0.365	9.01	9.27
S	0.365	0.375	9.27	9.53
aaa	0.013 REF		0.33 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.020 REF		0.51 REF	

- STYLE 1:
1. DRAIN
 2. DRAIN
 3. GATE
 4. GATE
 5. SOURCE

CASE 375D-04
ISSUE C
NI-1230



- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

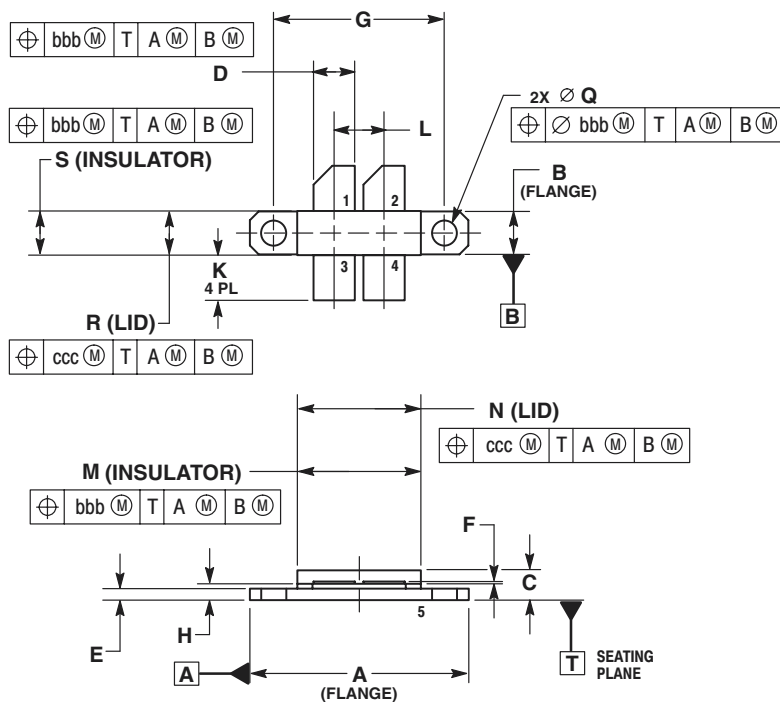
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.325	1.335	33.66	33.91
B	0.395	0.405	10.03	10.29
C	0.150	0.200	3.81	5.08
D	0.455	0.465	11.56	11.81
E	0.062	0.066	1.57	1.68
F	0.004	0.007	0.10	0.18
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.219	1.241	30.96	31.52
N	1.218	1.242	30.94	31.55
R	0.355	0.365	9.01	9.27
S	0.365	0.375	9.27	9.53
Z	0	0.040	0	1.02
aaa	0.013 REF		0.33 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.020 REF		0.51 REF	

- STYLE 1:
1. DRAIN
 2. DRAIN
 3. GATE
 4. GATE
 5. SOURCE

CASE 375E-03
ISSUE C
NI-1230S

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



NOTES:

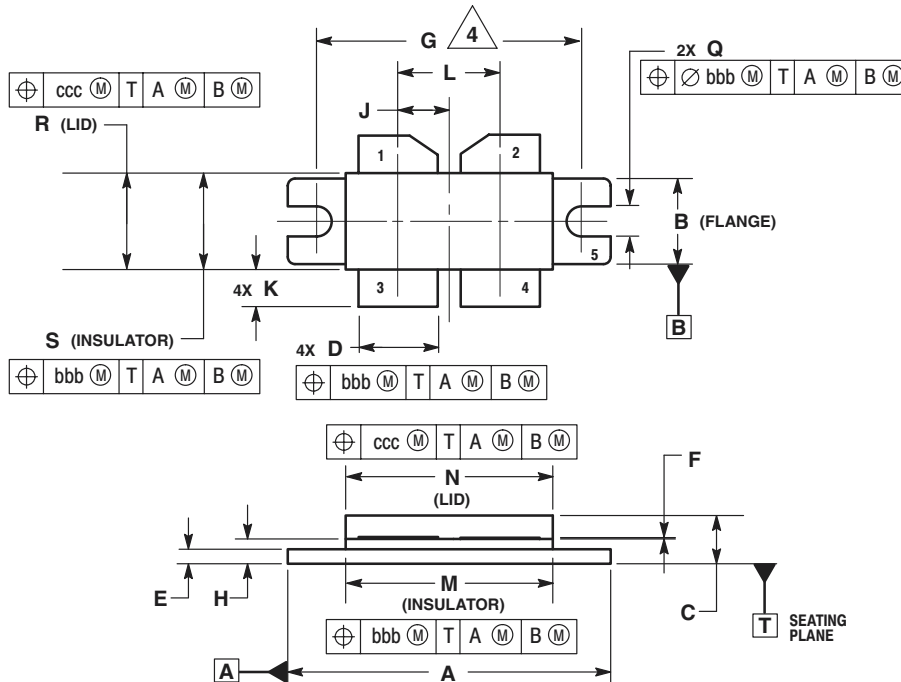
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.135	1.145	28.80	29.10
B	0.225	0.235	5.72	5.97
C	0.135	0.178	3.43	4.52
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.11	0.15
G	0.900		22.86	BSC
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
L	0.260		6.60	BSC
M	0.643	0.657	16.33	16.69
N	0.638	0.650	16.20	16.50
Q	0.125	0.135	3.175	3.43
R	0.227	0.233	5.77	5.92
S	0.225	0.235	5.715	5.97
bbb	0.010		0.254	BSC
ccc	0.015		0.381	BSC

STYLE 1:

- PIN 1. DRAIN
- PIN 2. DRAIN
- PIN 3. GATE
- PIN 4. GATE
- PIN 5. SOURCE

**CASE 375F-04
ISSUE D
NI-650**



NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSION H TO BE MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.140 (28.96) BASED ON 3M SCREW.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.180	0.224	4.57	5.69
D	0.325	0.335	8.26	8.51
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	1.100		27.94	BSC
H	0.097	0.107	2.46	2.72
J	0.2125		5.397	BSC
K	0.135	0.165	3.43	4.19
L	0.425		10.8	BSC
M	0.852	0.868	21.64	22.05
N	0.851	0.869	21.62	22.07
Q	0.118	0.138	3.00	3.30
R	0.395	0.405	10.03	10.29
S	0.394	0.406	10.01	10.31
bbb	0.010		0.25	REF
ccc	0.015		0.38	REF

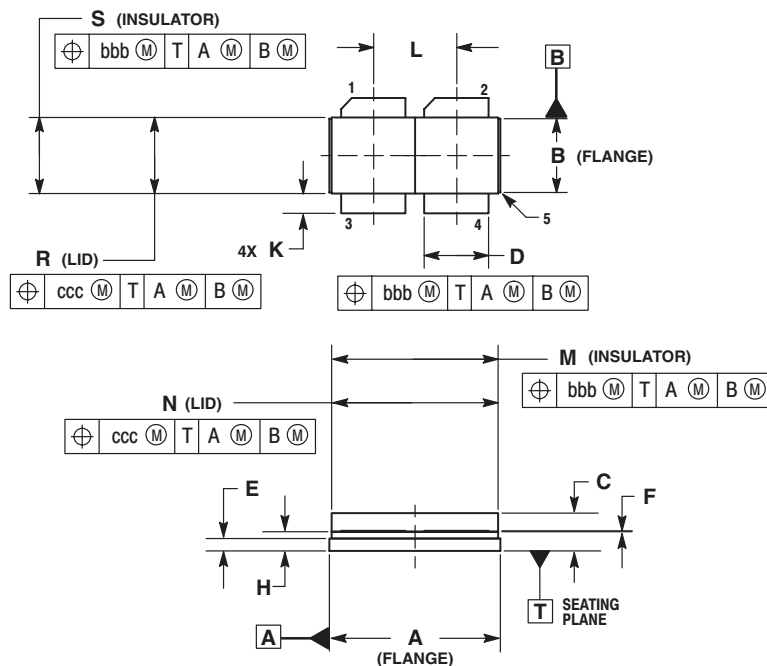
STYLE 1:

- PIN 1. DRAIN
- PIN 2. DRAIN
- PIN 3. GATE
- PIN 4. GATE
- PIN 5. SOURCE

**CASE 375G-04
ISSUE E
NI-860C3**

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)

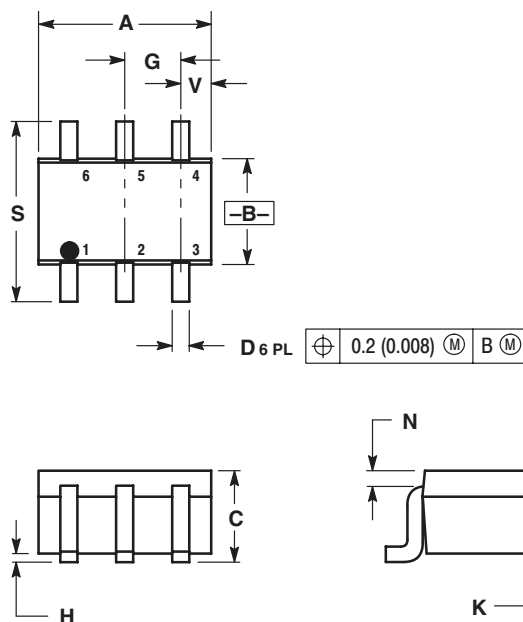


- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "H" TO BE MEASURED 0.030 (0.762) INCHES FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.885	.895	22.48	22.73
B	.380	.390	9.65	9.91
C	.180	.224	4.57	5.69
D	.325	.335	8.26	8.51
E	.060	.070	1.52	1.78
F	.004	.006	0.10	0.15
H	.097	.107	2.46	2.72
K	.085	.115	2.16	2.92
L	.425 BSC		10.8 BSC	
M	.852	.868	21.64	22.05
N	.851	.869	21.62	22.07
R	.395	.405	10.03	10.29
S	.394	.406	10.01	10.31
bbb	.010 REF		0.25 REF	
ccc	.015 REF		0.38 REF	

- STYLE 1:
- PIN 1: DRAIN
 - DRAIN
 - GATE
 - GATE
 - SOURCE

**CASE 375H-03
ISSUE B
NI-860S**



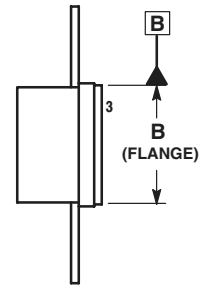
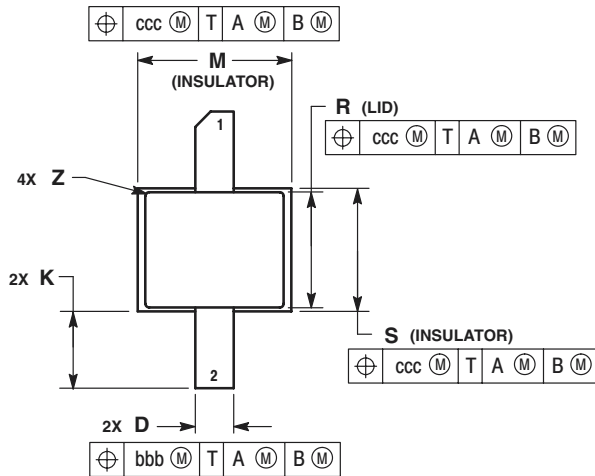
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

**CASE 419B-01
ISSUE G
SOT-363**

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



- NOTES:
1. CONTROLLING DIMENSIONS: INCHES.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. ALL DIMENSIONS ARE SYMMETRICAL ABOUT CENTERLINE UNLESS OTHERWISE NOTED.

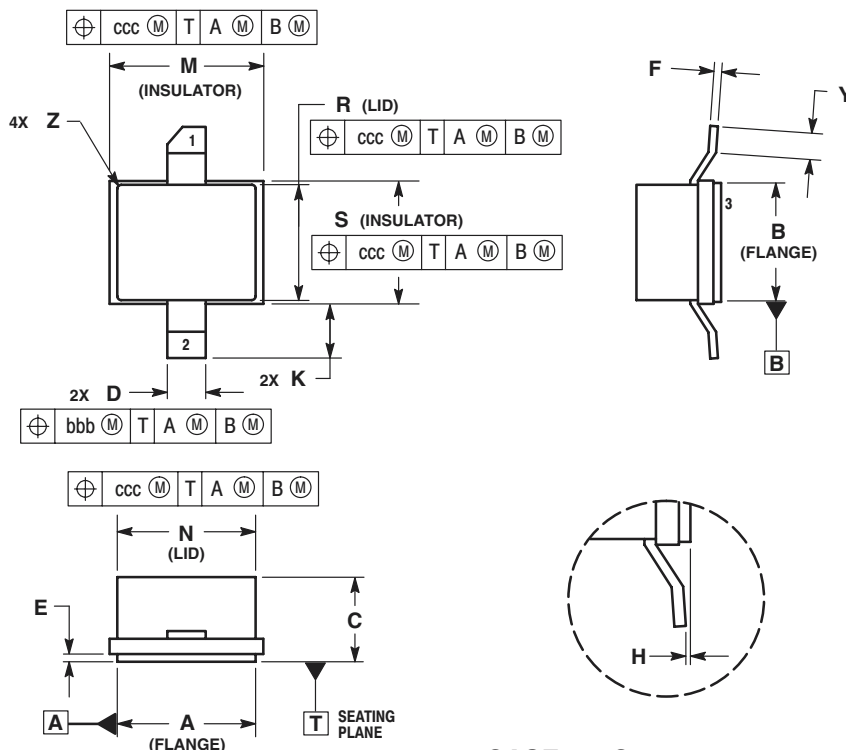
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.180	0.190	4.572	4.83
B	0.140	0.150	3.556	3.81
C	0.082	0.116	2.083	2.946
D	0.047	0.053	1.194	1.346
E	0.004	0.010	0.102	0.254
F	0.004	0.006	0.102	0.152
H	0.025	0.031	0.635	0.787
K	0.060	0.110	1.524	2.794
M	0.197	0.203	5.004	5.156
N	0.177	0.183	4.496	4.648
R	0.147	0.153	3.734	3.886
S	0.157	0.163	3.988	4.14
Z	---	0.020	---	0.508
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 458B-03
ISSUE D
NI-200S

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)

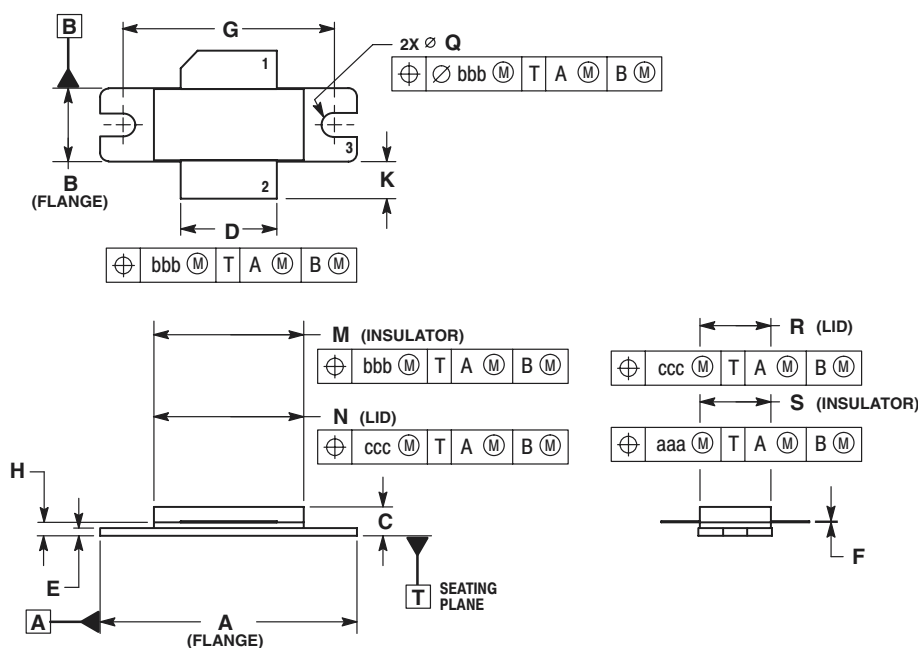


- NOTES:
1. CONTROLLING DIMENSIONS: INCHES.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSION H (PACKAGE COPLANARITY): THE BOTTOM OF LEADS AND REFERENCE PLANE T MUST BE COPLANAR WITHIN DIMENSION H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.180	0.190	4.572	4.830
B	0.140	0.150	3.556	3.810
C	0.082	0.116	2.083	2.946
D	0.047	0.053	1.194	1.346
E	0.004	0.010	0.102	0.254
F	0.004	0.006	0.102	0.152
H	0.000	0.004	0.000	0.102
K	0.050	0.090	1.270	2.286
M	0.197	0.203	5.004	5.156
N	0.177	0.183	4.496	4.648
R	0.147	0.153	3.734	3.886
S	0.157	0.163	3.988	4.140
Y	0.020	0.040	0.508	1.016
Z	---	R .020	---	R .508
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.381 REF	

- STYLE 1:
- PIN 1. DRAIN
 - GATE
 - SOURCE

CASE 458C-03
ISSUE D
NI-200Z



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DELETED
 4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

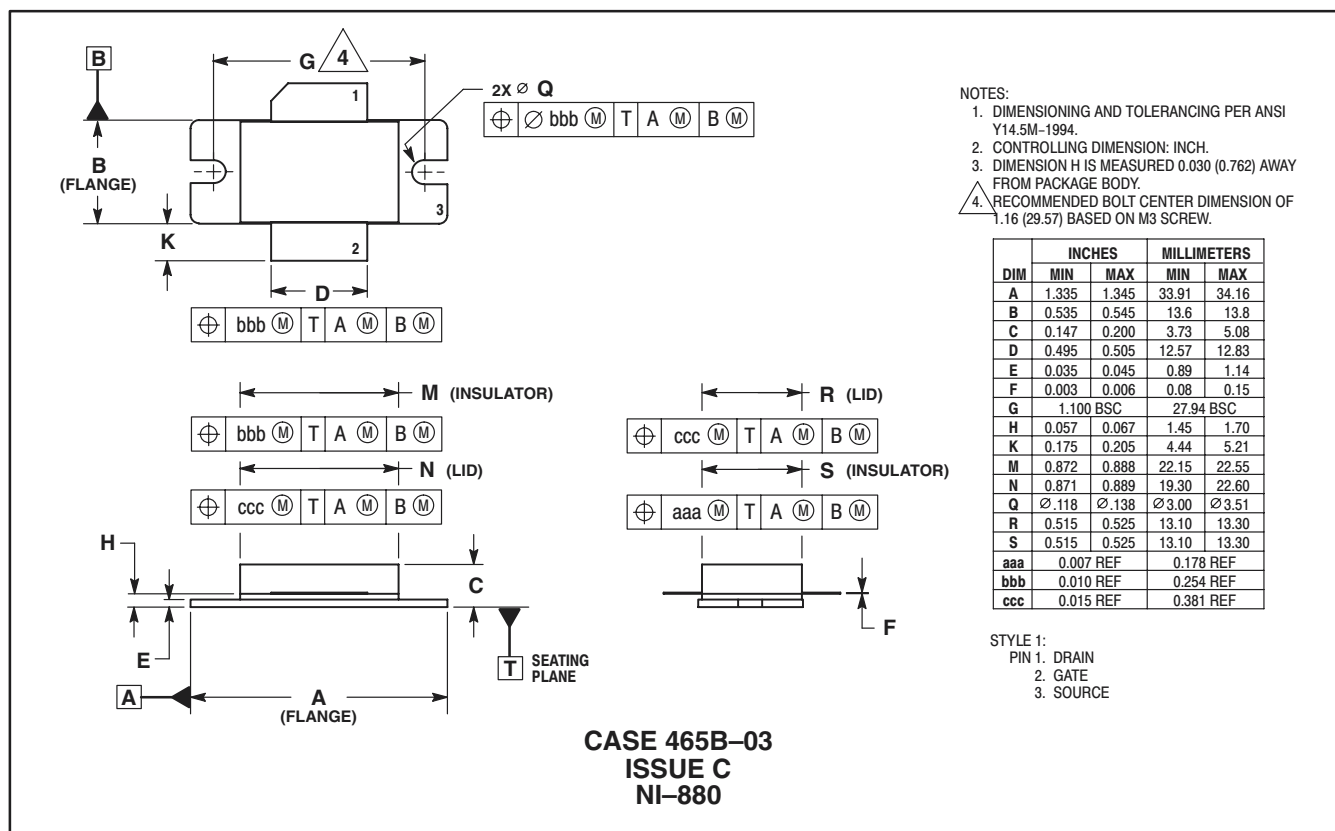
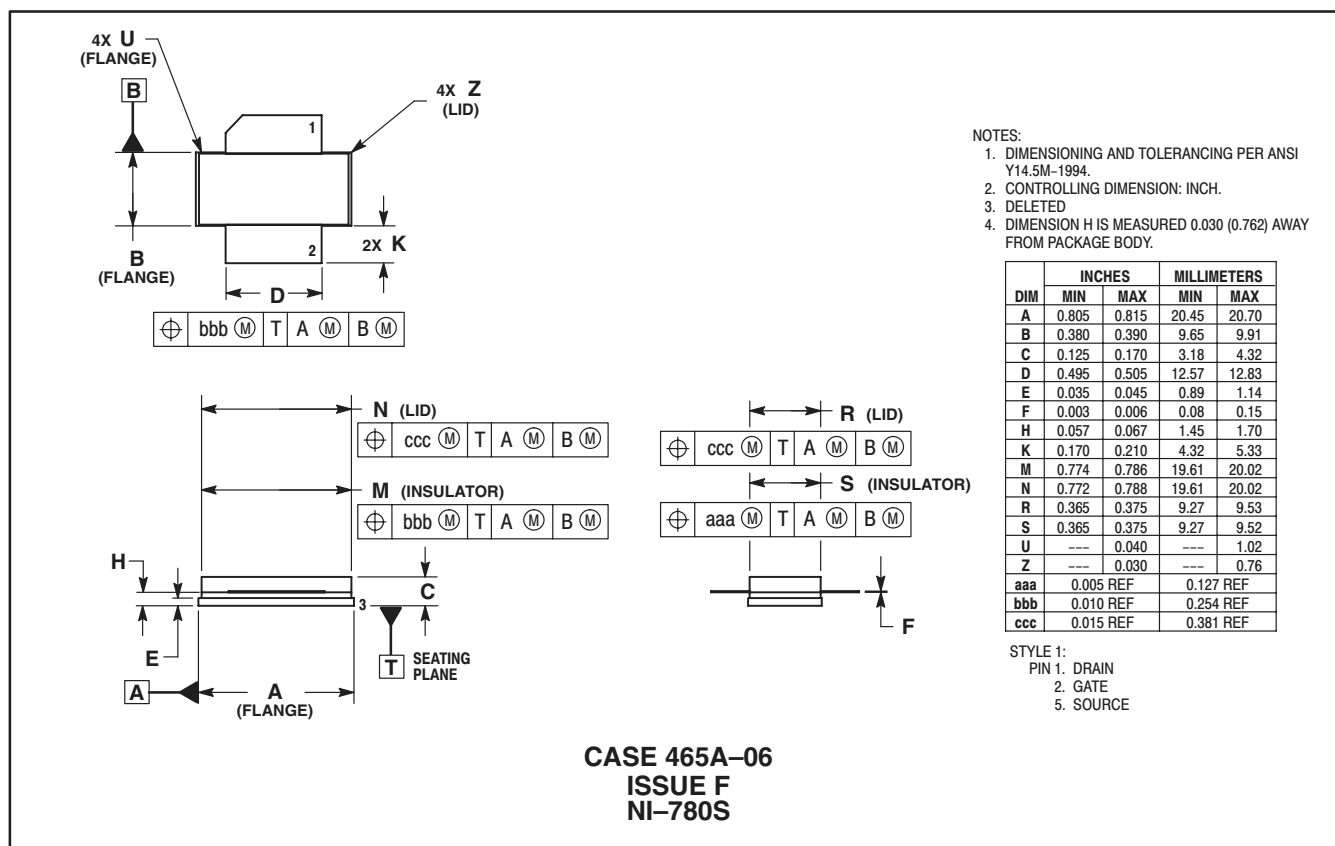
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	$\varnothing$.118	$\varnothing$.138	$\varnothing$ 3.00	$\varnothing$ 3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
- PIN 1. DRAIN
 - GATE
 - SOURCE

CASE 465-06
ISSUE F
NI-780

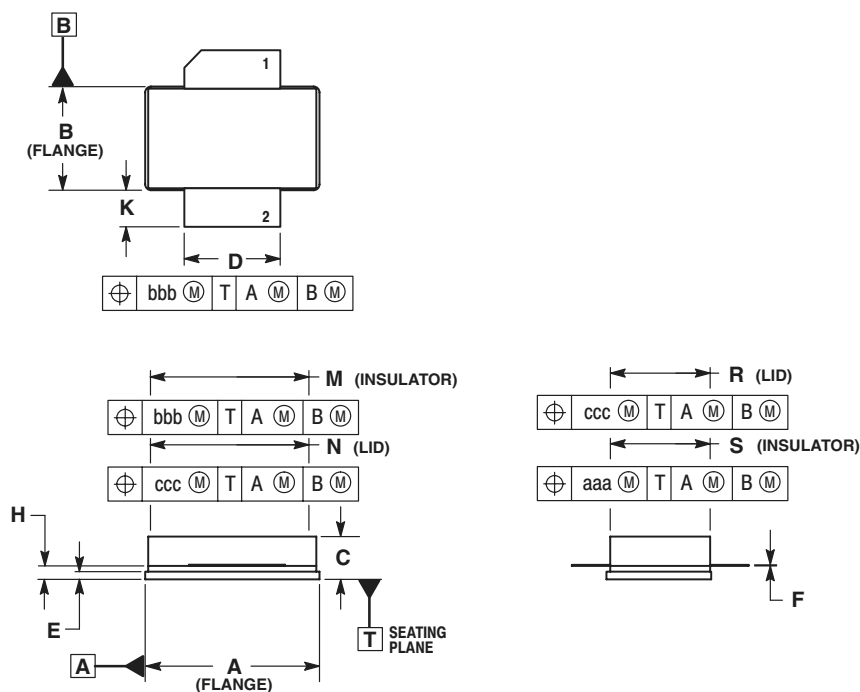
Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)

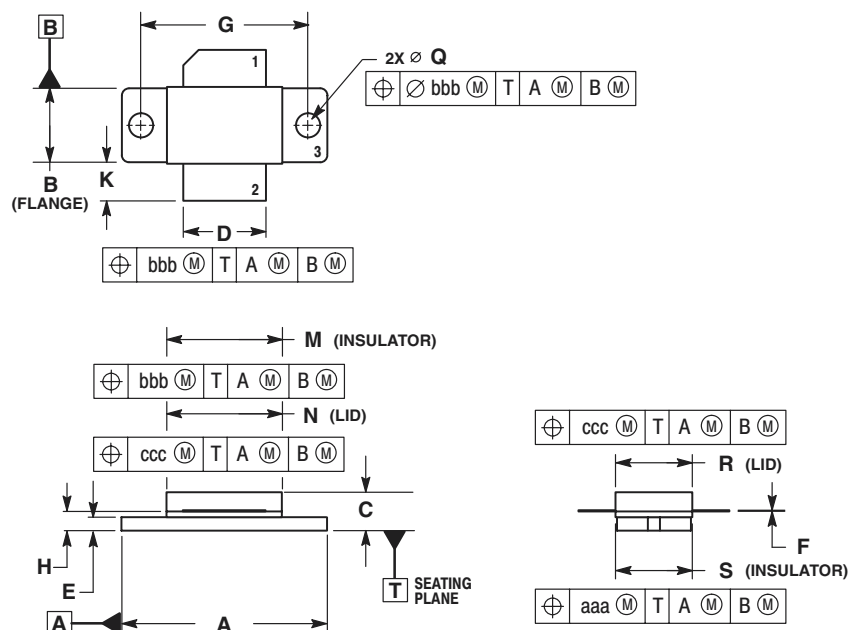


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
- PIN 1. DRAIN
 - GATE
 - SOURCE

CASE 465C-02
ISSUE A
NI-880S



- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

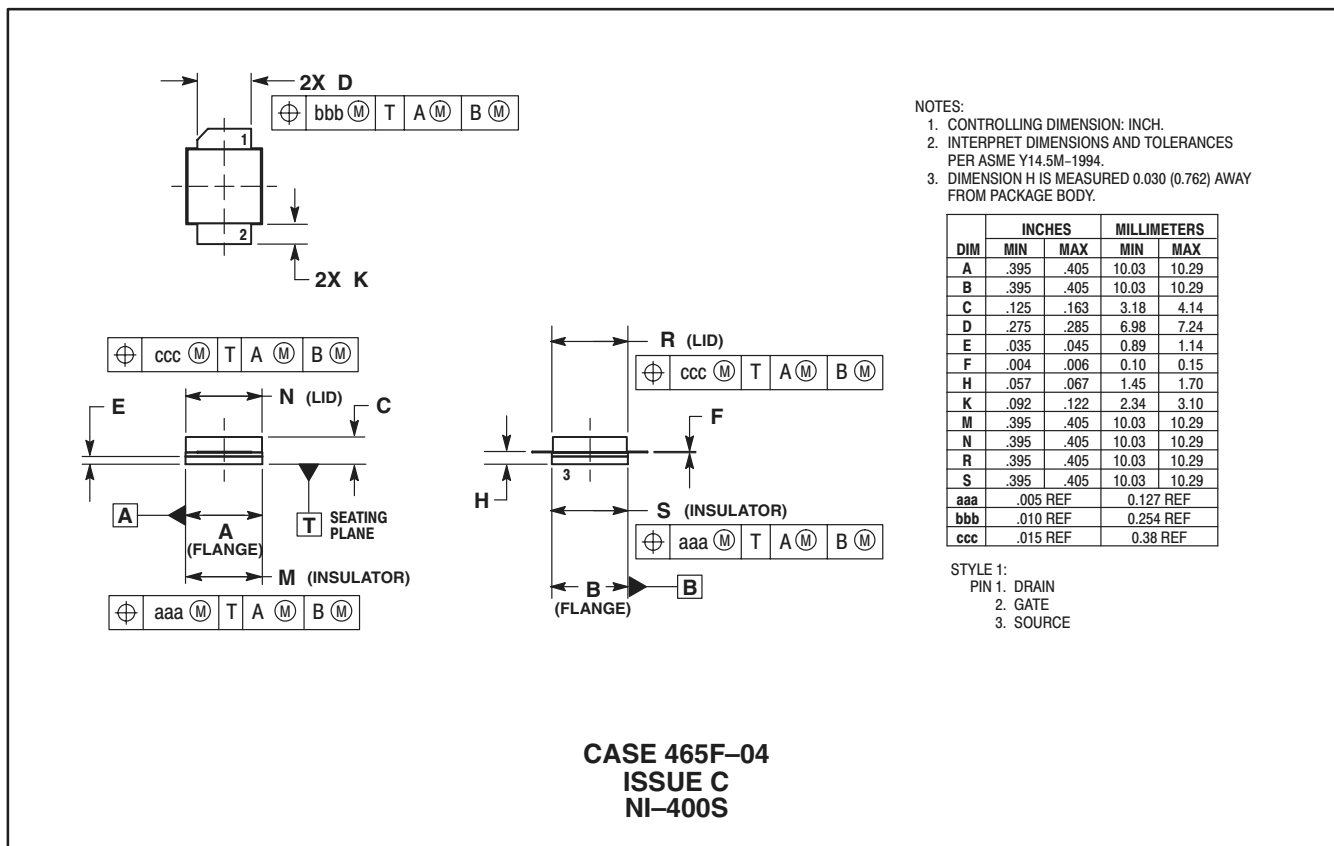
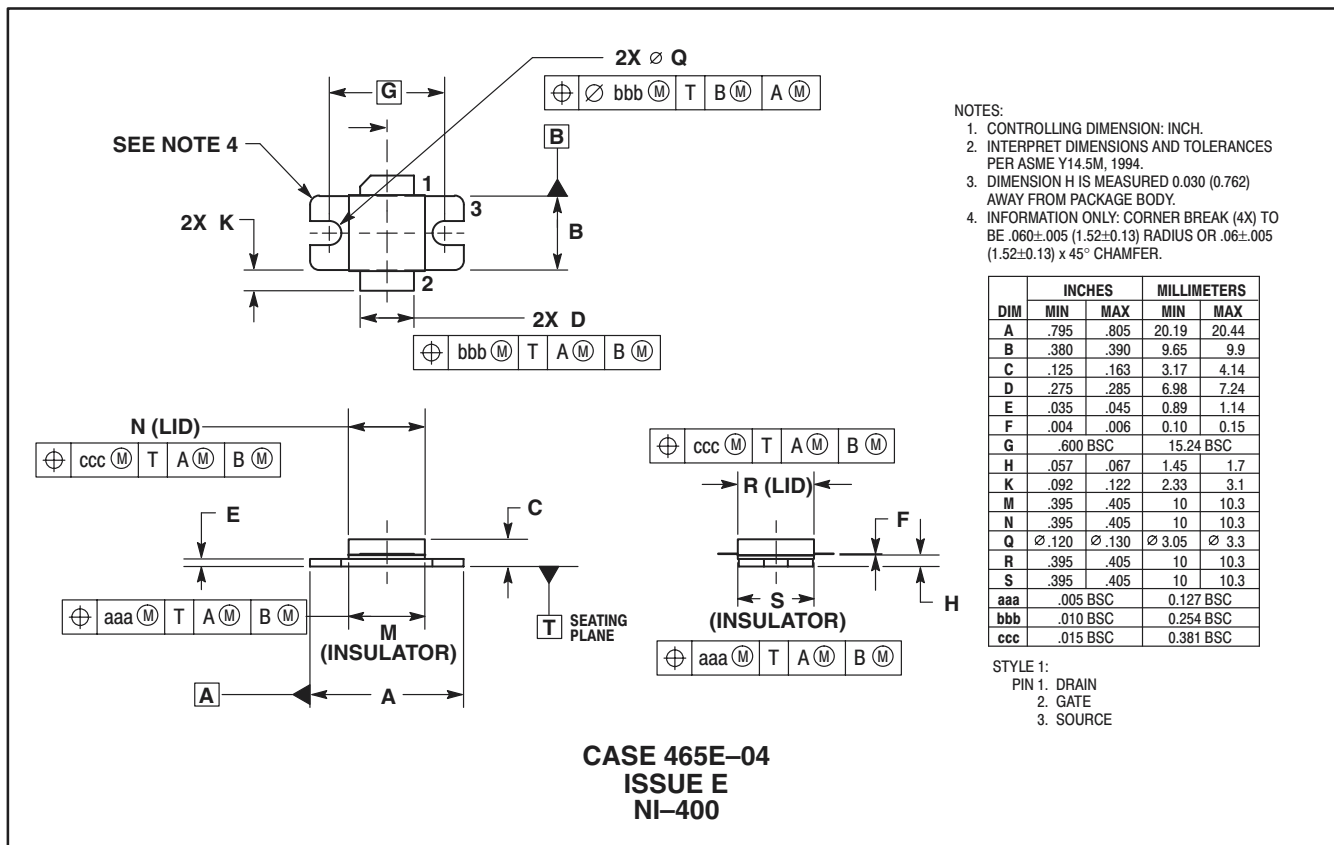
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.065	1.075	27.05	27.30
B	0.380	0.390	9.65	9.91
C	0.160	0.205	4.06	5.21
D	0.425	0.435	10.80	11.05
E	0.060	0.070	1.52	1.78
F	0.004	0.006	0.10	0.15
G	0.870 BSC		22.10 BSC	
H	0.096	0.106	2.44	2.69
K	0.190	0.223	4.83	5.66
M	0.594	0.606	15.09	15.39
N	0.591	0.601	15.01	15.27
Q	0.124	0.130	3.15	3.30
R	0.394	0.404	10.01	10.26
S	0.395	0.405	10.03	10.29
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

- STYLE 1:
- PIN 1. DRAIN
 - GATE
 - SOURCE

CASE 465D-05
ISSUE D
NI-600

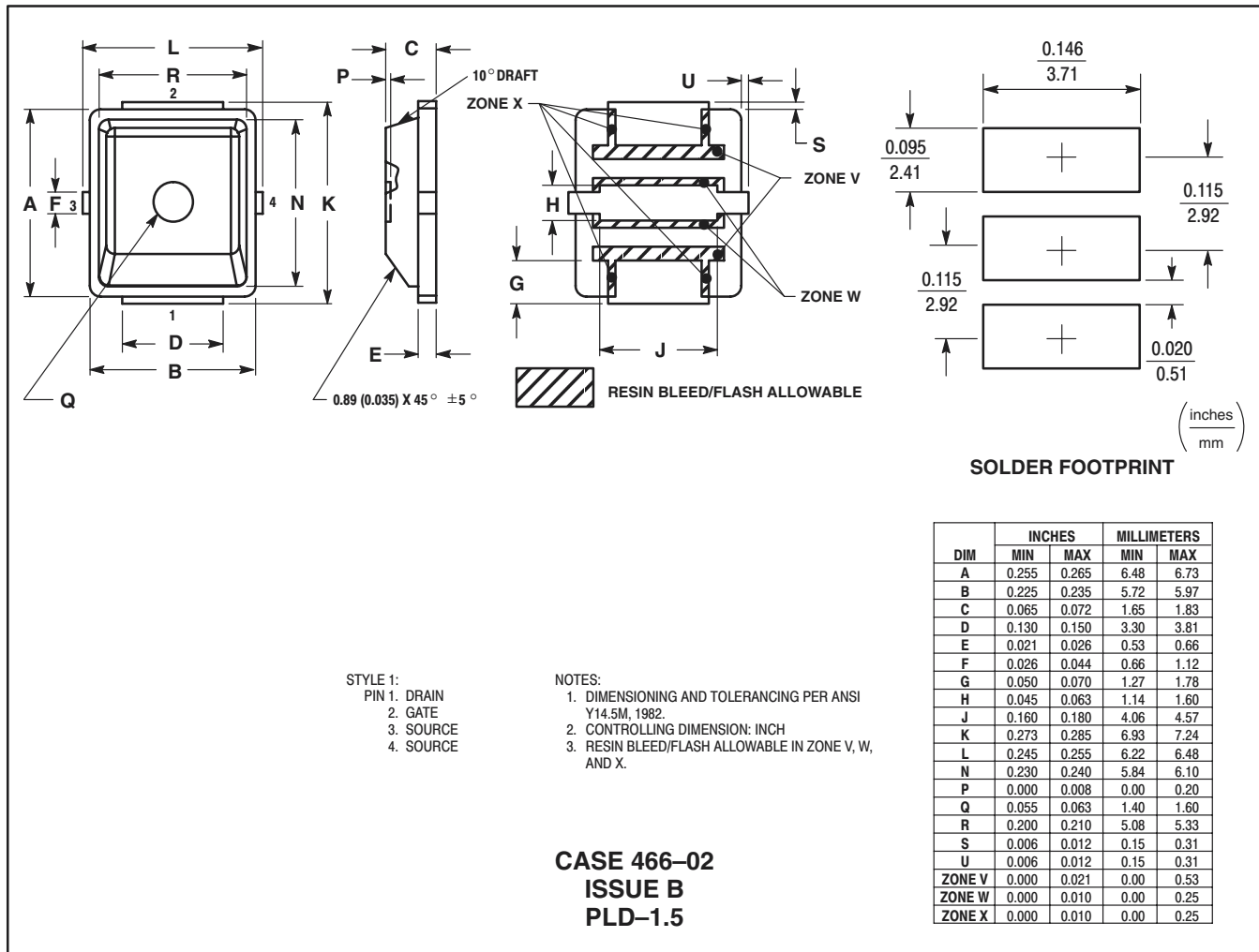
Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



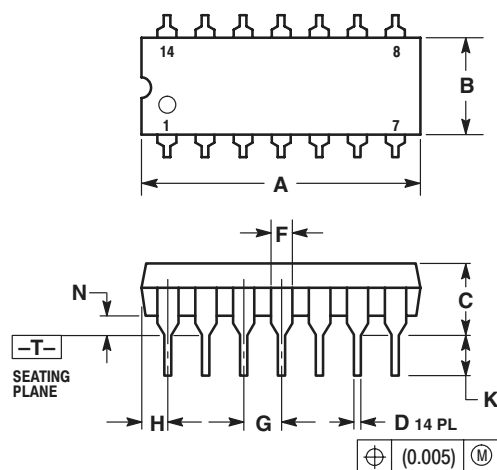
Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



Freescale Semiconductor, Inc.

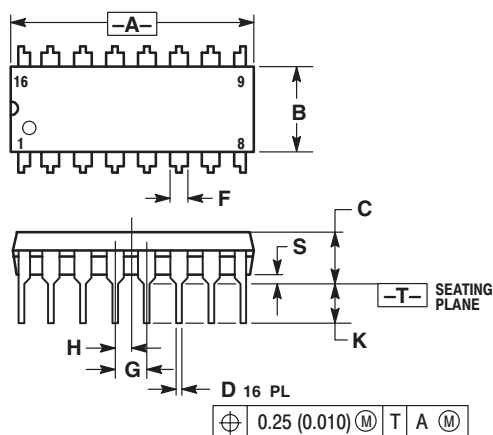
CASE DIMENSIONS (continued)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.
 6. 646-05 OBSOLETE, NEW STANDARD 646-06.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

**CASE 646-06
ISSUE N
DIP-14**



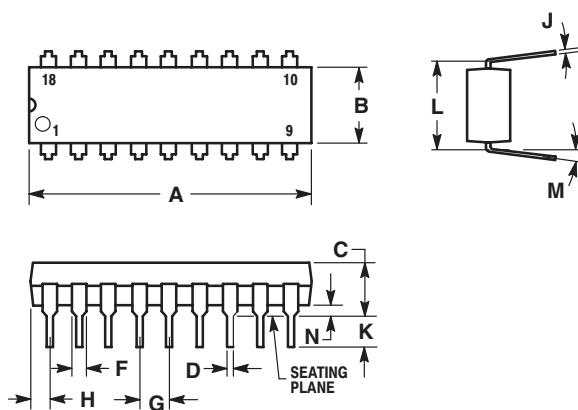
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

**CASE 648-08
ISSUE R
DIP-16**

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)

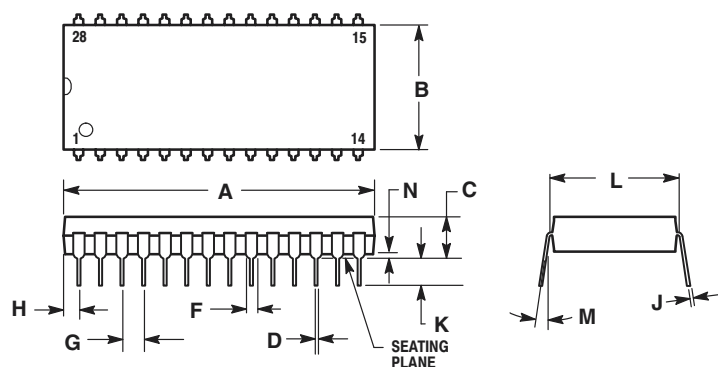


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

**CASE 707-02
ISSUE C
DIP-18**



NOTES:

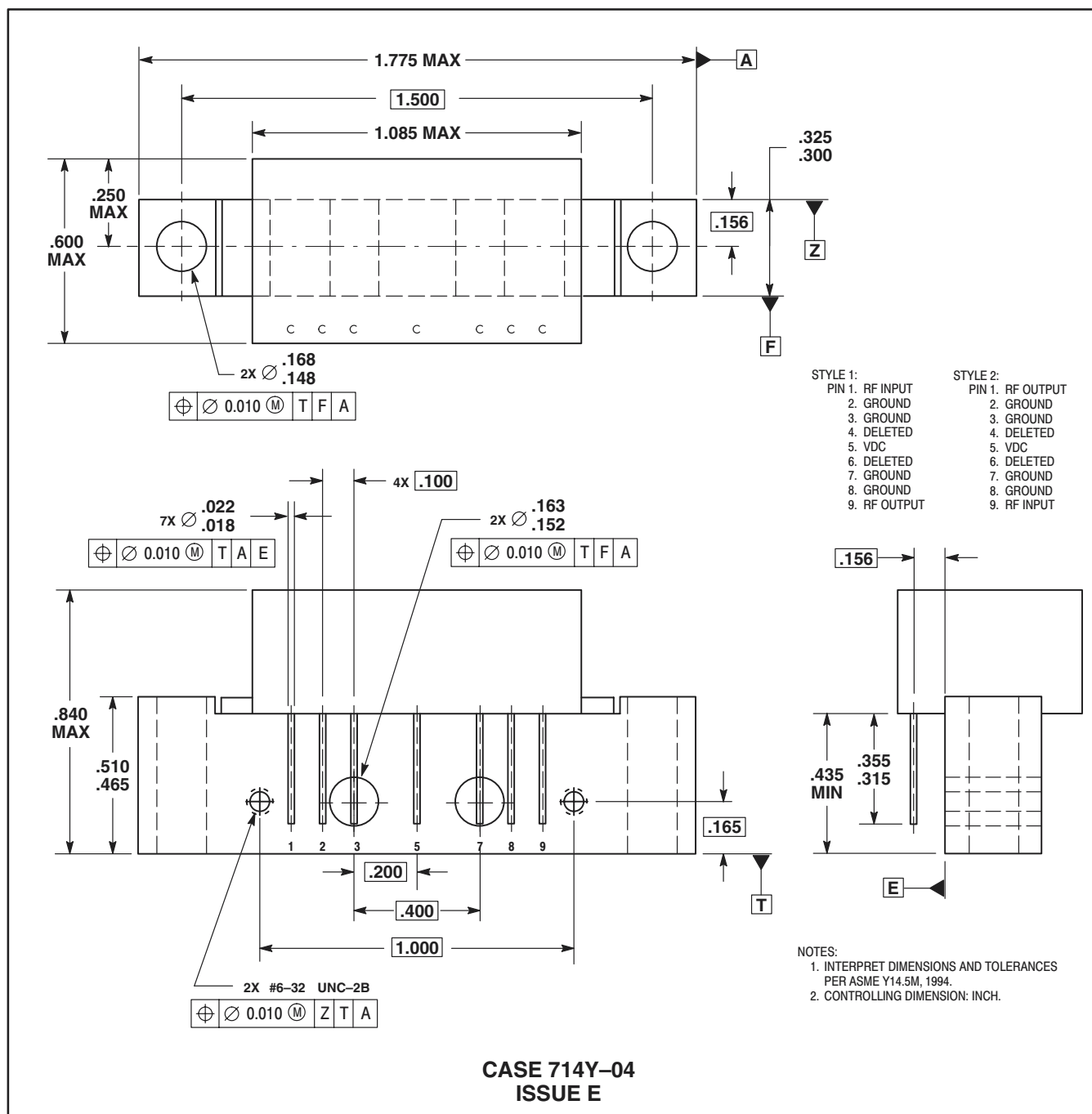
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.085	1.65	2.16
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

**CASE 710-02
ISSUE B
DIP-28**

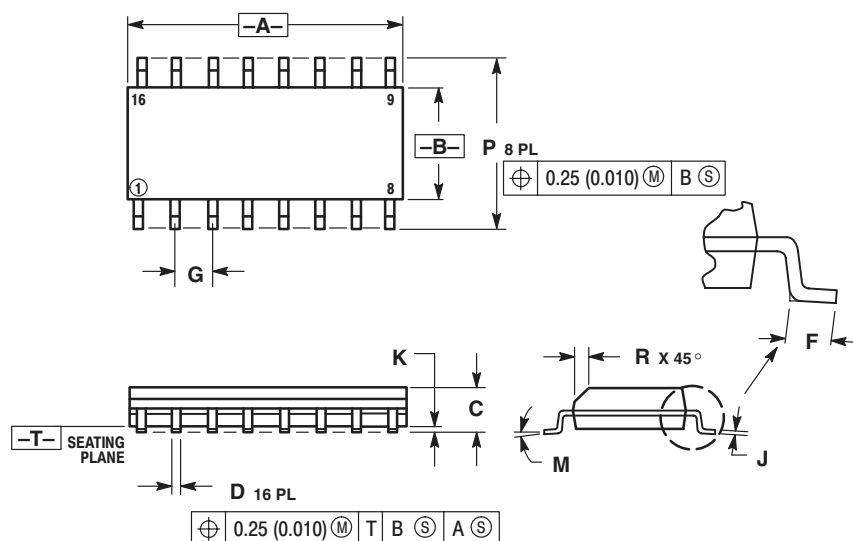
Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



Freescale Semiconductor, Inc.

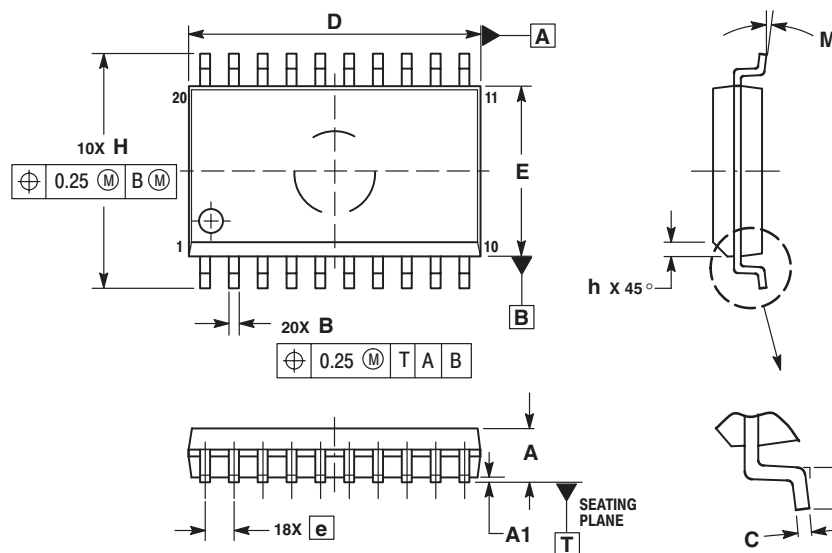
CASE DIMENSIONS (continued)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC			
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751B-05
ISSUE J
SO-16



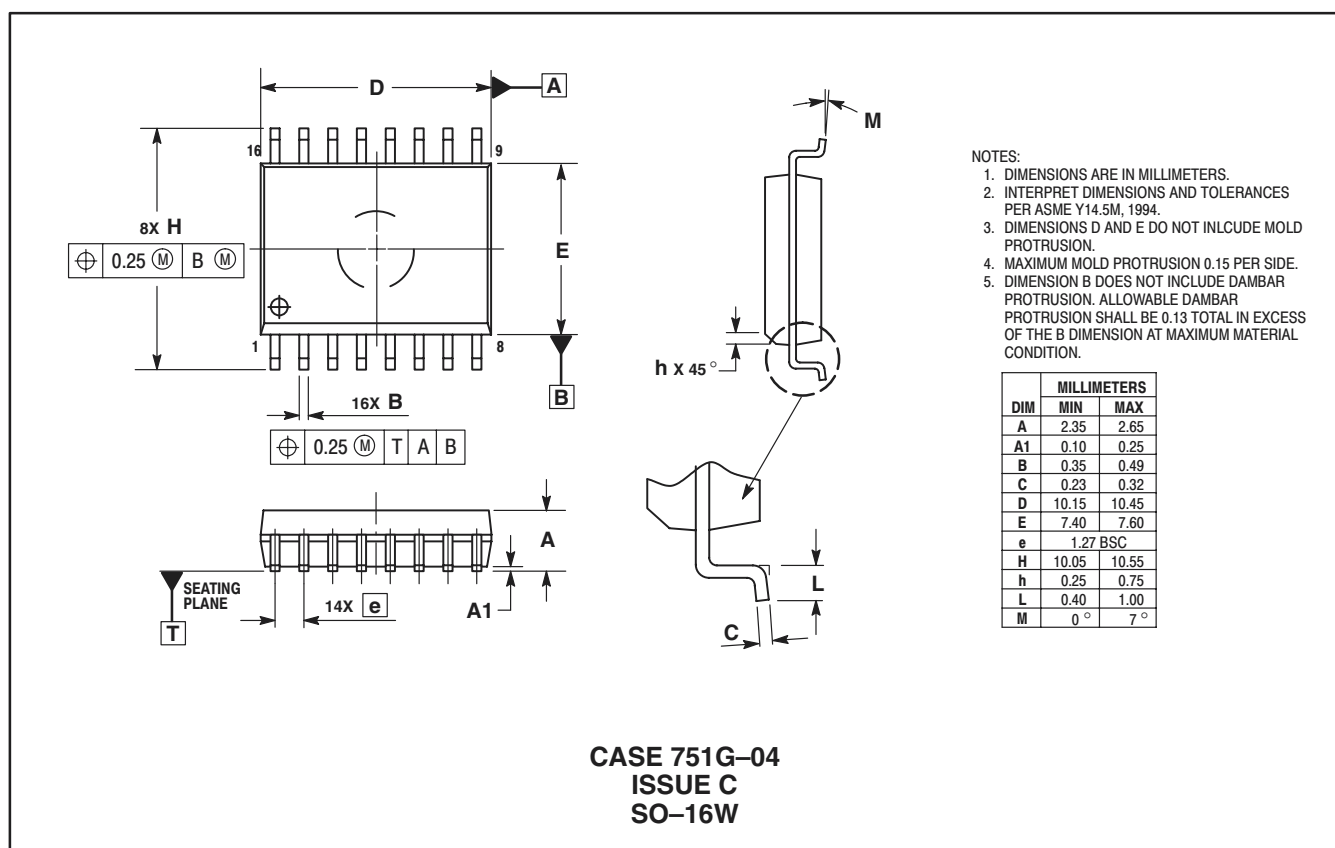
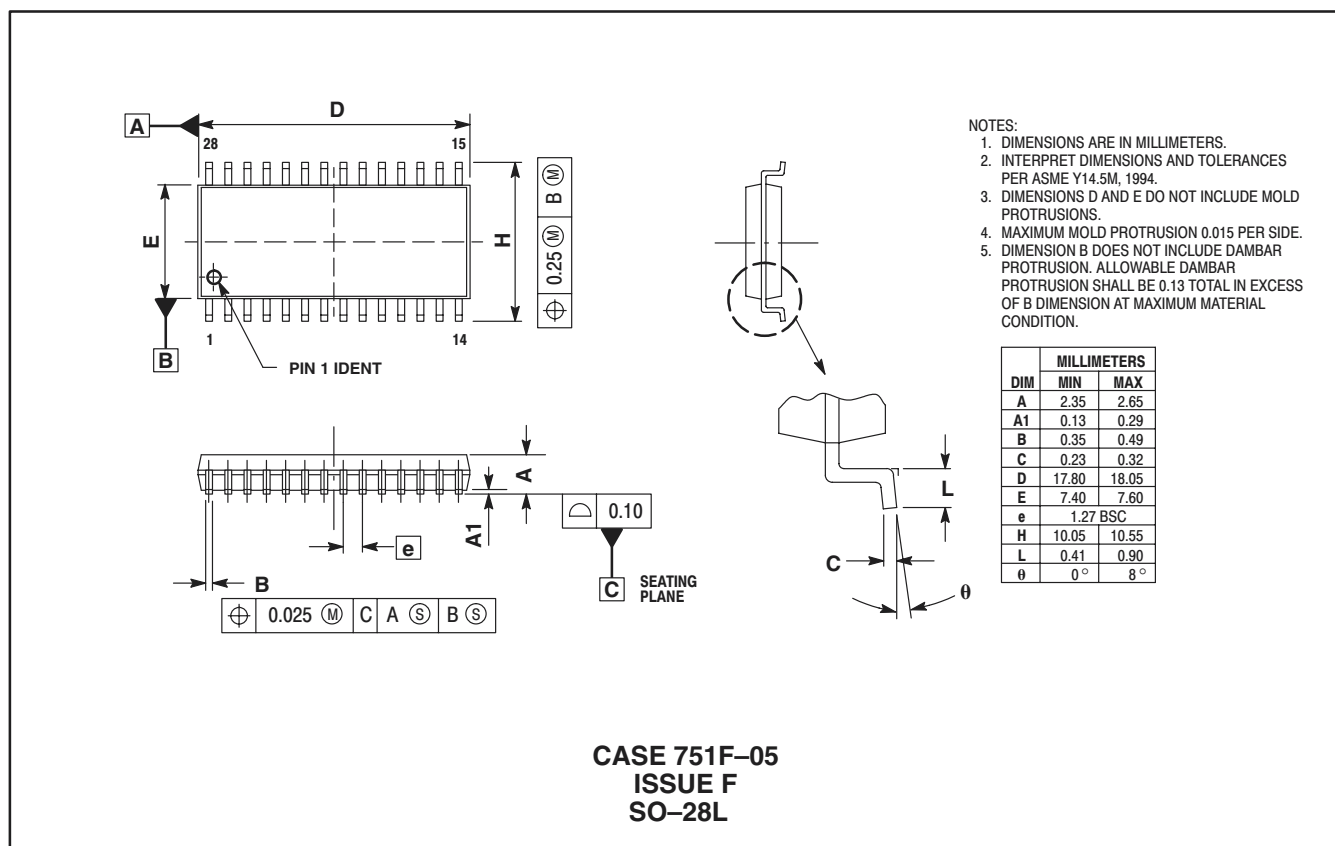
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.40	1.00
θ	0°	7°

CASE 751D-06
ISSUE G
SO-20L

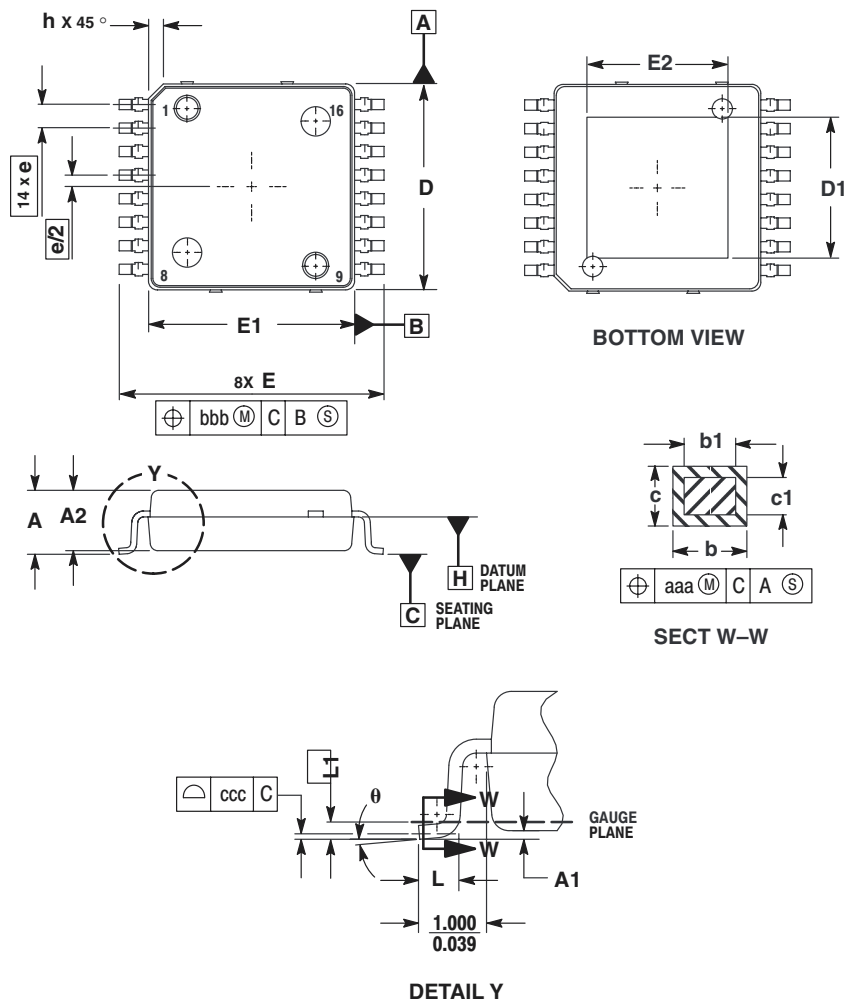
Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



NOTES:

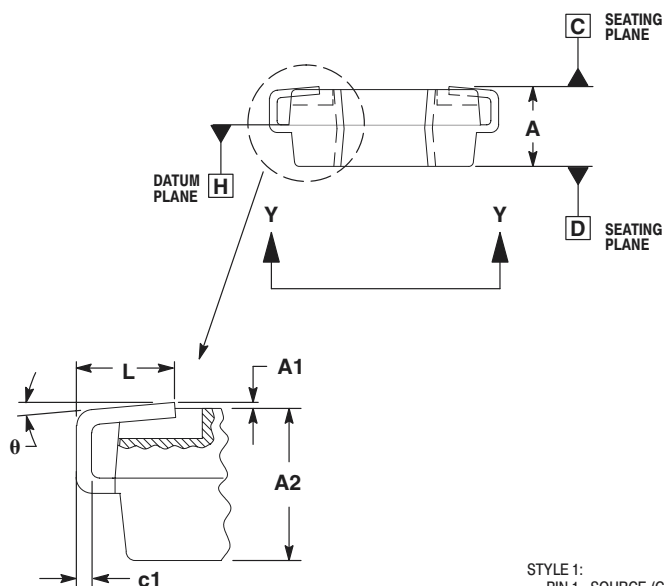
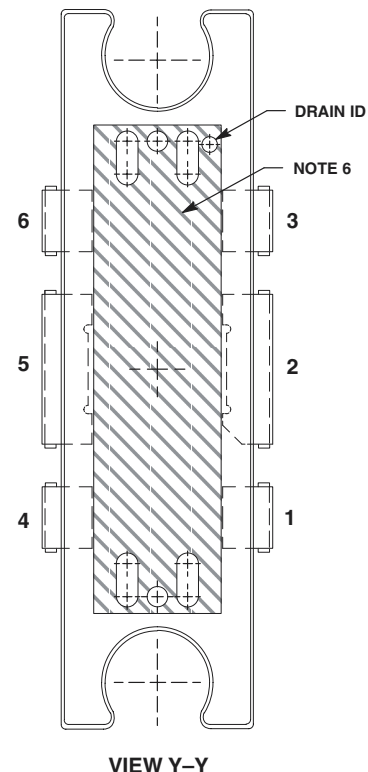
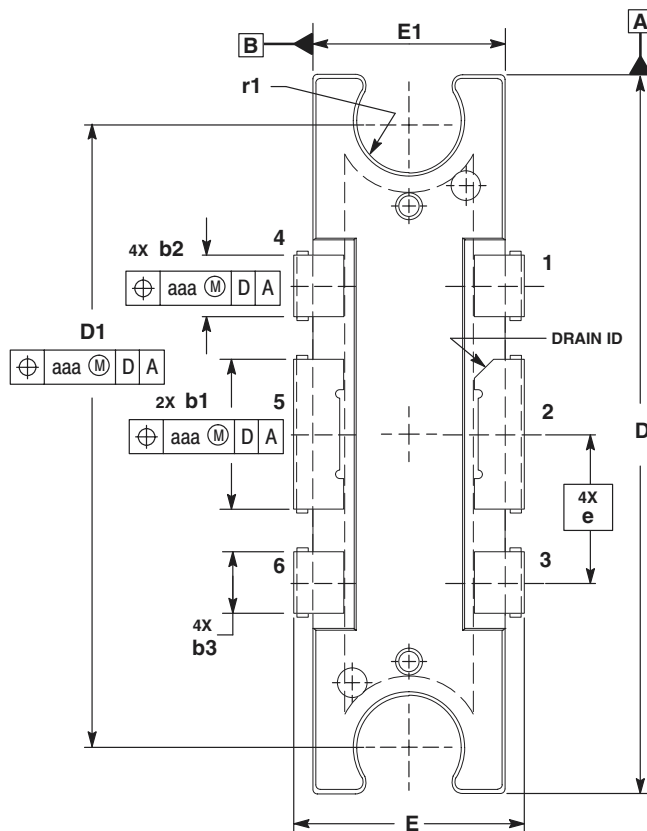
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

DIM	MILLIMETERS	
	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978-03
ISSUE B
PFP-16

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



STYLE 1:
PIN 1: SOURCE (COMMON)
2: DRAIN
3: SOURCE (COMMON)
4: SOURCE (COMMON)
5: GATE
6: SOURCE (COMMON)

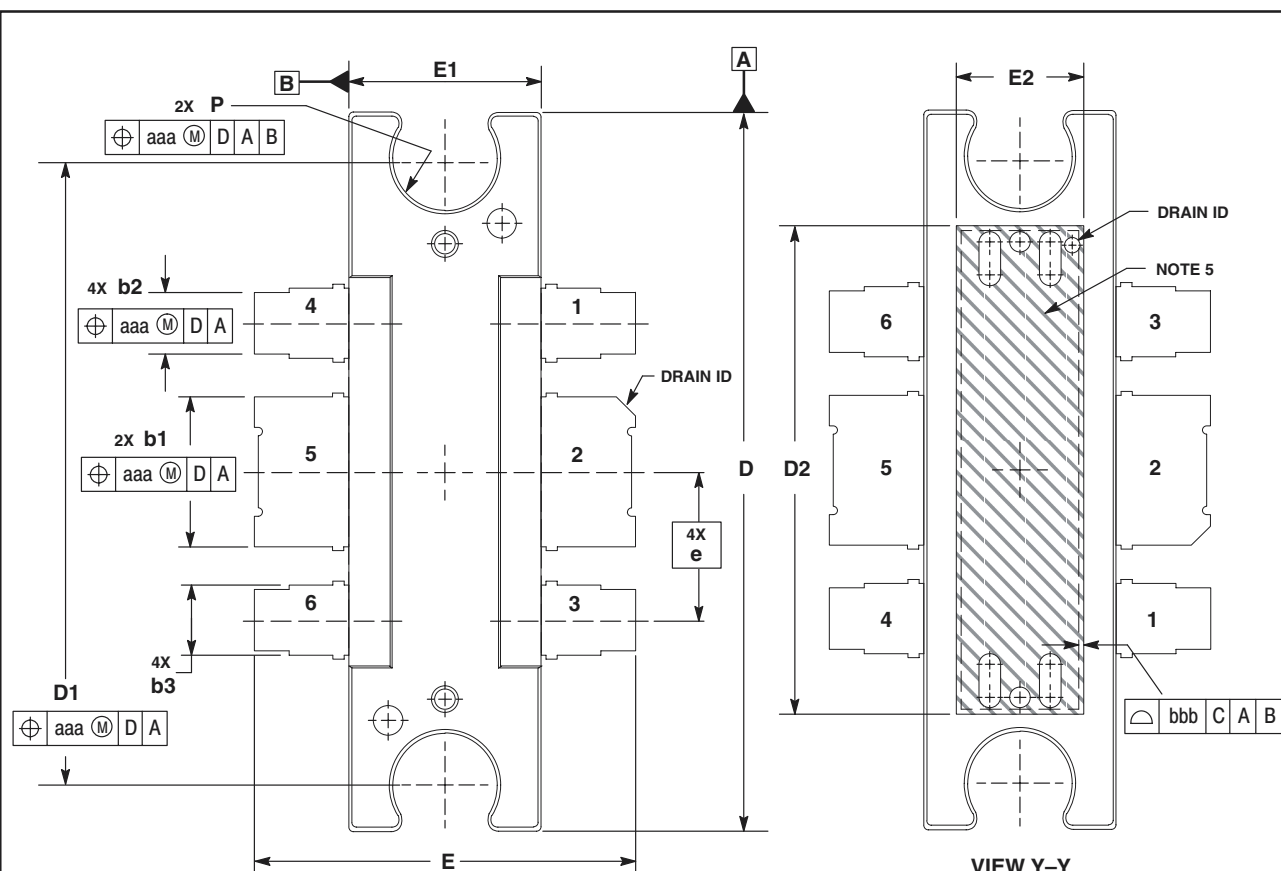
- NOTES:
1. CONTROLLING DIMENSION: INCH.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
 4. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSION D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
 5. DIMENSIONS b1 AND b3 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
 6. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.098	0.110	2.489	2.794
A1	0.000	0.004	0.000	0.102
A2	0.098	0.106	2.489	2.692
D	0.926	0.934	23.520	23.724
D1	0.806	0.814	20.472	20.676
E	0.296	0.304	7.518	7.722
E1	0.246	0.254	6.248	6.452
L	0.060	0.070	1.524	1.778
b1	0.193	0.199	4.902	5.055
b2	0.078	0.084	1.981	2.134
b3	0.088	0.094	2.235	2.388
c1	0.007	0.011	0.178	0.279
e	0.193 BSC		4.902 BSC	
r1	0.063	0.068	1.600	1.727
θ	0°	6°	0°	6°
aaa	0.004		0.102	

CASE 1264-08
ISSUE H
TO-272

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



- NOTES:
1. CONTROLLING DIMENSION: INCH.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
 4. DIMENSIONS b1 AND b3 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
 5. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
 6. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

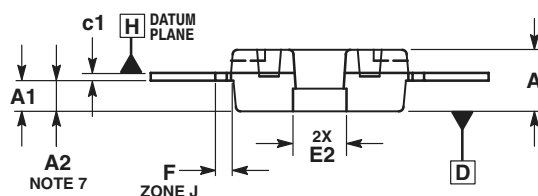
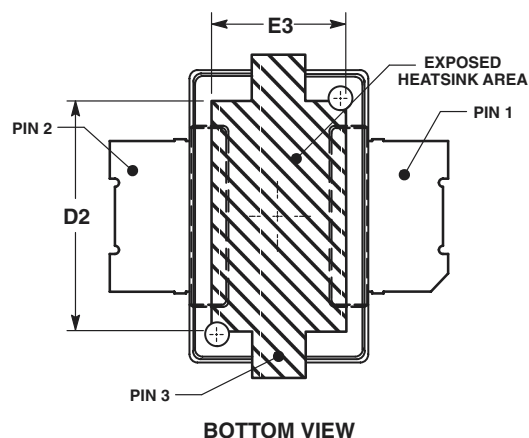
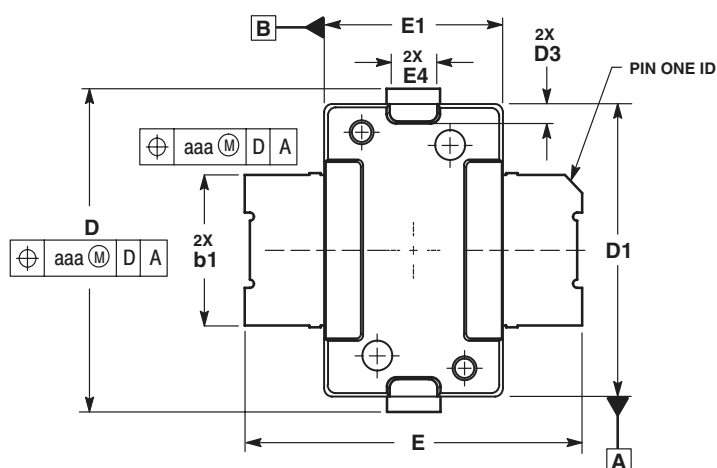
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.098	0.106	2.49	2.69
A1	0.038	0.044	0.96	1.12
A2	0.040	0.042	1.02	1.07
D	0.926	0.934	23.52	23.72
D1	0.810 BSC		20.57 BSC	
D2	0.608 BSC		15.44 BSC	
E	0.492	0.500	12.50	12.70
E1	0.246	0.254	6.25	6.45
E2	0.170 BSC		4.32 BSC	
F	0.025 BSC		0.64 BSC	
P	0.126	0.134	3.20	3.40
b1	0.193	0.199	4.90	5.05
b2	0.078	0.084	1.98	2.13
b3	0.088	0.094	2.24	2.39
c1	0.007	0.011	0.178	0.279
e	0.193 BSC		4.90 BSC	
aaa	0.004		0.10	
bbb	0.008		0.20	

- STYLE 1:
1. SOURCE (COMMON)
 2. DRAIN
 3. SOURCE (COMMON)
 4. SOURCE (COMMON)
 5. GATE
 6. SOURCE (COMMON)

CASE 1264A-02
ISSUE A
TO-272 STRAIGHT LEAD

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .003 PER SIDE. DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -D-.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.076	.084	1.93	2.13
A1	.038	.044	0.96	1.12
A2	.040	.042	1.02	1.07
D	.416	.424	10.57	10.77
D1	.376	.384	9.55	9.75
D2	.290	.320	7.37	8.13
D3	.016	.024	0.41	0.61
E	.436	.444	11.07	11.28
E1	.236	.244	5.99	6.20
E2	.066	.074	1.68	1.88
E3	.150	.180	3.81	4.57
E4	.058	.066	1.47	1.68
F	.025 BSC		0.64 BSC	
b1	.193	.199	4.90	5.06
c1	.007	.011	0.18	0.28
aaa	.004		0.10	

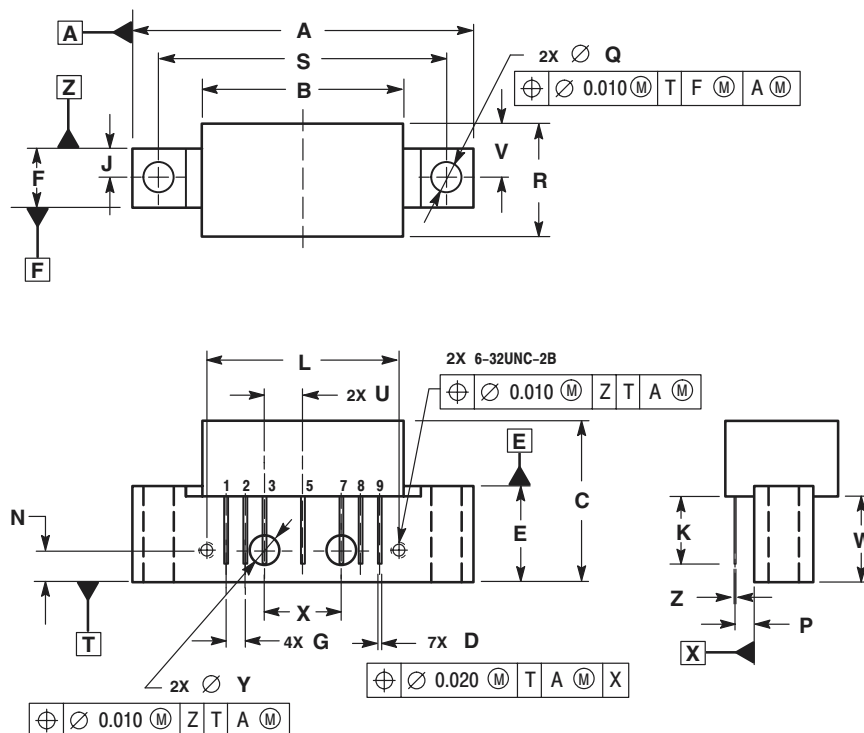
STYLE 1:

1. DRAIN
2. GATE
3. SOURCE

CASE 1265-07
ISSUE F
TO-270

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



- NOTES:
1. DIMENSIONS ARE IN INCHES.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

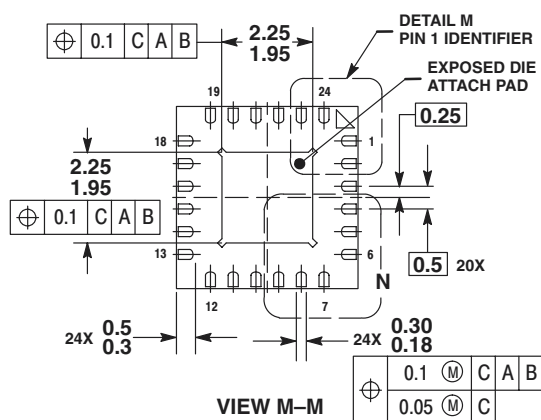
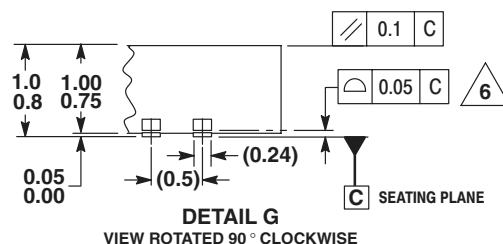
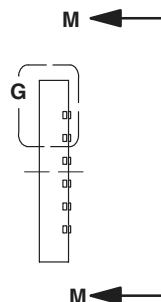
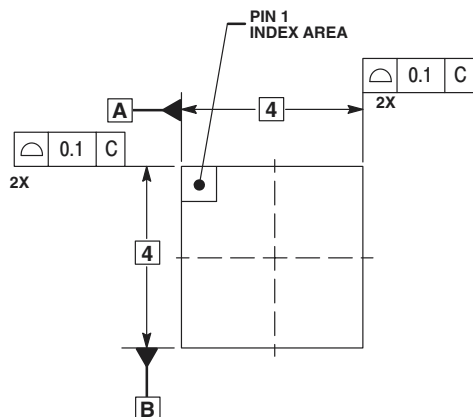
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	1.775	---	45.085
B	---	1.085	---	27.559
C	---	0.840	---	21.336
D	0.015	0.021	0.381	0.533
E	0.465	0.510	11.811	12.954
F	0.300	0.325	7.62	8.255
G	0.100 BSC		2.540 BSC	
J	0.156 BSC		3.962 BSC	
K	0.315	0.355	8.001	9.017
L	1.000 BSC		25.400 BSC	
N	0.165 BSC		4.191 BSC	
P	0.100 BSC		2.540 BSC	
Q	0.148	0.168	3.759	4.267
R	---	0.600	---	15.24
S	1.500 BSC		38.100 BSC	
U	0.200 BSC		5.080 BSC	
V	---	0.250	---	6.350
W	0.435	---	11.049	---
X	0.400 BSC		10.160 BSC	
Y	0.152	0.163	3.861	4.140
Z	0.009	0.011	0.229	0.279

- STYLE 1:
- PIN 1. RF INPUT
 - GROUND
 - GROUND
 - DELETED
 - VDC
 - DELETED
 - GROUND
 - GROUND
 - RF OUTPUT

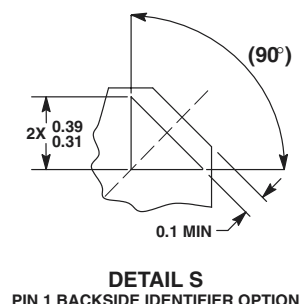
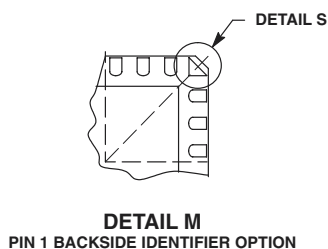
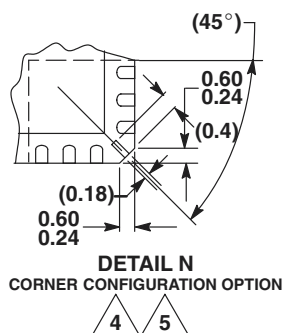
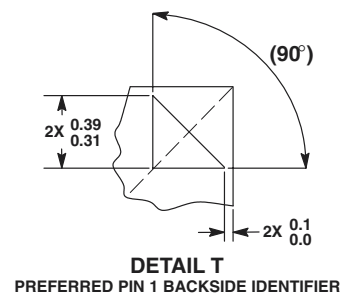
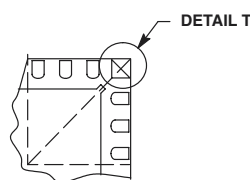
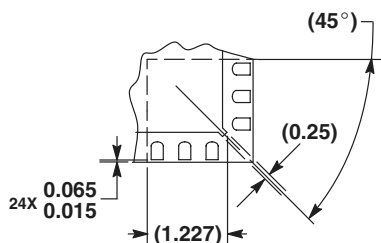
CASE 1302-01
ISSUE B

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



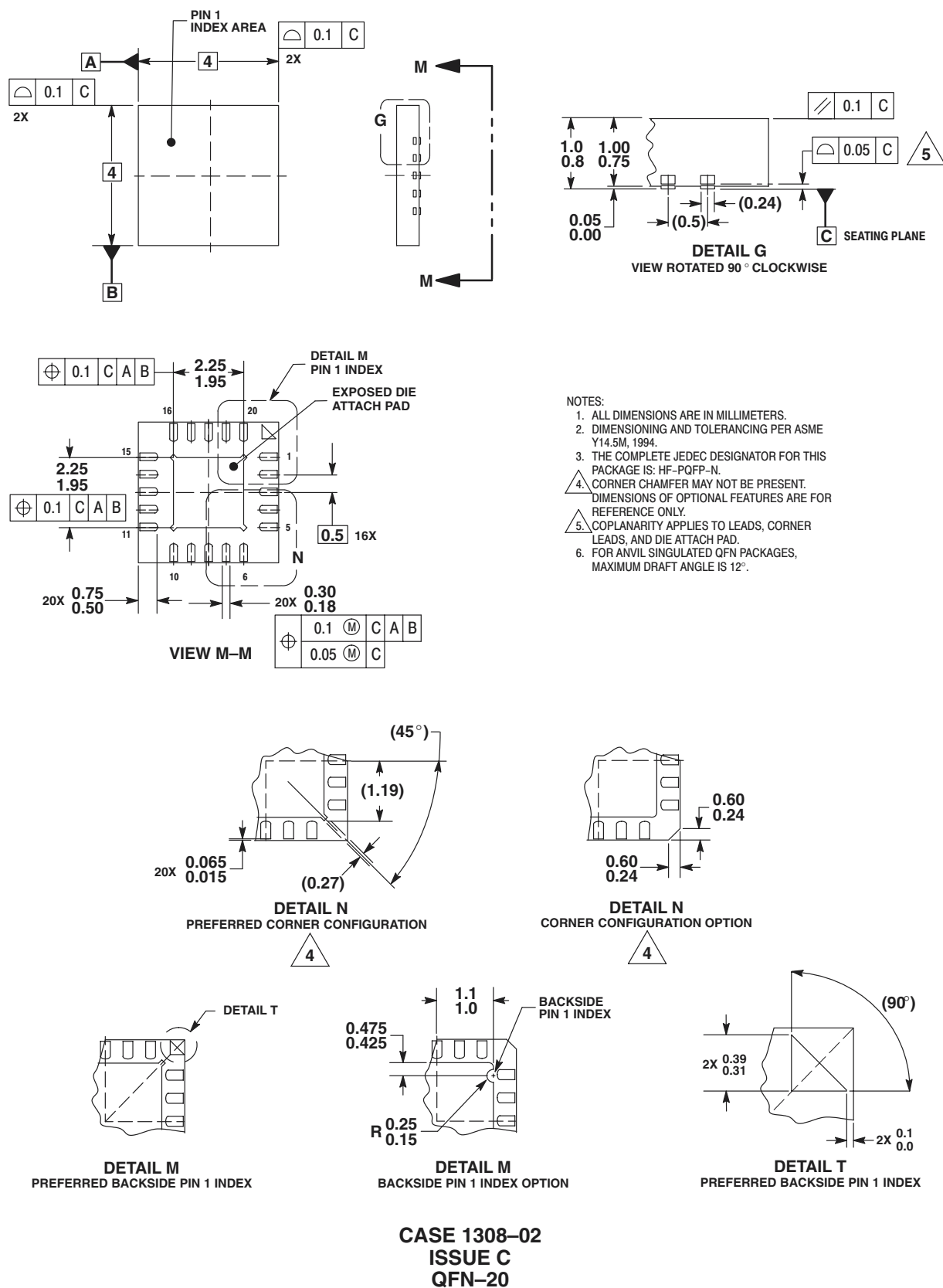
- NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
 4. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
 5. CORNER LEADS CAN BE USED FOR THERMAL OR GROUND AND ARE TIED TO THE DIE ATTACH PAD. THESE LEADS ARE NOT INCLUDED IN THE LEAD COUNT.
 6. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
 7. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12°.



CASE 1307-01
ISSUE B
QFN-24

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



PIN 1 INDEX AREA

VIEW M-M

DETAIL N
PREFERRED CORNER CONFIGURATION

DETAIL M
PREFERRED PIN 1 BACKSIDE INDEX

DETAIL M
BACKSIDE PIN 1 INDEX OPTION

DETAIL T
PREFERRED PIN 1 BACKSIDE INDEX

DETAIL G
VIEW ROTATED 90° CLOCKWISE

DETAIL N
CORNER CONFIGURATION OPTION

DETAIL T
PREFERRED PIN 1 BACKSIDE INDEX

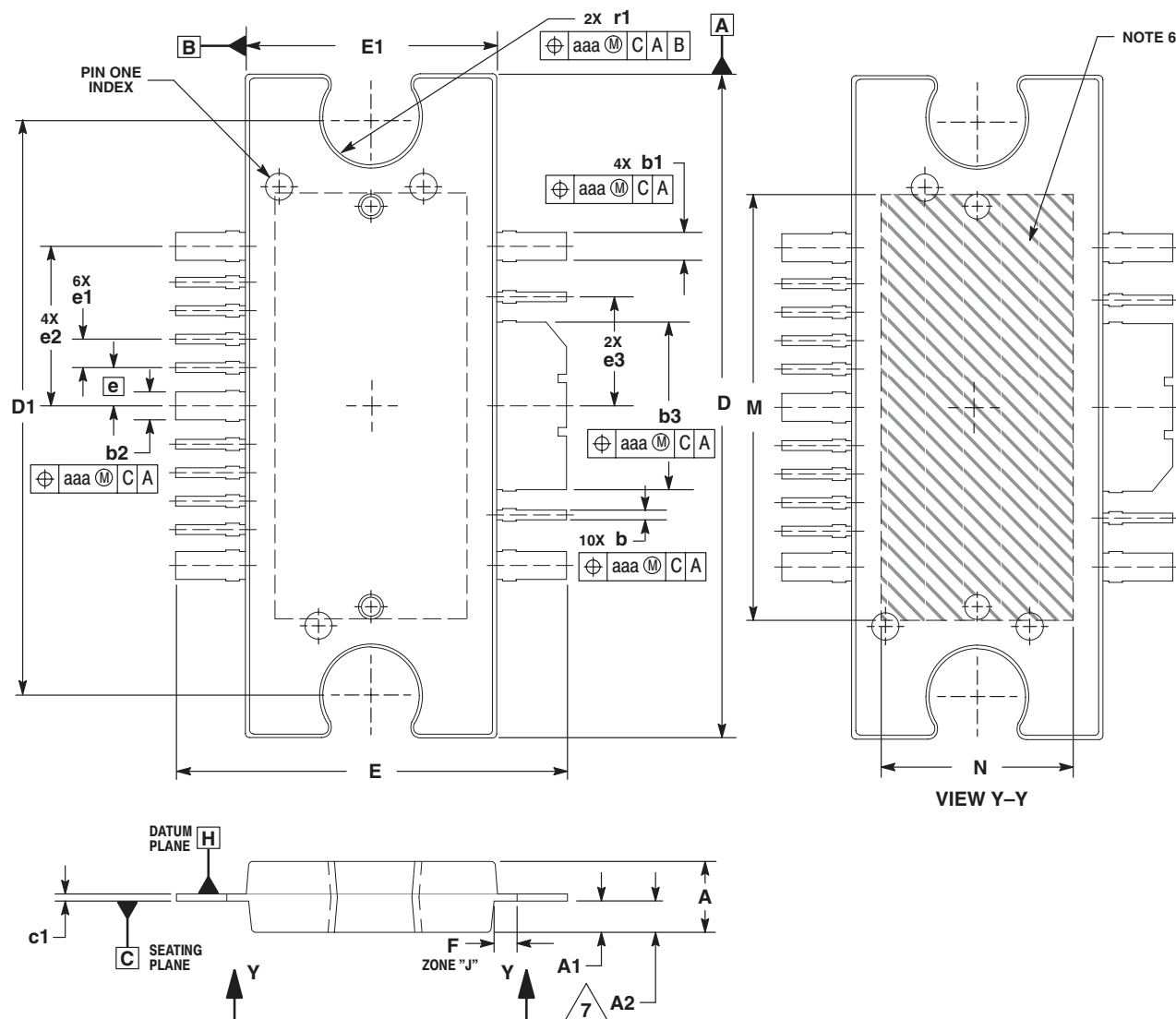
NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
- CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
- COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
- FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12°.

CASE 1311-02
ISSUE D
QFN-32, 5x5 mm

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



NOTES:

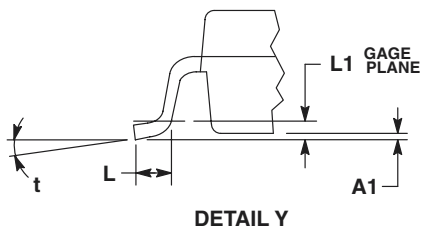
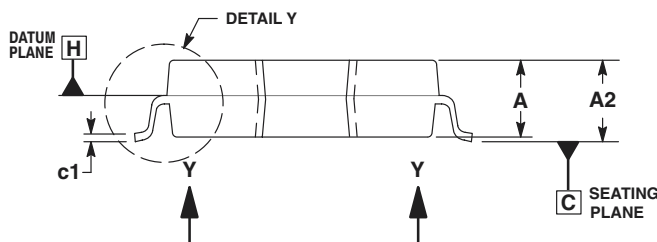
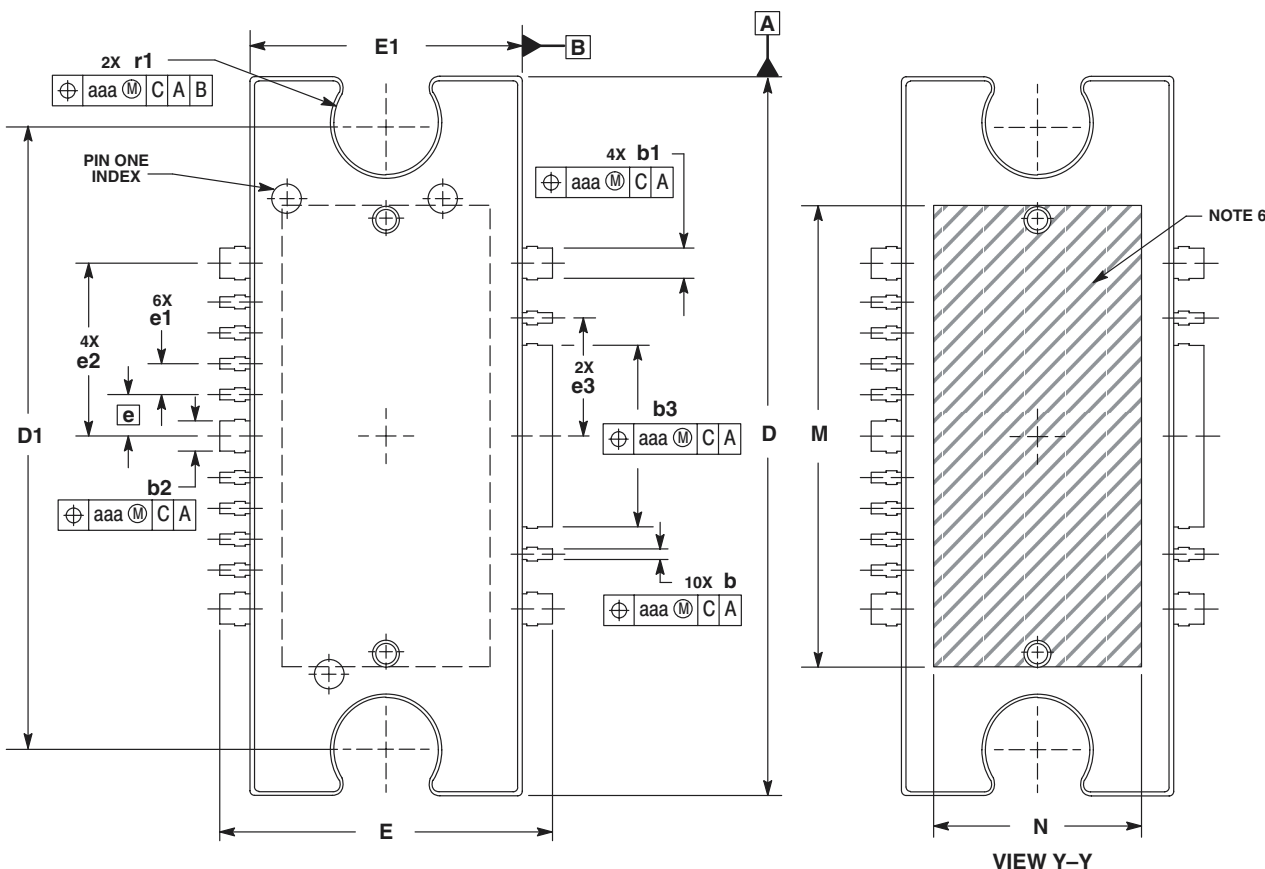
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.098	.106	2.49	2.69
A1	.038	.044	0.96	1.12
D	.926	.934	23.52	23.72
D1	.810	BSC	20.57	BSC
E	.551	.559	14.00	14.20
E1	.351	.359	8.92	9.12
F	.025	BSC	0.64	BSC
M	.600	---	15.24	---
N	.270	---	6.86	---
b	.011	.017	0.28	0.43
b1	.037	.043	0.94	1.09
b2	.037	.043	0.94	1.09
b3	.225	.231	5.72	5.87
c1	.007	.011	.18	.28
e	.054	BSC	1.37	BSC
e1	.040	BSC	1.02	BSC
e2	.224	BSC	5.69	BSC
e3	.150	BSC	3.81	BSC
r1	.063	.068	1.6	1.73
aaa	.004	---	.10	---

CASE 1329-08
ISSUE H
TO-272 Wide Body Multi Lead

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



NOTES:

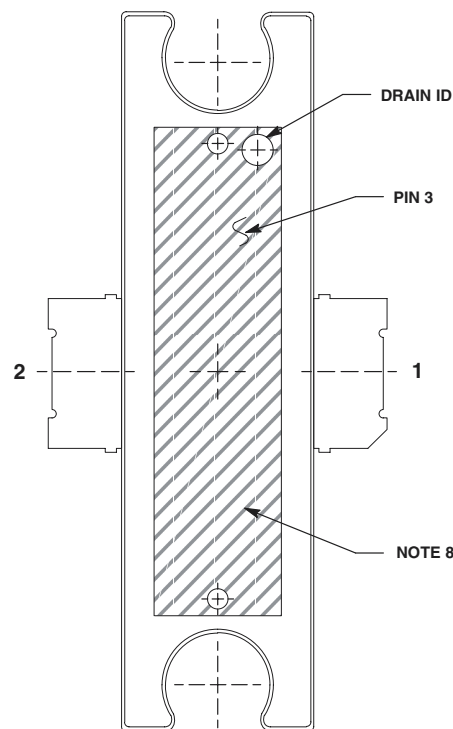
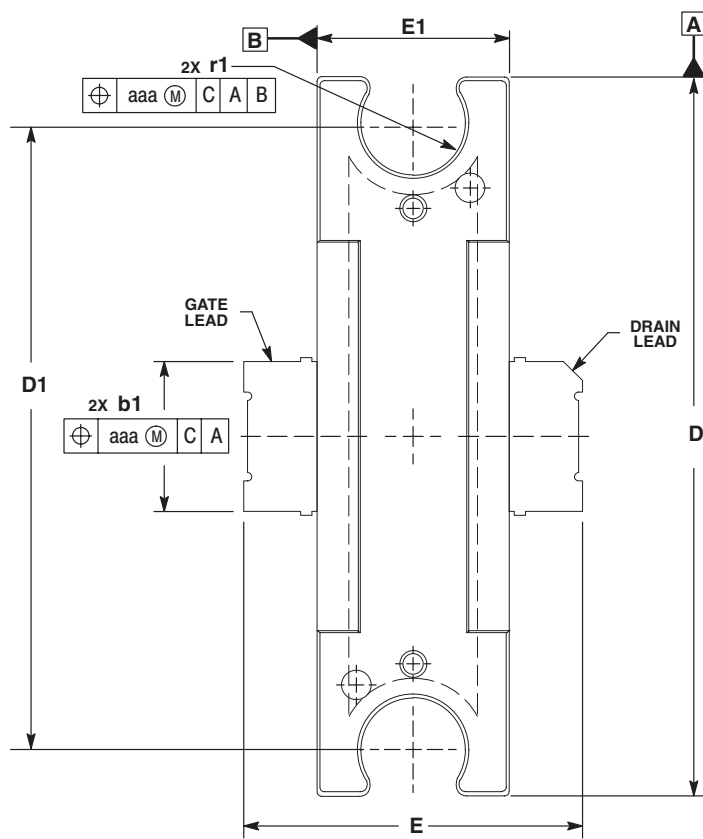
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SINK.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.098	.106	2.49	2.69
A1	.001	.004	0.02	0.10
A2	.099	.110	2.51	2.79
D	.926	.934	23.52	23.72
D1	.810 BSC		20.57 BSC	
E	.429	.437	10.90	11.10
E1	.351	.359	8.92	9.12
L	.018	.024	4.90	5.06
L1	.01 BSC		0.25 BSC	
M	.600	---	15.24	---
N	.270	---	6.86	---
b	.011	.017	0.28	0.43
b1	.037	.043	0.94	1.09
b2	.037	.043	0.94	1.09
b3	.225	.231	5.72	5.87
c1	.007	.011	.18	.28
e	.054 BSC		1.37 BSC	
e1	.040 BSC		1.02 BSC	
e2	.224 BSC		5.69 BSC	
e3	.150 BSC		3.81 BSC	
r1	.063	.068	1.6	1.73
t	2°		8°	
aaa	.004		.10	

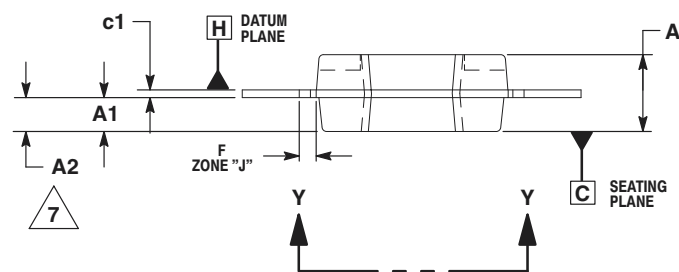
CASE 1329A-02 ISSUE A TO-272 Wide Body Multi Lead Gull Wing

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



VIEW Y-Y



NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.098	.106	2.49	2.69
A1	.038	.044	0.96	1.12
A2	.040	.042	1.02	1.07
D	.926	.934	23.52	23.72
D1	.810 BSC		20.57 BSC	
E	.438	.442	11.12	11.23
E1	.246	.254	6.25	6.45
F	.025 BSC		0.64 BSC	
b1	.193	.199	4.90	5.05
c1	.007	.011	.18	.28
r1	.063	.068	1.60	1.73
aaa	.004		.10	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 1337-02
ISSUE A
TO-272 Dual Lead

Top View: Shows a square package with a central die area. Dimensions include 3x3 mm for the central area, 2X 0.1 mm for the central area, and 2X 0.1 mm for the central area. A laser mark for pin 1 identification is indicated in the top-left corner.

Bottom View: Shows the package from the underside. Dimensions include 12x 0.3 mm for the central area, 12x 0.18 mm for the central area, 12x 0.75 mm for the central area, 8x 0.5 mm for the central area, and 12x 0.065 mm for the central area. A detail M pin 1 identifier is shown.

Detail G: View rotated 90° clockwise. Shows the package from the underside. Dimensions include 1.0 mm, 0.8 mm, 1.00 mm, 0.75 mm, 0.05 mm, 0.00 mm, 0.24 mm, 0.5 mm, 0.1 mm, 0.05 mm, and 0.00 mm. A seating plane is indicated.

Detail M: Pin 1 backside identifier. Shows the package from the underside. Dimensions include 1.25 mm, 0.95 mm, 1.25 mm, 0.95 mm, 12x 0.3 mm, 12x 0.18 mm, 12x 0.75 mm, 8x 0.5 mm, 12x 0.065 mm, 0.015 mm, 3x (R0.09), 4x (0.18), 4x (45°), 4x (0.25), 8x (0.777), 2x 0.39 mm, 0.31 mm, 2x 0.1 mm, and 0.0 mm.

Detail N: Corner configuration. Shows the package from the underside. Dimensions include 12x 0.065 mm, 0.015 mm, 3x (R0.09), 4x (0.18), 4x (45°), 4x (0.25), 8x (0.777), 2x 0.39 mm, 0.31 mm, 2x 0.1 mm, and 0.0 mm.

Detail S: Pin 1 backside identifier. Shows the package from the underside. Dimensions include 12x 0.3 mm, 12x 0.18 mm, 12x 0.75 mm, 8x 0.5 mm, 12x 0.065 mm, 0.015 mm, 3x (R0.09), 4x (0.18), 4x (45°), 4x (0.25), 8x (0.777), 2x 0.39 mm, 0.31 mm, 2x 0.1 mm, and 0.0 mm.

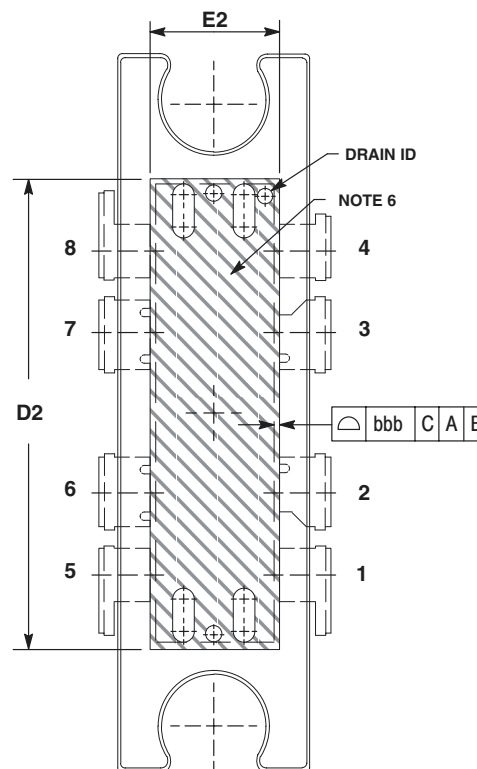
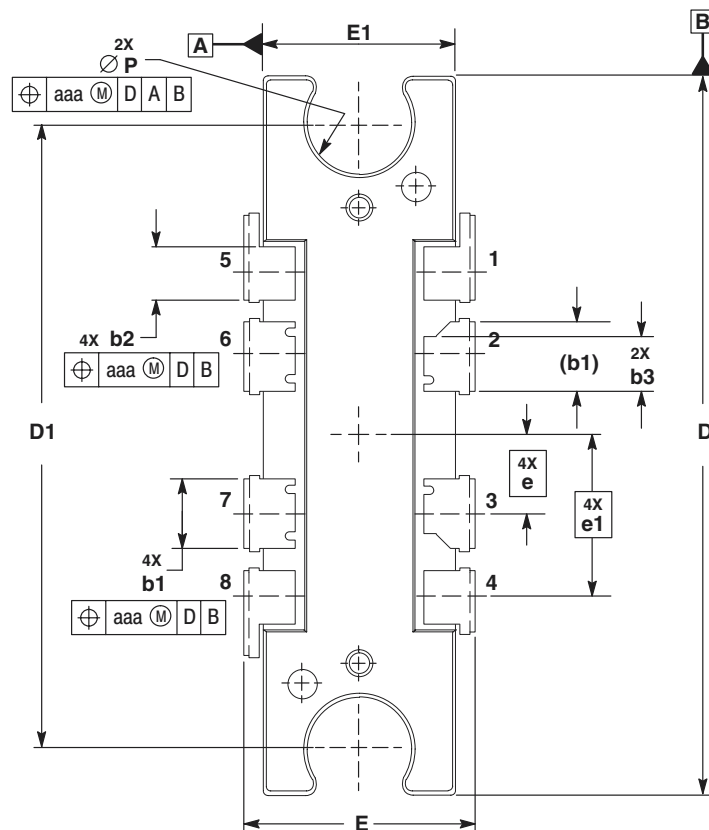
Notes:

- DIMENSIONS ARE IN MILLIMETERS.
- INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
- CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
- COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.

**CASE 1345-01
ISSUE A
QFN-12**

Freescale Semiconductor, Inc.

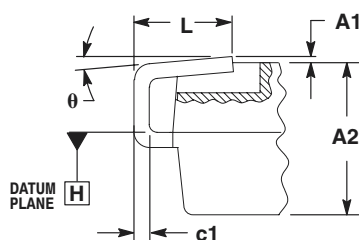
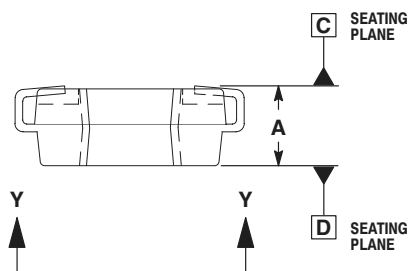
CASE DIMENSIONS (continued)



VIEW Y-Y

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSION D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS b1 AND b2 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.



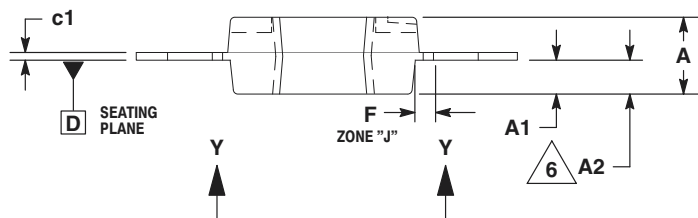
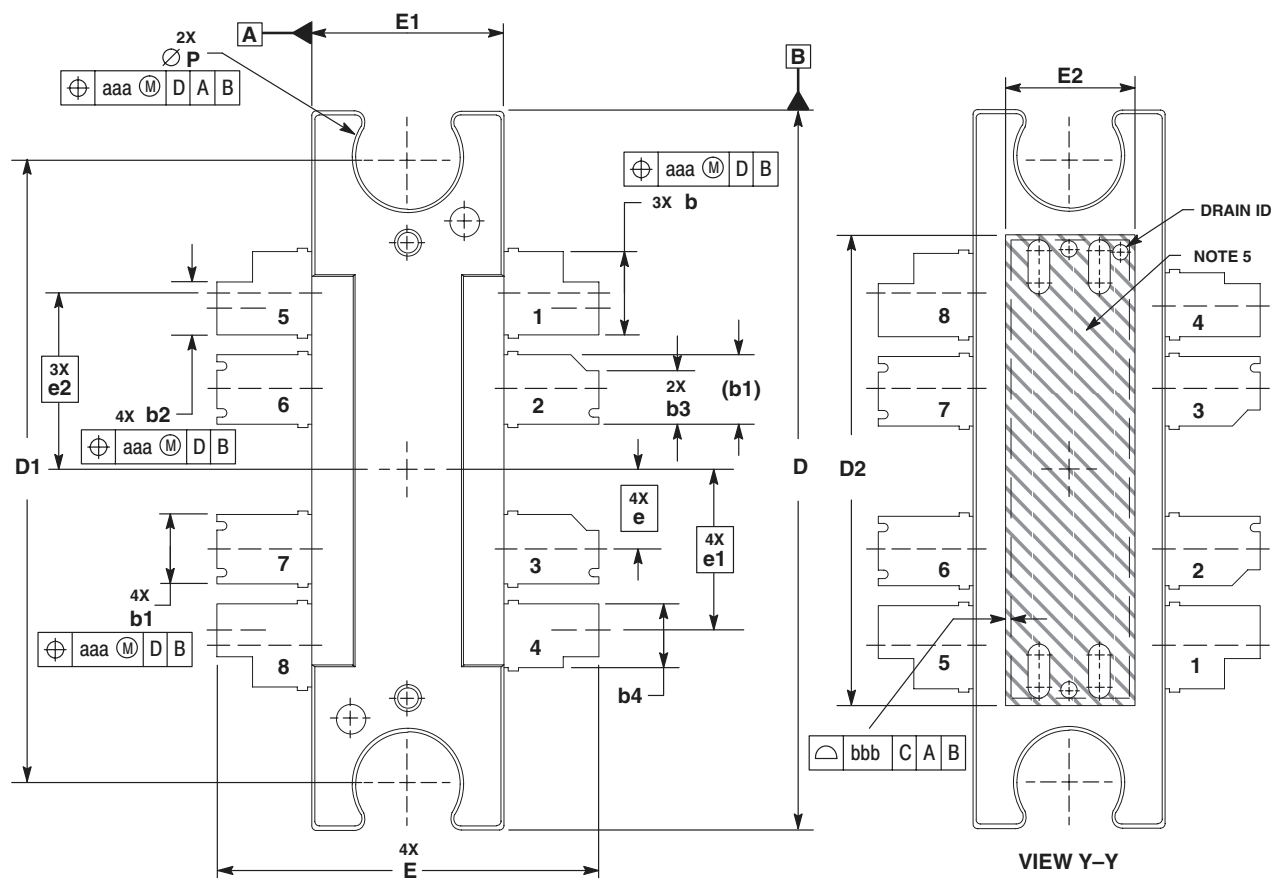
- STYLE 1:
- PIN 1. SOURCE (COMMON)
 - DRAIN
 - DRAIN
 - SOURCE (COMMON)
 - SOURCE (COMMON)
 - GATE
 - GATE
 - SOURCE (COMMON)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.098	0.110	2.49	2.79
A1	0.000	0.004	0.00	0.10
A2	0.098	0.106	2.49	2.69
D	0.926	0.934	23.52	23.72
D1	0.810 BSC		20.57 BSC	
D2	0.608 BSC		15.44 BSC	
E	0.296	0.304	7.52	7.72
E1	0.246	0.254	6.25	6.45
E2	0.170 BSC		4.32 BSC	
L	0.060	0.070	1.52	1.78
P	0.126	0.134	3.20	3.40
b1	0.088	0.094	2.24	2.39
b2	0.066	0.072	1.68	1.83
b3	0.067	0.073	1.70	1.85
c1	0.007	0.011	0.178	0.279
e	0.104 BSC		2.64 BSC	
e1	0.210 BSC		5.33 BSC	
theta	0°	6°	0°	6°
aaa	0.004		0.10	
bbb	0.008		0.20	

CASE 1366-03
ISSUE B
TO-272 Split Lead

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
4. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE "b1" AND "b2" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
5. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
6. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

STYLE 1:

- PIN 1. SOURCE (COMMON)
- DRAIN
- DRAIN
- SOURCE (COMMON)
- SOURCE (COMMON)
- GATE
- GATE
- SOURCE (COMMON)

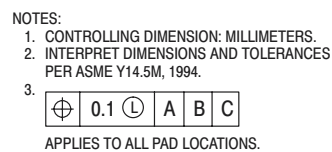
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.098	0.106	2.49	2.69
A1	0.038	0.044	0.96	1.12
A2	0.040	0.042	1.02	1.07
D	0.926	0.934	23.52	23.72
D1	0.810 BSC		20.57 BSC	
D2	0.608 BSC		15.44 BSC	
E	0.492	0.500	12.50	12.70
E1	0.246	0.254	6.25	6.45
E2	0.170 BSC		4.32 BSC	
F	0.025 BSC		0.64 BSC	
P	0.126	0.134	3.20	3.40
b	0.105	0.111	2.67	2.82
b1	0.088	0.094	2.24	2.39
b2	0.066	0.072	1.68	1.83
b3	0.067	0.073	1.70	1.85
b4	0.077	0.083	1.96	2.11
c1	0.007	0.011	0.178	0.279
e	0.104 BSC		2.64 BSC	
e1	0.210 BSC		5.33 BSC	
e2	0.229 BSC		5.82 BSC	
aaa	0.004		0.10	
bbb	0.008		0.20	

CASE 1366A-02

ISSUE A

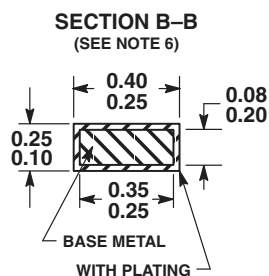
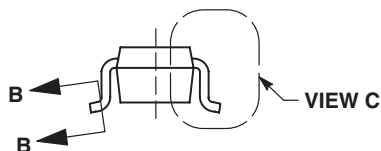
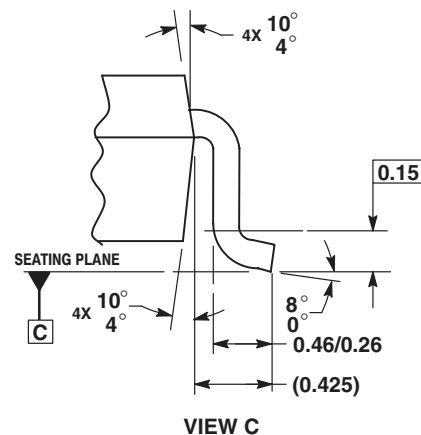
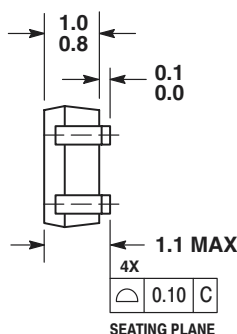
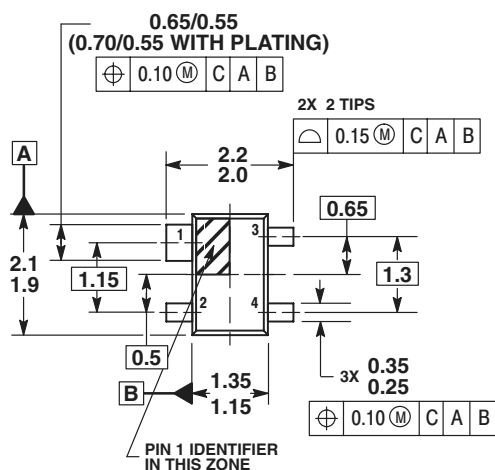
TO-272 Split Lead – Straight Lead Version

Technical drawing of a square plate. The top view shows a square with a side length of 7. The bottom view shows a rectangular plate with a width of 1.01 ± 0.1 and a thickness of 0.7 ± 0.05 . The drawing includes datum A (bottom center) and datum B (top center). A feature control frame on the right side of the top view indicates a circular feature with a tolerance of 0.1.

MOTOROLA WIRELESS
RF PRODUCT DEVICE DATA

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)

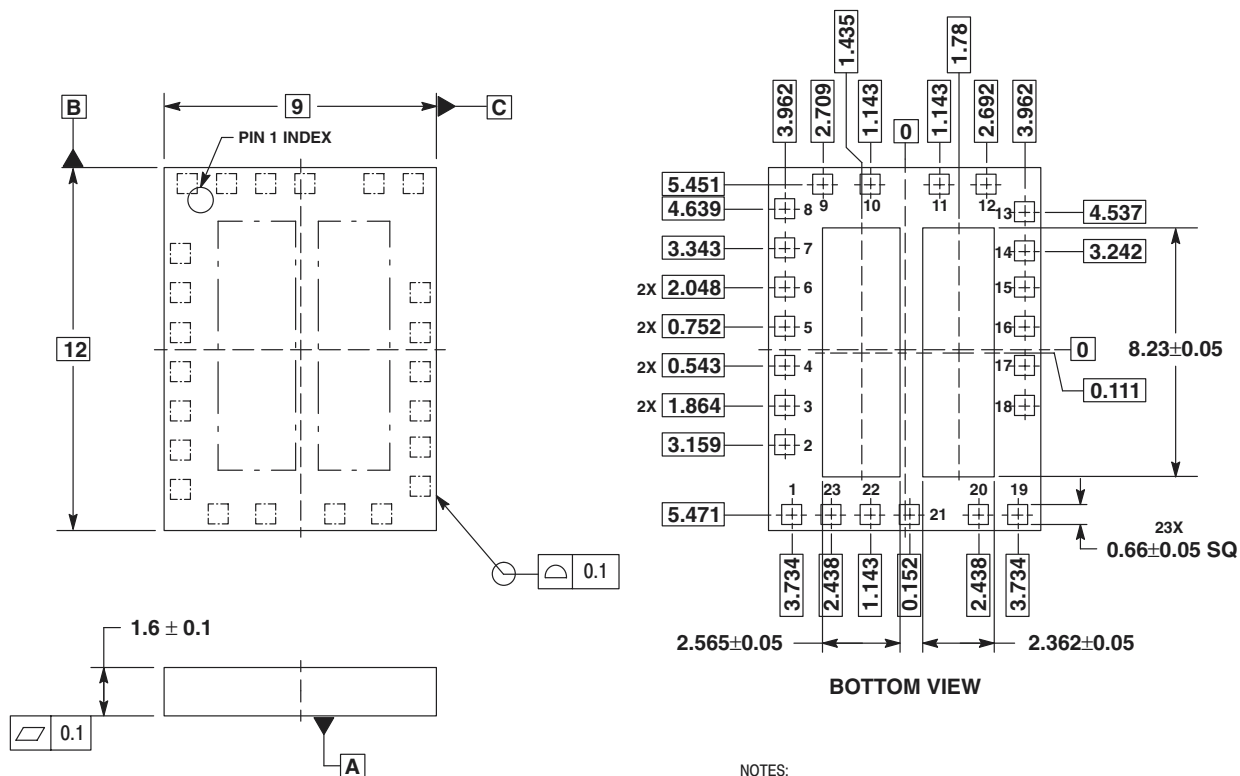


- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSION AT DATUM A AND B DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 4. DIMENSION AT DATUM A AND B ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF PLASTIC BODY.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08mm AND 0.15mm FROM THE LEAD TIP.

CASE 1404-01
ISSUE O
Plastic
SOT-343R

Freescale Semiconductor, Inc.

CASE DIMENSIONS (continued)



NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. $\oplus 0.1 \text{ } \ominus A B C$
APPLIES TO ALL PAD LOCATIONS.

CASE 1440-01
ISSUE O
9x12 mm Module

Chapter Ten

Applications and Product Literature

Motorola's Applications Literature provides guidance to the effective use of its semiconductor families across a broad range of practical applications. Many different topics are discussed in a way that is not possible in a device data sheet, from detailed circuit designs complete with PCB layouts, through matters to consider when embarking on a design, to complete overviews of product families and their design philosophies.

Information is presented in the form of Application Notes, Article Reprints and Engineering Bulletins.

Table of Contents

	Page
Applications Literature	10-2
Product Literature	10-3

Applications and Product Literature

Application Notes, Engineering Bulletins and Article Reprints of special interest to designers of RF and RF/IF equipment are listed below. This technical documentation is available on the Motorola Semiconductor Product Sector Web site or is available through the Motorola Literature Distribution Center. Phone and fax numbers for ordering literature are listed on the back cover of this book and in our Accessing Data On-line section.

Application Notes

AN211A	Field Effect Transistors in Theory and Practice	AN1674	Mounting Method with Mechanical Fasteners for the MRF286 and Similar Packages
AN419	UHF Amplifier Design Using Data Sheet Design Curves	AN1696	Broadband Intermodulation Performance Development Using the Rohde & Schwarz Vector Network Analyzer ZVR
AN423	Field Effect Transistor RF Amplifier Design Techniques	AN1697	GSM900/DCS/1800 Dual-Band 3.6 V Power Amplifier Solution with Open Loop Control Scheme
AN535	Phase-Locked-Loop Design Fundamentals	AN1907	Surface Mount Solder Attach Method for the MRF9045MR1 in the TO-270 Plastic RF Package
AN548A	Microstrip Design Techniques for UHF Amplifiers	AN1908	Solder Mounting Method for the MRF19090S and Similar Packages
AN721	Impedance Matching Networks Applied to RF Power Transistors	AN1923	Mounting Method with Mechanical Fasteners for the MRF19090 and Similar Packages
AN923	800 MHz Test Fixture Design	AN1938	Sensitivity of High Power RF Transistors to Source and Output Loads
AN955	A Cost Effective VHF Amplifier for Land Mobile Radios	AN1941	Modeling Thermal Effects in RF LDMOS Transistors
AN1022	Mechanical and Thermal Considerations in Using RF Linear Hybrid Amplifiers	AN1944	Generating Temperature-Dependent IV Curves Using ADS
AN1024	RF Linear Hybrid Amplifiers	AN1946	Interfacing Motorola's MC13190 2.4 GHz Transceiver IC with HC08 Family MCU's
AN1025	Reliability Considerations in Design and Use of RF Integrated Circuits	AN1949	Mounting Method for the MHVIC910HR2 (PFP-16) and Similar Surface Mount Packages
AN1026	Extending the Range of an Intermodulation Distortion Test	AN1955	Thermal Measurement Methodology of RF Power Amplifiers
AN1027	Reliability/Performance Aspects of CATV Amplifier Design	AN4005	Thermal Management and Mounting Method for the PLD 1.5 RF Power Surface Mount Package
AN1032	How Load VSWR Affects Non-Linear Circuits		
AN1033	Match Impedances in Microwave Amplifiers		
AN1034	Three Balun Designs for Push-Pull Amplifiers		
AN1040	Mounting Considerations for Power Semiconductors		
AN1207	The MC145170 in Basic HF and VHF Oscillators		
AN1253	An Improved PLL Design Method Without ω_n and ζ		
AN1277	Offset Reference PLLs for Fine Resolution or Fast Hopping		
AN1526	RF Power Device Impedances: Practical Considerations		
AN1530	Motorola Advanced Amplifier Concept Package		
AN1539	An IF Communication Circuit Tutorial		
AN1602	3.6 V and 4.8 V GSM/DCS1800 Dual Band PA Application with DECT Capability Using Standard Motorola RFIC's		
AN1617	Mounting Recommendations for Copper Tungsten Flanged Transistors		
AN1639	Phase Noise Measurement Using the Phase Lock Technique		
AN1643	RF LDMOS Power Modules for GSM Base Station Application: Optimum Biasing Circuit		
AN1670	60 Watts, GSM 900 MHz, LDMOS Two-Stage Amplifier		
AN1671	MC145170 PSpice Modeling Kit		
AN1673	Solder Reflow Mounting Method for the MRF286 and Similar Packages		

Article Reprints

AR164	Good RF Construction Practices and Techniques
AR254	Phase-Locked Loop Design Articles
AR510	VSWR Protection of Solid State RF Power Amplifiers
AR511	Biasing Solid State Amplifiers to Linear Operation
AR579	CAD of a Broadband, Class-C 65 Watt UHF Power Amplifier
AR581	Procedure Performs Thermal Measurements on Pulsed Devices
AR612	Plastic Packages Hold Power RF MOSFETs
AR624	Aluminum-Based Metallization Enhances Device Reliability
AR628	Impedance Measurements for High Power RF Transistors Using the TRL Method
AR629	Digital Predistortion Techniques for RF Power Amplifiers with CDMA Applications

Freescale Semiconductor, Inc.

Engineering Bulletins

EB38	Measuring the Intermodulation Distortion of Linear Amplifiers
EB105	A 30 Watt, 800 MHz Amplifier Design
EB209	Mounting Method for RF Power Leadless Surface Mount Transistors
EB211	Thermal Management and Solder Mounting Method for the MRF286, 60 Watt Power Device in a CuW (Copper Tungsten) Base Package

Product Literature

DL110/D	Wireless RF Product Device Data Library
DL209/D	CATV Distribution Amplifier Module Device Data Book
SG46/D	Wireless RF Product Selector Guide

Freescale Semiconductor, Inc.

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

JAPAN:

Motorola Japan Ltd.; SPS, Technical Information Center
3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573, Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre, 2 Dai King Street
Tai Po Industrial Estate, Tai Po, N.T. Hong Kong
852-26668334

HOME PAGE:

<http://www.motorola.com/semiconductors>

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

**MOTOROLA**

MOTOROLA and the Stylized M Logo are registered in the U.S. Patent and Trademark Office. All other product or service names are the property of their respective owners.
© Motorola, Inc. 2003

DL110/D
Rev. 14
2/2003

**For More Information On This Product,
Go to: www.freescale.com**