CTI

CT2525/26/27
MIL-STD-1553
SINGLE PACKAGE SOLUTION

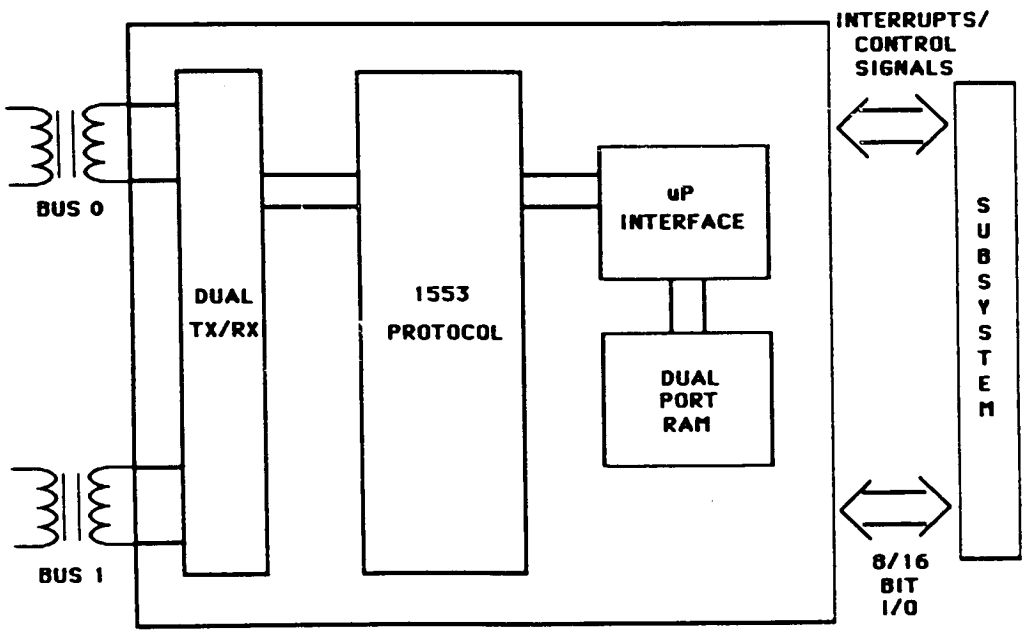
ADVANCE INFORMATION

GENERAL DESCRIPTION

The CT2525 provides a complete one package interface between the MIL-STD-1553 bus and all microprocessor systems. The hybrid provides all data buffers and control registers to function as a Bus Controller or Remote Terminal. Control of the hybrid by the subsystem is through simple I/O port commands. Internal hybrid logic removes all critical timing imposed on a typical subsystem, thereby simplifying the implementation of this interface.

FEATURES

- Incorporates transceivers, Protocol and sub-system Interface components into a single Hybrid Package
- Functions as a Remote Terminal or Bus Controller
- Interfaces to uP as a simple peripheral unit
- Available with several options for transceivers: ± 15V, ± 12V and + 5V only
- Provides Fully Buffed Dual Port RAM storage for transmit and receive sub-addresses



CT2525

CT2525/26/27

SINGLE HYBRID PROTOCOL/SUBSYSTEM INTERFACE

Key Features

*Functional Superset of CT1800

*Downward compatible with existing base of CT1800 designs.

*Incorporates Transceivers, Protocol and Interface Hybrids into a single package.

*Functions as a Remote Terminal or Bus Controller.

General

The CT2525 provides a complete interface between the MIL-STD-1553 bus and any microprocessor system. Functioning as a superset of the CT1800 interface, the hybrid separates the bus from the subsystem. The hybrid provides all data buffers and control registers necessary to implement RT and BC functions. Internal arbitration and data transfer control circuitry eliminates subsystem response requirements. All data written into or read from this interface are double buffered on a message basis. Only valid and complete receive messages are transferred into the receive RAM.

The CT2525 supports all 15 mode codes and all types of data transfers allowed by MIL-STD-1553B. All circuitry (excluding transceiver drivers) are CMOS which results in very low power requirements.

Interfacing to the subsystem is simplified through the use of tri-stated input/output buffers onto the subsystem bus. Control signals basically consist of four address lines, a device select input, read strobe, write strobe and several interrupts, the use of which are optional. Hybrid is accessed as a memory mapped I/O port of a microprocessor. Valid transmission and reception of data are indicated to the subsystem through the use of interrupts. This frees up the system processor from actively monitoring the port unitl a valid message is received.