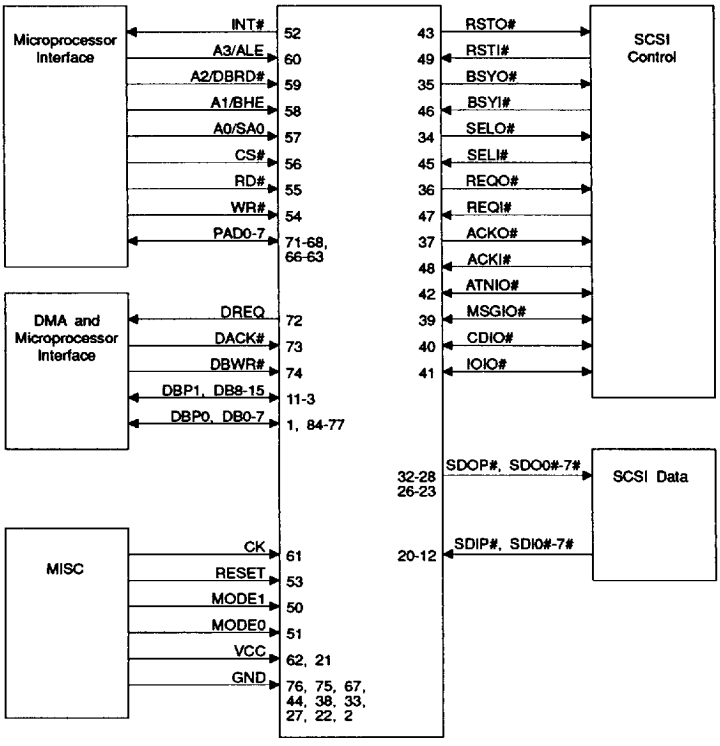
Features

- One-Chip SCSI-2 Fast Architecture Controller for Host and 8-bit or 16-bit Peripheral Applications
- 84-Pin PLCC Package, Sub-Micron CMOS Technology
- Supports ANSI X3T9.2 SCSI Standard, with SCSI-2 Fast Architecture
- Functions as an Initiator or a Target
- Implements SCSI Bus Sequences without Host Processor Intervention
- Asynchronous Data Transfers up to 7 Mbytes/sec
- Synchronous Data Transfers up to 10 Mbytes/sec
- DMA Burst Transfers up to 20 Mbytes/sec
- Programmable Synchronous Transfer Period and Offset
- 24-Bit Transfer Counter
- Pipeline Command Structure
- 16-Byte, Parity Pass-through Data FIFO Between the DMA and SCSI Channels
- On-Chip 48-mA Single-Ended SCSI Transceivers

Single Chip SCSI Controller

System Block Diagram



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Description

The AT43216 is a high performance single-chip SCSI-2 compatible controller that typically replaces SCSI interface circuitry consisting of discrete devices, external drivers, and a low performance SCSI interface chip.

The chip incorporates both initiator and target modes and can be used in host and peripheral applications. Bus arbitration, target selection, and initiator reselection are all handled on chip.

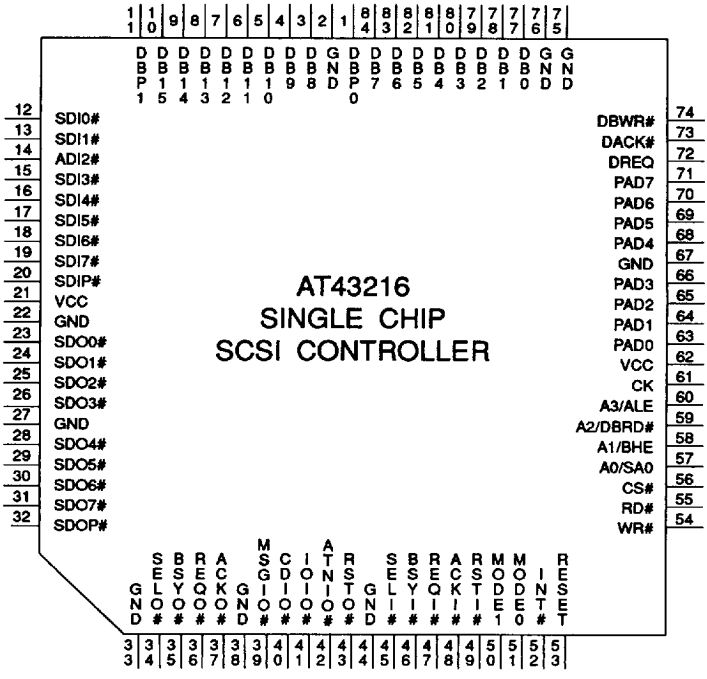
Overhead interaction with the host processor is minimized by use of an interrupt-driven architecture in conjunction with a command pipeline and a powerful instruction set that reduces common SCSI bus sequences to single commands. The chip controls message, command, status, and data transfers between the SCSI bus and the internal 16-byte FIFO.

In order to maximize throughput, the AT43216 architecture incorporates three independent buses: the 8-bit SCSI bus, the 8-bit or 16-bit with parity pass-through data bus (DB), and the 8-bit processor bus (PAD). The SCSI bus supports synchronous transfers of 5 Mbytes per second and 10 Mbytes per second in addition to asynchronous transfers up to 7 Mbytes per second. The data bus includes a high-speed DMA interface for burst transfer rates up to 20 Mbytes per second. The processor bus can be configured for multiplexed or non-multiplexed operation to simplify interfacing to the host processor.

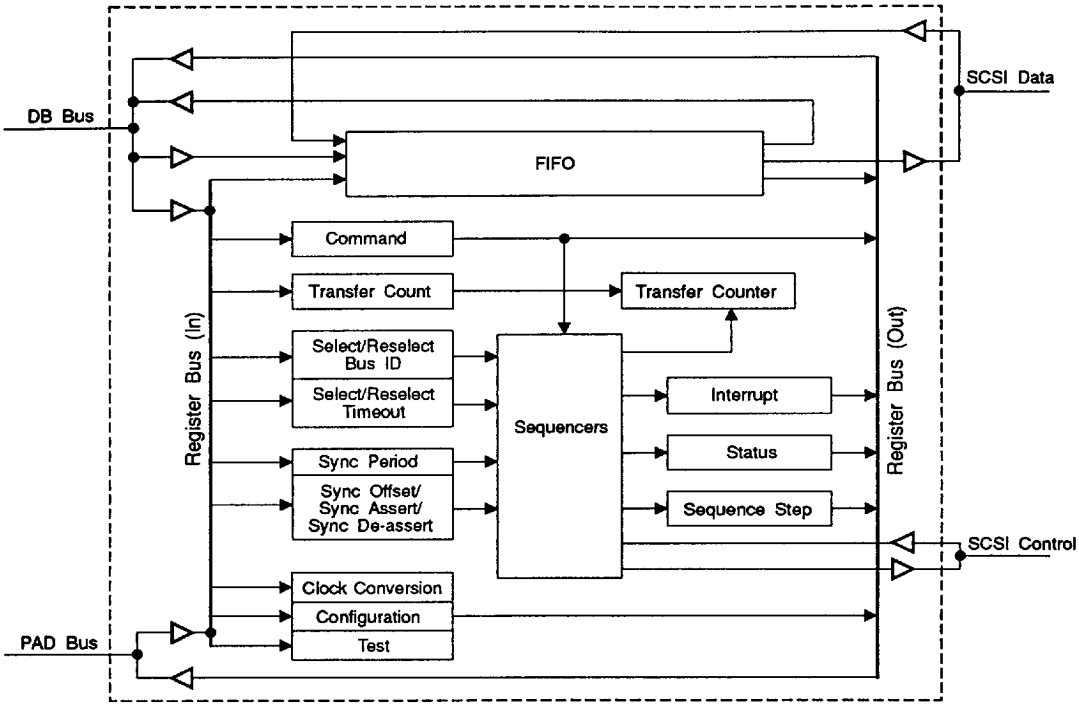
The AT43216 is designed for singled-ended operations with separate SCSI data input and output buses including on-chip 48-mA bus drivers.

Pin Configuration

84-PIN PLCC



SCSI Controller Block Diagram



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Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Temperature Range
40	5 V ± 5%	AT43216-40JC	84J	Commercial (0°C to 70°C)

Package Type	
84J	84 Lead, J-Leaded Chip Carrier (PLCC)