Philips Semiconductors-Signetics

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FAST Products	

FAST 74F670
Register File

4 x 4 Register File (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F670	6.5ns	50mA

FEATURES

- **Simultaneous and independent Read and Write operations**
- **Expandable to almost any word size and bit length**
- **3-state outputs**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F670N
16-Pin Plastic SOL	N74F670D

DESCRIPTION

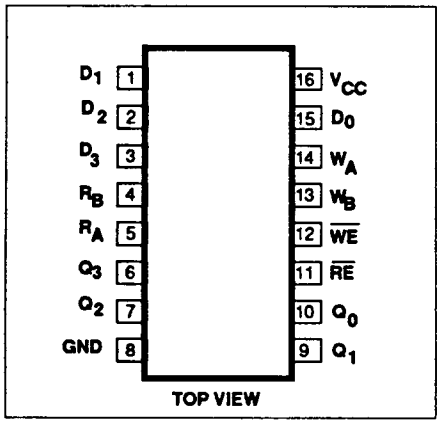
The 74F670 is a 16 bit 3-state Register File organized as a 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The Write address inputs (W_A and W_B) determine the location of the stored word. The Write Address inputs should only be changed when the Write Enable input ($\overline{WE}$) is High for conventional operation. When the $\overline{WE}$ is Low, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is Low. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs. Data and address inputs are inhibited when the $\overline{WE}$ is High. Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A, R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is Low. Data outputs are in the high impedance "off" state when the $\overline{RE}$ is High. This permits outputs to be tied together to increase the word capacity to very large numbers.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

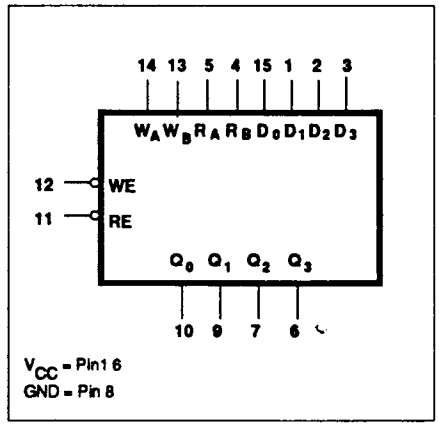
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
W_A, W_B	Write address inputs	1.0/1.0	20µA/0.6mA
R_A, R_B	Read address inputs	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{RE}$	Read Enable inputs	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Data output	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

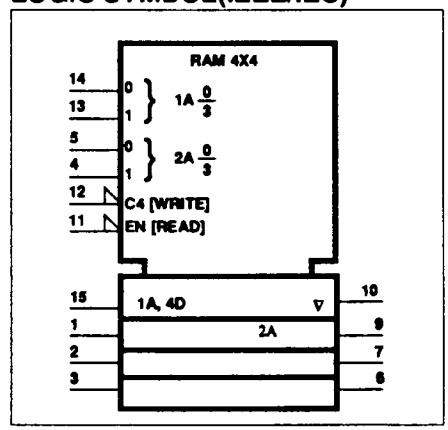
PIN CONFIGURATION



LOGIC SYMBOL



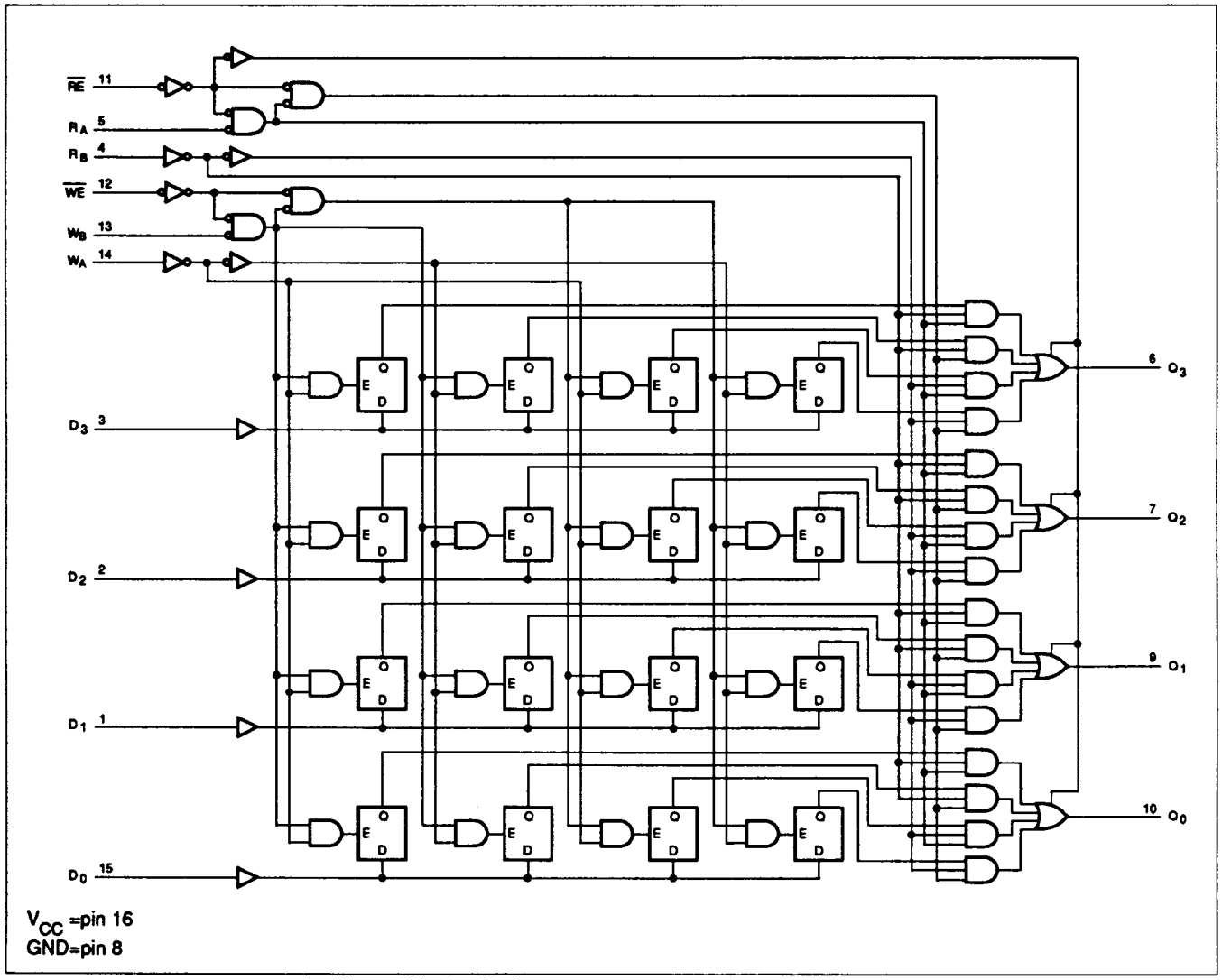
LOGIC SYMBOL(IEEE/IEC)



Register File | FAST 74F670

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-state outputs together. Since the limiting factor for expansion is the output High current, further stacking is possible by tying pullup resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the Low levels which cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and address inputs of each device in parallel.

LOGIC DIAGRAM



WORD SELECT FUNCTION TABLE

WRITE MODE		READ MODE		OPERATING MODE
W_B	W_A	R_B	R_A	Word Selected
L	L	L	L	Word 0
L	H	L	H	Word 1
H	L	H	L	Word 2
H	H	H	H	Word 3

H = High voltage level
L = Low voltage level

WRITE MODE FUNCTION TABLE

INPUTS		INTERNAL LATCHES*	OPERATING MODE
$\overline{WE}$	D_n		
L	L	L	Write data
L	H	H	
H	X	NC	Data latched

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
* = The write address (W_A and W_B) to the "internal latches" must be stabled while $\overline{WE}$ is Low for conventional operation.

READ MODE FUNCTION TABLE

INPUT	INTERNAL LATCHES*	OUTPUT	OPERATING MODE
$\overline{RE}$		Q_n	
L	L	L	Read
L	H	H	
H	X	Z	Disabled

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
* = The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			50	70	mA
		I_{CCL}				50	70	mA
		I_{CCZ}				55	80	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed lasty.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay R_A, R_B to Q_n	Waveform 2	3.5 4.0	5.5 5.5	9.0 8.5	3.0 3.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{WE}$ to Q_n	Waveform 1	5.0 6.5	7.0 8.5	10.0 11.5	4.5 6.0	11.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	3.5 6.0	6.0 8.0	8.5 11.0	3.0 5.5	9.5 12.5	ns
t_{PZH} t_{PZL}	$\overline{RE}$ Enable time Q_n to High or Low Level	Waveform 3 Waveform 4	3.0 4.5	7.0 6.5	12.0 9.0	2.5 4.0	13.0 10.0	ns
t_{PHZ} t_{PLZ}	$\overline{RE}$ Disable time Q_n to High or Low Level	Waveform 3 Waveform 4	2.0 3.0	3.0 5.0	6.5 8.5	1.5 3.0	7.5 8.5	ns

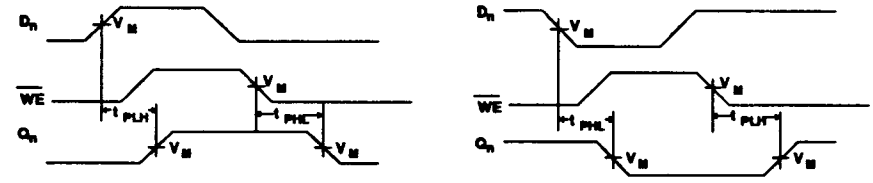
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to positive going $\overline{WE}$	Waveform 2	1.5 6.0			1.5 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to positive going $\overline{WE}$	Waveform 2	0 1.0			0 1.0		ns
t_s(H) t_s(L)	Setup time, High or Low W_A, W_B to negative going $\overline{WE}$[1]	Waveform 2	0 0			0 0		ns
t_h(H) t_h(L)	Hold time, High or Low W_A, W_B to negative going $\overline{WE}$[1]	Waveform 2	0 0			0 0		ns
t_w(L)	$\overline{WE}$ Pulse width, Low	Waveform 2	6.5			8.5		ns

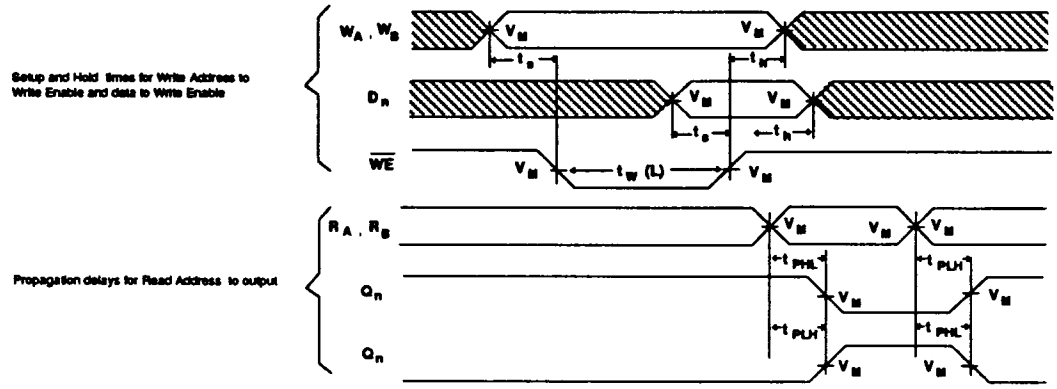
NOTES:

1. Write Address (W_A, W_B) setup time will protect the data written into the previous address. If protection of data in the previous address is not required, setup time for Write Address to $\overline{WE}$ can be ignored. Any address selection sustained for the final 7ns of the $\overline{WE}$ pulse during hold time for Write Address to $\overline{WE}$ will result in data being written into that location.

AC WAVEFORMS



Waveform1. Propagation delay, Write Enable And Data To Outputs



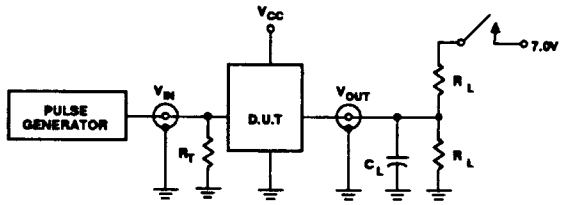
Waveform 2. Setup and Hold Times, Write Address To Write Enable and Data To Write Enable And Propagation Delay Read Address To Output

Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

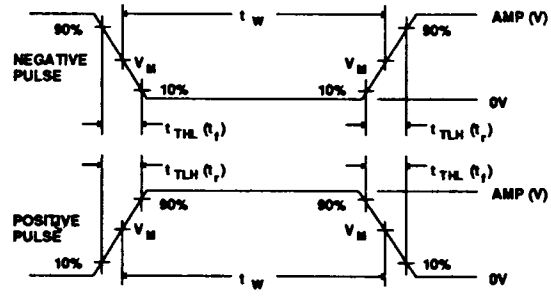
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns