Philips Semiconductors-Signetics

Document No.	853-0068
ECN No.	98494
Date of issue	January 8, 1990
Status	Product Specification
FAST Products	

FAST 74F540, 74F541 Buffers

74F540 Octal Inverter Buffer (3-State)
74F541 Octal Buffer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F540	3.5ns	58mA
74F541	5.5ns	55mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Low power, light bus loading**
- **Functional similar to the 'F240 and 'F241**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **Efficient pinout to facilitate PC board layout**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION

The 74F540 and 74F541 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature input and outputs on opposite sides of the package to facilitate printed circuit board layout.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F540N, N74F541N
20-Pin Plastic SOL	N74F540D, N74F541D

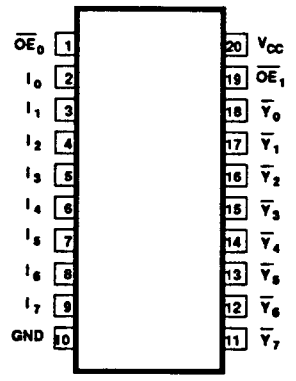
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0- I_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$ $\overline{OE}_1$	3-state output enable inputs (active Low)	1.0/0.033	20μA/20μA
Y_0- Y_7	Data outputs ('F541)	750/106.7	15mA/64mA
$\overline{Y}_0$- $\overline{Y}_7$	Data outputs ('F540)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

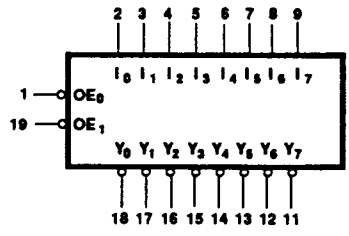
PIN CONFIGURATION

74F540



LOGIC SYMBOL

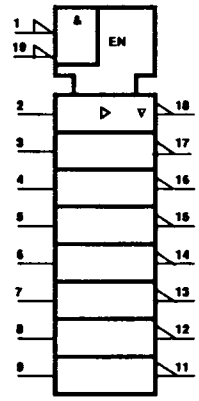
74F540



V_{CC} = Pin 20
GND = Pin 10

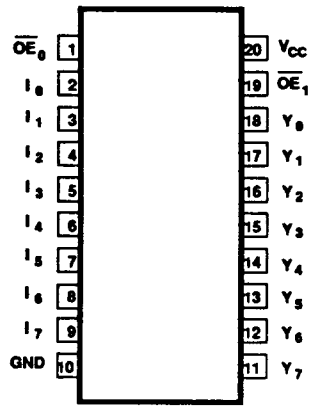
LOGIC SYMBOL(IEEE/IEC)

74F540



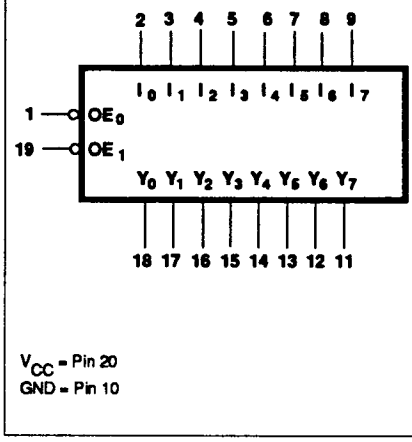
PIN CONFIGURATION

74F541



LOGIC SYMBOL

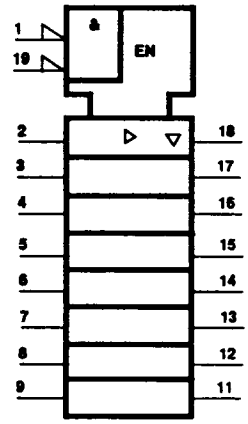
74F541



V_{CC} = Pin 20
GND = Pin 10

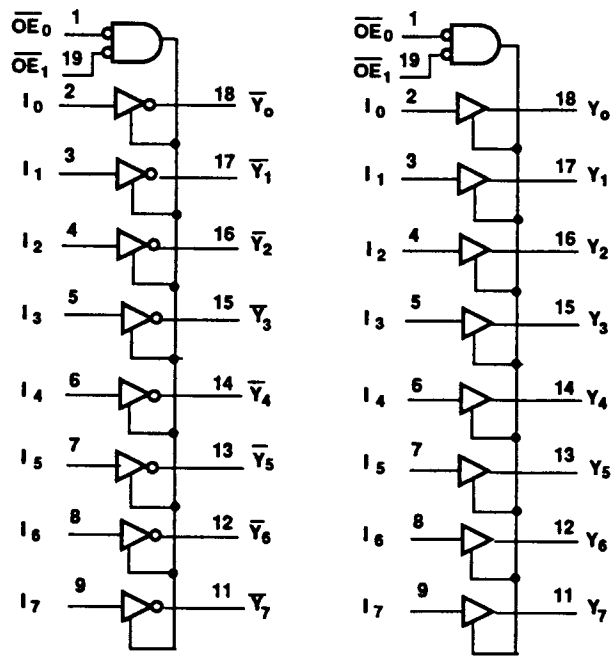
LOGIC SYMBOL(IEEE/IEC)

74F541



LOGIC DIAGRAM

74F540 74F541



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS			OUTPUTS	
			'F541	'F540
$\overline{OE}_0$	$\overline{OE}_1$	I_n	Y_n	$\overline{Y}_n$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH}=-15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
				±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F540	I_{CCH}	V_{CC} = MAX, I_n=$\overline{OE}_n$=GND		22	30	mA
			I_{CCL}	I_n=4.5V, $\overline{OE}_n$=GND		58	75	mA
			I_{CCZ}	I_n=GND, $\overline{OE}_n$=4.5V		40	55	mA
		'F541	I_{CCH}	I_n=4.5V, $\overline{OE}_n$=GND		30	40	mA
			I_{CCL}	I_n=$\overline{OE}_n$=GND		55	72	mA
			I_{CCZ}	I_n=GND, $\overline{OE}_n$=4.5V		45	58	mA

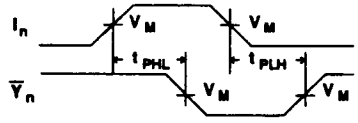
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

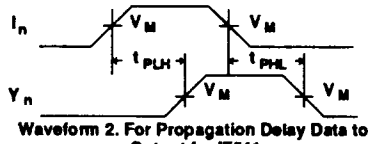
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	74F540	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 4.0	3.5 7.5	6.5 9.5	2.0 4.0	7.0 10.0	ns
t_{PZH} t_{PZL}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	74F541	Waveform 2	2.5 3.5	5.0 6.0	6.5 7.0	2.5 3.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	3.0 3.0	5.5 6.5	7.0 8.5	3.0 3.0	7.5 9.5	ns
t_{PZH} t_{PZL}	Output Disable time from High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns

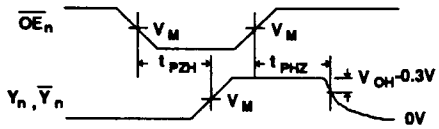
AC WAVEFORMS



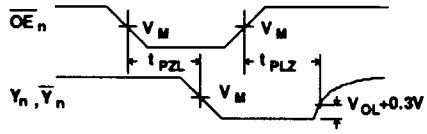
Waveform 1. For Propagation Delay Data to Output for 'F540



Waveform 2. For Propagation Delay Data to Output for 'F541



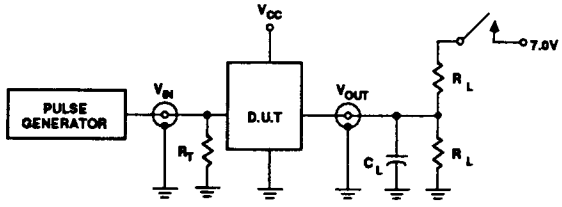
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

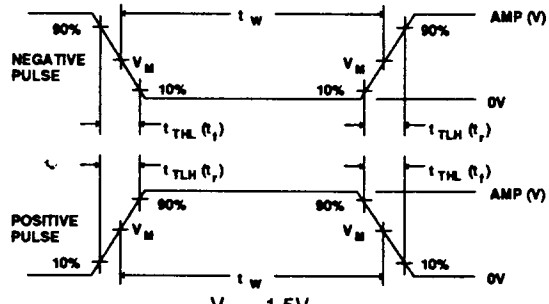
TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns