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LZ22251 B/W CCD Area Sensor

Description

LZ22251 is a 2/3 inch solid-state image sensor composed of PN photodiodes and CCDs (charge-coupled device). With its approximately 250,000 pixels (530 horizontal×490 vertical), it provides a high-resolution stable monochrome image.

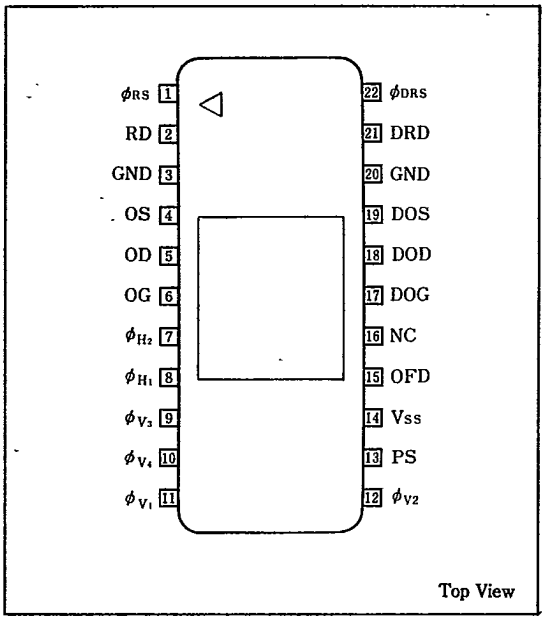
Features

1. The number of pixels of 530 horizontal×490 vertical
   Pixel pitch of 17.2 μm (H)×13.5 μm (V)
   (530 horizontal pixels consists of 510 effective pixels+20 optical black reference pixels)
2. Low fixed pattern noise and lag
3. No burn-in
4. No geometric distortion
5. Anti-blooming structure
6. Built-in output amplifier and compensation amplifier
7. 22-pin dual-in-line package (ceramic)

Applications

1. Camera (for consumer use, for industrial supervision)
2. Shape recognition

Pin Connections



Block Diagram

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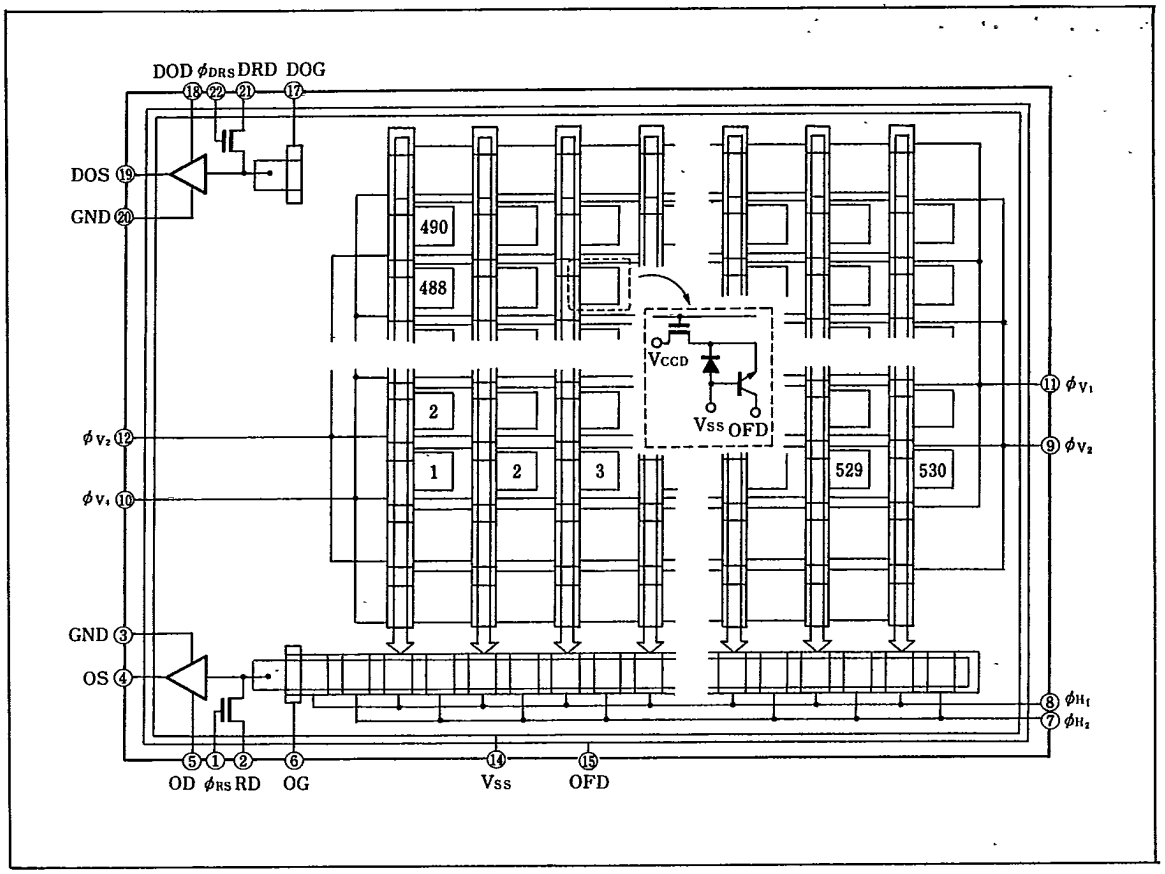

Pin Description

Pin name	Name
DRD	(Dummy) reset transistor drain
DOG	(Dummy) output gate
DOD	(Dummy) output transistor drain
DOS	(Dummy) video output
ϕ_{DRS}	(Dummy) reset transistor gate clock
ϕ_{V1}, ϕ_{V2}, ϕ_{V3}, ϕ_{V4}	Vertical shift register clock
ϕ_{H1}, ϕ_{H2}	Horizontal shift register clock
OFD	Overflow drain
PS	Photoshield
V_{SS}	Substrate
GND	Ground
NC	Non connection

■ Absolute Maximum Ratings

(Ta=25℃)

Parameter	Symbol	Conditions	Rating	Unit	Note
Applied voltages	V_{TE} ①	V_{SS}=0V	−6.0 to +20	V	1
	V_{TE} ②	V_{SS}=0V	−0.3 to +20	V	2
	V_{TE} ③	V_{SS}=0V	−0.3 to +18	V	3
	V_{TE} ④	V_{SS}=0V	0 to +22	V	4
Storage temperature	T_{stg}		−40 to +150	℃	
Operating temperature	T_{opr}		−10 to +55	℃	

Note 1 : Applied to pins ϕ_{V1}, ϕ_{V2}, ϕ_{V3} and ϕ_{V4}.
Note 2 : Applied to pins ϕ_{H1}, ϕ_{H2}, ϕ_{RS}, ϕ_{DRS}, OG, DOG and PS.
Note 3 : Applied to pins OD, DOD RD and DRD.
Note 4 : Applied to OFD pin.

■ Recommended Operating Conditions

(Frame-Integration Mode)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Operating temperature	T_{opr}	0	25.0	45.0	℃
Reset transister drain voltage	V_{RD}	13.0	13.5	14.0	V
Dummy reset transister drain voltage	V_{DRD}	13.0	13.5	14.0	V
Output gate voltage	V_{OG}	2.0	2.5	3.0	V
Dummy output gate voltage	V_{DOG}	2.0	2.5	3.0	V
Output transister drain voltage	V_{OD}	13.0	13.5	14.0	V
Dummy output transister drain voltage	V_{DOD}	13.0	13.5	14.0	V
Overflow drain voltage	V_{OFD}	4.0		19.0	V
Photoshield voltage	V_{PS}		0		V
Substrate voltage	V_{SS}		0		V
Ground voltage	GND		0		V
Vertical shift register "Low" clock	$V\phi_{V1L}$, $V\phi_{V2L}$ $V\phi_{V3L}$, $V\phi_{V4L}$	−5.5	−5.0	−4.5	V
Vertical shift register INTERMEDIATE clock	$V\phi_{V1I}$, $V\phi_{V2I}$ $V\phi_{V3I}$, $V\phi_{V4I}$	0	0.5	1.0	V
Vertical shift register "High" clock	$V\phi_{V1H}$, $V\phi_{V3H}$	5.5	6.0	6.5	V
Horizontal shift register "Low" clock	$V\phi_{H1L}$, $V\phi_{H2L}$	−0.2	0	0.35	V
Horizontal shift register "High" clock	V_{H1H}, V_{H2H}	8.5	9.0	9.5	V
Reset gate clock Dummy reset gate "Low" clock	$V\phi_{RSL}$, $V\phi_{DRSL}$	−0.2	0	0.35	V
Reset gate clock Dummy reset gate "Low" clock	$V\phi_{RSH}$, $V\phi_{DRSH}$	8.5	9.0	9.5	V
Vertical shift register clock frequency	$f\phi_{V1}$, $f\phi_{V2}$ $f\phi_{V3}$, $f\phi_{V4}$		15.75		kHz
Horizontal shift register frequency	$f\phi_{H1}$, $f\phi_{H2}$		9.58		MHz
Reset gate clock Dummy reset gate clock frequency	$f\phi_{RS}$, $f\phi_{DRS}$		9.58		MHz

Electrical Characteristics

Ta=25℃ T-41-55

Operating conditions : Use typical values for the recommended operating conditions.

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Standard output voltage	V_O	250			mV	
Photo response non-uniformity	PRNU			10	mV	1, 2
Saturation output voltage	V_{sat}	350			mV	3
Dark output voltage	V_{dark}			30	mV	
Dark signal non-uniformity	DSNU			7	mV	1, 4
Responsivity	R	20	25		mV/Lx	5, 6
Gamma	γ		1			
Signal/Noise ratio	S/N		58		dB	7
Smear ratio	SMR	65	75		−dB	8, 9
Dissipation current	$I_{OD}+I_{DOD}$	11	14	17	mA	10
Lag	AI		6	8	%	11
Antiblooming	ABL	50				12

Note 1 : The image area is sectioned into 10×10 small areas. The signal on the small area is calculated by averaging pixel signals over the small area.

Note 2 : Defined by $V_{MAX.}$-$V_{MIN.}$ under standard-exposure, where $V_{MAX.}$ and $V_{MIN.}$ are the maximum and the minimum of the signals on the small areas.

Note 3 : Under 20 times exposure of standard signal.

Note 4 : Defined by $V_{MAX.}$-$V_{MIN.}$ under non-exposure, where $V_{MAX.}$ and $V_{MIN.}$ are the maximum and the minimum of the signals on the small areas.

Note 5 : The light source is 3200°K tungsten illumination with the IR-absorbing filter (HOYA CM500 1mm thick).

Note 6 : Defined by the signal voltage at 1 lux.

Note 7 : Defined by V_s/V_{rms}, where V_{rms} is the temporal r.m.s. output noise (50k-3MHz) in the dark and V_s is the saturation output.

Note 8 : Defined by the ratio of the maximum signal to the V/10 smear level that is detected during the vertical blanking period.

Note 9 : The light source is 3200°K halogen illumination with the IR-absorbing filter (HOYA CM500, 1mm thick).

Note 10 : Defined by the total current flowing to OD and DOD pins.

Note 11 : Defined by the ratio of the maximum signal to the lag that is detected after 3-field under 1/3 standard-exposure.

Note 12 : Judged by the image of V/10 square under 50 times exposure of the knee point, where V represents the picture height.

Specification of Blemish

(T_{opr}=+55℃, Effective area except for outer 2 pixels)

Total Blemishes	3		
Blemish level	White Blemish	Over+15mV	Dark
	Black Blemish	Under−20mV	Average signal level is 150mV
Row & Column blemish	0		
Interrelation of blemish	Signal-point blemish		

Handling Precautions

1. Caution should be exercised against a possible damage to the cap caused by a mechanical stress as it uses glass building material.
2. Keep as much as you can from touching the glass surface as the charged glass surface may destroy elements inside.
3. As in the ordinary MOS or LSI, electrically conductive material should be provided for protection against an efectrostatic destruction when it is not in use.
4. When handling device, make sure that you and the tools are grounded for the static electricity to be discharged.
   A human body shall be grounded through a register of approximately 1MΩ. Keep always in mind, the electrostatic voltage be lower than the ordinary MOSs or LSIs withstand.
5. To clean the glass surface use an applicator with a small amount of iso-propyl alcohol on the tip, stroke the glass-surface gently in one direction.
6. Do not expose the device to light except in operation when the device is mounted on a camera.

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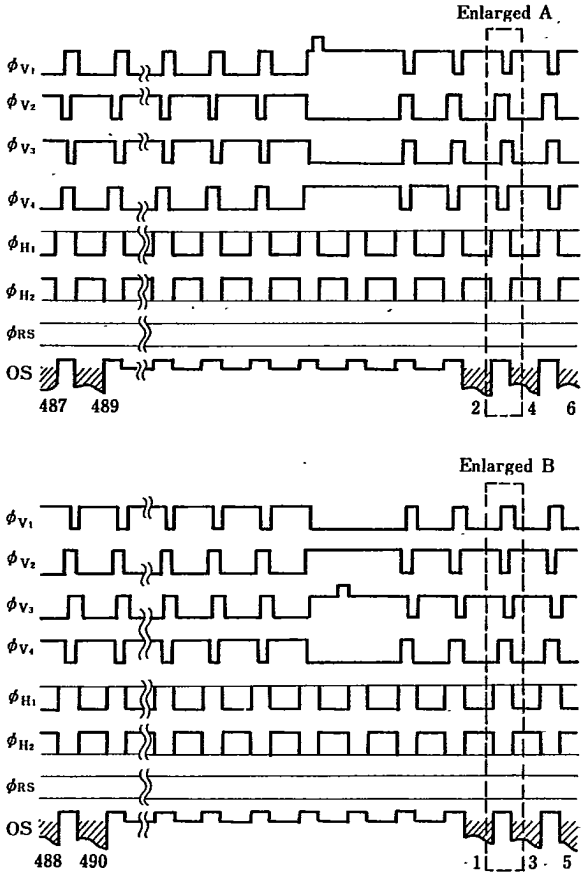
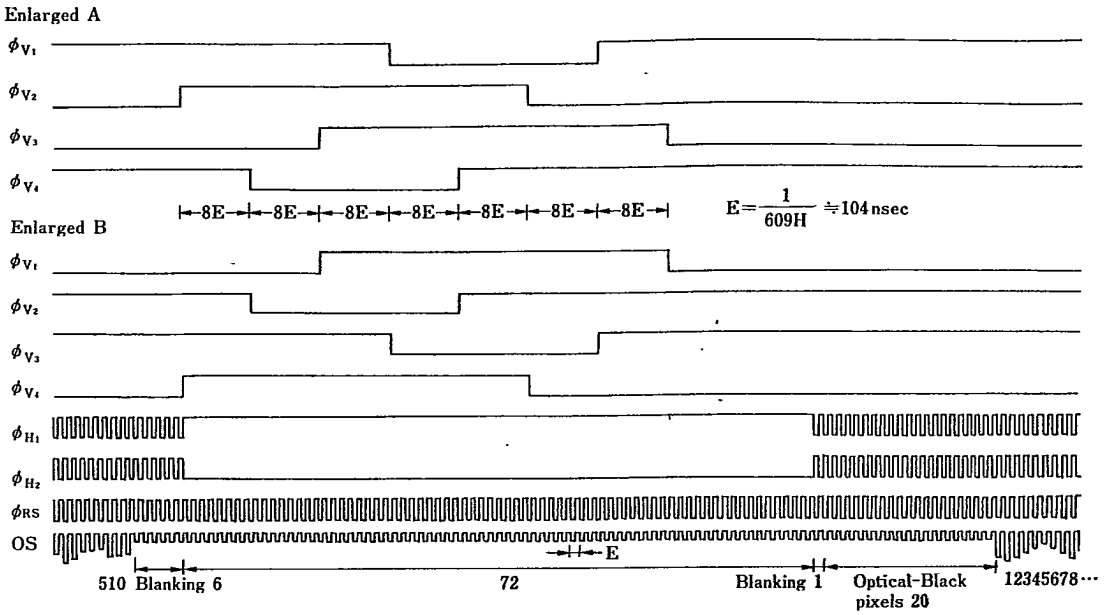
Clock Timing Chart





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■ Standard Operating Circuit

(B/W video camera for NTSC TV in the frame-integration mode)