L8150

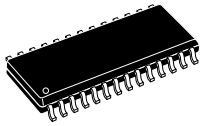
Brushless motor predriver

Feature

- Integrated Predriver IC for 3 phase BL motor.
- Integrated Smooth driving concept with sinusoidal driving waveforms.
- BCD5 technology 0.6mm.
- Package: SO28.
- Three Hall effects, differential input comparators.
- Integrated Undervoltage lockout (VCC).
- PWM output duty (voltage) control / Torque optimizer / protection functions
- PWM carrier 17kHz min / integrated dead time

Functions

- C-MOS level predriver output (high active)
- Free Run function
- Dead time (3 values selectable)
- Sinusoidal waveform PWM logic
- Detected rotation speed (FG) output terminal
- PWM duty control by analog input (KVAL control)
- Forward/backward rotation input terminal (FR) / rotation direction detection output terminal (DM)
- Thermistor connection terminal (thermal protection)
- Torque optimizer terminal controlled by analog voltage input
- V regulator output terminalExternal HVIC bootstrap capacitor pre-charge function



SO28

- External HVIC bootstrap capacitor refresh function during 120 degree drive (rectangular drive).
- This means both upper and lower chopping and low side current recirculation for rectangular drive.
- Current limiter circuit
- VCC lower voltage protection / VDC over voltage protection circuit / Hall sensor fail protection
- FAULT signal output

Description

The L8150 device is a motor predriver intended to drive brushless fan motors with Hall effect sensors. The device, realized in BCD5 0.6mm mixed technology, is characterized by a mostly digital architecture assuring high integration density and high test coverage.

The L8150 with few external components forms a complete control circuit, since the smooth driver logic is fully integrated: its peculiar driving solution (smooth driving) allows a very low current ripple and speed control even at low rotation speeds.

Order codes

Part number	Temp range, °C	Package	Packing
E-L8150	-20 to 95	SO28	TUBE
E-L8150TR	-20 to 95	SO28	Tape & Reel

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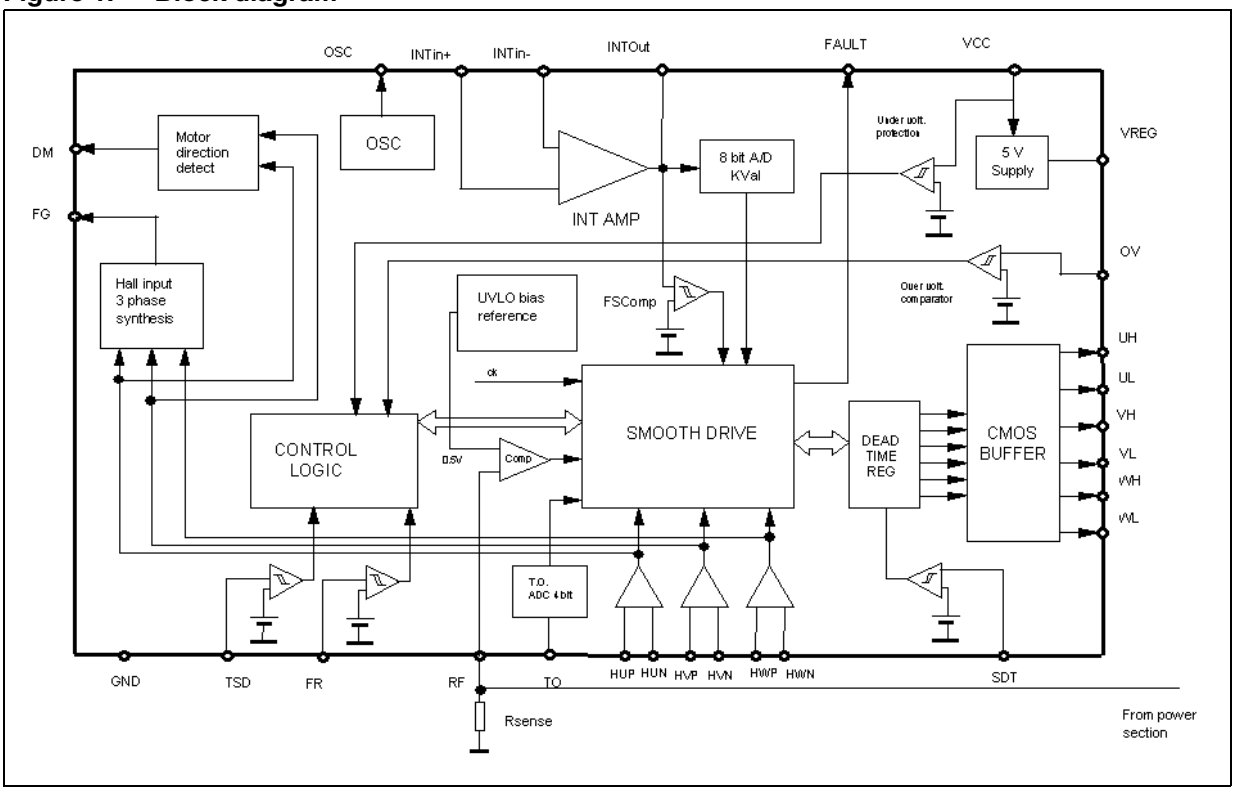
1.1 Block diagram

Figure 1. Block diagram



1.2 Pins description

Figure 2. Pins connection (top view)

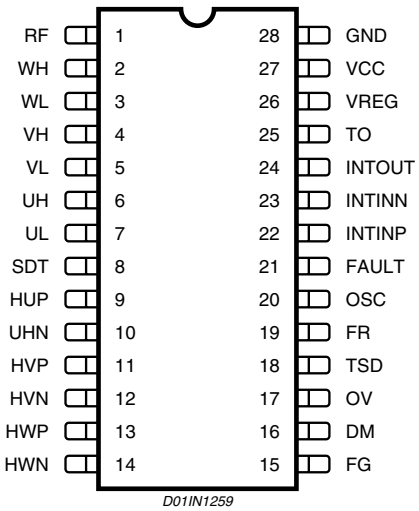


Table 1. Pins description

N°	Pin	Function
1	RF	External sense resistance pin
2	WH	W bridge high-side MOS output command
3	WL	W bridge low-side MOS output command
4	VH	V bridge high-side MOS output command
5	VL	V bridge low-side MOS output command
6	UH	U bridge high-side MOS output command
7	UL	U bridge low-side MOS output command
8	SDT	Dead time selection input pin
9	HUP	Hall sensor differential input
10	HUN	Hall sensor differential input
11	HVP	Hall sensor differential input
12	HVN	Hall sensor differential input
13	HWP	Hall sensor differential input
14	HWN	Hall sensor differential input
15	FG	Multiplexed Hall effects output
16	DM	Motor direction detected output
17	OV	Over-voltage comparator input
18	TSD	External thermal shutdown input
19	FR	Forward/backward rotation input
20	OSC	External 20.5kΩ polarization resistance pin
21	FAULT	Fault signal output
22	INTinP	Error amplifier reference input pin
23	INTinN	Error amplifier negative input pin
24	INTout	Error amplifier output
25	TO	Torque optimizer analog input
26	VREG	Internal 5V regulator output
27	VCC	External 15V supply
28	GND	Ground pin

2 Electrical specifications

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

No.	Item	Symbol	Terminal	Value	Unit	Remark
1	VCC supply voltage	V_{CC}	VCC	20	V	
2	FG terminal voltage	V_{FG}	FG	-0.3/20	V	
3	FAULT terminal voltage	V_{FAULT}	FAULT	-0.3/20	V	
4	DM terminal voltage	V_{DM}	DM	-0.3/20	V	
5	FG, FAULT, DM currents	I_{od}	FG, FAULT, DM	15	mA	Maximum current
6	RF voltage	V_{RF}	RF	-5 to VREG	V	
7	Other pin voltage		SDT,HUP,HUN,HVP HVN,HWP,HWN,OV,TSD FR,INTinN,INTinP,TO	-0.3 / 6	V	
8	Inject current		SDT,HUP,HUN,HVP HVN,HWP,HWN,OV,TSD FR,INTinN,INTinP,TO	5	mA	
9	Operating ambient temp.	T_{opg}		-20/+95	°C	
10	Junction temp.	T_j		150	°C	
11	Storage temp.	T_{stg}		-55/+150	°C	
12	Latch up tolerance		all pin	±200	mA	
13	ESD tolerance		all pin	±200	V	Machine model
				±2000	V	Human body model

2.2 Operating condition

Table 3. Operating condition

No.	item	symbol	terminal	MIN	TYPE	MAX	unit
remark							
1	supply voltage	V_{CC}	VCC	12.75	15	17.25	V

3 Electrical characteristcs

T_{amb} = 25 °C, V_{CC} =15V, V_{REG} = 5V unless otherwise specified

Table 4. Supply Voltage Terminal VCC

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	current consumption 1-1	I_{CC1-1}	VCC		10.0	20.0	mA	

Table 5. Regulator Output Terminal Vreg

NO.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	output voltage	V_{REG}	VREG	4.7	5.0	5.3	V	
2	voltage variation	ΔV_{REG1}	VREG		40	100	mV	VCC1=12.75 to 17.25V
3	load variation	ΔV_{REG2}	VREG		5	30	mV	IO=5 TO 20mA (note 1)
4	thermal coefficient	ΔV_{REG3}	VREG		0		mV/°C	

Table 6. Driver Output Terminal UH,VH,WH,UL,VL,WL

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
2	H level output voltage 2	V_{OH}	UH,…	3.70			V	IOH=-2.5mA
4	L level output voltage 2	V_{OL}	UH,…			0.40	V	IOL=2.5mA

Table 7. Dead Time Select Terminal SD

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	H level input voltage	V_{SDTH}	SDT	9/10 Vreg		Vreg	V	dead time =0 usec
2	M level input voltage	V_{SDTM}	SDT	4/10 Vreg		6/10 Vreg	V	dead time=1.5usec (Tdeadtime=15xTck)
3	L level input voltage	V_{SDTL}	SDT	0		1/10 Vreg	V	dead time=1.0usec (Tdeadtime=10xTck)

Table 8. Hall Sensor Input Terminal HUP,HUN,HVP,HVN,HWP,HWN

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	input bias current	$I_{HB(HA)}$	HUP,…	-2			uA	
2	common mode input range	V_{ICM}	HUP,…	0.50		3.00	V	for hall device
3	input voltage range	V_I	HUP,…	0.00		5.00	V	for hall IC, note 2
4	hall input sensitivity		HUP,…	50			mVp-p	
5	hysteresis width	$\Delta V_{IN(HA)}$	HUP,…	20	30	50	mV	
6	hysteresis L -> H	$V_{SLH(HA)}$	HUP,…	5	15	25	mV	
7	hysteresis H -> L	$V_{SHL(HA)}$	HUP,…	-25	-15	-5	mV	

Table 9. Torque Optimizer Input Terminal T.O.

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	max analog conversion input		T.O.		15/25Vreg			
2	min analog conversion input		T.O.		0			
3	hysteresis		T.O.		100		mV	

Table 10. Over Current Sense Input Terminal R

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	over current sense level	V_{RF}	RF	0.45	0.50	0.55	V	

Table 11. Forward Backward Select Terminal FR (note 7)

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	H level input voltage	$V_{IH\ (FR)}$	FR	2.0		VREG	V	
2	L level input voltage	$V_{IL\ (FR)}$	FR	0.0		1.0	V	
3	pull-up resistor to VREG	$R_{u\ (FR)}$	FR	-20%	50.0	+20%	kOhm	
4	hysteresis width	$V_{IS\ (FR)}$	FR	0.2	0.3	0.4	V	

Table 12. Thermal Sense Input Terminal TSD

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	TSD Threshold	$V_{IH\ (TSD)}$	TSD	2.60		3.00	V	
2	Hysteresis	$V_{hy\ (TSD)}$	TSD	0.20		0.30	V	

Table 13. FG Output Terminal FG

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	Output saturation voltage	V_{FGL}	FG			0.50	V	Io=15mA, open drain
2	Output leak current	I_{FGleak}	FG			10	uA	Vo=16.5V

Table 14. OSC Terminal OSC

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	Current setting	V_{osc}	OSC		1.235		V	R=20.5kohm (Class E96), Fsys=512*Fpwm
2	PWM frequency	F_{pwm}		18k		20.4k	Hz	17kHz - 21kHz for Tj=0 to 125 deg

Table 15. OP Amp Input Output Terminal INTin+, INTin-, INTout (note 3, note 4)

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	H level output voltage	$V_{oH\ (INT)}$	INTout	4.0	Vreg2-0.2	Vreg	V	Io=1mA
2	L level output voltage	$V_{oL\ (INT)}$	INTout			1.0	V	Io=1mA
3	input bias current	$I_{B\ (INT)}$	INTin+, -	-0.2		0.2	uA	
4	offset						V	

Table 16. Over Voltage Protection Terminal OV

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	H level input voltage (operative)	$V_{IH\ (OV)}$	OV	-6%	3.0	+6%	V	
2	Hysteresis width	$V_{IS\ (OV)}$	OV	0.3		0.4	V	

Table 17. Low Voltage Protection

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	operation voltage	$V_{IL\ (LV)}$	LV	10	11	12	V	
2	release voltage	$V_{IH\ (LV)}$	LV	10.35	11.50	12.65	V	
3	hysteresis width	$V_{IS\ (LV)}$	LV	0.35	0.50	0.65	V	

Table 18. FAULTS Output Terminal FAULTS

No.	item	symbol	terminal	MIN	TYP	MAX	unit	remark
1	output saturation voltage	$V_{FaultsL}$	FAULTS			0.50	V	Io=15mA, open drain
2	output leak current	$I_{Faultsleak}$	FAULTS			10	uA	Vo=17.25V

Table 19. Rotation Direction Detection Terminal DM

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	output saturation voltage	V_{DML}	DM			0.50	V	Io=15mA, open drain
2	output leak current	I_{DMleak}	DM			10	uA	Vo=17.25V

Table 20. KVAL Contro

No.	Item	Symbol	Terminal	Min	Typ	Max	Unit	Remark
1	FS threshold voltage		INTout	-3%	4.5Vreg/5	+3%	V	Note 3
2	KVAL Min voltage		INTout	-3%	3.7Vreg/5	+3%	V	Note 3
3	KVAL max voltage		INTout	-7%	0.7Vreg/5	+7%	V	Note 3
4	FS Hysteresis		INTout		70.0		mV	

Note: 1 If 20mA is a problem for design because of power dissipation etc., it can be reduced to something like 5mA

2 one input is set at 2.5V by means of a resistor divider. The other input moves from 0V to Vreg. The Hall comparator must operate correctly for all its input range.

3 Opamp need to be designed to meet with Kval control by VSP.
External circuit for Vsp control (example) is shown in following Figure 4.
The tolerance at Vsp including external resistor (E96) is as follows:

	mini	typ	max
V1(V)	0.85	1.23	1.6
V2(V)	1.7	2.1	2.5
V3(V)	4.9	5.4	6.1

4 FR and INTin+ are used to set test mode as follows:
Test mode is set by 8 events (clock rising edges) on FR during INTin+>4.5
(Power is kept as high-impedance for INTin+ > 4.5 until 7th event occur)
(counter for FR is reset by INTin+ < 4.5)

Figure 3. Kval control by VSP

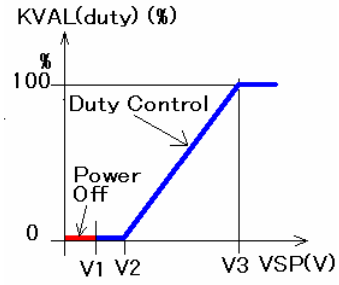
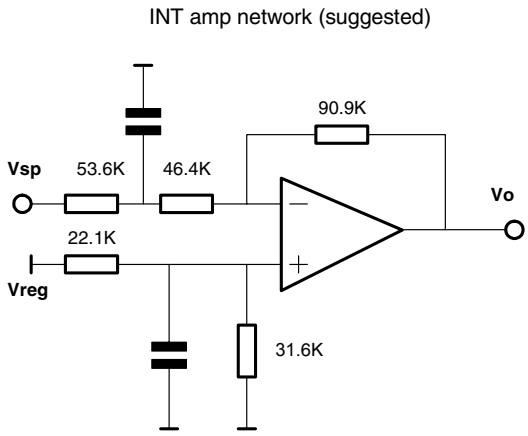


Figure 4. External circuit for Vsp control



4 General description

4.1 Drive stage

Voltage-controlled PWM drive.

Smooth drive architecture (see following dedicated paragraph).

External sense resistor as current limiter.

FR terminal: Low = Forward, High or Open = Backward.

4.2 Output

U, V, W upper and lower arm power transistors control output (6 outputs)

CMOS level (Low: 0V, High: 5V, need output buffer)

dead time (0, 1usec, 1.5usec selectable).

4.3 I/O

FG output: multiplexed by Hall signal (open drain)

(Hall signal after digital filter are used)

Forward/backward control

FAULT output: monitor signal for protection operation (low active, open drain), active if one of over voltage, lower voltage, thermal protection, Hall sensor fail protection is operative

Torque optimizer: controlled by analog input

DM output is the monitor signal of Hall input sequence:

- IF UVW hall signal sequence is as the direction set by FR, DM=H
- IF UVW hall signal sequence is opposite for the direction set by FR, DM=L
- Reset or some case in which UVW sequence can not be monitored, DM=H (Hall signals after digital filter are used for this control).

4.4 Hall Sensor Input Terminals

There are 2 types of application, Hall device and Hall IC

Hall Device application: differential inputs with some bias

Hall IC application: one input is fixed around VREG/2 by resistor divider between VREG and GND the other input comes from Hall IC whose span is between 0 and 5V.

4.5 Protection Functions

- Over-current protection: Low side current recirculation for both smooth and rectangular drive in normal working condition.
- Over-voltage protection: compare motor supply VDC (140V, 280V) and IC internal reference. All power transistor OFF (all 6 outputs = GND) during over-voltage. Return to normal operation if VDC is recovered from over-voltage condition. An hysteresis is present.

Lower voltage protection: all power TR OFF (all 6 outputs = GND), if VCC is lower than a defined voltage threshold (All power Transistors OFF if VCC is between 0 to the defined voltage threshold). Return to normal operation if VCC is recovered from lower voltage condition. An hysteresis is present.

Thermal protection: all power transistors OFF by external thermal sense signal. If signal is high (exceeds Vth), the power is OFF (all 6 output = GND).

Hall sensor fail protection: all power transistor OFF (all output = GND) if Hall signals are HHH or LLL (Hall signals after digital filter are used).

Power ON reset (SD): internal logic reset when power ON or recovery from short time Power OFF. All power transistor OFF (all 6 outputs = GND) during reset.

4.6 PWM

carrier frequency: 17-21kHz for Tj = 0 to 125 deg, 18kHz - 20.4kHz for Tj = 25 °C.

4.7 System Clock

Internal oscillator: Fsys =1/Tck= 9.8 MHz typical value.

One pin for external resistor sets the clock frequency (OSC pin).

4.8 External HVIC Bootstrap Capacitor Initialization

Lower arm ALL ON (3 outputs for low side are High, 3 outputs for High side are GND) when VSP becoming ON (free run release), (while this initialization should not be done when VSP becoming OFF) initializing time is 0.333 - 0.5 msec.

4.9 Package

28 pins SO28. It is suitable for both reflow and flow soldering.

4.10 Others

Upper and lower arm PWM during rectangular drive; it means both side (upper and lower) chopping, not one side chopping, during rectangular drive).

A maximum current of 5mA can be injected into OV protection terminal in case VCC = OFF and VDC = ON without damaging the device. Moreover the output does not cause malfunctioning (all power Transistors are OFF).

A maximum current of 5mA can be injected into TO terminal from external circuit during VCC OFF without damaging the device. The output does not cause malfunctioning (all power Transistors are OFF).

A maximum current of 5mA can be injected into INTinN terminal by VSP abnormal operation without damaging the device. The output does not cause malfunctioning (in particular it is needed to avoid VDC short-circuit by Power Transistor cross-conduction).

OSC pin sets the main bias currents for the whole device, including system clock.

5 Operating description

5.1 Free-Run (FS) and Reset (SD) functions

This device does not have an actual startup signal, the working or standby condition depends on two internally-generated signals:

- FS signal;
- SD (shut down) signal.

The first one (FS) is related to the Vsp external signal in the following way. Given the transfer function of the INTAMP network shown below, which is obtained from the suggested INTamp feedback network (see note 6 on Electrical characteristics section):

$$Vo[V] = 5.617V - 0.909 \cdot Vsp[V]$$

we have that when Vsp=1.23V, Vo equals to 4.5V; this signal (amplifier output) is fed to a comparator (FScomp) whose threshold is set at 4.5V (plus some hysteresis). When Vo is greater than 4.5V the device is in the so called "free running" mode, that is all the power outputs are in high impedance; when the threshold is crossed the logic signal FS commutates from High to Low, thus enabling normal device operation.

The second one (SD) switches from High to Low, thus enabling normal device operation. When SD is High it acts as a reset signal for the whole logic block and as a stand-by signal for the system oscillator and the speed amplifier. SD = High is generated by a low voltage condition on VREG.

5.2 Smooth Drive and Control logic description

Two basic driving techniques are applied according to different conditions:

- rectangular driving
- sinusoidal driving (Smooth Drive)

The first one is used during **startup** phase or when the motor is rotating in the opposite direction with respect to FR signal or T>TMAX, while Smooth Drive is used in normal operation.

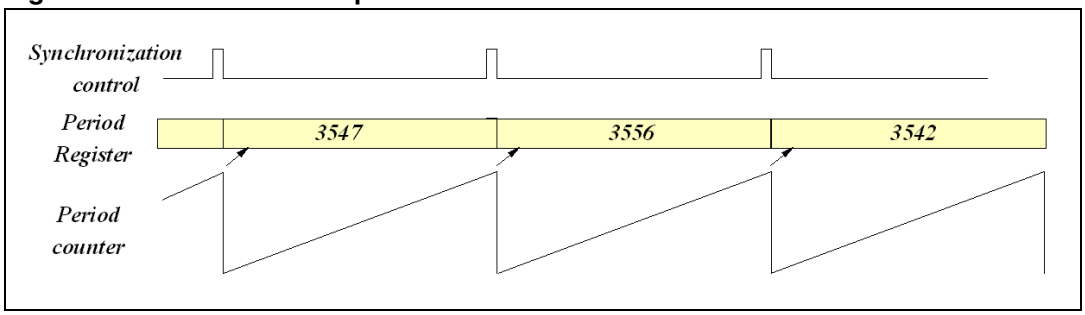
If a DC brushless motor has BEMF voltage with a sinusoidal-like shape, also the currents in the windings are sinusoidal-like, if the applied voltage is sinusoidal. This means that the torque is almost constant and the ripple is very small, allowing acoustic noise reduction and lower EMI.

Smooth Drive basically applies three voltage patterns to the motor windings, each 120 electrical degrees out of phase with respect to the other, taking as reference the period measured during the last electrical period. In order to do this, an internal 16-bit counter **(Period counter)** is provided which is triggered (current value is stored in a register and the counter is reset) at every rising edge of signal coming from U phase Hall sensor (HallU). This kind of behavior is sketched in the picture (*Figure 5*), where the synchronization control is represented by HallU rising edge.

The clock of the counter is the system clock (Fsys) divided by 36: this results in a maximum value of the electrical period that the device can measure and consequently a minimum speed at which Smooth Drive can work; this maximum period is:

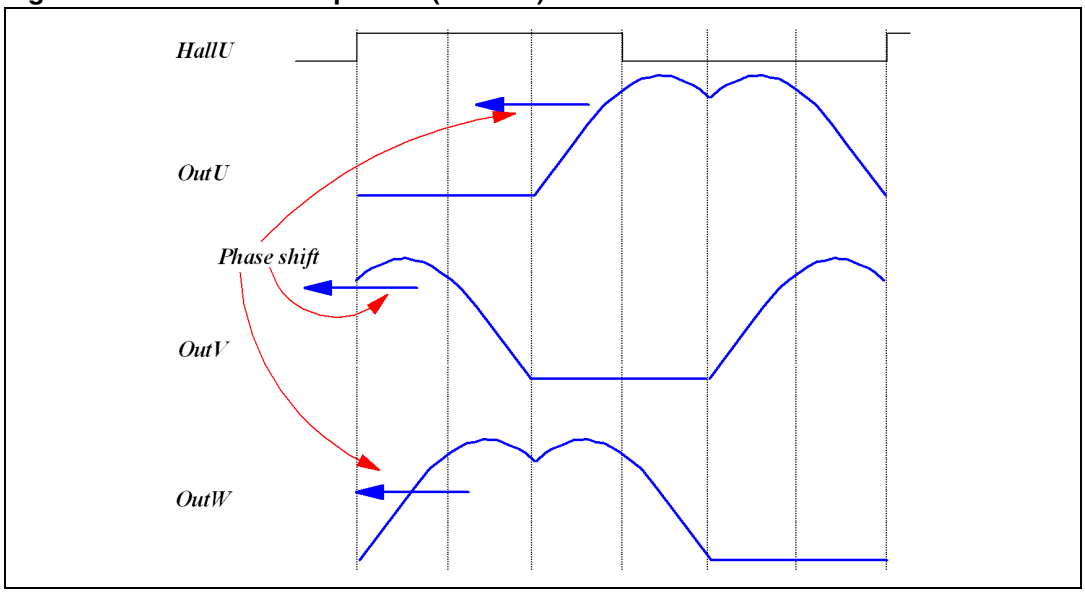
TMAX = 36*38656*Tck " 141.5 msec, with Tck = 101.7ns (Typical target value)

Figure 5. 16 bit counter operation



Smooth Drive basic functionality is to apply to the motor the voltage waveforms represented in the following pictures (*Figure 6*) in case of forward rotation (CW).

Figure 6. Smooth drive pattern (forward)



This kind of profile, which realizes waveforms that are differentially sinusoids, is digitally described by a table of 36 8-bit samples stored in a decoding circuit. The final amplitude of the voltage applied on the outputs is obtained by multiplying each sample by a value generated through an 8-bit ADC, whose input is coming from the speed control.

The motor is controlled in voltage mode, so no current control compensation network is required. Actuation is done on motor windings through a fixed frequency PWM conversion.

Since Smooth Drive is basically a voltage mode driving there can be the need of shifting the applied profile with respect to the BEMF (here sensed through the Hall sensors). This applied phase shift is called **Torque Optimizer**.

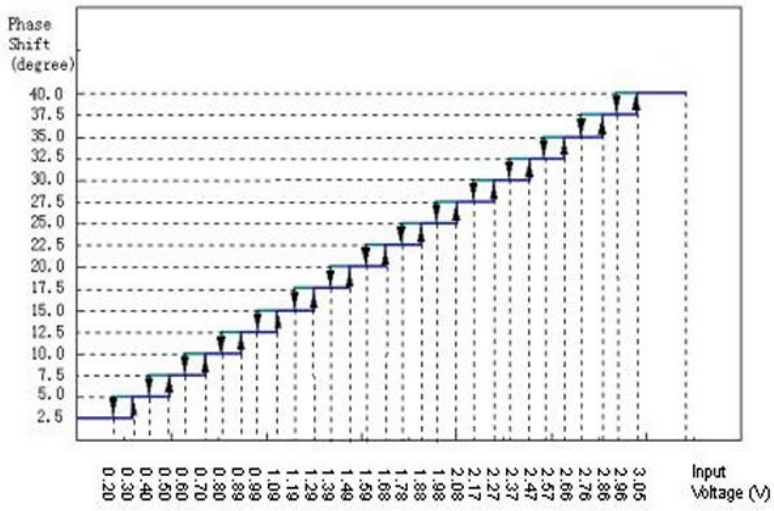
The value (expressed in electrical degrees, hereafter referred to as degrees) can be chosen applying an analog voltage to TO pin, that will be internally converted using a 4-bit A/D.

The phase shift range is from 2.5 to 40 degrees with a 2.5-degrees step. As a reference the correspondence between phase shift values and analog voltages is reported in *Table 21*.

Table 21. Phase Shift

Phase Shift [°C]	Analog low threshold [V]	Analog high threshold [V]
2.5	<0.20	<0.30
5.0	0.20	0.30
7.5	0.40	0.50
10.0	0.60	0.70
12.5	0.80	0.89
15.0	0.99	1.09
17.5	1.19	1.29
20.0	1.39	1.49
22.5	1.59	1.68
25.0	1.78	1.88
27.5	1.98	2.08
30.0	2.17	2.27
32.5	2.37	2.47
35.0	2.57	2.66
37.5	2.76	2.86
40.0	2.96	3.05

Figure 7. Phase shift vs input voltage

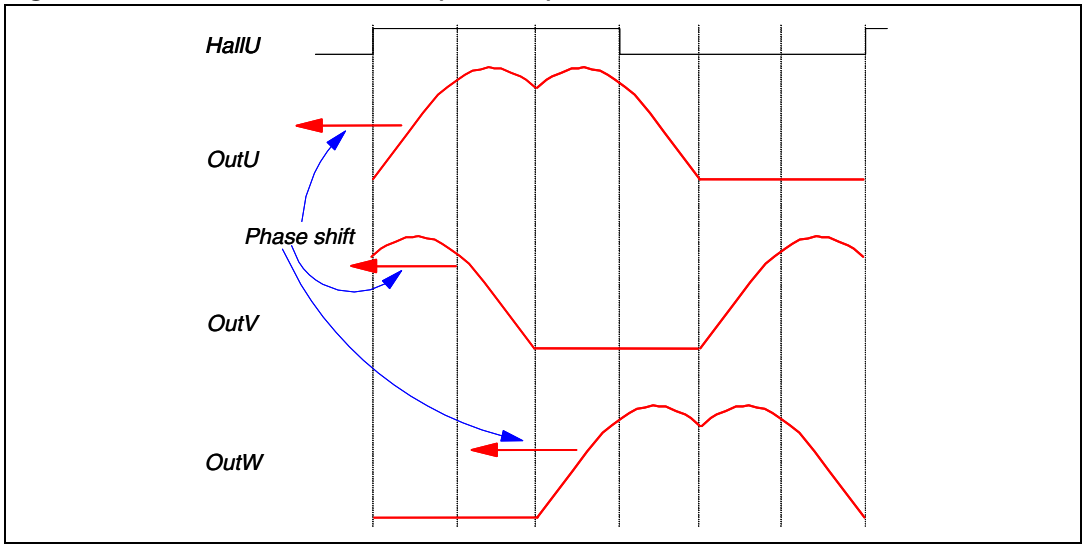


The 4-bit A/D has an internal hysteresis so that "Analog high thresholds" are the A/D thresholds applying a rising edge on TO pin, the "Analog low thresholds" are the A/D thresholds applying a falling edge on TO pin.

The applied phase shift "moves" the voltage profile with respect to the Hall effect sensor in the direction indicated by the arrows in the picture.

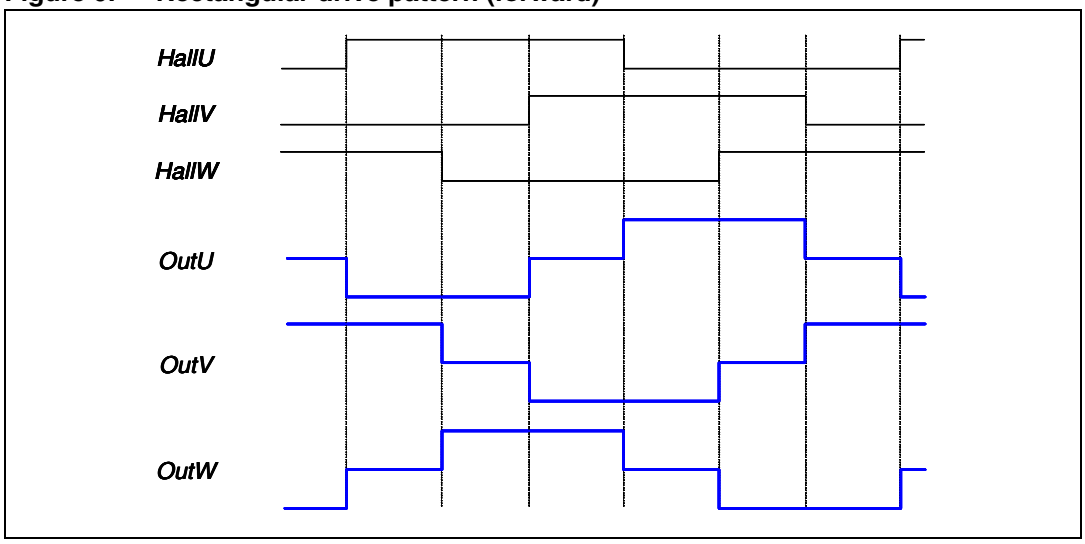
In case of **reverse** rotation **(CCW)**, Smooth Drive applies the voltage profiles represented in the following pictures (*Figure 8*).

Figure 8. Smooth Drive Pattern (Reverse)



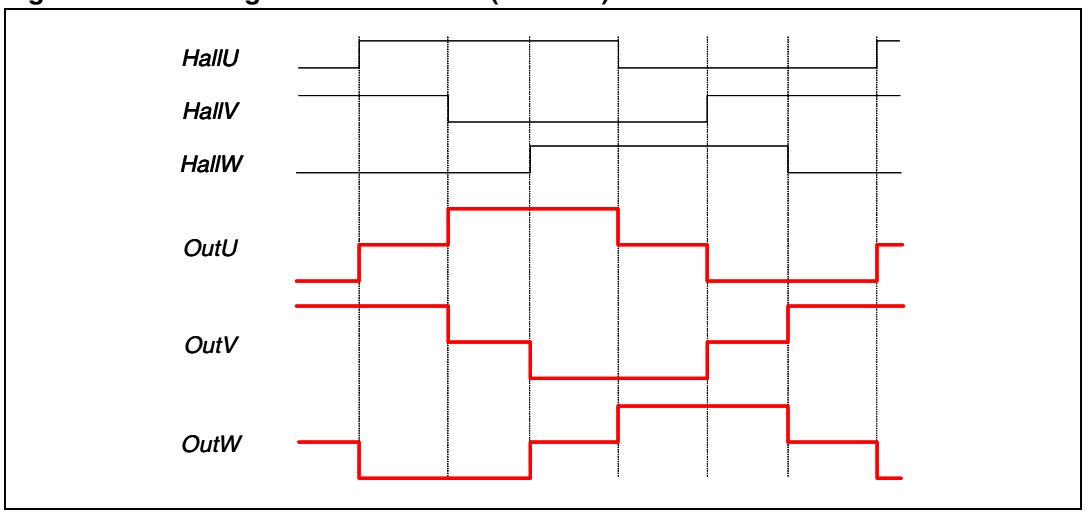
In case sinusoidal mode cannot be applied, a rectangular pattern will be applied, that is driving one phase fixed to GND, one phase in tri-state while the other is switching from low to high with a duty cycle depending on the ADC conversion , max. duty cycle about 95%, according to the following diagram:

Figure 9. Rectangular drive pattern (forward)



The diagram (*Figure 9*) is showing the applied driving pattern in case of applied torque in **forward** (continuous blue line) direction, while in case of **reverse** (continuous red line) direction, the applied pattern can be found in the following picture (*Figure 10*); in both pictures the meaning of the pattern line is the following: when the line is low, the correspondent winding is driven continuously low; when the line is high, the winding is driven with a duty cycle defined from the ADC conversion at a frequency 512 times slower than the clock. On the other hand, when the line is at middle height the correspondent phase will be left tri-stated.

Figure 10. Rectangular Drive Pattern (Reverse)



Smooth Drive mode is activated when three consecutive periods shorter than TMAX are detected and device will keep driving in Smooth mode until an external command is applied (through FR pin) or motor electrical period becomes longer than the maximum period the device is able to follow.

Startup phase (rectangular driving) is activated in one of the following conditions:

- when the Period Counter saturates;
- when the desired rotation direction (coming from FR command) is different from the detected rotation direction;
- SD = High → Low

During all working conditions a **current limitation** circuit is active. It is composed of a current comparator sensing current flowing in the sense resistor (usually a sense resistor is connected between the sources of all power low side driver transistors and ground) and of some control logic.

Current limitation is achieved in three possible ways according to the different motor situations.

The current limiter control method is a consequence of the rotation speed and the detected direction of the motor.

Let's divide the possible situations in two different cases:

1. The motor is rotating and its frequency is lower than the one used to switch between rectangular and sinusoidal driving pattern
2. The motor is rotating and its frequency is bigger than the one used to switch between rectangular and sinusoidal driving pattern

In case 1) even if the detected rotation direction is different from the desired direction, the current limiter control method is to force two phases to GND and one phase is left in high impedance state.

In case 2) the possible situations can be the following:

2a) The desired direction is equal to the detected direction and sinusoidal mode is applied, the current limiter control method is forcing all the phases to GND

2b) The desired direction is not equal to the detected direction so that rectangular mode is used, the current limiter control method is forcing all the phases in high impedance state.

In any case, current control method is updated every PWM cycle period.

The amplitude of the voltage waveform applied to the motor windings allows the control to modulate the rotation speed; this is achieved through an 8-bit analog-to-digital converter (ADC) transforming the output voltage of the control amplifier (INTAMP) into an 8-bit digital word that is used to scale the voltage waveform applied to the motor windings. A digital multiplier, whose inputs are the 8-bit samples of the voltage waveform (that is the output of the 8-bit ADC), gives an 8-bit word that represents the voltage to be applied to the motor winding.

Furthermore, control signal actuation is performed through a fixed frequency digital PWM converter, that is converting the 8-bit word coming from the comparator into a digital signal, whose duty cycle is proportional to the resulting voltage to be applied to the motor windings. The period of the PWM output signal is:

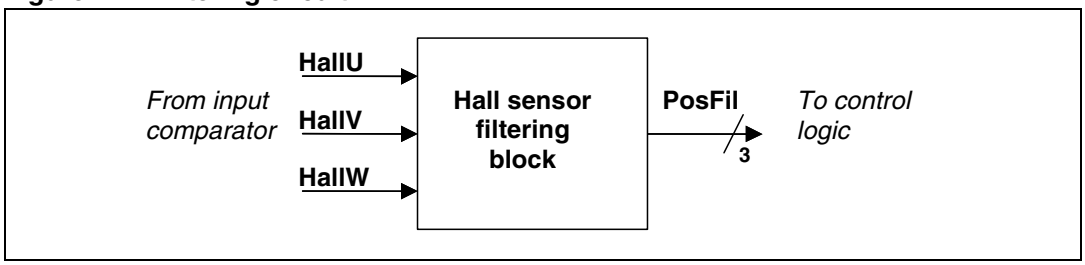
$$T_{PWM} = 512\ Tck$$

resulting in a frequency that is 19.2 kHz in the typical case.

Motor position is detected through a set of three Hall sensor, whose output is differentially fed into the device; after processing the signal by means of a comparator (whose characteristics are explained in the **Electrical Characteristics** section) the signal is furtherly filtered through a digital circuit to prevent noise from causing any device malfunctioning.

The filtering circuit processes signals coming from Hall sensors comparators (HallU, HallV, HallW) and generates a set of three internal signals used inside the digital part of the circuit (PosFil).

Figure 11. Filtering circuit



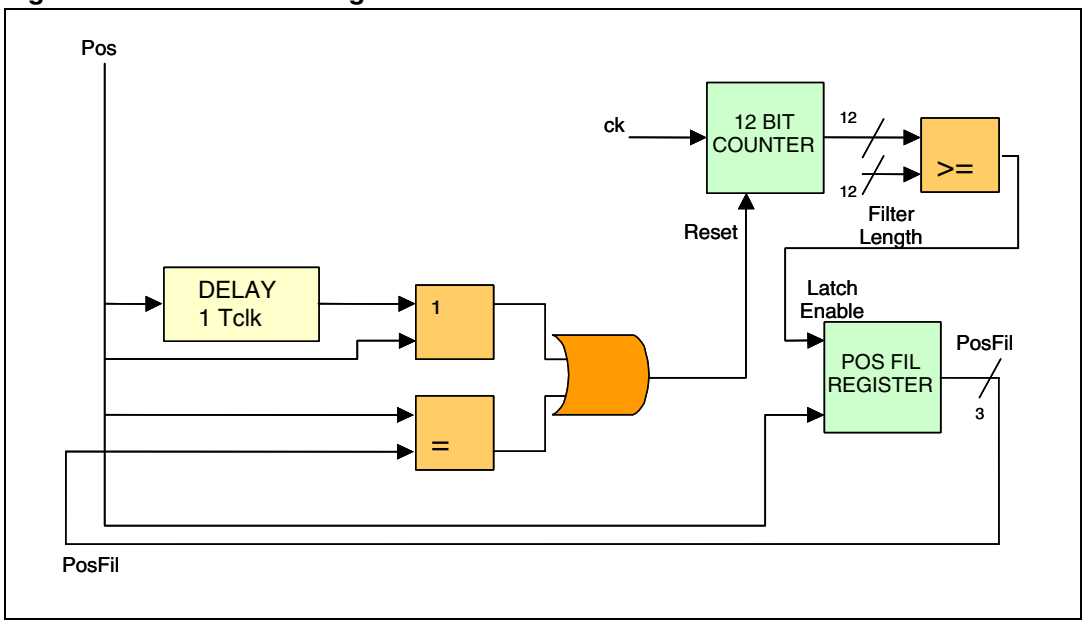
In order to simplify the explanation of the filtering circuit a signal Pos will be defined that can assume 7 different values according to the following table:

Table 22. 7 different values of the signal Pos

HallU	1	1	1	0	0	0	0
HallV	0	0	1	1	1	0	0
HallW	1	0	0	0	1	1	0
Pos	**p1**	**p2**	**p3**	**p4**	**p5**	**p6**	**pErr**

The filtering action takes place according to the following picture (Fig. 7).

Figure 12. Filter Block Diagram



The filter working principle is explained in the previous diagram (*Figure 12*): the main component of the filter circuit is a 12-bit counter that is reset (to the value 0) whenever the PosFil signal is equal to the **Pos** one. When the two signals are different (meaning that a transition is happening), the counter will start counting as long as one of the following conditions will occur:

- **Pos** signal is again equal to former **PosFil**: in this case a noise is generating some Hall comparator commutation,
- the counter has reached or overcome the value set by **Filter Length** signal: in this case the internal Hall signals will be latched into the **PosFil** register; immediately after this event, **PosFil** will become equal to **Pos** and the counter will be reset.

At the same time (at the end of the filtering time), a flip-flop detecting the direction is updated with the right direction information according to the former Hall decoding PosFil and the new one Pos, immediately before latching it into the register.

12-bit Filter Length is set to two values according to different possibilities:

- maximum filtering time, corresponding to 4096 clock periods (≈420us in the typical case, same used for pre-charge function) when an hall effect commutation is detected just after a startup signal edge (SD or FS) and before TMAX/6 is elapsed. This filtering time is also used when the motor accelerate starting from a stopped condition (no hall effect commutation is detected from FS or SD edge to TMAX/6)
- the filter length is a fraction of the elapsed time between two Zero Crossing signal (ZC). During normal working (in case motor period is shorter than TMAX) it is equivalent to 0.625 electrical degrees.

A ZC signal is produced every time one of these situations happens:

- a falling edge of the FS signal is detected
- a rising edge of the HallU signal is detected
- any hall effect commutations when the high impedance condition is forced by the IC and the motor is in free-run condition

5.3 Speed Control Circuitry

The rotation speed control signal (VSP) is an external signal, whose range is 2.1V÷5.4V. This signal is amplified by an inverting amplifier which takes as reference a voltage derived from VREG through a voltage divider.

The amplifier output is the input signal of an 8-bit ADC which generates the digital word KVAL, used to determine the duty cycle value according to the following *Figure 13*:

Speed control:

Intout 0-0.7V: duty =100% for smooth drive

(max duty is limited at about 95% for rectangular as shown in the following figure)

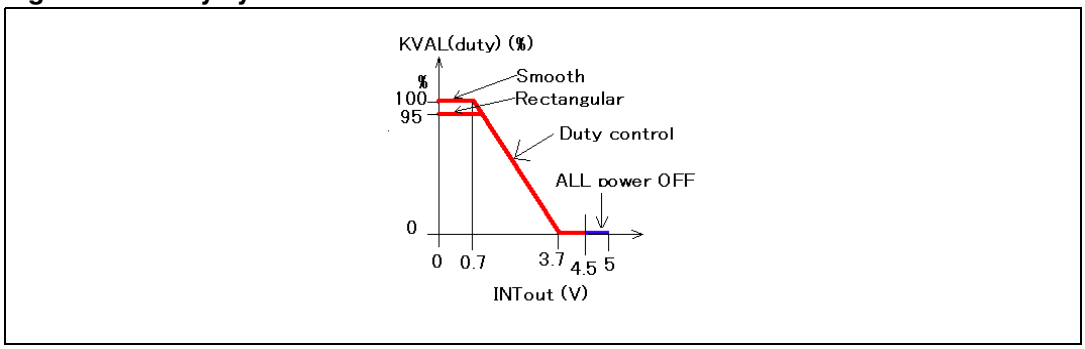
Intout 0.7-3.7V: duty control 100-0%

Intout 3.7-4.5: duty = 0 %

Intout 4.5V - 5V (VREG): all power off (all 6 output = GND)

(Each Vth depends linearly on VREG, being obtained by means of voltage dividers).

Figure 13. Duty cycle

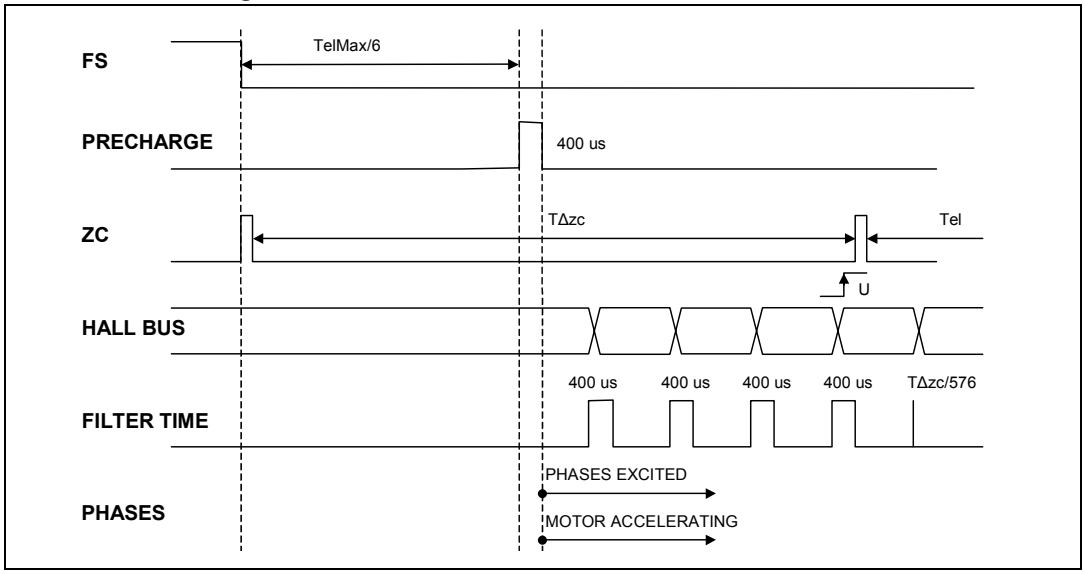


6 Precharge and hall effects filtering time description

6.1 Startup sequence with FS signal

- Let's startup sequence forced by FS comparator, assuming the motor is not rotating:

Figure 14. Startup sequence forced by FS comparator, assuming the motor is not rotating



When the signal coming from the FS comparator has a falling edge (corresponding to a Vsp signal crossing the 1.23V threshold), the logic starts counting, to verify if the motor is rotating or not. If the motor is stopped and no Hall effect commutation is detected, the counter has reached its saturation time, given by the following equation:

$$Tel_{MAX} = (7MHz)^{-1} \cong 141.5msec \Rightarrow \frac{Tel_{MAX}}{6} \cong 24msec$$

N.B. TelMAX is equal to TMAX used in the previous sections of this document.

After this saturation time the logic has decided to do a precharge function, and for a period of time given by the following equation all the output logic signals UL,VL,WL become high while the signals UH, VH, WH are low.

$$T_{CHARGE} = 4096 \cdot T_{ck} \cong 400\mu sec$$

When the precharge is over, the logic outputs start applying the right rectangular pattern to accelerate the motor.

During this sequence the Hall filtering time is 400usec until the first rising edge on signal HallU is detected. Then a filter given by the following equation is used:

$$T_{FILTER} = \frac{1}{576} \cdot T\Delta_{ZC}$$

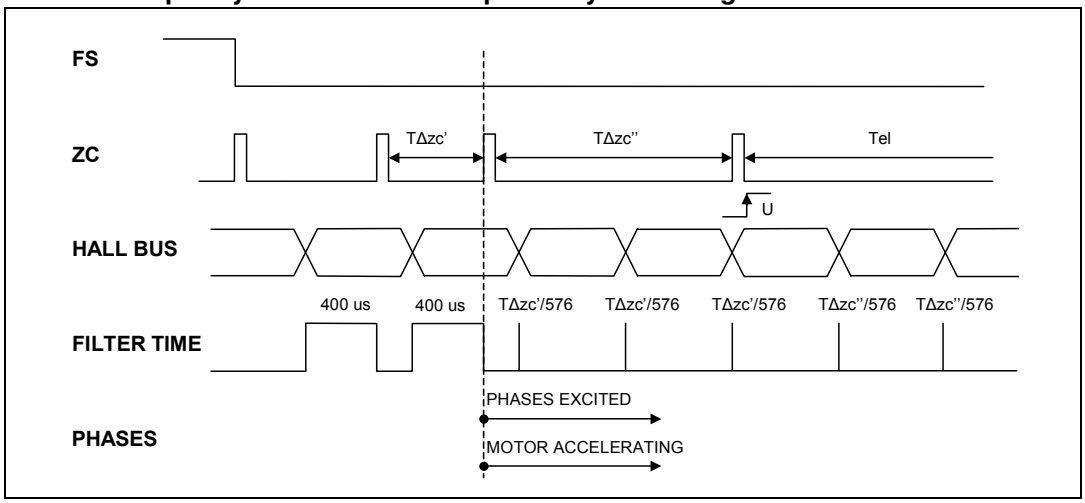
TΔZC is the elapsed time between two consecutive zero-crossing signals. By default a zero-crossing signal is generated when a falling edge of the FS comparator is detected, and after that a zero-crossing signal is generated when a rising edge on signal HallU is detected.

Assumed this operation mode, it is easy to understand that as soon as the startup sequence is over, Hall effects commutations are filtered using a fraction of the electrical period given by the following equation, since TΔZC is equal to TEL when two consecutive zero-crossing signals generated by a rising edge on signal HallU are detected:

$$T_{FILTER-ROATING} = \frac{1}{576} \cdot T\Delta_{ZC} = \frac{1}{576} \cdot T_{EL}$$

- Let's consider a startup sequence forced by FS comparator, supposing the motor rotating quickly in the direction imposed by the FR signal:

Figure 15. Startup sequence forced by FS comparator, supposing the motor rotating quickly in the direction imposed by the FR signal:



When the signal coming from the FS comparator has a falling edge, by default a zero-crossing signal is generated and the logic waits for a Hall effect commutation and applies to it a filtering time of $T_{PRECHARGE}$=400μsec. The first significant zero-crossing signal is generated.

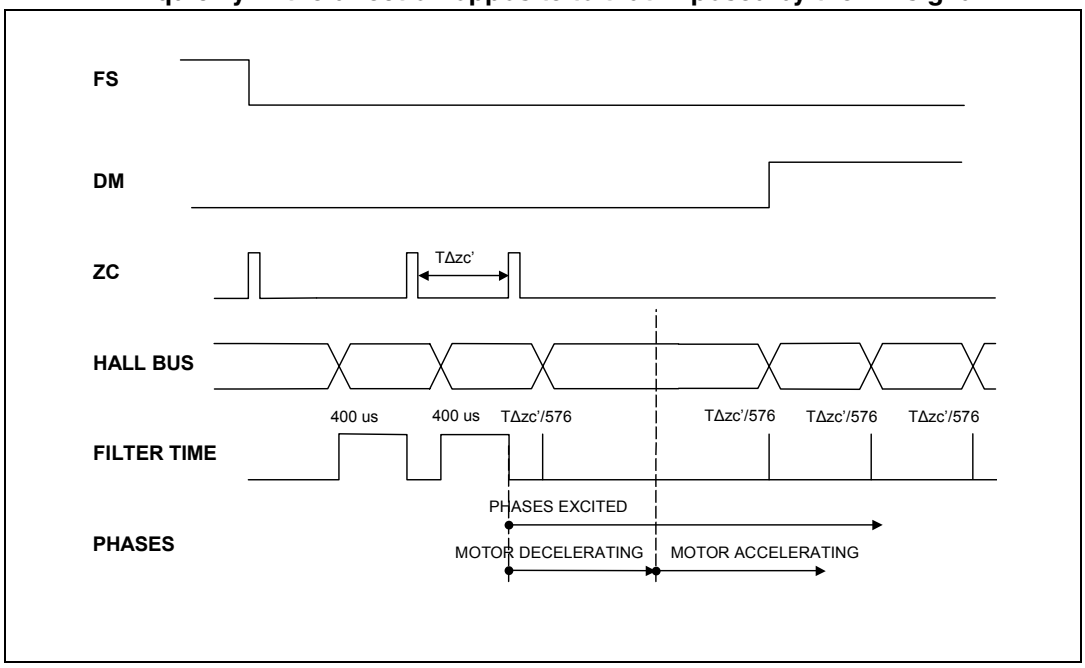
Also the second Hall effect commutation is filtered using $T_{PRECHARGE}$, after that the second zero-crossing signal is generated.

Starting from the second Hall effect commutation, after the acquisition of the filtered Hall commutation, the logic outputs start applying the right pattern, and the motor is able to accelerate again.

The next filtering time used for the Hall commutation is a fraction of the elapsed time between the first two Hall effect commutations, according to the previous T_{FILTER} equation. This filtering time is used until the first rising edge on signal HallU is detected and a zero-crossing signal is generated. After that the filtering time used is a fraction of the elapsed time between the last two detected zero-crossing signals, in other words between the second Hall effect commutation and the rising edge on signal HallU. Finally, when the second rising edge on signal HallU is detected, the filtering time used is a fraction of the electrical period, as described in previous $T_{FILTER-ROTATING}$ equation.

- Let's consider a startup sequence forced by FS comparator, supposing the motor rotating quickly in the direction opposite to that imposed by the FR signal:

Figure 16. Startup sequence forced by FS comparator, supposing the motor rotating quickly in the direction opposite to that imposed by the FR signal



This situation is similar to the one described before, except DM behaviour. Let's suppose the FS signal high, which means all phases in high impedance state. Even if the signal FS is high, the logic is able to detect if the motor is rotating in the desired direction or not. So when the signal coming from the FS comparator has a falling edge, by default a zero-crossing signal is generated and the DM signal is already low, indicating that the detected direction is not equal to desired direction.

From now on the logic waits for a Hall effect commutation and applies to it a filtering time of $T_{PRECHARGE}$=400µsec. The first significant zero-crossing signal is generated.

Also the second Hall effect commutation is filtered using $T_{PRECHARGE}$, and the second zero-crossing signal is generated.

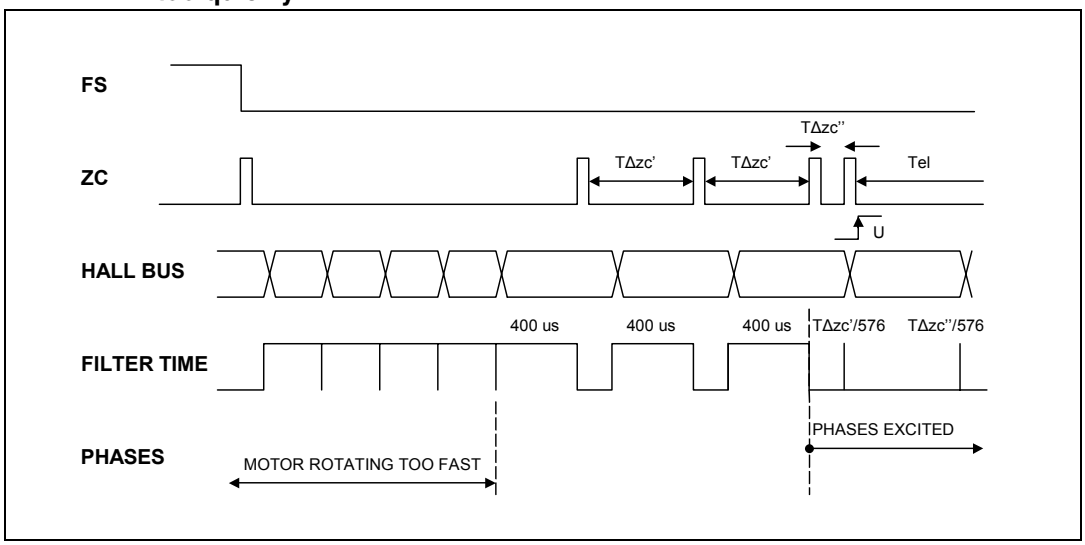
Starting form the second Hall effect commutation, after the acquisition of the filtered Hall commutation, the logic outputs start applying the rectangular pattern, and the motor is able to decelerate until the rotation direction changes becoming equal to the desired one.

After the first two Hall commutations, the filtering time used is a fraction of the elapsed time between the first two Hall effect commutations, according to the previous T_{FILTER} equation. This filtering time is used until the first rising edge on signal HallU is detected and a zero-crossing signal is generated. After that the filtering time used is a fraction of the elapsed time between the last two detected zero-crossing signals, in other words between the second Hall effect commutation and the rising edge on signal HallU. Finally, when the second rising edge on signal HallU is detected, the filtering time used is a fraction of the electrical period, as described in previous $T_{FILTER-ROTATING}$ equation.

Only when a Hall effect commutation consistent with the desired direction is detected the DM signal becomes high, indicating the right direction detection.

- Let's consider a startup sequence forced by FS comparator, supposing the motor rotating too quickly:

Figure 17. Startup sequence forced by FS comparator, supposing the motor rotating too quickly



When the signal coming from the FS comparator has a falling edge, by default a zero-crossing signal is generated and the logic waits for a Hall effect commutation and applies to it a filtering time of $T_{PRECHARGE}$ = 400µsec. If the motor is rotating too quickly the next Hall effect commutation happens before the filtering time is elapsed: this causes the reset of the filter and, in consequence, a new count for the filter time of 400µsec. Until the motor is rotating too quickly no Hall effect commutation is acquired by the logic, thus the logic outputs force high impedance condition.

Only when the motor speed becomes lower than the speed necessary to obtain a Tel/6>400µsec the Hall effect commutations are filtered and acquired.

If no Hall effect commutation is acquired during a period of TelMax/6, a precharge function will be done.

Depending on the last filtered Hall effect codification present in the logic and, also, on the Hall effect codification having a duration longer than 400µsec (because the Hall effect codifications filtered have to be consecutive), the Hall effect commutations filtered using a filter time of 400usec could be two or, more probably, three.

After this Hall effect commutations the logic outputs start applying the right pattern to the motor windings.

The motor rotation direction is irrelevant, in fact this can influence only the kind of pattern applied after the two or three filtered Hall effect commutation.

- Let's consider a startup sequence forced by FS-Comparator, supposing the motor rotating slowly.

When the signal coming from the FS comparator has a falling edge, the logic waits for a Hall effect commutation for a period of time equal to TelMAX/6. If no Hall effect commutation happens during this time, the behaviour is the one described in the previous section, when a startup sequence with motor stopped is described.

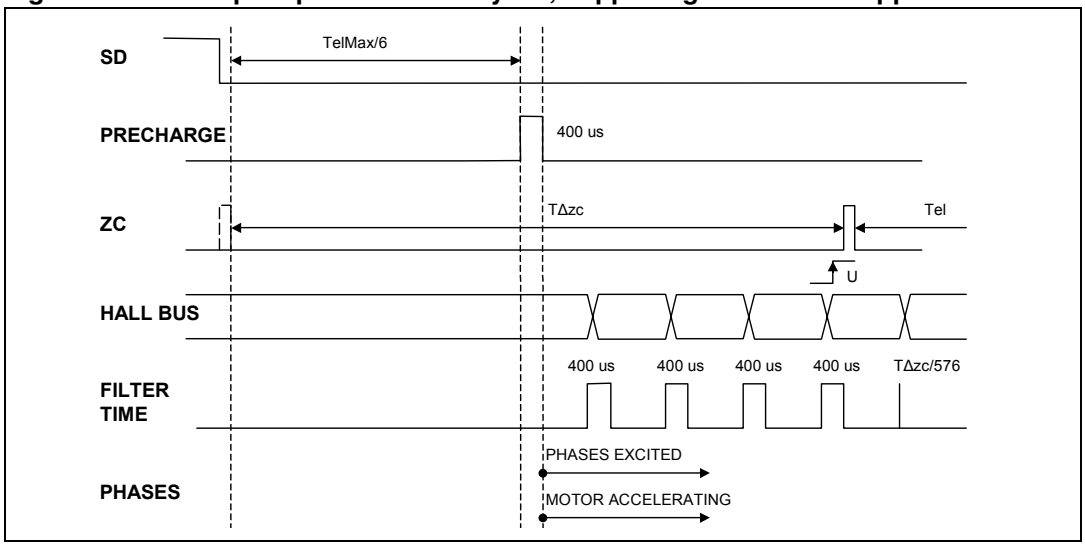
Let's suppose that during the counting period of TelMAX/6 a Hall effect commutation is detected. This commutation is filtered using 400usec. Considering the hypothesis done, starting from the Hall effect commutation detection, no more commutation will be detected

for the successive TelMAX/6 and the behaviour is the one described in the startup sequence with motor stopped.

6.2 Startup sequence with SD signal

- Let's consider a startup sequence forced by SD, supposing the motor stopped:

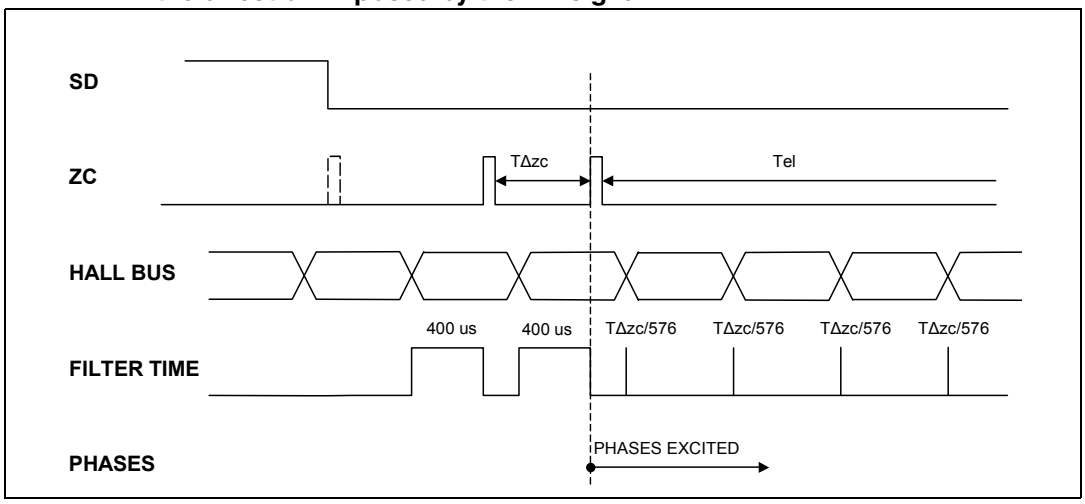
Figure 18. Startup sequence forced by SD, supposing the motor stopped



When the SD signal has a falling edge (corresponding to a VREG signal that's crossing the lower voltage protection), the logic can produce a ZC signal, depending on FS signal behaviour induced by Vsp voltage value. In any case, even if no ZC signal is produced, if the motor is stopped and no Hall effect commutation is detected, the counter reaches its saturation time TelMAX/6 and the system evolves like in the situation described in previous startup sequence with motor stopped.

- Let's consider a startup sequence forced by SD, supposing the motor rotating quickly in the direction imposed by the FR signal:

Figure 19. Startup sequence forced by SD, supposing the motor rotating quickly in the direction imposed by the FR signal



When the SD signal has a falling edge the logic acquires the Hall codification and waits for next Hall effect commutation, which is filtered using a filtering time of $T_{PRECHARGE}$ = 400µsec. The first significant zero-crossing signal is generated.

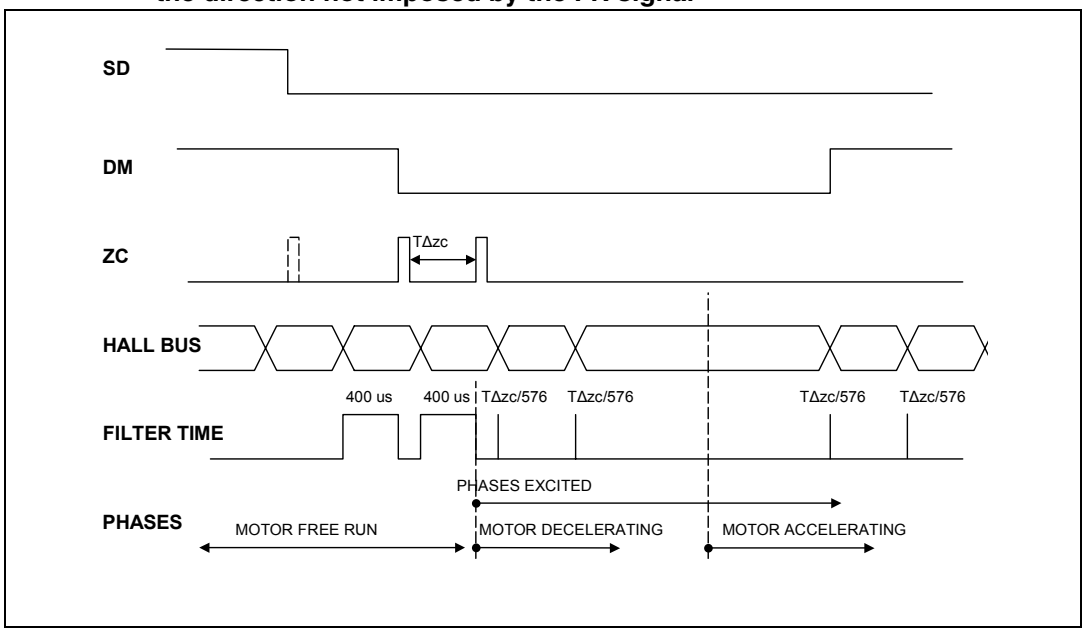
Also the second Hall effect commutation is filtered using $T_{PRECHARGE}$, after that the second zero-crossing signal is generated.

Starting form the second Hall effect commutation, after the acquisition of the filtered Hall commutation, the logic outputs start applying the right pattern, and the motor is able to accelerate again.

Next filtering time used for the Hall commutation is a fraction of the elapsed time between the last two zero-crossing signals TDzc. This filtering time is used until the first rising edge on signal HallU is detected and a new zero-crossing signal is generated.

- Let's consider a startup sequence forced by SD, supposing the motor rotating quickly in the direction not imposed by the FR signal:

Figure 20. Startup sequence forced by SD, supposing the motor rotating quickly in the direction not imposed by the FR signal



This situation is similar to that described before, except DM behaviour. Let's suppose the SD signal high, which means all phases in high impedance state. Since the signal SD is high and considering that this is the reset signal for the whole logic part, the system is not able to detect if the motor is rotating in the desired direction or not and by default the DM signal will be high. So when the signal SD has a falling edge, the DM signal remains high, indicating that the detected direction is equal to desired direction.

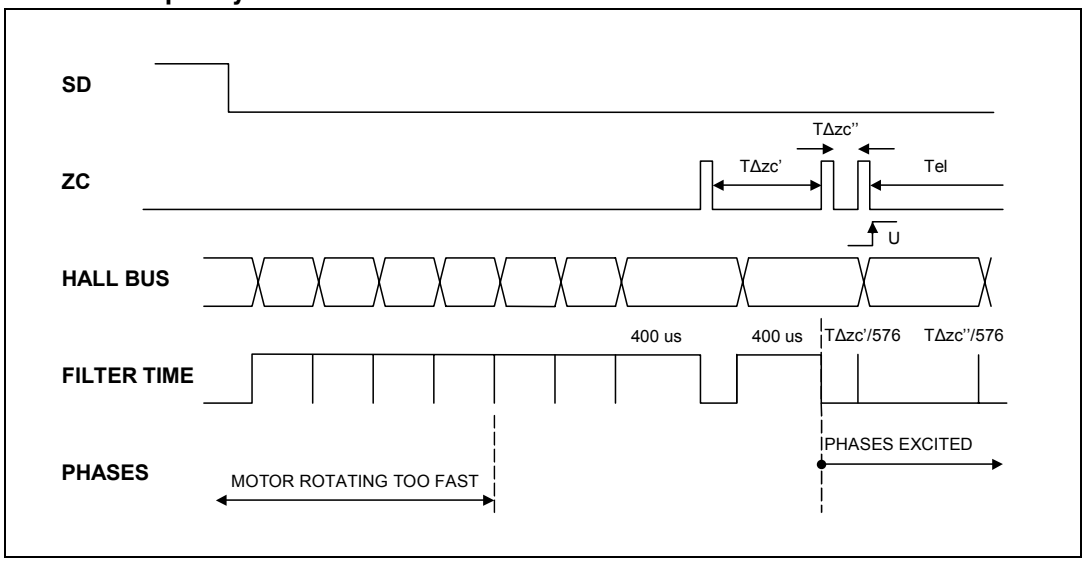
Only after the first filtered Hall effect commutation the system is able to determines if the rotation direction is equal to the desired one. At this moment the DM signal becomes low.

Starting from the second Hall effect commutation, after the acquisition of the filtered Hall commutation, the logic outputs starts applying the right pattern, and the motor starts to decelerate.

Only when an Hall effect commutation consistent with the desired direction is detected, the DM signal becomes high, indicating the right direction detection.

- Let's consider a startup sequence forced by SD signal, supposing the motor rotating too quickly:

Figure 21. Startup sequence forced by SD signal, supposing the motor rotating too quickly



When the SD signal has a falling edge the logic waits for an Hall effect commutation. If the motor is rotating too quickly the next Hall effect commutation occurs before the filtering time has elapsed.

This means that a new Hall filter count is performed and no Hall effect codification is acquired until $T_{PRECHARGE}$ has elapsed while the Hall bus is not changed.

Until the motor rotates too quickly no Hall effect commutation is acquired by the logic, thus the logic outputs force high impedance condition.

Only when the motor speed becomes lower than the speed necessary to obtain a Tel/6>400µsec the Hall effect commutation are filtered and acquired.

After the first two or three filtered Hall effect commutations (because they have to be consecutive), the logic outputs start applying the right pattern to the motor windings.

The motor rotation direction is not important, in fact this can influence only the kind of pattern applied after the two or three filtered Hall effect commutation. In the picture is reported the less likely situation.

- Let's consider a startup sequence forced by SD, supposing the motor rotating slowly.

When the signal coming from the SD-Comparator has a falling edge, the logic waits for an Hall effect commutation for a period of time equal to TelMAX/6. If no Hall effect commutation occurs during this time, the behaviour is that described in the previous section, when a startup sequence with motor stopped is described.

Let's suppose that during the counting period of TelMAX/6 an Hall effect commutation is detected. This commutation is filtered using 400µsec. Considering the hypothesis done, starting from the Hall effect commutation detection, no more commutation will be detected for the following TelMAX/6 and the behaviour is the one described in the startup sequence with motor stopped.

7 Application example

Figure 22. Basic motor control circuit

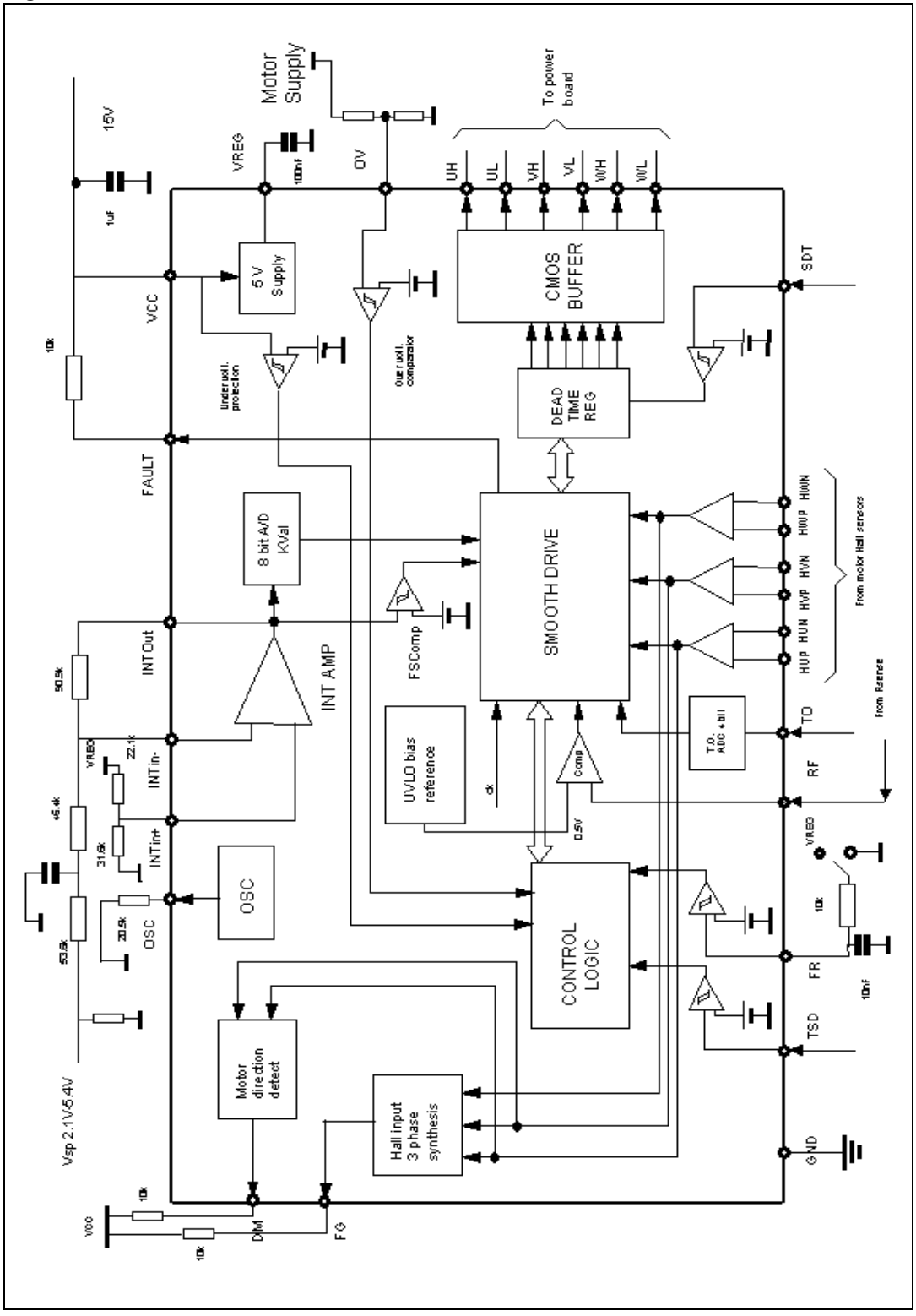
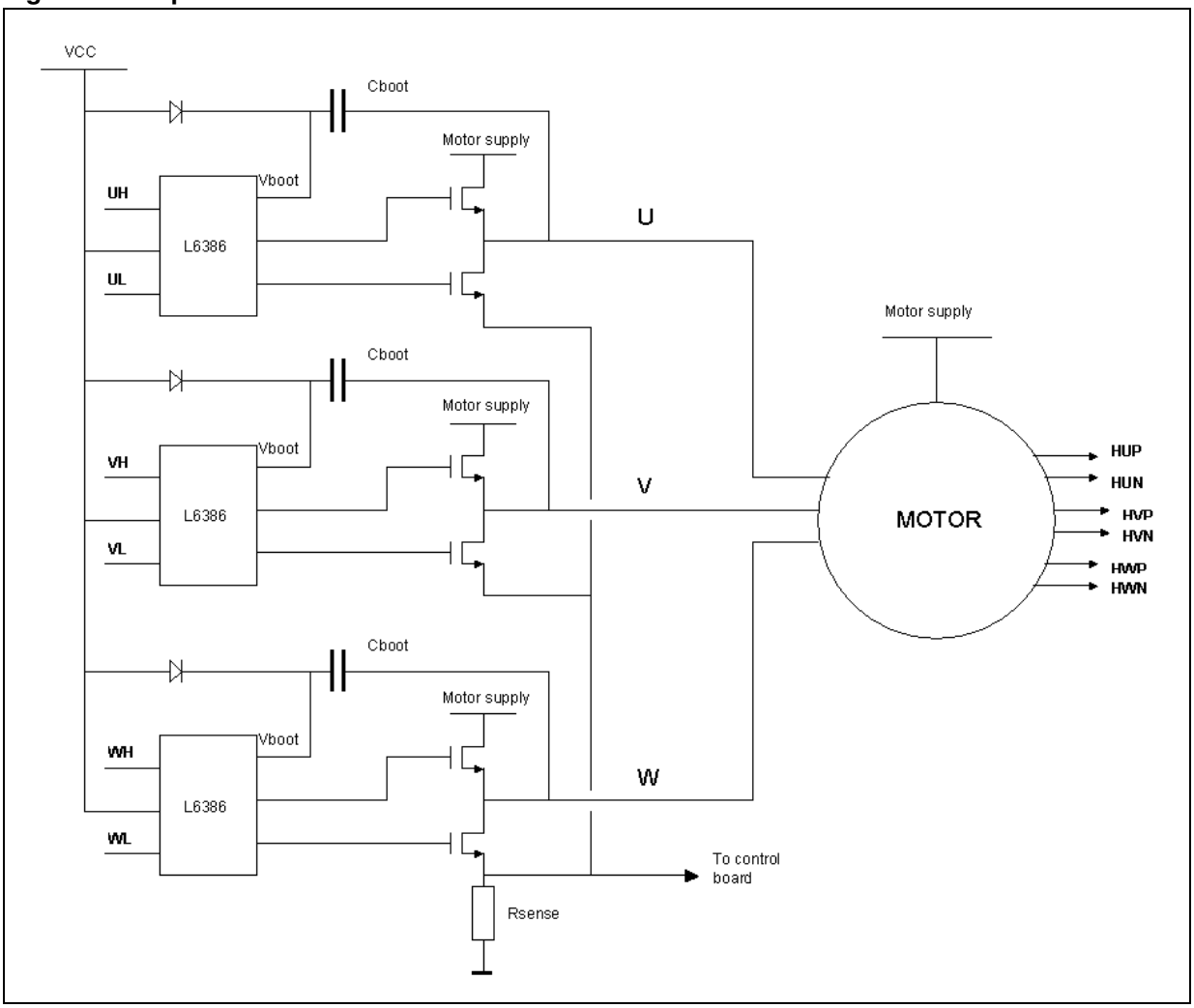


Figure 23. 3 phases motor control circuit



8 Input Output Pins Interface

In the following the simplified schematics of all the device pins.

Figure 24. Pins: TSD, OV, SDT, INTinN, INTinP

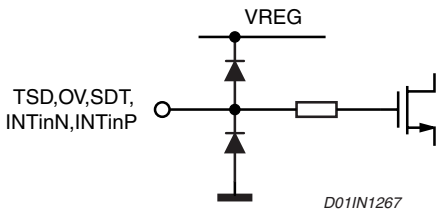


Figure 25. Pins: TO

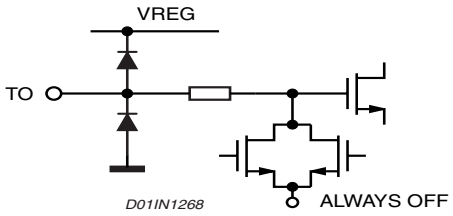


Figure 26. Pins: RF

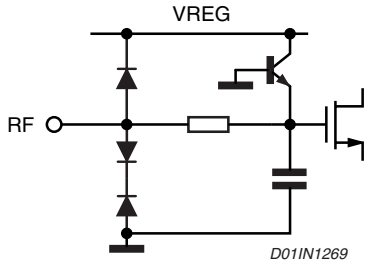


Figure 27. Pins: INTout

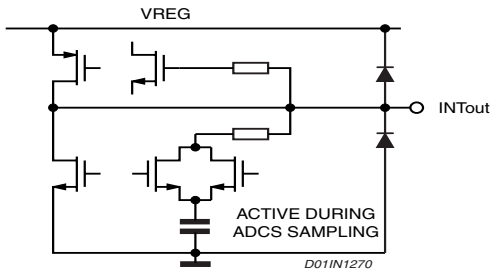


Figure 28. Pins: OSC

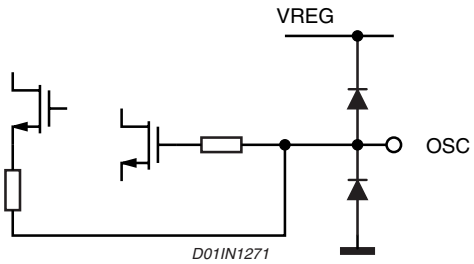


Figure 29. Pins: FG, DM, FAULT

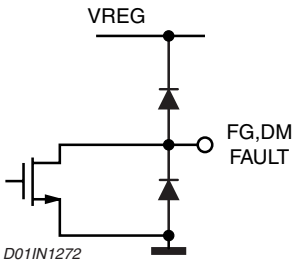


Figure 30. ESD clamping

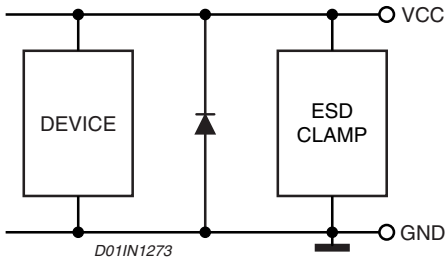


Figure 31. Recirculation diode

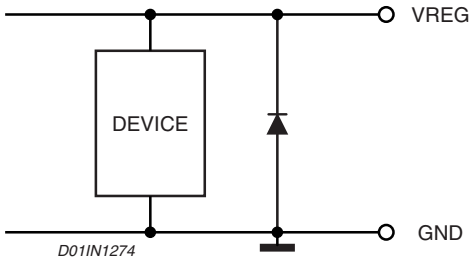


Figure 32. Pins: FR

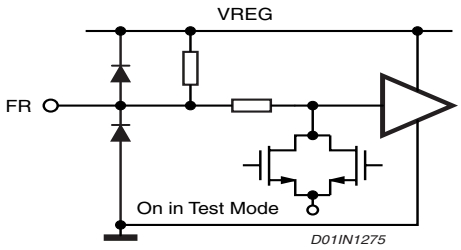


Figure 33. Pins: HWN, HWP

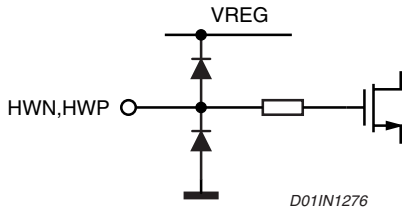


Figure 34. Pins: HUN, HUVP, HVN, HVP

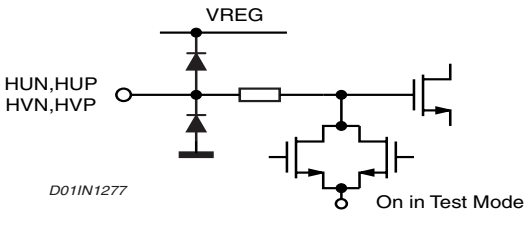
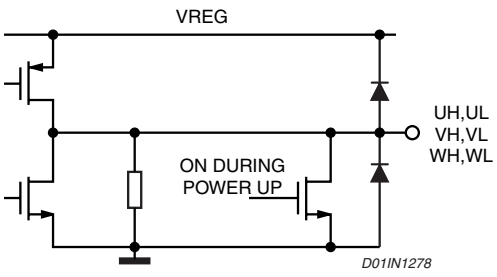


Figure 35. Pins: UH, UL, VH, VL, WH, WL



9 Package information

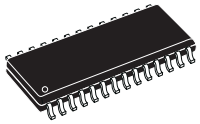
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: http://www.st.com.

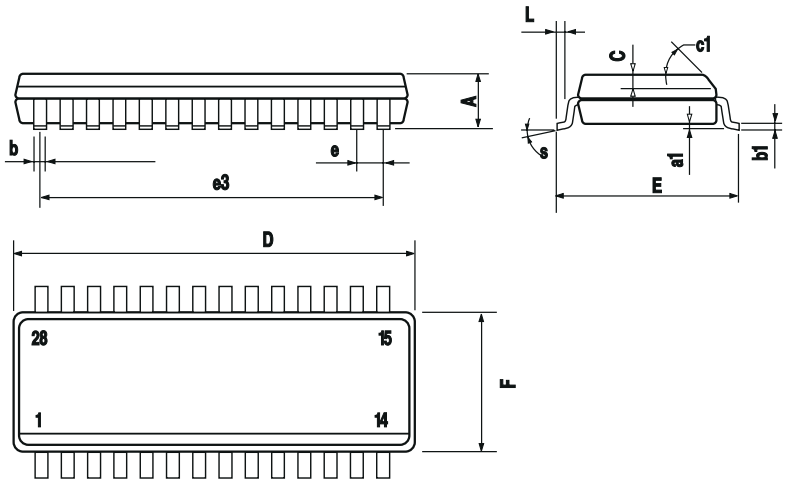
Figure 36. SO-28 Mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO-28



10 Revision history

Table 23. Document revision history

Date	Revision	Changes
20-Mar-2006	1	Initial release.

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