

# 1

## PRODUCT OVERVIEW

### SAM87RI PRODUCT FAMILY

Samsung's SAM87Ri family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A address/data bus architecture and a large number of bit-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations.

### KS86C4004/C4104 MICROCONTROLLER

The KS86C4004/C4104 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM87Ri CPU core. The KS86C4004/C4104 is a versatile microcontroller, with its A/D converter and a zero-crossing detection capability it can be used in a wide range of general purpose applications.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The KS86C4004/C4104 has 4-Kbytes of program memory on-chip (ROM) and 208-bytes of general purpose register area RAM.

Using the SAM87Ri design approach, the following peripherals were integrated with the SAM87Ri core:

- Four configurable I/O ports (KS86C4004: 22 pins, KS86C4104: 16 pins)
- Six interrupt sources with one vector and one interrupt level
- Two 8-bit timer/counter with various operating modes
- Analog to digital converter (KS86C4004: 8-bit, 8-channel, KS86C4104: 10-bit, 5-channel)
- One zero cross detection module

The KS86C4004/C4104 microcontroller is ideal for use in a wide range of electronic applications requiring simple timer/counter, PWM, ADC, ZCD and capture functions. KS86C4004 is available in a 30-pin SDIP and a 32-pin SOP package. KS86C4104 is available in a 24-pin SDIP and a 24-pin SOP package.

### OTP

The KS86P4004/P4104 is an OTP (one time programmable) version of the KS86C4004/C4104 microcontroller. The KS86P4004/P4104 has on-chip 4-Kbyte one-time programmable EEPROM instead of masked ROM. The KS86P4004/P4104 is fully compatible with the KS86C4004/C4104, in function, in D.C. electrical characteristics and in pin configuration.

## FEATURES

### CPU

- SAM87Ri CPU core

### Memory

- 4-Kbyte internal program memory (ROM)
- 208-byte general purpose register area (RAM)

### Instruction Set

- 41 instructions
- IDLE and STOP instructions added for power-down modes.

### Instruction Execution Time

- 600 ns at 10 MHz  $f_{OSC}$  (minimum)

### Interrupts

- 6 interrupt sources with one vector and one level interrupt structure

### Oscillation Frequency

- 1 MHz to 10 MHz external crystal oscillator
- Maximum 10 MHz CPU clock
- 4 MHz RC oscillator

### General I/O

- Four I/O ports (22 pins for KS86C4004, 16 pins for KS86C4104)
- Bit programmable ports

### A/D Converter

- Eight analog input pins
- 8-bit conversion resolution (KS86C4004)
- 10-bit conversion resolution (KS86C4104)

### Timer/Counter

- One 8-bit basic timer for watchdog function
- One 8-bit timer/counter with three operating modes (10-bit PWM 1ch)
- One 8-bit timer/counter for the zero-crossing detection circuit

### Zero-Crossing Detection Circuit

- Zero-crossing detection circuit that generates a digital signal in synchronism with an AC signal input

### Buzzer Frequency Range

- 200 Hz to 20 kHz signal can be generated

### Operating Temperature Range

- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### Operating Voltage Range

- 2.7 V to 5.5 V

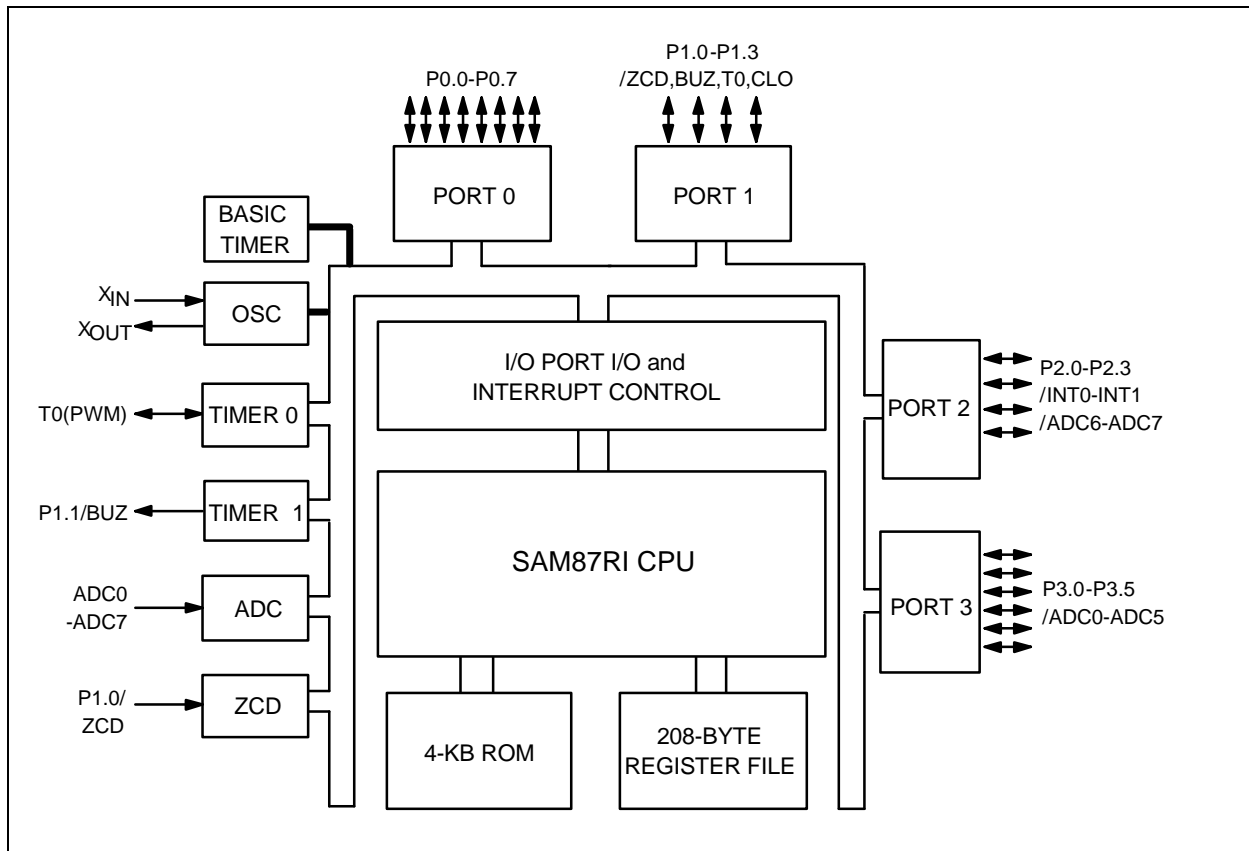
### OTP Interface Protocol Spec

- Serial OTP

### Package Types

- 30-pin SDIP, 32-pin SOP for KS86C4004/P4004
- 24-pin SDIP, 24-pin SOP for KS86C4104/P4104

**BLOCK DIAGRAM**



**Figure 1-1. Block Diagram**

**PIN ASSIGNMENTS**

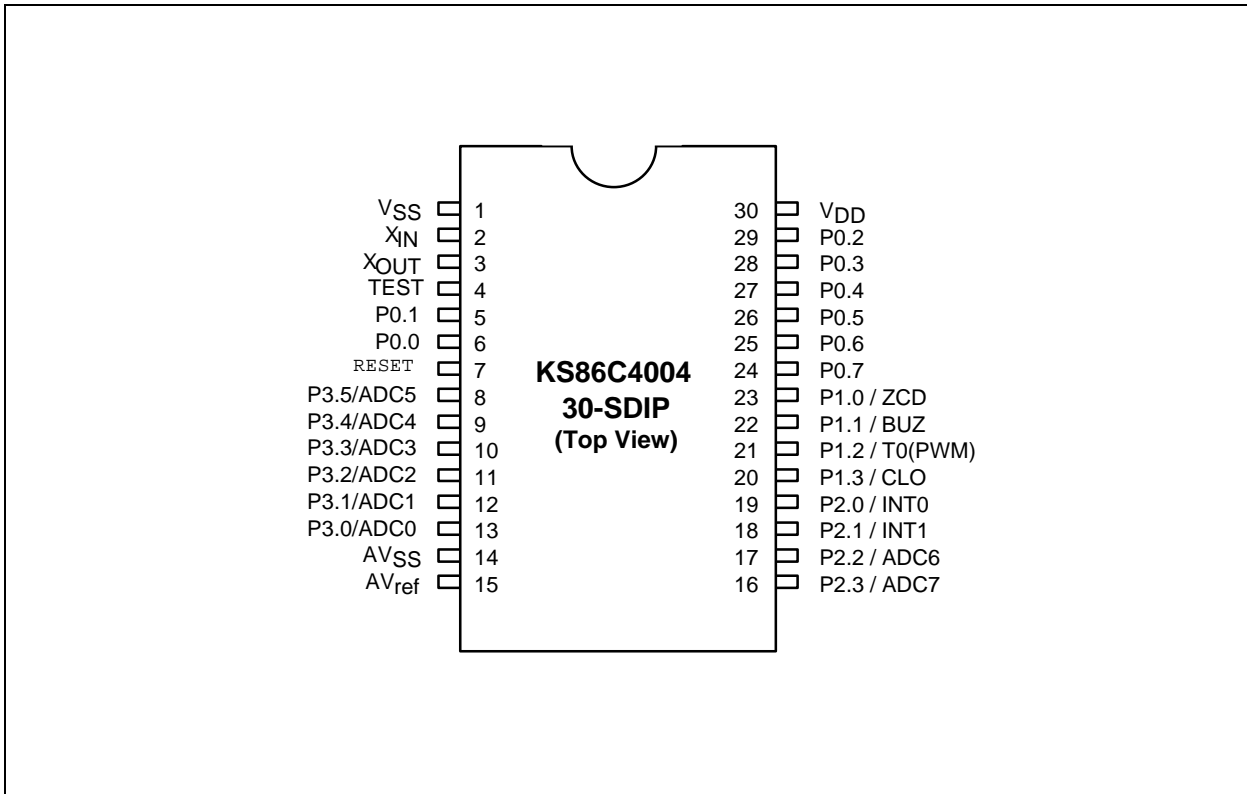


Figure 1-2. Pin Assignment Diagram (30-Pin SDIP Package)

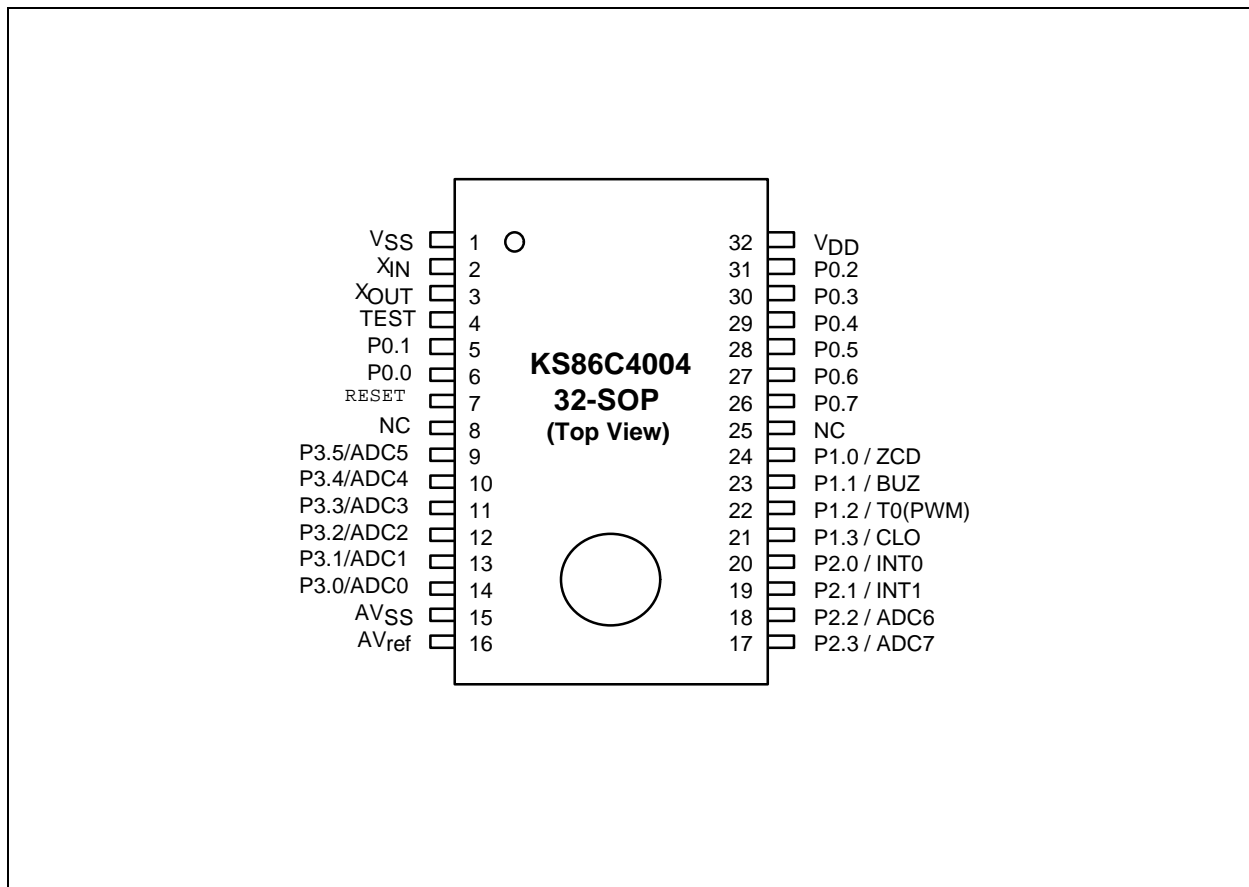


Figure 1-3. Pin Assignment Diagram (32-Pin SOP Package)

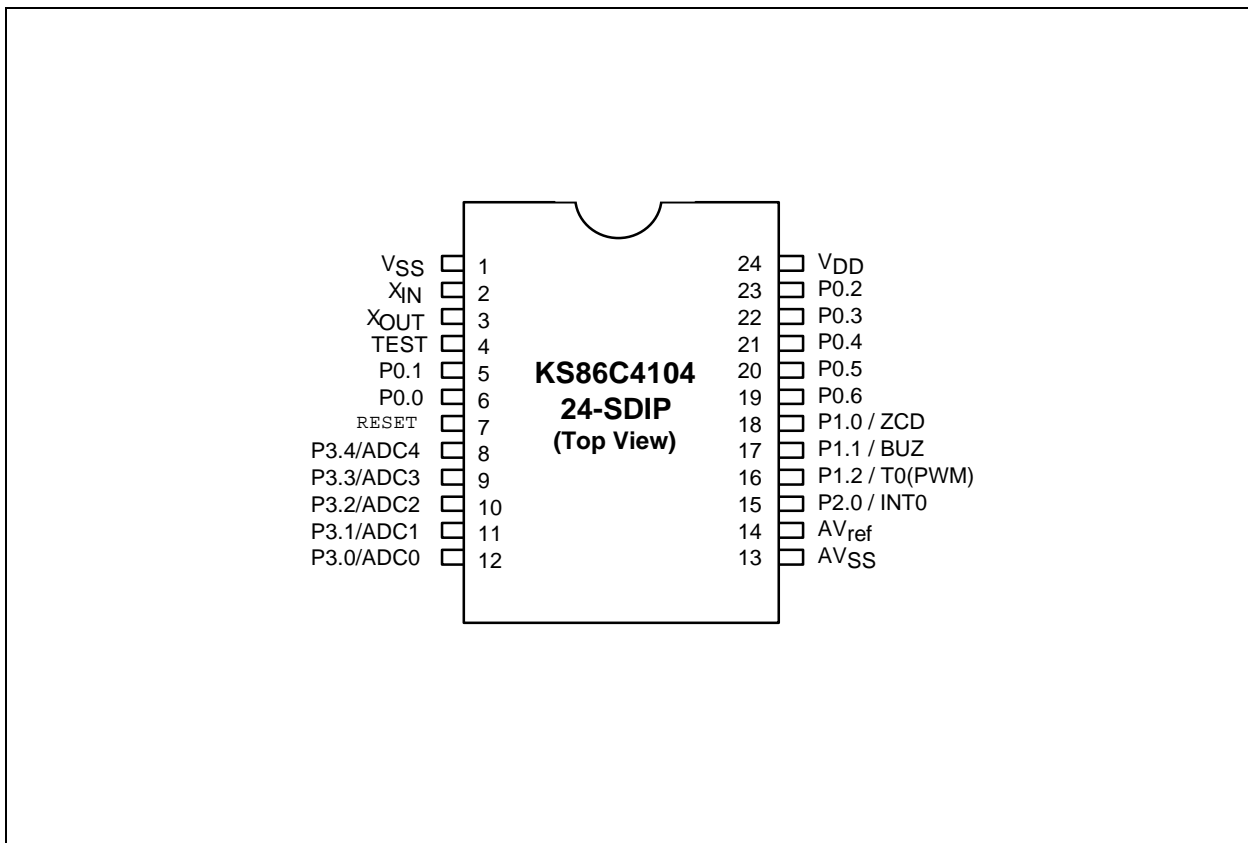


Figure 1-4. Pin Assignment Diagram (24-Pin SDIP Package)

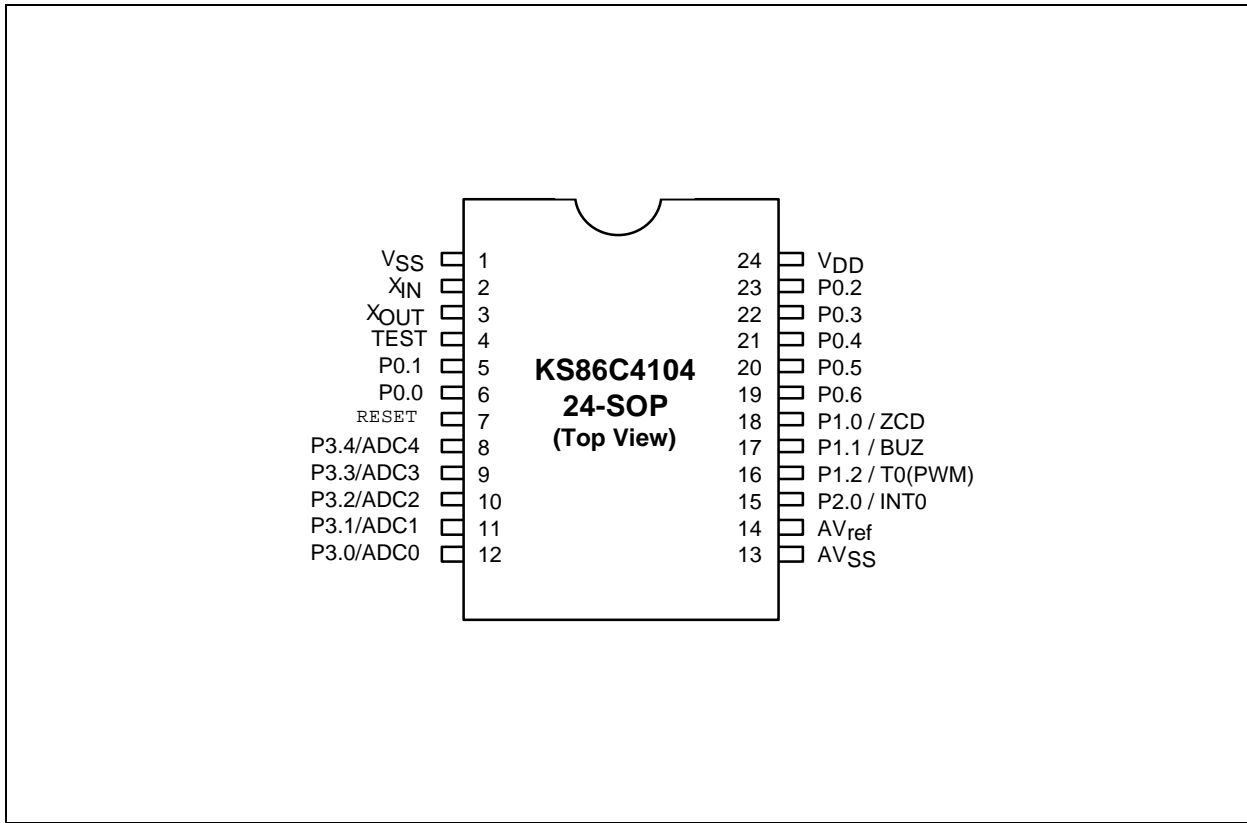


Figure 1-5. Pin Assignment Diagram (24-Pin SOP Package)

**PIN DESCRIPTIONS**

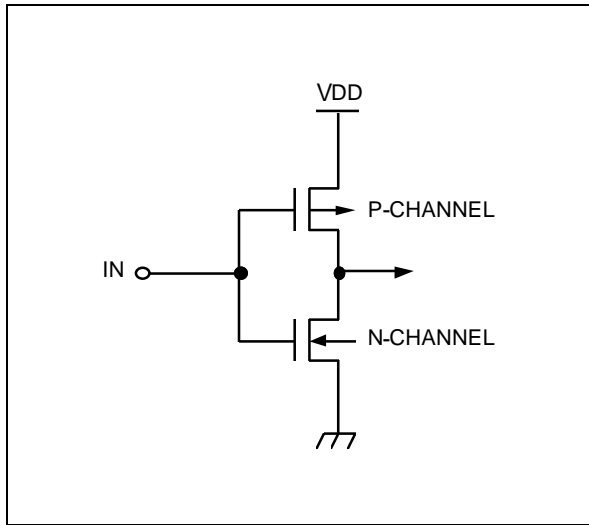
**Table 1-1. KS86C4004/C4104 Pin Descriptions**

Pin Names	Pin Type	Pin Description	Circuit Type	Share Pins
P0.0-P0.7	I/O	Bit-programmable I/O port for normal input or push-pull, open-drain output. Pull-up resistors are assignable by software.	E-2	
P1.0-P1.3	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are assignable by software. Port 1 pins can also be used as alternative functions.	F D D D	ZCD BUZ T0(PWM) CLO
P2.0-P2.3	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, open drain output. Pull up resistors are assignable by software. Port 2 can also be used as external interrupt, A/D input.	E E-1	INT0-INT1 ADC6-ADC7
P3.0-P3.5	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are assignable by software. Port 3 pins can also be used as A/D converter input.	F	ADC0-ADC5
X <sub>IN</sub> , X <sub>OUT</sub>	-	Crystal/ceramic, or RC oscillator signal for system clock.	-	-
INT0-INT1	I	External interrupt input.	E	P2.0-P2.1
RESET	I	System RESET signal input pin.	B	-
TEST	I	Test signal input pin (for factory use only: must be connected to V <sub>SS</sub> )	-	-
V <sub>DD</sub> , V <sub>SS</sub>	-	Voltage input pin and ground	-	-
A <sub>VREF</sub> , A <sub>VSS</sub>	-	A/D converter reference voltage input and ground	-	-
ZCD	I	Zero crossing detector input	F	P1.0
BUZ	O	200 Hz-20 kHz frequency output for buzzer sound	D	P1.1
T0	I/O	Timer 0 capture input or 10-bit PWM output	D	P1.2
CLO	O	System clock output port	D	P1.3
ADC0-ADC7	I	A/D converter input	F E-1	P3.0-P3.5 P2.2-P2.3

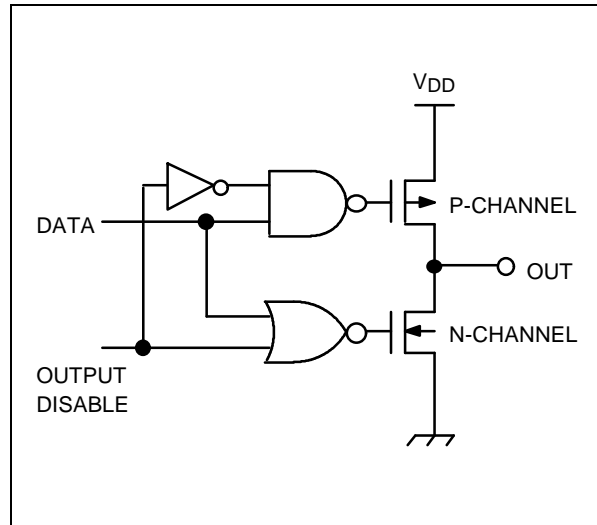
**NOTE:** Port 0.7, P1.3, P2.1-P2.3 and P3.5 is not available in KS86C4104/P4104 .



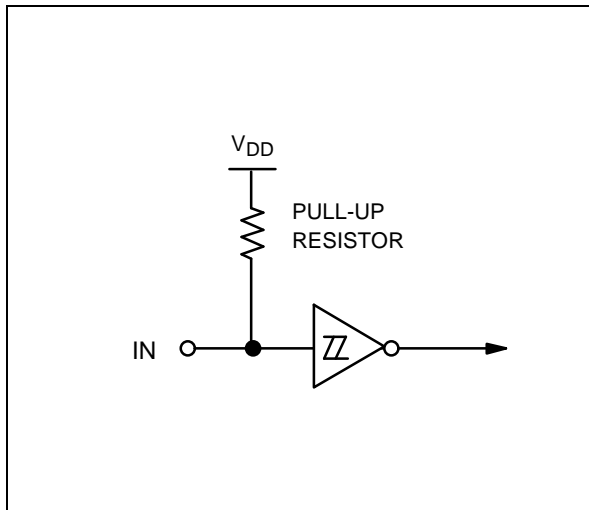
**PIN CIRCUITS**



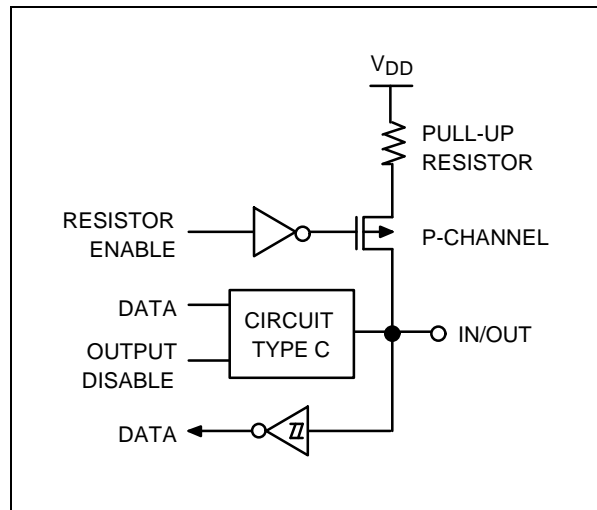
**Figure 1-6. Pin Circuit Type A**



**Figure 1-8. Pin Circuit Type C**



**Figure 1-7. Pin Circuit Type B**



**Figure 1-9. Pin Circuit Type D**

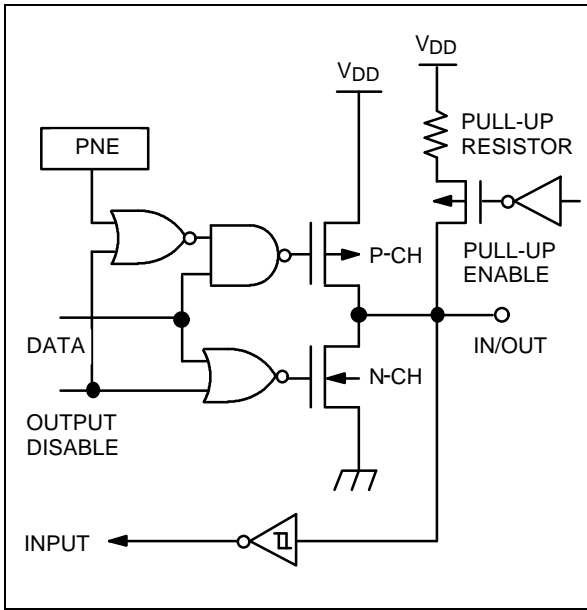


Figure 1-10. Pin Circuit Type E

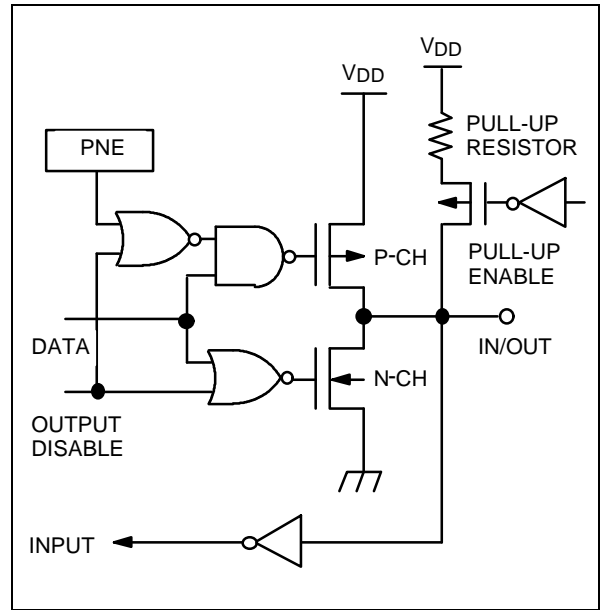


Figure 1-10. Pin Circuit Type E-2

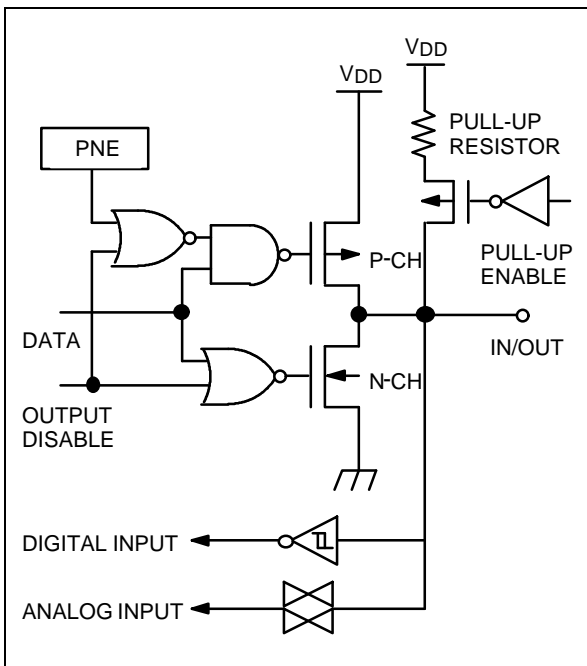


Figure 1-11. Pin Circuit Type E-1

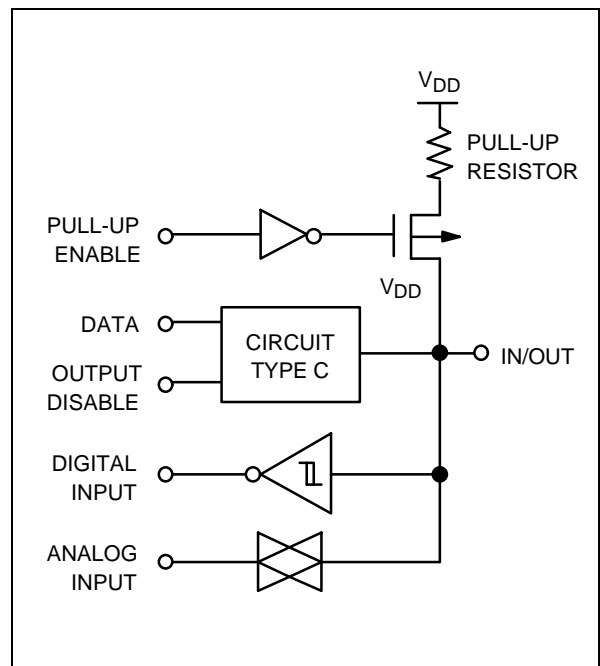


Figure 1-12. Pin Circuit Type F

# 13

## ELECTRICAL DATA

### OVERVIEW

In this section, the following KS86C4004/C4104 electrical characteristics are presented in tables and graphs:

- Absolute maximum ratings
- D.C. electrical characteristics
- A.C. electrical characteristics
- Oscillator characteristics
- Oscillation stabilization time
- Operating Voltage Range
- Schmitt trigger input characteristics
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by a RESET
- A/D converter electrical characteristics
- Zero-crossing detector
- Zero Crossing Waveform Diagram

Table 13-1. Absolute Maximum Ratings

 $(T_A = 25^\circ\text{C})$ 

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	$V_{DD}$	–	– 0.3 to + 6.5	V
Input voltage	$V_I$	All input ports	– 0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_O$	All output ports	– 0.3 to $V_{DD} + 0.3$	V
Output current high	$I_{OH}$	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current low	$I_{OL}$	One I/O pin active	+ 30	mA
		Total pin current for ports 1, 2, 3	+ 100	
		Total pin current for ports 0	+ 200	
Operating temperature	$T_A$	–	– 40 to + 85	$^\circ\text{C}$
Storage temperature	$T_{STG}$	–	– 65 to + 150	$^\circ\text{C}$

Table 13-2. DC Electrical Characteristics

 $(T_A = -40^\circ\text{C to } +85^\circ\text{C}, V_{DD} = 2.7\text{ V to } 5.5\text{ V})$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Input high voltage	$V_{IH1}$	Ports 1,2,3, and RESET	$V_{DD} = 2.7\text{ to } 5.5\text{ V}$	$0.8 V_{DD}$	–	$V_{DD}$	V
	$V_{IH2}$	Port 0		$0.7 V_{DD}$			
	$V_{IH3}$	$X_{IN}$ and $X_{OUT}$		$V_{DD} - 0.1$			
Input low voltage	$V_{IL1}$	Ports 1,2,3, and RESET	$V_{DD} = 2.7\text{ to } 5.5\text{ V}$	–	–	$0.2 V_{DD}$	V
	$V_{IL2}$	Port 0				$0.3 V_{DD}$	
	$V_{IL3}$	$X_{IN}$ and $X_{OUT}$				0.1	
Output high voltage	$V_{OH}$	$I_{OH} = -1\text{ mA}$ ports 0, 1, 2, 3	$V_{DD} = 4.5\text{ to } 5.5\text{ V}$	$V_{DD} - 1.0$	–	–	V
Output low voltage	$V_{OL1}$	$I_{OL} = 15\text{ mA}$ port 0	$V_{DD} = 4.5\text{ to } 5.5\text{ V}$	–	0.4	2.0	V
	$V_{OL2}$	$I_{OL} = 4\text{ mA}$ port 1,2,3	$V_{DD} = 4.5\text{ to } 5.5\text{ V}$		0.4	2.0	

Table 13-2. DC Electrical Characteristics (Continued)

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit		
Input high leakage current	I <sub>LIH1</sub>	All inputs except I <sub>LIH2</sub>	V <sub>IN</sub> = V <sub>DD</sub>	-	-	1	μA		
	I <sub>LIH2</sub>	X <sub>IN</sub> , X <sub>OUT</sub>	V <sub>IN</sub> = V <sub>DD</sub>			20			
Input low leakage current	I <sub>LIL1</sub>	All inputs except I <sub>LIL2</sub> and RESET	V <sub>IN</sub> = 0 V	-	-	-1	μA		
	I <sub>LIL2</sub>	X <sub>IN</sub> , X <sub>OUT</sub>	V <sub>IN</sub> = 0 V			-20			
Output high leakage current	I <sub>LOH</sub>	All outputs	V <sub>OUT</sub> = V <sub>DD</sub>	-	-	2	μA		
Output low leakage current	I <sub>LOL</sub>	All outputs	V <sub>OUT</sub> = 0 V	-	-	-2	μA		
Pull-up resistors	R <sub>P</sub>	V <sub>IN</sub> = 0 V Ports 0-3 and RESET	V <sub>DD</sub> = 5 V	30	47	70	kΩ		
			V <sub>DD</sub> = 3 V	30	280	350			
Supply current	I <sub>DD1</sub>	Run mode 10 MHz CPU clock	V <sub>DD</sub> = 5 V ± 10%	-	7.5	15	mA		
		8 MHz CPU clock	V <sub>DD</sub> = 3 V ± 10%			3		6	
	I <sub>DD2</sub>	Idle mode 10 MHz CPU clock	V <sub>DD</sub> = 5 V ± 10%			2		5	
		8 MHz CPU clock	V <sub>DD</sub> = 3 V ± 10%			0.7		2.5	
	I <sub>DD3</sub>	Stop mode	V <sub>DD</sub> = 5 V ± 10%			0.1		5	μA
			V <sub>DD</sub> = 3 V ± 10%						

**NOTE:** D.C. electrical values for Supply current (I<sub>DD1</sub> to I<sub>DD3</sub>) do not include current drawn through internal pull-up resistors, output port drive current, ZCD and ADC.

Table 13-3. AC Electrical Characteristics

(T<sub>A</sub> = -20°C to +85°C, V<sub>DD</sub> = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width	t <sub>INTH</sub> , t <sub>INTL</sub>	Port 2 V <sub>DD</sub> = 5V ± 10%	-	200	-	ns
RESET input low width ZCD noise filter	t <sub>RSL</sub> -	Input V <sub>DD</sub> = 5V ± 10%	-	1	-	μs

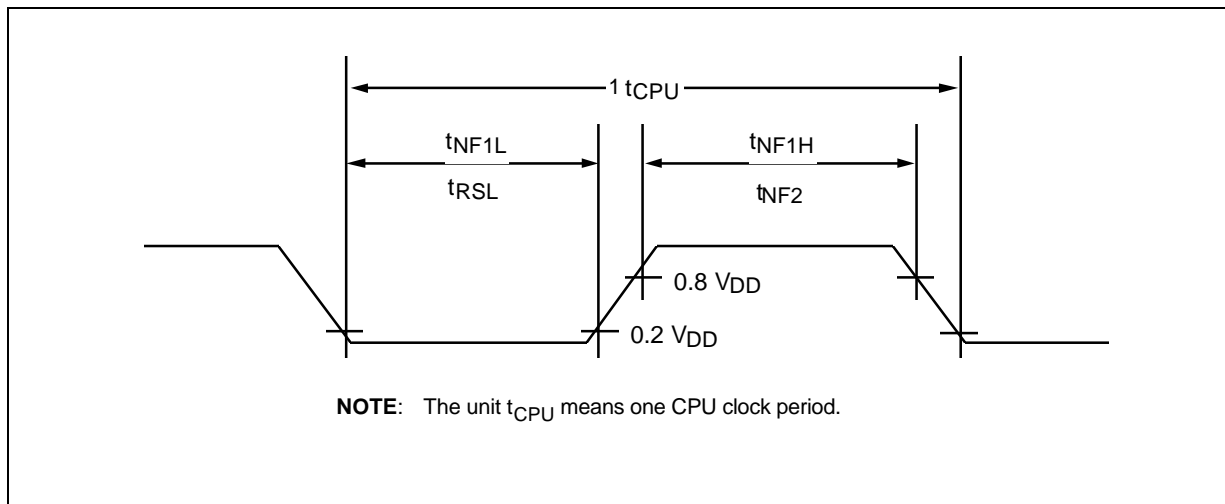


Figure 13-1. Input Timing Measurement Points

Table 13-4. Oscillator Characteristics

(T<sub>A</sub> = -40°C to +85°C)

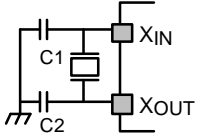
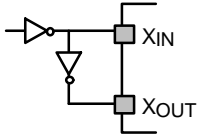
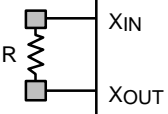
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Main crystal or ceramic		V <sub>DD</sub> = 4.5 to 5.5 V V <sub>DD</sub> = 2.7 to 4.5 V	1 1	– –	10 8	MHz
External clock		V <sub>DD</sub> = 4.5 to 5.5 V V <sub>DD</sub> = 2.7 to 4.5 V	1 1	– –	10 8	
RC oscillator		V <sub>DD</sub> = 4.75 to 5.25 V R = 8.2K	–	4 (P1.3/ CLO)	–	

Table 13-5. Oscillation Stabilization Time

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 2.7 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main crystal	f <sub>OSC</sub> > 1.0 MHz	–	–	20	ms
Main ceramic	Oscillation stabilization occurs when V <sub>DD</sub> is equal to the minimum oscillator voltage range.	–	–	10	
External clock (main system)	X <sub>IN</sub> input high and low width (t <sub>XH</sub> , t <sub>XL</sub> )	25	–	500	ns
Oscillator stabilization wait time	t <sub>WAIT</sub> when released by a reset <sup>(1)</sup>	–	2 <sup>16</sup> /f <sub>OSC</sub>	–	ms
	t <sub>WAIT</sub> when released by an interrupt <sup>(2)</sup>	–	–	–	

**NOTES:**1. f<sub>OSC</sub> is the oscillator frequency.2. The duration of the oscillator stabilization wait time, t<sub>WAIT</sub>, when it is released by an interrupt is determined by the settings in the basic timer control register, BTCON.

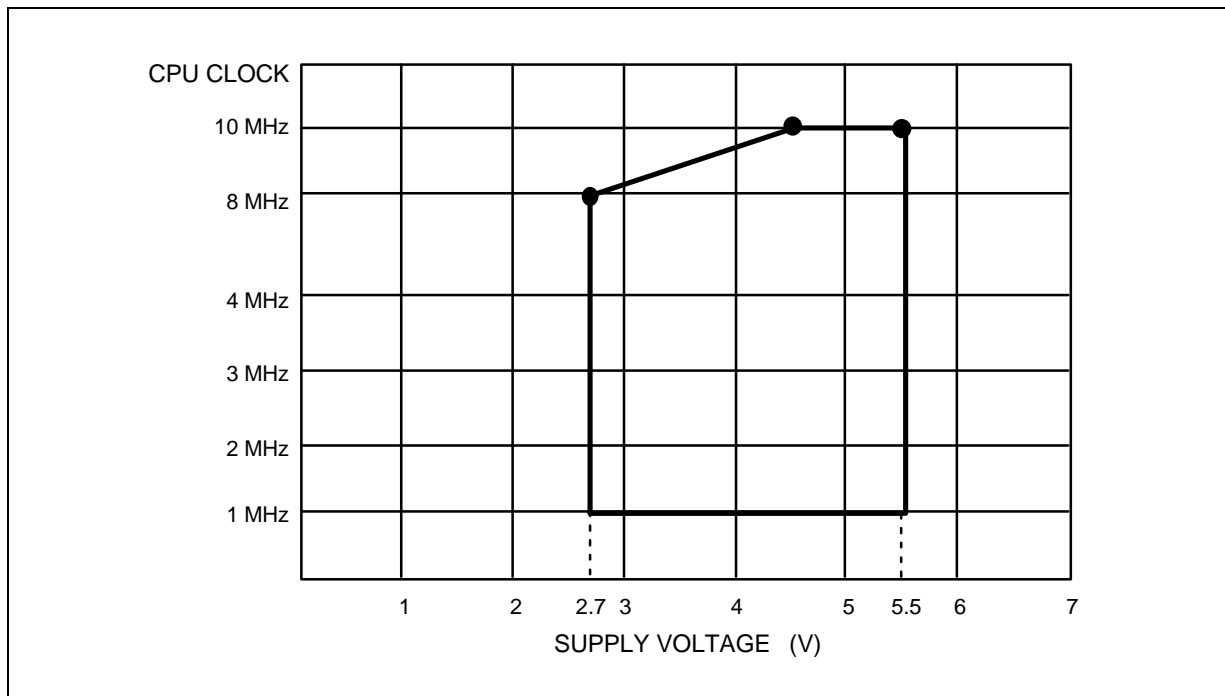


Figure 13-2. Operating Voltage Range

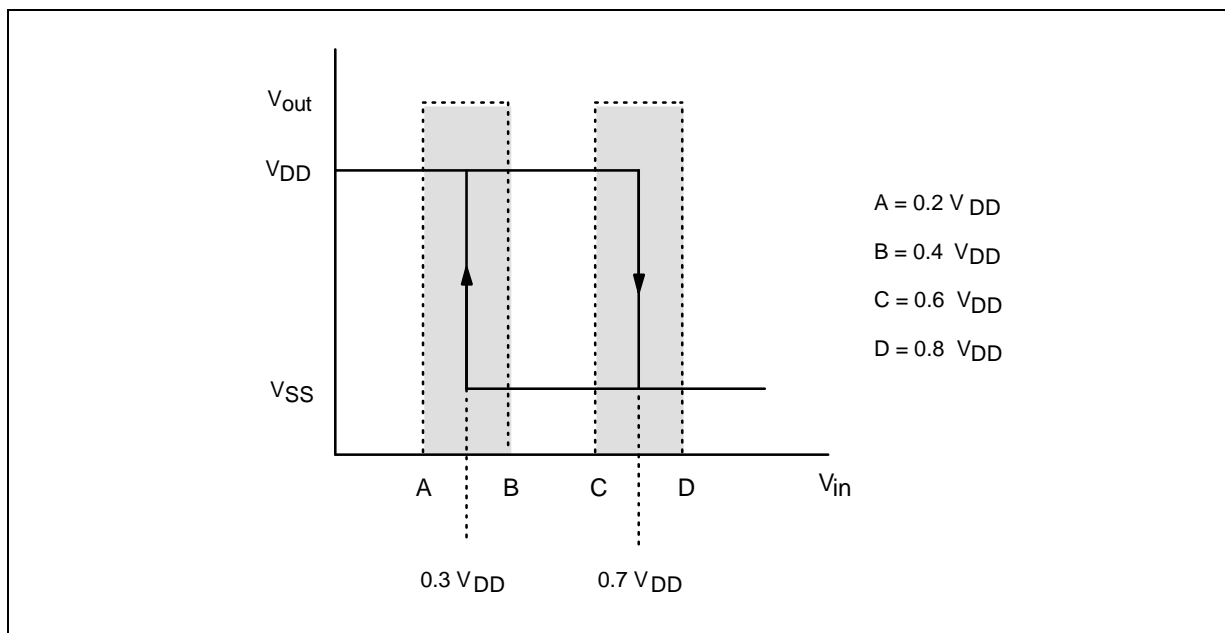


Figure 13-3. Schmitt Trigger Input Characteristics Diagram

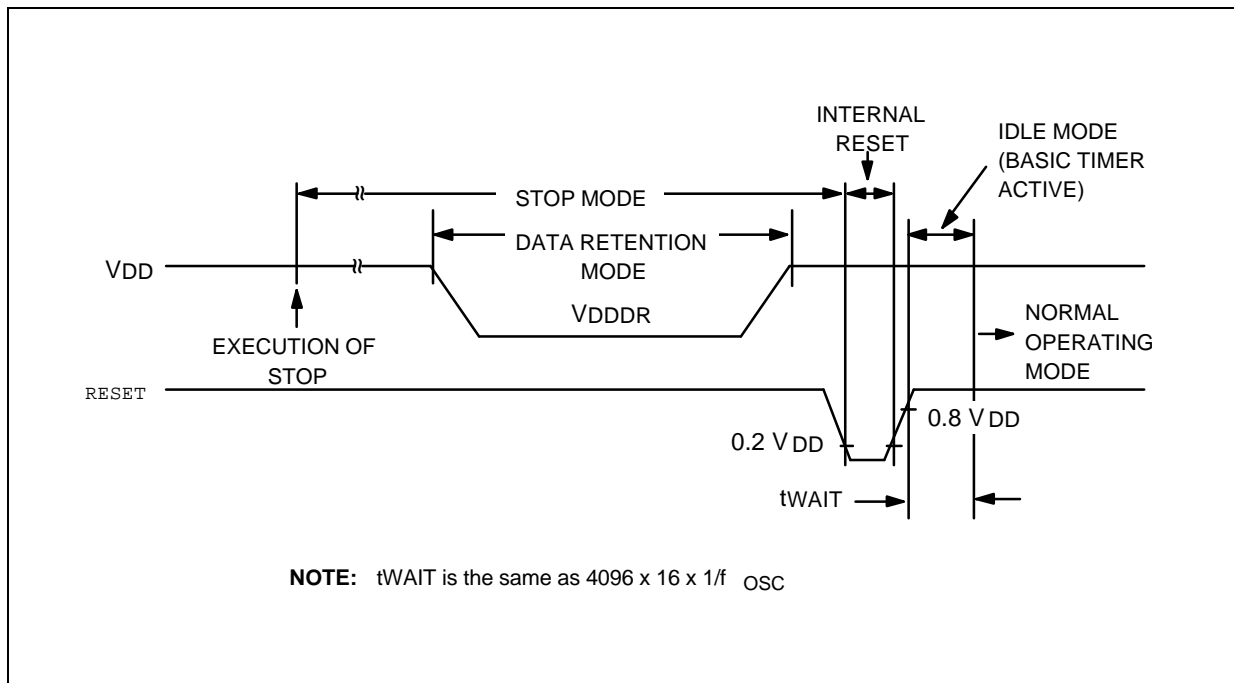


**Table 13-6. Data Retention Supply Voltage in Stop Mode**

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{ V}$  to  $5.5\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	$V_{DDDR}$	Stop mode	2.0	–	5.5	V
Data retention supply current	$I_{DDDR}$	Stop mode; $V_{DDDR} = 2.0\text{ V}$	–	0.1	5	$\mu\text{A}$

**NOTE:** Supply current does not include current drawn through internal pull-up resistors or external output current loads.



**Figure 13-4. Stop Mode Release Timing When Initiated by a RESET**

Table 13-7. A/D Converter Electrical Characteristics (KS86C4004)

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

KS86C4004: 8-bit ADC

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total accuracy		V <sub>DD</sub> = 5.12 V	–	–	± 2	LSB
Integral linearity error	ILE	CPU clock = 10 MHz AV <sub>REF</sub> = 5.12 V		–	± 1.5	
Differential linearity error	DLE	AV <sub>SS</sub> = 0 V		–	± 1	
Offset error of top	EOT			– 1	± 2	
Offset error of bottom	EOB			– 1	± 2	
Conversion time <sup>(1)</sup>	t <sub>CON</sub>	f <sub>cpu</sub> = 10 MHz	5	–	–	μs
Analog input voltage	V <sub>IAN</sub>	–	AV <sub>SS</sub>	–	AV <sub>REF</sub>	V
Analog input impedance	R <sub>AN</sub>	–	2	–	–	MΩ
ADC reference voltage	AV <sub>REF</sub>	–	2.5	–	V <sub>DD</sub>	V
ADC reference ground	AV <sub>SS</sub>	–	V <sub>SS</sub>	–	V <sub>SS</sub> + 0.3	V
Analog input current	I <sub>ADIN</sub>	AV <sub>REF</sub> = V <sub>DD</sub> = 5 V conversion time = 5 μs	–	–	10	μA
ADC block current <sup>(2)</sup>	I <sub>ADC</sub>	AV <sub>REF</sub> = V <sub>DD</sub> = 5 V conversion time = 5 μs	–	1	3	mA
		AV <sub>REF</sub> = V <sub>DD</sub> = 3 V conversion time = 5 μs		0.5	1.5	
		AV <sub>REF</sub> = V <sub>DD</sub> = 5 V Power down mode	–	100	500	nA

**NOTES:**

1. "Conversion time" is the time required from the moment a conversion operation starts until it ends.
2. I<sub>ADC</sub> is operating current during A/D conversion.

Table 13-8. A/D Converter Electrical Characteristics (KS86C4104)

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

KS86C4104: 10-bit ADC

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution			-	10	-	bit
Total accuracy		V <sub>DD</sub> = 5.12 V	-	-	± 3	LSB
Integral linearity error	ILE	CPU clock = 10 MHz AV <sub>REF</sub> = 5.12 V		-	± 2	
Differential linearity error	DLE	AV <sub>SS</sub> = 0 V		-	± 1	
Offset error of top	EOT			± 1	± 3	
Offset error of bottom	EOB			± 0.5	± 2	
Conversion time (1)	t <sub>CON</sub>	10-bit conversion 50 x 4/ f <sub>OSC</sub> (3)	20	-	-	μs
Analog input voltage	V <sub>IAN</sub>	-	AV <sub>SS</sub>	-	AV <sub>REF</sub>	V
Analog input impedance	R <sub>AN</sub>	-	2	-	-	MΩ
Analog reference voltage	AV <sub>REF</sub>	-	2.5	-	V <sub>DD</sub>	V
Analog ground	AV <sub>SS</sub>	-	V <sub>SS</sub>	-	V <sub>SS</sub> + 0.3	V
Analog input current	I <sub>ADIN</sub>	AV <sub>REF</sub> = V <sub>DD</sub> = 5 V conversion time = 20 μs	-	-	10	μA
Analog block current (2)	I <sub>ADC</sub>	AV <sub>REF</sub> = V <sub>DD</sub> = 5 V conversion time = 20 μs		1	3	mA
		AV <sub>REF</sub> = V <sub>DD</sub> = 3 V conversion time = 20 μs		0.5	1.5	mA
		AV <sub>REF</sub> = V <sub>DD</sub> = 5 V when power down mode		100	500	nA

**NOTES:**

- "Conversion time" is the time required from the moment a conversion operation starts until it ends.
- I<sub>ADC</sub> is operating current during A/D conversion.
- f<sub>OSC</sub> is the main oscillator clock.

Table 13-9. Zero Crossing Detector

(T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = 4.5 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Zero-crossing detection input voltage	V <sub>ZC</sub>	AC connection c = 0.1 μF	1.0	–	3.0	Vp-p
Zero-crossing detection accuracy	V <sub>AZC</sub>	f <sub>ZC</sub> = 60 Hz (sine wave) V <sub>DD</sub> = 5 V f <sub>OSC</sub> = 10 MHz	–	–	± 150	mV
Zero-crossing detection input frequency	f <sub>ZC</sub>	–	40	–	200	Hz

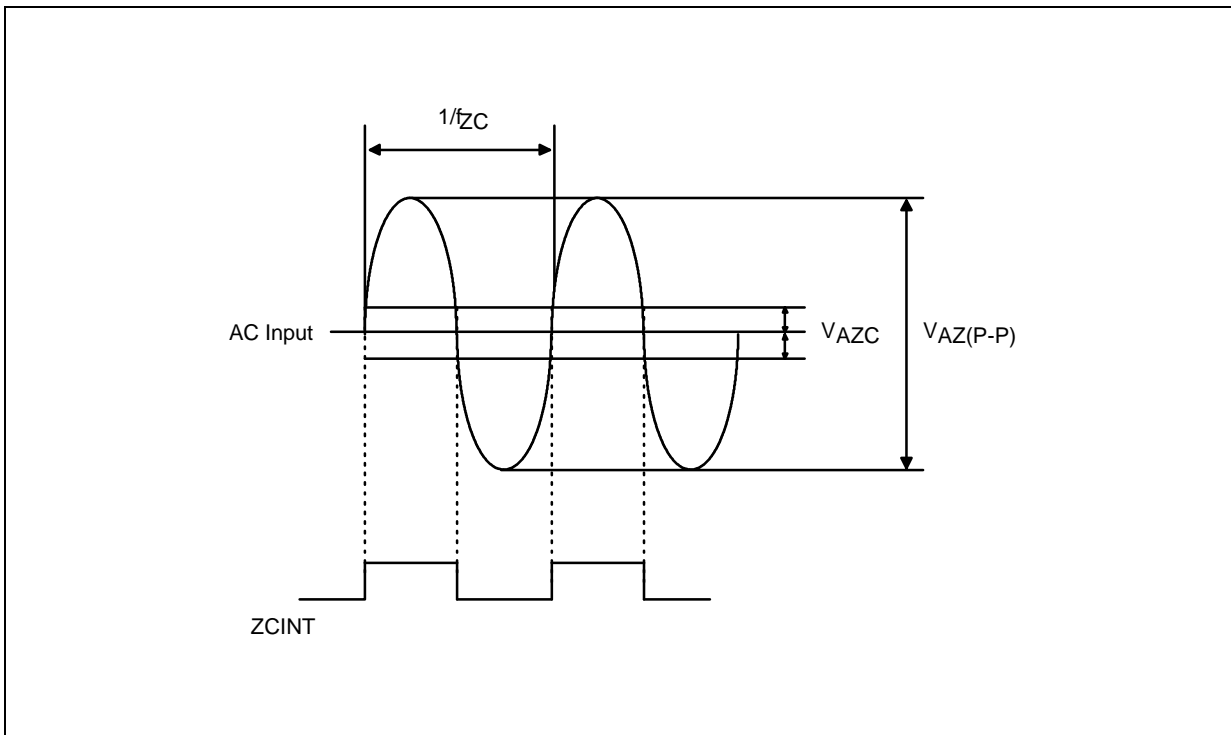


Figure 13-5. Zero Crossing Waveform Diagram

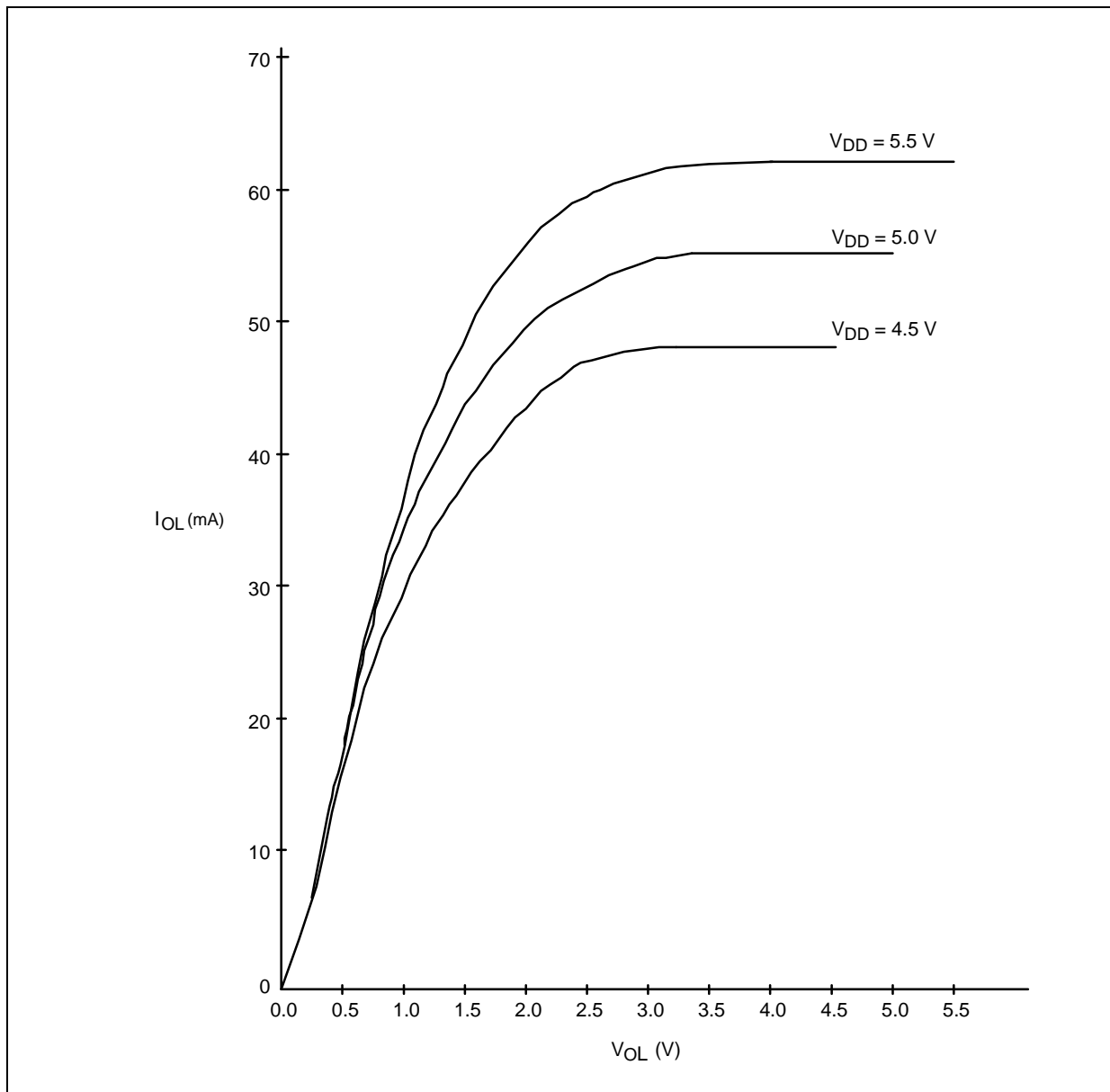


Figure 13-6.  $I_{OL}$  vs.  $V_{OL}$  (P0,  $T_A = 25\text{ }^\circ\text{C}$ )

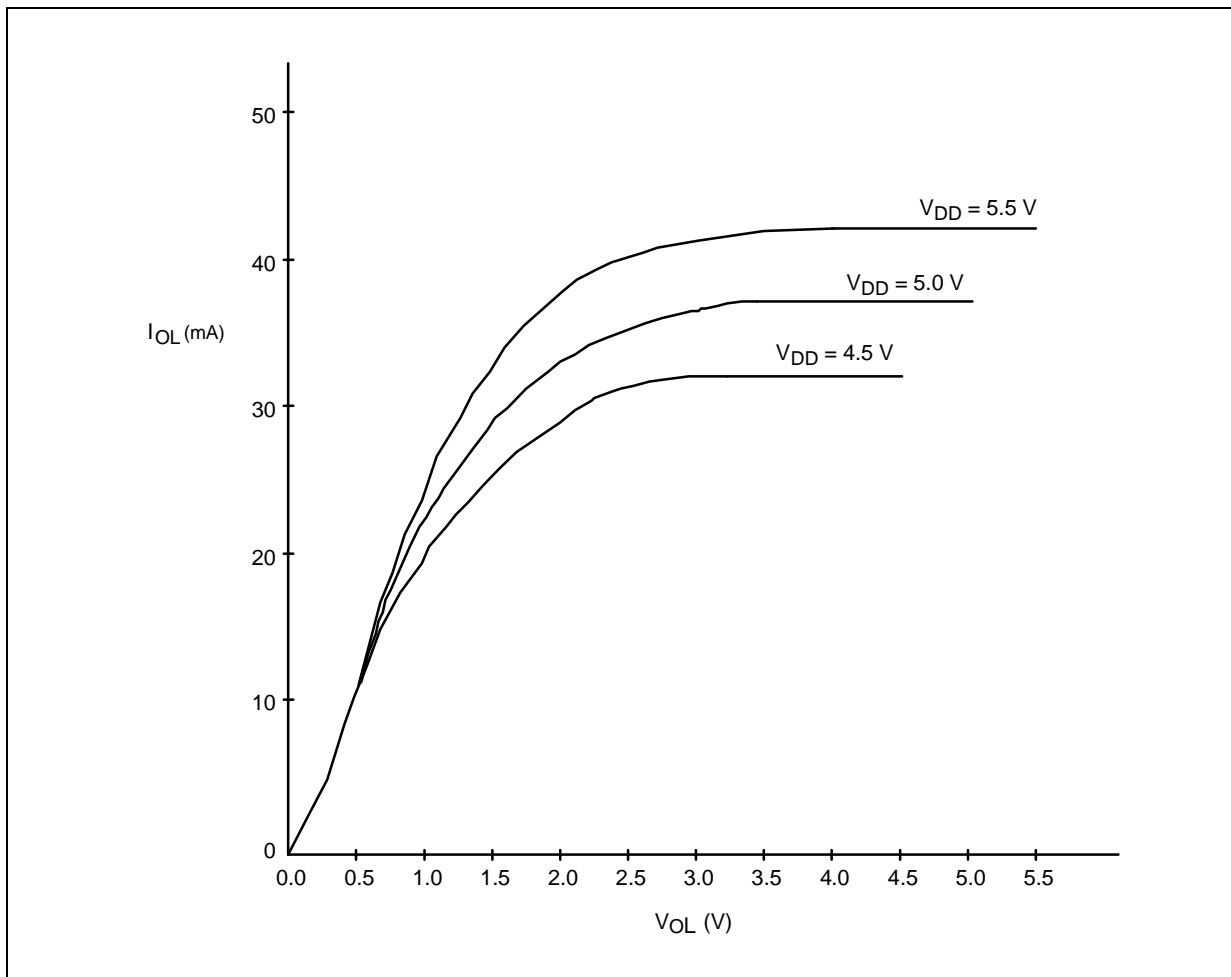


Figure 13-7.  $I_{OL}$  vs.  $V_{OL}$  (P1-P3,  $T_A = 25$  °C)

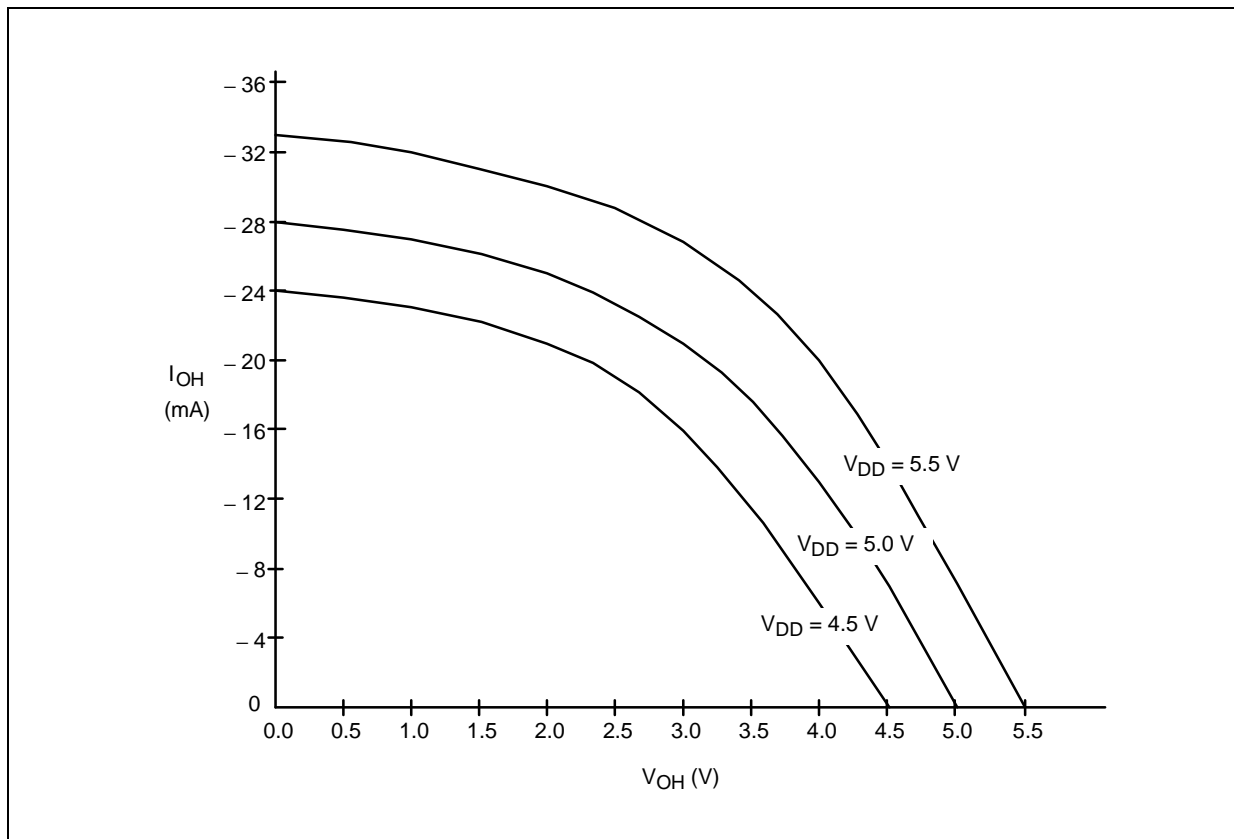


Figure 13-8. I<sub>OH</sub> vs. V<sub>OH</sub> (P0, TA = 25 °C)

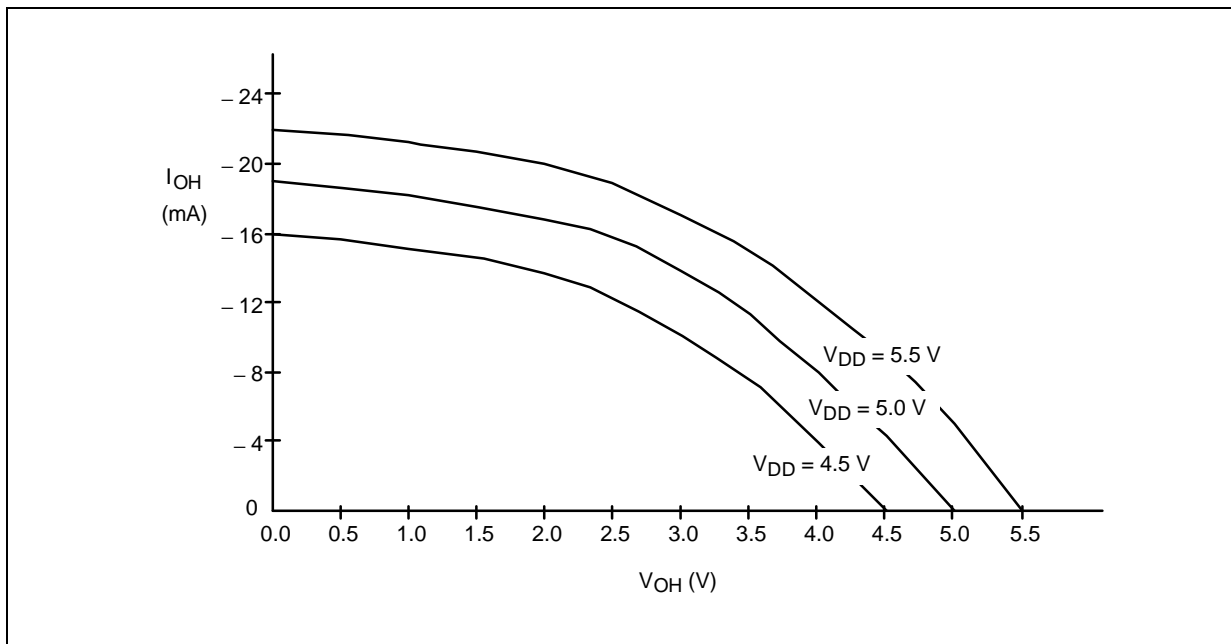


Figure 13-9.  $I_{OH}$  vs.  $V_{OH}$  (P1-P3,  $T_A = 25^\circ\text{C}$ )



# 14 MECHANICAL DATA

## OVERVIEW

The KS86C4004/C4104 is available in a 30-pin SDIP package (Samsung: 30-SDIP-400) and a 32-pin SOP package (32-SOP-450A), a 24-pin SDIP package (24-SDIP-300) and a 24-pin SOP package (24-SOP-375). Package dimensions are shown in Figures 14-1, 14-2, 14-3, and 14-4.

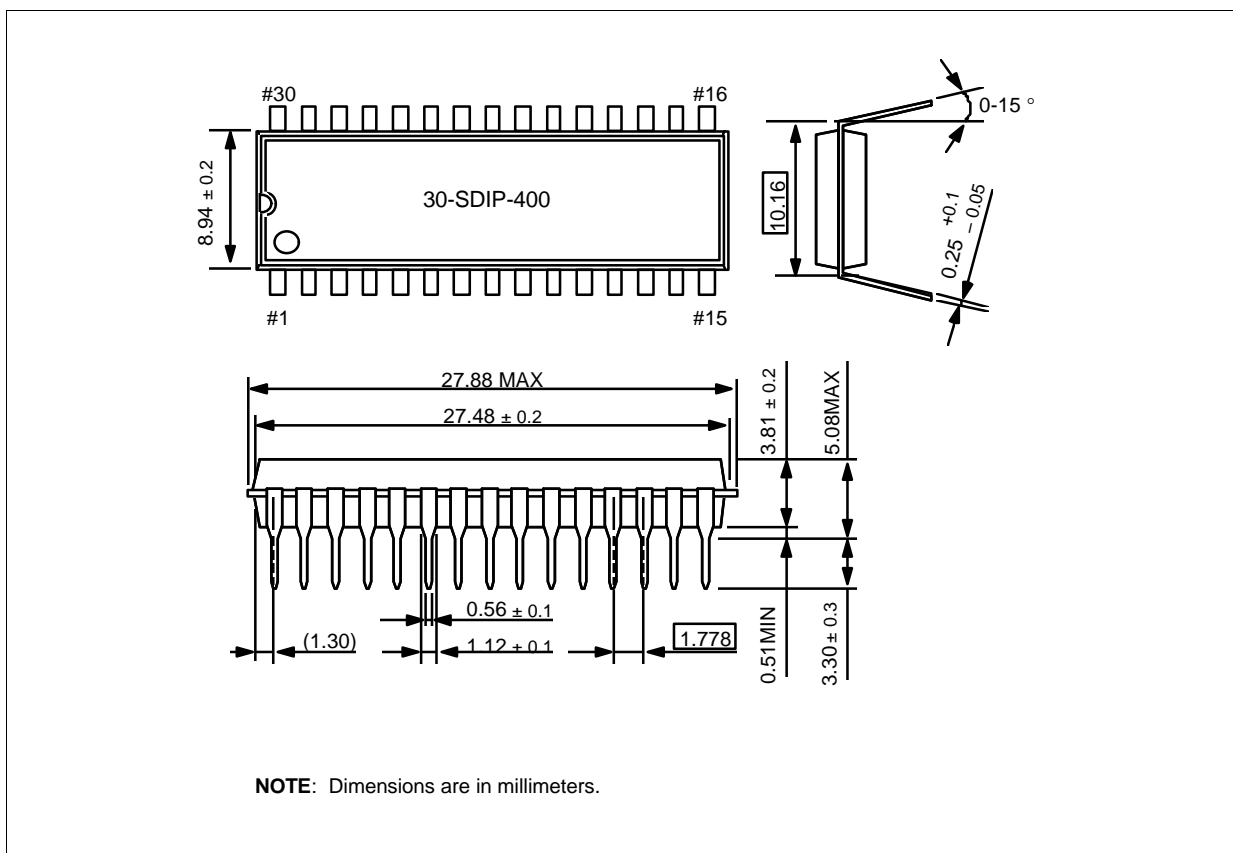


Figure 14-1. 30-Pin SDIP Package Dimensions

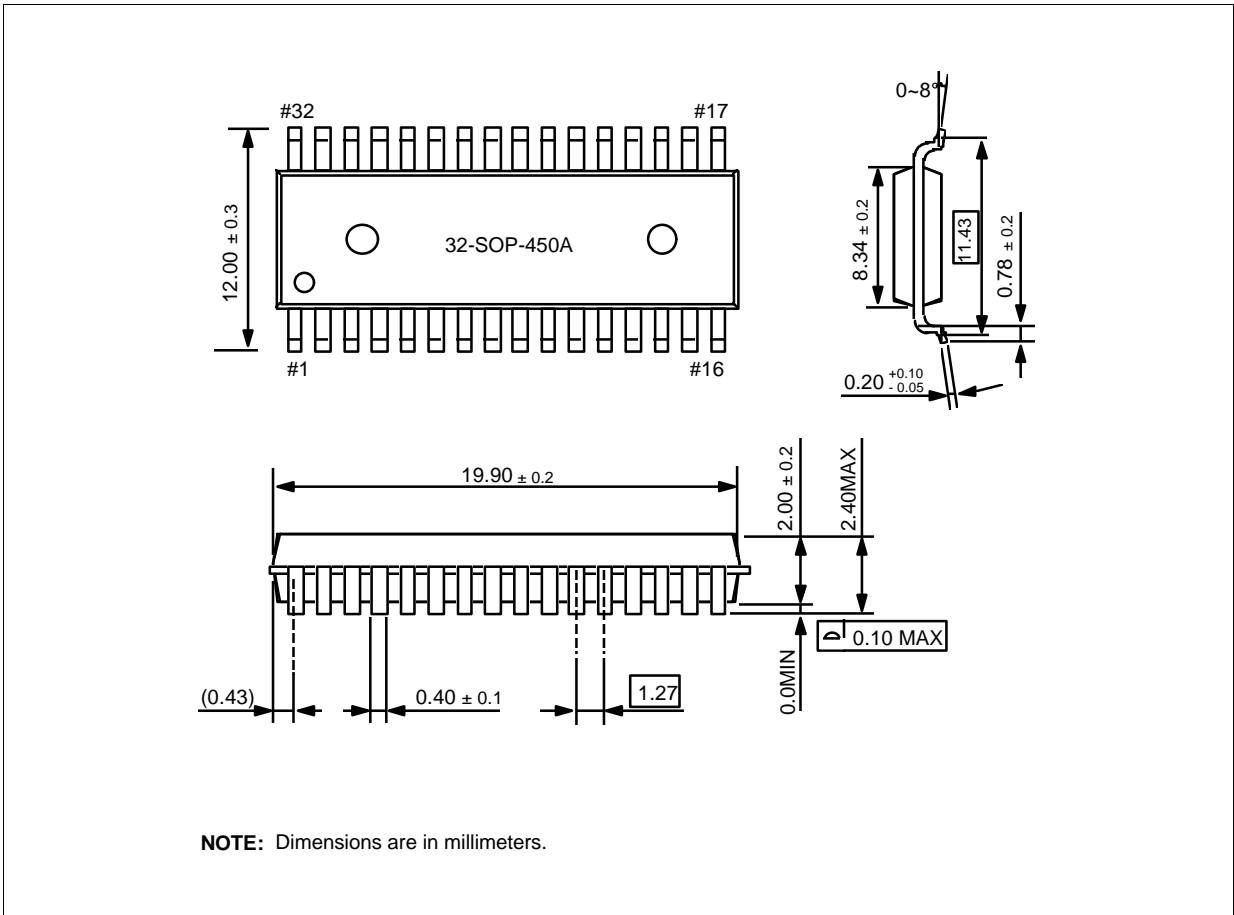


Figure 14-2. 32-SOP-450A Package Dimensions

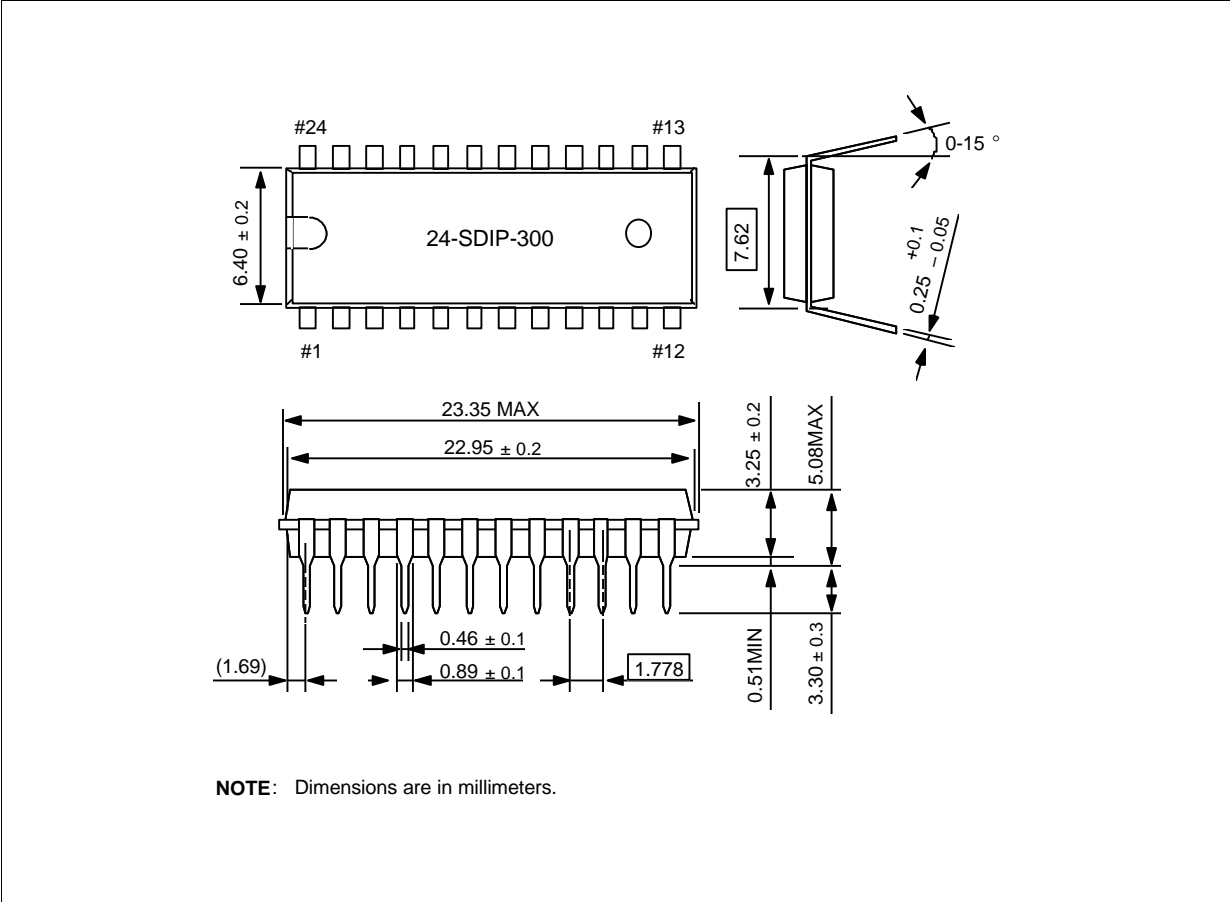


Figure 14-3. 24-SDIP-300 Package Dimensions

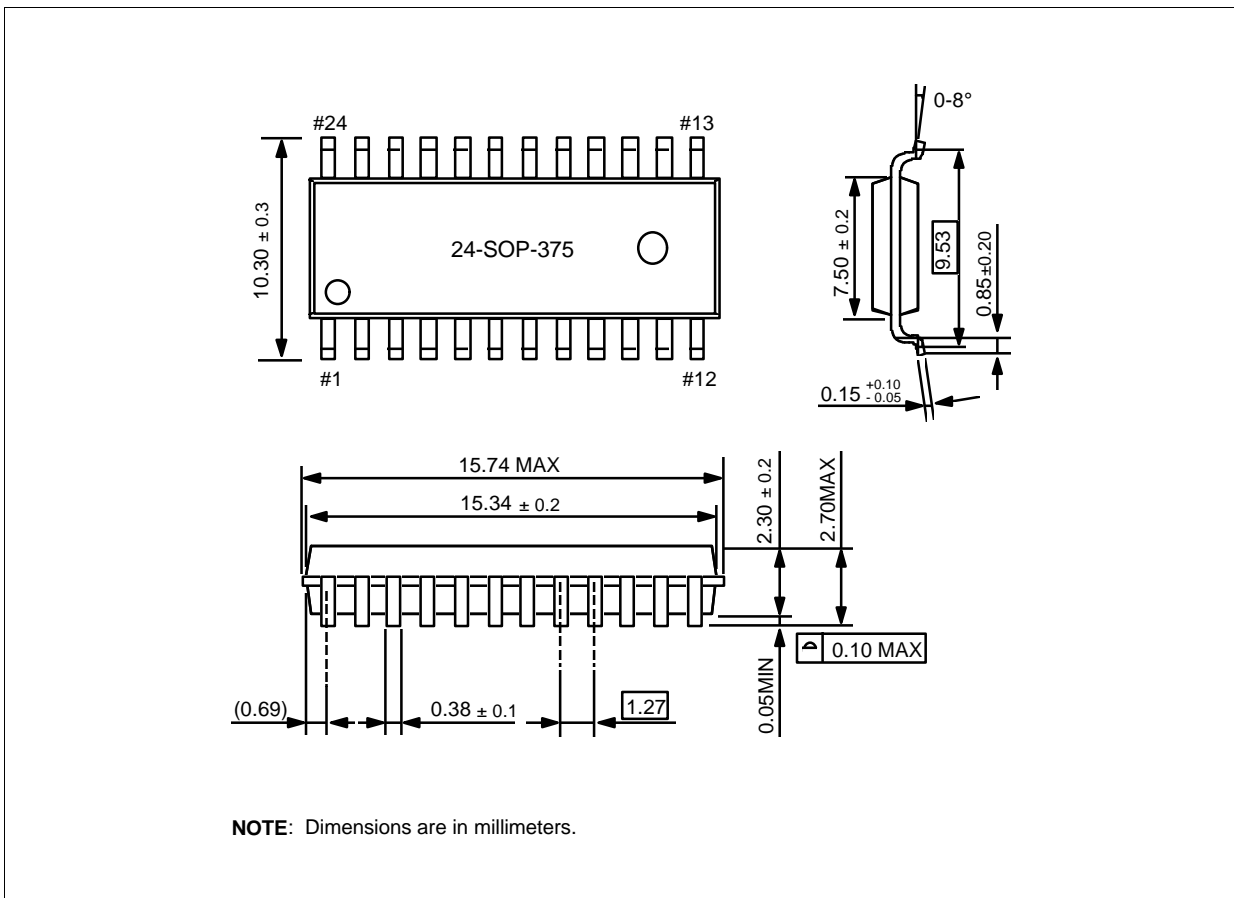


Figure 14-4. 24-SOP-375 Package Dimensions

# 15

## KS86P4004/P4104 OTP

### OVERVIEW

The KS86P4004/P4104 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS86C4004/C4104 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The KS86P4004/P4104 is fully compatible with the KS86C4004/C4104, both in function and in pin configuration. Because of its simple programming requirements, the KS86P4004/P4104 is ideal for use as an evaluation chip for the KS86C4004/C4104.

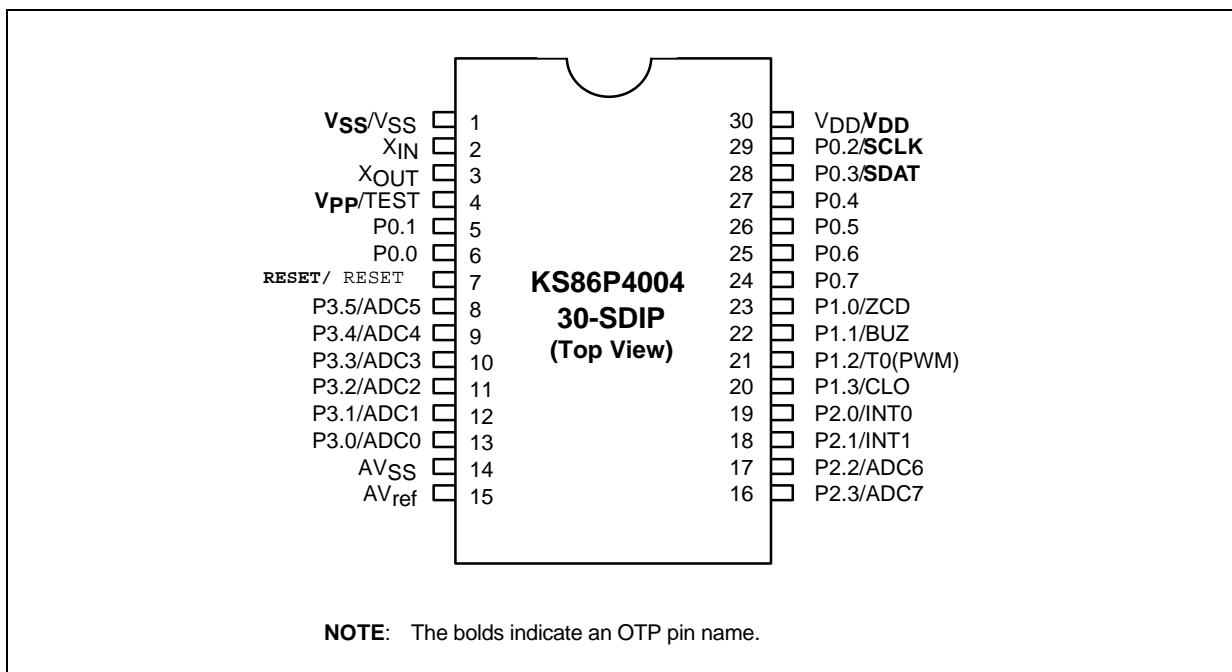


Figure 15-1. Pin Assignment Diagram (30-Pin SDIP Package)

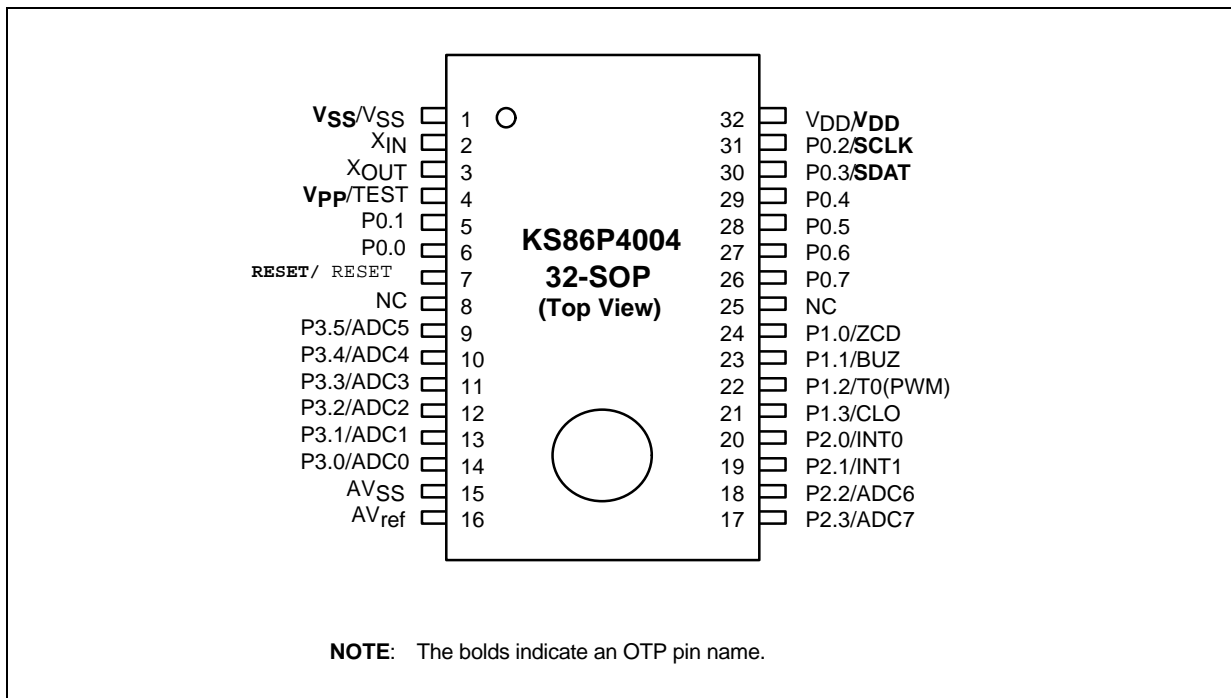


Figure 15-2. Pin Assignment Diagram (32-Pin SOP Package)

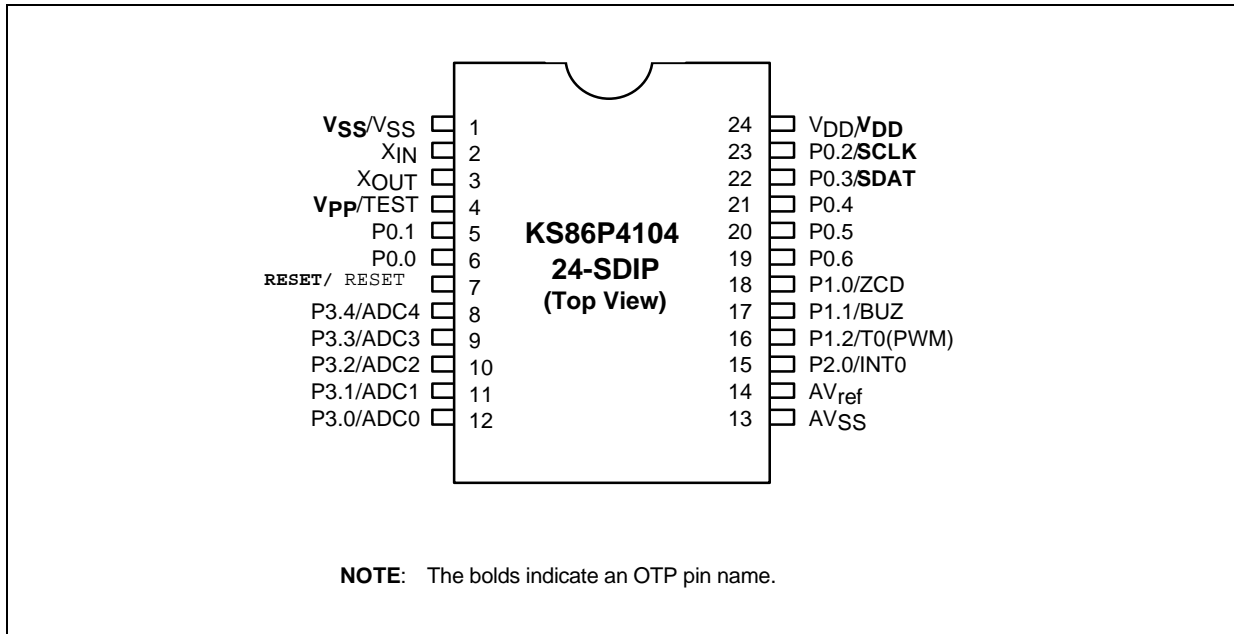


Figure 15-3. Pin Assignment Diagram (24-Pin SDIP Package)

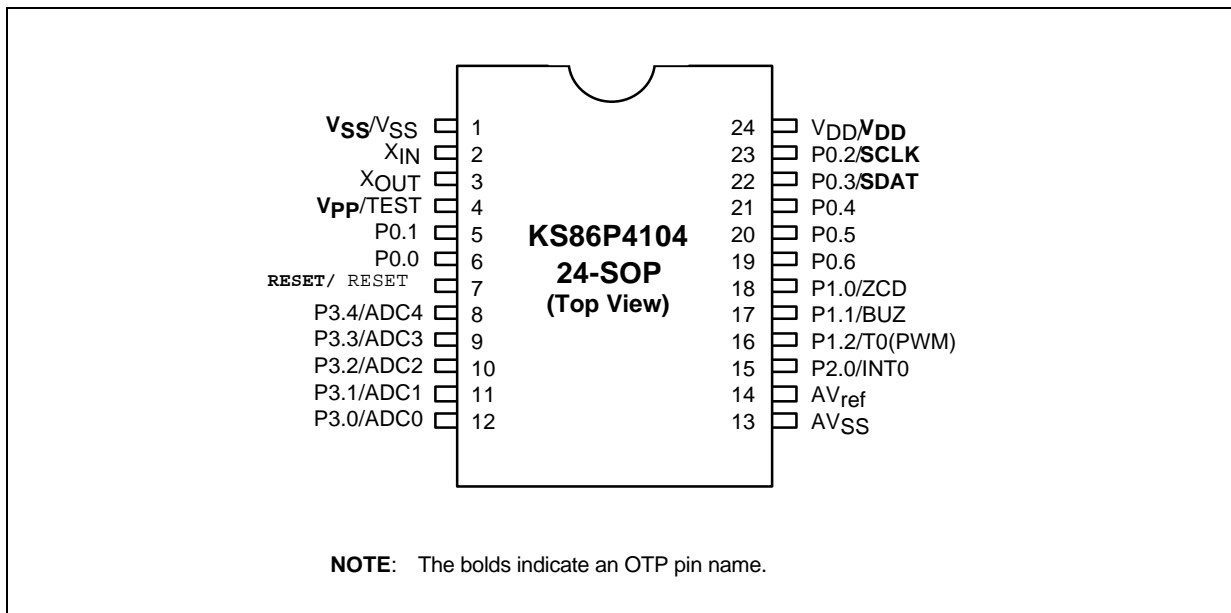


Figure 15-4. Pin Assignment Diagram (24-Pin SOP Package)



Table 15-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P0.3	SDAT	KS86P4004: 28 (30) KS86P4104: 22 (22)	I/O	Serial data pin (output when reading, Input when writing) Input and push-pull output port can be assigned
P0.2	SCLK	KS86P4004: 29 (31) KS86P4104: 23 (23)	I/O	Serial clock pin (input only pin)
TEST	V <sub>PP</sub> (TEST)	4	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	7	I	Chip Initialization
V <sub>DD</sub> /V <sub>SS</sub>	V <sub>DD</sub> /V <sub>SS</sub>	KS86P4004: 30 (32) / 1 KS86P4104: 24 (24) / 1	I	Logic power supply pin.

NOTE: ( ) means the SOP OTP pin number.

Table 15-2. Comparison of KS86P4004/P4104 and KS86C4004/C4104 Features

Characteristic	KS86P4004/P4104	KS86C4004/C4104
Program Memory	4-Kbyte EPROM	4-Kbyte mask ROM
Operating Voltage (V <sub>DD</sub> )	2.7 V to 5.5 V	2.7 V to 5.5 V
OTP Programming Mode	V <sub>DD</sub> = 5 V, V <sub>PP</sub> (TEST) = 12.5 V	
Pin Configuration	30 SDIP/32 SOP/24 SDIP/24 SOP	
EPROM Programmability	User Program 1 time	Programmed at the factory

### OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V<sub>PP</sub> (TEST) pin of the KS86P4004/P4104, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 15-3 below.

Table 15-3. Operating Mode Selection Criteria

V <sub>DD</sub>	V <sub>PP</sub> (TEST)	REG/MEM	ADDRESS (A15-A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

**NOTES**

