National Semiconductor

November 1993

GAL16V8QS-10L, -15L 20-Pin 0.8μ EECMOS PLDs

General Description

The EECMOS GAL16V8QS devices are fabricated using National's CS80BEV 0.8μ Electrically Erasable CMOS process. This advanced process makes National's GAL16V8QS extremely fast, allowing controlled output edge rates which dramatically reduce noise. Low noise is actually specified and guaranteed with National's GAL16V8QS Quiet Series™ devices.

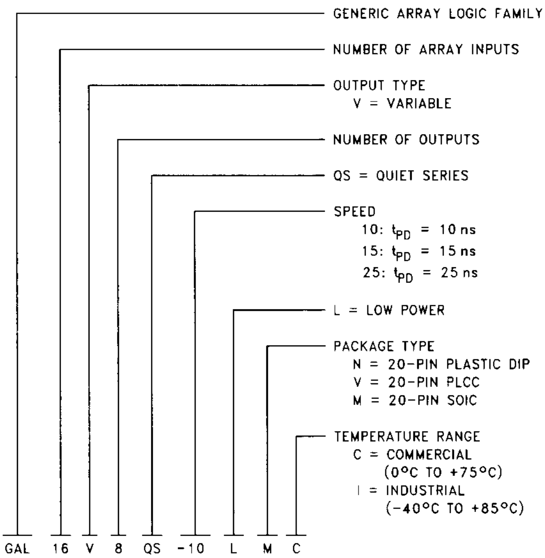
National's fast programming algorithm allows the GAL16V8QS to be programmed significantly faster than similar devices using industry standard programmers. Fast programming reduces the cost of programming by greatly increasing programming throughput. National guarantees a minimum of 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell, and functionality testing during manufacture. Therefore, National guarantees 100% field programmability and functionality of GAL® devices. In addition, a security circuit is built-in, providing proprietary designs with copy protection.

Features

- High performance 0.8 μ EECMOS technology
  - — 10 ns maximum propagation delay
  - — 5 ns setup time delay
  - — 7.5 ns clock to registered output delay
  - — f_{MAX} = 80 MHz
  - — Reduced ground bounce
  - — 2000V ESD protection
- Reduced power
  - — I_{CC} max = 90 mA @ 25 MHz
- Electrically erasable cell technology
  - — 100% tested at manufacture
- Fast programming algorithm
  - — Reduces programming cost, increases throughput
- Emulates popular PAL® devices
- Fully supported by National's OPAL™ and OPAL jr software as well as 3rd-party PLD development software
- Commercial and industrial grades

Ordering Information



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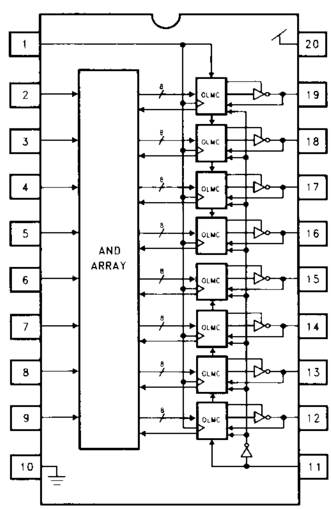
Block Diagram



TL/L/11916–1

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RRD-B20M113/Printed in U. S. A.

COMMERCIAL

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Off-State Output Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Output Current	±100 mA
Storage Temperature	−65°C to +150°C
Latchup Current	200 mA
Ambient Temperature with Power applied	−65°C to +125°
Junction Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Tolerance	2000V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

Symbol	Parameter	Commercial			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	0	25	75	°C
t_r	Clock Rise Time		3	250	ns
t_f	Clock Fall Time		3	250	ns
t_{rVCC}	V_{CC} Rise Time			250	ms

Electrical Characteristics

Symbol	Parameter	Conditions		Commercial		Units
				Min	Max	
V_{IH}	High Level Input Voltage			2.0	V_{CC} + 1.0	V
V_{IL}	Low Level Input Voltage			−0.5	0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −3.2 mA		2.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 24 mA			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = V_{CC} (max)			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = GND			−10	μA
I_{OS}	Output Short Circuit Current	V_{CC} = 5.0V, V_O = 0.5V T_A = 25°C (One Output, Duration <1 second)		−30	−135	mA
I_{CC}	Supply Current (Note 3)	f = 25 MHz, V_{CC} = Max, No Load	-10L		115	mA
			-15L		90	mA
C_I	Input Capacitance	V_{CC} = 5.0V, T_A = 25°C, f = 25 MHz			5	pF
$C_{I/O}$	I/O Capacitance	V_{CC} = 5.0V, T_A = 25°C, f = 25 MHz			6	pF

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified Recommended Operating Conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: I_{CC} parameters not directly 100% tested.

AC Specifications

Symbol	Parameter	Conditions (Note 4)	Commercial				Units
			-10L		-15L		
			Min	Max	Min	Max	
t_{PD}	Input or F/B to Combinatorial Output			10		15	ns
t_{SU}	Input or F/B Setup Time before Clock		5		7		ns
t_H	Hold Time (Input after Clock)		0		0		ns
t_{CLK}	Clock to Registered Output or F/B			7.5		9	ns
f_{MAX}	Clock Frequency (Note 5)	With Feedback		80		62.5	MHz
		Without Feedback		83.3		62.5	
t_W	Clock Pulse Width (High/Low)	Referenced at 1.5V	6		8		ns
t_{CYCLE}	Clock Period (with F/B)	$t_{CYCLE} = t_{SU} + t_{CLK}$	12.5		16		ns
t_{PZxI}	Input to Output Enable			10		15	ns
t_{PxZI}	Input to Output Disable (Note 6)			12		15	ns
t_{PZxG}	$\overline{G}$ to Output Enable			10		15	ns
t_{PxZG}	$\overline{G}$ to Output Disable (Note 6)			12		15	ns
t_{RESET}	Power-Up to Registered Output High			45		45	µs
f_I	Input Frequency (Note 7)			100		66.6	MHz
t_{PR}	Clock Valid after Power-Up			100		100	ns

Note 4: See AC test load on page 7. I_{CC} is measured with the GAL16V8QS configured as two 4-bit Gray code counters.

Note 5: f_{MAX} parameters not directly 100% tested.

Note 6: Values are tested with $C_L = 50$ pF

Note 7: $f_I = (t_{PD})^{-1}$

INDUSTRIAL

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Off-State Output Voltage (Note 2)	−2.5V to V_{CC} + 1.0V
Output Current	±100 mA
Storage Temperature	−65°C to +150°C
Latchup Current	200 mA
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Tolerance	2000V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

Symbol	Parameter	Industrial			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.50	5	5.50	V
T_A	Operating Free-Air Temperature	−40	25	85	°C
t_r	Clock Rise Time		3	250	ns
t_f	Clock Fall Time		3	250	ns
t_{rVCC}	V_{CC} Rise Time			250	ms

Electrical Characteristics

Symbol	Parameter	Conditions		Industrial		Units
				Min	Max	
V_{IH}	High Level Input Voltage			2.0	V_{CC} + 1.0	V
V_{IL}	Low Level Input Voltage			−0.5	0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −3.2 mA		2.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 24 mA			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = V_{CC} (Max)			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = GND			−10	μA
I_{OS}	Output Short Circuit Current	V_{CC} = 5.0V, V_O = 0.5V T_A = 25°C (One Output, Duration <1 second)		−30	−135	mA
I_{CC}	Supply Current (Note 3)	f = 25 MHz, V_{CC} = Max, No Load	-10L		130	mA
			-15L		130	
C_I	Input Capacitance	V_{CC} = 5.0V, T_A = 25°C, f = 25 MHz			5	pF
$C_{I/O}$	I/O Capacitance	V_{CC} = 5.0V, T_A = 25°C, f = 25 MHz			6	pF

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified Recommended Operating Conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: I_{CC} parameters not directly 100% tested.

INDUSTRIAL

AC Specifications

Symbol	Parameter	Conditions (Note 4)	Industrial				Units
			-10L		-15L		
			Min	Max	Min	Max	
t_{PD}	Input or F/B to Combinatorial Output			10		15	ns
t_{SU}	Input or F/B Setup Time before Clock		5		7		ns
t_H	Hold Time (Input after Clock)		0		0		ns
t_{CLK}	Clock to Registered Output or F/B			7.5		9	ns
f_{MAX}	Clock Frequency (Note 5)	With Feedback		80		62.5	MHz
		Without Feedback		83.3		62.5	MHz
t_W	Clock Pulse Width (High/Low)	Referenced at 1.5V	6		8		ns
t_{CYCLE}	Clock Period (with F/B)	$t_{CYCLE} = t_{SU} + t_{CLK}$	12.5		16		ns
t_{PZXI}	Input to Output Enable			10		15	ns
t_{PXZI}	Input to Output Disable (Note 6)			12		15	ns
t_{PZXG}	$\overline{G}$ to Output Enable			10		15	ns
t_{PXZG}	$\overline{G}$ to Output Disable (Note 6)			12		15	ns
t_{RESET}	Power-Up to Registered Output High			45		45	μs
f_I	Input Frequency (Note 7)			100		66.6	MHz
t_{PR}	Clock Valid after Power-Up			100		100	ns

Note 4: See AC test load on page 7. I_{CC} is measured with the GAL16V8QS configured as two 4-bit Gray code counters.

Note 5: f_{MAX} parameters not directly 100% tested.

Note 6: Values are tested with $C_L = 50$ pF

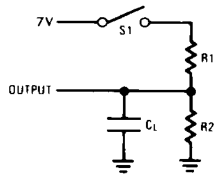
Note 7: $f_I = (t_{PD})$

GAL16V8QS Quiet Electrical Characteristics

Symbol	Parameter	Conditions (Note 1)	Commercial		Units
			Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	V_{CC} = 5.0V, T = 25°C	1.2	1.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	V_{CC} = 5.0V, T = 25°C	−0.3	−1.2	V
V_{IHD}	Maximum High Level Dynamic Input Voltage	V_{CC} = 5.0V, T = 25°C, f = 1 MHz	1.9	2.2	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage	V_{CC} = 5.0V, T = 25°C, f = 1 MHz	1.2	0.8	V
t_{WGB}	Width of Ground Bounce Peak Measured at +0.8V	V_{CC} = 5.0V, T = 25°C		3.0	ns

Note 1: AC test load is used with $R_1 = R_2 = 500\Omega$, S1 open. Quiet Electrical Characteristics are measured with seven outputs switching from HIGH to LOW, with the remaining output LOW. V_{OLP} and V_{OLV} are measured at the non-switching output. Input-under-test switching is 3V to threshold for V_{ILD} and 0V to threshold for V_{IHD}. Quiet Electrical Parameters are not directly 100% tested, but are characterized and guaranteed by design.

AC Test Load



R1 = R2 = 500Ω
C_L = 50 pF
For:
t_{PD}: S1 open
$t_{PZH/HZ}$: S1 open
$t_{PZL/LZ}$: S1 closed
Active to TRI-STATE measurement level = active output level ±0.3V.

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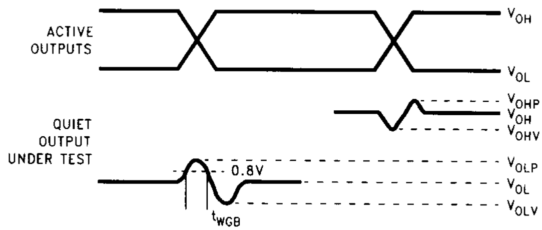
Test Waveforms

Quiet Output Noise Voltage Waveforms



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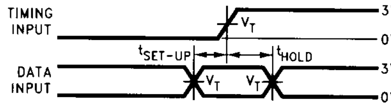
Note A. V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B. Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, skew < 150 ps.

Note C. Test load for Quiet output: C_L = 50 pF, $R_L = 500\Omega$.

Setup and Hold



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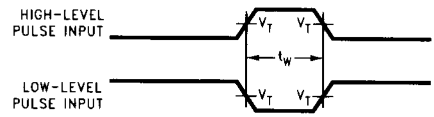
Pulse Width



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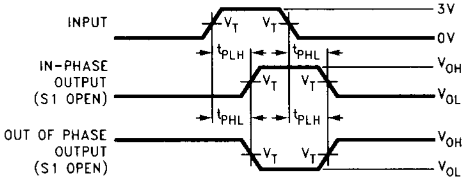
Test Waveforms (Continued)

Propagation Delay



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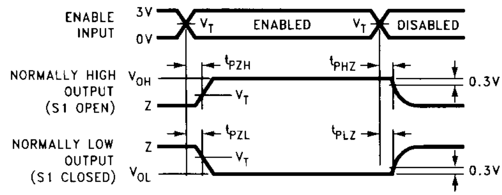
Enable and Disable



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Notes:

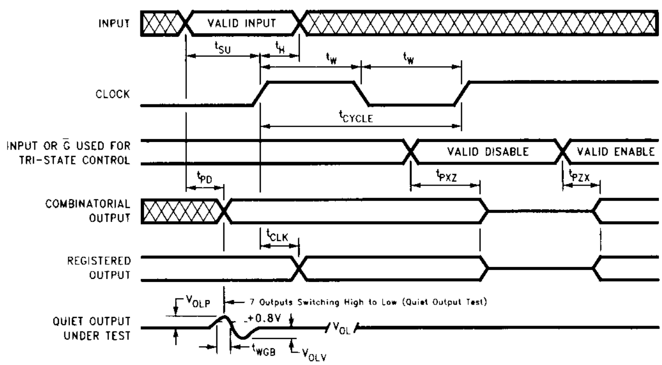
C_L includes probe and jig capacitance.

V_T = 1.5V.

Test Inputs have rise and fall times of 3 ns between 0.3V and 2.7V.

In the examples above, the phase relationship between inputs and outputs have been chosen arbitrarily.

Switching Waveforms



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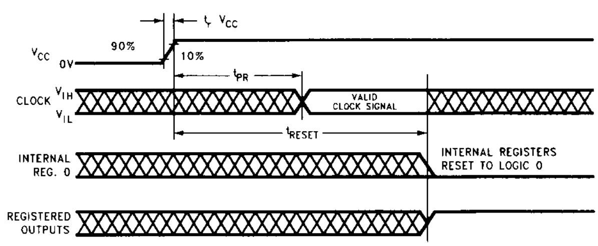
Power-Up Reset Waveforms



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Functional Description

The GAL logic array consists of a programmable AND array with fixed OR-gate connections, similar to the bipolar PAL architecture. The logic array is organized as 16 complementary input lines crossing 64 "product term" lines with a programmable EEPROM cell at each intersection (2048 cells). Each programmable cell may establish a connection between an input line (true or complement phase of an array input signal) and a product term. A product term is satisfied (logically true) while all of the input lines "connected" to it are in the high logic state.

The 64 product terms are organized into eight output groups with eight terms each. Seven or eight of the product terms in each output group feed into an OR-gate to produce each output logic function; one of the product terms may instead be used to control the associated TRI-STATE device output.

The fundamental transfer function of each GAL output is the familiar Boolean sum-of-products. Design development software is available which accepts Boolean equations and converts them automatically into GAL programming patterns.

As shown in the GAL16V8QS Block Diagram *(Figure 2)*, a total of eight output logic functions are available. Each of the AND/OR logic functions feeds into an "output logic macrocell" (OLMC). The eight OLMCs control the flow of input and output signals between the logic array and the device's I/O pins.

Under control of an OLMC, each output may be designated either registered or combinatorial (non-registered). In the registered output configuration, the logic function output passes through a D-type flip-flop triggered by the rising edge of the clock input. Additionally, the logic function's output polarity may be designated active-low or active-high (adjusted before the register, if present). OLMC options such as these are selected using a set of programmable architecture control cells. These architecture cells are normally configured automatically by the development software or programming hardware.

All of the possible I/O configurations of the GAL16V8QS are classified into three basic modes: "Small-PAL" mode, "Registered-PAL" mode and "Medium-PAL" mode. These modes correspond to the architectures of the PAL families which the GAL16V8QS can emulate. The modes determine the mixture of OLMC configurations which can be selected for the device. The OLMC Selection table (Table I) lists which functions can be selected on the device pin* 1 and pins* 11 through 19 for each of the three modes. The logic diagram in *Figure 3* illustrates these OLMC functions. "OUTPUT" represents the always-active combinatorial output configuration available in the "Small-PAL" mode. "REGISTER" is the registered output with register feedback available in the "Registered-PAL" mode. "I/O" is the combinatorial bidirectional I/O available in "Registered-PAL" and "Medium-PAL" modes. "TRI-STATE" is the TRI-STATE combinatorial output function appearing on pins* 12 and 19 in the "Medium-PAL" mode. "INPUT" in Table I denotes an OLMC used as a dedicated input only.

In the "Small-PAL" and "Medium-PAL" modes (Table I), pins* 1 and 11 are always dedicated inputs. In the "Registered-PAL" mode, however, pin* 1 becomes the clock input controlling all OLMC registers, and pin* 11 becomes the output enable ($\overline{G}$) input controlling the TRI-STATE outputs of all registered OLMCs. Within the "Small-PAL" and "Registered-PAL" modes in Table I, the functions of pins* 12 through 19 can be selected individually from either of the two functions listed. For example, in "Registered-PAL" mode, pins* 12 through 19 can each be designated as either a registered output or a combinatorial I/O. The "Medium-PAL" mode represents a single fixed configuration used to emulate combinatorial medium PAL devices (16L8, 16H8, 16P8).

Table II lists the bipolar PAL products which the GAL16V8QS can emulate, and the specific input/output configurations used. This is just a subset, however, of all the configurations provided in Table I.

All registers in a GAL device are reset to the low state upon power-up. The active-low outputs, in turn, assume high logic levels (if enabled) regardless of the selected output polarity. This may simplify sequential circuit design and test. To ensure successful power-up reset, V_{CC} must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible (within the specified time, t_{PR}) to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

It should be noted that the switching of any input not logically connected to a product term or logic function has no effect on the associated output logic state. To minimize power consumption, however, unused inputs should be connected to a stable logic level such as ground or V_{CC} (CMOS GAL inputs may be tied directly to the supply voltage without causing excessive loading conditions).

*Applies to 20-pin DIP, 20-pin SOIC and 20-lead PLCC packages for GAL16V8QS.

Quiet Series

As system frequencies increase, so do concerns over both device generated and system generated noise. Proper printed circuit board layout and construction techniques should be followed by the designer to minimize system generated noise, additionally however, IC manufacturers should bear the responsibility to minimize device generated noise. One of the biggest sources of device generated noise is ground bounce. Ground bounce not only manifests itself on the ground pin, but more importantly on quiet outputs, input thresholds, and other internal circuitry. Noise on quiet outputs can cause the false triggering of external devices, while a shift in the device's internal ground can cause false triggering and even instability in the device itself. Often these problems are attributed to a damaged or faulty PLD when, in fact, the PLD has marginally lower noise immunity than other seemingly identical devices.

The magnitude of ground bounce has a direct correlation with output edge rates. Therefore National's Quiet Series devices have slower more "gentle" edges. National uses an advanced 0.8μ back-biased EECMOS process to decrease propagation times in order to accomodate the slower edge rates. The result is a very robust, high speed PLD. Since National offers Quiet Series devices at comparable pricing to non-Quiet Series devices, **Quiet Series devices are recommended for new designs.**

GAL16V8QS Block Diagram/DIP and SOIC Connections

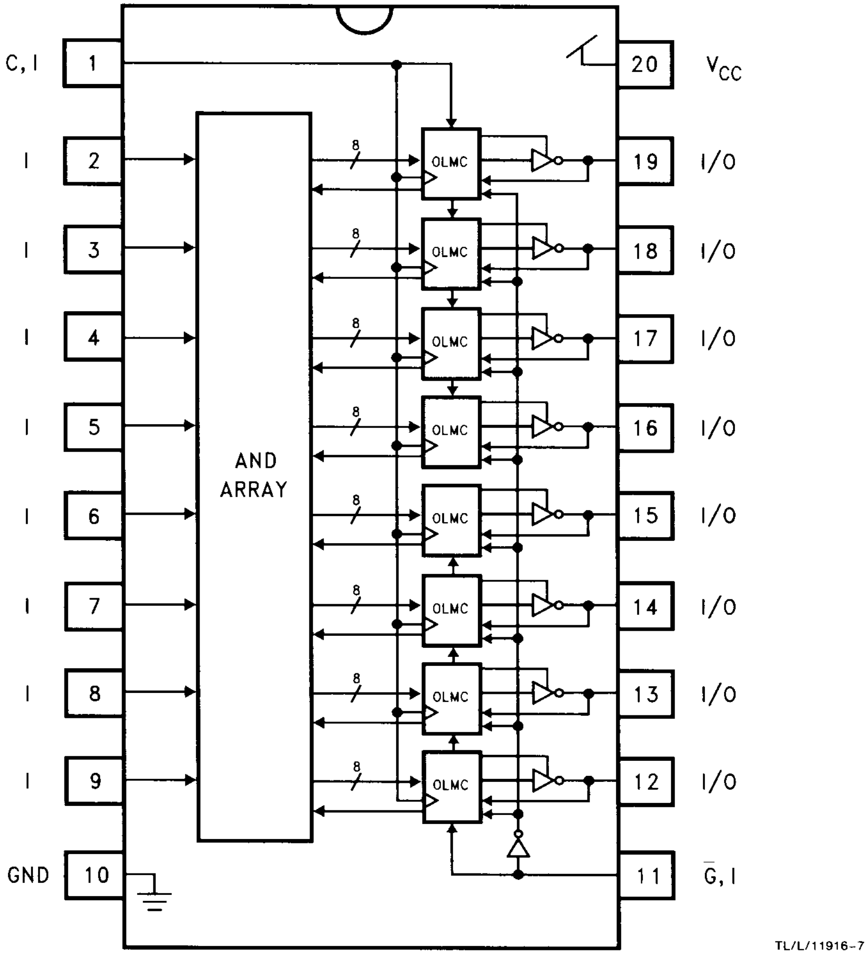

FIGURE 1

GAL16V8QS PLCC Connections

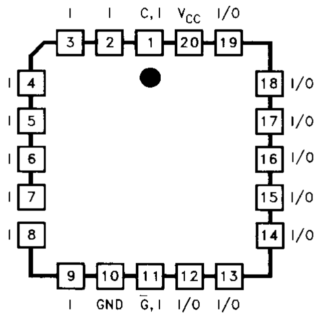

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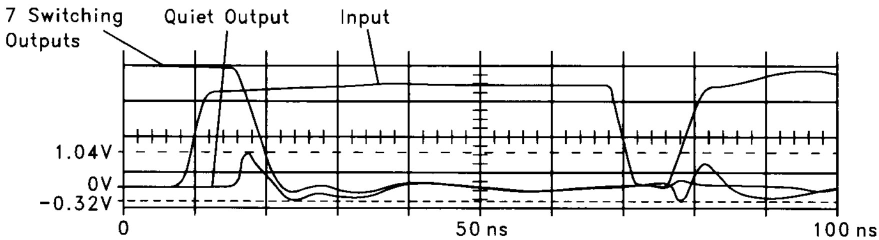
FIGURE 2

Quiet Series Testing

Quiet Series testing is performed with seven outputs switching. The remaining output, referred to as the "quiet output", maintains a low logic level. V_{OLP} and V_{OLV} measure the peak and valley, respectively, of the "bounce" on this quiet output (referenced to ground) as the seven outputs swing from high to low. Notice V_{OLP} and V_{OLV} do not directly measure the ground itself (which is stabilized through the use of proper PCB design techniques), but more importantly quantify how ground bounce affects a non-switching output. Noise on the quiet output will be propagated to the inputs of subsequent devices and can falsely trigger these devices. False triggering occurs when the magnitude of a signal exceeds the input thresholds of these devices for a sufficient duration. Therefore, the width of the bounce, t_{WGB}, is also measured. Based on extensive empirical analysis, the values for V_{OLP} and t_{WGB} have been found to be below the triggering requirements of common types of logic devices.

Just as ground bounce affects external circuitry, it also affects the internal silicon circuitry of the PLD. Usually the effect of ground bounce on device input thresholds is most significant. V_{IHD} and V_{ILD} measure the effect of a change in the ground potential on the input thresholds of the PLD. V_{IHD} and V_{ILD} are measured with seven outputs switching at 1 MHz while the input voltage at one input is gradually changed until the device shows signs of triggering. Note that the outputs may only exhibit small differences that show they are being affected by the input under test. The test is repeated on all inputs.



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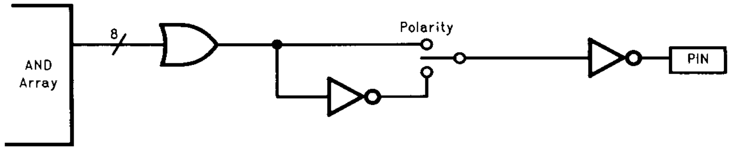
Typical Quiet Electrical Measurements
Seven Outputs Switching into AC Test Load
V_{CC} = 5.0V, T = 25°C

OLMC Configuration

OUTPUT (Active Combinatorial Output)



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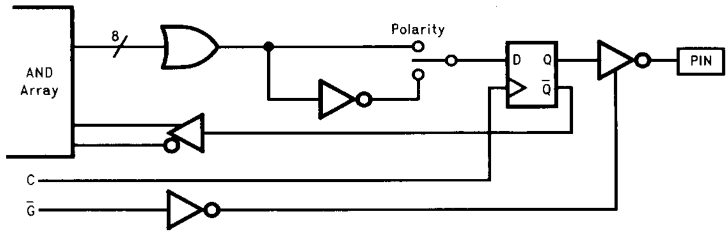
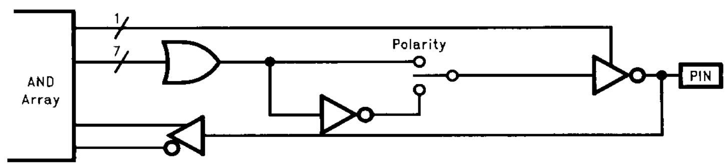
REGISTER (Registered Output)



TL/L/11916-10

I/O (Combinatorial Input/Output)



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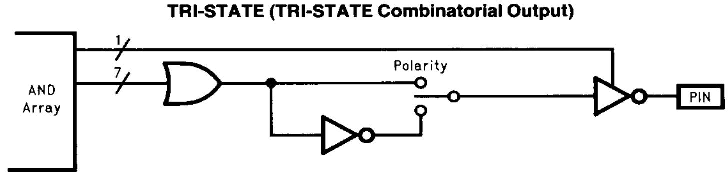
TRI-STATE (TRI-STATE Combinatorial Output)



TL/L/11916-12

FIGURE 3

Clock/Input Frequency Specifications

The clock frequency (f_{CLK}) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e. based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_w high + t_w low) and the minimum "data window" period (t_{SU} + t_H). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period ($t_{CYCLE} = f_{CLK}^{-1}$ with feedback) is defined as $t_{CLK} + t_{SU}$. This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle.

The input frequency (f_I) parameter specifies the maximum rate at which each GAL input can be toggled and still produce valid logic transitions on each combinatorial output. The f_I specification is derived as the inverse of the combinatorial propagation delay (t_{PD}).

Security Cell

A security cell is provided on all GAL16V8QS devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature

Each GAL16V8QS device contains a User Electronic Signature (UES) word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information is read out of the device using the normal program verification procedure provided by the programming equipment. The information may be accessed at any time independent of the state of the security cell. National's OPAL and OPAL jr development softwares allow electronic signature data to be entered by the user and downloaded to the programming equipment.

Bulk Erase

The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Manufacturer Testing

Because of EECMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to datasheet specifications.

Development Support

National's GAL16V8QS family is supported by popular industry-standard PLD development software and device programmers. In addition, GAL16V8QS devices are supported by National's OPAL and OPAL jr PLD development software packages. OPAL and OPAL jr also contain a PAL to GAL conversion utility for converting designs from PAL devices to GAL devices. OPAL jr is distributed free of charge and can be obtained through your local National Semiconductor sales representative or by downloading it from National's PLD Applications and Support Bulletin Board at (408) 721-7418, (8-n-1), 2400-19200 bps.

National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells.

OLMC Configuration Details

Understanding the information in this section is not essential when using approved programming equipment and software for developing GAL designs. This is a more thorough disclosure of the GAL architecture provided for direct JEDEC cell-map editing and diagnostic purposes. This section alone, however, does not contain sufficient information to implement the GAL programming algorithm. If detailed specifications of the GAL programming algorithm are needed, please contact the National Semiconductor Programmable Products Applications and Support Department.

OLMC Configuration Details (Continued)

As mentioned in the Functional Description, the OLMC is responsible for selecting input and/or output paths, registered vs. combinatorial outputs, active-high or low polarity, and common vs. locally-controlled TRI-STATE control. Additionally, the OLMCs select between alternate logic array input paths to maintain JEDEC cell-map compatibility with either "small-PAL" or "medium-PAL" logic arrays.

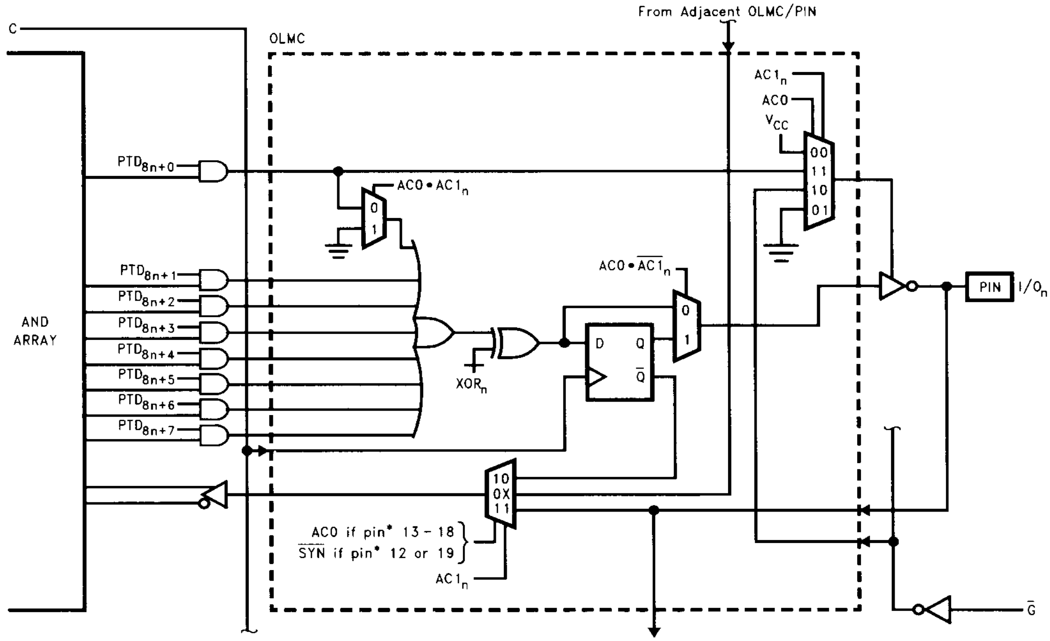
The various configurations of the OLMCs are controlled by a set of programmable "architecture" cells, separate from the logic-defining array cells. Each GAL device contains two "global" architecture cells, "SYN" and "AC0", which affect all OLMCs. Each of the device's eight OLMCs also contains two "local" cells, "AC1" and "XOR". The OLMC Logic Diagram in *Figure 4* shows how the architecture cells select the different paths through the OLMC.

The SYN bit controls whether a device will have any registered outputs (SYN = 0) or will be purely combinatorial (SYN = 1). The SYN bit determines whether device pins* 1 and 11 are used as the clock and global TRI-STATE control inputs (SYN = 0) or whether they are ordinary inputs (SYN = 1). The AC0 bit selects between the "Small-PAL" mode and the "Medium/Registered-PAL" modes. The function of the AC1 bits depend on the state of the AC0 bit. In "Small-PAL" mode (AC0 = 0), the AC1 bit in each OLMC determines whether the associated device pin is an output (AC1 = 0) or an input (AC1 = 1). In "Registered-PAL" mode (AC0 = 1), the AC1 bit determines whether each OLMC is registered (AC1 = 0) or combinatorial (AC1 = 1). In "Medium-PAL" mode (AC0 = 1), the AC1 bits in all OLMCs must be set to 1 (combinatorial). All of the valid architecture bit configurations are shown in the OLMC Architecture table (Table I).

Independent of SYN, AC0 and the AC1 bits, the XOR bit in each OLMC selects between active-low (XOR = 0) or active-high (XOR = 1) output polarity.

*Applies to both 20-pin DIP and 20-lead PLCC packages for GAL16V8QS.

OLMC Logic Diagram



*Applies to 20-pin DIP, 20-pin SOIC and 20-lead PLCC packages for GAL16V8QS.

FIGURE 4

Input Schematic

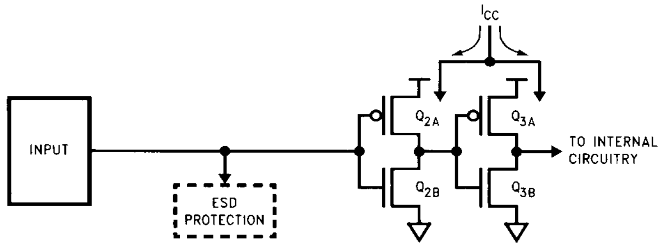


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TABLE I. OLMC Architecture Configuration

Pin Number	"Small PAL" Mode Function		"Registered PAL" Mode Function		"Medium PAL" Mode Function
1	INPUT	INPUT	CLOCK	CLOCK	INPUT
19***	I/O	INPUT	REGISTER	I/O	TRI-STATE**
18***	I/O	INPUT	REGISTER	I/O	I/O
17***	I/O	INPUT	REGISTER	I/O	I/O
16***	OUTPUT*	NC	REGISTER	I/O	I/O
15***	OUTPUT*	NC	REGISTER	I/O	I/O
14***	I/O	INPUT	REGISTER	I/O	I/O
13***	I/O	INPUT	REGISTER	I/O	I/O
12***	I/O	INPUT	REGISTER	I/O	TRI-STATE**
11	INPUT	INPUT	$\overline{G}$	$\overline{G}$	INPUT
Architecture Bits Configuration	$AC1_n = 0$	$AC1_n = 1$	$AC1_n = 0$	$AC1_n = 1$	$AC1_n = 1$
	SYN = 1, AC0 = 0		SYN = 0, AC0 = 0		SYN = 1, AC0 = 0
	All outputs are combinatorial and always active		At least one output is registered		All I/O pins are combinatorial

Note: Pin numbers above apply to 20-pin DIP, 20-pin SOIC and 20-lead PLCC packages for GAL16V8.

* Active combinatorial output

** TRI-STATE combinatorial output

*** $AC1_n$ applies to these I/O pins only

PAL Replacement Configurations

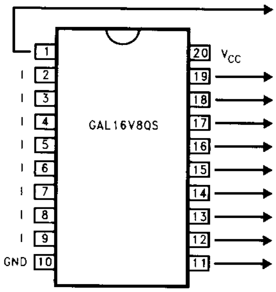

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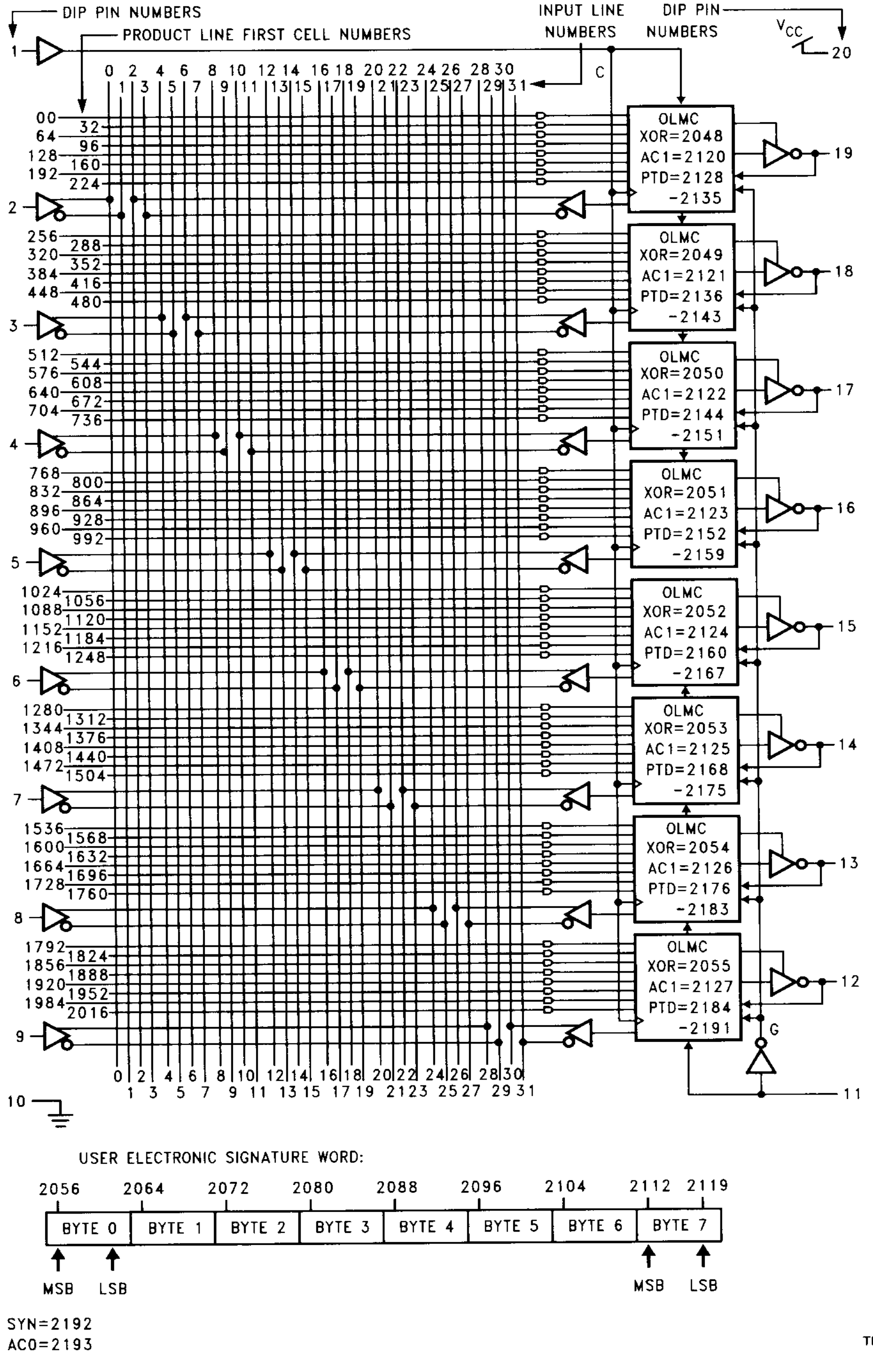
TABLE II. OLMC Architecture Configuration

	"Small PAL" Mode				"Registered-PAL" Mode			"Medium-PAL" Mode
	INPUT	INPUT	INPUT	INPUT	CLOCK	CLOCK	CLOCK	INPUT
	OUTPUT*	INPUT	INPUT	INPUT	REGISTER	I/O	I/O	TRI-STATE**
	OUTPUT*	OUTPUT*	INPUT	INPUT	REGISTER	REGISTER	I/O	I/O
	OUTPUT*	OUTPUT*	OUTPUT*	INPUT	REGISTER	REGISTER	REGISTER	I/O
	OUTPUT*	OUTPUT*	OUTPUT*	OUTPUT*	REGISTER	REGISTER	REGISTER	I/O
	OUTPUT*	OUTPUT*	OUTPUT*	OUTPUT*	REGISTER	REGISTER	REGISTER	I/O
	OUTPUT*	OUTPUT*	OUTPUT*	INPUT	REGISTER	REGISTER	REGISTER	I/O
	OUTPUT*	OUTPUT*	INPUT	INPUT	REGISTER	REGISTER	I/O	I/O
	OUTPUT*	INPUT	INPUT	INPUT	REGISTER	I/O	I/O	TRI-STATE**
	INPUT	INPUT	INPUT	INPUT	$\overline{G}$	$\overline{G}$	$\overline{G}$	INPUT
EMULATED PAL PRODUCTS	10L8 10H8 10P8	12L6 12H6 12P6	14L4 14H4 14P4	16L2 16H2 16P2	16R8 16RP8	16R6 16RP6	16R4 16RP4	16L8 16H8 16P8

*Active combinatorial output.

**TRI-STATE combinatorial output.

GAL16V8QS Logic Diagram



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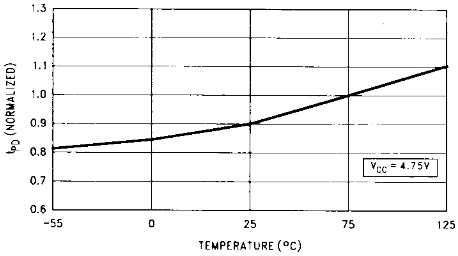
Typical Performance Characteristics

t_{PD} vs Temperature



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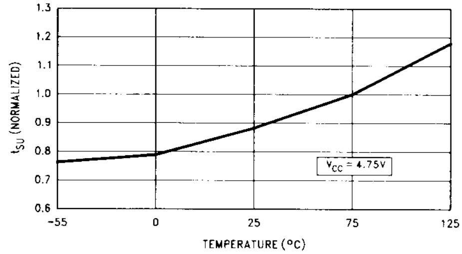
t_{SU} vs Temperature



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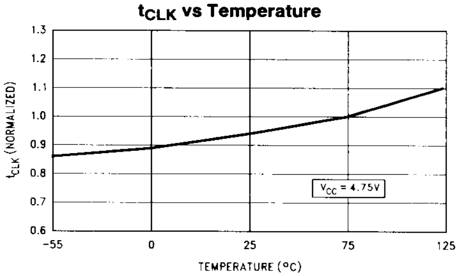
t_{CLK} vs Temperature



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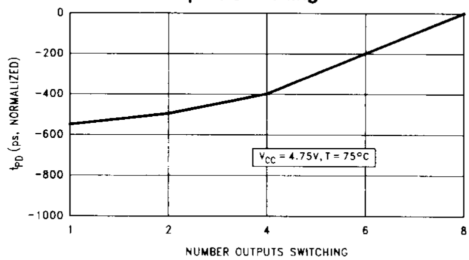
t_{PD} vs Number of Outputs Switching



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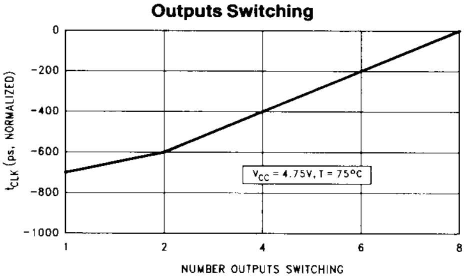
t_{CLK} vs Number of Outputs Switching



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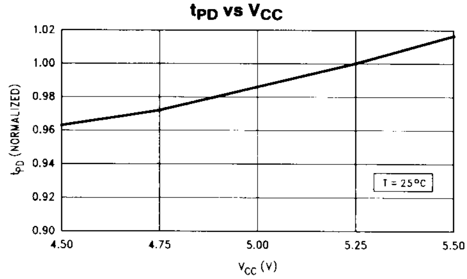
t_{PD} vs V_{CC}



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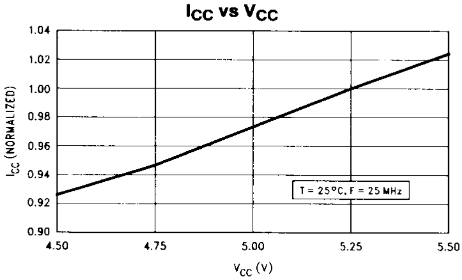
I_{CC} vs V_{CC}



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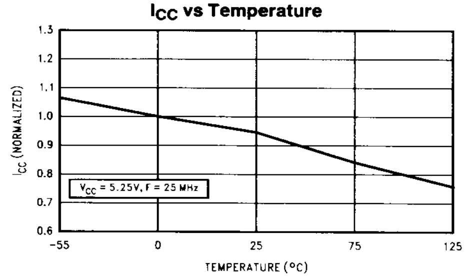
I_{CC} vs Temperature



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Ordering Information†

Commercial Devices

t_{PD} (ns)	t_{SU} (ns)	t_{CLK} (ns)	I_{CC} (mA)	QS	Part Number	Package
10	5	7.5	115	Y	GAL16V8QS-10LNC	PDIP
10	5	7.5	115	Y	GAL16V8QS-10LVC	PLCC
10	5	7.5	115	Y	GAL16V8QS-10LMC	SOIC
15	7	9	90	Y	GAL16V8QS-15LNC	PDIP
15	7	9	90	Y	GAL16V8QS-15LVC	PLCC
15	7	9	90	Y	GAL16V8QS-15LMC	SOIC

Industrial Devices

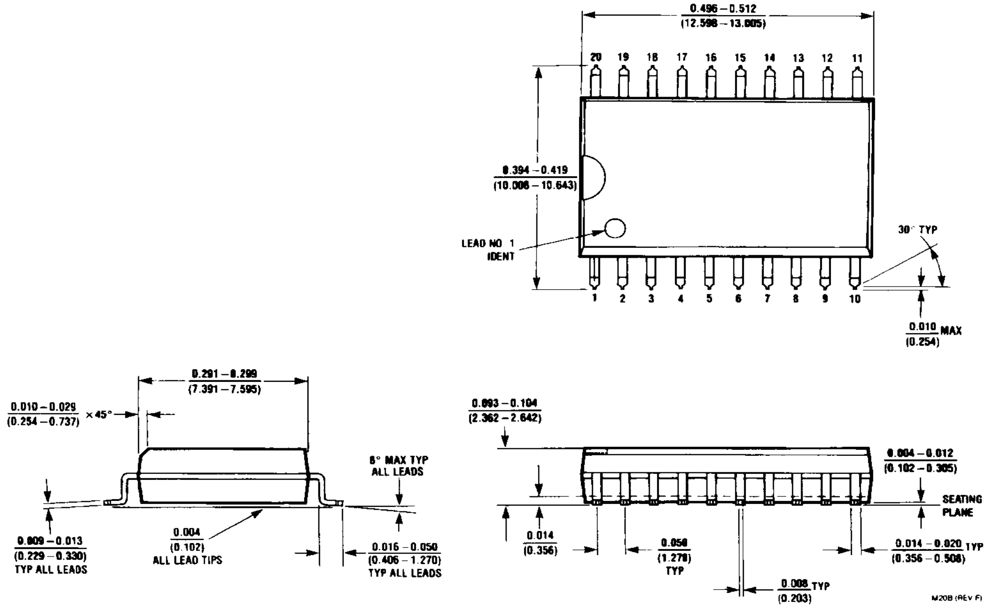
t_{PD} (ns)	t_{SU} (ns)	t_{CLK} (ns)	I_{CC} (mA)	QS	Part Number	Package
10	5	7.5	130	Y	GAL16V8QS-10LNI	PDIP
10	5	7.5	130	Y	GAL16V8QS-10LVI	PLCC
10	5	7.5	130	Y	GAL16V8QS-10LMI	SOIC
15	7	9	130	Y	GAL16V8QS-15LNI	PDIP
15	7	9	130	Y	GAL16V8QS-15LVI	PLCC
15	7	9	130	Y	GAL16V8QS-15LMI	SOIC

Military Devices

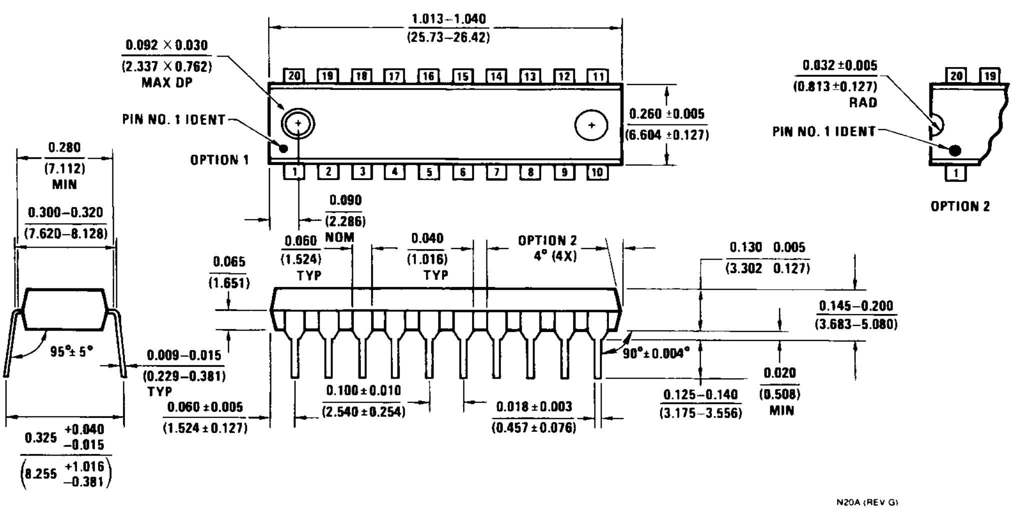
Contact your local National Semiconductor sales representative for availability of military grade GAL16V8QS devices.

†Quiet Series devices (GAL16V8QS) recommended for new designs. Refer to 1993 Programmable Logic Devices Databook and Design Guide (Lit# 400081) for quarter power GAL16V8A specifications.

Physical Dimensions inches (millimeters)



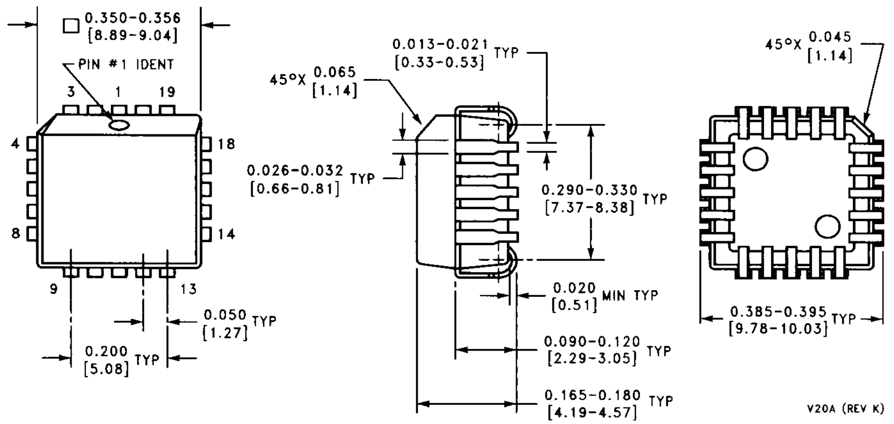
20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B



20-Lead (0.300″ Wide) Molded Dual-In-Line Package
NS Package Number N20A

Lit # 104311-001

Physical Dimensions inches (millimeters) (Continued)



20-Lead Molded Plastic Leaded Chip Carrier
NS Package Number V20A

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