

CAT28F010/CAT28F010I

1 Megabit CMOS FLASH MEMORY

FEATURES

- Fast Read Access Time: 120/150/200 ns
- Low Power CMOS Dissipation:
 - Active: 30 mA max (CMOS/TTL levels)
 - Standby: 1 mA max (TTL levels)
 - Standby: 100 μ A max (CMOS levels)
- High Speed Programming:
 - 10 μ S per byte
 - 2 Sec Typ Chip Program
- 12.0V \pm 5% Programming and Erase Voltage
- Stop Timer for Program/Erase
- On-Chip Address and Data Latches
- JEDEC Standard Pinouts:
 - 32 pin DIP
 - 32 pin PLCC
 - 32 pin TSOP (8 x 14; 8 x 20)
- 10,000 Program/Erase Cycles
- 10 Year Data Retention
- Electronic Signature

DESCRIPTION

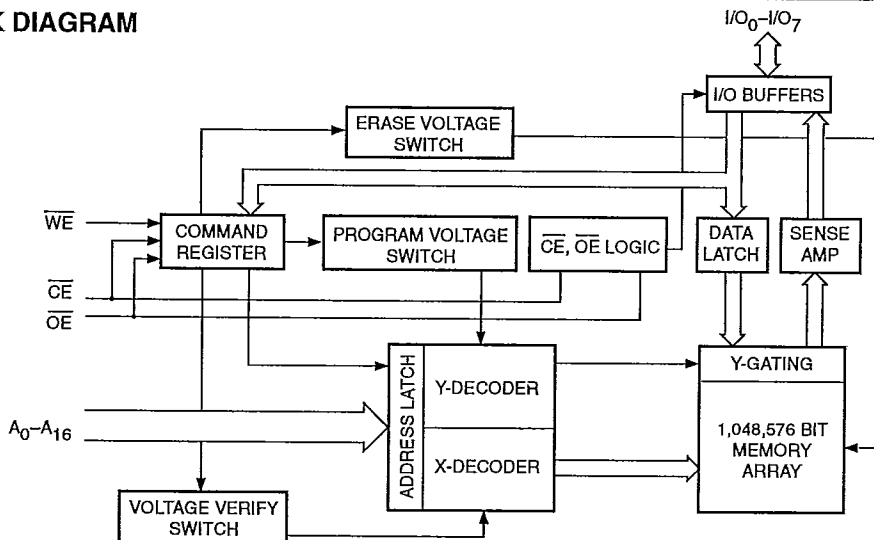
The CAT28F010/CAT28F010I is a high speed 128K x 8 bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 1 second.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a

two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F010/CAT28F010I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32 pin plastic DIP, 32 pin PLCC or 32 pin TSOP packages.

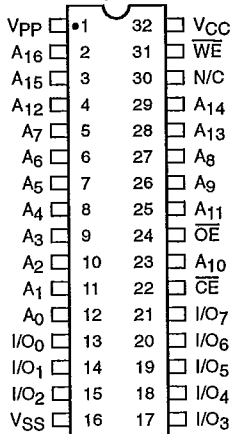
BLOCK DIAGRAM



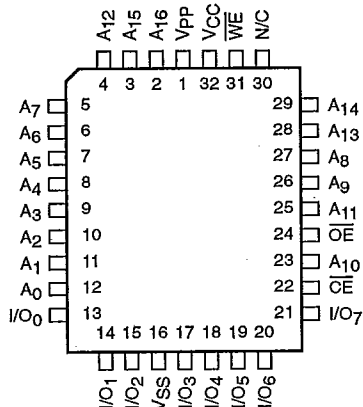
5108 FHD F02

PIN CONFIGURATION

DIP Package



PLCC Package

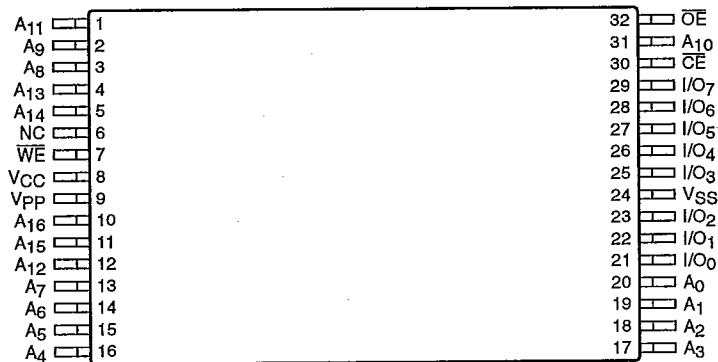


5108 FHD F01

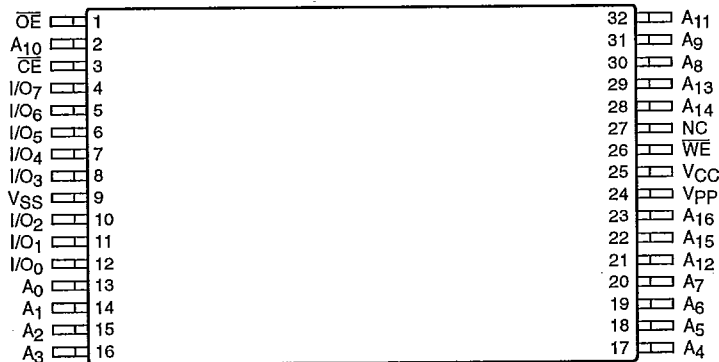
PIN FUNCTIONS

Pin Name	Type	Function
A ₀ –A ₁₆	Input	Address Inputs for memory addressing
I/O ₀ –I/O ₇	I/O	Data Input/Output
$\overline{\text{CE}}$	Input	Chip Enable
$\overline{\text{OE}}$	Input	Output Enable
WE	Input	Write Enable
V _{CC}		Voltage Supply
V _{SS}		Ground
V _{PP}		Program/Erase Voltage Supply

TSOP Package (Standard Pinout)



TSOP Package (Reverse Pinout)



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +95°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground ⁽¹⁾	-2.0V to +V _{CC} + 2.0V
Voltage on Pin A ₀ with Respect to Ground ⁽¹⁾	-2.0V to +13.5V
V _{PP} with Respect to Ground during Program/Erase ⁽¹⁾	-2.0V to +14.0V
V _{CC} with Respect to Ground ⁽¹⁾	-2.0V to +7.0V
Package Power Dissipation Capability (T _A = 25°C)	1.0 W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽²⁾	100 mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N _{END} ⁽³⁾	Endurance	1K, 10K		Cycles/Byte	MIL-STD-883, Test Method 1033
T _{DR} ⁽³⁾	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V _{ZAP} ⁽³⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I _{LTH} ⁽³⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C _{IN} ⁽³⁾	Input Pin Capacitance		6	pF	V _{IN} = 0V
C _{OUT} ⁽³⁾	Output Pin Capacitance		10	pF	V _{OUT} = 0V
C _{VPP} ⁽³⁾	V _{PP} Supply Capacitance		25	pF	V _{PP} = 0V

Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} + 1V.

CATALYST SEMICONDUCTOR

D.C. OPERATING CHARACTERISTICS

CAT28F010 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, unless otherwise specified.CAT28F010I $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		± 1.0	μA	$V_{IN} = V_{CC}$ or V_{SS} $V_{CC} = 5.5\text{V}$, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		± 10	μA	$V_{OUT} = V_{CC}$ or V_{SS} , $V_{CC} = 5.5\text{V}$, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	μA	$\overline{CE} = V_{CC} \pm 0.5\text{V}$, $V_{CC} = 5.5\text{V}$
I_{SB2}	V_{CC} Standby Current TTL		1.0	mA	$\overline{CE} = V_{IH}$, $V_{CC} = 5.5\text{V}$
I_{CC1}	V_{CC} Active Read Current		30	mA	$V_{CC} = 5.5\text{V}$, $\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{mA}$, $f = 6\text{MHz}$
$I_{CC2}^{(3)}$	V_{CC} Programming Current		15	mA	$V_{CC} = 5.5\text{V}$, Programming in Progress
$I_{CC3}^{(3)}$	V_{CC} Erase Current		15	mA	$V_{CC} = 5.5\text{V}$, Erase in Progress
$I_{CC4}^{(3)}$	V_{CC} Prog./Erase Verify Current		15	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current		± 10	μA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		200	μA	$V_{PP} = V_{PPH}$
$I_{PP2}^{(3)}$	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$, Programming in Progress
$I_{PP3}^{(3)}$	V_{PP} Erase Current		30	mA	$V_{CC} = 5.5\text{V}$, Erase in Progress
$I_{PP4}^{(3)}$	V_{PP} Prog./Erase Verify Current		5.0	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	-0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	-0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	$I_{OL} = 5.8\text{mA}$, $V_{CC} = 4.5\text{V}$
V_{IH}	Input High Level TTL	2.0	$V_{CC} + 0.5$	V	
V_{IHC}	Input High Level CMOS	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	
V_{OH}	Output High Level TTL	2.4		V	$I_{OH} = -2.5\text{mA}$, $V_{CC} = 4.5\text{V}$
V_{OH1}	Output High Level CMOS	$0.85 V_{CC}$		V	$I_{OH} = -2.5\text{mA}$, $V_{CC} = 4.5\text{V}$
V_{OH2}	Output High Level CMOS	$V_{CC} - 0.4$		V	$I_{OH} = -400\mu\text{A}$, $V_{CC} = 4.5\text{V}$
V_{ID}	A_9 Signature Voltage	11.4	13.0	V	$A_9 = V_{ID}$
I_{ID}	A_9 Signature Current		200	μA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:

(3) This parameter is tested initially and after a design or process change that affects the parameter.

CATALYST SEMICONDUCTOR

SUPPLY CHARACTERISTICS

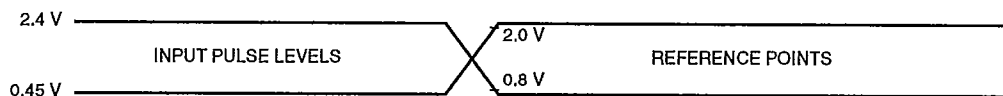
Symbol	Parameter	Limits		Unit
		Min	Max.	
V _{CC}	V _{CC} Supply Voltage	4.5	5.5	V
V _{PPL}	V _{PP} During Read Operations	0	6.5	V
V _{PPH}	V _{PP} During Read/Erase/Program	11.4	12.6	V

A.C. CHARACTERISTICS, Read Operation

CAT28F010 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.CAT28F010I T_A = -40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

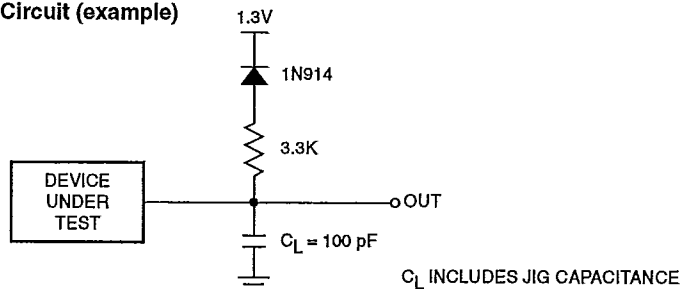
Symbol	Parameter	28F010-12 28F010I-12		28F010-15 28F010I-15		28F010-20 28F010I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	120		150		200		ns
t _{CE}	$\overline{\text{OE}}$ Access Time		120		150		200	ns
t _{ACC}	Address Access Time		120		150		200	ns
t _{OE}	$\overline{\text{OE}}$ Access Time		50		55		60	ns
t _{OH}	Output Hold from Address $\overline{\text{OE}}/\overline{\text{CE}}$ Change	0		0		0		ns
t _{OLZ} ⁽³⁾⁽⁹⁾	$\overline{\text{OE}}$ to Output in Low-Z	0		0		0		ns
t _{ILZ} ⁽³⁾⁽⁹⁾	$\overline{\text{CE}}$ to Output in Low-Z	0		0		0		ns
t _{DF} ⁽³⁾⁽⁵⁾	$\overline{\text{OE}}$ High to Output High-Z		30		35		40	ns
t _{EHQZ} ⁽³⁾⁽⁵⁾	$\overline{\text{CE}}$ High to Output High-Z		55		55		55	ns
t _{WHGL} ⁽³⁾	Write Recovery Time Before Read	6		6		6		μs

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Figure 1. A.C. Testing Input/Output Waveform⁽⁶⁾⁽⁷⁾⁽⁸⁾

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Figure 2. A.C. Testing Load Circuit (example)



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Note:

- (3) This parameter is tested initially and after a design or process change that affects the parameter.
 (5) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
 (6) Input Rise and Fall Times (10% to 90%) < 10 ns.
 (7) Input Pulse Levels = 0.45V and 2.4V.
 (8) Input and Output Timing Reference = 0.8V and 2.0V.
 (9) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

A.C. CHARACTERISTICS, Program/Erase OperationCAT28F010 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, unless otherwise specified.CAT28F010I $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, unless otherwise specified.

Symbol	Parameter	28F010-12 28F010I-12		28F010-15 28F010I-15		28F010-20 28F010I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	120		150		200		ns
t _{AS}	Address Setup Time	0		0		0		ns
t _{AH}	Address Hold Time	60		60		75		ns
t _{DS}	Data Setup Time	50		50		50		ns
t _{DH}	Data Hold Time	10		10		10		ns
t _{CS}	$\overline{\text{CE}}$ Setup Time	0		0		0		ns
t _{CH}	$\overline{\text{CE}}$ Hold Time	0		0		0		ns
t _{WP}	$\overline{\text{WE}}$ Pulse Width	60		60		60		ns
t _{WPH}	$\overline{\text{WE}}$ High Pulse Width	20		20		20		ns
t _{WPWH1} ⁽¹¹⁾	Program Pulse Width	10		10		10		μs
t _{WPWH2} ⁽¹¹⁾	Erase Pulse Width	9.5		9.5		9.5		ms
t _{WPL}	Write Recovery Time Before Read	6		6		6		μs
t _{GHWL}	Read Recovery Time Before Write	0		0		0		μs
t _{VPEL}	V _{PP} Setup Time to $\overline{\text{CE}}$	100		100		100		ns

ERASE AND PROGRAMMING PERFORMANCE⁽¹⁰⁾

Parameter	28F010-12 28F010I-12			28F010-15 28F010I-15			28F010-20 28F010I-20			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time ⁽¹²⁾⁽¹⁴⁾		1.0	10		1.0	10		1.0	30	sec
Chip Program Time ⁽¹²⁾⁽¹³⁾		2	12.5		2	12.5		2	12.5	sec

Note:

(10) Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switched, V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.

(11) Program and Erase operations are controlled by internal stop timers.

(12) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.

(13) Minimum byte programming time (excluding system overhead) is 16 μs (10 μs program + 6 μs write recovery), while maximum is 400 μs /byte (16 μs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.

(14) Excludes 00H Programming prior to Erasure.

CATALYST SEMICONDUCTOR

FUNCTION TABLE⁽¹⁵⁾

Mode	Pins					Notes
	CE	OE	WE	V _{PP}	I/O	
Read	V _{IL}	V _{IL}	V _{IH}	V _{PPL}	D _{OUT}	
Output Disable	V _{IL}	V _{IH}	V _{IH}	X	High-Z	
Standby	V _{IH}	X	X	V _{PPL}	High-Z	
Signature (MFG)	V _{IL}	V _{IL}	V _{IH}	X	31H	A ₀ = V _{IL} , A ₉ = 12V
Signature (Device)	V _{IL}	V _{IL}	V _{IH}	X	B4H	A ₀ = V _{IL} , A ₉ = 12V
Program/Erase	V _{IL}	V _{IH}	V _{IL}	V _{PPH}	D _{IN}	See Command Table
Write Cycle	V _{IL}	V _{IH}	V _{IL}	V _{PPH}	D _{IN}	During Write Cycle
Read Cycle	V _{IL}	V _{IL}	V _{IH}	V _{PPH}	D _{OUT}	During Write Cycle

WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{pp} is high and the instruction byte is latched on the rising edge of WE. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D _{IN}	Operation	Address	D _{IN}	D _{OUT}
Set Read	Write	X	00H	Read	Any		D _{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		B4H
Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	X	A0H	Read	X		D _{OUT}
Program	Write	X	40H	Write	A _{IN}	D _{IN}	
Program Verify	Write	X	C0H	Read	X		D _{OUT}
Reset	Write	X	FFH	Write	X	FFH	

Note:

(15) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

CATALYST SEMICONDUCTOR

READ OPERATIONS

Read Mode

A Read operation is performed with both \overline{CE} and \overline{OE} low and with \overline{WE} high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 17 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the \overline{CE} and \overline{OE} pins low (with \overline{WE} high), and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL} .

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7 :

CATALYST Code = 00110001 (31H)

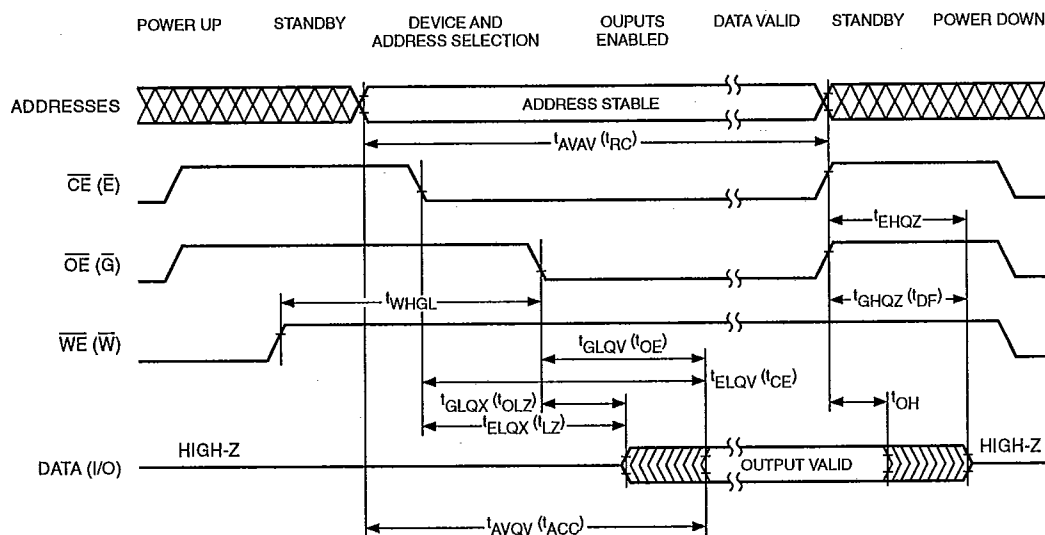
A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7 .

28F010/28F010I Code = 1011 0100 (B4H)

Standby Mode

With \overline{CE} at a logic-high level, the CAT28F010/CAT28F010I is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

Figure 3. A.C. Timing for Read Operation



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WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E²PROM Read.

Signature Mode

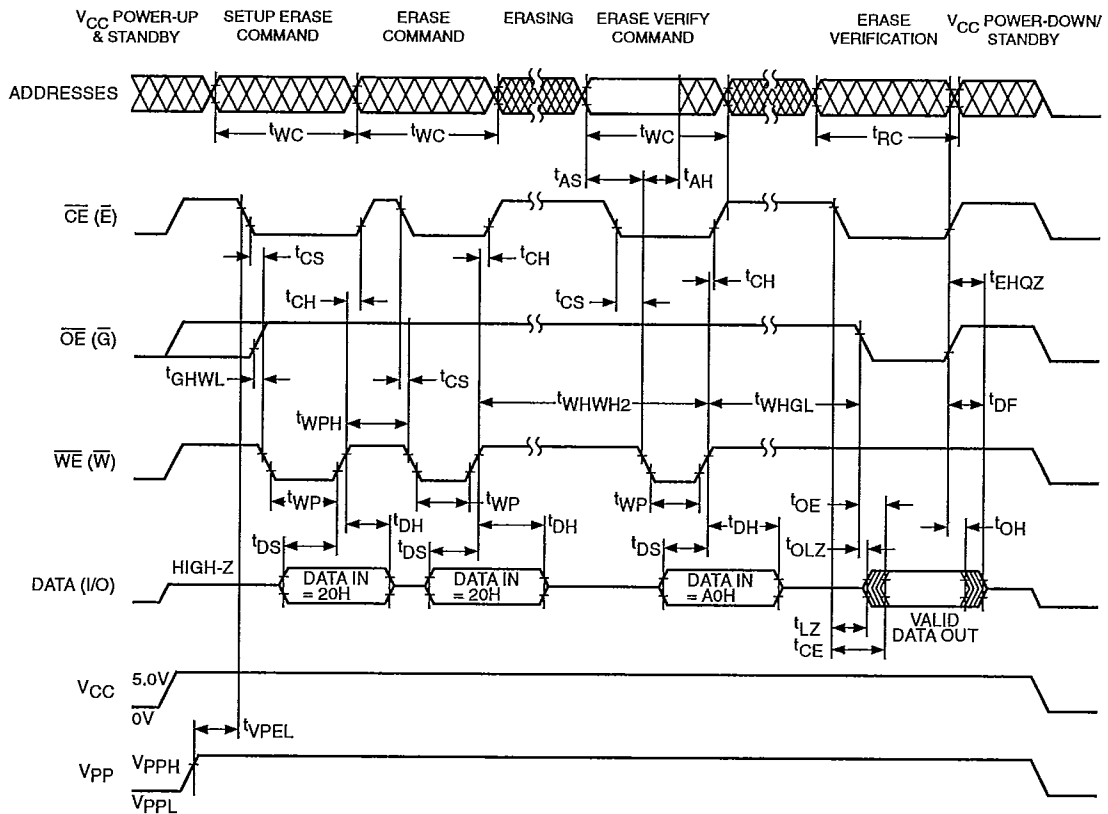
An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with \overline{CE} and \overline{OE} low (and \overline{WE} high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O₀ to I/O₇.

28F010/28F010I Code = 1011 0100 (B4H)

Figure 4. A.C. Timing for Erase Operation



5108 FHD F11

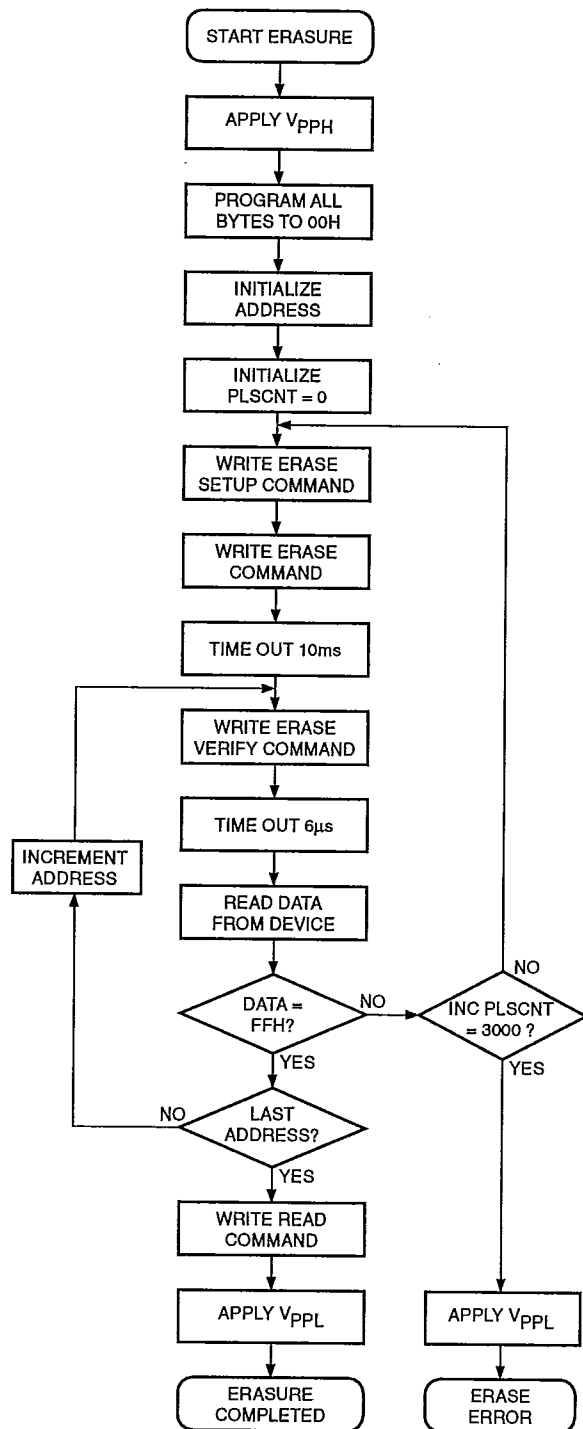
Erase Mode

During the first Write cycle, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of \overline{WE} , at which time the Erase Verify command

(A0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when \overline{WE} goes high. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

Figure 5. Chip Erase Algorithm⁽¹⁶⁾

BUS OPERATION	COMMAND	COMMENTS
STANDBY		V _{pp} RAMPs TO V _{ppH} (OR V _{pp} HARDWIRED)
		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		INITIALIZE ADDRESS
WRITE	ERASE	PLSCNT = PULSE COUNT
	ERASE	ACTUAL ERASE NEEDS 10ms PULSE, DATA = 20H
	ERASE	DATA = 20H
WRITE	ERASE VERIFY	WAIT
	ERASE VERIFY	ADDRESS = BYTE TO VERIFY DATA = 20H; STOPS ERASE OPERATION
	ERASE VERIFY	WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCREMENT PULSE COUNT
WRITE	READ	DATA = 00H RESETS THE REGISTER FOR READ OPERATION
STANDBY		V _{pp} RAMPs TO V _{pPL} (OR V _{pp} HARDWIRED)

Note:

(16) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

5108 FHD F10

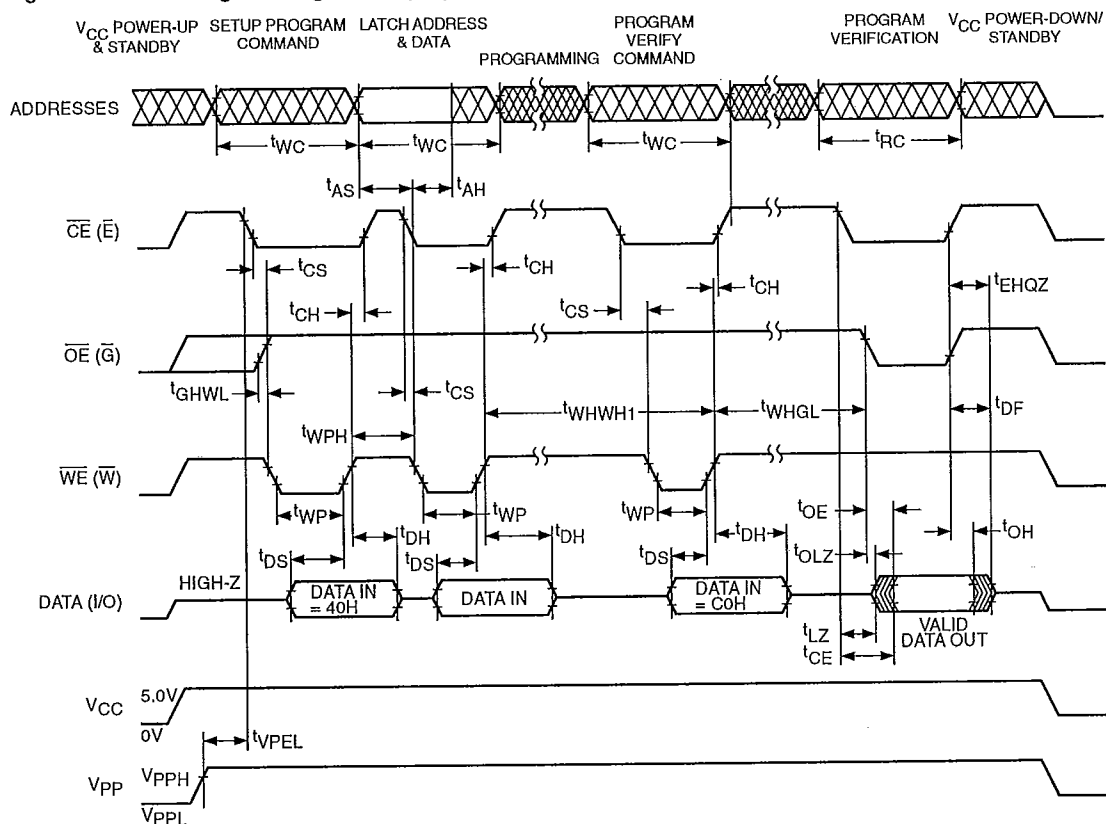
Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command

register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of \overline{WE} , while the data is latched on the rising edge of \overline{WE} . The program operation terminates with the next rising edge of \overline{WE} . An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 6. A.C. Timing for Programming Operation

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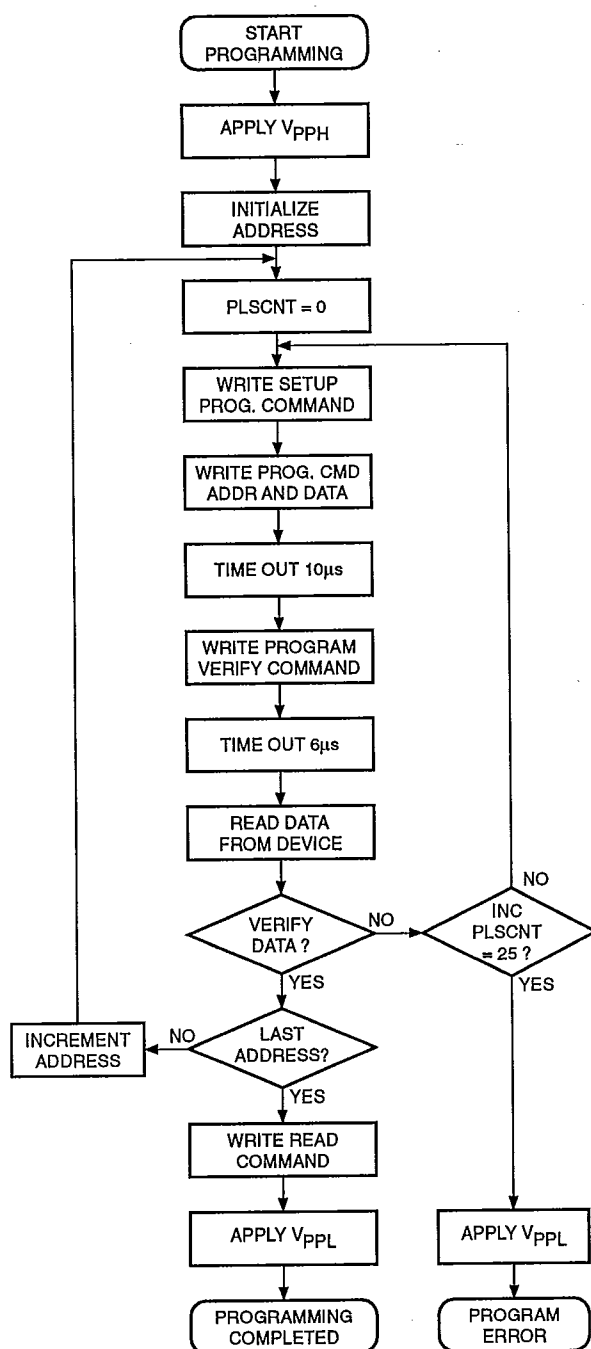
Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-

verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC} . Refer to AC Characteristics (Program/Erase) for specific timing parameters.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
tAS	tAVWL	tLZ	tELQX
tAH	tWLAX	tOE	tGLQV
tCE	tELQV	tOLZ	tGLQX
tCH	tWHEH	tRC	tAVAV
tCS	tELWL	tWC	tAVAV
tDF	tGHQZ	tWP	tWLWH
tDH	tWHDX	tWPH	tWHWL
tDS	tDVWH		

Figure 7. Programming Algorithm⁽¹⁶⁾

BUS OPERATION	COMMAND	COMMENTS
STANDBY		V _{pp} RAMPS TO V _{ppH} (OR V _{pp} HARDWIRED)
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = 40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = C0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = 00H SETS THE REGISTER FOR READ OPERATION
STANDBY		V _{pp} RAMPS TO V _{pPL} (OR V _{pp} HARDWIRED)

Note:

(16) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

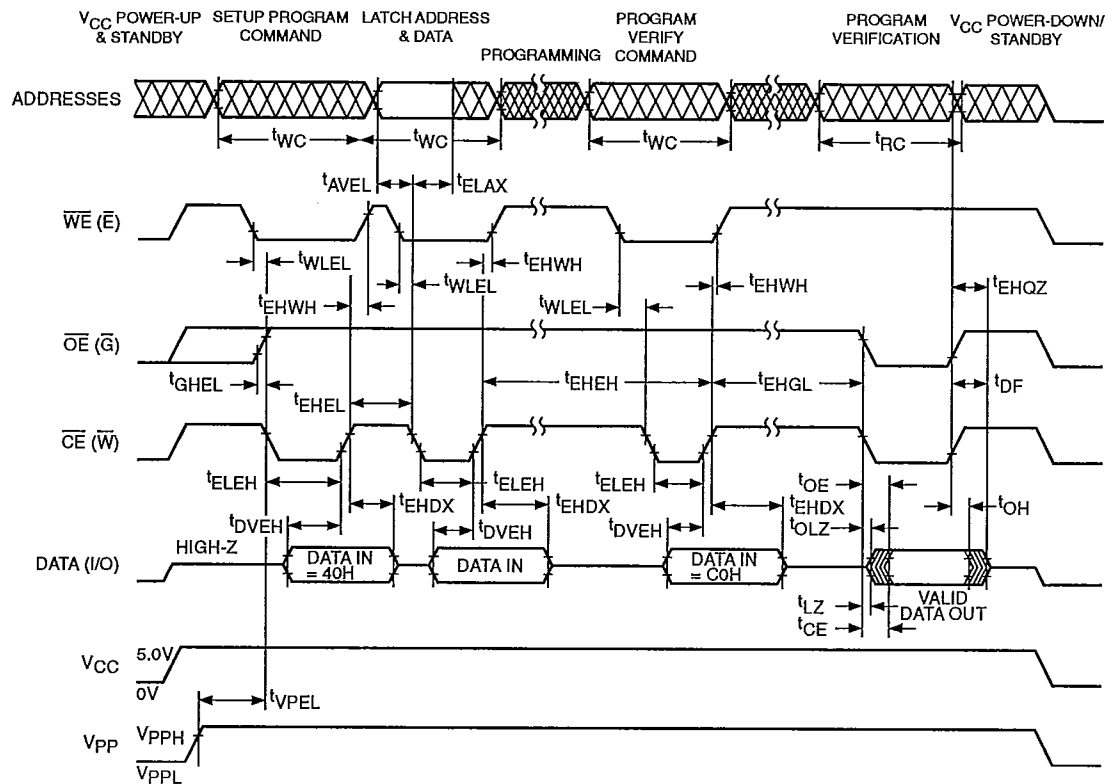
CATALYST SEMICONDUCTOR

Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with FFH on the data bus will abort an erase or a program operation. The abort/

reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

Figure 8. Alternate A.C. Timing for Program Operation



51C8 FHD F09

POWER UP/DOWN PROTECTION

The CAT28F010/CAT28F010I offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F010/CAT28F010I is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a $0.1\mu\text{F}$ ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS} . These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

TIMING PARAMETER SYMBOLS

Standard	JEDEC
t_{WC}	t_{AVAV}
t_{OLZ}	t_{GLQX}
t_{LZ}	t_{ELQX}
t_{CE}	t_{ELQV}
t_{DE}	t_{ELQV}
t_{DF}	t_{GHQZ}

CATALYST SEMICONDUCTOR

ALTERNATE \overline{CE} -CONTROLLED WRITES

Symbol	Parameter	28F010-12 28F010I-12		28F010-15 28F010I-15		28F010-20 28F010I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{AVAV}	Write Cycle Time	120		150		200		ns
t _{AVEL}	Address Setup Time	0		0		0		ns
t _{ELAX}	Address Hold Time	80		80		95		ns
t _{DVEH}	Data Setup Time	50		50		50		ns
t _{HDX}	Data Hold Time	10		10		10		ns
t _{EHGL}	Write Recovery Time Before Read	6		6		6		μs
t _{GHEL}	Read Recovery Time Before Write	0		0		0		μs
t _{WLEL}	\overline{WE} Setup Time Before \overline{CE}	0		0		0		ns
t _{EHWH}	Write Enable Hold Time	0		0		0		ns
t _{ELEH}	Write Pulse Width	70		70		80		ns
t _{EHEL}	Write Pulse Width High	20		20		20		ns
t _{VPEL}	V _{PP} Setup Time to \overline{CE} Low	1.0		1.0		1.0		μs