1.1 Scope.

This specification covers the detail requirement for a monolithic CMOS 12-bit sampling analog-to-digital converter. It features 100 ksps throughput, on board buried Zener reference and specified dynamic parameters.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD7870S(X)/883B
−2	AD7870T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Positive Supply Voltage (V_{DD}) to AGND ..... −0.3 V to +7.0 V
Negative Supply Voltage (V_{SS}) to AGND ..... +0.3 V to −7.0 V
AGND to DGND ..... −0.3 V to V_{DD} +0.3 V
Analog Input Range (V_{IN}) to AGND ..... −15.0 V to +15.0 V
Voltage Reference Output (REF OUT) to AGND ..... 0 V to V_{DD}
Digital Input Voltage to DGND ..... −0.3 V to V_{DD} +0.3 V
Digital Output Voltage to DGND ..... −0.3 V to V_{DD} +0.3 V
Thermal Resistance, Junction-to-Case (θ_{JC}) ..... See MIL-M-38510, Appendix C
Thermal Resistance, Junction-to-Ambient (θ_{JA}) ..... 120°C/W
Maximum Power Dissipation (P_D) to +75°C ..... 450 mW
Lead Temperature (Soldering 10 sec) ..... +300°C
Storage Temperature Range (T_{STG}) ..... −65°C to +150°C

1.4 Recommended Operating Conditions.

Positive Supply Voltage Range (V_{DD}) ..... +4.75 V dc to +5.25 V dc
Negative Supply Voltage Range (V_{SS}) ..... −4.75 V dc to −5.25 V dc
Analog Input Range ..... −3.0 V to +3.0 V
Ambient Operating Temperature Range ..... −55°C to +125°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-24 and E-28A
θ_{JA} = 120°C/W for Q-24 and E-28A

AD7870—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Limit Min	Limit Max	Sub Group 1	Test Condition[1, 2]/Comments $-55°C \le T_C \le +125°C$ unless otherwise noted	Units
Signal-to-Noise[3] Ratio	SNR	All	69		4, 5, 6	V_{IN} = 10 kHz Sine Wave f_{SAMPLE} = 100 kHz	dB
Total Harmonic Distortion	THD	All		−78	4, 5, 6	V_{DD} = +4.75 V, V_{SS} = −5.25 V	dB
Peak Harmonic	PH	All		−78	4, 5, 6		dB
Intermodulation Distortion (2nd Order Terms)	IMD[2]	All		−78	4, 5, 6	fa = 9 kHz; fb = 9.5 kHz; f_{SAMPLE} = 50 kHz	dB
Intermodulation Distortion (3rd Order Terms)	IMD[3]					V_{DD} = +4.75 V, V_{SS} = −5.25 V	
Track/Hold Acquisition Time[4]	t_{ACQ}	All		2	4, 5, 6	V_{DD} = +4.75 V, V_{SS} = −5.25 V	μs
Integral Linearity Error	LE	−2		±1	1, 2, 3	V_{DD} = +4.75 V, V_{SS} = −5.25 V	LSB
Differential Linearity Error	DLE	−2		±1	1, 2, 3	V_{DD} = +4.75 V, V_{SS} = −5.25 V	LSB
Bipolar Zero Error	BZE	All		±5	1, 2, 3	V_{DD} = +4.75 V, V_{SS} = −5.25 V	LSB
Positive Full-Scale Error[5]	PFSE	All		±5	1, 2, 3	V_{DD} = +4.75 V, V_{SS} = −5.25 V	LSB
Negative Full-Scale Error[5]	NFSE	All		±5	1, 2, 3	V_{DD} = +4.75 V, V_{SS} = −5.25 V	LSB
Minimum Resolution for Which No Missing Codes Are Guaranteed	NMC	All	12		1, 2, 3	V_{DD} = +4.75 V, V_{SS} = −5.25 V	Bits
Analog Input Voltage	V_{IN}	All		±3	1, 2, 3	V_{DD} = +4.75 V, V_{SS} = −5.25 V	V
Analog Input Current	I_{IN}	All		±500	1, 2, 3	V_{DD} = +5.25 V, V_{SS} = −5.25 V	μA
Voltage Reference Output	V_{REF}	All	2.99	3.01	1	V_{DD} = +5 V, V_{SS} = −5 V	V
Voltage Reference Output Temperature Coefficient	dREF/dT	−1		+60	2, 3	V_{DD} = +5 V, V_{SS} = −5 V	ppm/°C
		−2		±35			
Reference Load Sensitivity	ΔREF	All		±1	1, 2, 3	V_{DD} = +5 V, V_{SS} = −5 V Reference Load Not Changed During Conversion. Reference Load Current Change (0–500 μA)	mV
Digital Input High Voltage	V_{INH}	All	2.4		7, 8	V_{DD} = +4.75 V, V_{SS} = −5.25 V	V
Digital Input Low Voltage	V_{INL}	All		0.8	7, 8	V_{DD} = +4.75 V, V_{SS} = −5.25 V	V
Digital Input Current	I_{IN}	All		±10	1, 2, 3	V_{DD} = +5.25 V, V_{SS} = −5.25 V	μA
Digital Input Capacitance[4]	C_{IN}	All		10	4	V_{DD} = +5 V, V_{SS} = −5 V	pF
Digital Output High Voltage	V_{OH}	All	4.0		1, 2, 3	I_{SOURCE} = 40 μA V_{DD} = +4.75 V, V_{SS} = −5.0 V	V
Digital Output Low Voltage	V_{OL}	All		0.4	1, 2, 3	I_{SINK} = 1.6 mA V_{DD} = +4.75 V, V_{SS} = −5.0 V	V
Floating State Leakage Current	I_{LKG}	All		±10	1, 2, 3	DB11–DB0, V_{DD} = +5.25 V, V_{SS} = −5.25 V	μA
Floating State Output Capacitance[5]	C_{OUT}	All		15	4	V_{DD} = +5 V, V_{SS} = −5 V	pF
Conversion Time (External Clock)	t_{CONV}	All		8.0	9, 10, 11	f_{CLK} = +2.5 MHz V_{DD} = +5 V, V_{SS} = −5 V	μs
Conversion Time (Internal Clock)	t_{CONV}	All	7.0	9.0	9, 10, 11	V_{DD} = +5 V, V_{SS} = −5 V	μs

Test	Symbol	Device	Limit Min	Limit Max	Sub Group 1	Test Condition[1, 2]/Comments $-55°C \le T_C \le +125°C$ unless otherwise noted	Units
Positive Supply Current from V_{DD}	I_{DD}	All		13		V_{DD} = +5.25 V, V_{SS} = −5.25 V	mA
Negative Supply Current from V_{SS}	I_{SS}	All		6	1, 2, 3	V_{DD} = +5.25 V, V_{SS} = −5.25 V	mA
$\overline{CONVST}$ Pulse Width	t_1[4]	All	50		9, 10, 11		ns
$\overline{CS}$ to $\overline{RD}$ Setup	t_2[4]	All	0		9, 10, 11	Mode 1	ns
$\overline{RD}$ Pulse Width	t_3	All	75		9, 10, 11		ns
$\overline{CS}$ to $\overline{RD}$ Hold	t_4[4]	All	0		9, 10, 11	Mode 1	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_5[4]	All		70	9, 10, 11		ns
Data Access Time After $\overline{RD}$	t_6	All		70	9, 10, 11	Note 8	ns
Bus Relinquish Time After $\overline{RD}$	t_7	All	5	50	9, 10, 11	Note 9	ns
HBEN to $\overline{RD}$ Setup	t_8[4]	All	0		9, 10, 11		ns
HBEN to $\overline{RD}$ Hold	t_9[4]	All	0		9, 10, 11		ns
$\overline{SSTRB}$ to SCLK Falling Edge Setup	t_{10}[4]	All	100		9, 10, 11		ns
SCLK Cycle	t_{11}[4]	All	370		9, 10, 11	Note 10	ns
SCLK to Valid Data Delay	t_{12}[4]	All		150	9, 10, 11	C_L = 35 pF[11]	ns
SCLK Rising Edge to $\overline{SSTRB}$	t_{13}[4]	All	20	100	9, 10, 11		ns
Bus Relinquish Time After SCLK	t_{14}[4]	All	10	100	9, 10, 11		ns
$\overline{CS}$ to $\overline{RD}$ Setup	t_{15}[4]	All	60		9, 10, 11	Mode 2	ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	t_{16}[4]	All		120	9, 10, 11		ns
Data Setup Time Prior to $\overline{BUSY}$	t_{17}[4]	All	200		9, 10, 11		ns
$\overline{CS}$ to $\overline{RD}$ Hold	t_{18}[4]	All	0		9, 10, 11	Mode 2	ns
HBEN to $\overline{CS}$ Setup	t_{19}[4]	All	0		9, 10, 11		ns
HBEN to $\overline{CS}$ Hold	t_{20}[4]	All	0		9, 10, 11		ns

NOTES

[1]V_{DD} = +4.75 V to +5.25 V; V_{SS} = −4.75 V or −5.25 V; AGND = DGND = 0 V. Parts are guaranteed over this supply range. Unless otherwise stated tests are done at V_{DD} = 5 V, V_{SS} = −5 V.

[2]f_{CLK} = 2.5 MHz.

[3]SNR calculation includes distortion and noise components.

[4]Measured only at initial design characterization and after design or process changes which might affect this parameter. These limits are guaranteed even though they are not tested.

[5]Measured with respect to internal refernece and includes bipolar offset error.

[6]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[7]Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2 kΩ pull-up on SCLK. The capacitance on all three outputs is 35 pF.

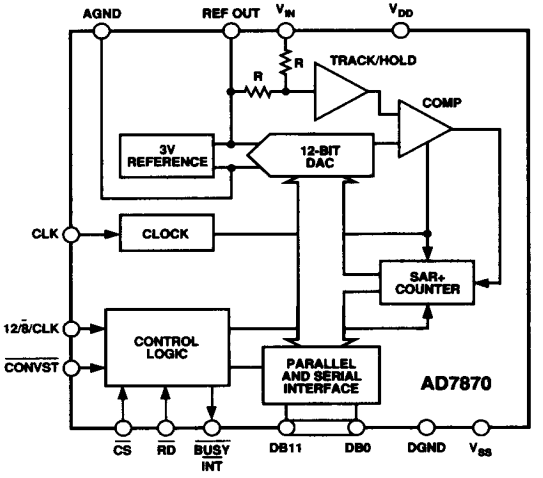
[8]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[9]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

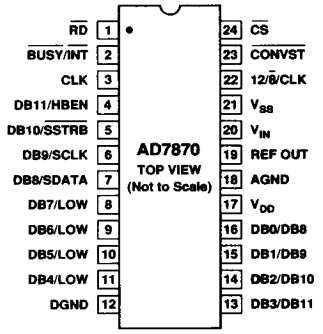
[10]SCLK mark/space ratio measured from a voltage level of 1.6 V is 40/60 to 60/40.

[11]SDATA will drive higher capacitive loads but this will add the t_{12} since it increases the external RC time circuit (4.7 kΩ‖C_L) and hence the time to reach 2.4 V.

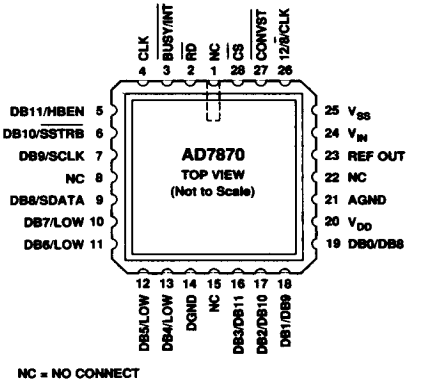
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)

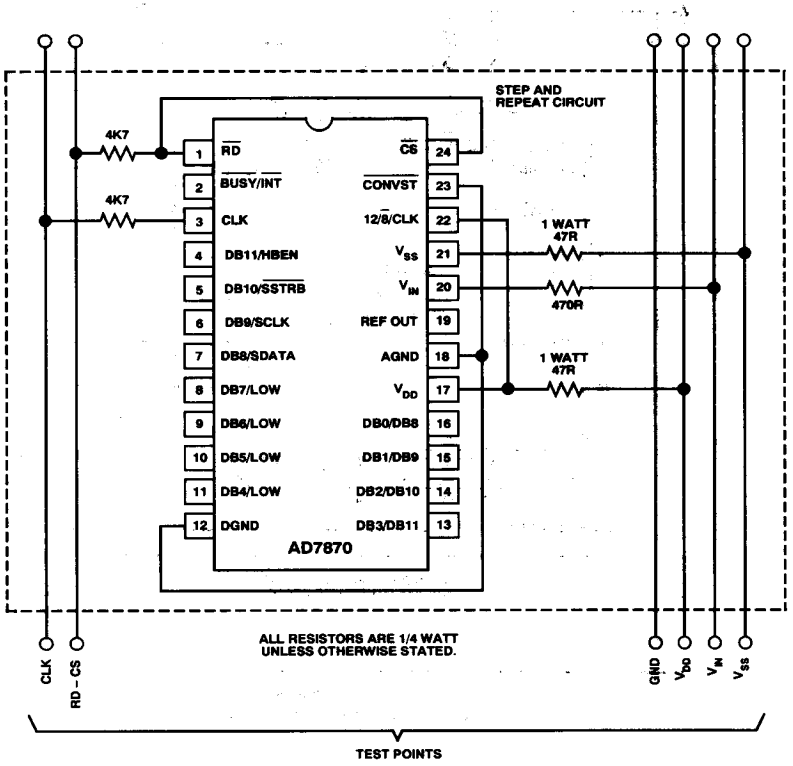


3.2.4 Microcircuit Technology Group.

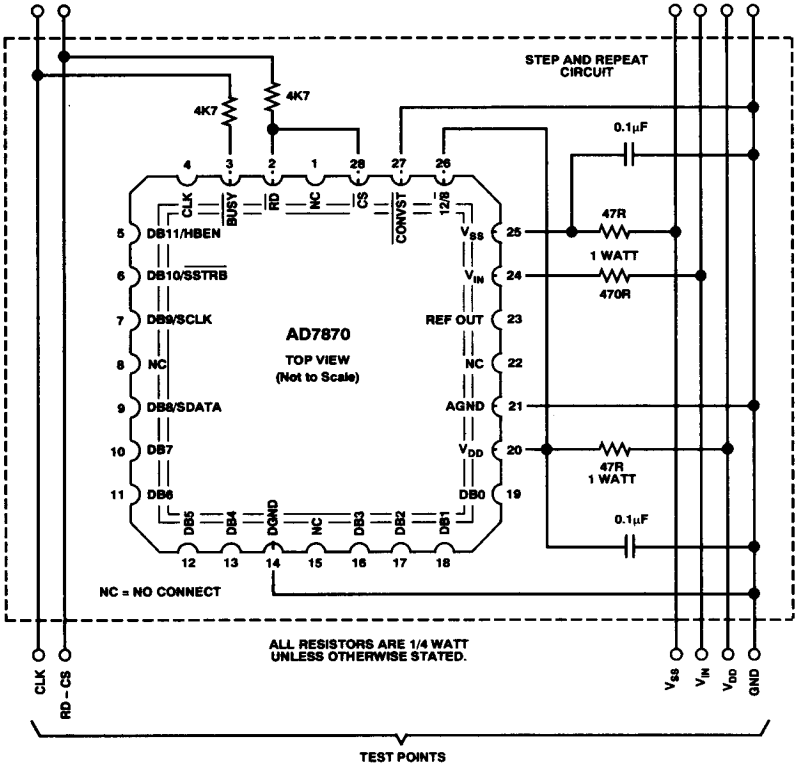
This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

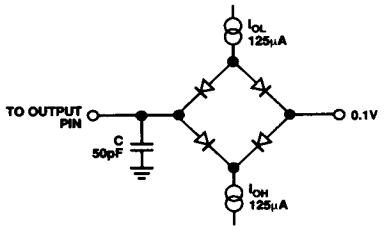
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



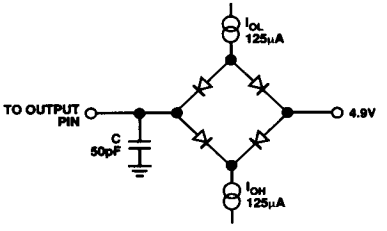
AD7870 Edge Connections (DIP)



AD7870 Edge Connections (LCC)

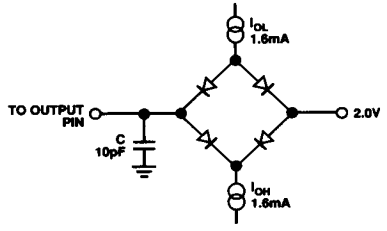


a. High Z to V_{OH}

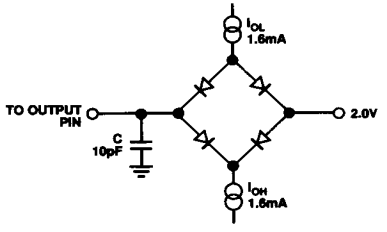


b. High Z to V_{OL}

Figure 1. Load Circuits



a. V_{OH} to High Z



b. V_{OL} to High Z

Figure 2. Load Circuits