

1.1 Scope.

This specification covers the detail requirements for a 10- and a 12-bit monolithic CMOS multiplying digital-to-analog converters.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number
-1	AD7520SQ/883B
	AD7521SQ/883B
-2	AD7520TQ/883B
	AD7521TQ/883B
-3	AD7520UQ/883B
	AD7521UQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-16 – AD7520
Q-18 – AD7521

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND		+17V
V_{REF} to GND		$\pm 25\text{V}$
Digital Input Voltage Range		V_{DD} to GND
Output Voltage (Pins 1 and 2)		-100mV to V_{DD}
Power Dissipation		
Up to $+75^\circ\text{C}$		450mW
Derates above $+75^\circ\text{C}$		6mW/ $^\circ\text{C}$
Digital Input Voltage Range		V_{DD} to GND
Operating Temperature Range		-55°C to $+125^\circ\text{C}$
Storage Temperature Range		-65°C to $+150^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-16 or Q-18
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-16 or Q-18

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AD7520				Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Test	Symbol	Device							
Resolution	RES	-1, 2, 3	10						Bits
Relative Accuracy	RA	-1	2	2	2				± LSB max
		-2	1	2	1	1			
		-3	1/2	2	1/2	1/2			
Nonlinearity Tempco	TC _{NL}	-1, 2, 3	2						± ppm/°C max
Gain Tempco	TC _{AE}	-1, 2, 3	20						± ppm/°C max
Output Leakage Current Pin 1	I _{OUT1}	-1, 2, 3	200	200	200			Digital Inputs = V _{IL} .	± nA max
Pin 2	I _{OUT2}	-1, 2, 3	200	200	200			Digital Inputs = V _{IH} .	± nA max
Output Current Settling Time ²	t _{SL}	-1, 2, 3	500					To ± 1/2LSB. All Digital Inputs V _{IL} to V _{IH} and V _{IH} to V _{IL} .	ns max
Feedthrough Error ^{2,3}	FT	-1, 2, 3	30					V _{REF} = 20V p-p, 100kHz, All Digital Input = V _{IL} .	mV p-p max
Reference Input Resistance	R _{IN}	-1, 2, 3	5 20	5 20	5 20			Measured at Pin 15.	kΩ min kΩ max
Digital Input High Voltage	V _{IH}	-1, 2, 3	2.4	2.4	2.4				V min
Digital Input Low Voltage	V _{IL}	-1, 2, 3	0.8	0.8	0.8				V max
Digital Input Leakage Current	I _{IN}	-1, 2, 3	1.0						± μA max
Output Capacitance Pin 1	C _{OUT1}	-1, 2, 3	120					All Digital Inputs V _{IH} .	pF max
Pin 2	C _{OUT2}	-1, 2, 3	37					All Digital Inputs V _{IH} .	pF max
Pin 1	C _{OUT1}	-1, 2, 3	37					All Digital Inputs V _{IL} .	pF max
Pin 2	C _{OUT2}	-1, 2, 3	120					All Digital Inputs V _{IL} .	pF max
Supply Current from V _{DD}	I _{DD}	-1, 2, 3	2	2	2			All Digital Inputs V _{IL} or V _{IH} .	mA max

NOTES

¹V_{REF} = +10V, unless otherwise stated.

²These design limits are +25°C only.

³Feedthrough error can be further minimized by connecting the metal lid to ground.

Table 1.

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AD7521 Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Resolution	RES	-1, 2, 3	12					Bits
Relative Accuracy	RA	-1	8	8	8			$\pm$ LSB max
		-2	4	8	4	4		
		-3	2	8	2	2		
Nonlinearity Tempco	TC _{NL}	-1, 2, 3	2					$\pm$ ppm/ $^{\circ}$ C max
Gain Tempco	TC _{AE}	-1, 2, 3	20					$\pm$ ppm/ $^{\circ}$ C max
Output Leakage Current Pin 1	I _{OUT1}	-1, 2, 3	200	200	200		Digital Inputs = V_{IL} .	$\pm$ nA max
Pin 2	I _{OUT2}	-1, 2, 3	200	200	200		Digital Inputs = V_{IH} .	$\pm$ nA max
Output Current Settling Time ²	t _{SL}	-1, 2, 3	500				To $\pm 1/2$ LSB. All Digital Inputs V_{IL} to V_{IH} and V_{IH} to V_{IL} .	ns max
Feedthrough Error ^{2,3}	FT	-1, 2, 3	30				$V_{REF} = 20V$ p-p, 100kHz, All Digital Input = V_{IL} .	mV p-p max
Reference Input Resistance	R _{IN}	-1, 2, 3	5 20	5 20	5 20		Measured at Pin 17.	k Ω min k Ω max
Digital Input High Voltage	V _{IH}	-1, 2, 3	2.4	2.4	2.4			V min
Digital Input Low Voltage	V _{IL}	-1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I _{IN}	-1, 2, 3	1.0					$\pm$ μ A max
Output Capacitance Pin 1	C _{OUT1}	-1, 2, 3	120				All Digital Inputs V_{IH} .	pF max
Pin 2	C _{OUT2}	-1, 2, 3	37				All Digital Inputs V_{IH} .	pF max
Pin 1	C _{OUT1}	-1, 2, 3	37				All Digital Inputs V_{IL} .	pF max
Pin 2	C _{OUT2}	-1, 2, 3	120				All Digital Inputs V_{IL} .	pF max
Supply Current from V_{DD}	I _{DD}	-1, 2, 3	2	2	2		All Digital Inputs V_{IL} or V_{IH} .	mA max

NOTES

¹ $V_{REF} = +10V$, unless otherwise stated.

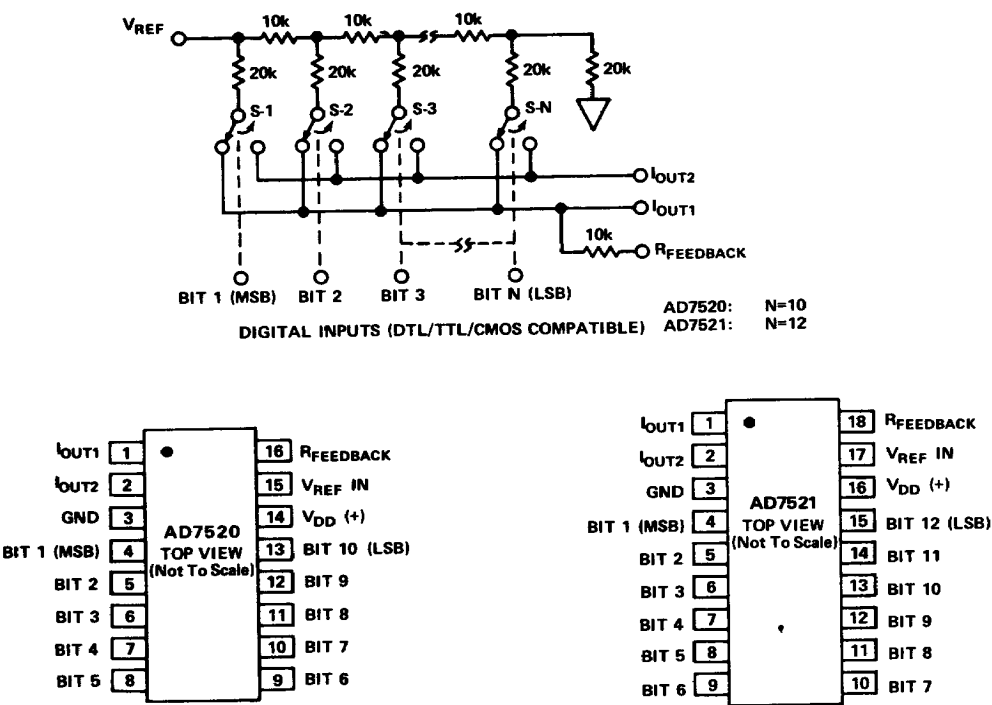
²These design limits are $+25^{\circ}$ C only.

³Feedthrough error can be further minimized by connecting the metal lid to ground.

Table 2.

AD7520/AD7521

3.2.1 Functional Block Diagram and Terminal Assignments.

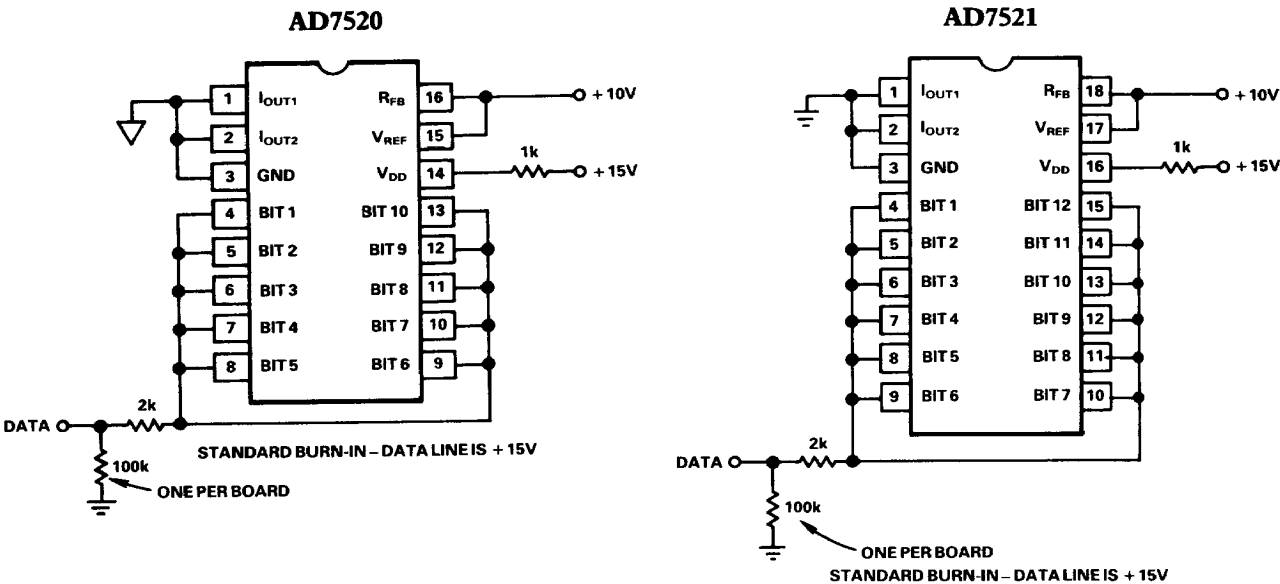


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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