REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Update boilerplate of document. Add devices 06 and 07. Add vendor CAGE 61772 as source of supply for devices 06 and 07. Editorial changes throughout.	93-11-15	M. A. Frye
D	Changes in accordance with NOR 5962-R187-95	95-08-14	M. A. Frye
E	Updated boilerplate to one-part, one-part number format. Added provisions for the inclusion of radiation-hardened devices. - glg	00-01-21	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	E	E	E	E	E	E	E	E	E	E									
SHEET	15	16	17	18	19	20	21	22	23	24									

REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
8 November 1989

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 4K X 9 FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89568**

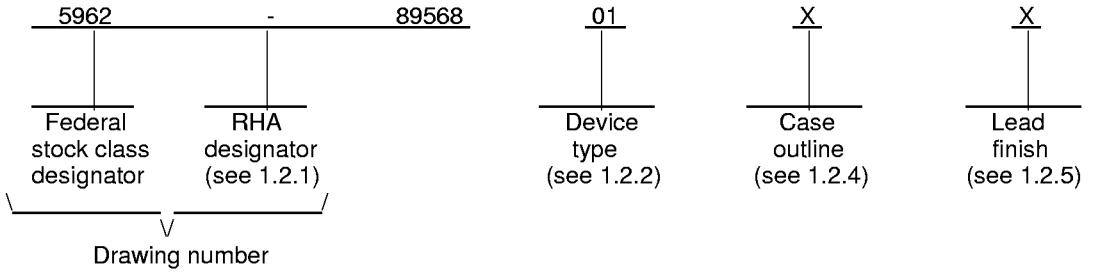
SHEET 1 OF 24

1. SCOPE

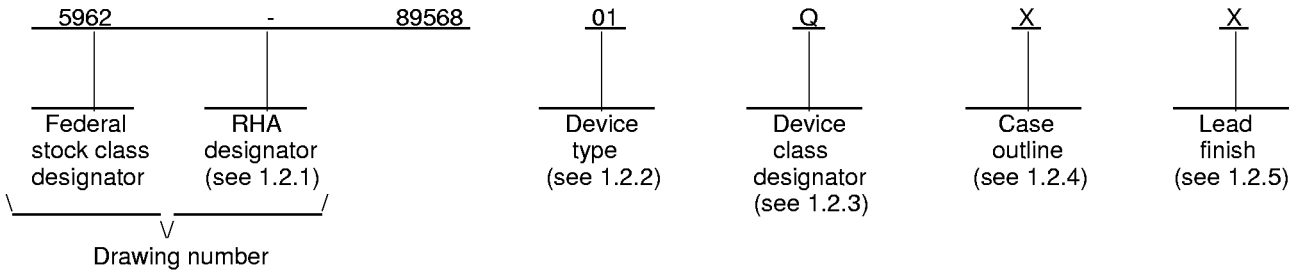
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

For device classes M and Q not using class designator in the PIN:



For device classes Q and V where class designator is included in the PIN:



1.2.1 (RHA) designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7204	4K X 9-bit parallel FIFO	120 ns
02	7204	4K X 9-bit parallel FIFO	80 ns
03	7204	4K X 9-bit parallel FIFO	65 ns
04	7204	4K X 9-bit parallel FIFO	50 ns
05	7204	4K X 9-bit parallel FIFO	40 ns
06	7204	4K X 9-bit parallel FIFO	30 ns
07	7204	4K X 9-bit parallel FIFO	20 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as listed below. Since the device class designator for some M and Q level devices was established after this drawing was developed, the class designator will not be specified in the part number and will not be marked on the parts.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	GDFP2-F28	28	Flat pack
Z	CQCC1-N32	32	Rectangular leadless chip carrier
U	GDIP4-T28 or CDIP3-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings.

Terminal voltage with respect to ground	-0.5 V dc to +7.0 V dc
DC output current	50 mA
Storage temperature range	-65°C to +155°C
Maximum power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C 1/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	2.2 V dc minimum 2/
Input low voltage (V_{IL})	0.8 V dc maximum 3/
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	4/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

1/ Maximum junction temperature may be increased to +175°C during burn-in and steady state life.
2/ V_{IH} is 2.2 V minimum for all input pins except $\overline{XT}$, which is 3.5 V minimum.
3/ 1.5 V undershoots are allowed for 10 ns once per cycle.
4/ Values will be added when they become available.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's)
MIL-HDBK-780 - Standard Microcircuit Drawings

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition C or D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	$0.0 V \le V_{IN} \le V_{CC}$	1, 2, 3	All	-10	10	µA
		M, D, P	1 1/		2/	2/	
Output leakage current	I_{LO}	$0.0 V \le V_{OUT} \le V_{CC}$, $\overline{R} \ge V_{IH}$	1, 2, 3	All	-10	10	µA
		M, D, P	1 1/		2/	2/	
Output low voltage	V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 8.0$ mA $V_{IL} = 0.8$ V, $V_{IH} = 2.2$ V	1, 2, 3	All		0.4	V
		M, D, P	1 1/			2/	
Output high voltage	V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -2.0$ mA $V_{IL} = 0.8$ V, $V_{IH} = 2.2$ V	1, 2, 3	All	2.4		V
		M, D, P	1 1/		2/		
Operating supply current	I_{CC1}	$f = f_S$, outputs open, $V_{CC} = 5.5$ V	1, 2, 3	01-04, 06,07		150	mA
		M, D, P	1 1/			2/	
		f = 15.3 MHz, outputs open, $V_{CC} = 5.5$ V	1, 2, 3	05		150	
		M, D, P	1 1/			2/	
Standby current	I_{CC2}	$\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$, outputs open	1, 2, 3	All		25	mA
		M, D, P	1 1/			2/	
Power down current	I_{CC3}	All inputs = V_{CC} - 0.2 V, outputs open	1, 2, 3	All		4	mA
		M, D, P	1 1/			2/	
Input capacitance	C_{IN}	$V_I = 0.0$ V, f = 1 MHz $T_A = +25°C$, See 4.4.1e	4	01-05		8	pF
				06,07		10	
Output capacitance	C_{OUT}	$V_O = 0.0$ V, f = 1 MHz $T_A = +25°C$, See 4.4.1e	4	All		12	pF
Functional tests		See 4.4.1c.	7, 8A, 8B				
		M, D, P	7 1/		2/	2/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Shift frequency	f_S	C_L = 30 pF, See figures 3 and 4		9, 10, 11	01		7.0	MHz
					02		10	
					03		12.5	
					04		15	
					05		20	
					06		25	
					07		33.3	
			M, D, P	9 1/			2/	
Read cycle time	t_{RC}			9, 10, 11	01	140		ns
					02	100		
					03	80		
					04	65		
					05	50		
					06	40		
					07	30		
			M, D, P	9 1/		2/		
Access time	t_A			9, 10, 11	01		120	ns
					02		80	
					03		65	
					04		50	
					05		40	
					06		30	
					07		20	
			M, D, P	9 1/			2/	
Read recovery time	t_{RR}			9, 10, 11	01,02	20		ns
					03,04	15		
					05-07	10		
			M, D, P	9 1/		2/		
Read pulse width	t_{RPW}			9, 10, 11	01	120		ns
					02	80		
					03	65		
					04	50		
					05	40		
					06	30		
					07	20		
			M, D, P	9 1/		2/		
Read pulse low to data bus at low-Z	t_{RLZ} 3/			9, 10, 11	01-04	10		ns
					05-07	5.0		
			M, D, P	9 1/		2/		
Write pulse low to data bus at low-Z	t_{WLZ} 3/ 4/			9, 10, 11	01-04, 06,07	5.0		ns
					05	10		
			M, D, P	9 1/		2/		
Data valid from read pulse high	t_{DV}			9, 10, 11	All	5.0		ns
			M, D, P	9 1/		2/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Read pulse high to data bus high-Z	t_{RHZ} 3/	C_L = 30 pF, See figures 3 and 4		9, 10, 11	01		35	ns
					02-04		30	
					05		25	
					06		20	
					07		15	
			M, D, P	9 1/			2/	
Write cycle time	t_{WC}			9, 10, 11	01	140		ns
					02	100		
					03	80		
					04	65		
					05	50		
					06	40		
					07	30		
			M, D, P	9 1/		2/		
Write pulse width	t_{WPW}			9, 10, 11	01	120		ns
					02	80		
					03	65		
					04	50		
					05	40		
					06	30		
					07	20		
			M, D, P	9 1/		2/		
Write recovery time	t_{WR}			9, 10, 11	01,02	20		ns
					03,04	15		
					05-07	10		
			M, D, P	9 1/		2/		
Data setup time	t_{DS}			9, 10, 11	01,02	40		ns
					03,04	30		
					05	20		
					06	18		
					07	12		
			M, D, P	9 1/		2/		
Data hold time	t_{DH}			9, 10, 11	01-03	10		ns
					04	5		
					05-07	0		
			M, D, P	9 1/		2/		
Reset cycle time	t_{RSC}			9, 10, 11	01	140		ns
					02	100		
					03	80		
					05	50		
					06	40		
					07	30		
			M, D, P	9 1/		2/		
Reset pulse width	t_{RS}			9, 10, 11	01	120		ns
					02	80		
					03	65		
					04	50		
					05	40		
					06	30		
					07	20		
			M, D, P	9 1/		2/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Reset recovery time	t_{RSR}	C_L = 30 pF, See figures 3 and 4.		9, 10, 11	01,02	20		ns
					03,04	15		
					05-07	10		
			M, D, P	9 1/		2/		
Reset setup time	t_{RSS} 3/			9, 10, 11	01	120		ns
					02	80		
					03	65		
					04	50		
					05	40		
					06	30		
					07	20		
			M, D, P	9 1/		2/		
Retransmit cycle time	t_{RTC}			9, 10, 11	01	140		ns
					02	100		
					03	80		
					04	65		
					05	50		
					06	40		
					07	30		
			M, D, P	9 1/		2/		
Retransmit pulse width	t_{RT} 3/			9, 10, 11	01	120		ns
					02	80		
					03	65		
					04	50		
					05	40		
					06	30		
					07	20		
Retransmit recovery time	t_{RTR}			9, 10, 11	01,02	20		ns
					03,04	15		
					05-07	10		
			M, D, P	9 1/		2/		
Reset to empty flag low	t_{EFL}			9, 10, 11	01		140	ns
					02		100	
					03		80	
					04		65	
					05		50	
					06		40	
					07		30	
			M, D, P	9 1/			2/	
Read low to empty flag low	t_{REF}			9, 10, 11	01-03		60	ns
					04		45	
					05		35	
					06		30	
					07		20	
			M, D, P	9 1/			2/	
Read high to full flag high	t_{RFF}			9, 10, 11	01-03		60	ns
					04		45	
					05		35	
					06		30	
					07		20	
			M, D, P	9 1/			2/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Write high to empty flag high	t_{WEF}	C_L = 30 pF, See figures 3 and 4.		9, 10, 11	01-03		60	ns
					04		45	
					05		35	
					06		30	
					07		20	
			M, D, P	9 1/			2/	
Write low to full flag low	t_{WFF}			9, 10, 11	01-03		60	ns
					04		45	
					05		35	
					06		30	
					07		20	
			M, D, P	9 1/			2/	
Reset to half-full and full flag high	t_{HFH} t_{FFH}			9, 10, 11	01		140	ns
					02		100	
					03		80	
					04		65	
					05		50	
					06		40	
					07		30	
			M, D, P	9 1/			2/	
Expansion out low delay from clock	t_{XOL}			9, 10, 11	01		120	ns
					02		80	
					03		65	
					04		50	
					05		40	
					06		30	
					07		20	
			M, D, P	9 1/			2/	
Expansion out high delay from clock	t_{XOH}			9, 10, 11	01		120	ns
					02		80	
					03		65	
					04		50	
					05		40	
					06		30	
					07		20	
			M, D, P	9 1/			2/	
$\overline{XI}$ pulse width	t_{XI}			9, 10, 11	01	120		ns
					02	80		
					03	65		
					04	50		
					05	40		
					06	30		
					07	20		
			M, D, P	9 1/		2/		
$\overline{XI}$ recovery time	t_{XIR}			9, 10, 11	All	10		ns
			M, D, P	9 1/		2/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
$\overline{XI}$ set-up time	t_{XIS}			9, 10, 11	01-05	15		ns
					06,07	10		
			M, D, P	9 1/		2/		
Retransmit setup time	t_{RTS} 1/			9, 10, 11	01	120		ns
					02	80		
					03	65		
					04	50		
					05	40		
					06	30		
					07	20		
			M, D, P	9 1/		2/		
Read pulse width after $\overline{EF}$ high	t_{RPE}			9, 10, 11	01	120		ns
					02	80		
					03	65		
					04	50		
					05	40		
					06	30		
					07	20		
			M, D, P	9 1/		2/		
Write low to half-full flag low	t_{WHF}			9, 10, 11	01		140	ns
					02		100	
					03		80	
					04		65	
					05		50	
					06		40	
					07		30	
			M, D, P	9 1/			2/	
Read high to half-full flag high	t_{RHF}			9, 10, 11	01		140	ns
					02		100	
					03		85	
					04		65	
					05		50	
					06		40	
					07		30	
			M, D, P	9 1/			2/	
Write pulse width after $\overline{FF}$ high	t_{WPF}			9, 10, 11	01	120		ns
					02	80		
					03	65		
					04	50		
					05	40		
					06	30		
					07	20		
			M, D, P	9 1/		2/		

1/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$. The M, D, and P in the test condition column are the postirradiation limits for the device types specified in the device types column.
2/ Preirradiation values for RHA marked devices shall also be the postirradiation values unless otherwise specified.
3/ If not tested, shall be guaranteed to the limits specified in table I.
4/ Only applies to read data flow-through mode.

Device types	All	
Case outlines	X,Y and U	Z
Terminal number	Terminal symbol	
1	$\overline{W}$	NC
2	D_8	$\overline{W}$
3	D_3	D_8
4	D_2	D_3
5	D_1	D_2
6	D_0	D_1
7	$\overline{XT}$	D_0
8	$\overline{FF}$	$\overline{XT}$
9	Q_0	$\overline{FF}$
10	Q_1	Q_0
11	Q_2	Q_1
12	Q_3	NC
13	Q_8	Q_2
14	GND	Q_3
15	$\overline{R}$	Q_8
16	Q_4	GND
17	Q_5	NC
18	Q_6	$\overline{R}$
19	Q_7	Q_4
20	$\overline{XO}/\overline{HF}$	Q_5
21	$\overline{EF}$	Q_6
22	$\overline{RS}$	Q_7
23	$\overline{FL}/\overline{RT}$	$\overline{XO}/\overline{HF}$
24	D_7	$\overline{EF}$
25	D_6	$\overline{RS}$
26	D_5	$\overline{FL}/\overline{RT}$
27	D_4	NC
28	V_{CC}	D_7
29	---	D_6
30	---	D_5
31	---	D_4
32	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Reset and retransmit
Single device configuration/width expansion mode

Mode	Inputs			Internal status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/write	1	1	0	Increment 1/	Increment 1/	X	X	X

1/ Pointer will increment if flag is high.

Reset and first load
Depth expansion/compound expansion mode

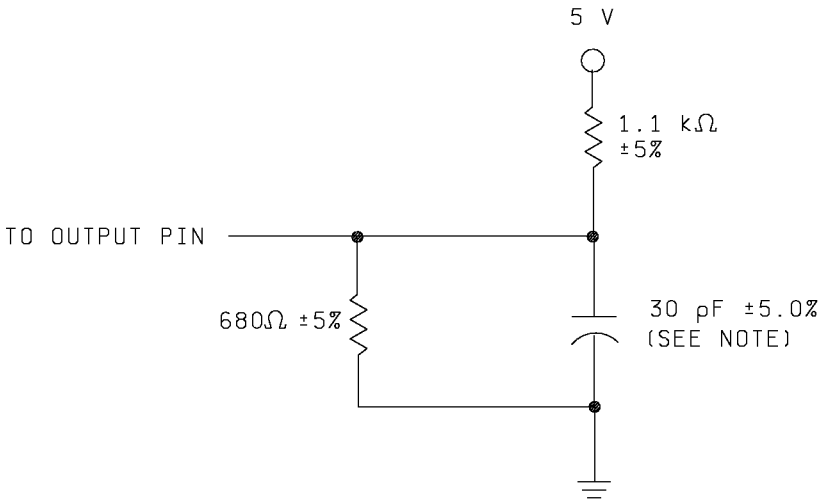
	Inputs			Internal status		Outputs	
Mode	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$
Reset first device	0	0	1/	Location zero	Location zero	0	1
Reset all other devices	0	1	1/	Location zero	Location zero	0	1
Read/write	1	X	1/	X	X	X	X

1/ $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

NOTES: $\overline{RS}$ = Reset input, $\overline{FL}/\overline{RT}$ = First load/retransmit $\overline{EF}$ = Empty flag output,
$\overline{FF}$ = Full flag output, $\overline{XI}$ = Expansion input, and $\overline{HF}$ = Half-full flag output
0 = Low level voltage
1 = High level voltage
X = Don't care

FIGURE 2. Truth tables.

OUTPUT LOAD CIRCUIT (OR EQUIVALENT)



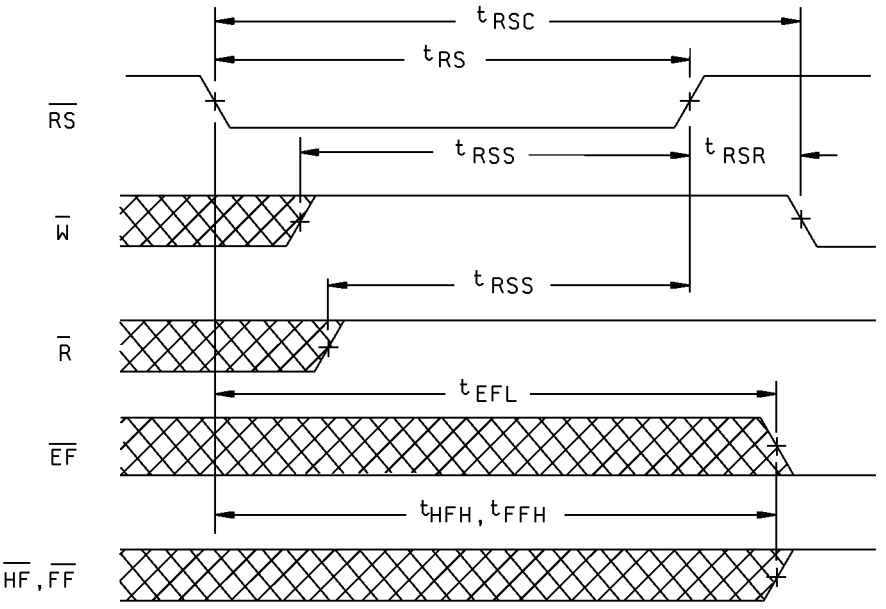
NOTE: C_L includes scope and jig capacitance.

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and ac test conditions.

RESET TIMING (SEE NOTES 1 AND 2)



ASYNCHRONOUS WRITE AND READ OPERATION TIMING

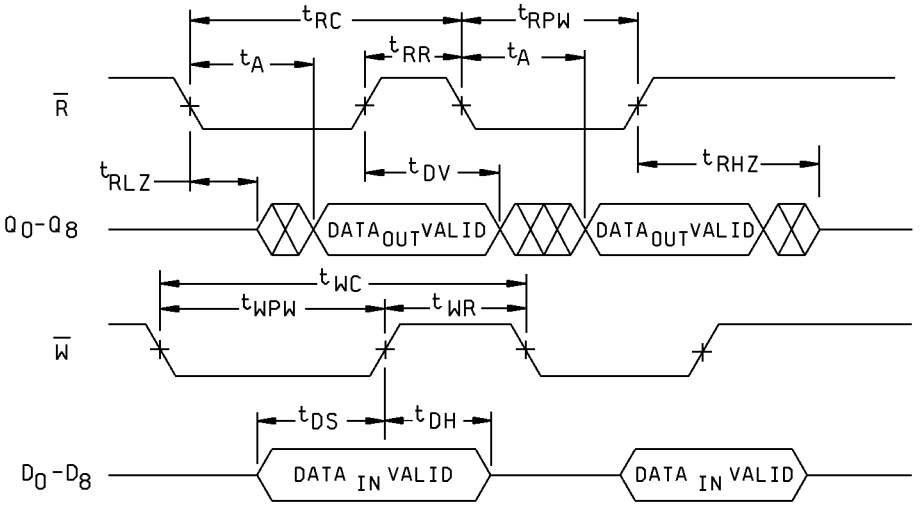
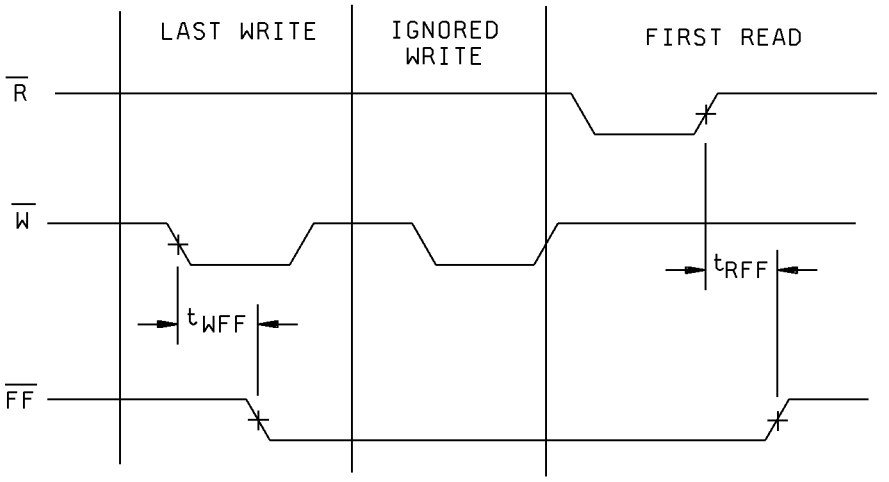


FIGURE 4. Timing waveforms.

FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE TIMING

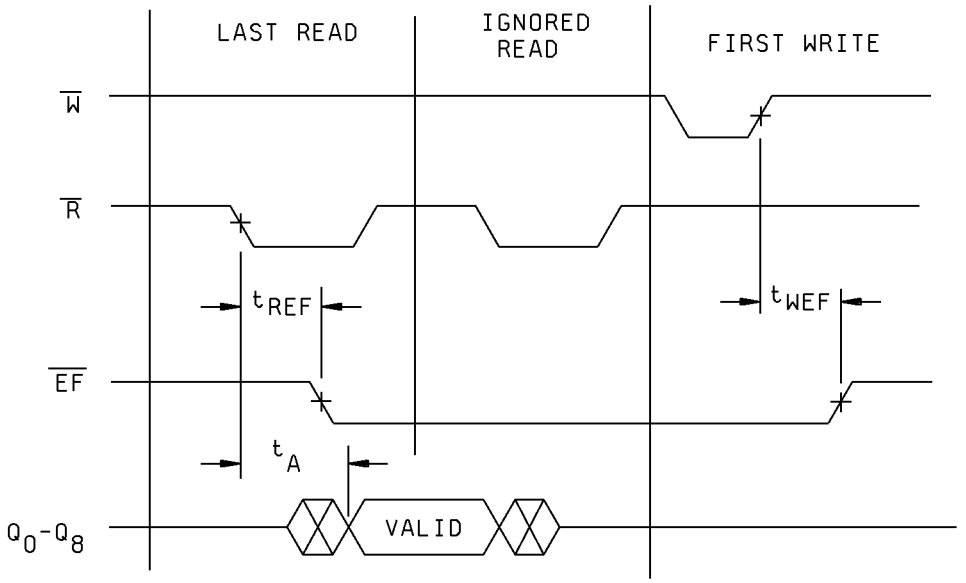
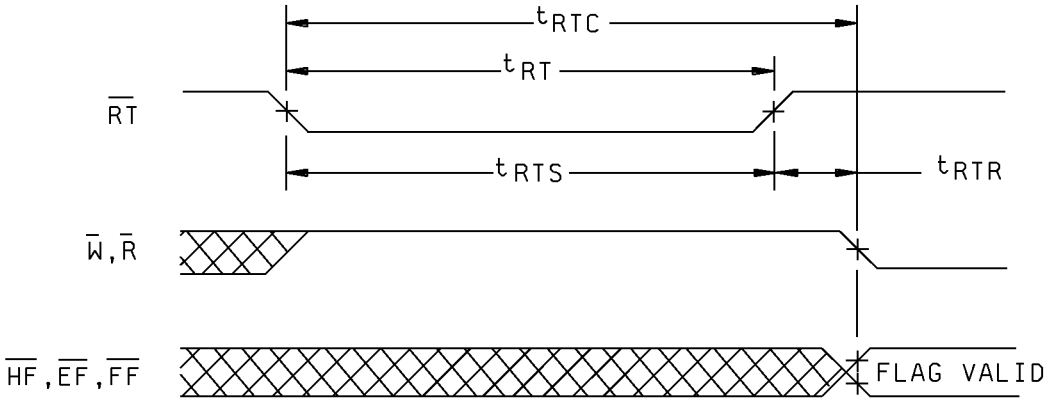
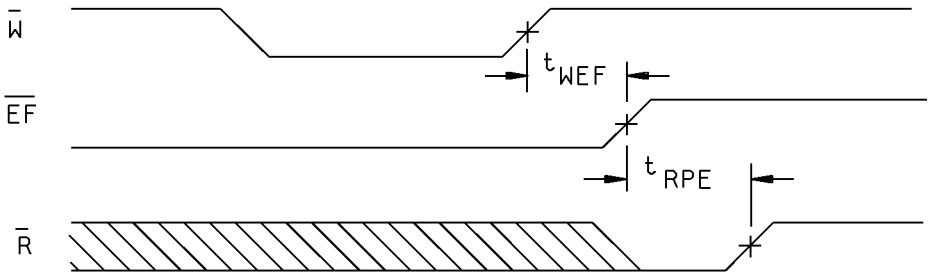


FIGURE 3. Timing waveforms - Continued.

RETRANSMIT TIMING (SEE NOTE 3)



EMPTY FLAG TIMING



FULL FLAG TIMING

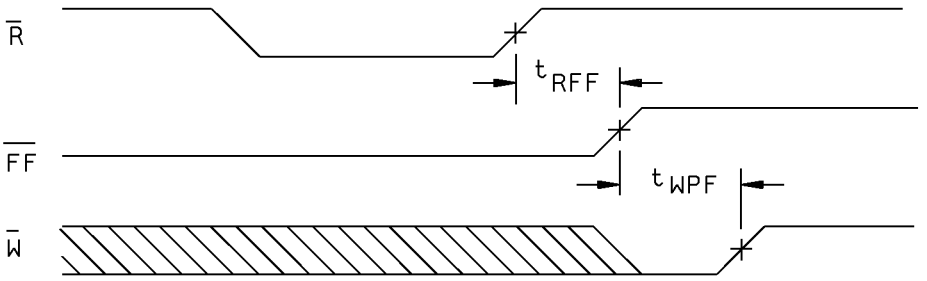


FIGURE 3. Timing waveforms - Continued.

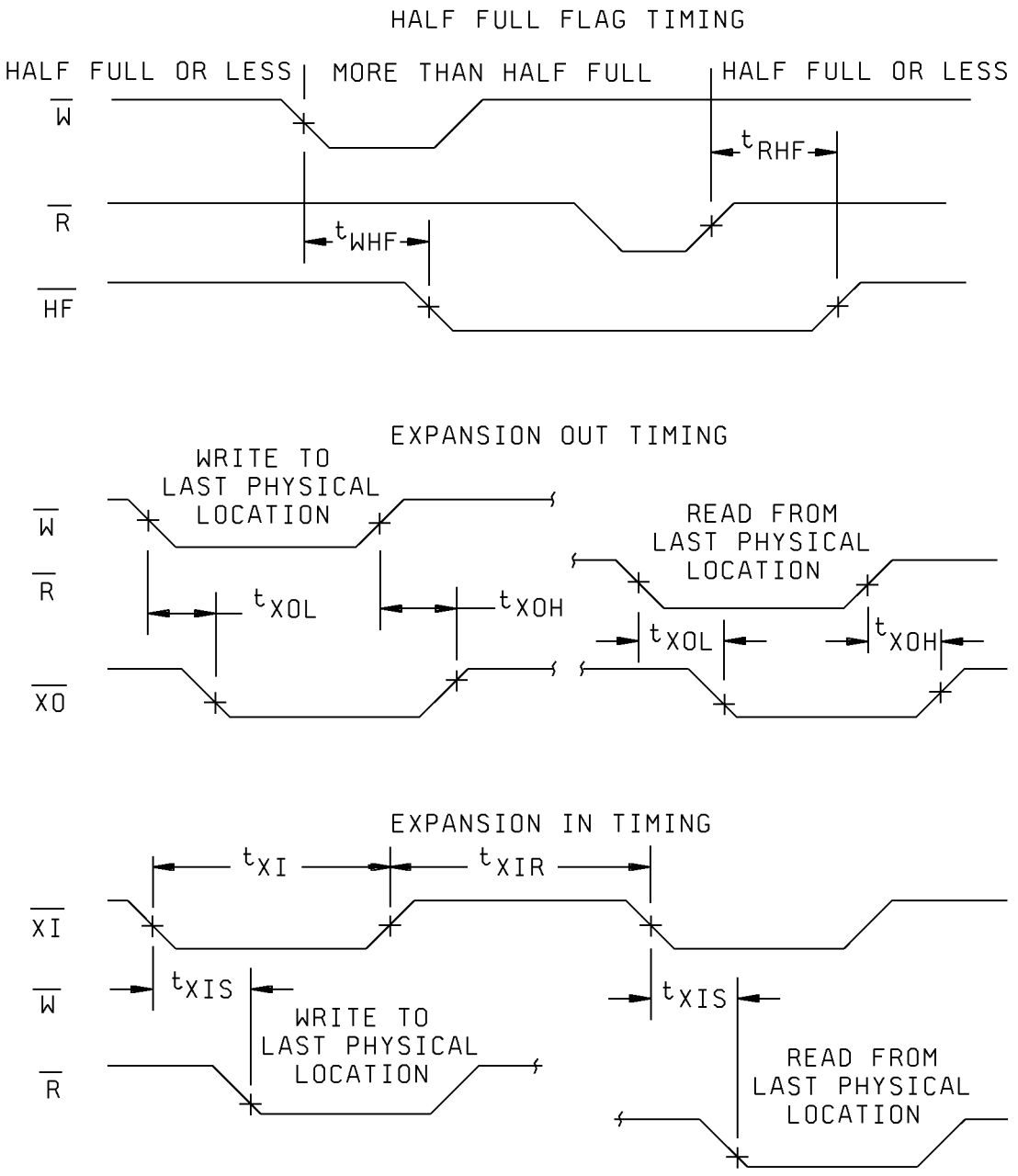
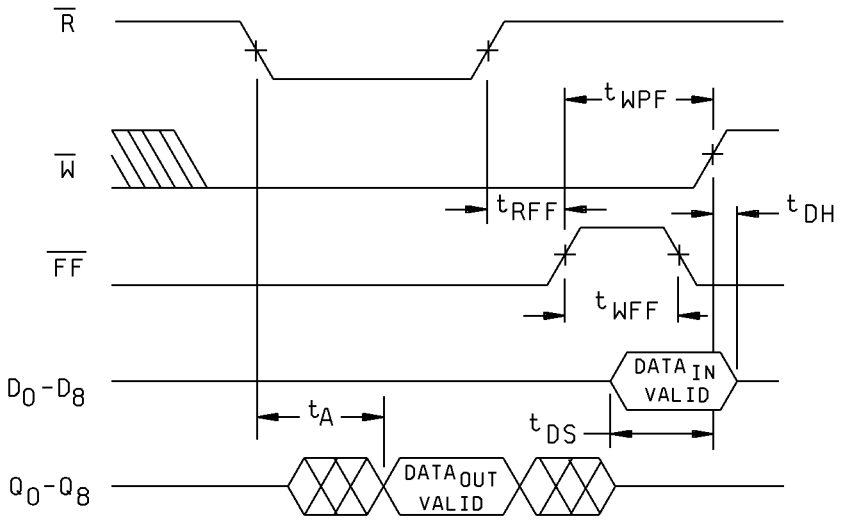
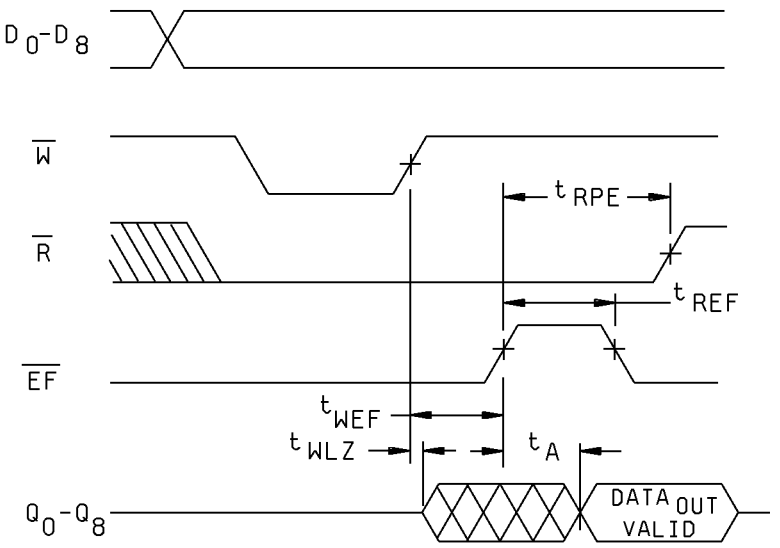


FIGURE 3. Timing waveforms - Continued.

WRITE DATA FLOW - THROUGH MODE TIMING



READ DATA FLOW - THROUGH MODE TIMING



NOTES:
1. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.
3. During Retransmit, $\overline{EF}$, $\overline{FF}$, and $\overline{HF}$ may change status, but flags will be valid at t_{RTC}.

FIGURE 4. Timing waveforms - continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)	Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I method 1015	Not required	Not required	Not required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10,11	1*,2,3,7*, 8A,8B,9,10,11	1*,2,3,7*, 8A,8B,9,10,11
7	Group A test requirements	1,2,3,4**,7,8A, 8B,9,10,11	1,2,3,4**,7, 8A,8B,9,10,11	1,2,3,4**,7, 8A,8B,9,10,11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroups 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).For device classes Q and V performance of delta limits shall be as specified in the manufacturer's QM plan.
7/ See 4.4.1d.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC2}, I_{CC3}	±10% of specified value in table I.
I_{LI}, I_{LO}	±10% of specified value in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein. Test shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 3.14 V dc for the upset measurements and V_{DD} = 3.46 V dc for the latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits see table IB herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

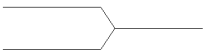
6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331, and as follows.

C_{IN} ..... Input terminal capacitance.
C_{OUT} ..... Output and bidirectional output terminal capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{LI} ..... Input leakage current.
I_{LO} ..... Output leakage current.
T_C ..... Case temperature.
V_{CC} ..... Positive supply voltage.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 00-01-21

Approved sources of supply for SMD 5962-89568 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535 .

Standardized military drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-8956801XA	61772 2/	IDT7204L120DB MM1I-67204-55MB
5962-8956801YA	61772	IDT7204L120XEB
5962-8956801ZA	61772 2/	IDT7204L120LB MM4J-67204-55MB
5962-8956802XA	61772 2/	IDT7204L80DB MM1I-67204-55MB
5962-8956802YA	61772	IDT7204L80XEB
5962-8956802ZA	61772 2/	IDT7204L80LB MM4J-67204-55MB
5962-8956803XA	61772 2/	IDT7204L65DB MM1I-67204-55MB
5962-8956803YA	61772	IDT7204L65XEB
5962-8956803ZA	61772 2/	IDT7204L65LB MM4J-67204-55MB
5962-8956804XA	61772 2/ 2/	IDT7204L50DB MM1I-67204-45MB AM7204A-50BXA
5962-8956804UA	61772	IDT7204L50TDB
5962-8956804YA	61772	IDT7204L50XEB
5962-8956804ZA	61772 2/ 2/	IDT7204L50LB MM4J-67204-45MB AM7204A-50BUA
5962-8956804QYA	0HGZ7	MMDP67204EV-50MQ
5962-8956804VYA	0HGZ7	MMDP67204EV-50SV

See footnote at end of list.

Standardized military drawing PIN 1/	Vendor CAGE number 2/	Vendor similar PIN 3/
5962-8956805XA	61772 2/ 2/	IDT7204L40DB MM1I-67204-35MB AM7204A-40BXA
5962-8956805UA	61772	IDT7204L40TDB
5962-8956805YA	61772	IDT7204L40XEB
5962-8956805ZA	61772 2/ 2/	IDT7204L40LB MM4J-67204-35MB AM7204A-40BUA
5962-8956805QUA	0HGZ7	MMCP67204EV-40MQ
5962-8956805VUA	0HGZ7	MMCP67204EV-40SV
5962-8956805QYA	0HGZ7	MMDP67204EV-40MQ
5962-8956805VYA	0HGZ7	MMDP67204EV-40SV
5962-8956806XA	61772	IDT7204L30DB
5962-8956806YA	61772	IDT7204L30XEB
5962-8956806ZA	61772	IDT7204L30LB
5962-8956806UA	61772	IDT7204L30TDB
5962-8956806QUA	0HGZ7	MMCP67204EV-30MQ
5962-8956806VUA	0HGZ7	MMCP67204EV-30SV
5962-8956806QYA	0HGZ7	MMCP67204EV-30MQ
5962-8956806VYA	0HGZ7	MMCP67204EV-30SV
5962-8956807XA	61772	IDT7204L20DB
5962-8956807YA	61772	IDT7204L20XEB
5962-8956807ZA	61772	IDT7204L20LB
5962-8956807UA	61772	IDT7204L20TDB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ No longer available from an approved source.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Incorporated 2975 Stender Way Santa Clara, CA 95054-8015
0HGZ7	TEMIC MHS BP70602 La chantrerie 44306 NANTES CEDEX 3 - France U.S.A point of contact: TEMIC 2325 Orchard Parkway San Jose, CA 95131

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