16-BIT MONOLITHIC TRACKING RESOLVER-TO-DIGITAL CONVERTER

DESCRIPTION

The RD-19230 is a versatile, low cost, state-of-the-art 16-bit monolithic Resolver-to-Digital Converter. This single chip converter offers programmable features such as resolution, bandwidth, velocity output scaling and encoder emulation.

Resolution programming allows selection of 10, 12, 14, or 16-bit, with accuracies to 2.3 min. The parallel digital data and the internal encoder emulation signals (A QUAD B) have independent resolution control. Internal encoder emulation will permit inhibiting (freezing) the parallel digital data without interrupting the A and B outputs.

The internal Synthesized Reference section eliminates errors due to quadrature voltage and ensures operation with a rotor-to-stator phase shift of up to 45 degrees. The velocity output (VEL) can be used in place of a tachometer. It has a range of ±4 V relative to analog ground. The velocity scale factor/tracking rate is programmed with a single resistor. This converter provides the option of using a second set of filter components which can be used in dual bandwidth or switch on the fly applications.

The RD-19230 is available with operating temperature ranges of 0° to +70°C and -40° to +85°C.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the RD-19230 converter is ideal for use in modern high performance industrial control systems. It is ideal for users who wish to use a resolver input in their encoder based system. Typical applications include motor control, machine tool control, robotics, and process control.

FEATURES

- ***Accuracy up to 2.3 arc minutes***
- ***Internal Synthesized Reference***
- ***+5 Volt Only Option***
- ***Programmable Resolution, Bandwidth and Tracking Rate***
- ***Internal Encoder Emulation with Independent Resolution Control***
- ***Differential Resolver Input Mode***
- ***Velocity Output Eliminates Tachometer***
- ***Built-In-Test (BIT) Output, No 180° Hangup***
- ***-40° to +85°C Operating Temperature***

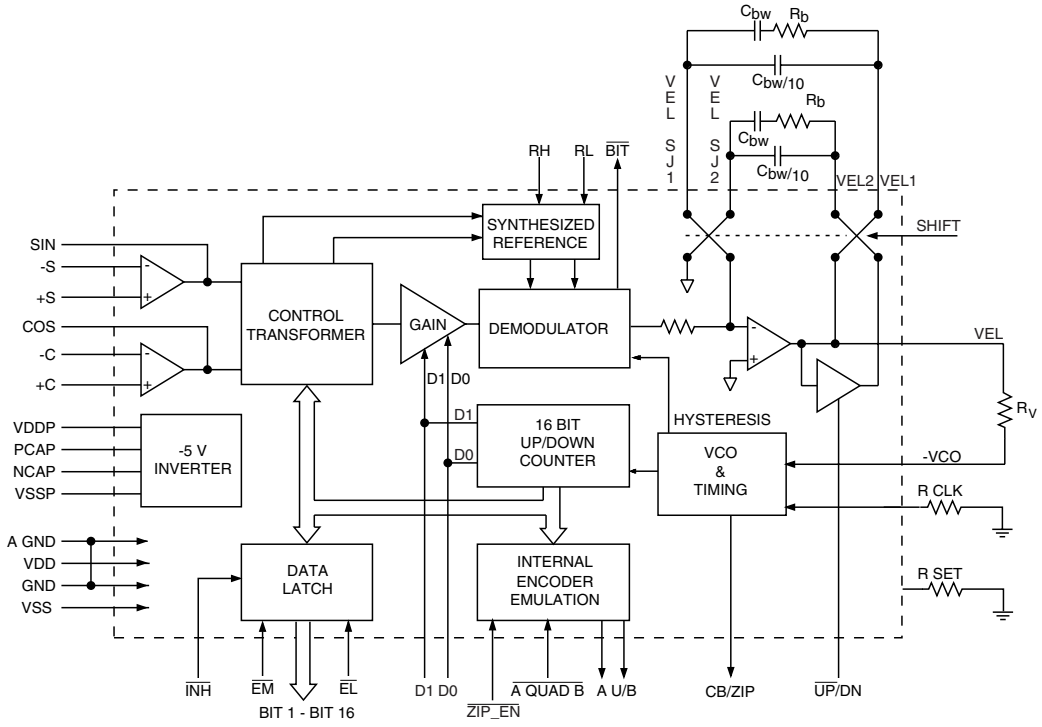

FIGURE 1. RD-19230 SERIES BLOCK DIAGRAM

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TABLE 1. RD-19230 SPECIFICATIONS

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion.

PARAMETER	UNIT	VALUE		
RESOLUTION	Bits	10, 12, 14, or 16 (note 1 & 2)		
FREQUENCY RANGE	Hz	**47-1k[4]**	**1k - 4k**	**4k - 10k**
ACCURACY -XX2	Min	4 +1 LSB	4 +1 LSB	5 +1 LSB
-XX3 (note 3)	Min	2 +1 LSB	2 +1 LSB	3 +1 LSB
REPEATABILITY	LSB	±1	±1	± 2
DIFFERENTIAL LINEARITY	LSB	±1	±1	± 2
REFERENCE		(+REF, -REF)		
Type		Differential		
Voltage: differential	Vp-p	±10 max.		
single ended	Vp	±5 max.		
overload	Vrms	±25 continuous; ±100 transient		
Frequency	Hz	DC to 10k		
Input Impedance	Ω	10M min. ‖ 20 pf		
SYNTHESIZED REFERENCE		(note 5)		
±Sig/Ref Phase Shift Correction	deg	45 max. from 400 Hz to 10kHz		
SIGNAL INPUT		(+S, -S, SIN, +C, -C, COS)		
Type		Resolver, differential, groundbased		
Voltage: operating	Vrms	2 ±15%		
overload	Vrms	±25 continuous		
Input impedance	Ω	10M min ‖ 10 pF.		
DIGITAL INPUTS				
TTL / CMOS Compatible Inputs		Logic 0 = 0.8 V max. Logic 1 = 2.0 V min. Loading = 10 µA max P.U. current source to +5 V ‖ 5 pF max. CMOS transient protected		
Inhibit ($\overline{INH}$)		Logic 0 inhibits; Data stable within 150 ns		
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables; Data stable within 150 ns		
Enable Bits 9 to 16 ($\overline{EL}$)		Logic 1 = High Impedance; Data High Z within 100 ns		
Resolution and Mode Control (D1 & D0) (See notes 1 & 2)		**Mode** **D1** **D0** **Resolution** resolver 0 0 10 bits 0 1 12 bits 1 0 14 bits 1 1 16 bits LVDT -5V 0 8 bits 0 -5V 10 bits 1 -5V 12 bits -5V -5V 14 bits		
$\overline{ZIP\_EN}$		Logic 0 enables ZIP Logic 1 enables CB		
CMOS Compatable Inputs		Logic 0 = 1.5 V max. Logic 1 = 3.5 V min. negative voltage = -3.5 V min.		
SHIFT		Logic 1 select VEL1 components Logic 0 select VEL2 components		
$\overline{UP}$/DN		Logic 1 will increase gain by 4 Logic 0 will decrease gain by 4 -5 V gain remains constant		
$\overline{A\ QUAD\ B}$		Logic 0 enables encoder emulation Falling edge latches encoder resolution		

TABLE 1. RD-19230 SPECIFICATIONS (CONTINUED)

PARAMETER	UNIT	VALUE			
DIGITAL OUTPUTS					
Parallel Data (1-16)		10, 12, 14, or 16 parallel lines; natural binary angle positive logic (see note 2)			
Converter Busy (CB)		0.25 to 0.75 µs positive pulse leading edge initiates counter update. (CB functions with $\overline{ZIP\_EN}$ pin tied to +5 V or NC)			
Zero Index Pulse (ZIP)		Logic 1 at all 0's ($\overline{ZIP\_EN}$ pin tied to GND)			
Built-In-Test ($\overline{BIT}$)		Logic 0 for BIT condition. ~ ±100 LSB's of error with a filter of 500 µs, Loss of Signal (LOS) less than 500 mV, or Loss of Reference (LOR) less than 500 mV			
A, B		Incremental Encoder Output			
Drive Capability		50 pF+ Logic 0: 1 TTL load, 1.6 mA at 0.4 V max. Logic 1; 10 TTL loads, -0.4 mA at 2.8 V min. Logic 0; 100 mV max. driving CMOS Logic 1; +5 V supply minus 100 mV min. driving CMOS High Z; 10 µA ‖ 5 pF max.			
DYNAMIC CHARACTERISTICS		(at maximum bandwidth)			
Resolution	bits	**10**	**12**	**14**	**16**
Tracking Rate (min)(note 6)	rps	1152	288	72	18
Bandwidth (Closed Loop)	Hz	1200	1200	600	300
Ka	$1/sec^2$	5.7M	5.7M	1.4M	360k
A1	1/sec	19.5	19.5	4.9	1.2
A2	1/sec	295k	295k	295k	295k
A	1/sec	2400	2400	1200	600
B	1/sec	1200	1200	600	300
Acceleration (1 LSB lag)	deg/s^2	2M	500k	30k	2k
Settling Time (179° step)	msec	2	8	20	50
VELOCITY CHARACTERISTICS					
Polarity		Positive for increasing angle			
Voltage Range (Full Scale)	V	±4 (at nominal power supply)			
Scale Factor Error	%	10 typ		20 max	
Scale Factor TC	PPM/°C	100 typ		200 max	
Reversal Error	%	0.75 typ		1.3 max	
Linearity	%	0.25 typ		0.50 max	
Zero Offset	mV	5 typ		10 max	
Zero Offset TC	µV/°C	15 typ		30 max	
Load	kΩ			8 max	
POWER SUPPLIES		(note 6)			
Nominal Voltage	V	+5 (VDD)		-5 (VSS)	
Voltage Range	%	±5		±5	
Max Volt. w/o Damage	V	+7		-7	
Current	mA	25 max. (each)			
TEMPERATURE RANGE					
Operating					
-30X	°C	0 to +70			
-20X	°C	-40 to +85			
Storage	°C	-40 to +85			
PHYSICAL CHARACTERISTICS					
Size: 64-pin Quad Flat Pack	in(mm)	0.52 x 0.52 (13.2 x 13.2)			
WEIGHT					
	oz(g)	0.018 (0.5)			

TABLE 1 notes:

1. Unused data bits are set to logic "0."
2. In LVDT mode, Bit 3 is the MSB and resolution is programmable to 8,10, 12, and 14 bits.
3. Accuracy in LVDT mode is 0.15% + 1 LSB of full scale.
4. In the frequency range of 47Hz to 1kHz, there will be 1 LSB of jitter at quadrant boundaries.
5. The maximum phase shift tolerance will degrade linearly from 45 degrees at 400 Hz to 30 degrees at 60 Hz.
6. When using the -5V inverter, the V_{DD} supply current will double and V_{SSP} can be up to 20% low, or -4V.
7. || = in parallel with.

THEORY OF OPERATION

The RD-19230 is a mixed signal CMOS IC containing analog input and digital output sections. Precision analog circuitry is merged with digital logic to form a complete high-performance tracking resolver-to-digital converter. For user flexibility and convenience, the converter bandwidth, dynamics, and velocity scaling are externally set with passive components.

FIGURE 1 is the Functional Block Diagram of RD-19230. The analog conversion electronics require ±5 VDC power supplies, and the converter contains a charge pump to provide the user with the option of a single-ended +5 VDC supply. The converter front-end consists of differential sine and cosine input amplifiers which are protected up to ±25 V with 2 kΩ resistors and diode clamps to the ±5 VDC supplies. By performing the following trigonometric identity, $SIN\theta(COS\phi) - COS\theta(SIN\phi) = SIN(\theta-\phi)$, the Control Transformer (CT) compares the analog input signals (θ) with the digital output (ϕ), resulting in an error signal proportional to the sin of the angular difference. The CT uses a combination of amplifiers, switches, logic and capacitors in precision ratios to perform the calculation.

Note: The error output of the CT is normally sinusoidal, but in LVDT mode, it is triangular (linear) and can be used to convert any linear transducer output.

The converter accuracy is limited by the precision of the computing elements in the CT. Instead of a traditional precision resistor network, this converter uses capacitors with precisely controlled ratios. Sampling techniques are used to eliminate errors due to voltage drift and op-amp offsets.

The error processing is performed using the industry standard technique for Type II tracking converters. The DC error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a Type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above. The settings of the various error processor gains and break frequencies are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

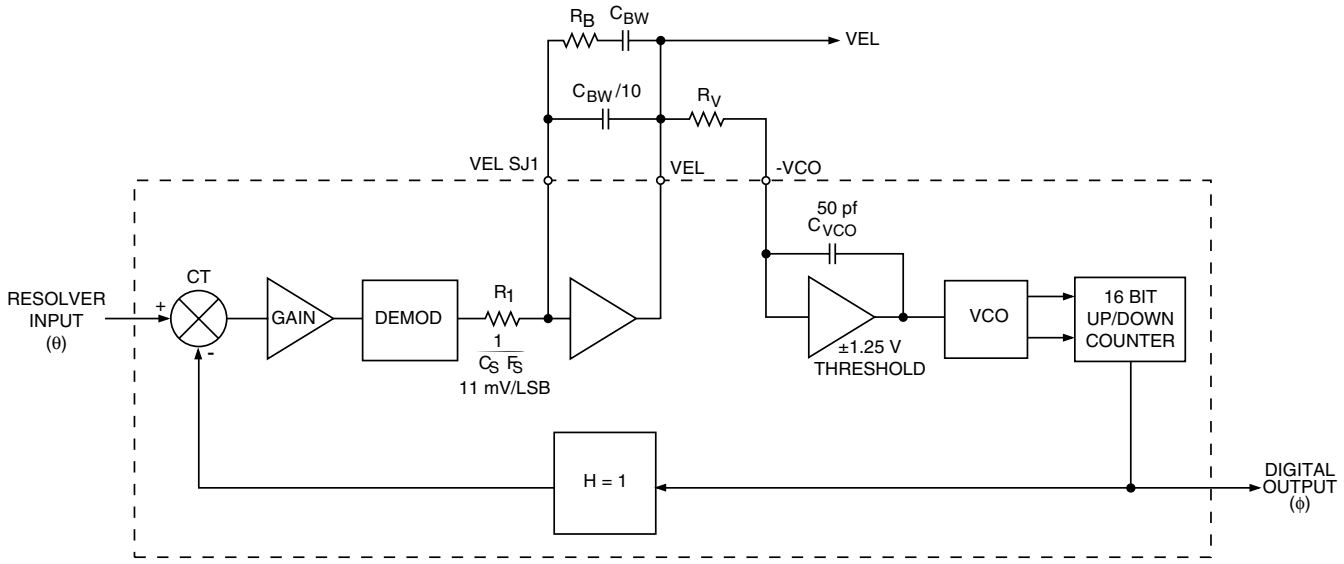


FIGURE 2. TRANSFER FUNCTION BLOCK DIAGRAM #1

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Transfer Function Block Diagrams and Bode Plots (open and closed loop). These are shown in FIGURES 2, 3, and 4.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient and $A^2=A_1A_2$
and B is the frequency of lead compensation.

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT + Error Amp + Demod with 2 Vrms input)

- Integrator Gain = $\frac{Cs\ Fs}{1.1\ C_{BW}}$ volts per second per volt

- VCO Gain = $\frac{1}{1.25\ R_V\ C_{VCO}}$ LSBs per second per volt

where: Cs = 10 pF
Fs = 67 kHz when R CLK = 30 kΩ
C_{VCO} = 50 pF

R_V, R_B, and C_{BW} are selected by the user to set velocity scaling and bandwidth.

GENERAL SETUP CONDITIONS

DDC has external component selection software which considers all the criteria below. In a simple fashion, it asks the key system parameters (carrier frequency, resolution, bandwidth, and tracking rate) needed to derive the external component values.

The following recommendations should be considered when installing the RD-19230 R/D converter:

1) In setting the bandwidth (BW) and Tracking Rate (TR) (selecting five external components), the system requirements need to be considered. For the greatest noise immunity, select the minimum BW and TR the system will allow. Selecting a f_{BW} that is too low relative to the maximum application tracking rate can create a spin-around condition in which the converter never settles. The relationship to insure against this condition is detailed in TABLE 2.

2) Power supplies are ±5 VDC. For lowest noise performance it is recommended that a 0.1 µF or larger cap be connected from each supply to ground near the converter package.

3) Resolver inputs and velocity output are referenced to AGND. This pin should be connected to GND near the converter package. Digital currents flowing through ground will not disturb the analog signals.

4) This device has several high impedance amplifier inputs (+C, -C, +S, -S, -VCO, VEL SJ1, and VEL SJ2) that are sensitive to noise coupling. External components should be connected as close to the converter as possible.

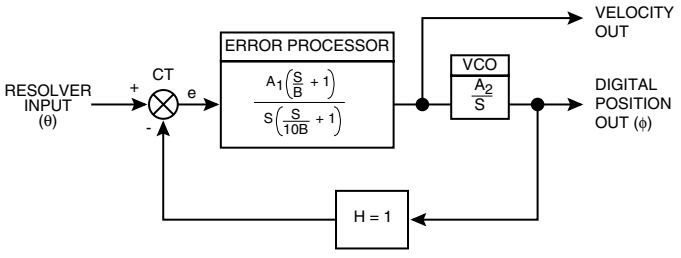


FIGURE 3. TRANSFER FUNCTION BLOCK DIAGRAM #2

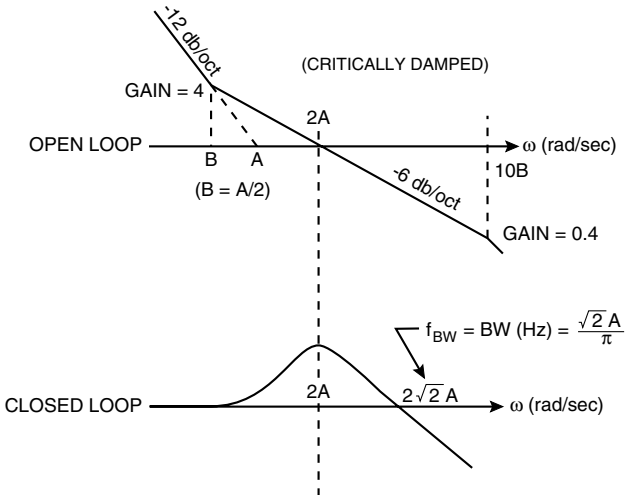


FIGURE 4. BODE PLOTS

5) Setup of bandwidth and velocity scaling for the optimized critically damped case should proceed as follows:

· Select the desired f_{BW} (closed loop) based on overall system dynamics.

· Select $f_{carrier} \geq 3.5 f_{BW}$

· Select the applications tracking rate (in accordance with TABLE 3), and use appropriate values for R SET and R CLK

· Compute $Rv = \frac{\text{Full Scale Velocity Voltage}}{\text{Tracking Rate (rps)} \times 2^{\text{resolution}} \times 50\text{ pF} \times 1.25\text{ V}}$

· Compute $C_{BW}\text{ (pF)} = \frac{3.2 \times Fs\text{ (Hz)} \times 10^8}{Rv \times (f_{BW})^2}$

· Where Fs = 67 kHz for R CLK = 30 KΩ
100 kHz for R CLK = 20 KΩ
125 kHz for R CLK = 15 KΩ

· Compute $R_B = \frac{0.9}{C_{BW} \times f_{BW}}$

· Compute $\frac{C_{BW}}{10}$

As an example:

Calculate component values for a 16 bit converter with 100Hz bandwidth, a tracking rate of 10 RPS and a full scale velocity of 4 Volts.

- $Rv = \frac{4\text{ V}}{10\text{ rps} \times 2^{16} \times 50\text{ pF} \times 1.25\text{ V}} = 97655\ \Omega$

- Compute $C_{BW}\text{ (pF)} = \frac{3.2 \times 67\text{ kHz} \times 10^8}{97655 \times 100\text{ Hz}^2} = 21955\text{ pF}$

- Compute $R_B = \frac{0.9}{21955 \times 10^{-12} \times 100\text{ Hz}} = 410\text{ k}\Omega$

6) Using the -5V Inverter will eliminate the need for a -5 V supply. Refer to FIGURE 5. for the necessary connections.

When using the built-in -5 V inverter, the maximum tracking rate should be scaled for a full-scale velocity output of 3.5 V max.

TABLE 2. TRACKING/BW RELATIONSHIP

RPS (MAX)/BW	RESOLUTION
1	10
0.50	12
0.25	14
0.125	16

Note: Use of the -5 V inverter is not recommended for applications that require the highest BW and Tracking Rates.

HIGHER TRACKING RATES AND CARRIER FREQUENCIES.

Maximum tracking rate is limited by the velocity voltage saturation (nominally 4 V) and the maximum internal clock rate (nominally 1,333,333 Hz for R CLK = 30k). To achieve higher tracking

TABLE 3. MAX TRACKING RATE (MIN) IN RPS

R SET (Ω)	R CLK (Ω)	RESOLUTION			
		10	12	14	16
30k** or open	30k	1152	288	72	18
23k	20k	1728	432	108	27
23k	15k	2304	576	*	*

TABLE 4. CARRIER FREQUENCY (MAX) IN KHZ

R SET (Ω)	R CLK (Ω)	RESOLUTION			
		10	12	14	16
30k** or open	30k	10	10	7	5
23k	30k	10	10	10	7
23k	20k	10	10	10	10
23k	15k	10	10	*	*

* Not recommended.
** The use of a high quality thin-film resistor will provide better temperature stability than leaving open.

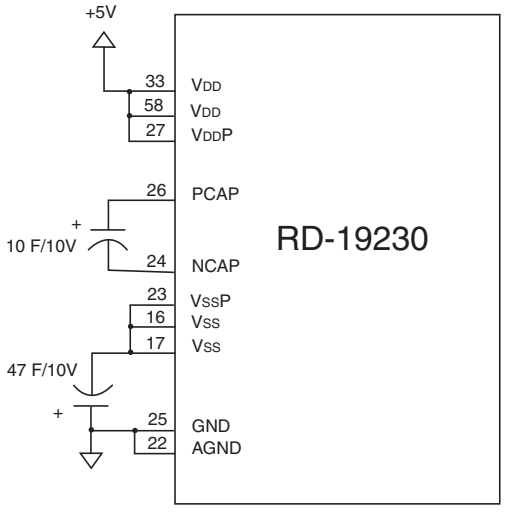


FIGURE 5. -5V INVERTER CONNECTIONS

rates, a higher internal counting rate must be programmed by setting RCLK to a value less than 30k. See TABLE 4. for the appropriate values.

The Rv resistor and an internal 50pF cap are configured as an integrating circuit that resets to zero after a count occurs in either direction. This circuit acts as a VCO with velocity as its input and CB as its output. The Rv resistor and an internal 50pF cap determine the maximum rate of the VCO. Rv must be chosen such that the maximum rate of the VCO is less than the maximum internal clock rate. Choose the tracking rate in accordance with TABLE 3 to insure this relationship. The rates shown in TABLE 3 are based on ~90% of the nominal internal clock rate.

The relationship between the velocity voltage and the VCO rate is given by:

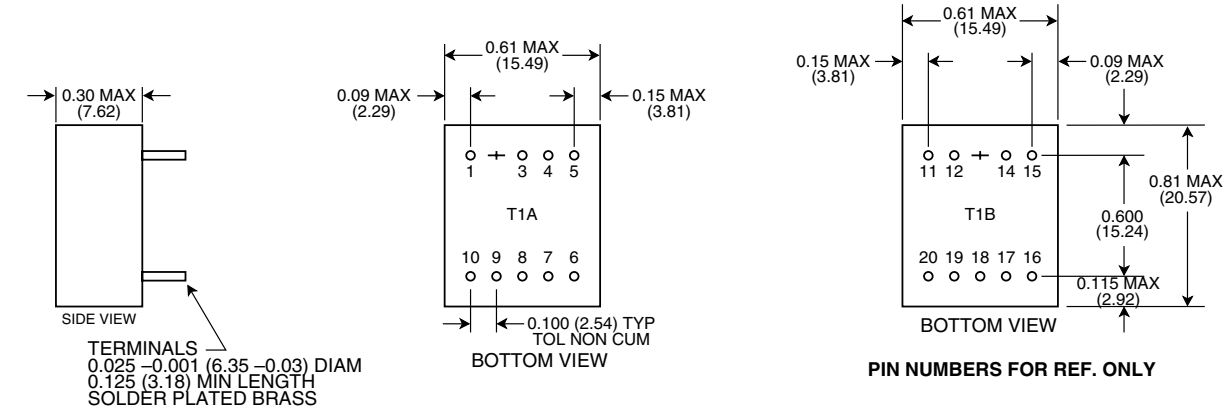
$$\frac{\text{Velocity Voltage}}{\text{VCO Frequency}} = \frac{1}{(\text{Rv} \times 50\ \text{pF} \times 1.25)}$$

TABLE 5. TRANSFORMERS

INPUT SIGNAL TYPE	INPUT VOLTAGE (Vrms)	INPUT FREQUENCY (HZ)	PART NUMBER	FIGURE NUMBER
Synchro	11.8	400	52034	6
Synchro	90	400	52035	6
Resolver	11.8	400	52036	7
Resolver	26	400	52037	7
Resolver	90	400	52038	7
Reference	Reference	400	B-426*	8
Synchro	Synchro	60	52039**	9
Reference	Reference	60	24133**	9

* Beta Transformer

** 60 Hz synchro transformers are active (require ±15V DC power supplies) and are available in two temperature ranges; -1: -55° to +125° and -3: 0° to + 70°.



Dimensions are shown in inches (mm).

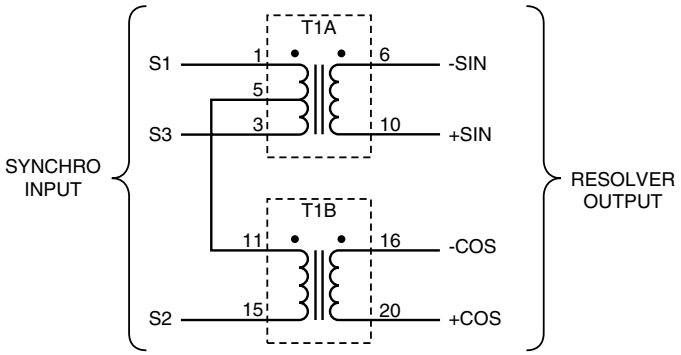
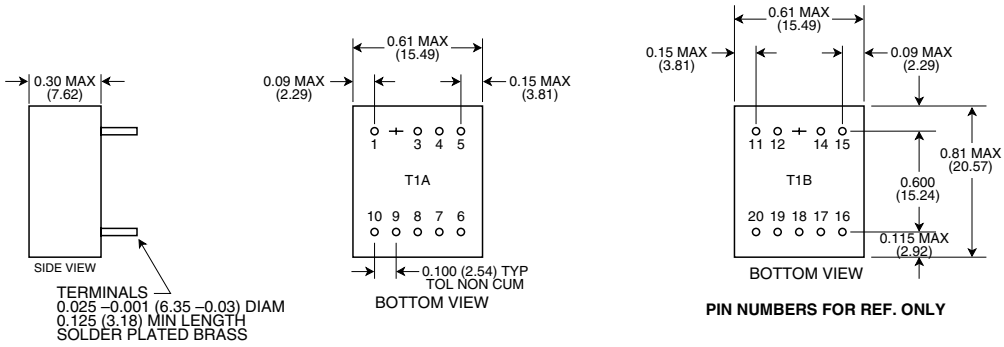


FIGURE 6. TRANSFORMER LAYOUT AND SCHEMATIC (SYNCHRO INPUT - 52034/52035)



Dimensions are shown in inches (mm).

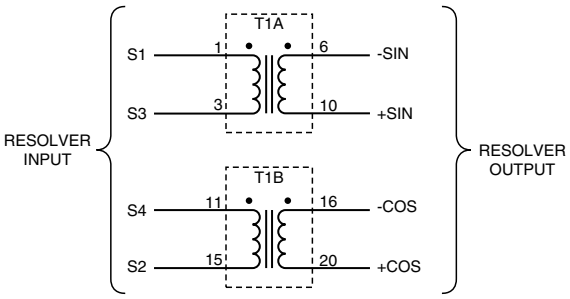


FIGURE 7. TRANSFORMER LAYOUT AND SCHEMATIC (RESOLVER INPUT - 52036/52037/52038)

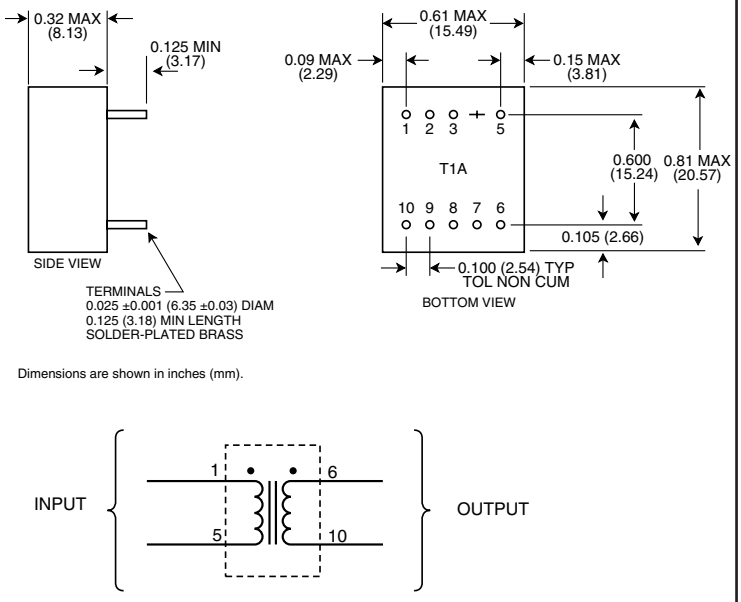
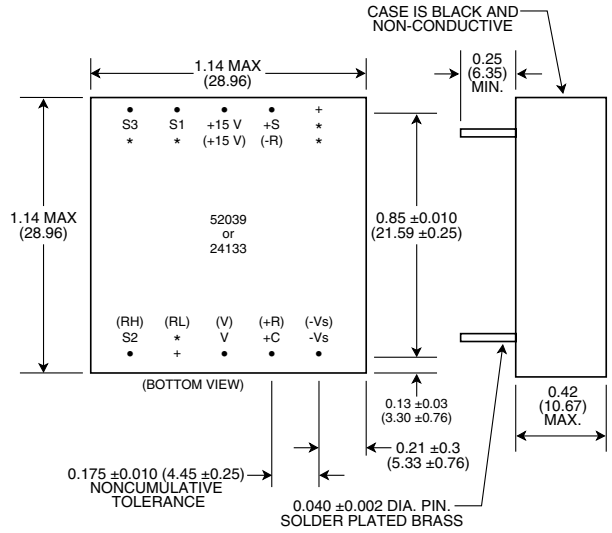


FIGURE 8. TRANSFORMER LAYOUT AND SCHEMATIC (REFERENCE INPUT - B-426)



The mechanical outline is the same for the synchro input transformer (52039) and the reference input transformer (24133), except for the pins. Pins for the reference transformer are shown in parenthesis ( ) below. An asterisk * indicates that the pin is omitted.

FIGURE 9. 60 HZ SYNCHRO AND REFERENCE TRANSFORMER DIAGRAMS (SYNCHRO INPUT - 52039 / REFERENCE INPUT - 24133)

TYPICAL INPUTS

FIGURES 10 through 14 illustrate typical input configurations.

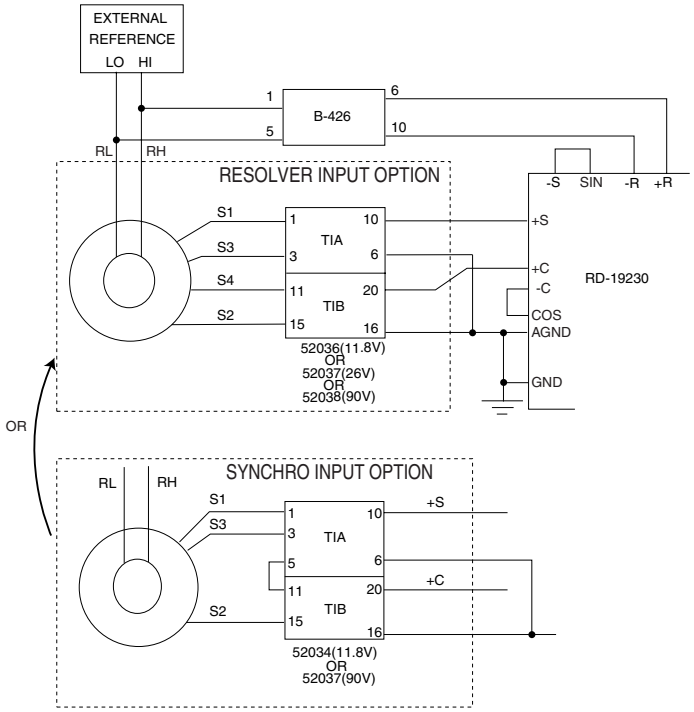
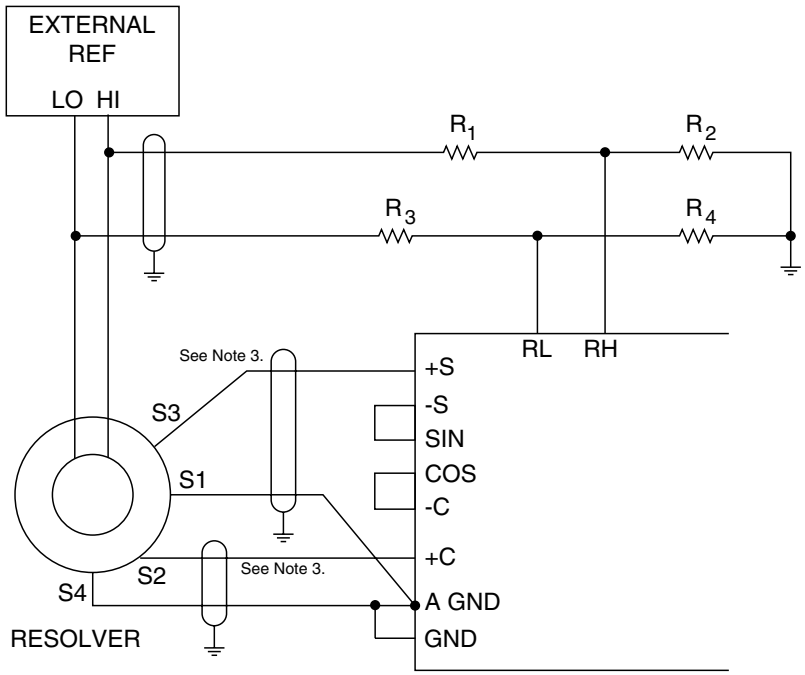
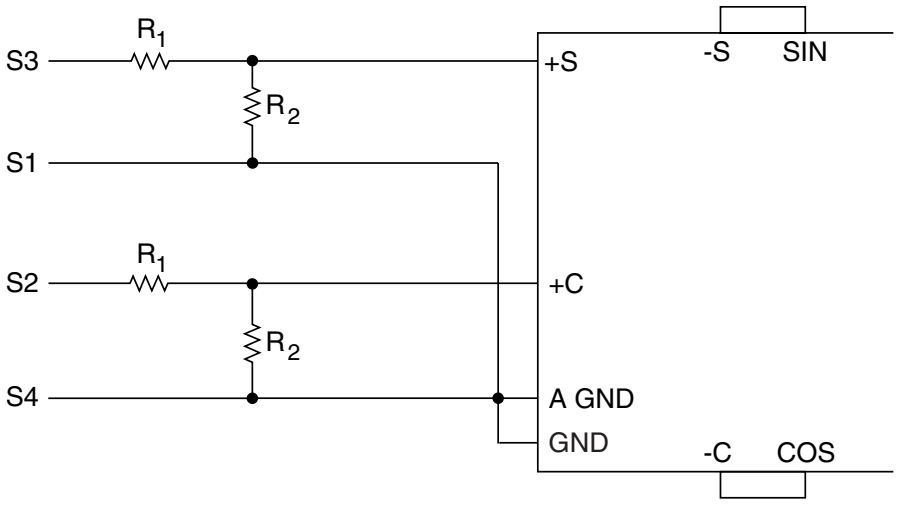


FIGURE 10. TYPICAL TRANSFORMER CONNECTIONS



Notes:
1) Resistors selected to limit Vref peak to between 1.5 V and 4 V.
2) External reference LO is grounded, then R3 and R4 are not needed, and -R is connected to GND.
3) 10k ohms, 1% series current limit resistors are recommended.

FIGURE 11. TYPICAL CONNECTIONS, 2 V RESOLVER, DIRECT INPUT

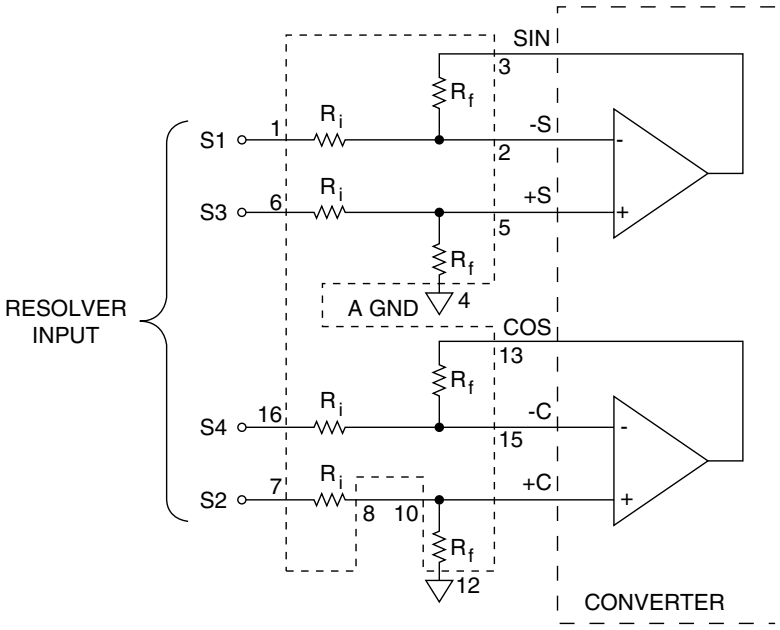


$$\frac{R_2}{R_1 + R_2} = \frac{2}{X\ Volt}$$

$R_1 + R_2$ should not load the Resolver; it is recommended to use a $R_2 = 10\ k\Omega$

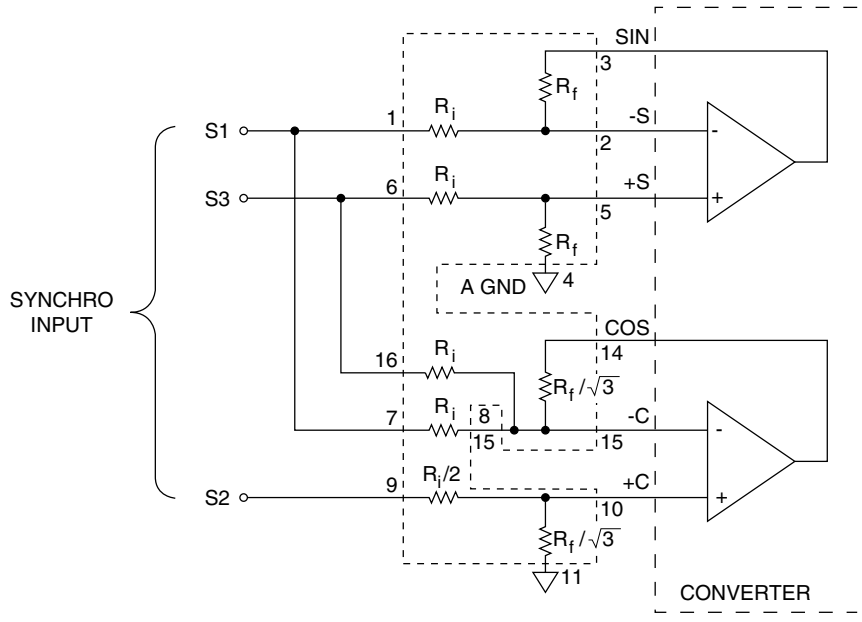
$R_1 + R_2$ Ratio erros will result in Angular errors,
2 cycle, 0.1% Ratio error = 0.029 Peak Error.

FIGURE 12. TYPICAL CONNECTIONS, X- VOLT RESOLVER, DIRECT INPUT



S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to GND at the converter.
For DDC-49530: R_i = 70.8 KΩ, 11.8 V input, synchro or resolver.
For DDC-49590: R_i = 270 KΩ, 90 Volt input, synchro or resolver.
Maximum additional error is 1 minute.
When using discrete resistors: Resolver L-L voltage = $\frac{R_i}{R_f}$ x 2 Vrms, where $R_f \geq 6$ kΩ

FIGURE 13. DIFFERENTIAL RESOLVER INPUT, USING DDC-49530 (11.8 V) OR DDC-49590 (90 V)



S1, S2, S3 should be triple twisted shielded; RH and RL should be twisted shielded;
In both cases the shield should be tied to GND at the converter.
11.8 Volt input = DDC-49530: R_i = 70.8 KΩ, 11.8 V input, synchro or resolver.
90 Volt input = DDC-49590: R_i = 270 KΩ, 90 Volt input, synchro or resolver.
Maximum additional error is 1 minute.
When using discrete resistors: Resolver L-L voltage = $\frac{R_i}{R_f}$ x 2 Vrms, where $R_f \geq 6$ kΩ

FIGURE 14. SYNCHRO INPUT, USING DDC-49530 (11.8 V) OR DDC-49590 (90 V)

DC INPUTS

As noted in TABLE 1 the RD-19230 will accept DC inputs. It is necessary to set the REF input to DC by tying RH to +5 V and RL to GND or -5 V.

VELOCITY TRIMMING

RD-19230 specifications for velocity scaling, reversal error, and offset are contained in TABLE 1. Velocity scaling and offset are externally trimmable for applications requiring tighter specifications than those available from the standard unit. FIGURE 15 shows the setup for trimming these parameters with external pots. It should also be noted that when the resolution is changed, VEL Scaling is also changed.

OPTIONAL BANDWIDTH COMPONENTS

The RD-19230 provides the option of using a second set of bandwidth components. The second set of components can be used for switch-on-the-fly or dual-bandwidth applications. The SHIFT and $\overline{\text{UP}}$/DN inputs are used when when switching bandwidth components, and their operation is described below. Refer to the block diagram on page 1.

SHIFT

The SHIFT pin is an input that chooses between the VEL1 and VEL2 bandwidth components. This pin has an internal pull-up to +5V. When the SHIFT pin is left open, or a logic 1 is applied, the VEL1 components are selected. When a Logic 0 is applied, the VEL2 components are selected. The deselected set of bandwidth components are driven by an amplifier, with programmable gain, that follows the velocity amplifier. This amplifier can be used to pre-charge the deselected set of components to the voltage level that is expected after a change in resolution. (See description on BENEFIT OF SWITCHING RESOLUTION ON THE FLY.)

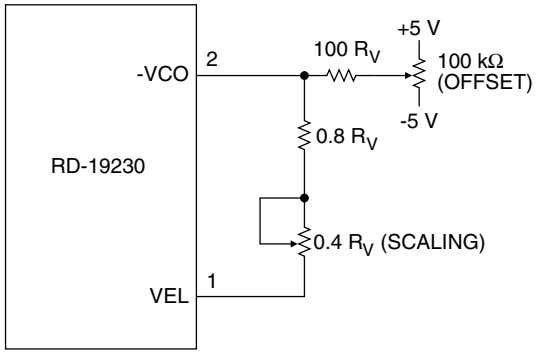


FIGURE 15. VELOCITY TRIMMING

TABLE 6. PRECHARGE AMPLIFIER GAIN PROGRAMMING

UP/DN	GAIN
Logic 0	4
Logic 1	1/4
-5 V	1

UP/DN

The $\overline{\text{UP}}$/DN input selects the gain of the amplifier driving the deselected set of bandwidth components. $\overline{\text{UP}}$/DN has three input states. See TABLE 6 to relate input to gain.

BENEFIT OF SWITCHING RESOLUTION ON THE FLY

Switching resolution on the fly can be used in applications that require high resolution for accurate position control, and tracking rates or settling times that are faster than the high resolution mode will allow.

The RD-19230 can track four times faster for each step down in resolution (i.e., a step from 16 bits to 14 bits). The velocity output will be scaled down by a factor of four with each step down in resolution. For example, if the velocity output is scaled such that 4 Volts = 10 RPS in 16 bit resolution, then the same converter will output 1 Volt for 10 RPS in 14 bit resolution. To avoid glitches in the velocity output, the second set of bandwidth components can be pre-charged to the expected voltage, and switched in using the SHIFT input at the same time the resolution is changed. This will allow for a smooth velocity transition, resulting in reduced errors and minimal settling time after the change.

FIGURE 17 shows the way the converter behaves during a change in resolution while tracking at a constant velocity. The first illustration shows the benefits of switching in pre-charged components while changing resolution. The second illustration shows the result without the benefits of switching on the fly.

The signals that have been recorded are:

1) VEL: velocity output pin on the RD-19230

2) ERROR: this is the analog representation of the error between the input and the output of the RD-19230

3) D0: an input resolution control line to the RD-19230

4) $\overline{\text{BIT}}$: built-in-test output pin of the RD-19230

When this system uses the switch resolution on the fly implementation, the velocity signal immediately assumes the pre-

charged level of the second set of components, resulting in small errors and reduced settling times. Notice that the $\overline{BIT}$ output does not indicate a fault condition. (refer to FIGURE 17)

When this system type does not use the switch resolution on the fly implementation, large errors and increased settling times result. The errors exceed 100 LSBs causing the $\overline{BIT}$ to flag for a fault condition.

SWITCH ON THE FLY IMPLEMENTATION

The following steps detail switching resolution on the fly.

1) The SHIFT pin should be controlled synchronously with the change in resolution. When shift is logic high, the VEL1 components will be selected. When shift is logic 0, the VEL2 components will be selected.

2) The second set of BW components (C_{BW2}, R_{B2}, $C_{BW2/10}$) should typically be of the same value as the first set (C_{BW1}, R_{B1}, $C_{BW1/10}$,) and should be installed on VEL_2 and VEL SJ_2.

Note: Each set of bandwidth components must be chosen to insure that the tracking rate to BW ratio (listed in TABLE 2) is not exceeded for the resolution in which it will be used.

3) $\overline{UP}$/DN will program the direction of the gain. If the resolution is increasing ($\overline{UP}$/DN logic 0), the gain of the pre-charge amplifier should be set to four. If the resolution is decreasing ($\overline{UP}$/DN logic 1), the gain should be set to 1/4. The gain of the pre-charge amplifier should be programmed prior to switching the resolution of the converter, allowing enough time for the the components to settle to the pre-charged level. This time will depend on the time constant of the bandwidth components being charged. If switching is limited to two adjacent resolutions (i.e., 14 and 16) then the pre-charge amplifier can be set up to continuously maintain the appropriate velocity voltage on the deselected components, resulting in the fastest possible switching times. See FIGURE 16 for an example of the input wiring connections necessary for switching on the fly between 14 and 16 bit resolution.

DUAL BANDWIDTHS

With the second set of BW component pins, the user can set two bandwidths for the RD-19230 and choose between them. To use two bandwidths, proceed as follows:

1) Tie $\overline{UP}$/DN to pin -5V.

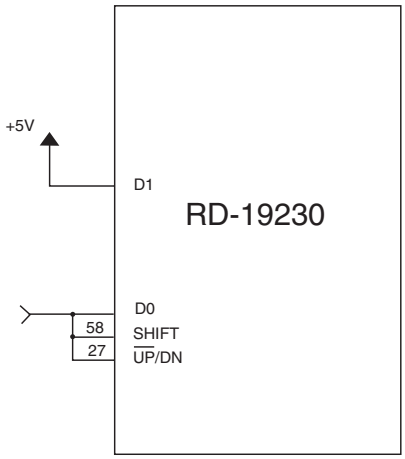
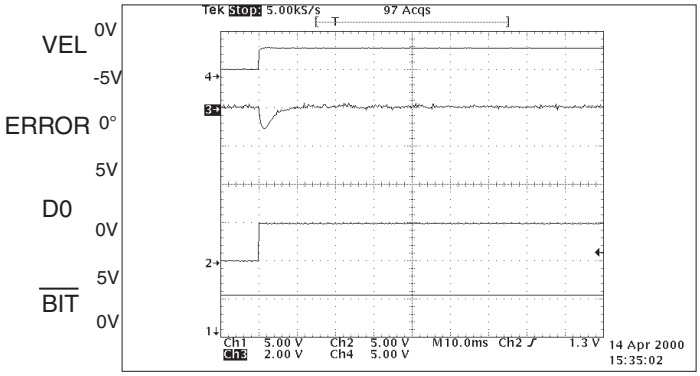


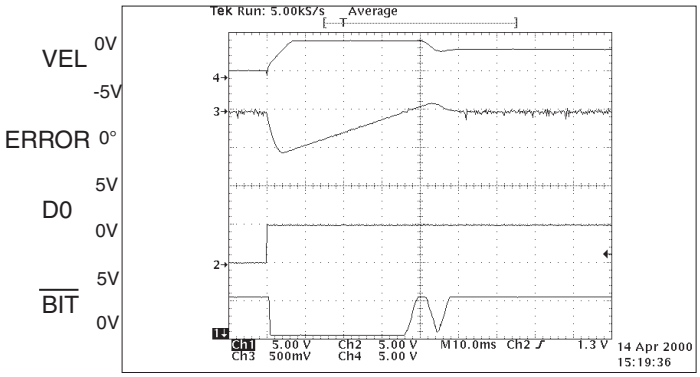
FIGURE 16. INPUT WIRING - SWITCHING ON THE FLY BETWEEN 14 AND 16 BIT RESOLUTION

With Switch Resolution on the Fly Implemented



ERROR = 13.6 LSBs per box

Without Switch Resolution on the Fly Implemented



ERROR = 1500 LSBs per box

FIGURE 17. BENEFIT OF SWITCHING RESOLUTION ON THE FLY

2) Choose the two bandwidths following the guidelines in the General Setup Considerations; the R_V resistor must be the same value for both bandwidths.

3) Use the SHIFT pin to choose between bandwidths. A logic 1 selects the VEL1 components and a logic 0 selects the VEL2 components.

INHIBIT, ENABLE, AND CB TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in FIGURE 18, angular output data is valid 150 ns maximum after the application of the negative inhibit pulse.

Output angle data is enabled onto the tri-state data bus in two bytes. Enable MSBs ($\overline{EM}$) is used for the most significant 8 bits and Enable LSBs ($\overline{EL}$) is used for the least significant 8 bits. As shown in FIGURE 19, output data is valid 150 ns maximum after the application of a negative enable pulse. The tri-state data bus returns to the high impedance state 100 ns maximum after the rising edge of the enable signal.

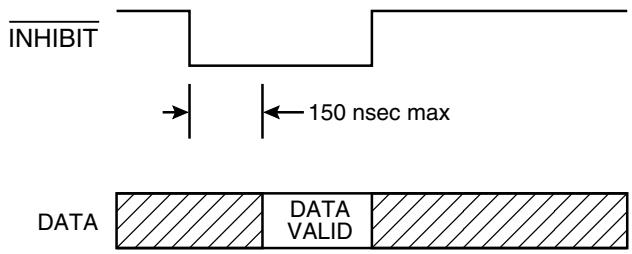


FIGURE 18. INHIBIT TIMING

The Converter Busy (CB) signal indicates that the tracking converter output angle is changing 1 LSB. As shown in FIGURE 20, output data is valid 50 nS maximum after the middle of the CB pulse. CB pulse width is 1/40 F_S, which is nominally 375 ns.

INTERNAL ENCODER EMULATION

The RD-19230 can be programmed to encoder emulation mode by connecting the $\overline{A\_QUAD\_B}$ input to GND. The U/B output pin becomes B (LSB XOR LSB + 1) The A (LSB + 1) and B output signals can be used in control systems that are designed to interface with incremental optical encoders. To enable the Zero Index pulse, $\overline{ZIP\_EN}$ should be tied to GND.

The resolution of the incremental outputs is latched from the D0 and D1 inputs on the low going edge of $\overline{A\_QUAD\_B}$. The resolution of the parallel data outputs may be changed any time after the encoder resolution is latched (see FIGURE 23).

Note: The encoder resolution must be less than or equal to the resolution of the parallel data outputs. Refer to FIGURE 21.

The timing of the A, B and ZIP (or North Reference Pole [NRP]) output is dependent on the rate of change of the synchro/resolver position (rps or degrees per second) and the encoder resolution latched into the RD-19230 (refer to FIGURE 22). The calculations for the timing is:

n = encoder resolution latched into RD-19230

$t = 1 / (2^{n*} \text{ Velocity(RPS)})$

$T = 1 / (\text{Velocity(RPS)})$

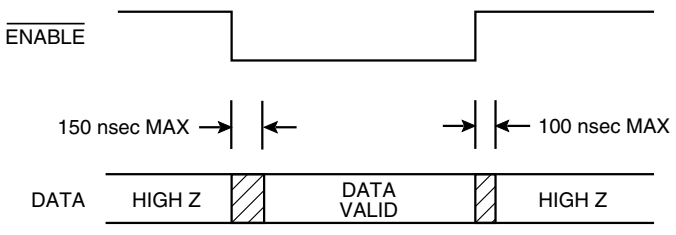


FIGURE 19. ENABLE TIMING

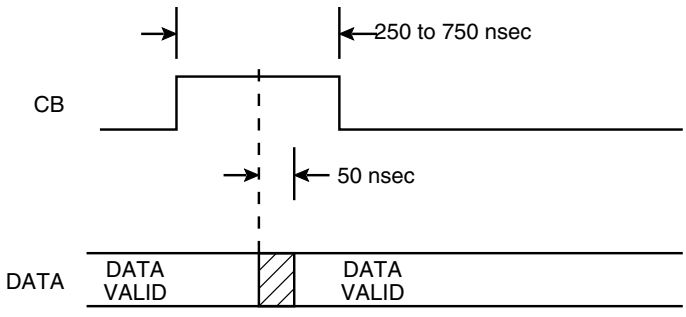


FIGURE 20. CONVERTER BUSY TIMING

SYNTHESIZED REFERENCE

The synthesized reference section of the RD-19230 eliminates errors due to phase shift between the reference and signal inputs. Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of synchros and resolvers, their output signals lead the reference input signal (RH and RL). When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. As shown in FIGURE 1, the converter synthesizes its own internal reference signal based on the SIN and COS signal inputs. Therefore, the phase of the synthesized (internal) reference is determined by the signal input, resulting in reduced quadrature errors.

BUILT-IN-TEST ($\overline{\text{BIT}}$)

The $\overline{\text{BIT}}$ output is active low, and will be asserted during the following three error conditions:

Loss of Signal (LOS) - Sin and Cos inputs both less than 500mV.

Loss of Reference (LOR) - Reference Input less than 500 mV.

Excessive Error - This error is detected by monitoring the demodulator output, which is proportional to the difference between the analog input and digital output. When it exceeds approximately 100 LSBs (in the selected resolution), $\overline{\text{BIT}}$ will be asserted. This condition can occur any time the analog input changes at a rate in excess of the maximum tracking rate. During power up, the converter may see a large difference between the sin/cos inputs and the digital output angle held in its counter. $\overline{\text{BIT}}$ will be asserted until the converter settles within ~ 100 LSB's of the final result.

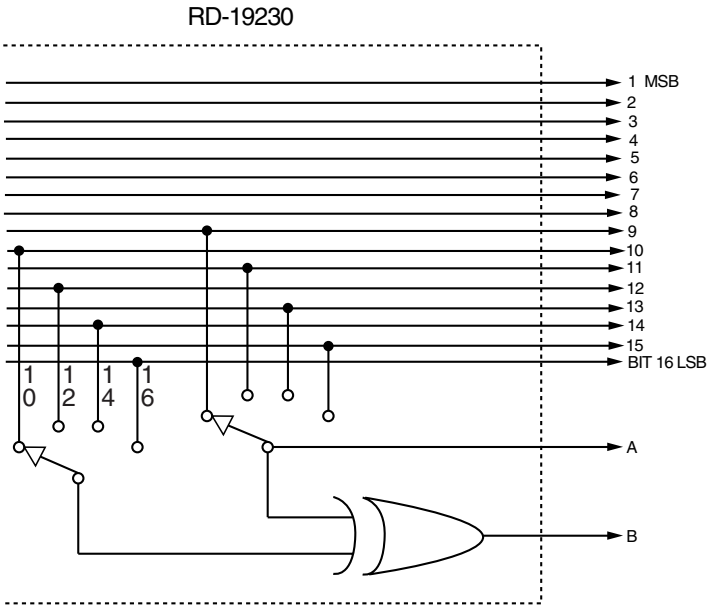


FIGURE 21. INCREMENTAL ENCODER EMULATION RESOLUTION CONTROL

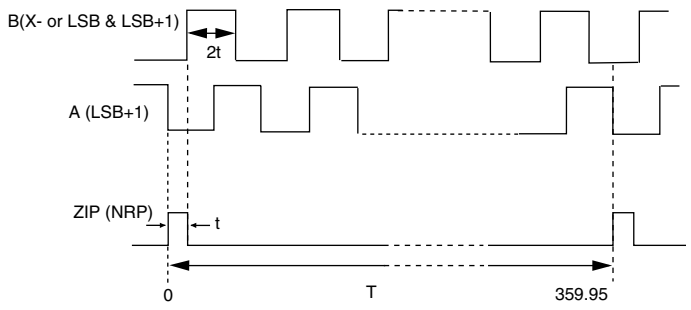


FIGURE 22. INCREMENTAL ENCODER EMULATION

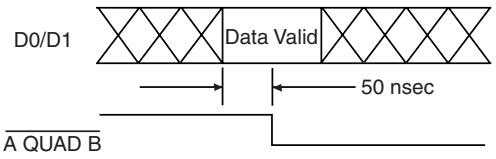


FIGURE 23. TIMING FOR INCREMENTAL ENCODER EMULATION RESOLUTION CONTROL

LVDT MODE

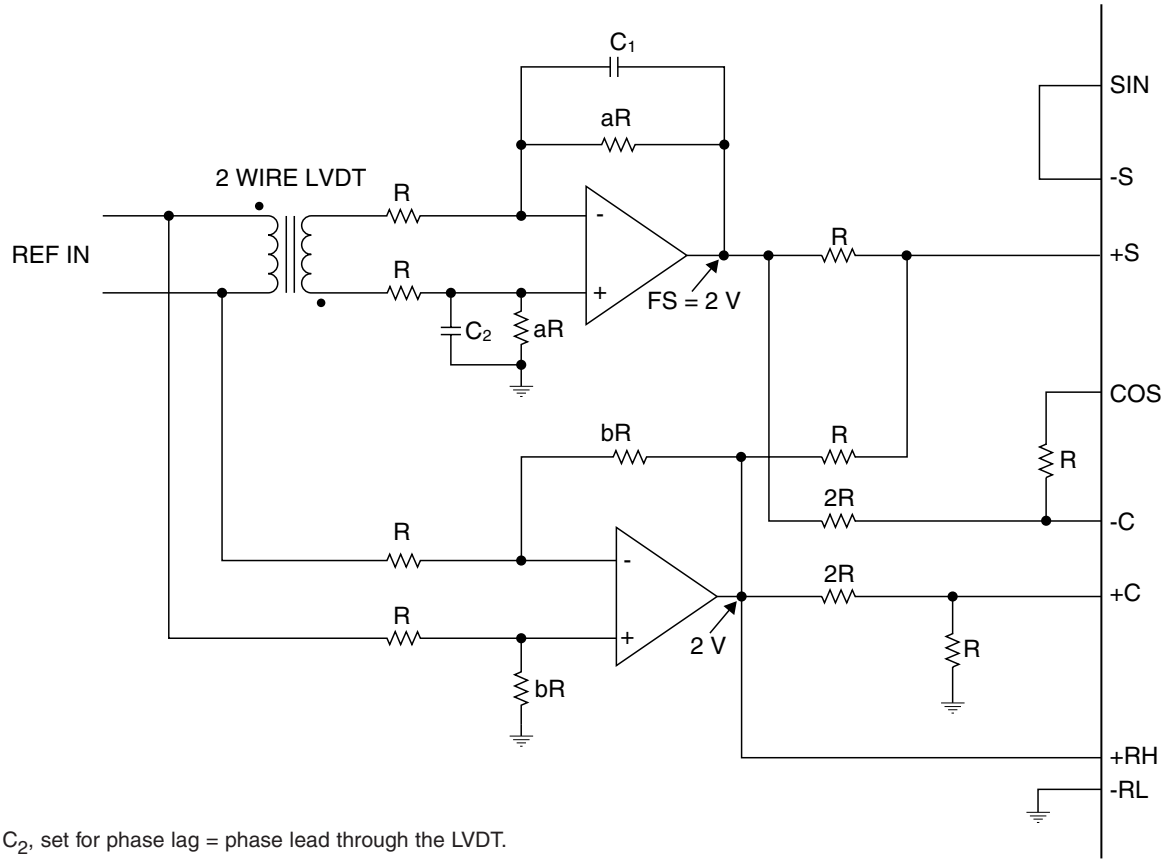
As shown in TABLE 1 the RD-19230 unit can be made to operate as an LVDT-to-digital converter. In this mode the RD-19230 functions as a ratiometric tracking linear converter. When linear AC inputs are applied from a LVDT the converter operates over one quarter of its range. This results in two less bits of resolution for LVDT mode than are provided in resolver mode.

LDVT output signals need to be scaled to be compatible with the converter input. FIGURE 25 is a schematic of an input scaling circuit applicable to 3-wire LVDTs. The value of the scaling constant “a” is selected to provide an input of 2 Vrms at full stroke of the LVDT. The value of scaling constant “b” is selected to provide an input of 1 Vrms at null of the LVDT. Suggested components for implementing the input scaling circuit are a quad op-amp, such as a OP11 type, and precision thin-film resistors of 0.1% tolerance. FIGURE 24 illustrates a 2-wire LVDT configuration.

Data output of the RD-19230 is Binary Coded in LVDT mode. The most negative stroke of the LVDT is represented by ALL ZEROS and the most positive stroke of the LVDT is represented by ALL ONES. The most significant 2 bits (2 MSBs) may be used as overrange indicators. Positive overrange is indicated by code “01” and negative overrange is indicated by code “11“ (see TABLE 7).

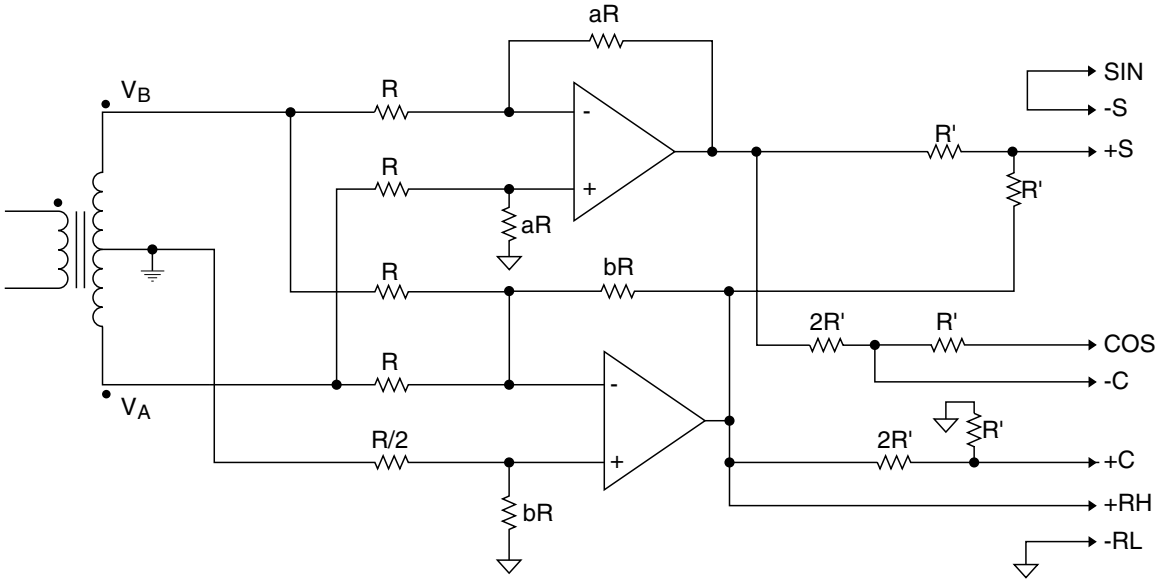
TABLE 7. 12-BIT LVDT OUTPUT CODE FOR FIGURE 25

LVDT OUTPUT	MSB			LSB
+ over full travel	01	xxxx	xxxx	xxxx
+ full travel -1 LSB	00	1111	1111	1111
+0.5 travel	00	1100	0000	0000
+1 LSB	00	1000	0000	0001
null	00	1000	0000	0000
- 1 LSB	00	0111	1111	1111
-0.5 travel	00	0100	0000	0000
- full travel	00	0000	0000	0000
- over full travel	11	xxxx	xxxx	xxxx



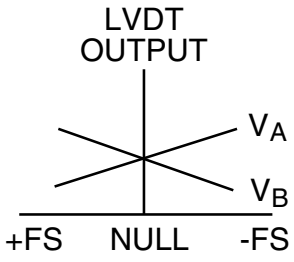
$C_1 = C_2$, set for phase lag = phase lead through the LVDT.

FIGURE 24. 2-WIRE LVDT DIRECT INPUT



Notes:

1. R' ≥ 10 kΩ
2. Consideration for the value of R is LVDT loading.



$$b = \frac{1}{V_{Anull}} = \frac{1}{V_{Bnull}}$$

$$a = \frac{2}{(V_A - V_B)_{max}}$$

$$SIN = 1 + \frac{a}{2}(V_A - V_B)$$

$$COS = 1 - \frac{a}{2}(V_A - V_B)$$

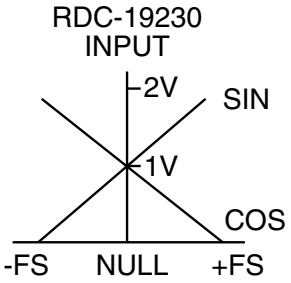


FIGURE 25. 3-WIRE LVDT SCALING CIRCUIT

TABLE 8. RD-19230 PINOUTS							
#	NAME	#	NAME	#	NAME	#	NAME
1	VEL	17	VSS (-5V)	33	VDD (+5V)	49	Bit 8
2	-VCO	18	TP3 (test point)	34	N/C	50	Bit 16
3	SJ1	19	R CLK	35	Bit 9	51	A (LSB + 1)
4	SJ2	20	R SET	36	Bit 2	52	TP4 (test point)
5	SHIFT	21	$\overline{\text{ENM}}$	37	Bit 10	53	N/C
6	VEL2	22	AGND	38	Bit 3	54	TP5 (test point)
7	TP1 (test point)	23	VSSP	39	Bit 11	55	$\overline{\text{ZIP\_EN}}$
8	VEL1	24	NCAP	40	Bit 4	56	TP6 (test point)
9	TP2 (test point)	25	GND	41	N/C	57	$\overline{\text{ENL}}$
10	+C	26	PCAP	42	Bit 12	58	VDD (+5V)
11	COS	27	VDDP	43	Bit 5	59	$\overline{\text{UP}}$/DN
12	-C	28	$\overline{\text{BIT}}$	44	Bit 13	60	D0
13	+S	29	U/B	45	Bit 6	61	D1
14	SIN	30	$\overline{\text{A\_QUAD\_B}}$	46	Bit 14	62	$\overline{\text{INH}}$
15	-S	31	CB (ZI)	47	Bit 7	63	RH
16	VSS (-5V)	32	Bit 1	48	Bit 15	64	RL

Notes:
1. See FIGURE 5 for +5 V only operation.

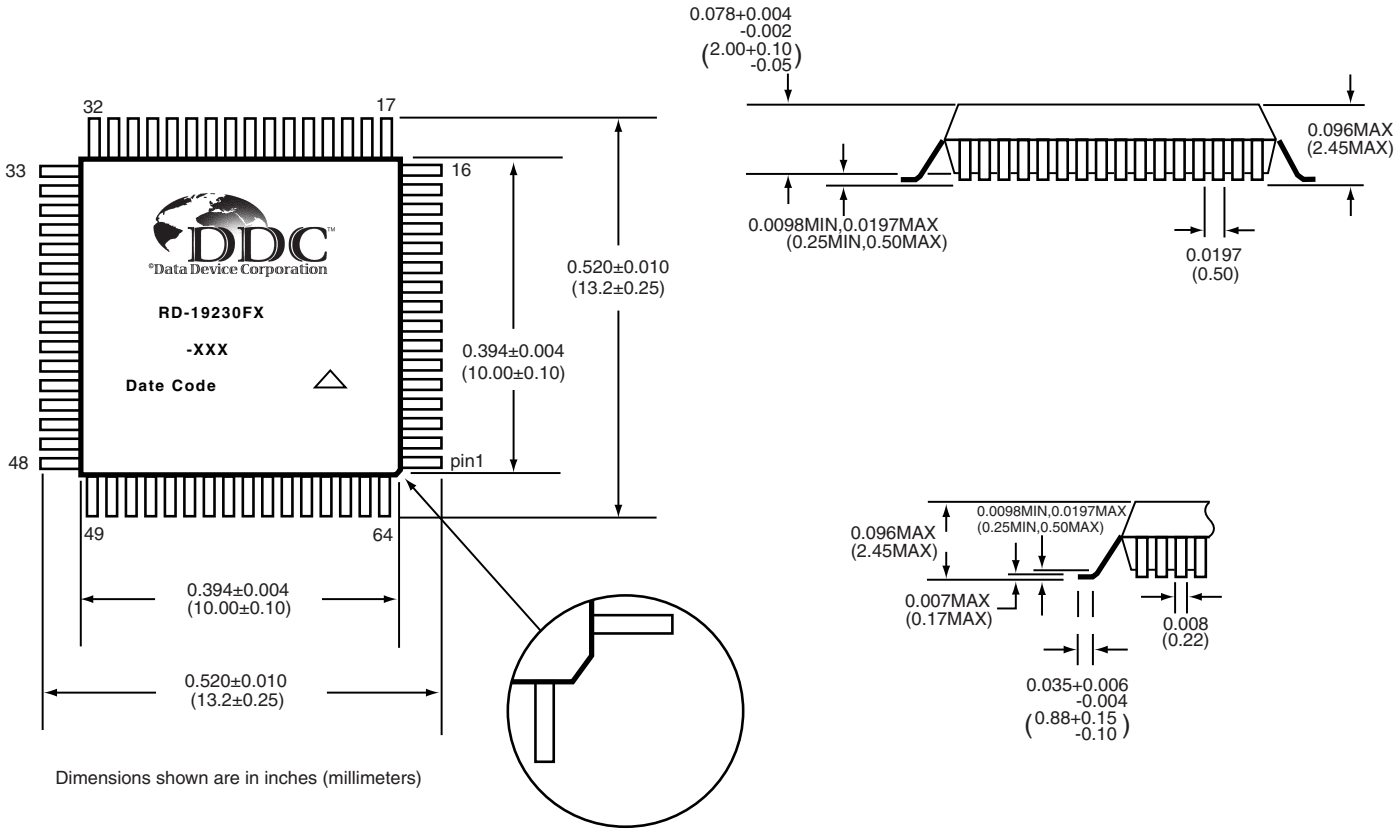


FIGURE 26. RD-19230 MECHANICAL OUTLINE

TABLE 9. FRONT-END THIN-FILM RESISTOR NETWORKS (SEE FIGURE 27)						
DDC-49530, DDC-57470 RESISTOR VALUES (11.8 V INPUTS)						
SYMBOL	**ABS VALUE**	**TOL (%)**	**REL TO**	**REL VALUE**	**TOL (%)**	**TCR(PPM)**
R1	70.8 k	0.1				25
R2			R1	12 k	0.02	2
R3			R4	12 k	0.02	2
R4			R1	70.8 k	0.02	2
R5			R1	70.8 k	0.02	2
R6			R1	35.4 k	0.02	2
R7			R6	6.9282 k	0.02	2
R8			R6	5.0718 k	0.02	2
R9			R11	5.0718	0.02	2
R10			R11	6.9282 k	0.02	2
R11			R1	70.8 k	0.02	2
DDC-49590 RESISTOR VALUES (90 V INPUTS)						
R1	270 k	0.1				25
R2			R1	6 k	0.02	2
R3			R4	6 k	0.02	2
R4			R1	270 k	0.02	2
R5			R1	270 k	0.02	2
R6			R1	135 k	0.02	2
R7			R6	3.4641 k	0.02	2
R8			R6	2.5359 k	0.02	2
R9			R11	2.5359 k	0.02	2
R10			R11	3.4641 k	0.02	2
R11			R1	270 k	0.02	2

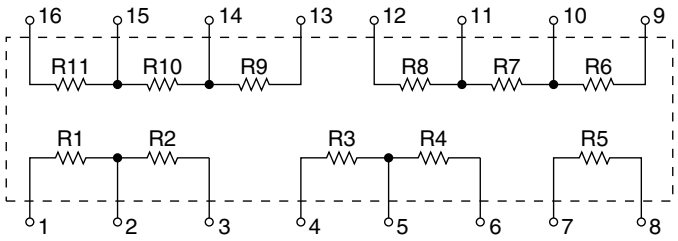
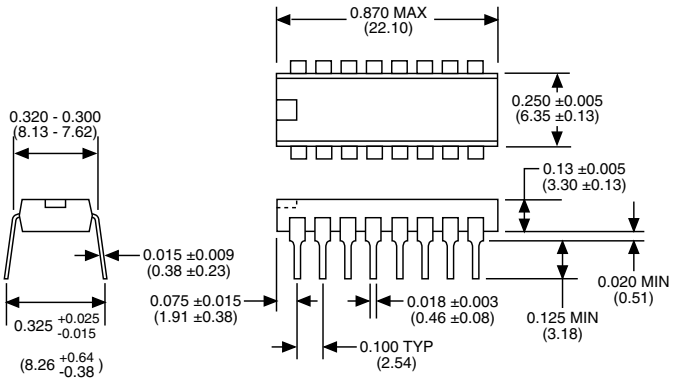
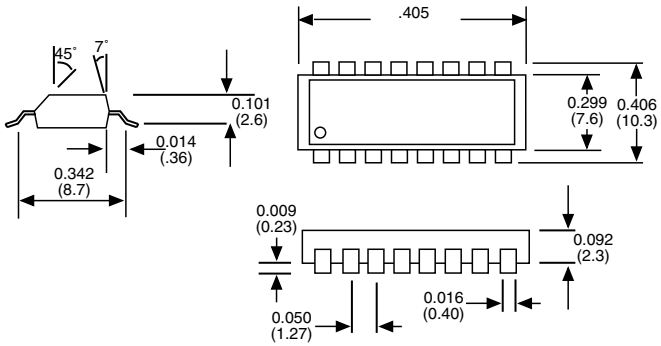


FIGURE 27. (DDC-49530, DDC-49590, DDC-57470) LAYOUT AND RESISTOR VALUES (SEE TABLE 9)



DIMENSIONS SHOWN ARE IN INCHES (MM).

FIGURE 28. 16-PIN THIN-FILM RESISTOR NETWORK DIP MECHANICAL OUTLINE (DDC-49530, DDC-49590)



DIMENSIONS SHOWN ARE IN INCHES (MM).

FIGURE 29. 16-PIN THIN-FILM RESISTOR NETWORK FLAT-PACK MECHANICAL OUTLINE (DDC-57470)

ORDERING INFORMATION

RD-19230FX-X X X X

Supplemental Process Requirements:
T = Tape and Reel (50 pc. min. order)

Accuracy:
2 = 4 min + 1 LSB
3 = 2 min + 1 LSB

Reliability:
0 = Standard DDC Procedures

Operating Temperature Range:
2 = -40° to +85°C
3 = 0° to +70°C

THIN-FILM RESISTOR NETWORKS:

DDC-49530 = 11.8 V inputs DIP package
DDC-57470 = 11.8 V inputs Flat-pack package
DDC-49590 = 90 V inputs DIP package

COMPONENT SELECTION SOFTWARE:

Component selection software can be downloaded from our website (www.ddc-web.com)

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