Low-Noise Phase-Locked Loop Clock Driver with 20 Clock Outputs

Product Features

- Low-Noise Phase-Locked Loop Clock Distribution.
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction. The clock outputs track the Clock Input modulation.
- Maximum clock frequency of 125 MHz.
- Zero Input-to-Output delay.
- Low jitter: Cycle-to-Cycle jitter ±100ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction.
- Operates at 3.3V V_{CC}.
- Output-to-Output skew less than 200ps.
- Package: Plastic 56-pin TSSOP (A).

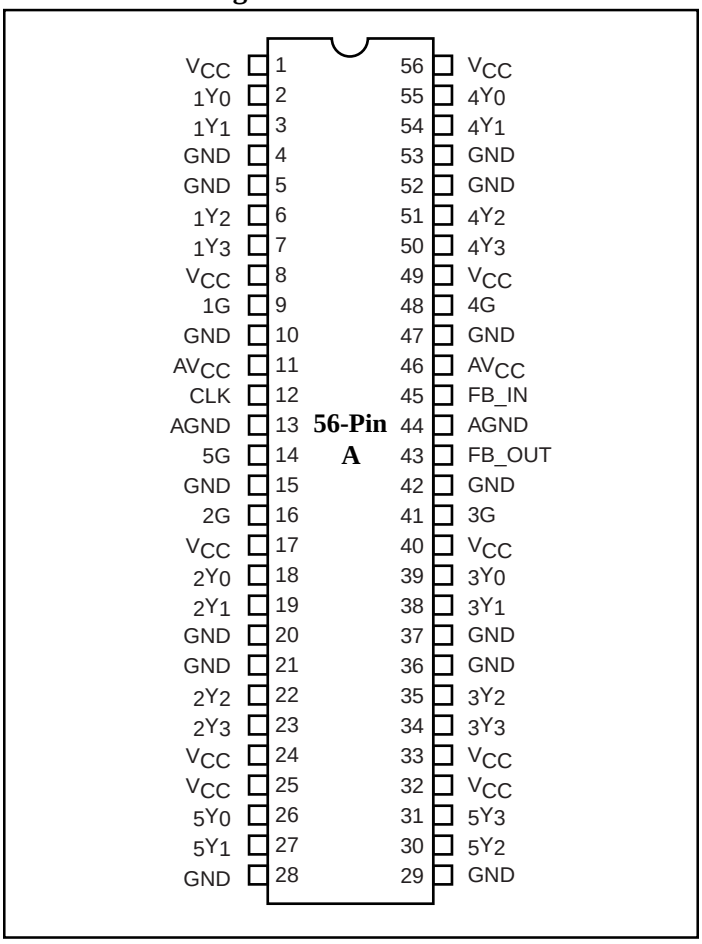
Product Description

The PI6C2520 is a low-skew, low-jitter, phase-locked loop (PLL) clock driver, distributing low-noise clock signals for Networking Applications. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero. This zero-delay feature allows the CLK_IN input clock to be distributed, providing 5 banks of 4 clocks and an extra clock for feedback.

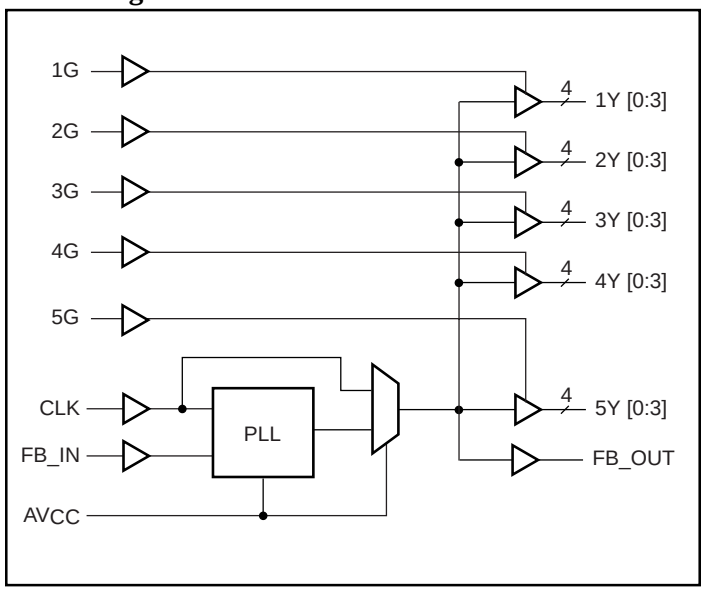
For test purposes, the PLL can be bypassed by strapping AV_{CC} to ground. The PI6C2520, which allows a Spread Spectrum clock input, operates at 3.3V V_{CC} and provides integrated series-damping resistors that make it ideal for driving point-to-point loads. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at the input clock.

Each bank of outputs can be enabled or disabled via the 1G, 2G, 3G, 4G, and 5G control inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK_IN. When the G inputs are low, the outputs are disabled to the logic low state.

Product Pin Configuration



Block Diagram



Pin Functions

Pin Name	Pin Number	Type	Description
CLK	12	I	Clock input. CLK allows spread spectrum.
FB_IN	45	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
1G	9	I	Output bank enable. When 1G is LOW, outputs 1Y[0:3] are disabled to a logic low state. When 1G is HIGH, all outputs 1Y[0:3] are enabled.
2G	16	I	Output bank enable. When 2G is LOW, outputs 2Y[0:3] are disabled to a logic low state. When 2G is HIGH, all outputs 2Y[0:3] are enabled.
3G	41	I	Output bank enable. When 3G is LOW, outputs 3Y[0:3] are disabled to a logic low state. When 3G is HIGH, all outputs 3Y[0:3] are enabled.
4G	48	I	Output bank enable. When 4G is LOW, outputs 4Y[0:3] are disabled to a logic low state. When 4G is HIGH, all outputs 4Y[0:3] are enabled.
5G	14	I	Output bank enable. When 5G is LOW, outputs 5Y[0:3] are disabled to a logic low state. When 5G is HIGH, all outputs 5Y[0:3] are enabled.
FB_OUT	43	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs 1Yx, 2Yx, 3Yx, 4Yx, and 5Yx.
1Y[0:3]	2,3,6,7	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
2Y[0:3]	18,19,22,23	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
3Y[0:3]	34,35,38,39	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
4Y[0:3]	50,51.54,55	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
5Y[0:3]	26,27,30,31	O	Clock outputs. These outputs provide low-skew copies of CLK. Each output has an embedded series-damping resistor.
AV_{CC}	11,46	Power	Analog power supply. AV_{CC} can be also used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	13,44	Ground	Analog ground. AGND provides the ground reference for the analog circuitry
V_{CC}	1,8,17,24,25,32,33,40, 49,56	Power	Power supply
GND	4,5,10,15,20,21,28,29, 36,37,42,47,52,53	Ground	Ground

Absolute Maximum Ratings Over Operating Free-Air Temperature
(unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5V to 4.6V
Input voltage range, V_I (1)	–0.5V to 6.5V
Voltage range applied to any output in the high or low state, V_O(1,2)	–0.5V to V_{CC} +0.5V
Input clamp current, I_{IK} (V_I <0)	–50mA
Output clamp current, I_{OK} (V_O <0 or V_O > V_{CC})	±50mA
Continuous output current, I_O (V_O - 0 to V_{CC})	±50mA
Continuous current through each V_{CC} or GND	±100mA
Maximum power dissipation at T_A = 55°C (in still air)(3)	0.85W
Storage Temperature Range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

Notes:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6V maximum.
3. Maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions(4)

		Min.	Max.	Units
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		
V_{IL}	Low-level input voltage		0.8	
V_I	Input Voltage	0	VCC	
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	
T_A	Operating free-air temperature	0	70	°C

Notes:
4. Unused inputs must be held high or low to prevent them from floating.

Electrical Characteristics Over Recommended Operating Free-air Temperature Range

(unless otherwise noted)

Symbol	Test Condition	V_{CC}	Min.	Typ.(1)	Max.	Units
V_{IK}, Input clamp voltage	Input current at –18mA	3V		–0.79	–1.2	V
V_{OH}	I_{OH} = –100µA	Min. to Max.	V_{CC} –0.2	2.99		
	I_{OH} = –12mA	3V	2.1	2.66		
	I_{OH} = –6mA		2.4	2.83		
V_{OL}	I_{OL} = 100µA	Min. to Max.		0.01	0.2	
	I_{OL} = 12mA	3V		0.3	0.8	
	I_{OL} = 6mA			0.15	0.55	
I_I, Input current	Clock input voltage = V_{CC} or GND	3.6V			±5	µA
Analog supply current I_{CC}(2)	Clock input voltage = V_{CC} or GND				20	
C_i	Input voltage = V_{CC} or GND	3.3V		4	3.5	pF
C_O	Output voltage = V_{CC} or GND			6		
ΔI_{CC}	One input @ V_{CC} –0.6V, other inputs @ V_{CC} or GND	3.3V to 3.6V		4.0	500	µA

Notes:

1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. For ICC of AV_{CC}, see Figure 5. For dynamic digital I_{CC}, see Figure 6.

Function Table

1G	2G	3G	4G	5G	CLK	1Y	2Y	3Y	4Y	5Y	FBOUT
X	X	X	X	X	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	H	L	L	L	L	L	H	H
L	L	L	H	L	L	L	L	L	H	L	H
L	L	L	H	H	L	L	L	L	H	H	H
L	L	H	L	L	L	L	H	H	L	L	H
L	L	H	L	H	L	L	H	H	L	H	H
L	L	H	H	L	L	L	H	H	H	L	H
L	L	H	H	H	L	L	H	H	H	H	H
L	H	L	L	L	L	H	L	L	L	L	H
L	H	L	L	H	L	H	L	L	L	H	H
L	H	L	H	L	L	H	L	L	H	L	H
L	H	L	H	H	L	H	L	L	H	H	H
L	H	H	L	L	L	H	H	H	L	L	H
L	H	H	L	H	L	H	H	H	L	H	H
L	H	H	H	L	L	H	H	H	H	L	H
L	H	H	H	H	L	H	H	H	H	H	H
H	L	L	L	L	H	L	L	L	L	L	H
H	L	L	L	H	H	L	L	L	L	H	H
H	L	L	H	L	H	L	L	L	H	L	H
H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	L	H	L	H	H	L	L	H
H	L	H	L	H	H	L	H	H	L	H	H
H	L	H	H	L	H	L	H	H	H	L	H
H	L	H	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	L	L	L	L	H
H	H	L	L	H	H	H	L	L	L	H	H
H	H	L	H	L	H	H	L	L	H	L	H
H	H	L	H	H	H	H	L	L	H	H	H
H	H	H	L	L	H	H	H	H	L	L	H
H	H	H	L	H	H	H	H	H	L	H	H
H	H	H	H	L	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	H	H

AC Specifications

Timing Requirements

(Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature).

Symbol	Parameter	Min.	Max.	Units	Note
F_{CLK}	Clock Frequency	25	125	MHz	1
D_{CYI}	Input clock duty cycle	40	60	%	
$t_{Stabilization}$	Stabilization Time after power up		1	ms	

Notes:

1. Operating Clock Frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters (used for low-speed system debug).
2. Application Clock Frequency indicates a range over which the PLL must meet all of the timing parameters.

Switching Characteristics

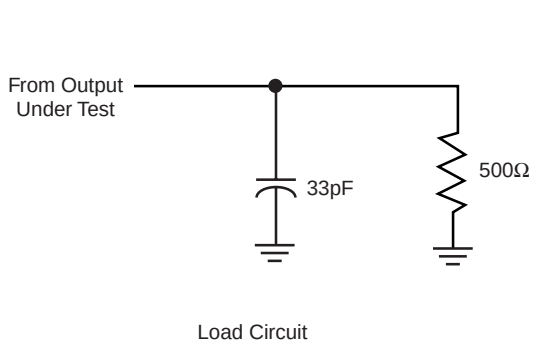
Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature, C_L = 30pF [1, 3]

Parameter	From (INPUT)	To (Output)	V_{CC} = 3.3V ± 0.3V			Units
			Min.	Typ.	Max.	
t_{phase} error	CLKIN↑ = 100MHz	FBIN↑		170		ps
$t_{sk(O)}$ [2]	Any Y or FBOUT	Any Y or FBOUT			200	
$Jitter_{(pk-pk)}$	F(clkin > 66MHz)		–100		100	
Duty cycle	F(clkin ≤ 66MHz)		45		55	%
	F(clkin > 66MHz)		43		55	
t_r			0.7		2.6	ns
t_f			1.2		2.5	

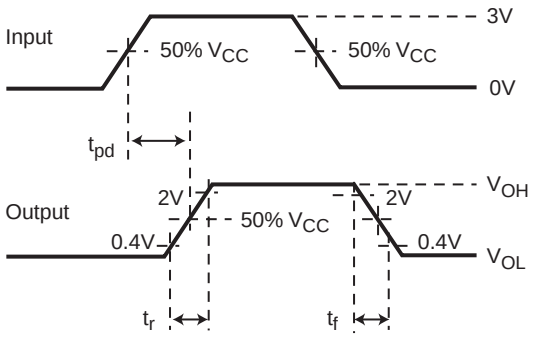
Notes:

1. These parameters are not production tested.
2. The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
3. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

Parameter Measurement Information



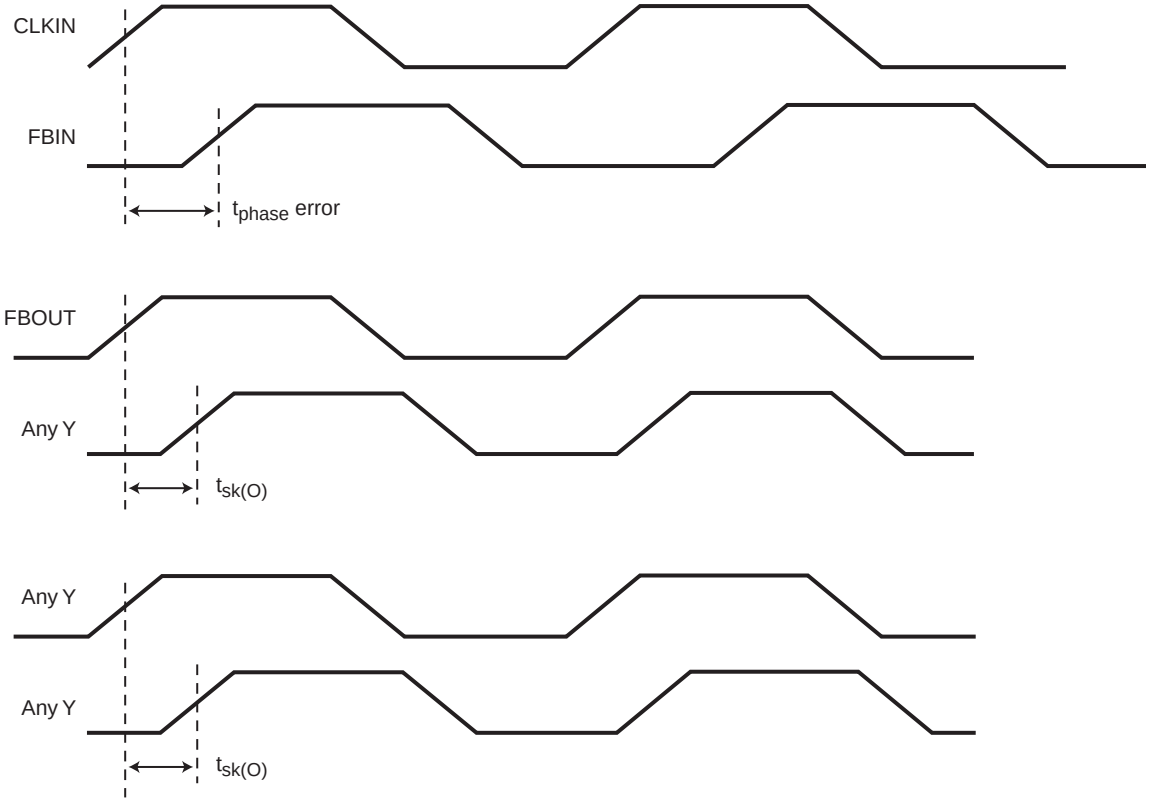
Load Circuit



Voltage Waveforms
Propagation Delay times

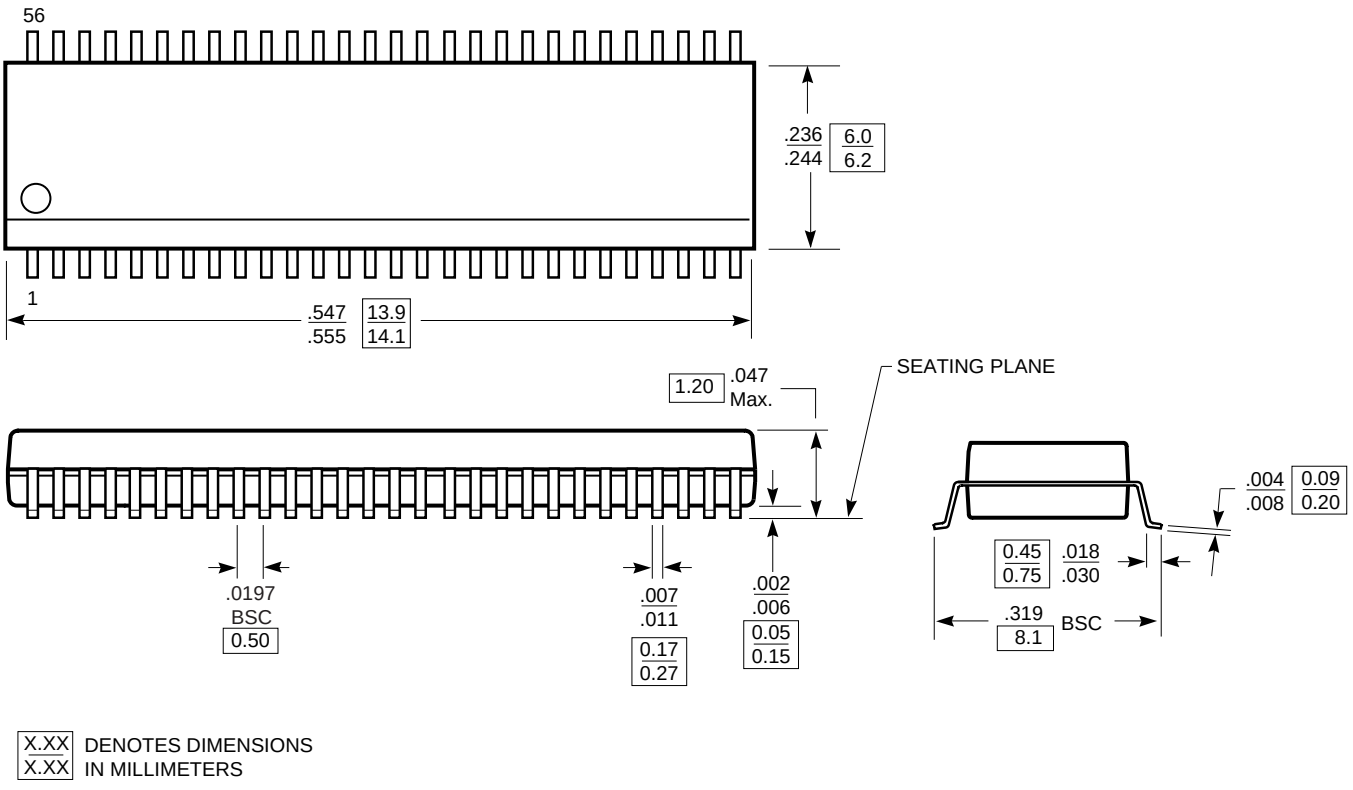
Notes:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤100MHz, Z_O = 50 Ohm, t_r ≤1.2ns, t_f ≤1.2ns.
3. The outputs are measured one at a time with one transition per measurement.



Phase Error and Skew Calculations

Package Mechanical Information: Plastic 56-pin Thin Shrink Small-Outline Package (A package)



Ordering Information

Part Number	Ordering P/N	Package
PI6C2520	PI6C2520A	56-Pin TSSOP