L64118 MPEG-2 Transport Controller with Embedded MIPS CPU (TR4101)

Preliminary Datasheet

LSI Logic's L64118 MPEG-2 Transport Controller with Embedded MIPS CPU (TR4101) is a highly integrated set-top box control and communication device, combining most of the logic needed for a digital broadcast system (DBS) or cable set-top box onto a single chip. The L64118's embedded 32-bit TinyRISC™ MIPS CPU core provides processing power to support transport and system data, as well as general-purpose system control.

The L64118 interfaces directly to LSI Logic's L64704 and L64724 (satellite), and the L64768 (cable) single-chip channel decoders, as well as to the L64105 MPEG-2 A/V decoder.

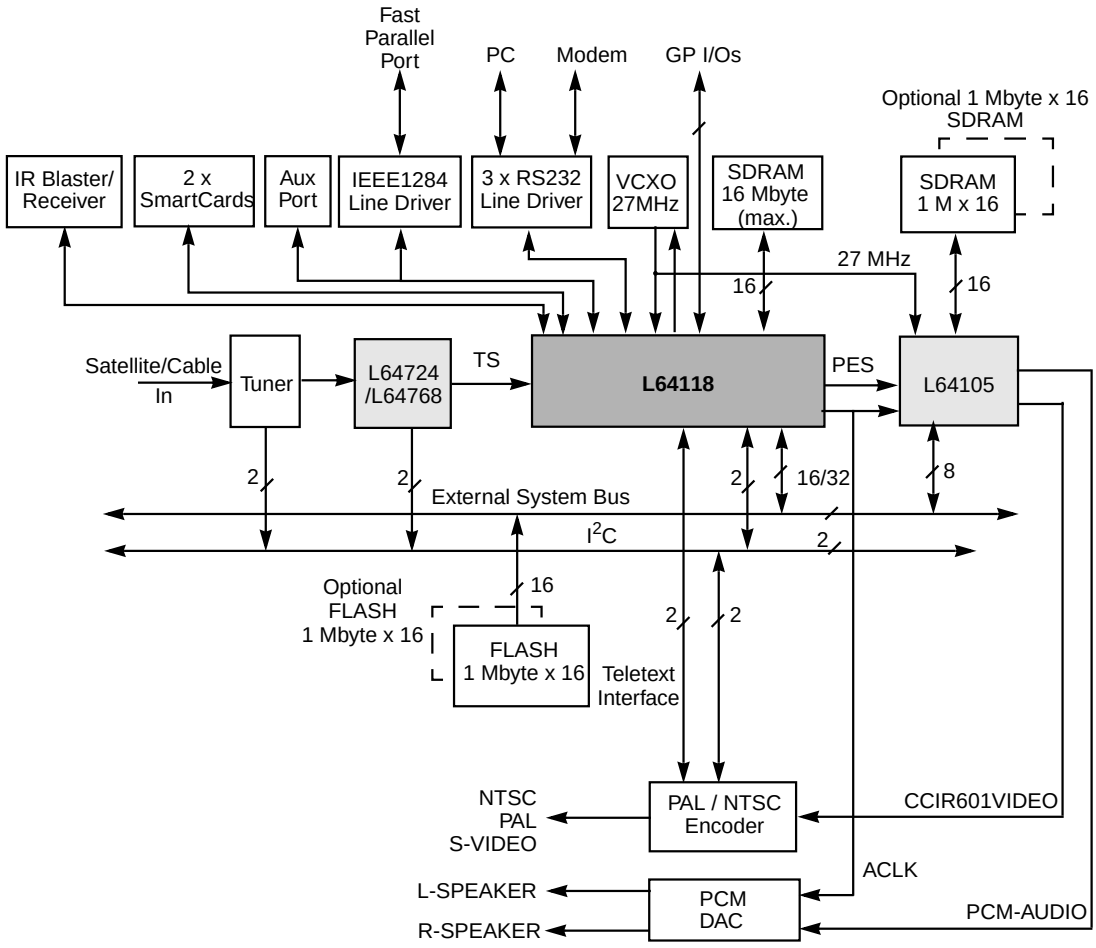
The MPEG-2 transport and system demultiplexer can handle 32 Packet Identifications (PIDs) simultaneously, including audio, video, and general-purpose data services. It integrates a Digital Video Broadcasting (DVB)-compliant descrambler block, substantially increasing the security of the set-top box.

The L64118's synchronous External System Bus (EBus) communicates with external peripherals. The L64118 communicates with peripherals through serial, parallel, SmartCard, and infrared ports. Several general-purpose I/O pins are provided that let system designers expand the system's capabilities.

The L64118 supports industry-standard SDRAM memory of up to 16 Mbytes, using 16 and 64 Mbit SDRAMs. The SDRAM interface supports PC66/100-compliant SDRAMS.

The L64118 is offered in LSI Logic's 3.3 V G10®-p cell-based technology and is packaged in a 256-pin PBGA (IF) package.

Figure 1 Typical Set-Top Box Using the L64118



The L64118's embedded 32-bit MIPS CPU (TR4101) runs at 54 MHz. The chip's CPU block is 32 bit, while the bus interface to external memory (through the SDRAM controller) is 16 bit. The CPU can run MIPS16 and MIPS32 instructions. The 32-bit operations allow high-performance operation, while 16-bit operations allow for code optimization and memory savings. Since most transport processing and filtering is implemented in hardware, much of the CPU's processing power can be devoted to system processing.

The L64118 processes the transport data packets in the PID Processing Unit (PPU) according to the MPEG-2 standard draft 13818-1, making Packetized Elementary Stream (PES), Program Specific Information (PSI), Service Information (SI), and Private data available to the system. It also buffers and transfers audio and video PES data packets to the external decoder device.

The L64118 interfaces directly to LSI Logic's L64105 MPEG-2 A/V decoder. It outputs demultiplexed audio and video PES streams for processing by the L64105. This decoder's extended channel buffer feature lets you use part of the L64118 SDRAM space to store A/V PES data directed to the L64105. One benefit of this is that it lets you free memory in the L64105 and increases its On-Screen Display (OSD) capability.

The L64118 also interfaces directly to LSI Logic's family of single-chip channel decoders (L64704, L64724, and L64768), which allows channel data to be transferred in parallel or serial modes. The L64118 implements an automatic sync locking mechanism with a programmable hysteresis function for reliable locking onto MPEG-2 (0x47) transport packet sync bytes.

The External System Bus (EBus) is a general-purpose, 32-bit wide system bus. It is controlled by the L64118 for communication with external components in the system. This bus provides the system designer with an interface that permits the glueless connection of devices such as FLASH, ROMs, and external peripherals.

The L64118's peripheral interface blocks let you connect external systems directly to the set-top box. The RS232 ports let you connect a PC, modem, or terminal directly to the chip. The IEEE1284 parallel port lets you connect to fast peripheral devices and transfer filtered transport packets. The IEEE1284 parallel port includes an on-chip DMA controller for expediting data transfers between memory to, and from, the port.

The L64118 includes an infrared transmitter (blaster) port for applications such as (remotely) programming a VCR, as well as two independent infrared receiver ports, which can be used to program the set-top box using a remote controller.

The 27 MHz system clock drives the L64118 internal demultiplexer block, as well as most of the peripheral modules. The PLL block generates 54 MHz from the 27 MHz system clock to drive the CPU logic.

The L64118 includes four DMA channels (one dedicated to the IEEE1284 port, three independent) that can be used to transfer data between peripheral ports and memory, from one memory location to another, or from memory to an external system device.

Features

The L64118 provides additional system features for a set-top box application, including:

Channel

- Compliance with ISO/IEC 13818-1 (MPEG-2) Transport specifications
- Sustained rates up to 90 Mbits/s serial and up to 13.0 Mbytes/s parallel transport stream input interface
- Direct interface to LSI Logic single-chip channel decoder devices, such as the L64704, the L64768, and the L64724

Demux

- PID filtering (32 user-programmable PIDs)
  - Hardware-assisted section filtering for 30 general-purpose PIDs (PSI, SI, and Private)
  - Each filter includes 12 match bytes and 12 mask bytes
  - Each PID can select up to 32 filters simultaneously
- Support of a Program Clock Reference (PCR) PID
- CRC32 in parallel to all sections in the filtering process
- Descrambler core compliant to DVB common scrambling specifications
- Support for transport-level and PES-level descrambling
- Seamless support of scrambled and unscrambled data
- Support of up to 12 pairs of 64-bit keys

- Two 256-byte transport buffers for supporting audio and video PES streams
- 32 programmable cyclic buffers in SDRAM memory assignable to a PID or section filter index
- Support for an additional programmable cyclic buffer in SDRAM to post data to adaptation fields
- Program Clock Reference (PCR) recovery and locking
- Automatic detecting and switching of audio and video PIDs on splice points
- Audio oversampling (256 or 384 times oversampling) clock generation

CPU and Subsystems

- Integration of the CPU system:
  - 32-bit TR4101 54 MHz TinyRISC CPU
  - MIPS16 and MIPS-II instruction set compatible
  - Four Kbyte Data (direct mapped) and Eight Kbyte (two-way set associative) instruction cache
  - Basic Bus and Cache Controller unit (BBCC)
  - Multiply/Divide Unit (MDU)
  - Debugger Building Module (DBX)
  - 32-bit Timers and Interrupt Controller
  - In-Circuit Emulator (ICE) port
- Two interrupt handling modes:
  - Interrupt Compatibility mode supports 12 interrupt ports and six main interrupt levels. This mode is compatible with the L64108 interrupt structure.
  - Interrupt Extension mode supports 25 interrupt ports with a software index to each interrupt source. This new mode can reduce interrupt latency.

Peripherals

- Programmable audio clock generator for oversampling audio DAC (ACLK)
- Three RS232 serial I/O channels
- IEEE1284 parallel interface port (shared with the Aux port)
- Two ISO7816 SmartCard interfaces
- Two Infrared (IR) receivers
- One IR transmitter
- Auxiliary (Aux) fast input/output port with multiple configurations and settings (shared with the IEEE1284 port)
- Teletext serial interface port with direct interface to NTSC or PAL encoders
- I^2C-compatible interface port supporting multimaster or slave modes for interfacing to external devices
- Four DMA channels (one dedicated to IEEE1284 port, three independent)
- Synchronous extension bus
  - 32-bit external addressing
  - 8-/16-/32-bit data bus width
  - Multiplexed address/data as well as eight demultiplexed address pins
  - Synchronous to a 27 MHz output clock
- Up to 47 general-purpose pins
- Six programmable chip-select output signals (five dedicated and one multiplexed)
- Enhanced serial I/O for modem use

SDRAM Controller

- SDRAM Controller supports 16 and 64 Mbit SDRAM devices
- SDRAM Controller support for up to 16 Mbytes

General

- On-chip PLL (54 MHz) with internal loop filter
- JTAG support
- 256-pin Plastic Ball Grid Array (PBGA) Package
- Commercial temperature range 0 °C–70 °C ambient
- Low-power, 3.3 V (± 10%) process

Architectural Overview

The components of the L64118 are integrated to provide a complete system solution for demultiplexing and processing incoming MPEG-2 Transport Stream packets. Figure 2 shows the three main blocks of the L64118: the TR4101 CPU and associated core building blocks, the transport (demultiplexer) block, and the peripheral device interfaces.

Additionally, the L64118 has three main buses:

- Basic Bus (BBus)

  The BBus is an internal 32-bit bus that connects the CPU core and building blocks with internal memory and peripherals through the CPU-to-Peripheral (C2P) bridge.

- Peripheral Bus (PBus)

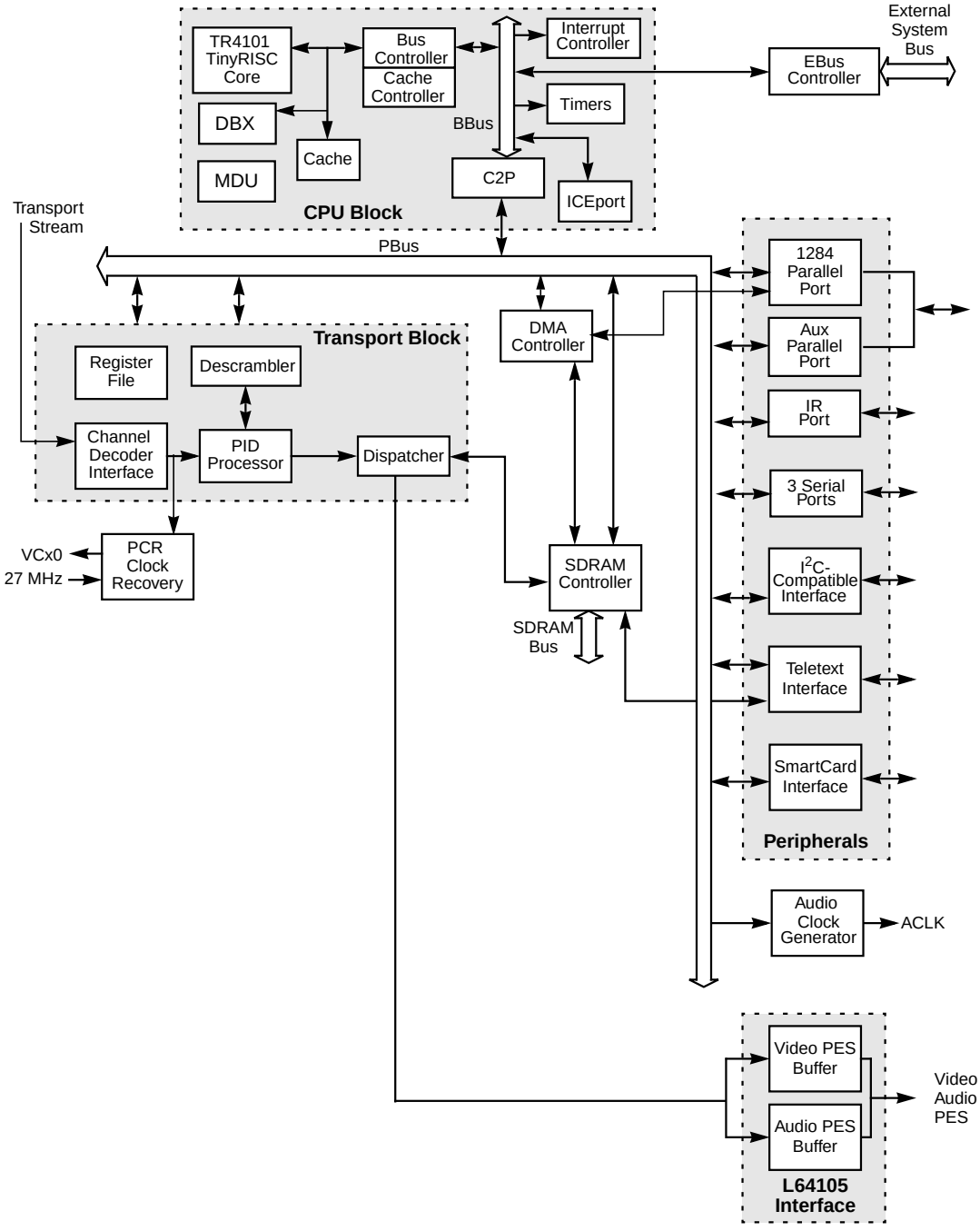
  The PBus is the internal peripheral bus; it links the CPU to SDRAM memory, internal peripheral devices, and the demultiplexer using the C2P bridge.

- External System Bus (EBus)

  The EBus is a general-purpose 16- and 32-bit synchronous system bus that lets the L64118 communicate with external components in the system. The EBus connects to the BBus through the EBus controller.

The following subsections provide an overview of the chip's main blocks.

Figure 2 L64118 Internal Block Diagram



TinyRISC MIPS CPU Core

With its powerful MIPS CPU, the L64118 can support all of the system's general-purpose control requirements, including:

- Complete set-top system initialization and testing
- Security handling
- Communication ports protocol processing
- Remote control handling
- PCR recovery and locking
- Audio/video synchronization for lip-syncing

The CPU also supports transport and system data software processing on data posted to the SDRAM by the transport processing block. This includes operations such as:

- PSI and DVB SI table maintenance (Program Association Table (PAT), Conditional Access Table (CAT), Program Map Table (PMT), Network Information Table (NIT))
- Private Section filtering
- Subtitle processing and OSD overlay
- Closed caption and teletext
- Electronic Program Guide

The MIPS CPU in the L64118 has more than enough processing power to implement all the tasks listed above.

The CPU core can be programmed with 16- or 32-bit instructions. The 32-bit operations allow high-performance operation; using the 16-bit architecture permits a reduced code size, saving memory. Both 16- and 32-bit instructions can be used in the same design.

The L64118's TR4101 MIPS CPU is part of LSI Logic's CoreWare® technology. The chip integrates the complete CPU subsystem, including:

- CPU (TR4101)
- Cache memory for instruction (2 x 4 Kbyte) and data (4 Kbyte) cache
- Basic BIU and Cache Controller (BBCC)
- Timers (including watchdog timer)
- Interrupt Controller
- Debugger Building Module (DBX)
- Multiply/Divide Unit (MDU)
- ICE port (full-duplex, serial receive and transmit port)
- CPU-to-Peripheral bus (C2P)

The L64118's embedded 32-bit MIPS CPU runs at 54 MHz. This clock rate permits a peak processing rate of 54 MIPS. The chip's internal CPU core is implemented in 32-bit architecture, but it can execute both 16-bit and 32-bit instructions. The L64118 has a 16-bit data interface to external SDRAM, and a 32-bit data interface to the external system bus (EBus). The CPU operates in Big Endian[1] mode.

Since most transport processing and filtering is implemented in hardware, much of the CPU's processing power can be devoted to system processing. The chip includes address decoding logic for directly interfacing to external memory (FLASH, SDRAM) without requiring external glue logic.

The interface between the CPU subsystem and the rest of the L64118 is implemented by the C2P unit. The C2P module translates 32-bit data accesses by the CPU to 8- and 16-bit data accesses on the Peripheral Bus, which connects all other blocks. The PBus is synchronous to the 27 MHz system clock.

Transport Demultiplexer Block

The transport demultiplexer block processes the transport stream data coming from the channel interface. The input of the L64118 transport block interfaces to the channel decoder; the output interfaces to the

1. Big-Endian means that the address of a multiple-byte data type is the address of its most significant byte.

SDRAM controller module. The block includes a PID processor unit (PPU) that is compliant with DVB and JSAT and meets the requirements of many other service providers, including Canal+, SkyPerfect, and BSkyB.

The unit can process up to 32 PIDs simultaneously. It provides extensive filtering of PSI, SI, and Private Sections. The PSI, SI, and Private Sections are filtered according to 32 user-programmable match/mask PIDs. Section data that passes filtering is stored in cyclic buffers (in off-chip memory) associated with each PID. Each section in each PID can be filtered against 32 filters. (Every section undergoes a CRC32 check. An enable bit controls the CRC checking of all section types.) The on-chip descrambler unit increases system security. The audio and video data are reduced to PES streams and delivered to the A/V decoder.

SDRAM Controller

The SDRAM controller and resource arbitration logic makes efficient use of SDRAM bandwidth. This chip's low-cost system implementation approach dictates usage of the external SDRAM for both transport and general system functions. The L64118 supports various SDRAM configurations using 16 Mbit and 64 Mbit devices, for a total memory size of 2, 8, or 16 Mbytes of external SDRAM.

The SDRAM controller arbitrates access to the external SDRAM. This logic provides the maximum possible SDRAM bandwidth to the on-chip CPU without increasing the need for buffers or other resources.

External System Bus (EBus)

The External System Bus is a general-purpose 16- and 32-bit system bus used for communication with external components in the system. This bus provides the system designer with an interface that permits the glueless connection of devices like FLASH, ROMs, and external peripherals.

The EBus comprises a 32-bit wide interface with multiplexed address and data. Eight address bits are available as demultiplexed bits for easy interface to devices that do not need the full address space. In addition a demultiplexed mode can be configured to provide a 24-bit address and 16-bit data bus.

The EBus controller registers let the user program customized timing for each address space used in a given system. Six address spaces are supported, each with a dedicated chip select output.

The main features of the EBus are:

- 32-bit physical addressing space
- 32-bit data width
- Synchronized to 27 MHz clock
- Five external interrupt ports

The EBus supports the following main signals:

- 32-bit multiplexed address/data
- 8-bit demultiplexed (low order) address bits
- RDn
- WRn
- EACKn
- ALE (Address latch enable)
- Five dedicated chip-selects and one multiplexed (with memory strobe) chip select
- 4-bit byte enable bus
- 27 MHz output clock

Peripherals

The L64118 integrates several serial and parallel ports, providing a high degree of connectivity to various types of peripherals. The communication ports include:

- Three 8251 RS232 serial communication ports connect the set-top box to a dumb monitor, modem, or PC. The modem communicates between the subscriber and the main station, or back channel.

  One serial I/O includes a V24-compatible UART for a glueless connection to modem datapump ICs.

- One IEEE1284 parallel communication port for fast communication with a PC or workstation. The L64118 includes an on-chip DMA controller dedicated for data transfers between the IEEE1284 parallel communication port and the main memory.
- One I^2C-compatible serial communication port to communicate with devices using I^2C data links. This type of bus is common in video encoders, audio DACs, remote control devices, and RF tuners.
- Two independent SmartCard ports ISO-7816-3 compliant SmartCard ports interface through a SmartCard coupler, and support the T = 0, T = 1 asynchronous protocol. The ports also feature V_{CC}, V_{PP} control.
- One Teletext port that interfaces to an NTSC or PAL encoder and allows for direct insertion of teletext data into an NTSC or PAL video encoder device. The teletext data usually is transmitted using a special-purpose PID. The data is then extracted by the Transport processor and posted to SDRAM. Finally, the L64118 controller transfers the teletext data to the Teletext port upon request from the video encoder device. The Teletext port includes a FIFO between the real-time timing required on the output pins and the internal data transfer.
- An Aux parallel port for outputting/inputting transport packets from/to the internal demultiplexer. The port's direction is controlled through a configuration bit or through the AUXTX input pin. The port can be programmed to deliver or receive transport packets at various points within the demultiplexer's pipeline. This port is multiplexed with signals from the IEEE1284 port.
- An Infrared port with a single IR blaster with two identical output pins and two identical, yet independent, IR receiver modules. The IRT (transmitter) can be used to communicate with off-board elements (e.g., to program a VCR). The two IR receivers, IR0 and IR1, support remote control of the STB.
- Forty-seven general-purpose I/O pins (GPIOs) are configurable and can be used to control and monitor a subset of processor functions, thus easing system integration and minimizing external glue logic. Forty-one of these I/Os are multiplexed, six are dedicated GPIOs.

DMA Controller

The L64118 integrates a four-channel DMA controller that reduces a major portion of the load the CPU might incur during data transfer between peripheral ports, memory, and elements residing on the EBus.

One DMA channel is dedicated for data transfers between the IEEE1284 port and main memory. The other three DMA channels are general-purpose. One general-purpose DMA channel (Channel #1) supports transfers between PBus and Ebus devices.

In typical applications, one DMA channel can be assigned to a SmartCard, one channel to a serial port, and one to memory to memory data transfers.

Addressing

The MIPS architecture uses two types of addresses: virtual addresses (used in a program), and physical addresses (that appear on an address bus). This allows support of kernel and user modes, while combining cacheable and noncacheable addresses.

Virtual addresses are partitioned into four, fixed-size segments: *kuseg*, *kseg0*, *kseg1*, and *kseg2*, according to Table 1.

Table 1 Memory Segment Address Mapping

Virtual CPU Address [31:29]	Segment	Size
0b000–0b011	kuseg	2 Gbytes
0b100	kseg0 (cache)	512 Mbytes
0b101	kseg1 (noncache)	512 Mbytes
0b110–0b111	kseg2 (not used)	1 Gbytes

The *kuseg* addresses are accessible in user and kernel mode; they are for use by user-mode programs, while also providing direct access (requiring no system call) to those same addresses in kernel mode.

Because the L64118 does not have a Memory Management Unit (MMU), *kuseg* addresses are mapped unchanged to physical addresses. The L64118 does not map *kseg2*; thus, *kseg2* addresses cannot be used by

the programmer. Noncacheable *kseg1* addresses are used for accessing peripheral registers and for code that requires noncacheability (for example, initialization code that is executed before the caches have been flushed). Cacheable *kseg0* addresses are used for all other code.

The on-chip CPU performs virtual to physical address translation; the resultant 32-bit physical addresses are output on the internal BBus. The CPU to Peripheral (C2P) bridge module maps the 32-bit BBus address to the internal 24-bit PBus address. The EBus interface module (which resides on the internal BBus) maps the 32-bit BBus address to the 24/32[1]-bit EBus address, according to the mode in which the EBus interface is configured and the width of the area being accessed.

The L64118 supports a 16 or 32 Mbyte physical address space (depending on the size of the SDRAM supported in the system). Virtual addresses in *kseg0* and *kseg1* are always mapped to the same physical addresses, namely to the lowest 16 (or 32) Mbytes of physical memory. The programmer can differentiate between cacheable and noncacheable addresses by using a virtual address either in *kseg0* or *kseg1* (e.g., PSI/PES data is stored in a noncacheable location, since they are posted by the PID processor).

As part of the CPU subsystem, the L64118 a small module (the MMU Stub) that maps the *kseg0* and *kseg1* segments to the same physical address. It does this by clearing the three most significant bits of the address in the *kseg0* and *kseg1* segments presented by the CPU (on the internal CPU bus). Segments *kuseg* and *kseg2* are unaffected by the MMU Stub.

Note that the L64118 CPU operates only in Big-Endian mode; the Ebus must be set to operate in Big-Endian mode. A strap option on the GPIO[42] pin (sampled during reset) determines the physical connection on the EBus.

1. The EBus uses either a 24-bit address or a 32-bit address, depending on the address space being accessed.

The address space of the L64118 is partitioned into the following areas:

- CPU/Peripheral
  This address space contains the control and status registers for the CPU and core building blocks.
- Configuration Register Space
  The space contains registers that define the configuration of each peripheral on the PBus. It is partitioned into 1 Kbyte segments, where each segment corresponds to the Configuration register entry for each PBus component. See Table 3.
- Attribute Register Space
  The Attribute register space contains the Attribute register 0 for each peripheral on the PBus. This space is partitioned into 1 Kbyte segments, where each segment corresponds to the Attribute register entry for each PBus component. See Table 3.
- Internal I/O
  The internal I/O space contains I/O registers and functions for each peripheral on the PBus. It is partitioned into 256 4 Kbyte segments, where each segment corresponds to an I/O entry for a PBus component. See Table 3.
- External ROM
  External ROM contains the operating system, user's application programs (*kseg0*), configuration code, and initialized data (*kseg1*).
- External space for the EBus

  The external space is used for user-defined external memory and external devices residing on the EBus. It is divided into three subspaces, each one supporting devices with a different width (8, 16, 32 bits).
- Primary SDRAM
  The lowest 2/8/16 Mbytes of addressable space are mapped to the external SDRAM through the internal SDRAM controller. See Table 2, “PBus to EBus Address Mapping,”

Table 2 PBus to EBus Address Mapping

118 EBus	PBus Address
2 Mbytes SDRAM	0x0000.0000–0x1F.FFFF
8 Mbytes SDRAM	0x0100.0000–0x017F.FFFF
16 Mbytes SDRAM	0x0100.0000–0x01FF.FFFF

Note that the PBus addresses are not driven on the EBus, but rather are routed to the SDRAM controller. The two Mbyte and eight Mbyte mode are software compatible with the L64108 code, since the External Space 2 (ES2) of the L64108 is located at PBus address 0x0080.0000 (by default).

Table 3 summarizes the L64118 address space.

Table 3 L64118 Address Mapping

Virtual CPU Base Address		BBus Base Address	Address Space Name	PBus/EBus Physical Base Address	Size (Mbytes)
Noncache kseg1	Cache kseg0				
0xBFFF.0000	N/A	0x1FFF.0000	CPU/Peripheral (Reserved[1])	Not used	0.50
0xBFF8.0000	N/A	0x1FF8.0000	Not used	Not used	0.50
0xBFF4.0000	N/A	0x1FF4.0000	Internal Configuration Registers	0xF4.0000 (PBus)	0.25
0xBFF0.0000	N/A	0x1FF0.0000	Internal Attribute Registers	0xF0.0000 (PBus)	0.25
0xBFE0.0000	N/A	0x1FE0.0000	Internal I/O	0xE0.0000 (PBus)	1
0xBFC0.0000	0x9FC0.0000	0x1FC0.0000	External ROM	0xC0.0000 (EBus demux mode)	2
0xB800.0000[2]	0x9800.0000	0x1800.0000	8-bit devices in the External Space	0x00.0000 (EBus demux mode)[3]	≤ 64
0xB400.0000[4]	0x9400.0000	0x1400.0000	16-bit devices in the External Space	0x00.0000 (EBus demux mode)[5]	≤ 64
0xB000.0000[6]	0x9000.0000	0x1000.0000	32-bit devices in the External Space	0x1000.0000 (EBus mux mode)[7]	≤ 64

Table 3 L64118 Address Mapping (Cont.)

Virtual CPU Base Address		BBus Base Address	Address Space Name	PBus/EBus Physical Base Address	Size (Mbytes)
Noncache kseg1	**Cache kseg0**				
0xA000.0000	0x8000.0000	0x0000.0000	Primary SDRAM when 2 Mbytes of SDRAM is used	0x0000.0000 (PBus)	2
0xA000.0000	0x8000.0000	0x0000.0000	Primary SDRAM when 8 or 16 Mbytes of SDRAM is used	0x0100.0000 (PBus)	8 or 16

1. These transactions do not appear on the PBus. This space is used only when the CPU accesses BBus components (BBCC, Timer, C2P, INTC, ICEport).
2. Within this range, used for 8-bit devices, specific address ranges can be selected (and the mode in which they are accessed) using the Ebus address compare registers.
3. Bits [23:0] of the BBus address are reflected onto the EBus Address bus for eight-bit devices.
4. Within this range used for 16-bit devices, specific address ranges can be selected (and the mode in which they are accessed) using the EBus Address Compare registers.
5. Bits [23:0] of the BBus address are reflected onto the EBus Address bus for 16-bit devices.
6. Within this range used for 32-bit devices, specific address ranges can be selected (and the mode in which they are accessed) using the EBus Address Compare registers.
7. Same address used on the EBus and BBus when 32-bit devices are accessed.

Signals

This section describes the signals used by the L64118. Figure 3 shows the L64118 non-GPIO mode signals in functional groups and Figure 4 shows the L64118 GPIO mode signals. The signals are described by group. Within each group, signals are listed in alphabetic order.

Figure 3 L64118 I/O Signal Summary (Non-GPIO Modes)

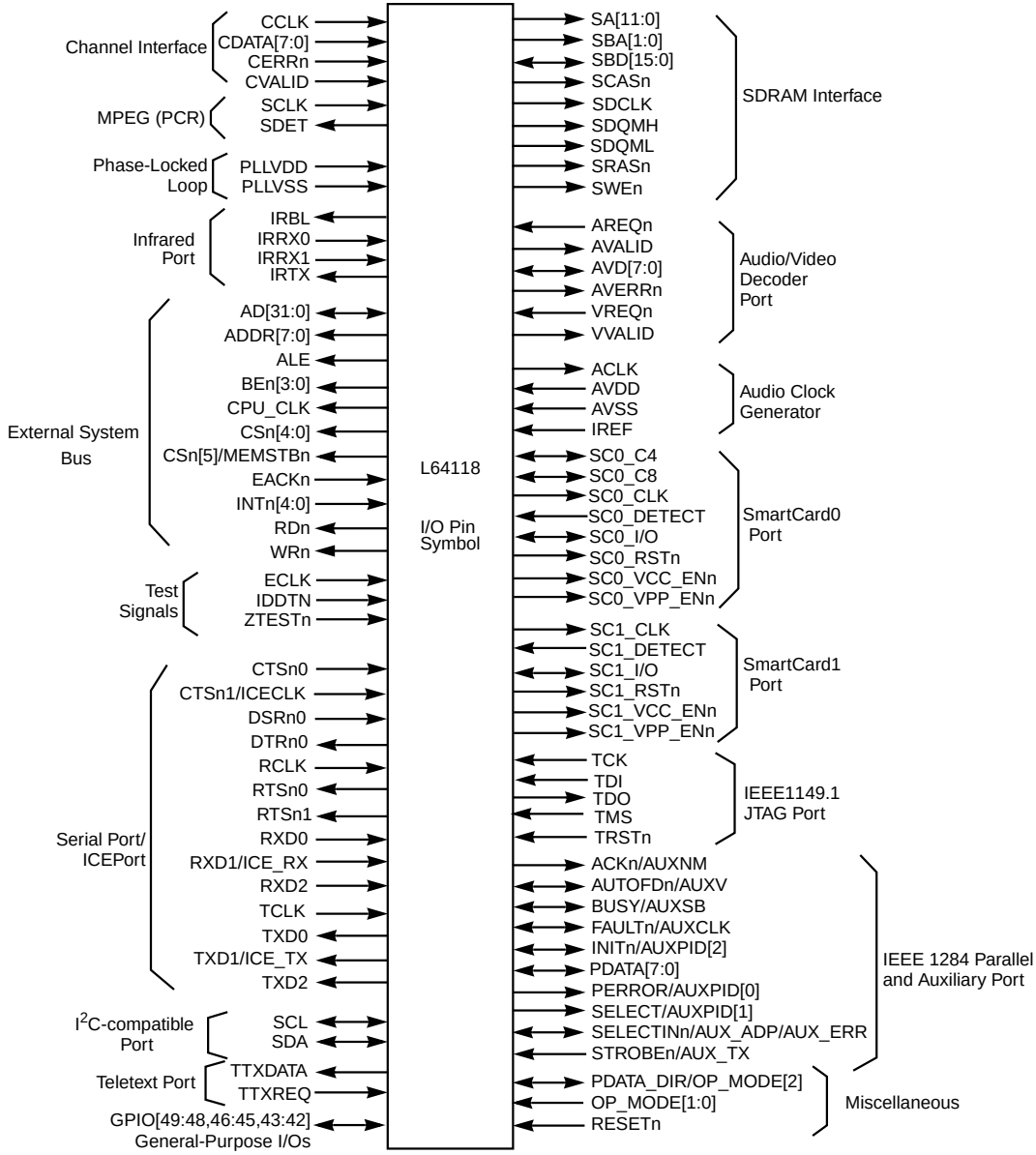


Figure 4 L64118 I/O Signal Summary (GPIO Mode)

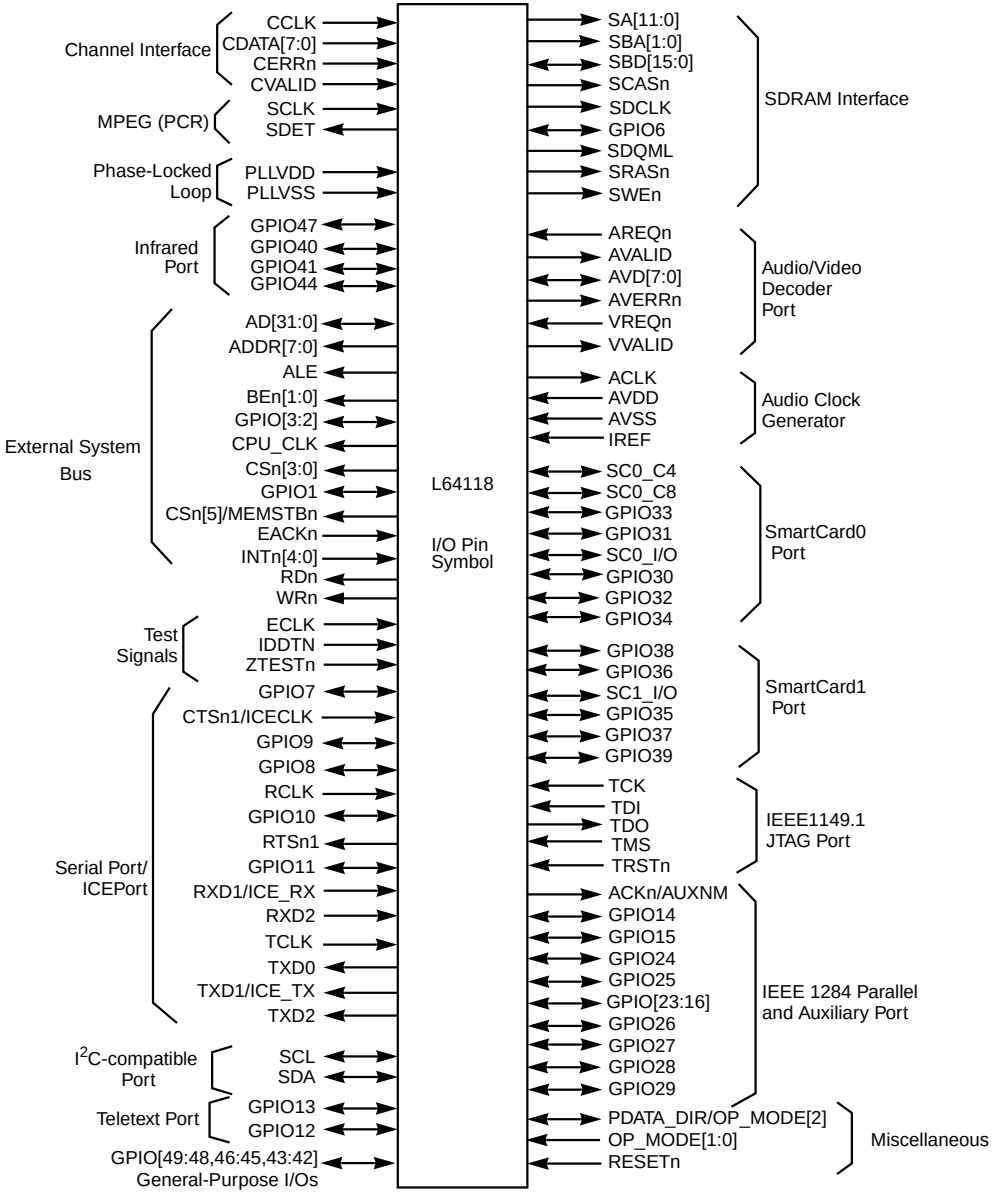


Table 4 lists the default values of the output and bidirectional signals. Note that during reset, all bidirectional signals (and some output signals) are floating.

Table 4 Default Values for L64118 Output and Bidirectional Signals After Reset[1]

Signal	Default Value	Notes
ACKn/AUXNM	not asserted	
ACLK	inactive (LOW)	
AD[31:0]	driving an unknown value	
ADDR[7:0]	driving an unknown value	
ALE	not asserted	
AUTOFDn/AUXV	not asserted	
AVALID	not asserted	
AVD[7:0]	driving an unknown value	
AVERRn	not asserted	
BEn[3:0]	not asserted	
BUSY/AUXSB	not asserted	
CSn[4:0]	not asserted	
CSn[5]/MEMSTBn	not asserted	
DTRn0	not asserted	
FAULTn/AUXSB	not asserted	
GPIO42, 43, 45, 46, 48, 49	floating	
INITn/AUXPID[0]	not asserted	
IRTX	not asserted	
PDATA_DIR/ OP_MODE[2]	drives assertion	
PDATA[7:0]	floating	
RDn	not asserted	

Table 4 Default Values for L64118 Output and Bidirectional Signals After Reset[1] (Cont.)

Signal	Default Value	Notes
RTSn0/1	not asserted	
SA[11:0]	driving an unknown value	
SBA[1:0]	driving an unknown value	
SBD[15:0]	floating	
SC0_C4, SC0_C8	pulled up by an external pull-up resistor	
SCASn	not asserted	
SCx_CLK	not asserted	
SCx_DETECT	floating	serves as an input
SCx_IO	pulled up by an external pull-up resistor	
SCx_RSTn	not asserted	
SCx_VPP_ENn	not asserted	
SCx_VCC_ENn	not asserted	
SCL	pulled up using an external pull-up resistor	
SDA	pulled up using an external pull-up resistor	
SDCLK	toggling	
SDQMH	not asserted	
SDQML	not asserted	
SRASn	not asserted	
SWEn	not asserted	

Table 4 Default Values for L64118 Output and Bidirectional Signals After Reset[1] (Cont.)

Signal	Default Value	Notes
TTXREQ/GPIO12	floating	behaves as an input
TTXDATA	not asserted	
TXD0/2	asserted	
TXD1/ICE_TX		
VVALID	not asserted	
WRn	not asserted	

1. A few cycles after reset (RESETn is driven HIGH), the L64118 initiates a transaction on the EBus, changing some of the default values in this table.

Channel Interface Port

These signals provide the physical connection to Channel Interface devices, such as LSI Logic's L64724 or L64768. This port supports both parallel and serial connections.

CCLK **Channel Clock** **Input**
When CVALID is asserted HIGH, the L64118 latches CDATA[7:0] on the rising edge of CCLK. In serial mode, the L64118 uses only CDATA[0]. In serial mode, the maximum clock rate is 60 MHz; in parallel mode, it is 13 MHz. The CCLK must toggle during reset to ensure proper reset of the channel interface block.

CDATA[7:0] **Channel Data** **Input**
These signals deliver channel information to the L64118. When CVALID is asserted, the chip latches the data on every rising edge of CCLK. When the L64118 is in parallel input mode, all CDATA[7:0] signals deliver data. When the L64118 is in serial mode, only CDATA[0] delivers data.

CERRn **Channel Data Error** **Input**
This active LOW input signal indicates that an uncorrected error occurred in the preceding channel interface. When CVALID is asserted, CERRn is latched on the rising edge of CCLK.

CVALID **Channel Data Valid** **Input**
This active HIGH input signal indicates that CDATA[7:0] and CERRn are carrying valid data. When CVALID is asserted, a rising edge of CCLK latches the CDATA[7:0] signals into the L64118.

MPEG Program Clock Reference (PCR) Recovery

These signals recover the Program Clock Reference (PCR). They interface to the external VCxO, which provides the 27 MHz clock to the decoder.

SCLK **27 MHz System Clock** **Input**
This input provides the clock signal to the L64118. It must be driven by the external 27 MHz VCxO (the voltage control input is controlled by SDET and the external RC filter).

SDET **System Clock Sigma-Delta Control Voltage** **Output**
This converter output signal from a 16-bit Sigma-Delta modulator inside the L64118 drives a simple low-pass filter to produce an analog control voltage to an external VCxO.

Phase-Locked Loop (PLL)

These signals supply power and ground to the internal PLL, which generates the internal 54 MHz CPU clock from the external 27 MHz SCLK input. The 54 MHz internal clock is then divided by two to generate the internal 27 MHz clock used by other internal modules. Isolate the PLLVDD and the PLLVSS signals from digital noise and digital logic on the PCB using layout and bypass filtering techniques.

PLLVDD **PLL Analog VDD** **Input**
This provides a separate filtered 3.3 V to the PLL circuit through PLLVDD so that switching noise from the digital portion of the chip can not affect PLL stability.

PLLVSS **PLL Analog VSS** **Input**
This provides a separate ground to the PLL circuit through PLLVSS so that switching noise from the digital portion of the chip does not affect PLL stability.

External System Bus (EBus)

The EBus comprises a 32-bit wide interface with multiplexed address and data. Eight address bits are available as demultiplexed bits for an easy interface to devices that do not need the full address space. All bus transactions are synchronous to the 27 MHz output CPU_CLK.

A subset of these signals can be programmed to act as general-purpose I/O signals by setting bit [0] in the General-Purpose Mode register.

AD[31:0] **Multiplexed Address/Data Bus** **Bidirectional**
AD[31:0] is the multiplexed address/data bus. The L64118 can be programmed to drive the full address on this bus at access start. After this address phase the bus presents write data for a write or the external device drives data on the bus in a read.

ADDR[7:0] **Demuxed Address Bus** **Output**
ADDR[7:0] provides eight bits of demultiplexed address bits. This bus allows some designs to remove the external address latch on the multiplexed address/data bus to hold the address throughout the transaction. The EBus uses byte addressing. All 16-bit devices must ignore ADDR[0]. All 32-bit devices must ignore ADDR[1:0].

ALE **Address Latch Enable** **Output**
This active HIGH signal controls the latches for demultiplexing the address from the AD bus.

BEn[1:0] **Byte Enables** **Output**
The four byte enable outputs are asserted during a read or write transaction on the EBus to control which of the four byte lanes are enabled. The byte lane selection is dependent on the width of the transaction (word, halfword, or byte) and the data width of the external device (32, 16, or 8 bits).

The byte enables always correspond to the same physical lines on the AD bus: BEn[1] corresponds to AD[15:8], BEn[0] to AD[7:0].

BEn[2] **Byte Enable** **Output**

The four byte enable outputs are asserted during a read or write transaction on the EBus to control which of the four byte lanes are enabled. The byte lane selection is dependent on the width of the transaction (word, halfword, or byte) and the data width of the external device (32, 16, or 8 bits).

The byte enables always correspond to the same physical lines on the AD bus: BEn[2] corresponds to AD[23:16].

GPIO2 **Bidirectional**

BEn[2] can serve as a general-purpose I/O signal (GPIO2) by setting bit 0 in the General-Purpose Mode register.

BEn[3] **Byte Enable** **Output**

The four byte enable outputs are asserted during a read or write transaction on the EBus, to control which of the four byte lanes are enabled. The byte lane selection is dependent on the width of the transaction (word, halfword, or byte) and the data width of the external device (32, 16, or 8 bits).

The byte enables always correspond to the same physical lines on the AD bus: BEn[3] corresponds to AD[31:24].

GPIO3 **Bidirectional**

BEn[3] can serve as a general-purpose I/O signal (GPIO4) by setting bit 0 in the General-Purpose Mode register.

CPU_CLK **EBus Output Clock** **Output**

This 27 MHz output clock is generated dividing the on-chip 54 MHz clock by two. This clock serves as the reference signal for all transactions on the EBus. The timing relationship between the SDCLK output clock, the 27 MHz SCLK input and the 27 MHz CPU_CLK output is unknown.

CSn[3:0] **Programmable Chip Selects** **Output**

Each chip select pin can be programmed to assert in a specific address area. These pins are used to select specific external devices according to on-chip address decoding. They make interfacing to various peripherals easier, as they can remove the need for external address decoders.

CSn[4] **Programmable Chip Select** **Output**

This pin is similar in function to the other five chip select output pins. It is used to select specific external devices according to on-chip address decoding.

GPIO1 **Bidirectional**

CSn[4] can serve as a general-purpose I/O signal (GPIO1) by setting bit 0 in the General-Purpose Mode register.

CSn[5]/MEMSTBn

Chip Select[5] or Memory Strobe **Output**

This pin is similar in function to the other five chip select output pins but holds the characteristic of being able to function as the MEMSTBn (active LOW memory strobe) signal. The MEMSTBn signal is a general-purpose signal. It can be used to indicate that a memory transaction is in progress. It is asserted in both read and write cycles. The timing on this signal is programmable.

EACKn **Target Acknowledge** **Input**

This signal indicates to the L64118 that the external device is ready to complete the current read or write cycle. The transaction will finish if both EACKn is asserted and the internal wait state generator has expired. This mechanism allows devices to extend an access beyond the number of wait states programmed for that particular address area.

EACKn can be programmed to be either active HIGH or LOW, using the XPOS bit in the CEBUSMODE register. EACKn must be deasserted before the next transaction acknowledge cycle.

For self-acknowledge devices, the external EACKn pin can be ignored, so the transaction completes when the wait state generator expires. This is controlled by the XACK bit in the CECFGn register.

INTn4 **Interrupt** **Input**
This unmaskable interrupt can be used for highest priority system needs.

INTn[3:0] **Interrupts** **Input**
These four external interrupts can be programmed to be level- or edge-triggered sensitive. Interrupts INTn[3:0] are maskable and for general-purpose use. When the L64118 receives an interrupt, the internal CPU completes the execution of the current instruction and jumps to a preprogrammed location in the memory containing the handler for this interrupt. By default, these signals are level triggered after reset.

RDn **Read** **Output**
The active LOW read strobe is asserted during read operations, and deasserted during writes.

WRn **Write Enable** **Output**
The active LOW write strobe is asserted during write operations and deasserted during reads.

Miscellaneous Signals

These general signals are not necessarily associated with a specific function or module of the L64118.

OP_MODE[1:0]
Operational Mode **Input**
These signals, along with OP_MODE[2], are used as strap options to configure various LSI Logic test modes. For normal operation, configure OP_MODE[2:0] to 0b000. That is, OP_MODE[1:0] should be tied LOW, and OP_MODE[2] should be pulled LOW with a 10 kΩ resistor.

OP_MODE[2]/PDATA_DIR
Operational Mode **Input**
This signal is used as a strap option during reset in conjunction with the OP_MODE[1:0] pins, and must be pulled LOW with a 10 kΩ resistor for proper device operation.

Parallel Data Direction **Output**
After reset, this signal serves as the PDATA_DIR output, which controls the parallel data bus buffers for the 1284 PDATA[7:0] data lines. When the 1284 port is used as an Aux port, this pin is driven HIGH.

RESETn **Asynchronous Reset** **Input**
Asserting this active LOW signal resets the L64118 to its power on state. To ensure a complete reset of the L64118, RESETn must be asserted for at least 16 SCLK cycles.

Test Signals

These signals are for LSI Logic test purposes. They must be tied to a constant value in normal operational mode.

ECLK **Connect to VSS** **Input**
This is an LSI Logic manufacturing test pin.

IDDTN **Connect to VSS** **Input**
This is an LSI Logic manufacturing test pin.

ZTESTn **Connect to VDD** **Input**
This is an LSI Logic manufacturing test pin. It is deasserted HIGH for normal chip operation.

Serial Port/ICEPort

These signals connect the L64118 to an external modem, PC, terminal, or other host that includes an RS232 interface. The L64118 contains three serial ports that comply with the asynchronous specification of the RS232 standard. The on-chip baud rate generators support the standard bit rate for serial communication.

Three of the SIO1 signals can be configured to serve the internal ICEport module.

CTSn0 **Clear to Send Port 0** **Input**
When reset LOW, this signal indicates that the external receiver is ready for data transfer through TxD0/RxD0. If the Transmit Enable bit in the SIO Command register is set HIGH when CTSn0 is reset LOW, data from the Transmit register of Port 0 is serialized through TxD0.

GPIO7 **Bidirectional**

CTSn0 can serve as a general-purpose I/O signal (GPIO7) by setting bit 1 in the General-Purpose Mode register.

CTSn1/ICECLK

Clear to Send Port1 **Input**

This pin can serve as either the Clear to Send signal of SIO1, or as the ICEport clock input for the ICEport module. The strap option on GPIO[43] controls this pin's functionality and usage. If GPIO[43] is sampled HIGH during reset, this pin serves as CTSn1.

When reset LOW, this signal indicates that the external receiver is ready for data transfer through TxD1/RxD1. If the Transmit Enable bit in the SIO Command register is set HIGH when CTSn1 is reset LOW, data from the Transmit register of Port 1 is serialized through TxD1.

Serial ICE Clock **Input**

When serial ICE mode is enabled, this pin functions as ICECLK, the synchronous ICE port clock input.

DSRn0 **Data Set Ready Port 0** **Input**

When reset to LOW, this general-purpose input control signal indicates that an external terminal device is ready for data transfer. The polarity of DSRn0 is latched in Port 0 Status register for the CPU to read.

GPIO9 **Bidirectional**

DSRn0 can serve as a general-purpose I/O signal (GPIO9) by setting bit 1 in the General-Purpose Mode register.

DTRn0 **Data Terminal Ready Port 0** **Output**

When this general-purpose output control signal is reset to LOW, data for the external terminal device is ready to be transmitted. DTRn0 can be set or reset by programming the DTR bit in the SIO Command register. By default, this signal is not asserted after reset.

GPIO8 **Bidirectional**

DTRn0 can serve as a general-purpose I/O signal (GPIO8) by setting bit 1 in the General-Purpose Mode register.

RCLK **Receive Serial Data Clock** **Input**

This signal is used for the receive clock input in the enhanced UART mode.

RTSn0 **Request to Send Port 0** **Output**

When this general-purpose, programmable control signal is reset to LOW, Port 1 is ready to send data through TxD1. This signal is set and reset by programming the RTS bit in the SIO Command register. By default, this signal is not asserted after reset.

GPIO10 **Bidirectional**

RTSn0 can serve as a general-purpose I/O signal (GPIO10) by setting bit 1 in the General-Purpose Mode register.

RTSn1 **Request to Send Port1** **Output**

When this general-purpose, programmable control signal is reset to LOW, Port 1 is ready to send data through TxD1. This signal is set and reset by programming the RTS bit in the SIO Command register.

RXD0 **Receive Data Port 0** **Input**

This signal provides serial data from an external RS232 device. Its protocol is similar to that of TxD0. The receive baud rate can be programmed in the SIO Baud Rate register. The data received on RXD0 is latched in the Receive register of Port 0.

GPIO11 **Bidirectional**

RXD0 can serve as a general-purpose I/O signal (GPIO11) by setting bit 1 in the General-Purpose Mode register.

RXD1/ICE_RX

Receive Data Port 1 **Input**

This pin serves either as the Receive port signal of SIO1, or as the ICEport receive input for the ICEport module. The strap option on GPIO[43] controls this pin's functionality and usage. If GPIO[43] is sampled HIGH during reset, this pin serves as RXD1. In that case, this signal provides serial data from an external RS232 device.

The protocol of this pin is similar to that of TxD1. The receive baud rate is determined by programming the SIO Baud Rate register. The data received on RXD1 is latched in the Receive register of Port 1. If GPIO[43] is sampled LOW during reset, then this pin serves as the receive port for the ICEport in the L64118.

Receive Data - Serial ICE Port **Input**
When the serial ICE mode is enabled, this pin functions as ICE_RX, the receive data port input.

RXD2 **Receive Data Port 2** **Input**
This signal provides serial data from an external RS232 device. The protocol of this pin is similar to that of TxD2. The receive baud rate is determined by programming the SIO Baud Rate register. The data received on RXD2 is latched in the Receive register of Port 2.

TCLK **Transmit Serial Data Clock** **Input**
This signal is used for the transmit clock in the enhanced UART mode.

TXD0 **Transmit Data Port 0** **Output**
This signal outputs data in compliance with the RS232 protocol's asynchronous specification. The transmit baud rate is determined by programming the SIO Baud Rate register. Data transmitted on TXD0 comes from the Transmit register of Port 0. By default, this signal is not asserted after reset.

TXD1/ICE_TX

Transmit Data Port 1 **Output**
This pin can serve as either the Transmit Data port signal of SIO1, or as the ICEport receive input for the ICEport module. The strap option on GPIO[43] controls this pin's functionality and usage. If GPIO[43] is sampled HIGH during reset, this pin serves as TXD1.

When set to TXD1, this signal outputs data in compliance with the RS232 protocol's asynchronous specification. The data rate on this pin is determined by programming the SIO Baud Rate register. Data transmitted on TXD1 comes from the Transmit register of Port 1.

Transmit Data - Serial ICEPort **Output**
If GPIO[43] is sampled LOW during reset, this pin serves as ICE_TX, the serial ICE transmit data output port. By default, this signal is not asserted after reset.

TXD2 **Transmit Data Port 2** **Output**
This signal outputs data in compliance with the RS232 protocol's asynchronous specification. The data rate on this pin is determined by programming the SIO Baud Rate register. Data transmitted on TXD2 comes from the Transmit register of Port 2. By default, this signal is not asserted after reset.

SDRAM Interface

The following group of signals provides the interface between the L64118 and external SDRAM devices. The SDRAM interface works with PC66/100 compliant SDRAMs. The L64118 SDRAM interface runs at 54 MHz and is capable of accessing 2, 4, 8, or 16 Mbyte memory configurations using 16 Mbit or 64 Mbit devices.

This interface has a 16-bit data bus (SBD[15:0]). The upper and lower byte mask signals (SDQMH and SDQML) control halfword and byte accesses. The SBA[1:0] outputs support two- and four-bank SDRAM devices. The L64118 automatically performs SDRAM refreshes.

The L64118 does not support the Chip Select (CSn) and Clock Enable (CKE) signals. Tie these SDRAM signals active LOW and HIGH, respectively, on the SDRAM device(s) used.

SA[11:0] **SDRAM Address Bus** **Output**
These signals carry the 12-bit SDRAM address bus. The number of row and column address bits used is programmable in the SDRAM Configuration register.

SBA[1:0] **SDRAM Bank Select** **Output**
These signals allow access to SDRAM devices with either two or four banks. The number of bank select bits used is programmable in the SDRAM Configuration register.

SBD[15:0] **SDRAM Data Bus** **Bidirectional**
This data bus is driven by the SDRAM during a read operation, and driven by the L64118 during a write operation. It is 3-stated after reset and when there are no memory accesses.

SCASn **Column Address Strobe** **Output**
This signal is the active LOW column address strobe. It is used in conjunction with the SRASn and SWEn outputs to form the SDRAM command.

SDCLK **SDRAM Clock** **Output**
This is the master SDRAM clock. All output signals are referenced to the rising edge of SDCLK. The programmable SDRAM timing parameters are expressed in SDCLK periods.

SDQMH **High Byte Mask** **Output**
This active HIGH signal is the high byte data mask, which controls the high byte input/output buffer of the external SDRAM. When asserted, it disables (masks) the high data byte of the SDRAM data bus.

GPIO6 **Bidirectional**
SDQMH can serve as a general-purpose I/O signal (GPIO6) by setting bit [0] in the General-Purpose Mode register.

SDQML **Low Byte Mask** **Output**
This active HIGH signal is the low byte data mask, which controls the low byte input/output buffer of the external SDRAM. When asserted, it disables (masks) the low data byte of the SDRAM data bus.

SRASn **Row Address Strobe** **Output**
This signal is the active LOW row address strobe. SRASn is used in conjunction with the SCASn and SWEn outputs to form the SDRAM command.

SWEn **Write Enable** **Output**
This signal is the active LOW write enable strobe. SWEn is used in conjunction with the SRASn and SCASn outputs to form the SDRAM command.

Audio/Video Decoder Port

These signals provide the interface between the L64118 and an external MPEG-2 Audio/Video decoder. This interface supports a seamless connection between the L64118 and LSI Logic's L64105 A/V decoders. It supports a serial data transfer rate up to 27 Mbits/s in serial mode, 9 Mbytes/s in parallel mode. The actual data rate is controlled by the audio and video request signals coming out from the A/V decoder device.

AREQn **Audio Data Request** **Input**
When asserted, this signal indicates that the external A/V decoder is requesting the audio bit to be clocked in to the external A/V decoder. Deassertion of AREQn indicates that the A/V decoder is not ready to accept audio data.

AVALID **Audio Data Valid** **Output**
When asserted, this signal indicates that valid audio data is available on the AVD[7:0] bus. A LOW-to-HIGH transition of SCLK causes the audio data bit on AVD to be latched in the external A/V decoder. In serial mode, AVALID is active HIGH. In parallel mode, AVALID latches data on the rising edge. This signal is not asserted after reset.

AVD[7:0] **Audio Video Compressed Data** **Bidirectional**
This bus provides data to the external A/V decoder. In serial mode, AVD[0] carries the data. In parallel mode, the entire bus carries the byte-wide data. The L64118 outputs PES audio and video data from the on-chip buffers and SDRAM buffers through AVD[7:0]. These signals drive an unknown value after reset.

AVERRn **Audio Video Data Error** **Output**
When asserted, this signal indicates that there is an uncorrected error in the bit stream entering the external A/V decoder. The L64118 generates AVERRn as a result of detection of discontinuity in the transport packets of the audio and/or video program being decoded. Usually, the discontinuity is the result of loss of packets from uncorrected errors. This signal is not asserted after reset.

VREQn **Video Data Request** **Input**
When asserted, this signal indicates that the external A/V decoder device is requesting the video bit to be

clocked in to the external A/V decoder. Deassertion of VREQn indicates that the A/V decoder is not ready to accept video data.

VVALID **Video Data Valid** **Output**
When asserted, this signal indicates that valid video data is available on the AVD line. The LOW-to-HIGH transition of SCLK causes the video data bit on the AVD[7:0] bus to be latched in the external A/V decoder. In serial mode, VVALID is active HIGH. In parallel mode, VVALID latches data on the rising edge. This signal is not asserted after reset.

Audio Clock Generator

These signals generate the oversampling audio clock, which drives the L64105 external A/V decoder and a low-cost audio DAC. The audio clock generation circuit provides oversampling audio frequencies locked to the 27 MHz program clock. The fully programmable circuit supports a wide range of oversampling audio frequencies. It is implemented using advanced mixed-signal technology.

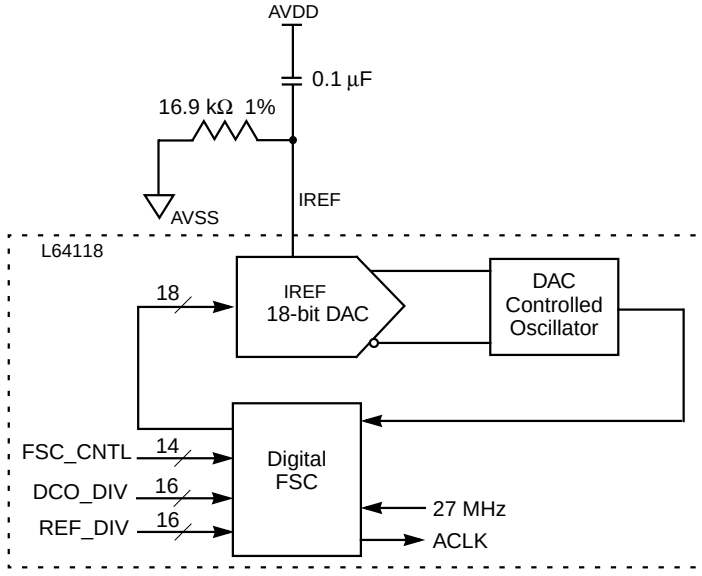
ACLK **Audio Clock** **Output**
ACLK provides the oversampling audio clock that drives the L64105 audio clock input and the system clock input pin of conventional stereo audio DAC. This signal is driven LOW after reset.

AVDD **Analog VDD 3.3 V** **Input**
AVDD provides the power voltage to the analog circuit of the audio clock generator. It must be isolated from the Digital VDD (DVDD) by a 10 µH ferrite insulator.

AVSS **Analog Ground** **Input**
AVSS provides the analog ground to the audio clock generator circuit. It should must be isolated from the digital ground supply (DGND).

IREF **Current Reference**
This pin must be connected as shown in Figure 5.

Figure 5 IREF Connection to RC Devices



IEEE 1149.1 (JTAG) Port

This group of signals drive the IEEE1149.1 Test Access Port (TAP).

TCK **Test Clock** **Input**
This is the clock pin to sample the JTAG input data.

TDI **Test Data In** **Input**
This line is for the JTAG input test data.

TDO **Test Data Out** **Output**
This line is for the JTAG output test data.

TMS **Test Mode Select** **Input**
This line lets you select between active and JTAG mode. When in JTAG mode, the I/Os are serialized. Active mode is for normal operation.

TRSTn **Test Port Reset** **Input**
When asserted LOW, this signal resets the internal JTAG controller. It does not reset the chip.

IEEE1284 Parallel Port and Auxiliary Port

These signals provide a parallel connection between the L64118 and an external peripheral device. The port complies to IEEE1284 standards and supports several modes. The 1284 mode is enabled when the AUX_SEL bit is reset (System Mode register, bit 4).

This port also serves as an auxiliary port for receiving and transmitting transport bitstreams from various points in the on-chip demultiplexer pipeline. The Aux mode is enabled when the AUX_SEL bit is set (System Mode register, bit 4).

The following list shows each pin's functionality as an IEEE1284 port and Aux port signal. Some of these pins also can serve as general-purpose I/O pins.

ACKn/AUXNM

1284 - Acknowledge **Output**
When the L64118 asserts this signal, valid data is latched in the L64118 IEEE1284 input register. By default, this signal is not asserted after reset.

Aux - Aux No Match **Output**
In Aux mode, this signal functions as AUXNM to indicate that the data being sent through the auxiliary port is for a transport packet that failed PID filtering.

AUTOFDn/AUXV

1284 - Autofeed **Input**
In 1284 mode, this pin functions as the Autofeed input.

Aux - Data Valid **Bidirectional**
In Aux mode, this pin functions as AUXV, which is used as a qualifier indicating that the data presented on the auxiliary data bus is valid.

GPIO14 **Bidirectional**
This signal can serve as a general-purpose I/O signal (GPIO14) by setting bit 3 in the General-Purpose Mode register.

BUSY/AUXSB

1284 - Peripheral Busy **Bidirectional**
In 1284 mode, this signal functions as BUSY. When this signal is HIGH, the 1284 port is not ready for a data transfer. By default, this signal is not asserted after reset.

Aux - Sync Byte **Bidirectional**
In Aux mode, this signal functions as AUXSB to indicate that the data being sent through the auxiliary port is the first byte (sync byte) of a transport packet.

GPIO15 **Bidirectional**
This signal can serve as a general-purpose I/O signal (GPIO15) by setting bit 3 in the General-Purpose Mode register.

FAULTn/AUXCLK

1284 - Peripheral Fault Operation **Bidirectional**
In 1284 mode, this signal functions as FAULTn. This signal indicates that the 1284 port encountered an error during operation. Typically, this error is due to overrun, underrun, or parity error.

Aux - Aux Port Clock **Bidirectional**
In Aux mode, this signal functions as AUXCLK, which is the reference clock for all transactions on the auxiliary port. When the Aux port is configured as an output port, this signal is an output with programmable frequencies of 13.5, 6.75 and 3.375 MHz. When the Aux port is configured as an input port, this signal is an input with a frequency based on the input transport stream data rate.

GPIO24 **Bidirectional**
This signal can also serve as a general-purpose I/O signal (GPIO24) by setting bit 3 in the General-Purpose Mode register.

INIT/AUXPID[2]

1284 - Peripheral Initialization **Input**
In 1284 mode, this signal functions as INITn. When reset LOW, this signal resets the IEEE1284 port and returns the logic to the compatibility and idle state.

Aux - Packet ID [2] **Output**
In Aux mode, this signal is part of a three-bit packet ID that can be assigned to PIDs that are output to the Aux port.

GPIO25 **Bidirectional**
This signal can also serve as a general-purpose I/O signal (GPIO25) by setting bit 3 in the General-Purpose Mode register.

PDATA[7:0] **Parallel I/O Data Signals**

1284 **Bidirectional**
In 1284 mode, these signals carry the data transferred between the host and the IEEE1284 port.

Aux **Bidirectional**
In Aux mode, PDATA[7:0] carry the transport packets from/to the L64118 demultiplexer and the Aux port.

GPIO[23:16] **Bidirectional**
These signals can also serve as a general-purpose I/O bus (GPIO[23:16]) by setting bit 3 in the General-Purpose Mode register.

By default, this signal is not asserted after reset.

PDATA_DIR/OP_MODE[2]

1284 - Peripheral Data Direction **Output**
After reset, this signal serves as the PDATA_DIR output signal that controls the parallel data bus buffers in 1284 mode. In Aux mode, this pin is driven HIGH.

Operational Mode 2 **Input**
This signal is used as a strap option during reset. For normal device operation, use a 10 kΩ to pull this signal LOW during reset.

PERROR/AUXPID[0]

1284 - Peripheral Error **Output**
In 1284 mode, this signal functions as PERROR. When HIGH, this signal indicates that the L64118 IEEE1284 port encountered an error during the data processing. FAULTn is asserted whenever PERROR is activated.

Aux - Packet ID [0] **Output**
In Aux mode, this signal is part of a three-bit packet ID that can be assigned to PIDs that are output to the Aux port.

GPIO26 **Bidirectional**
This signal can also serve as a general-purpose I/O signal (GPIO26) by setting bit 3 in the General-Purpose Mode register.

SELECT/AUXPID[1]

1284 - Peripheral Select **Output**
When set HIGH, this signal indicates that the L64118 IEEE1284 port was selected and is connected to the host.

Aux - Packet ID [1] **Output**
In Aux mode, this signal is part of a three-bit packet ID that can be assigned to PIDs that are output to the aux port.

GPIO27 **Bidirectional**
This signal can also serve as a general-purpose I/O signal (GPIO27) by setting bit 3 in the General-Purpose Mode register.

SELECTINn/AUX_ADP/AUX_ERR

1284 - Peripheral Selection Indicator **Input**
In 1284 mode, this signal (when asserted LOW) indicates that the external host is attempting to select a peripheral.

Aux - Adaptation Field Flag **Output**
In Aux output mode, this signal functions as AUX_ADP, which indicates if the output byte is part of an adaptation field.

Aux - Error Indicator **Input**
In Aux input mode, this signal functions as AUX_ERR, which indicates if the incoming byte is part of a packet that has an error.

GPIO28 **Bidirectional**
This signal can also serve as a general-purpose I/O signal (GPIO28) by setting bit 3 in the General-Purpose Mode register.

STROBEn/AUX_TX

1284 - Data Strobe **Input**

In 1284 mode, this signal functions as STROBEn. When set LOW, this signal indicates that valid data is present on PDATA[7:0]. L64118 latches the data on the rising edge of STROBEn.

Aux - Aux Port Direction **Input**

In Aux mode, this signal is used to specify the direction of the aux port if the PINACT bit (bit 4) is set in the Aux Control register. If AUX_TX is HIGH, then the Aux port is an output. If AUX_TX is LOW, then the Aux port is an input.

GPIO29 **Bidirectional**

This signal can also serve as a general-purpose I/O signal (GPIO29) by setting bit 3 in the General-Purpose Mode register.

I^2C-Compatible Port

These signals connect the L64118 to an external I^2C device. The L64118 uses them to initialize external devices in the system that have this interface.

SCL **Serial Clock** **Bidirectional**

SCL provides the clock signal for transmitting and receiving data through SDA.

SDA **Serial Data** **Bidirectional**

SDA provides the data connection to the I^2C-compatible port. Data is transmitted and received through this line according to the I^2C protocol. This signal should be pulled HIGH by an external pull-up resistor.

Teletext Port

These signals connect the L64118 to an external NTSC/PAL video encoder with a Teletext port.

TTXDATA **Teletext Data**
Master **Output**
This signal supplies the teletext data to the external video encoder. The L64118 outputs teletext data when TTXREQ is asserted and there are enough bits in the teletext output buffer to supply one complete teletext line. By default, this signal is not asserted after reset.

GPIO13 **Bidirectional**
TTXDATA can serve as a general-purpose I/O signal (GPIO13) by setting bit 2 in the General-Purpose Mode register.

TTXREQ **Teletext Data Request**
Master **Input**
When set HIGH, this signal indicates that the external video encoder device requests teletext data to be transferred through TTXDATA. The L64118 outputs teletext data on the TTXDATA pin as long as TTXREQ is asserted. You must program the Video Encoder device so the length of assertion of TTXREQ is compatible with the exact number of teletext bits per line. The L64118 Teletext port supports a direct connection to the Teletext port of NTSC/PAL video encoders. During normal operation, this is an input signal. By default, this signal is not asserted after reset.

GPIO12 **Bidirectional**
TTXREQ can serve as a general-purpose I/O signal (GPIO12) by setting bit 2 in the General-Purpose Mode register.

SmartCard Port

These signals provide the connection between the L64118 and external SmartCard devices. These signals are used by the L64118 to initialize external devices in a system with such a port. The L64118 supports two independent SmartCard devices.

SC0_C4 **SmartCard 0 Pin 4** **Bidirectional**

This signal is connected to the C4 pin on the SmartCard. This signal should be pulled up by an external pull-up resistor after reset.

SC0_C8 **SmartCard 0 Pin 8** **Bidirectional**

This signal is connected to the C8 pin on the SmartCard. This signal should be pulled up by an external pull-up resistor after reset.

SC0_CLK **SmartCard 0 Clock** **Output**

This signal is the output clock for SmartCard 0.

GPIO33 **Bidirectional**

SC0_CLK can serve as a general-purpose I/O signal (GPIO33) by setting bit 4 in the General-Purpose Mode register.

By default, this signal is not asserted after reset.

SC0_DETECT

SmartCard 0 Detect **Input**

When HIGH, this signal indicates that a card is inserted in slot 0.

GPIO31 **Bidirectional**

SC0_DETECT can serve as a general-purpose I/O signal (GPIO31) by setting bit 4 in the General-Purpose Mode register.

By default, this signal floats after reset.

SC0_I/O **SmartCard 0 I/O** **Bidirectional**

This signal transfers data (using the coupler) between SmartCard 0 and the SmartCard port of the L64118. It is open-drain. This signal must be pulled up by an external resistor after reset.

SC0_RSTn **SmartCard 0 Reset** **Output**

This signal resets SmartCard 0.

GPIO30 **Bidirectional**

SC0_RSTn can serve as a general-purpose I/O signal (GPIO30) by setting bit 4 in the General-Purpose Mode register.

By default, this signal is not asserted after reset.

SC0_VCC_ENn

SmartCard 0 VCC Enable **Output**

This signal turns the power supply of SmartCard 0 on or off. When LOW, it enables the VCC supply.

GPIO32 **Bidirectional**

SC0_VCC_ENn can serve as a general-purpose I/O signal (GPIO32) by setting bit 4 in the General-Purpose Mode register.

By default, this signal is not asserted after reset.

SC0_VPP_ENn

SmartCard 0 VPP Enable **Output**

This signal turns the power supply of SmartCard 0 on or off. When LOW, it enables the VCC supply.

GPIO34 **Bidirectional**

SC0_VPP_ENn can serve as a general-purpose I/O signal (GPIO34) by setting bit 4 in the General-Purpose Mode register.

By default, this signal is not asserted after reset.

SC1_CLK **SmartCard 1 Clock** **Output**

This signal clocks the output of SmartCard1.

GPIO38 **Bidirectional**

SC1_CLK can serve as a general-purpose I/O signal (GPIO38) by setting bit 5 in the General-Purpose Mode register.

By default, this signal is not asserted after reset.

SC1_DETECT

SmartCard 1 Detect **Input**

When HIGH, this signal indicates that a card is inserted in slot 1.

GPIO36 **Bidirectional**

SC1_CLK can serve as a general-purpose I/O signal (GPIO36) by setting bit 5 in the General-Purpose Mode register.

By default, this signal floats after reset.

SC1_I/O **SmartCard 1 I/O** **Bidirectional**

This signal transfers the data (using the coupler) between SmartCard1 and the SmartCard port of the L64118. It is open-drain. This signal must be pulled up by an external resistor after reset.

SC1_RSTn **SmartCard 1 Reset** **Output**

This signal resets SmartCard1.

GPIO35 **Bidirectional**

SC1_RSTn can serve as a general-purpose I/O signal (GPIO35) by setting bit 5 in the General-Purpose Mode register.

By default, this signal is not asserted after reset.

SC1_VCC_ENn

SmartCard 1 VCC Enable **Output**

This signal turns the power supply of SmartCard1 on or off. When LOW, it enables the VCC supply.

GPIO37 **Bidirectional**

SC1_VCC_ENn can serve as a general-purpose I/O signal (GPIO37) by setting bit 5 in the General-Purpose Mode register.

By default, this signal is not asserted after reset.

SC1_VPP_ENn

SmartCard 1 VPP Enable **Output**

This signal turns the power supply of SmartCard 0 on or off. When LOW, it enables the VPP pin.

GPIO39 **Bidirectional**

SC1_VPP_ENn can serve as a general-purpose I/O signal (GPIO39) by setting bit 4 in the General-Purpose Mode register.

By default, this signal is not asserted after reset.

Infrared Port

These signals provide the connection between the L64118 and an external infrared receiver and transmitter.

IRBL **Infrared Blaster** **Output**
This signal is the infrared blaster output. This signal can be configured to reflect the value of the infrared transmitter output.

GPIO47 **Bidirectional**
IRBL can serve as a general-purpose I/O signal (GPIO47) by setting bit 7 in the General-Purpose Mode register.

By default, this signal floats after reset.

IRRX0 **Infrared Receiver 0** **Input**
This signal serves as the receive port for the demodulated signal of one of the two infrared receivers ports.

GPIO40 **Bidirectional**
IRRX0 can serve as a general-purpose I/O signal (GPIO40) by setting bit 7 in the General-Purpose Mode register.

By default, this signal floats after reset.

IRRX1 **Infrared Receiver 1** **Input**
This signal serves as the receive port for the demodulated signal of one of the two infrared receivers ports.

GPIO41 **Bidirectional**
IRRX1 can serve as a general-purpose I/O signal (GPIO41) by setting bit 7 in the General-Purpose Mode register.

By default, this signal floats after reset.

IRTX **Infrared Transmitter** **Output**
This signal serves as the infrared transmitter output.

GPIO44 **Bidirectional**
IRRX1 can serve as a general-purpose I/O signal (GPIO44) by setting bit 7 in the General-Purpose Mode register.

By default, this signal floats after reset.

General-Purpose Pins

The general-purpose I/O signals for the L64118 let you control and monitor various external events. These signals consist of eight groups. Group 7 contains dedicated GPIO signals, whereas the other groups multiplex the GPIO signals with other functions. Note that all pins within a GPIO group must be enabled or disabled as a group; however, individual GPIO pins can be configured as inputs or outputs using the General-Purpose Control register. The GPIO groups and associated pins are listed in Table 5 through Table 12.

Table 5 Group 1: EBus Signals

Pin Name	GPIO Signal[1]
CSn[4]	GPIO1
BEn[2]	GPIO2
BEn[3]	GPIO4
SDQMH	GPIO6

1. The GPIO3 and GPIO5 signals are not available on the L64118.

Table 6 Group 2: SIO Signals

Pin Name	GPIO Signal
CTSn0	GPIO7
DTRn0	GPIO8
DSRn0	GPIO9
RTSn0	GPIO10
RXDn0	GPIO11

Table 7 Group 3: Teletext Signals

Pin Name	GPIO Signal
TTXREQ	GPIO12
TTXDATA	GPIO13

Table 8 Group 4: PIO (IEEE 1284) Signals

Pin Name	GPIO Signal
AUTOFDn	GPIO14
BUSY	GPIO15
PDATA[7:0]	GPIO[23:16]
FAULTn	GPIO24
INITn	GPIO25
PERROR	GPIO26
SELECT	GPIO27
SELECTINn	GPIO28
STROBEn	GPIO29

Table 9 Group 5: SmartCard 0 Signals

Pin Name	GPIO Signal
SC0_RSTn	GPIO30
SC0_DETECT	GPIO31
SC0_VCC_EN	GPIO32
SC0_CLK	GPIO33
SC0_VPP_ENn	GPIO34

Table 10 Group 6: SmartCard 1 Signals

Pin Name	GPIO Signal
SC1_RSTn	GPIO35
SC1_DETECT	GPIO36
SC1_VCC_ENn	GPIO37
SC1_CLK	GPIO38
SC1_VPP_ENn	GPIO39

Table 11 Group 8: Infrared Signals

Pin Name	GPIO Signal
IRRX0	GPIO[40]
IRRX1	GPIO[41]
IRTX	GPIO[44]
IRBL	GPIO[47]

Table 12 Group 7: Dedicated GPIO Signals

Pin Name	GPIO Signal
GPIO[43:42]	GPIO[43:42]
GPIO[46:45]	GPIO[46:45]
GPIO[49:48]	GPIO[49:48]

GPIO[49, 48, 46, 45, 43, 42]
Dedicated GPIO **Bidirectional**
These are the dedicated general-purpose I/O signals. By default, these signals float after reset. Note that for LSI Logic manufacturing test purposes, GPIO46 must be pulled HIGH during reset.

Programming the General-Purpose Pins

To use a general-purpose pin, enable the entire group by writing to the General-Purpose Mode register; then select the input/output for each pin within the group by writing to the specific General-Purpose Control register. (Note that no group has more than 16 general-purpose pins.)

After each pin is defined, the programmer can read the value of the GPIO signal using the General-Purpose Data registers, or write the value of a GPIO signal to the General-Purpose Data registers.

Latency of GPIO Updates

The use of the GPIO pins is intended for controlling/monitoring external logic by the software.

You should consider a delay between the time when the software writes a value to a general-purpose output pin and the time the value is valid on the output pin. This delay is caused by the transaction time between the on-chip processor to the on-chip peripheral component, and the delay time of the general-purpose module.

The delay that the general-purpose module inserts in writing to an output general-purpose pin is not more than 1 µs (for SCLK = 27 MHz).

When the processor reads a value from a general-purpose pin configured to be an input pin, there is no extra delay inserted; however, the register holding general-purpose input values is updated every 2 μs (for SCLK = 27 MHz).

Electrical Requirements

This section specifies the electrical requirements for the L64118. Five tables list electrical data in the following categories:

- Absolute Maximum Ratings (Table 13)
- Recommended Operating Conditions (Table 14)
- Capacitance (Table 15)
- DC Characteristics (Table 16)
- Pin Description Summary (Table 17)

The following tables provide the maximum ratings, operating conditions, and capacitances for the 3.3 V, G10-p implementation of the L64118.

Table 13 Absolute Maximum Ratings

Symbol	Parameter	Limits[1]	Unit
V_{DD}	DC Supply	– 0.3 to + 3.9	V
V_{IN}	5 V Compatible Input Voltage	– 1.0 to 6.0	V
V_{IN}	3.3 V Input Voltage	– 0.8 to 4.7	V
I_{IN}	DC Input Current	± 10	mA
T_{STGP}	Storage Temperature Range (Plastic)	– 40 to + 125	°C

1. Referenced to V_{SS}.

Table 14 Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply	+ 3.0 to + 3.6	V
T_A	Ambient Temperature	0 to + 70	°C

Table 15 Capacitance

Symbol	Parameter[1]	Min	Typ	Max	Units
C_{IN}	Input Capacitance	5.0	–	–	pF
C_{OUT}	Output Capacitance	5.0	–	–	pF
C_{IO}	I/O Bus Capacitance	5.0	–	–	pF

1. Measurement conditions are V_{IN} = TBD V, T_A = 25 °C, and clock frequency = 1 MHz.

Table 16 DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{IL}	Voltage Input Low TTL CMOS		 – –	 – –	 0.8 0.2 V_{DD}	 V V
V_{IH}	Voltage Input High TTL CMOS 5 V Compatible		 2.0 0.7 V_{DD} 2.0	 – – –	 – – 5.5	 V V V
V_{OL}	Voltage Output Low 2-mA Output Buffers 4-mA Output Buffers 6-mA Output Buffers	 I_{OL} = 2.0 mA I_{OL} = 4.0 mA I_{OL} = 6.0 mA	 – – –	 0.2 0.2 0.2	 0.4 0.4 0.4	 V V V
V_{OH}	Voltage Output High 2-mA Output Buffers 4-mA Output Buffers 6-mA Output Buffers	 I_{OH} = – 2.0 mA I_{OH} = – 4.0 mA I_{OH} = – 6.0 mA	 2.4 2.4 2.4	 – – –	 – – –	 V V V
I_{IL}	Current Input Leakage[2] with Pulldown with Pullup	V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS}	– 10 35 – 214	± 10 115 – 115	+ 10 222 – 35	µA µA µA
I_{OZ}	Current 3-State Output Leakage	V_{DD} = Max, V_{OUT} = V_{SS} or V_{DD}	– 10	± 1	+ 10	µA
I_{OSP4}	Current P-Channel Output Short Circuit (4-mA Output Buffers)[3, 4]	V_{DD} = Max, V_{OUT} = V_{SS}	– 117	– 75	– 40	mA
I_{OSN4}	Current N-Channel Output Short Circuit (4-mA Output Buffers)[3, 4]	V_{DD} = Max, V_{OUT} = V_{DD}	37	90	140	mA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS} = 0 mA	10	10	10	mA
I_{DD}	Dynamic Supply Current	V_{IN} = V_{IH} or V_{IL} = 27 MHz	215	215	215	mA

1. Specified at V_{DD} equals 3.3 V ± 5% at ambient temperature over the specified range.
2. For CMOS and TLL inputs.
3. Not more than one output may be shorted at a time for a maximum duration of one second.
4. These values scale proportionally for output buffers with different drive strengths.

Table 17 Pin Description Summary

Mnemonic	Description	Type[1]	Drive (mA)	Active[2]	Pull-Up/ Down
ACKn/ AUXNM	1284 Acknowledge Aux No Match	Output Output	6 6	LOW HIGH	–
ACLK	Audio Clock	Output	4	–	–
AD[31:0]	EBus Address/Data	Bidirectional	8	–	–
ADDR[7:0]	EBus Address/Data	Bidirectional	8	–	–
AD[15:0]	EBus Address/Data	Bidirectional	8	–	–
AREQn	Audio Data Request	Input	–	LOW	U [3]
ALE	EBus Address Latch Enable	Output	8	LOW	–
AUTOFDn/ AUXV GPIO14	1284 Auto Feed Aux Data Valid General-Purpose IO 14	Input Bidirectional Bidirectional	– 6 6	LOW	–
AVALID	Audio Data Valid	Output	6	HIGH	–
AVD[7:0]	Audio/Video Data	Bidirectional	6	–	–
AVDD	Analog Power	Input	–	–	–
AVERRn	Audio/Video Error	Output	2	LOW	–
AVSS	Analog Ground	Input	–	–	–
BEn[1:0]	EBus Byte Enable	Bidirectional	8	LOW	–
BEn[3:2] GPIO[3:2]	EBus Byte Enable	Output Bidirectional	6 6	LOW	–
BUSY/ AUXSB GPIO15	1284 Busy Aux Sync Byte General-Purpose IO 15	Bidirectional	6	LOW	–
CCLK	Channel Data Clock	Input	–	–	–
CDATA[7:0]	Channel Data	Input	–	–	–
CERRn	Channel Data Error	Input	–	LOW	U
CPU_CLK	EBus Clock Output	Output	6	LOW	–
CSn[3:0]	EBus Chip Select	Output	8	LOW	–

Table 17 Pin Description Summary (Cont.)

Mnemonic	Description	Type[1]	Drive (mA)	Active[2]	Pull-Up/ Down
CSn[4] GPIO1	EBus Chip Select General-Purpose IO 1	Output Bidirectional	6 6	LOW	–
CSn[5] / MEMSTBn	EBus Chip Select Memory Strobe	Output	6	LOW	–
CTSn0 GPIO7	Clear To Send (SIO 0) General-Purpose I/O 7	Input Bidirectional	– 6	LOW	U
CTSn1 ICECLK	Clear To Send (SIO 1) Serial ICE Clock	Input	–	LOW	U
CVALID	Channel Data Enable	Input	–	HIGH	D [4]
DSRn0 GPIO9	Data Send Ready (SIO 0) General-Purpose I/O 9	Input Bidirectional	– 6	LOW	U
DTRn0 GPIO8	Data Terminal Ready (SIO 0) General-Purpose I/O 8	Output Bidirectional	6 6	LOW	–
EACKn	EBus Data Acknowledge	Input	–	LOW	U
ECLK	PLL Test Clock	Input	–	–	–
FAULTn/ AUXCLK GPIO24	1284 Fault Aux Port Clock General-Purpose I/O 24	Bidirectional	6	LOW	–
GPIO[42:43]	General-Purpose I/O	Bidirectional	4	–	–
GPIO[46:45]	General-Purpose I/O	Bidirectional	4	–	U
GPIO[48:49]	General-Purpose I/O	Bidirectional	4	–	–
IDDTN	Test Pin	Input	–	HIGH	–
INITn/ AUXPID[2] GPIO25	1284 Initialization Aux Packet ID 2 General-Purpose I/O 25	Input Output Bidirectional	– 6 6	LOW	–
INTn[3:0]	Interrupt	Input	–	LOW	U
INTn4	Interrupt	Bidirectional (open drain)	6	LOW	–
IRBL GPIO47	IR Blaster General-Purpose I/O 47	Output Bidirectional	4 4	HIGH	–

Table 17 Pin Description Summary (Cont.)

Mnemonic	Description	Type[1]	Drive (mA)	Active[2]	Pull-Up/ Down
IREF	Current Reference	–	–	–	–
IRRX0 GPIO40	IR Receiver Port 0 General-Purpose I/O 40	Input Bidirectional	– 4	–	–
IRRX1 GPIO41	IR Receiver Port 1 General-Purpose I/O 41	Input Bidirectional	– 4	–	–
IRTX GPIO44	IR Transmitter Port General-Purpose I/O 44	Output Bidirectional	4 4	–	–
OP_MODE[1:0]	Operational Mode	Input	–	–	–
PDATA[7:0]	1284 Data	Bidirectional	4	–	–
PDATA_DIR / OP_MODE[2]	1284 Data Direction or Operational Mode[2]	Output Input	6 –	–	–
PERROR/ AUXPID[0] GPIO26	1284 Peripheral Error Aux Packet ID [0] General-Purpose I/O 26	Output Output Bidirectional	6 6 6	HIGH	–
PLLVDD	PLL Analog VDD	Input	–	–	–
PLLVSS	PLL Analog VSS	Input	–	–	–
RCLK	UART Receive Clock (SIO 0)	Input	4	–	–
RDn	EBus Read Strobe	Output	8	LOW	U
RESETn	Reset	Input (Schmitt trigger)	–	LOW	U
RTSn0 GPIO10	Request To Send (SIO 0) General-Purpose I/O 10	Output Bidirectional	6 6	LOW	–
RTSn1	Request To Send (SIO 1)	Output	6	LOW	–
RXD0 GPIO11	Receive Data (SIO 0) General-Purpose I/O 11	Input Bidirectional	– 6	–	U
RXD1/ ICE_RX	Receive Data (SIO 1) Receive Data Serial ICE Port	Input	4	–	U
RXD2	Receive Data (SIO 2)	Input	–	–	U
SA[11:0]	SDRAM Address Bus	Output	6	–	–

Table 17 Pin Description Summary (Cont.)

Mnemonic	Description	Type[1]	Drive (mA)	Active[2]	Pull-Up/ Down
SBA[0]	SDRAM Bank Select 0	Output	6	–	–
SBA[1]	SDRAM Bank Select 1	Output	6	–	–
SBD[15:0]	SDRAM Data Bus	Bidirectional	6	–	–
SC0_C4	SmartCard 0 C4	Bidirectional (open drain)	6	–	–
SC0_C8	SmartCard 0 C8	Bidirectional (open drain)	6	–	–
SC0_CLK GPIO33	SmartCard 0 Clock General-Purpose I/O 33	Output Bidirectional	6 6	–	–
SC0_DETECT GPIO31	SmartCard 0 Detect General-Purpose I/O 31	Input Bidirectional	4	HIGH	–
SC0_I/O	SmartCard 0 Data	Bidirectional (open drain)	6	–	–
SC0_RSTn GPIO30	SmartCard 0 Reset General-Purpose I/O 30	Output Bidirectional	4 4	LOW	–
SC0_VCC_ENn GPIO32	SmartCard 0 VCC Enable General-Purpose I/O 32	Output Bidirectional	4 4	LOW	–
SC0_VPP_ENn GPIO34	SmartCard 0 VPP Enable General-Purpose I/O 34	Output Bidirectional	4 4	LOW	–
SC1_CLK GPIO38	SmartCard 1 Clock General-Purpose I/O 38	Output Bidirectional	6 6	–	–
SC1_DETECT GPIO36	SmartCard 1 Detect General-Purpose I/O 36	Input Bidirectional	– 4	HIGH	–
SC1_I/O	SmartCard 1 Data	Bidirectional (open drain)	6	–	–
SC1_RSTn GPIO35	SmartCard 1 Reset General-Purpose I/O 35	Output Bidirectional	4 4	LOW	–
SC1_VCC_ENn GPIO37	SmartCard 1 VCC Enable General-Purpose I/O 37	Output Bidirectional	4 4	LOW	–
SC1_VPP_ENn GPIO39	SmartCard 1 VPP Enable General-Purpose I/O 39	Output Bidirectional	4 4	LOW	–

Table 17 Pin Description Summary (Cont.)

Mnemonic	Description	Type[1]	Drive (mA)	Active[2]	Pull-Up/ Down
SCASn	SDRAM Column Address Strobe	Output	8	LOW	–
SCL	I^2C Clock	Bidirectional (open drain)	8	–	–
SCLK	System Clock (27 MHz)	Input	–	–	–
SDA	I^2C Data	Bidirectional (open drain)	8	–	–
SDCLK	SDRAM Master Clock	Output	6	–	–
SDET	Sigma-Delta Control Voltage Output	Output (open drain)	6	–	D
SDQMH GPIO6	SDRAM Data Mask High Byte General-Purpose I/O 6	Output Bidirectional	8 8	HIGH	–
SDQML	SDRAM Data Mask Low Byte	Output	4	–	–
SELECT/ AUXPID[1] GPIO27	1284 Selection Aux Packet ID [1]	Output Output Bidirectional	6 6 6	LOW	–
SELECTINn/ AUX_ADP/ AUX_ERR GPIO28	1284 Selection Indicator Aux Adaptation Field Flag Aux Error Indicator General-Purpose I/O 28	Input Output Input Bidirectional	– 6 – 6	LOW	–
SRASn	SDRAM Row Address Strobe	Output	4	LOW	–
STROBEn/ AUX_TX GPIO29	1284 Data Strobe Aux Port Direction General-Purpose I/O 29	Input Input Bidirectional	– – 4	LOW	–
SWEn	SDRAM Write Enable	Output	6	LOW	–
TCLK	UART Transmit Clock (SIO 0)	Input	8	LOW	U
TCK	JTAG Scan Clock	Input	–	–	–
TDI	JTAG Scan In	Input	–	–	–
TDO	JTAG Scan Out	Output (3-State)	4	–	–
TMS	JTAG Mode	Input	–	–	–

Table 17 Pin Description Summary (Cont.)

Mnemonic	Description	Type[1]	Drive (mA)	Active[2]	Pull-Up/ Down
TRST	JTAG Reset	Input	–	HIGH	D
TTXDATA GPIO13	Teletext Data General-Purpose I/O 13	Output Bidirectional	6 6	–	U
TTXREQ GPIO12	Teletext Request General-Purpose I/O 12	Input Bidirectional	– 6	HIGH	D
TXD0	Transmit Data (SIO 0)	Output	6	–	–
TXD1 ICE_TX	Transmit Data (SIO 1) Transmit Data Serial ICEPort	Output	6	–	–
TXD2	Transmit Data (SIO 2)	Output	6	–	–
VDD	Power	–	–	–	–
VREQn	Video Data Request	Input	–	LOW	U
VSS	Ground	–	–	–	–
VVALID	Video Data Valid	Output	6	HIGH	–
WRn	EBus Write Strobe	Output	8	LOW	U
ZTESTn	Test Pin	Input	–	LOW	U

1. If only one pin type is listed, it applies to all possible pin configurations.
2. If only active state (LOW or HIGH) is listed, it applies to all possible pin configurations.
3. The internal pull-up resistor value is from 50–100 kΩ
4. The internal pull-down resistor value is from 50–100 kΩ

Packaging and Pinouts

Figure 6 shows the signal solder balls of the L64118. This diagram shows the location, ball number, and signal for each solder ball on the 256-pin Plastic Ball Grid Array (PBGA) package (package code IF).

This pinout drawing is followed by:

- a listing of the solder balls in numerical order for the L64118 (Table 18)
- a listing of the solder balls in alphabetic order for the L64118 (Table 19)
- mechanical drawings that provide the dimensions of the L64118 (Figure 7)

Note: All drawings in this section use the same origin. In other words, solder ball A1 in Figure 6 and Figure 7 are the same.

Figure 6 L64118 256-Pin PBGA Pinout

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
1	VSS	ACLK	GPIO43	IRTX	IRBL	GPIO48	GPIO45/ RCLK	CDATA[0]	CDATA[4]	TRST	SDET	AVD[6]	AVD[5]	AVD[3]	TDI	RXD2	NC	NC	AVERRn	SC0_VPP_ ENn
2	NC	NC	IRRX0	GPIO42	CERRn	CDATA[6]	CDATA[7]	CDATA[1]	CDATA[5]	NC	TXD2	AVD[7]	TDO	OP_ MODE[1]	AVD[1]	IRRX1	NC	NC	NC	SC0_ DETECT
3	PLLVDD	NC	NC	NC	ECLK	CDATA[3]	CDATA[2]	GPIO46	GPIO49	SCLK	TCK	TMS	AVD[2]	AVD[0]	AVALID	VREQn	NC	NC	SC0_ RSTn	SC0_C4
4	IREF	AVDD	NC	VSS	CVALID	VDD	CCLK	VSS	IDDTN	VDD	OP_ MODE[0]	AVD[4]	VSS	VVALID	VDD	AREQn	VSS	SC0_IO	SC0_ CLK	SC0_C8
5	SA[1]	ZTESTn	AVSS	PLLVSS													SC0_ VCC_ ENn	SC1_ VPP_ ENn	SC1_ RSTn	SC1_ DETECT
6	SA[4]	SA[2]	SDCLK	VDD													VDD	SC1_CLK	SC1_ VCC_ ENn	AD[15]
7	SA[6]	SA[5]	SA[3]	SA[0]													SC1_IO	AD[14]	AD[13]	AD[12]
8	SA[9]	SA[8]	SA[7]	VSS													VSS	AD[11]	AD[10]	AD[9]
9	SBA[1]	SBA[0]	SA[11]	SA[10]													AD[8]	AD[7]	AD[6]	AD[5]
10	SDQMH	SWEn	SCASn	SRASn													VDD	AD[3]	AD[4]	AD[2]
11	SDQML	SBD[14]	SBD[15]	VDD													ADDR[1]	ADDR[0]	AD[0]	AD[1]
12	SBD[13]	SBD[12]	SBD[11]	SBD[10]													ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]
13	SBD[9]	SBD[8]	SBD[7]	VSS													VSS	AD[16]	ADDR[7]	ADDR[6]
14	SBD[6]	SBD[5]	SBD[4]	SBD[1]													AD[23]	AD[20]	AD[18]	AD[17]
15	SBD[3]	SBD[2]	SBD[0]	VDD													VDD	AD[24]	AD[21]	AD[19]
16	TTXREQ	TTXDATA	DSRn0	TXD0													AD[29]	AD[27]	AD[25]	AD[22]
17	CTSn0	DTRn0	NC	VSS	RXD1	VDD	PERROR	VSS	PDATA[7]	STROBEn	VDD	CSn2	VSS	CPU_CLK	VDD	AD[30]	VSS	NC	NC	AD[26]
18	NC	TCLK	NC	NC	NC	SELECT	PDATA[0]	PDATA[4]	SELECT-INn	SDA	INTn2	CSn1	CSn5/ MEM-STBn	BEn2	WRn	EACKn	NC	NC	NC	AD[28]
19	RTSn0	CTSn1	NC	NC	FAULTn	ACKn	PDATA[2]	PDATA[5]	INTn	SCL	INTn1	CSn0	CSn4	BEn3	BEn0	ALE	NC	NC	NC	NC
20	RXD0	PDATA_ DIR/OP_ MODE[2]	RTSn1	TXD1	BUSY	PDATA[1]	PDATA[3]	PDATA[6]	AUTOFDn	INTn4	INTn3	INTn0	CSn3	RESETn	BEn1	RDn	AD[31]	NC	NC	NC

Table 18 L64118 Solder Ball Matrix List

Solder Ball	Signal	Solder Ball	Signal	Solder Ball	Signal	Solder Ball	Signal	Solder Ball	Signal
A1	VSS	P3	AVD[0]	C8	SA[7]	Y14	AD[17]	U18	NC
B1	ACLK	R3	AVALID	D8	VSS	A15	SBD[3]	V18	NC
C1	GPIO43	T3	VREQn	U8	VSS	B15	SBD[2]	W18	NC
D1	IRTX	U3	NC	V8	AD[11]	C15	SBD[0]	Y18	AD[28]
E1	IRBL	V3	NC	W8	AD[10]	D15	VDD	A19	RTSn0
F1	GPIO48	W3	SC0_RSTn	Y8	AD[9]	U15	VDD	B19	CTSn1
G1	GPIO45/RCLK	Y3	SC0_C4	A9	SBA[1]	V15	AD[24]	C19	NC
H1	CDATA[0]	A4	IREF	B9	SBA[0]	W15	AD[21]	D19	NC
J1	CDATA[4]	B4	AVDD	C9	SA[11]	Y15	AD[19]	E19	FAULTn
K1	TRST	C4	NC	D9	SA[10]	A16	TTXREQ	F19	ACKn
L1	SDET	D4	VSS	U9	AD[8]	B16	TTXDATA	G19	PDATA[2]
M1	AVD[6]	E4	CVALID	V9	AD[7]	C16	DSRn0	H19	PDATA[5]
N1	AVD[5]	F4	VDD	W9	AD[6]	D16	TXD0	J19	INITn
P1	AVD[3]	G4	CCLK	Y9	AD[5]	U16	AD[29]	K19	SCL
R1	TDI	H4	VSS	A10	SDQMH	V16	AD[27]	L19	INTn1
T1	RXD2	J4	IDDTN	B10	SWEn	W16	AD[25]	M19	CSn0
U1	NC	K4	VDD	C10	SCASn	Y16	AD[22]	N19	CSn4
V1	NC	L4	OP_MODE[0]	D10	SRASn	A17	CTSn0	P19	BEn3
W1	AVERRn	M4	AVD[4]	U10	VDD	B17	DTRn0	R19	BEn0
Y1	SC0_VPP_ENn	N4	VSS	V10	AD[3]	C17	NC	T19	ALE
A2	NC	P4	VVALID	W10	AD[4]	D17	VSS	U19	NC
B2	NC	R4	VDD	Y10	AD[2]	E17	RXD1	V19	NC
C2	IRRX0	T4	AREQn	A11	SDQML	F17	VDD	W19	NC
D2	GPIO42	U4	VSS	B11	SBD[14]	G17	PERROR	Y19	NC
E2	CERRn	V4	SC0_IO	C11	SBD[15]	H17	VSS	A20	RXD0
F2	CDATA[6]	W4	SC0_CLK	D11	VDD	J17	PDATA[7]	B20	PDATA_DIR/ OP_MODE[2]
G2	CDATA[7]	Y4	SC0_C8	U11	ADDR[1]	K17	STROBEn	C20	RTSn1
H2	CDATA[1]	A5	SA[1]	V11	ADDR[0]	L17	VDD	D20	TXD1
J2	CDATA[5]	B5	ZTESTn	W11	AD[0]	M17	CSn2	E20	BUSY
K2	NC	C5	AVSS	Y11	AD[1]	N17	VSS	F20	PDATA[1]
L2	TXD2	D5	PLLVSS	A12	SBD[13]	P17	CPU_CLK	G20	PDATA[3]
M2	AVD[7]	U5	SC0_VCC_ENn	B12	SBD[12]	R17	VDD	H20	PDATA[6]
N2	TDO	V5	SC1_VPP_ENn	C12	SBD[11]	T17	AD[30]	J20	AUTOFDn
P2	OP_MODE[1]	W5	SC1_RSTn	C12	SBD[10]	U17	VSS	K20	INTn4
R2	AVD[1]	Y5	SC1_DETECT	U12	ADDR[5]	V17	NC	L20	INTn3
T2	IRRX1	A6	SA[4]	V12	ADDR[4]	W17	NC	M20	INTn0
U2	NC	B6	SA[2]	W12	ADDR[3]	Y17	AD[26]	N20	CSn3
V2	NC	C6	SDCLK	Y12	ADDR[2]	A18	NC	P20	RESETn
W2	NC	D6	VDD	A13	SBD[9]	B18	TCLK	R20	BEn1
Y2	SC0_DETECT	U6	VDD	B13	SBD[8]	C18	NC	T20	RDn
A3	PLLVDD	V6	SC1_CLK	C13	SBD[7]	D18	NC	U20	AD[31]
B3	NC	W6	SC1_VCC_ENn	D13	VSS	E18	NC	V20	NC
C3	NC	Y6	AD[15]	U13	VSS	F18	SELECT	W20	NC
D3	NC	A7	SA[6]	V13	AD[16]	G18	PDATA[0]	Y20	NC
E3	ECLK	B7	SA[5]	W13	ADDR[7]	H18	PDATA[4]		
F3	CDATA[3]	C7	SA[3]	Y13	ADDR[6]	J18	SELECTINn		
G3	CDATA[2]	D7	SA[0]	A14	SBD[6]	K18	SDA		
H3	GPIO46	U7	SC1_IO	B14	SBD[5]	L18	INTn2		
J3	GPIO49	V7	AD[14]	C14	SBD[4]	M18	CSn1		
K3	SCLK	W7	AD[13]	D14	SBD[1]	N18	CSn5/MEMSTBn		
L3	TCK	Y7	AD[12]	U14	AD[23]	P18	BEn2		
M3	TMS	A8	SA[9]	V14	AD[20]	R18	WRn		
N3	AVD[2]	B8	SA[8]	W14	AD[18]	T18	EACKn		

Table 19 L64118 Alphabetical Signal List

Signal	Solder Ball	Signal	Solder Ball	Signal	Solder Ball	Signal	Solder Ball	Signal	Solder Ball
ACKn	F19	AVD[7]	M2	NC	V1	RXD2	T1	SELECT	F18
ACLK	B1	AVDD	B4	NC	A2	SA[0]	D7	SELECTINn	J18
AD[0]	W11	AVERRn	W1	NC	B2	SA[10]	D9	SRASn	D10
AD[10]	W8	AVSS	C5	NC	K2	SA[11]	C9	STROBEn	K17
AD[11]	V8	BEn0	R19	NC	U2	SA[1]	A5	SWEn	B10
AD[12]	Y7	BEn1	R20	NC	V2	SA[2]	B6	TCK	L3
AD[13]	W7	BEn2	P18	NC	W2	SA[3]	C7	TCLK	B18
AD[14]	V7	BEn3	P19	NC	B3	SA[4]	A6	TDI	R1
AD[15]	Y6	BUSY	E20	NC	C3	SA[5]	B7	TDO	N2
AD[16]	V13	CCLK	G4	NC	D3	SA[6]	A7	TMS	M3
AD[17]	Y14	CDATA[0]	H1	NC	U3	SA[7]	C8	TRST	K1
AD[18]	W14	CDATA[1]	H2	NC	V3	SA[8]	B8	TTXDATA	B16
AD[19]	Y15	CDATA[2]	G3	NC	C4	SA[9]	A8	TTXREQ	A16
AD[1]	Y11	CDATA[3]	F3	NC	C17	SBA[0]	B9	TXD0	D16
AD[20]	V14	CDATA[4]	J1	NC	V17	SBA[1]	A9	TXD1	D20
AD[21]	W15	CDATA[5]	J2	NC	W17	SBD[0]	C15	TXD2	L2
AD[22]	Y16	CDATA[6]	F2	NC	A18	SBD[10]	C12	VDD	F4
AD[23]	U14	CDATA[7]	G2	NC	C18	SBD[11]	C12	VDD	K4
AD[24]	V15	CERRn	E2	NC	D18	SBD[12]	B12	VDD	R4
AD[25]	W16	CPU_CLK	P17	NC	E18	SBD[13]	A12	VDD	D6
AD[26]	Y17	CSn0	M19	NC	U18	SBD[14]	B11	VDD	U6
AD[27]	V16	CSn1	M18	NC	V18	SBD[15]	C11	VDD	U10
AD[28]	Y18	CSn2	M17	NC	W18	SBD[1]	D14	VDD	D11
AD[29]	U16	CSn3	N20	NC	C19	SBD[2]	B15	VDD	D15
AD[2]	Y10	CSn4	N19	NC	D19	SBD[3]	A15	VDD	U15
AD[30]	T17	CSn5/MEMSTBn	N18	NC	U19	SBD[4]	C14	VDD	F17
AD[31]	U20	CTSn0	A17	NC	V19	SBD[5]	B14	VDD	L17
AD[3]	V10	CTSn1	B19	NC	W19	SBD[6]	A14	VDD	R17
AD[4]	W10	CVALID	E4	NC	Y19	SBD[7]	C13	VREQn	T3
AD[5]	Y9	DSRn0	C16	NC	V20	SBD[8]	B13	VSS	A1
AD[6]	W9	DTRn0	B17	NC	W20	SBD[9]	A13	VSS	D4
AD[7]	V9	EACKn	T18	NC	Y20	SC0_C4	Y3	VSS	H4
AD[8]	U9	ECLK	E3	OP_MODE[0]	L4	SC0_C8	Y4	VSS	N4
AD[9]	Y8	FAULTn	E19	OP_MODE[1]	P2	SC0_CLK	W4	VSS	U4
ADDR[0]	V11	GPIO42	D2	PDATA[0]	G18	SC0_DETECT	Y2	VSS	D8
ADDR[1]	U11	GPIO43	C1	PDATA[1]	F20	SC0_IO	V4	VSS	U8
ADDR[2]	Y12	GPIO45/RCLK	G1	PDATA[2]	G19	SC0_RSTn	W3	VSS	D13
ADDR[3]	W12	GPIO46	H3	PDATA[3]	G20	SC0_VCC_ENn	U5	VSS	U13
ADDR[4]	V12	GPIO48	F1	PDATA[4]	H18	SC0_VPP_ENn	Y1	VSS	D17
ADDR[5]	U12	GPIO49	J3	PDATA[5]	H19	SC1_CLK	V6	VSS	H17
ADDR[6]	Y13	IDDTN	J4	PDATA[6]	H20	SC1_DETECT	Y5	VSS	N17
ADDR[7]	W13	INITn	J19	PDATA[7]	J17	SC1_IO	U7	VSS	U17
ALE	T19	INTn0	M20	PDATA_DIR/		SC1_RSTn	W5	VVALID	P4
AREQn	T4	INTn1	L19	OP_MODE[2]	B20	SC1_VCC_ENn	W6	WRn	R18
AUTOFDn	J20	INTn2	L18	PERROR	G17	SC1_VPP_ENn	V5	ZTESTn	B5
AVALID	R3	INTn3	L20	PLLVDD	A3	SCASn	C10		
AVD[0]	P3	INTn4	K20	PLLVSS	D5	SCL	K19		
AVD[1]	R2	IRBL	E1	RDn	T20	SCLK	K3		
AVD[2]	N3	IREF	A4	RESETn	P20	SDA	K18		
AVD[3]	P1	IRRX0	C2	RTSn0	A19	SDCLK	C6		
AVD[4]	M4	IRRX1	T2	RTSn1	C20	SDET	L1		
AVD[5]	N1	IRTX	D1	RXD0	A20	SDQMH	A10		
AVD[6]	M1	NC	U1	RXD1	E17	SDQML	A11		

Figure 7. 256-Pin PBGA Package (IF) Mechanical Drawing

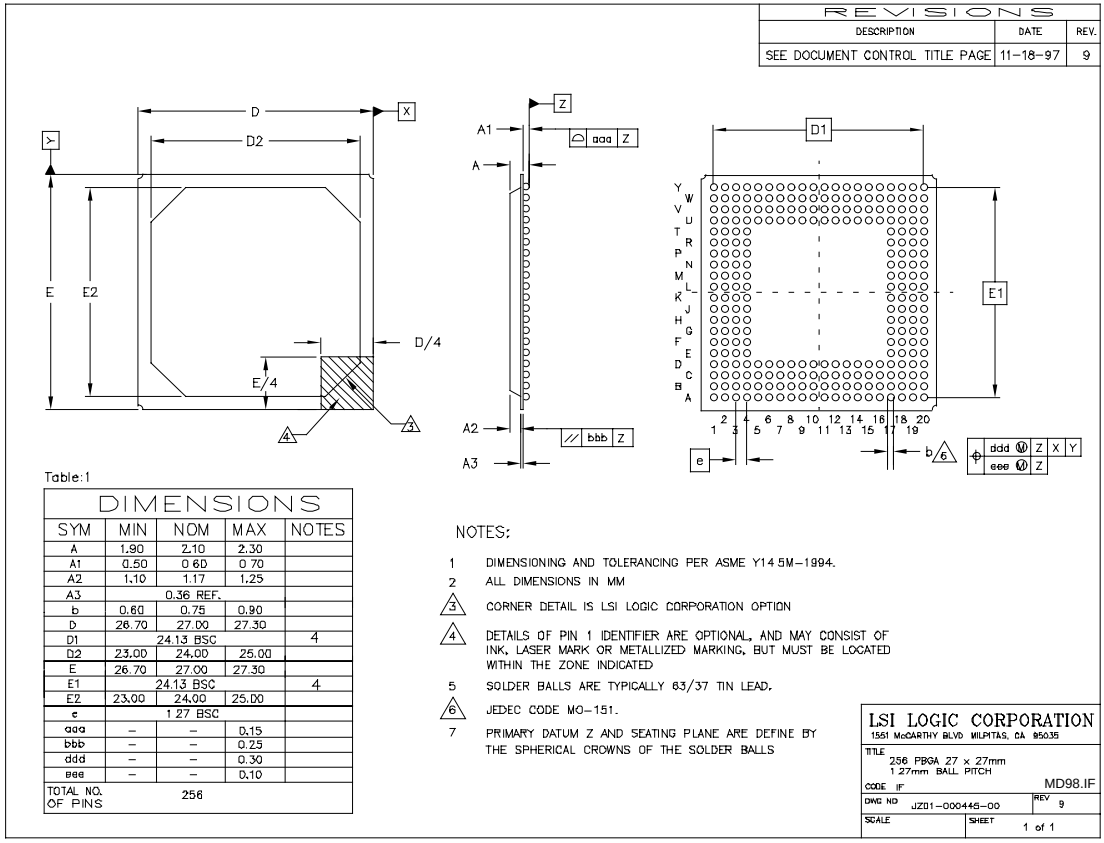


Table:1

DIMENSIONS				
SYM	MIN	NOM	MAX	NOTES
A	1.90	2.10	2.30	
A1	0.50	0.60	0.70	
A2	1.10	1.17	1.25	
A3		0.36 REF.		
b	0.60	0.75	0.90	
D	26.70	27.00	27.30	
D1		24.13 BSC		4
D2	23.00	24.00	25.00	
E	26.70	27.00	27.30	
E1		24.13 BSC		4
E2	23.00	24.00	25.00	
e		1.27 BSC		
aaa	–	–	0.15	
bbb	–	–	0.25	
ddd	–	–	0.30	
eee	–	–	0.10	
TOTAL NO. OF PINS		256		

Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code IF.**

Notes

Notes

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