



4 M × 4 BANKS × 16 BITS DDR SDRAM

Table of Contents-

1.	GENERAL DESCRIPTION.....	4
2.	FEATURES	4
3.	KEY PARAMETERS	5
4.	PIN CONFIGURATION	6
5.	PIN DESCRIPTION	7
6.	BLOCK DIAGRAM	8
7.	FUNCTIONAL DESCRIPTION.....	9
7.1	Power Up Sequence.....	9
7.2	Command Function	10
7.2.1	Bank Activate Command	10
7.2.2	Bank Precharge Command	10
7.2.3	Precharge All Command	10
7.2.4	Write Command	10
7.2.5	Write with Auto-precharge Command.....	10
7.2.6	Read Command	10
7.2.7	Read with Auto-precharge Command	10
7.2.8	Mode Register Set Command	11
7.2.9	Extended Mode Register Set Command	11
7.2.10	No-Operation Command	11
7.2.11	Burst Read Stop Command.....	11
7.2.12	Device Deselect Command	11
7.2.13	Auto Refresh Command	11
7.2.14	Self Refresh Entry Command.....	12
7.2.15	Self Refresh Exit Command	12
7.2.16	Data Write Enable /Disable Command	12
7.3	Read Operation	12
7.4	Write Operation	13
7.5	Precharge	13
7.6	Burst Termination	13
7.7	Refresh Operation	13
7.8	Power Down Mode	14
7.9	Input Clock Frequency Change during Precharge Power Down Mode	14
7.10	Mode Register Operation	14
7.10.1	Burst Length field (A2 to A0)	14



- 7.10.2 Addressing Mode Select (A3)..... 15
- 7.10.3 CAS Latency field (A6 to A4)..... 16
- 7.10.4 DLL Reset bit (A8)..... 16
- 7.10.5 Mode Register /Extended Mode register change bits (BA0, BA1)..... 16
- 7.10.6 Extended Mode Register field 16
- 7.10.7 Reserved field 16
- 8. OPERATION MODE 17
 - 8.1 Simplified Truth Table..... 17
 - 8.2 Function Truth Table 18
 - 8.3 Function Truth Table for CKE..... 21
 - 8.4 Simplified Stated Diagram 22
- 9. ELECTRICAL CHARACTERISTICS 23
 - 9.1 Absolute Maximum Ratings..... 23
 - 9.2 Recommended DC Operating Conditions 23
 - 9.3 Capacitance..... 24
 - 9.4 Leakage and Output Buffer Characteristics 24
 - 9.5 DC Characteristics..... 25
 - 9.6 AC Characteristics and Operating Condition..... 26
 - 9.7 AC Test Conditions..... 28
 - 9.8 AC Overshoot/Undershoot Specification for Address and Control Pins 30
 - 9.9 Overshoot/Undershoot Specification for Data, Strobe, and Mask Pins 31
- 10. TIMING WAVEFORMS 32
 - 10.1 Command Input Timing 32
 - 10.2 Timing of the CLK Signals 32
 - 10.3 Read Timing (Burst Length = 4) 33
 - 10.4 Write Timing (Burst Length = 4) 34
 - 10.5 DM, DATA MASK (W9425G6EH) 35
 - 10.6 Mode Register Set (MRS) Timing 36
 - 10.7 Extend Mode Register Set (EMRS) Timing 37
 - 10.8 Auto-precharge Timing (Read Cycle, CL = 2) 38
 - 10.9 Auto-precharge Timing (Read cycle, CL = 2), continued 39
 - 10.10 Auto-precharge Timing (Write Cycle)..... 40
 - 10.11 Read Interrupted by Read (CL = 2, BL = 2, 4, 8) 41
 - 10.12 Burst Read Stop (BL = 8) 41
 - 10.13 Read Interrupted by Write & BST (BL = 8) 42
 - 10.14 Read Interrupted by Precharge (BL = 8) 42
 - 10.15 Write Interrupted by Write (BL = 2, 4, 8) 43



10.16 Write Interrupted by Read (CL = 2, BL = 8)..... 43

10.17 Write Interrupted by Read (CL = 3, BL = 4)..... 44

10.18 Write Interrupted by Precharge (BL = 8) 44

10.19 2 Bank Interleave Read Operation (CL = 2, BL = 2) 45

10.20 2 Bank Interleave Read Operation (CL = 2, BL = 4) 45

10.21 4 Bank Interleave Read Operation (CL = 2, BL = 2) 46

10.22 4 Bank Interleave Read Operation (CL = 2, BL = 4) 46

10.23 Auto Refresh Cycle..... 47

10.24 Precharged/Active Power Down Mode Entry and Exit Timing 47

10.25 Input Clock Frequency Change during Precharge Power Down Mode Timing..... 47

10.26 Self Refresh Entry and Exit Timing 48

11. PACKAGE SPECIFICATION 49

 11.1 TSOP 66 II – 400 mil 49

12. REVISION HISTORY 50



1. GENERAL DESCRIPTION

W9425G6EH is a CMOS Double Data Rate synchronous dynamic random access memory (DDR SDRAM), organized as 4,194,304 words \times 4 banks \times 16 bits. W9425G6EH delivers a data bandwidth of up to 500M words per second (-4). To fully comply with the personal computer industrial standard, W9425G6EH is sorted into the following speed grades: -4/-5/-6 and -75. The -4 is compliant to the DDR500/CL3 specification. The -5 is compliant to the DDR400/CL3 specification. The -6 is compliant to the DDR333/CL2.5 specification. The -75 is compliant to the DDR266/CL2 specification.

All Input reference to the positive edge of CLK (except for DQ, DM and CKE). The timing reference point for the differential clock is when the CLK and $\overline{\text{CLK}}$ signals cross during a transition. Write and Read data are synchronized with the both edges of DQS (Data Strobe).

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. W9425G6EH is ideal for main memory in high performance applications.

2. FEATURES

- 2.5V \pm 0.2V Power Supply for DDR266/333/400
- 2.6V \pm 0.1V Power Supply for DDR500
- Up to 250 MHz Clock Frequency
- Double Data Rate architecture; two data transfers per clock cycle
- Differential clock inputs (CLK and $\overline{\text{CLK}}$)
- DQS is edge-aligned with data for Read; center-aligned with data for Write
- CAS Latency: 2, 2.5 and 3
- Burst Length: 2, 4 and 8
- Auto Refresh and Self Refresh
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = 1
- 7.8 μ S refresh interval (8K/64 mS refresh)
- Maximum burst refresh cycle: 8
- Interface: SSTL_2
- Packaged in TSOP II 66-pin, using Lead free materials with RoHS compliant

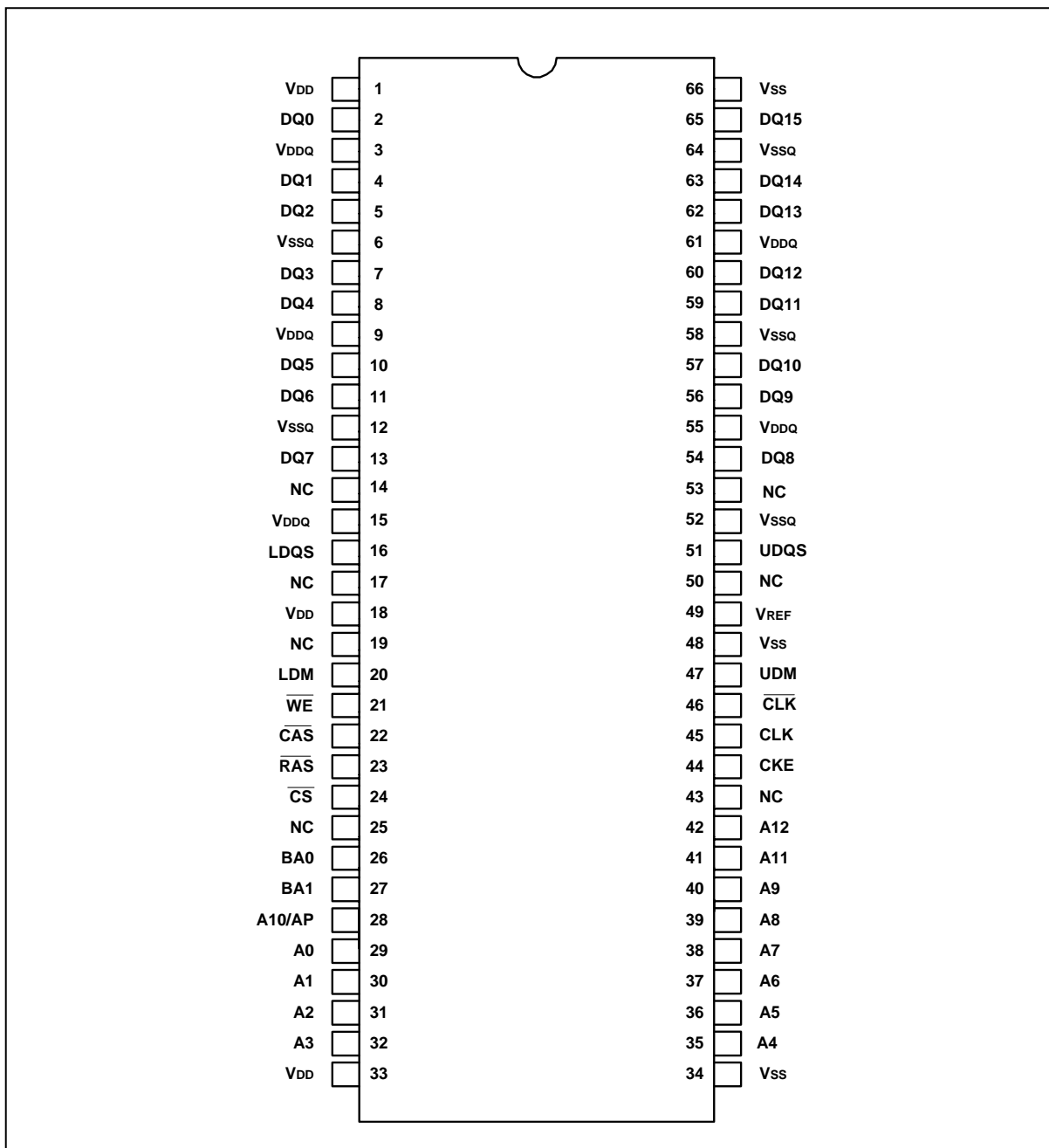


3. KEY PARAMETERS

SYMBOL	DESCRIPTION	MIN./MAX.	-4	-5	-6	-75	
tCK	Clock Cycle Time	CL = 2	Min.	-	7.5 nS	7.5 nS	7.5 nS
			Max.	-	12 nS	12 nS	12 nS
		CL = 2.5	Min.	-	6 nS	6 nS	7.5 nS
			Max.	-	12 nS	12 nS	12 nS
		CL = 3	Min.	4 nS	5 nS	6 nS	7.5 nS
			Max.	10 nS	12 nS	12 nS	12 nS
tRAS	Active to Precharge Command Period	Min.	36 nS	40 nS	42 nS	45 nS	
tRC	Active to Ref/Active Command Period	Min.	52 nS	55 nS	60 nS	67.5 nS	
I _{DD0}	Operating Current: One Bank Active-Precharge	Max.	110 mA	110 mA	110 mA	110 mA	
I _{DD1}	Operating Current: One Bank Active-Read-Precharge	Max.	150 mA	150 mA	150 mA	150 mA	
I _{DD4R}	Burst Operation Read Current	Max.	210 mA	180 mA	170 mA	160 mA	
I _{DD4W}	Burst Operation Write Current	Max.	210 mA	180 mA	170 mA	160 mA	
I _{DD5}	Auto Refresh Current	Max.	190 mA	190 mA	190 mA	190 mA	
I _{DD6}	Self-Refresh Current	Max.	3 mA	3 mA	3 mA	3 mA	



4. PIN CONFIGURATION



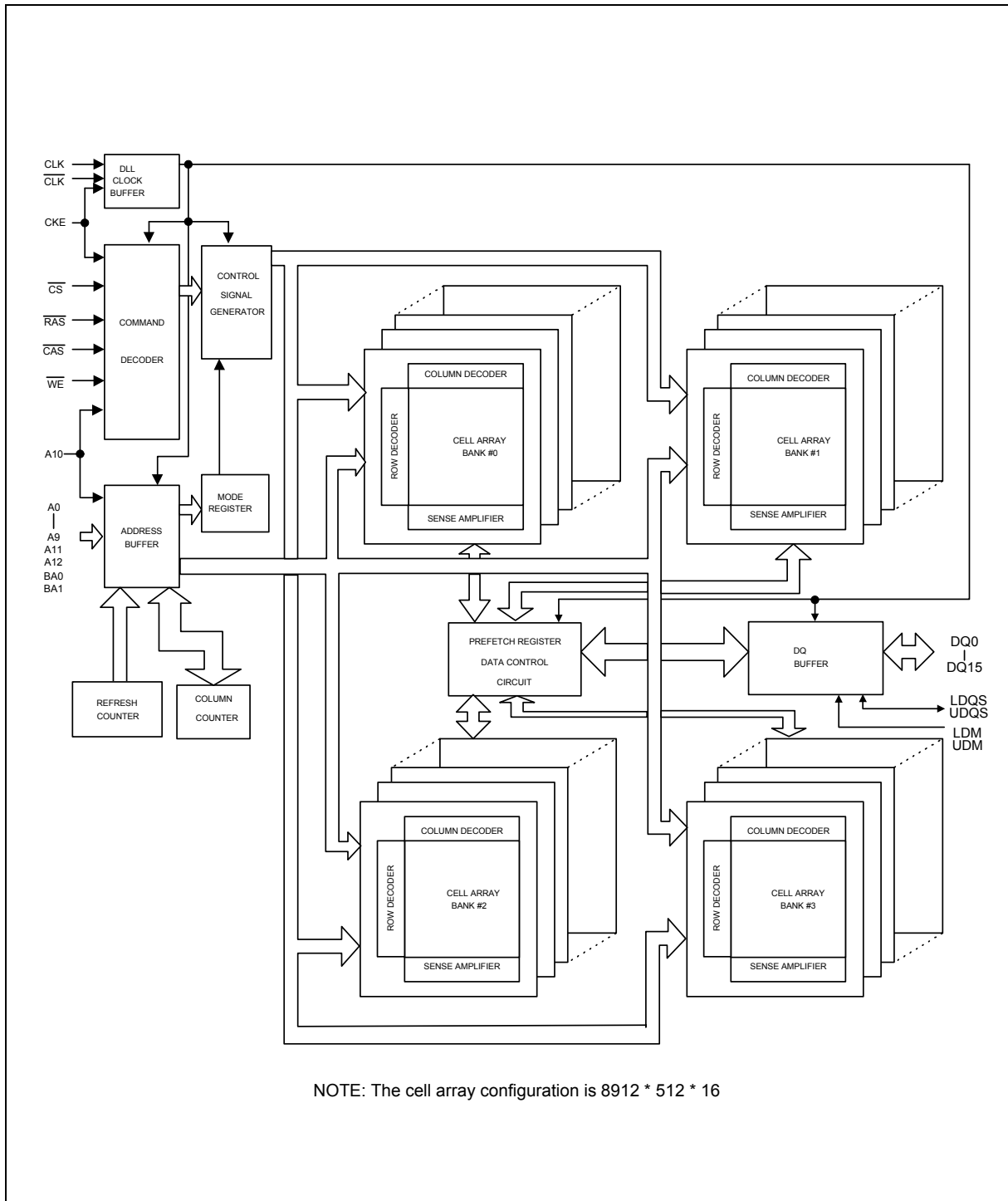


5. PIN DESCRIPTION

PIN NUMBER	PIN NAME	FUNCTION	DESCRIPTION
28 – 32, 35 – 42	A0 – A12	Address	Multiplexed pins for row and column address. Row address: A0 – A12. Column address: A0 – A8. (A10 is used for Auto-precharge)
26, 27	BA0, BA1	Bank Select	Select bank to activate during row address latch time, or bank to read/write during column address latch time.
2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ0 – DQ15	Data Input/ Output	The DQ0 – DQ15 input and output data are synchronized with both edges of DQS.
16,51	LDQS, UDQS	Data Strobe	DQS is Bi-directional signal. DQS is input signal during write operation and output signal during read operation. It is Edge-aligned with read data, Center-aligned with write data.
24	\overline{CS}	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
23, 22, 21	\overline{RAS} , \overline{CAS} , \overline{WE}	Command Inputs	Command inputs (along with \overline{CS}) define the command being entered.
20, 47	LDM, UDM	Write Mask	When DM is asserted “high” in burst write, the input data is masked. DM is synchronized with both edges of DQS.
45, 46	\overline{CLK} , CLK	Differential Clock Inputs	All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of \overline{CLK} .
44	CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
49	VREF	Reference Voltage	VREF is reference voltage for inputs.
1, 18, 33	VDD	Power (+2.5V)	Power for logic circuit inside DDR SDRAM.
34, 48, 66	VSS	Ground	Ground for logic circuit inside DDR SDRAM.
3, 9, 15, 55, 61	VDDQ	Power (+2.5V) for I/O Buffer	Separated power from VDD, used for output buffer, to improve noise.
6, 12, 52, 58, 64	VSSQ	Ground for I/O Buffer	Separated ground from VSS, used for output buffer, to improve noise.
14, 17, 19, 25, 43, 50, 53	NC	No Connection	No connection (NC pin should be connected to GND or floating)



6. BLOCK DIAGRAM



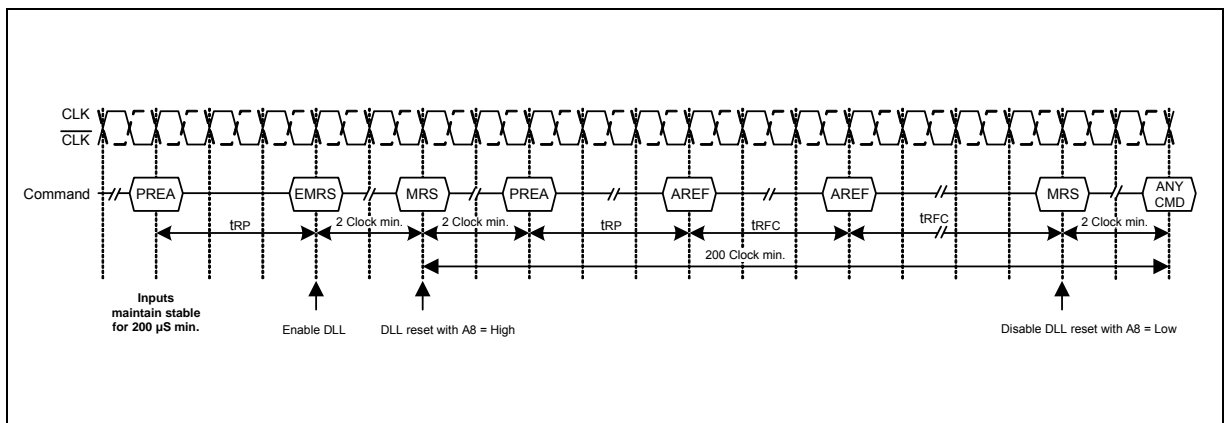
NOTE: The cell array configuration is 8912 * 512 * 16



7. FUNCTIONAL DESCRIPTION

7.1 Power Up Sequence

- (1) Apply power and attempt to CKE at a low state ($\leq 0.2V$), all other inputs may be undefined
 - 1) Apply VDD before or at the same time as VDDQ.
 - 2) Apply VDDQ before or at the same time as VTT and VREF.
- (2) Start Clock and maintain stable condition for 200 μS (min.).
- (3) After stable power and clock, apply NOP and take CKE high.
- (4) Issue precharge command for all banks of the device.
- (5) Issue EMRS (Extended Mode Register Set) to enable DLL and establish Output Driver Type.
- (6) Issue MRS (Mode Register Set) to reset DLL and set device to idle with bit A8.
- (An additional 200 cycles(min) of clock are required for DLL Lock before any executable command applied.)
- (7) Issue precharge command for all banks of the device.
- (8) Issue two or more Auto Refresh commands.
- (9) Issue MRS-Initialize device operation with the reset DLL bit deactivated A8 to low.



Initialization sequence after power-up



7.2 Command Function

7.2.1 Bank Activate Command

($\overline{\text{RAS}}$ = "L", $\overline{\text{CAS}}$ = "H", $\overline{\text{WE}}$ = "H", BA0, BA1 = Bank, A0 to A12 = Row Address)

The Bank Activate command activates the bank designated by the BA (Bank address) signal. Row addresses are latched on A0 to A12 when this command is issued and the cell data is read out of the sense amplifiers. The maximum time that each bank can be held in the active state is specified as $t_{\text{RAS (max)}}$. After this command is issued, Read or Write operation can be executed.

7.2.2 Bank Precharge Command

($\overline{\text{RAS}}$ = "L", $\overline{\text{CAS}}$ = "H", $\overline{\text{WE}}$ = "L", BA0, BA1 = Bank, A10 = "L", A0 to A9, A11, A12 = Don't Care)

The Bank Precharge command precharges the bank designated by BA. The precharged bank is switched from the active state to the idle state.

7.2.3 Precharge All Command

($\overline{\text{RAS}}$ = "L", $\overline{\text{CAS}}$ = "H", $\overline{\text{WE}}$ = "L", BA0, BA1 = Don't Care, A10 = "H", A0 to A9, A11, A12 = Don't Care)

The Precharge All command precharges all banks simultaneously. Then all banks are switched to the idle state.

7.2.4 Write Command

($\overline{\text{RAS}}$ = "H", $\overline{\text{CAS}}$ = "L", $\overline{\text{WE}}$ = "L", BA0, BA1 = Bank, A10 = "L", A0 to A8 = Column Address)

The write command performs a Write operation to the bank designated by BA. The write data are latched at both edges of DQS. The length of the write data (Burst Length) and column access sequence (Addressing Mode) must be in the Mode Register at power-up prior to the Write operation.

7.2.5 Write with Auto-precharge Command

($\overline{\text{RAS}}$ = "H", $\overline{\text{CAS}}$ = "L", $\overline{\text{WE}}$ = "L", BA0, BA1 = Bank, A10 = "H", A0 to A8 = Column Address)

The Write with Auto-precharge command performs the Precharge operation automatically after the Write operation. This command must not be interrupted by any other commands.

7.2.6 Read Command

($\overline{\text{RAS}}$ = "H", $\overline{\text{CAS}}$ = "L", $\overline{\text{WE}}$ = "H", BA0, BA1 = Bank, A10 = "L", A0 to A8 = Column Address)

The Read command performs a Read operation to the bank designated by BA. The read data are synchronized with both edges of DQS. The length of read data (Burst Length), Addressing Mode and CAS Latency (access time from $\overline{\text{CAS}}$ command in a clock cycle) must be programmed in the Mode Register at power-up prior to the Read operation.

7.2.7 Read with Auto-precharge Command

($\overline{\text{RAS}}$ = "H", $\overline{\text{CAS}}$ = "L", $\overline{\text{WE}}$ = "H", BA0, BA1 = Bank, A10 = "H", A0 to A8 = Column Address)

The Read with Auto-precharge command automatically performs the Precharge operation after the Read operation.



1) $READA \geq t_{RAS}(\text{min}) - (BL/2) \times t_{CK}$

Internal precharge operation begins after BL/2 cycle from Read with Auto-precharge command.

2) $t_{RCD}(\text{min}) \leq READA < t_{RAS}(\text{min}) - (BL/2) \times t_{CK}$

Data can be read with shortest latency, but the internal Precharge operation does not begin until after $t_{RAS}(\text{min})$ has completed.

This command must not be interrupted by any other command.

7.2.8 Mode Register Set Command

($\overline{RAS} = "L"$, $\overline{CAS} = "L"$, $\overline{WE} = "L"$, BA0 = "L", BA1 = "L", A0 to A12 = Register Data)

The Mode Register Set command programs the values of CAS Latency, Addressing Mode, Burst Length and DLL reset in the Mode Register. The default values in the Mode Register after power-up are undefined, therefore this command must be issued during the power-up sequence. Also, this command can be issued while all banks are in the idle state. Refer to the table for specific codes.

7.2.9 Extended Mode Register Set Command

($\overline{RAS} = "L"$, $\overline{CAS} = "L"$, $\overline{WE} = "L"$, BA0 = "H", BA1 = "L", A0 to A12 = Register data)

The Extended Mode Register Set command can be implemented as needed for function extensions to the standard (SDR-SDRAM). These additional functions include DLL enable/disable, output drive strength selection. The default value of the extended mode register is not defined; therefore this command must be issued during the power-up sequence for enabling DLL. Refer to the table for specific codes.

7.2.10 No-Operation Command

($\overline{RAS} = "H"$, $\overline{CAS} = "H"$, $\overline{WE} = "H"$)

The No-Operation command simply performs no operation (same command as Device Deselect).

7.2.11 Burst Read Stop Command

($\overline{RAS} = "H"$, $\overline{CAS} = "H"$, $\overline{WE} = "L"$)

The Burst stop command is used to stop the burst operation. This command is only valid during a Burst Read operation.

7.2.12 Device Deselect Command

($\overline{CS} = "H"$)

The Device Deselect command disables the command decoder so that the \overline{RAS} , \overline{CAS} , \overline{WE} and Address inputs are ignored. This command is similar to the No-Operation command.

7.2.13 Auto Refresh Command

($\overline{RAS} = "L"$, $\overline{CAS} = "L"$, $\overline{WE} = "H"$, CKE = "H", BA0, BA1, A0 to A12 = Don't Care)

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS-BEFORE-RAS (CBR) refresh in previous DRAM types. This command is non persistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The DDR SDRAM requires AUTO



REFRESH cycles at an average periodic interval of t_{REFI} (maximum). To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is $8 * t_{REFI}$.

7.2.14 Self Refresh Entry Command

(\overline{RAS} = "L", \overline{CAS} = "L", \overline{WE} = "H", CKE = "L", BA0, BA1, A0 to A12 = Don't Care)

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH. Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles should occur before a READ command can be issued. Input signals except CKE are "Don't Care" during SELF REFRESH. Since CKE is a SSTL_2 input, V_{REF} must be maintained during SELF REFRESH.

7.2.15 Self Refresh Exit Command

(CKE = "H", \overline{CS} = "H" or CKE = "H", \overline{RAS} = "H", \overline{CAS} = "H")

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for txSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra auto refresh command is recommended.

7.2.16 Data Write Enable /Disable Command

(DM = "L/H" or LDM, UDM = "L/H")

During a Write cycle, the DM or LDM, UDM signal functions as Data Mask and can control every word of the input data. The LDM signal controls DQ0 to DQ7 and UDM signal controls DQ8 to DQ15.

7.3 Read Operation

Issuing the Bank Activate command to the idle bank puts it into the active state. When the Read command is issued after t_{RCD} from the Bank Activate command, the data is read out sequentially, synchronized with both edges of DQS (Burst Read operation). The initial read data becomes available after CAS Latency from the issuing of the Read command. The CAS Latency must be set in the Mode Register at power-up.

When the Precharge Operation is performed on a bank during a Burst Read and operation, the Burst operation is terminated.

When the Read with Auto-precharge command is issued, the Precharge operation is performed automatically after the Read cycle then the bank is switched to the idle state. This command cannot be interrupted by any other commands. Refer to the diagrams for Read operation.



7.4 Write Operation

Issuing the Write command after t_{RC} from the bank activate command. The input data is latched sequentially, synchronizing with both edges (rising & falling) of DQS after the Write command (Burst write operation). The burst length of the Write data (Burst Length) and Addressing Mode must be set in the Mode Register at power-up.

When the Precharge operation is performed in a bank during a Burst Write operation, the Burst operation is terminated.

When the Write with Auto-precharge command is issued, the Precharge operation is performed automatically after the Write cycle, then the bank is switched to the idle state. The Write with Auto-precharge command cannot be interrupted by any other command for the entire burst data duration.

Refer to the diagrams for Write operation.

7.5 Precharge

There are two Commands, which perform the precharge operation (Bank Precharge and Precharge All). When the Bank Precharge command is issued to the active bank, the bank is precharged and then switched to the idle state. The Bank Precharge command can precharge one bank independently of the other bank and hold the unprecharged bank in the active state. The maximum time each bank can be held in the active state is specified as $t_{RAS(max)}$. Therefore, each bank must be precharged within $t_{RAS(max)}$ from the bank activate command.

The Precharge All command can be used to precharge all banks simultaneously. Even if banks are not in the active state, the Precharge All command can still be issued. In this case, the Precharge operation is performed only for the active bank and the precharge bank is then switched to the idle state.

7.6 Burst Termination

When the Precharge command is used for a bank in a Burst cycle, the Burst operation is terminated. When Burst Read cycle is interrupted by the Precharge command, read operation is disabled after clock cycle of (CAS Latency) from the Precharge command. When the Burst Write cycle is interrupted by the Precharge command, the input circuit is reset at the same clock cycle at which the precharge command is issued. In this case, the DM signal must be asserted "high" during t_{WR} to prevent writing the invalidated data to the cell array.

When the Burst Read Stop command is issued for the bank in a Burst Read cycle, the Burst Read operation is terminated. The Burst read Stop command is not supported during a write burst operation. Refer to the diagrams for Burst termination.

7.7 Refresh Operation

Two types of Refresh operation can be performed on the device: Auto Refresh and Self Refresh. By repeating the Auto Refresh cycle, each bank in turn refreshed automatically. The Refresh operation must be performed 8192 times (rows) within 64mS. The period between the Auto Refresh command and the next command is specified by t_{RFC} .

Self Refresh mode enters issuing the Self Refresh command (CKE asserted "low") while all banks are in the idle state. The device is in Self Refresh mode for as long as CKE held "low". In the case of distributed Auto Refresh commands, distributed auto refresh commands must be issued every 7.8 μ S and the last distributed Auto Refresh commands must be performed within 7.8 μ S before entering the self refresh mode. After exiting from the Self Refresh mode, the refresh operation must be performed within 7.8 μ S. In Self Refresh mode, all input/output buffers are disabled,



resulting in lower power dissipation (except CKE buffer). Refer to the diagrams for Refresh operation.

7.8 Power Down Mode

Two types of Power Down Mode can be performed on the device: Active Standby Power Down Mode and Precharge Standby Power Down Mode.

When the device enters the Power Down Mode, all input/output buffers and DLL are disabled resulting in low power dissipation (except CKE buffer).

Power Down Mode enter asserting CKE "low" while the device is not running a burst cycle. Taking CKE "high" can exit this mode. When CKE goes high, a No operation command must be input at next CLK rising edge. Refer to the diagrams for Power Down Mode.

7.9 Input Clock Frequency Change during Precharge Power Down Mode

DDR SDRAM input clock frequency can be changed under following condition:

DDR SDRAM must be in precharged power down mode with CKE at logic LOW level. After a minimum of 2 clocks after CKE goes LOW, the clock frequency may change to any frequency between minimum and maximum operating frequency specified for the particular speed grade. During an input clock frequency change, CKE must be held LOW. Once the input clock frequency is changed, a stable clock must be provided to DRAM before precharge power down mode may be exited. The DLL must be RESET via EMRS after precharge power down exit. An additional MRS command may need to be issued to appropriately set CL etc. After the DLL relock time, the DRAM is ready to operate with new clock frequency.

7.10 Mode Register Operation

The mode register is programmed by the Mode Register Set command (MRS/EMRS) when all banks are in the idle state. The data to be set in the Mode Register is transferred using the A0 to A12 and BA0, BA1 address inputs.

The Mode Register designates the operation mode for the read or write cycle. The register is divided into five fields: (1) Burst Length field to set the length of burst data (2) Addressing Mode selected bit to designate the column access sequence in a Burst cycle (3) CAS Latency field to set the access time in clock cycle (4) DLL reset field to reset the DLL (5) Regular/Extended Mode Register field to select a type of MRS (Regular/Extended MRS). EMRS cycle can be implemented the extended function (DLL enable/Disable mode).

The initial value of the Mode Register (including EMRS) after power up is undefined; therefore the Mode Register Set command must be issued before power operation.

7.10.1 Burst Length field (A2 to A0)

This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 2, 4, and 8 words.

A2	A1	A0	BURST LENGTH
0	0	0	Reserved
0	0	1	2 words
0	1	0	4 words
0	1	1	8 words
1	x	x	Reserved



7.10.2 Addressing Mode Select (A3)

The Addressing Mode can be one of two modes; Interleave mode or Sequential Mode, When the A3 bit is "0", Sequential mode is selected. When the A3 bit is "1", Interleave mode is selected. Both addressing Mode support burst length 2, 4, and 8 words.

A3	ADDRESSING MODE
0	Sequential
1	Interleave

7.10.2.1. Addressing Sequence of Sequential Mode

A column access is performed by incrementing the column address input to the device. The address is varied by the Burst Length as the following.

Addressing Sequence of Sequential Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	n	2 words (address bits is A0) not carried from A0 to A1
Data 1	n + 1	
Data 2	n + 2	4 words (address bit A0, A1) Not carried from A1 to A2
Data 3	n + 3	
Data 4	n + 4	8 words (address bits A2, A1 and A0) Not carried from A2 to A3
Data 5	n + 5	
Data 6	n + 6	
Data 7	n + 7	

7.10.2.2. Addressing Sequence for Interleave Mode

A Column access is started from the inputted column address and is performed by interleaving the address bits in the sequence shown as the following.

Addressing Sequence of Interleave Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words
Data 1	A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	4 words
Data 3	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	
Data 4	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0	8 words
Data 5	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$	
Data 6	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0	
Data 7	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$	



7.10.3 CAS Latency field (A6 to A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first data read. The minimum values of CAS Latency depend on the frequency of CLK.

A6	A5	A4	CAS LATENCY
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

7.10.4 DLL Reset bit (A8)

This bit is used to reset DLL. When the A8 bit is "1", DLL is reset.

7.10.5 Mode Register /Extended Mode register change bits (BA0, BA1)

These bits are used to select MRS/EMRS.

BA1	BA0	A12-A0
0	0	Regular MRS Cycle
0	1	Extended MRS Cycle
1	x	Reserved

7.10.6 Extended Mode Register field

1) DLL Switch field (A0)

This bit is used to select DLL enable or disable

A0	DLL
0	Enable
1	Disable

2) Output Driver Size Control field (A1)

This bit is used to select Output Driver Size, both Full strength and Half strength are based on JEDEC standard.

A1	OUTPUT DRIVER
0	Full Strength
1	Half Strength

7.10.7 Reserved field

- Test mode entry bit (A7)
This bit is used to enter Test mode and must be set to "0" for normal operation.
- Reserved bits (A9, A10, A11, A12)
These bits are reserved for future operations. They must be set to "0" for normal operation.



8. OPERATION MODE

The following table shows the operation commands.

8.1 Simplified Truth Table

SYM.	COMMAND	DEVICE STATE	CKEn-1	CKEn	DM ⁽⁴⁾	BA0, BA1	A10	A12, A11, A9-A0	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$
ACT	Bank Active	Idle ⁽³⁾	H	X	X	V	V	V	L	L	H	H
PRE	Bank Precharge	Any ⁽³⁾	H	X	X	V	L	X	L	L	H	L
PREA	Precharge All	Any	H	X	X	X	H	X	L	L	H	L
WRIT	Write	Active ⁽³⁾	H	X	X	V	L	V	L	H	L	L
WRITA	Write with Auto-precharge	Active ⁽³⁾	H	X	X	V	H	V	L	H	L	L
READ	Read	Active ⁽³⁾	H	X	X	V	L	V	L	H	L	H
READA	Read with Auto-precharge	Active ⁽³⁾	H	X	X	V	H	V	L	H	L	H
MRS	Mode Register Set	Idle	H	X	X	L, L	C	C	L	L	L	L
EMRS	Extended Mode Register Set	Idle	H	X	X	H, L	V	V	L	L	L	L
NOP	No Operation	Any	H	X	X	X	X	X	L	H	H	H
BST	Burst Read Stop	Active	H	X	X	X	X	X	L	H	H	L
DSL	Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AREF	Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
SELF	Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SELEX	Self Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X
									L	H	H	X
PD	Power Down Mode Entry	Idle/Active ⁽⁵⁾	H	L	X	X	X	X	H	X	X	X
									L	H	H	X
PDEX	Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
									L	H	H	X
WDE	Data Write Enable	Active	H	X	L	X	X	X	X	X	X	X
WDD	Data Write Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes:

1. V = Valid X = Don't Care L = Low level H = High level
2. CKEn signal is input level when commands are issued.
CKEn-1 signal is input level one clock cycle before the commands are issued.
3. These are state designated by the BA0, BA1 signals.
4. LDM, UDM (W9425G6EH).
5. Power Down Mode can not entry in the burst cycle.



8.2 Function Truth Table

(Note 1)

CURRENT STATE	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	ADDRESS	COMMAND	ACTION	NOTES
Idle	H	X	X	X	X	DSL	NOP	
	L	H	H	X	X	NOP/BST	NOP	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PREA	NOP	
	L	L	L	H	X	AREF/SELF	Refresh or Self refresh	2
	L	L	L	L	Op-Code	MRS/EMRS	Mode register accessing	2
Row Active	H	X	X	X	X	DSL	NOP	
	L	H	H	X	X	NOP/BST	NOP	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read: Determine AP	4
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write: Determine AP	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PREA	Precharge	5
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Read	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	Burst stop	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, new read: Determine AP	6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PREA	Term burst, precharging	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
Write	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, start read: Determine AP	6, 7
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, start read: Determine AP	6
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PREA	Term burst, precharging	8
	L	L	L	H	X	AREF/SELF	ILLEGAL	
L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL		



Function Truth Table, continued

CURRENT STATE	CS	RAS	CAS	WE	ADDRESS	COMMAND	ACTION	NOTES
Read with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Precharging	H	X	X	X	X	DSL	NOP -> Idle after trP	
	L	H	H	H	X	NOP	NOP -> Idle after trP	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PREA	Idle after trP	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Row Activating	H	X	X	X	X	DSL	NOP -> Row active after trCD	
	L	H	H	H	X	NOP	NOP -> Row active after trCD	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	



Function Truth Table, continued

CURRENT STATE	CS	RAS	CAS	WE	ADDRESS	COMMAND	ACTION	NOTES
Write Recovering	H	X	X	X	X	DSL	NOP ->Row active after tWR	
	L	H	H	H	X	NOP	NOP ->Row active after tWR	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRTA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
Write Recovering with Auto-precharge	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
	H	X	X	X	X	DSL	NOP ->Enter precharge after tWR	
	L	H	H	H	X	NOP	NOP ->Enter precharge after tWR	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRTA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	3
Refreshing	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
	H	X	X	X	X	DSL	NOP ->Idle after tRC	
	L	H	H	H	X	NOP	NOP ->Idle after tRC	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	X	READ/WRIT	ILLEGAL	
Mode Register Accessing	L	L	H	X	X	ACT/PRE/PREA	ILLEGAL	
	L	L	L	X	X	AREF/SELF/MRS/EMRS	ILLEGAL	
	H	X	X	X	X	DSL	NOP ->Row after tMRD	
	L	H	H	H	X	NOP	NOP ->Row after tMRD	
	L	H	H	L	X	BST	ILLEGAL	
L	H	L	X	X	READ/WRIT	ILLEGAL		
L	L	X	X	X	ACT/PRE/PREA/AREF/SELF/MRS/EMRS	ILLEGAL		

Notes:

1. All entries assume that CKE was active (High level) during the preceding clock cycle and the current clock cycle.
2. Illegal if any bank is not idle.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. Illegal if tRCD is not satisfied.
5. Illegal if tRAS is not satisfied.
6. Must satisfy burst interrupt condition.
7. Must avoid bus contention, bus turn around, and/or satisfy write recovery requirements.
8. Must mask preceding data which don't satisfy tWR

Remark: H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data



8.3 Function Truth Table for CKE

CURRENT STATE	CKE		\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	ADDRESS	ACTION	NOTES
	n-1	n							
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh -> Idle after t _{XSNR}	
	L	H	L	H	H	X	X	Exit Self Refresh -> Idle after t _{XSNR}	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power down -> Idle after t _{is}	
	L	L	X	X	X	X	X	Maintain power down mode	
All banks Idle	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power down	2
	H	L	L	H	H	X	X	Enter Power down	2
	H	L	L	L	L	H	X	Self Refresh	1
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power down	
Row Active	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power down	3
	H	L	L	H	H	X	X	Enter Power down	3
	H	L	L	L	L	H	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power down	
Any State Other Than Listed Above	H	H	X	X	X	X	X	Refer to Function Truth Table	

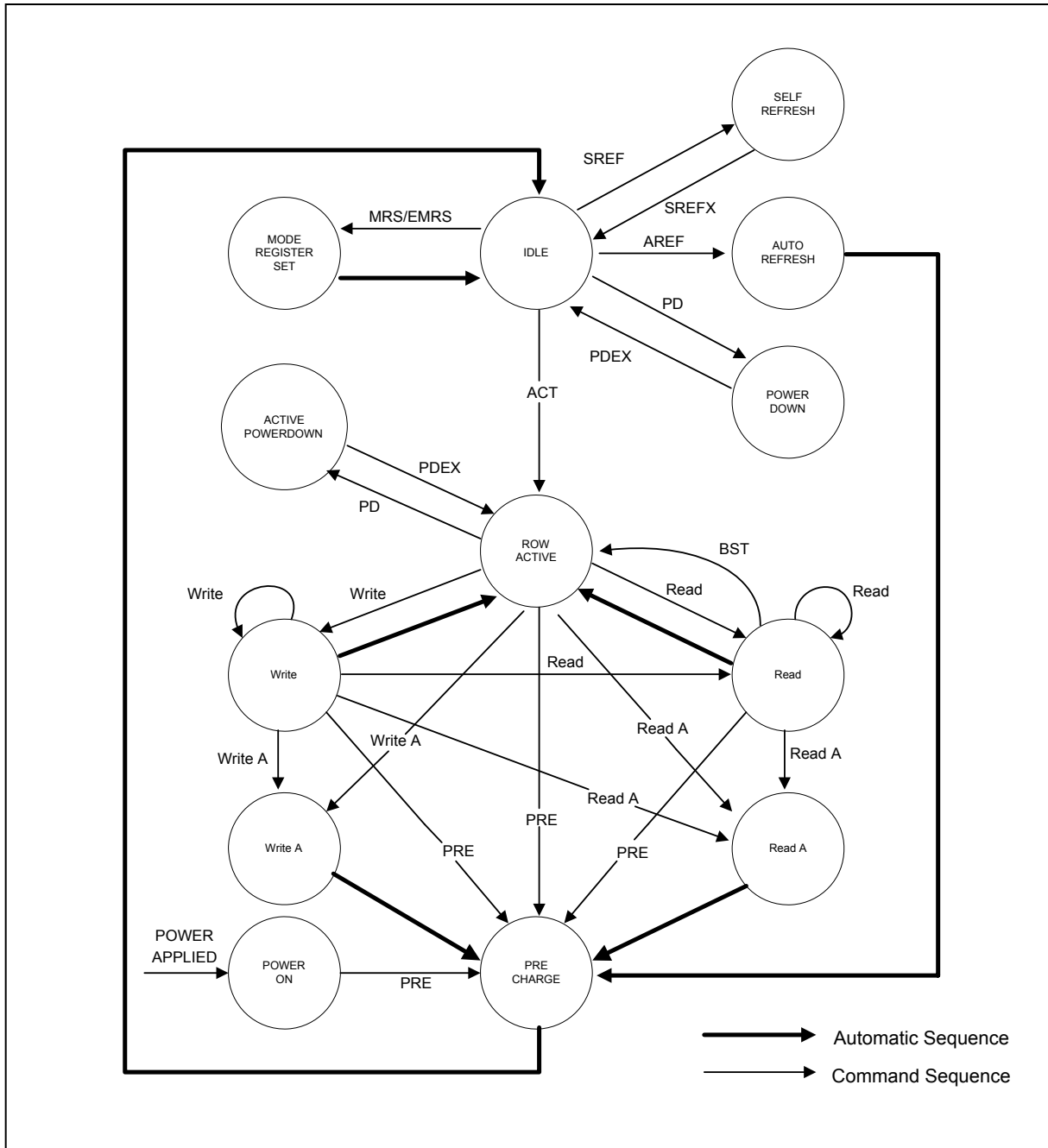
Notes:

1. Self refresh can enter only from the all banks idle state.
2. Power Down occurs when all banks are idle; this mode is referred to as precharge power down.
3. Power Down occurs when there is a row active in any bank; this mode is referred to as active power down.

Remark: H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data



8.4 Simplified Stated Diagram





9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Input/Output Voltage	V _{IN} , V _{OUT}	-0.3 ~ V _{DDQ} + 0.3	V
Power Supply Voltage	V _{DD} , V _{DDQ}	-0.3 ~ 3.6	V
Operating Temperature	T _{OPR}	0 ~ 70	°C
Storage Temperature	T _{STG}	-55 ~ 150	°C
Soldering Temperature (10s)	T _{SOLDER}	260	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OUT}	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect reliability.

9.2 Recommended DC Operating Conditions

(T_A = 0 to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V _{DD}	Power Supply Voltage (for -5/-6/-75)	2.3	2.5	2.7	V	2
V _{DD}	Power Supply Voltage (for -4)	2.5	2.6	2.7	V	2
V _{DDQ}	I/O Buffer Supply Voltage (for -5/-6/-75)	2.3	2.5	2.7	V	2
V _{DDQ}	I/O Buffer Supply Voltage (for -4)	2.5	2.6	2.7	V	2
V _{REF}	Input reference Voltage	0.49 x V _{DDQ}	0.50 x V _{DDQ}	0.51 x V _{DDQ}	V	2, 3
V _{TT}	Termination Voltage (System)	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04	V	2, 8
V _{IH} (DC)	Input High Voltage (DC)	V _{REF} + 0.15	-	V _{DDQ} + 0.3	V	2
V _{IL} (DC)	Input Low Voltage (DC)	-0.3	-	V _{REF} - 0.15	V	2
V _{ICK} (DC)	Differential Clock DC Input Voltage	-0.3	-	V _{DDQ} + 0.3	V	15
V _{ID} (DC)	Input Differential Voltage. CLK and $\overline{\text{CLK}}$ inputs (DC)	0.36	-	V _{DDQ} + 0.6	V	13, 15
V _{IH} (AC)	Input High Voltage (AC)	V _{REF} + 0.31	-	-	V	2
V _{IL} (AC)	Input Low Voltage (AC)	-	-	V _{REF} - 0.31	V	2
V _{ID} (AC)	Input Differential Voltage. CLK and $\overline{\text{CLK}}$ inputs (AC)	0.7	-	V _{DDQ} + 0.6	V	13, 15
V _X (AC)	Differential AC input Cross Point Voltage	V _{DDQ} /2 - 0.2	-	V _{DDQ} /2 + 0.2	V	12, 15
V _{ISO} (AC)	Differential Clock AC Middle Point	V _{DDQ} /2 - 0.2	-	V _{DDQ} /2 + 0.2	V	14, 15

Notes: Undershoot Limit: V_{IL} (min) = -1.5V with a pulse width ≤ 5 nS

Overshoot Limit: V_{IH} (max) = V_{DDQ} + 1.5V with a pulse width ≤ 5 nS

V_{IH} (DC) and V_{IL} (DC) are levels to maintain the current logic state.

V_{IH} (AC) and V_{IL} (AC) are levels to change to the new logic state.



9.3 Capacitance

(V_{DD} = V_{DDQ} = 2.5V ±0.2V, f = 1 MHz, T_A = 25 °C, V_{OUT} (DC) = V_{DDQ}/2, V_{OUT} (Peak to Peak) = 0.2V)

SYMBOL	PARAMETER	MIN.	MAX.	DELTA (MAX.)	UNIT
C _{IN}	Input Capacitance (except for CLK pins)	2.0	3.0	0.5	pF
C _{CLK}	Input Capacitance (CLK pins)	2.0	3.0	0.25	pF
C _{I/O}	DQ, DQS, DM Capacitance	4.0	5.0	0.5	pF
C _{NC}	NC Pin Capacitance	-	1.5	-	pF

Notes: These parameters are periodically sampled and not 100% tested.

The NC pins have additional capacitance for adjustment of the adjacent pin capacitance.

9.4 Leakage and Output Buffer Characteristics

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
I _I (L)	Input Leakage Current (0V ≤ V _{IN} ≤ V _{DDQ} , All other pins not under test = 0V)	-2	2	μA	
I _O (L)	Output Leakage Current (Output disabled, 0V ≤ V _{OUT} ≤ V _{DDQ})	-5	5	μA	
V _{OH}	Output High Voltage (under AC test load condition)	V _{TT} +0.76	-	V	
V _{OL}	Output Low Voltage (under AC test load condition)	-	V _{TT} -0.76	V	
I _{OH} (DC)	Output Minimum Source DC Current	-15.2	-	mA	4, 6
I _{OL} (DC)	Output Minimum Sink DC Current	15.2	-	mA	4, 6
I _{OH} (DC)	Output Minimum Source DC Current	-10.4	-	mA	5
I _{OL} (DC)	Output Minimum Sink DC Current	10.4	-	mA	5



9.5 DC Characteristics

SYM.	PARAMETER	MAX.				UNIT	NOTES
		-4	-5	-6	-75		
IDD0	Operating current: One Bank Active-Precharge; $t_{RC} = t_{RC} \text{ min}$; $t_{CK} = t_{CK} \text{ min}$; DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	110	110	110	110	mA	7
IDD1	Operating current: One Bank Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC} \text{ min}$; $CL = 3$; $t_{CK} = t_{CK} \text{ min}$; $I_{OUT} = 0 \text{ mA}$; Address and control inputs changing once per clock cycle.	150	150	150	150		7, 9
IDD2P	Precharge Power Down standby current: All Banks Idle; Power down mode; $CKE \leq V_{IL} \text{ max}$; $t_{CK} = t_{CK} \text{ min}$; $V_{in} = V_{REF}$ for DQ, DQS and DM	20	20	20	20		
IDD2F	Idle floating standby current: $\overline{CS} \geq V_{IH} \text{ min}$; All Banks Idle; $CKE \geq V_{IH} \text{ min}$; Address and other control inputs changing once per clock cycle; $V_{in} = V_{ref}$ for DQ, DQS and DM	45	45	45	40		7
IDD2N	Idle standby current: $\overline{CS} \geq V_{IH} \text{ min}$; All Banks Idle; $CKE \geq V_{IH} \text{ min}$; $t_{CK} = t_{CK} \text{ min}$; Address and other control inputs changing once per clock cycle; $V_{in} \geq V_{IH} \text{ min}$ or $V_{in} \leq V_{IL} \text{ max}$ for DQ, DQS and DM	45	45	45	40		7
IDD2Q	Idle quiet standby current: $\overline{CS} \geq V_{IH} \text{ min}$; All Banks Idle; $CKE \geq V_{IH} \text{ min}$; $t_{CK} = t_{CK} \text{ min}$; Address and other control inputs stable; $V_{in} \geq V_{REF}$ for DQ, DQS and DM	40	40	40	35		7
IDD3P	Active Power Down standby current: One Bank Active; Power down mode; $CKE \leq V_{IL} \text{ max}$; $t_{CK} = t_{CK} \text{ min}$	20	20	20	20		
IDD3N	Active standby current: $\overline{CS} \geq V_{IH} \text{ min}$; $CKE \geq V_{IH} \text{ min}$; One Bank Active-Precharge; $t_{RC} = t_{RAS} \text{ max}$; $t_{CK} = t_{CK} \text{ min}$; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	70	70	70	65		7
IDD4R	Operating current: Burst = 2; Reads; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; $CL=3$; $t_{CK} = t_{CK} \text{ min}$; $I_{OUT} = 0\text{mA}$	210	180	170	160		7, 9
IDD4W	Operating current: Burst = 2; Write; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; $CL = 3$; $t_{CK} = t_{CK} \text{ min}$; DQ, DM and DQS inputs changing twice per clock cycle	210	180	170	160		7
IDD5	Auto Refresh current: $t_{RC} = t_{RFC} \text{ min}$	190	190	190	190		7
IDD6	Self Refresh current: $CKE \leq 0.2V$	3	3	3	3		
IDD7	Random Read current: 4 Banks Active Read with activate every 20nS, Auto-precharge Read every 20 nS; Burst = 4; $t_{RCD} = 3$; $I_{OUT} = 0\text{mA}$; DQ, DM and DQS inputs changing twice per clock cycle; Address changing once per clock cycle	300	300	300	300		



9.6 AC Characteristics and Operating Condition

(Notes: 10, 12)

SYM.	PARAMETER	-4		-5		UNIT	NOTES	
		MIN.	MAX.	MIN.	MAX.			
tRC	Active to Ref/Active Command Period	52		55		nS		
tRFC	Ref to Ref/Active Command Period	60		70				
tRAS	Active to Precharge Command Period	36	70000	40	70000			
tRCD	Active to Read/Write Command Delay Time	16		15				
tRAP	Active to Read with Auto-precharge Enable	16		15				
tCCD	Read/Write(a) to Read/Write(b) Command Period	1		1		tck		
tRP	Precharge to Active Command Period	16		15		nS		
tRRD	Active(a) to Active(b) Command Period	8		10				
tWR	Write Recovery Time	15		15				
tdAL	Auto-precharge Write Recovery + Precharge Time	--		--				18
tCK	CLK Cycle Time	2	--	--	7.5		12	
		2.5	--	--	6		12	
		3	4	10	5		12	
tAC	Data Access Time from CLK, $\overline{\text{CLK}}$	-0.7	0.7	-0.7	0.7			16
tdQSK	DQS Output Access Time from CLK, $\overline{\text{CLK}}$	-0.6	0.6	-0.6	0.6			
tdSQS	Data Strobe Edge to Output Data Edge Skew		0.45		0.4			
tCH	CLK High Level Width	0.45	0.55	0.45	0.55	tck	11	
tCL	CLK Low Level Width	0.45	0.55	0.45	0.55			
tHP	CLK Half Period (minimum of actual tCH, tCL)	min (tCL,tCH)		Min, (tCL,tCH)		nS		
tQH	DQ Output Data Hold Time from DQS	tHP -0.5		tHP -0.5				
tRPRE	DQS Read Preamble Time	0.9	1.1	0.9	1.1	tck	11	
tRPST	DQS Read Postamble Time	0.4	0.6	0.4	0.6			
tDS	DQ and DM Setup Time	0.4		0.4		nS		
tDH	DQ and DM Hold Time	0.4		0.4				
tDIPW	DQ and DM Input Pulse Width (for each input)	1.75		1.75		tck	11	
tdQSH	DQS Input High Pulse Width	0.35		0.35				
tdQSL	DQS Input Low Pulse Width	0.35		0.35				
tdSS	DQS Falling Edge to CLK Setup Time	0.2		0.2				
tdSH	DQS Falling Edge Hold Time from CLK	0.2		0.2				
tWPRES	Clock to DQS Write Preamble Set-up Time	0		0		nS		
tWPRE	DQS Write Preamble Time	0.25		0.25		tck	11	
tWPST	DQS Write Postamble Time	0.4	0.6	0.4	0.6			
tdQSS	Write Command to First DQS Latching Transition	0.85	1.15	0.72	1.25			
tIS	Input Setup Time (fast slew rate)	0.6		0.6		nS	19, 21-23	
tIH	Input Hold Time (fast slew rate)	0.6		0.6			19, 21-23	
tIS	Input Setup Time (slow slew rate)	0.7		0.7			20-23	
tIH	Input Hold Time (slow slew rate)	0.7		0.7			20-23	
tIPW	Control & Address Input Pulse Width (for each input)	2.2		2.2				
tHZ	Data-out High-impedance Time from CLK, $\overline{\text{CLK}}$	-0.7	0.7	-0.7	0.7			
tLZ	Data-out Low-impedance Time from CLK, $\overline{\text{CLK}}$	-0.7	0.7	-0.7	0.7			
tT(SS)	SSTL Input Transition	0.5	1.5	0.5	1.5			
tWTR	Internal Write to Read Command Delay	1		2		tck		
tXSNR	Exit Self Refresh to non-Read Command	72		75		nS		
tXSRD	Exit Self Refresh to Read Command	200		200		tck		
tREFI	Refresh Time (8k/64mS)		7.8		7.8	μ S	17	
tMRD	Mode Register Set Cycle Time	8		10		nS		



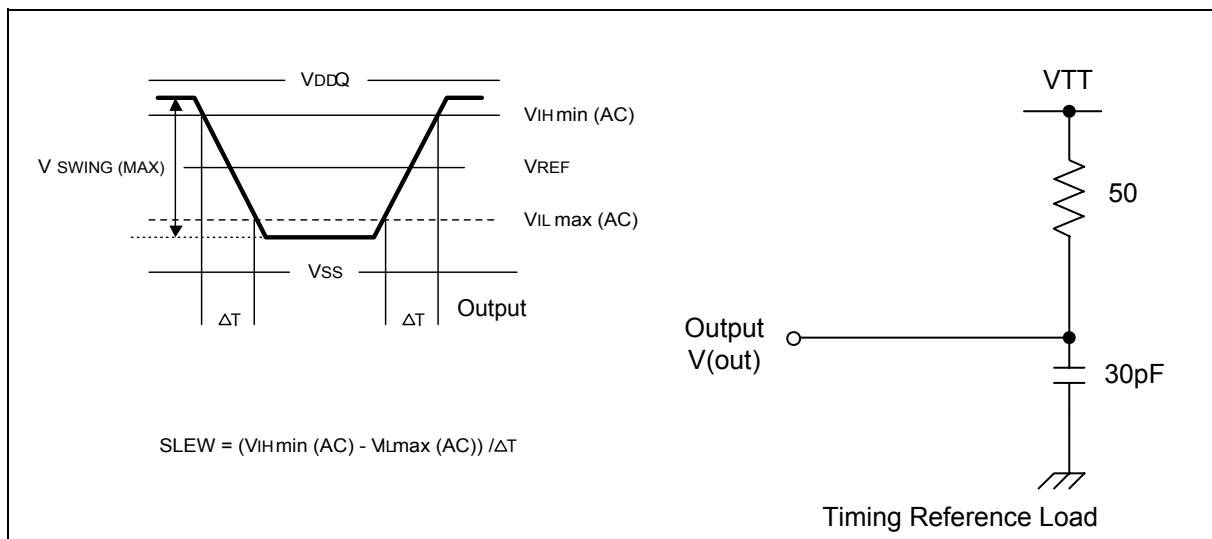
Continued

SYM.	PARAMETER	-6		-75		UNIT	NOTES	
		MIN.	MAX.	MIN.	MAX.			
tRC	Active to Ref/Active Command Period	60		67.5		nS		
tRFC	Ref to Ref/Active Command Period	72		75				
tRAS	Active to Precharge Command Period	42	100000	45	100000			
tRCD	Active to Read/Write Command Delay Time	18		20				
tRAP	Active to Read with Auto-precharge Enable	15		15				
tCCD	Read/Write(a) to Read/Write(b) Command Period	1		1		tck		
tRP	Precharge to Active Command Period	18		20		nS		
tRRD	Active(a) to Active(b) Command Period	12		15				
tWR	Write Recovery Time	15		15				
tDAL	Auto-precharge Write Recovery + Precharge Time	--		--			18	
tCK	CLK Cycle Time	2	7.5	12	7.5		12	
		2.5	6	12	7.5		12	
		3	6	12	7.5		12	
tAC	Data Access Time from CLK, $\overline{\text{CLK}}$	-0.7	0.7	-0.75	0.75		tck	16
tDQSK	DQS Output Access Time from CLK, $\overline{\text{CLK}}$	-0.6	0.6	-0.75	0.75			
tDQSQ	Data Strobe Edge to Output Data Edge Skew		0.45		0.5			
tCH	CLK High Level Width	0.45	0.55	0.45	0.55	tck	11	
tCL	CLK Low Level Width	0.45	0.55	0.45	0.55			
tHP	CLK Half Period (minimum of actual tCH, tCL)	min (tCL,tCH)		Min, (tCL,tCH)		nS		
tQH	DQ Output Data Hold Time from DQS	tHP -0.55		tHP -0.75				
tRPRE	DQS Read Preamble Time	0.9	1.1	0.9	1.1	tck	11	
tRPST	DQS Read Postamble Time	0.4	0.6	0.4	0.6			
tDS	DQ and DM Setup Time	0.45		0.5		nS		
tDH	DQ and DM Hold Time	0.45		0.5				
tDIPW	DQ and DM Input Pulse Width (for each input)	1.75		1.75				
tDQSH	DQS Input High Pulse Width	0.35		0.35		tck	11	
tDQSL	DQS Input Low Pulse Width	0.35		0.35				
tDSS	DQS Falling Edge to CLK Setup Time	0.2		0.2				
tDSH	DQS Falling Edge Hold Time from CLK	0.2		0.2				
tWPRES	Clock to DQS Write Preamble Set-up Time	0		0				
tWPRE	DQS Write Preamble Time	0.25		0.25		tck	11	
tWPST	DQS Write Postamble Time	0.4	0.6	0.4				
tDQSS	Write Command to First DQS Latching Transition	0.75	1.25	0.75	1.25			
tIS	Input Setup Time (fast slew rate)	0.75		0.9		nS	19, 21-23	
tIH	Input Hold Time (fast slew rate)	0.75		0.9			19, 21-23	
tIS	Input Setup Time (slow slew rate)	0.8		1.0			20-23	
tIH	Input Hold Time (slow slew rate)	0.8		1.0			20-23	
tIPW	Control & Address Input Pulse Width (for each input)	2.2		2.2				
tHZ	Data-out High-impedance Time from CLK, $\overline{\text{CLK}}$	-0.7	0.7	-0.75	0.75			
tLZ	Data-out Low-impedance Time from CLK, $\overline{\text{CLK}}$	-0.7	0.7	-0.75	0.75			
tT(SS)	SSTL Input Transition	0.5	1.5	0.5	1.5			
tWTR	Internal Write to Read Command Delay	1		1		tck		
tXSNR	Exit Self Refresh to non-Read Command	72		75		nS		
tXSRD	Exit Self Refresh to Read Command	200		200		tck		
tREFI	Refresh Time (8k/64mS)		7.8		7.8	μ S	17	
tMRD	Mode Register Set Cycle Time	12		15		nS		



9.7 AC Test Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Input High Voltage (AC)	V _{IH}	V _{REF} + 0.31	V
Input Low Voltage (AC)	V _{IL}	V _{REF} - 0.31	V
Input Reference Voltage	V _{REF}	0.5 x V _{DDQ}	V
Termination Voltage	V _{TT}	0.5 x V _{DDQ}	V
Differential Clock Input Reference Voltage	V _R	V _x (AC)	V
Input Difference Voltage. CLK and $\overline{\text{CLK}}$ Inputs (AC)	V _{ID} (AC)	1.5	V
Output Timing Measurement Reference Voltage	V _{OTR}	0.5 x V _{DDQ}	V

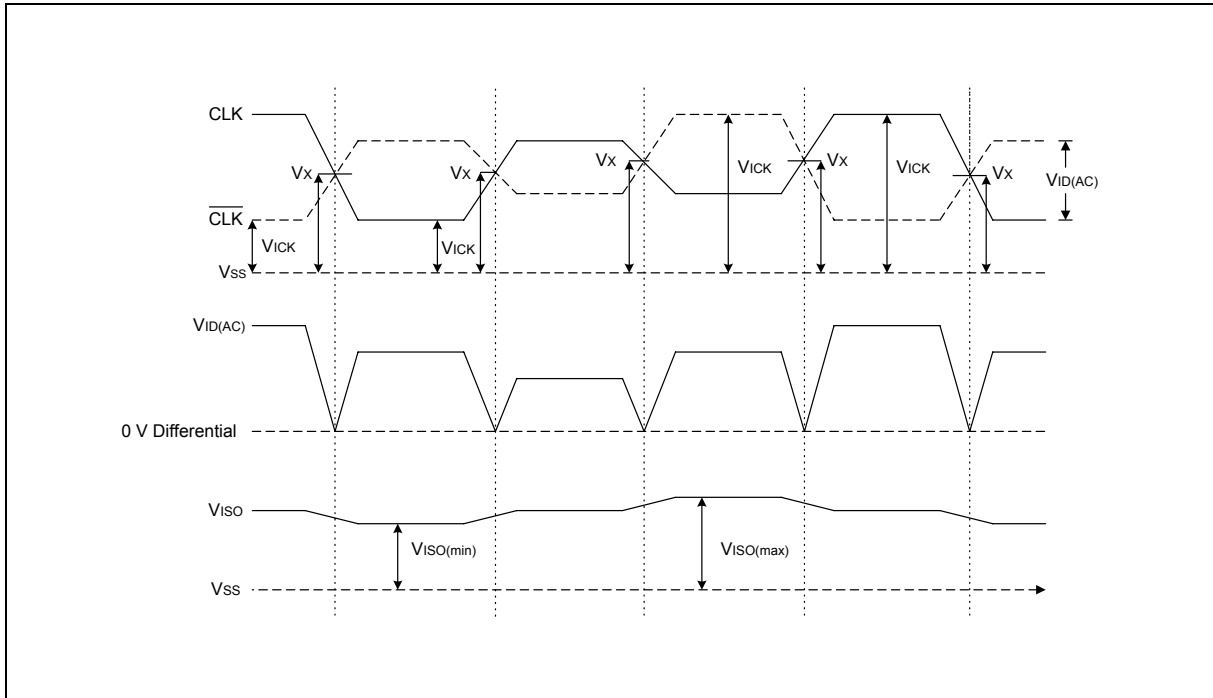


Notes:

- (1) Conditions outside the limits listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- (2) All voltages are referenced to V_{SS}, V_{SSQ} (2.6V±0.1V for DDR500)
- (3) Peak to peak AC noise on V_{REF} may not exceed ±2% V_{REF}(DC).
- (4) V_{OH} = 1.95V, V_{OL} = 0.35V
- (5) V_{OH} = 1.9V, V_{OL} = 0.4V
- (6) The values of I_{OH}(DC) is based on V_{DDQ} = 2.3V and V_{TT} = 1.19V.
The values of I_{OL}(DC) is based on V_{DDQ} = 2.3V and V_{TT} = 1.11V.
- (7) These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.
- (8) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- (9) These parameters depend on the output loading. Specified values are obtained with the output open.
- (10) Transition times are measured between V_{IH min}(AC) and V_{IL max}(AC). Transition (rise and fall) of input signals have a fixed slope.



- (11) IF the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., $T_{DQSS} = 0.75 \times t_{CK}$, $t_{CK} = 7.5 \text{ nS}$, $0.75 \times 7.5 \text{ nS} = 5.625 \text{ nS}$ is rounded up to 5.6 nS.)
- (12) V_x is the differential clock cross point voltage where input timing measurement is referenced.
- (13) V_{ID} is magnitude of the difference between CLK input level and $\overline{\text{CLK}}$ input level.
- (14) V_{ISO} means $\{V_{ICK}(\text{CLK}) + V_{ICK}(\overline{\text{CLK}})\} / 2$.
- (15) Refer to the figure below.



- (16) t_{AC} and t_{DQCK} depend on the clock jitter. These timing are measured at stable clock.
- (17) A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
- (18) $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$
- (19) For command/address input slew rate $\geq 1.0 \text{ V/nS}$.
- (20) For command/address input slew rate $\geq 0.5 \text{ V/nS}$ and $< 1.0 \text{ V/nS}$.
- (21) For CLK & $\overline{\text{CLK}}$ slew rate $\geq 1.0 \text{ V/nS}$ (single-ended).
- (22) These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
- (23) Slew Rate is measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.



9.8 AC Overshoot/Undershoot Specification for Address and Control Pins

PARAMETER	SPECIFICATION			
	DDR500	DDR400	DDR333	DDR266
Maximum peak amplitude allowed for overshoot	1.5 V	1.5 V	1.5 V	1.5 V
Maximum peak amplitude allowed for undershoot	1.5 V	1.5 V	1.5 V	1.5 V
The area between the overshoot signal and VDD must be less than or equal to Max. area in Figure 1	3.0 V-nS	3.0 V-nS	3.6 V-nS	4.5 V-nS
The area between the undershoot signal and GND must be less than or equal to Max. area in Figure 1	3.0 V-nS	3.0 V-nS	3.6 V-nS	4.5 V-nS

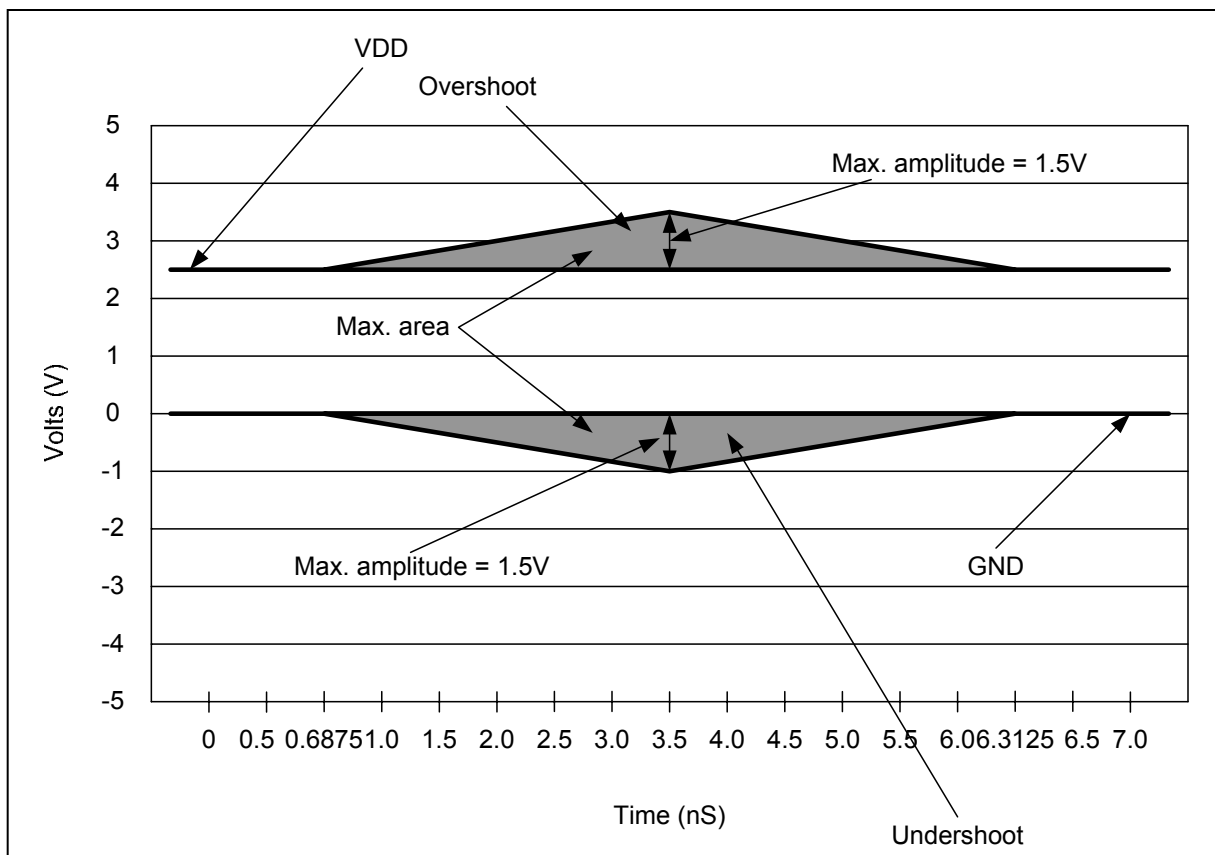


Figure 1: Address and Control AC Overshoot and Undershoot Definition



9.9 Overshoot/Undershoot Specification for Data, Strobe, and Mask Pins

PARAMETER	SPECIFICATION			
	DDR500	DDR400	DDR333	DDR266
Maximum peak amplitude allowed for overshoot	1.2 V	1.2 V	1.2 V	1.2 V
Maximum peak amplitude allowed for undershoot	1.2 V	1.2 V	1.2 V	1.2 V
The area between the overshoot signal and VDD must be less than or equal to Max. area in Figure 2	1.44 V-nS	1.44 V-nS	2.25 V-nS	2.4 V-nS
The area between the undershoot signal and GND must be less than or equal to Max. area in Figure 2	1.44 V-nS	1.44 V-nS	2.25 V-nS	2.4 V-nS

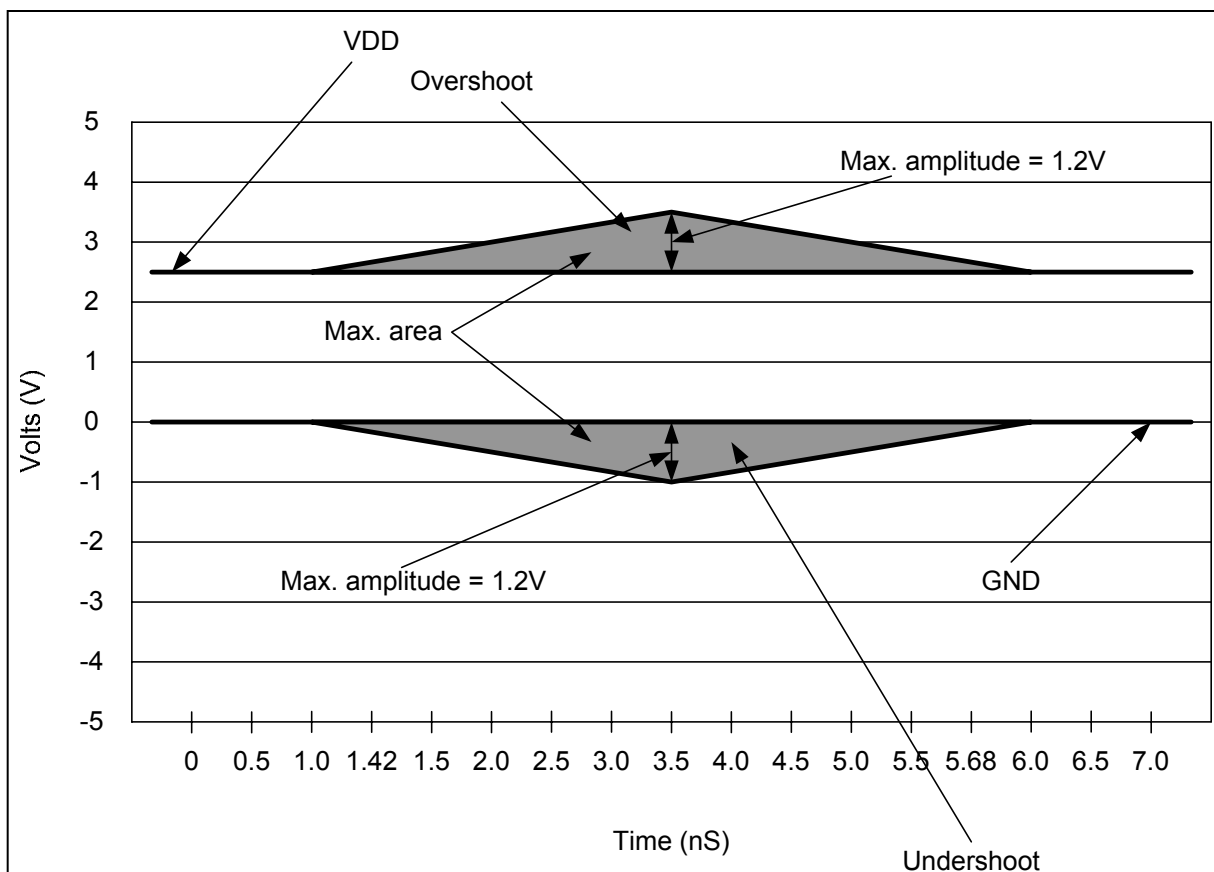
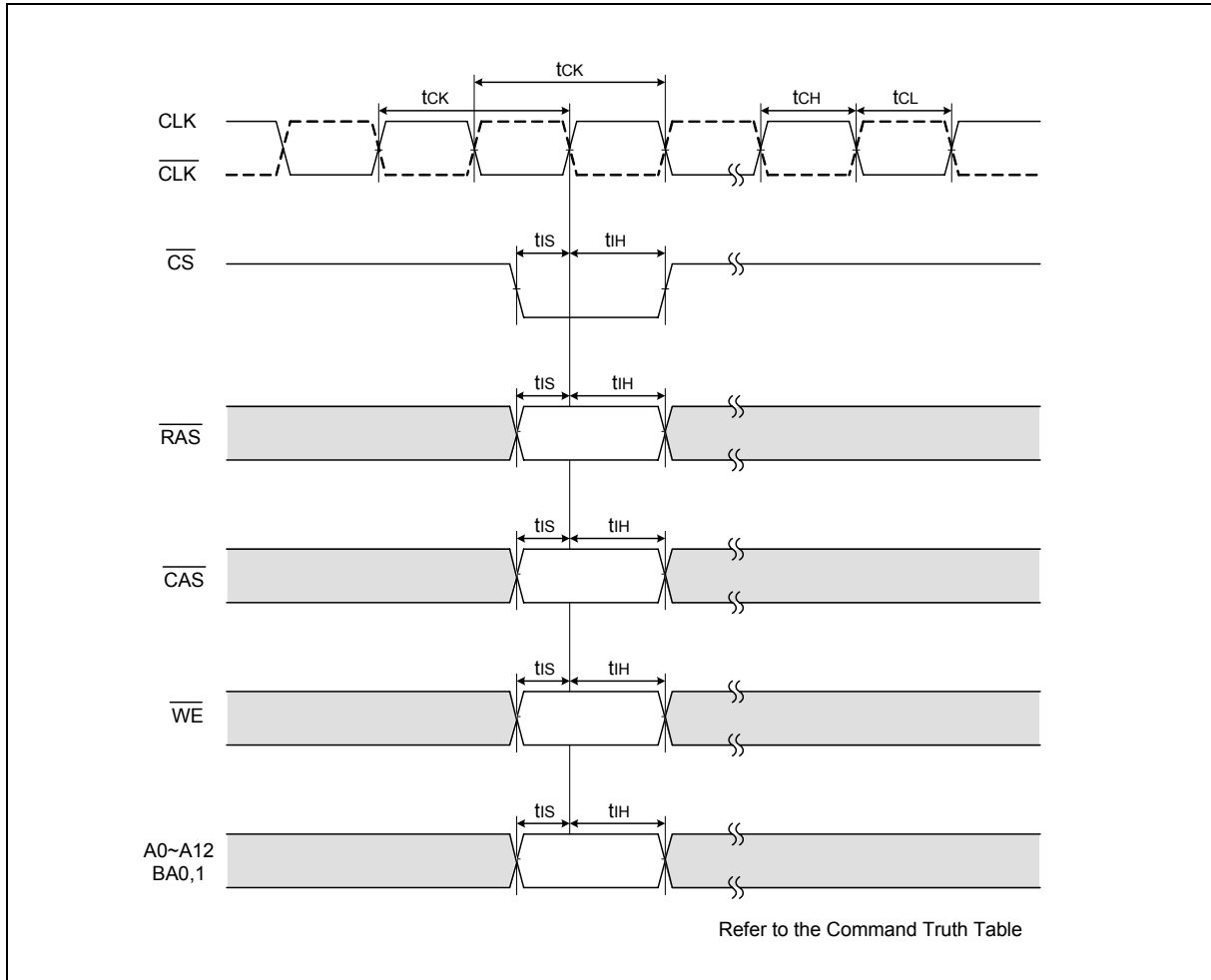


Figure 2: DQ/DM/DQS AC Overshoot and Undershoot Definition

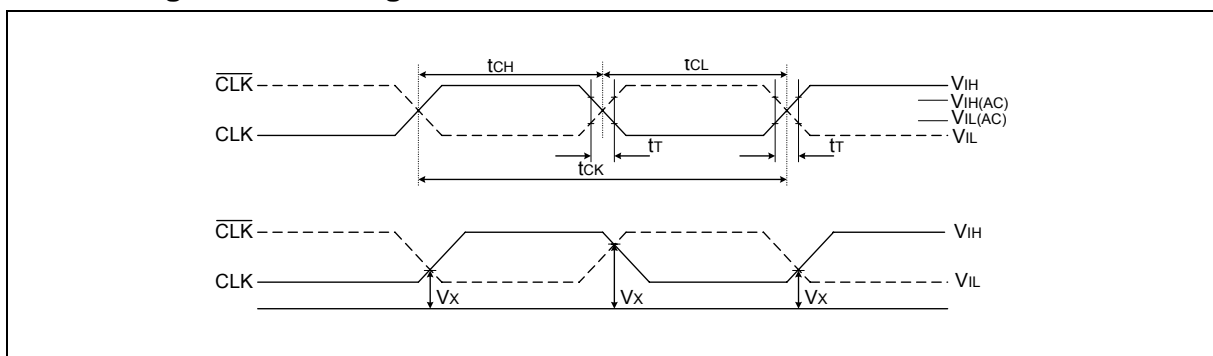


10. TIMING WAVEFORMS

10.1 Command Input Timing

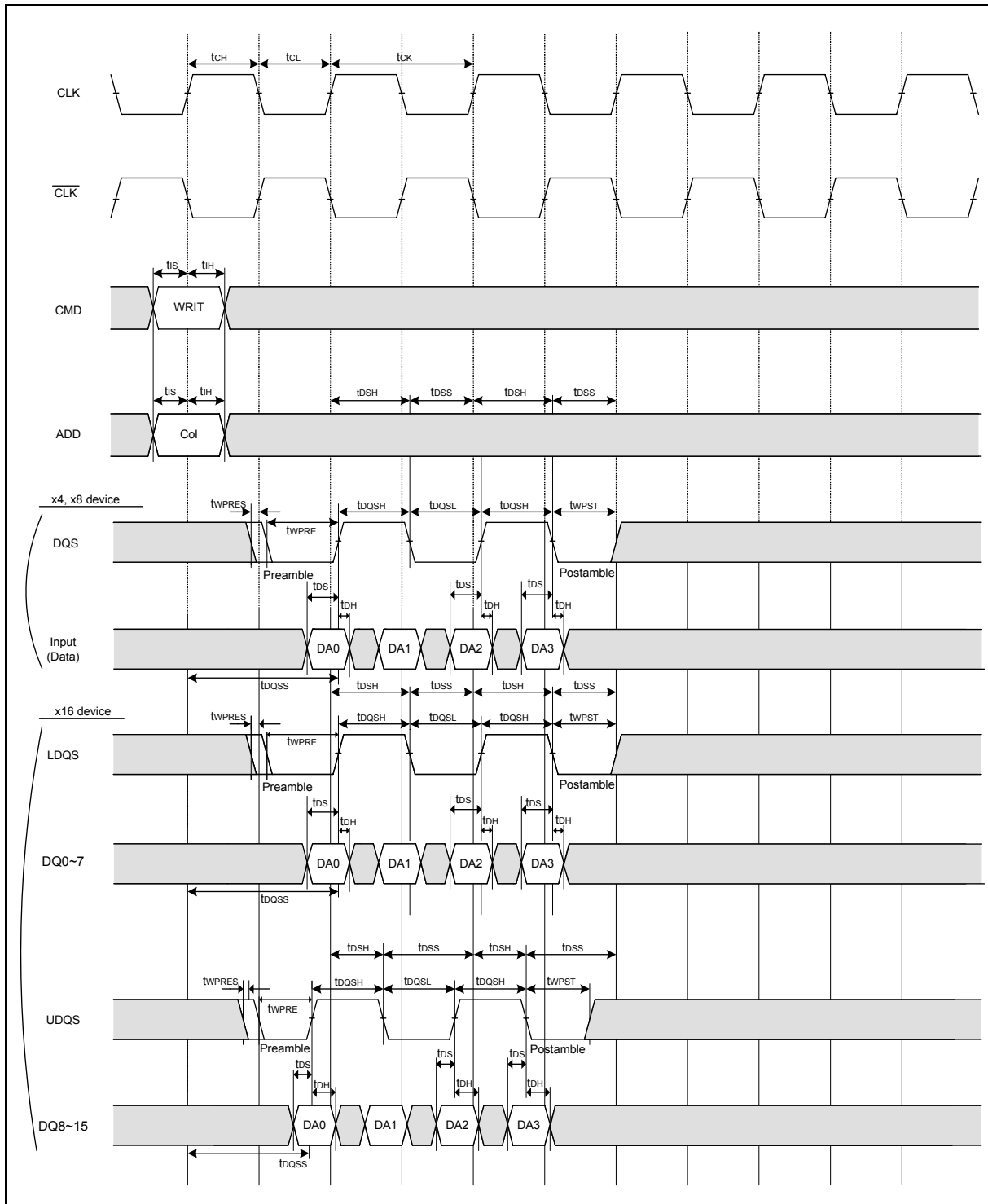


10.2 Timing of the CLK Signals





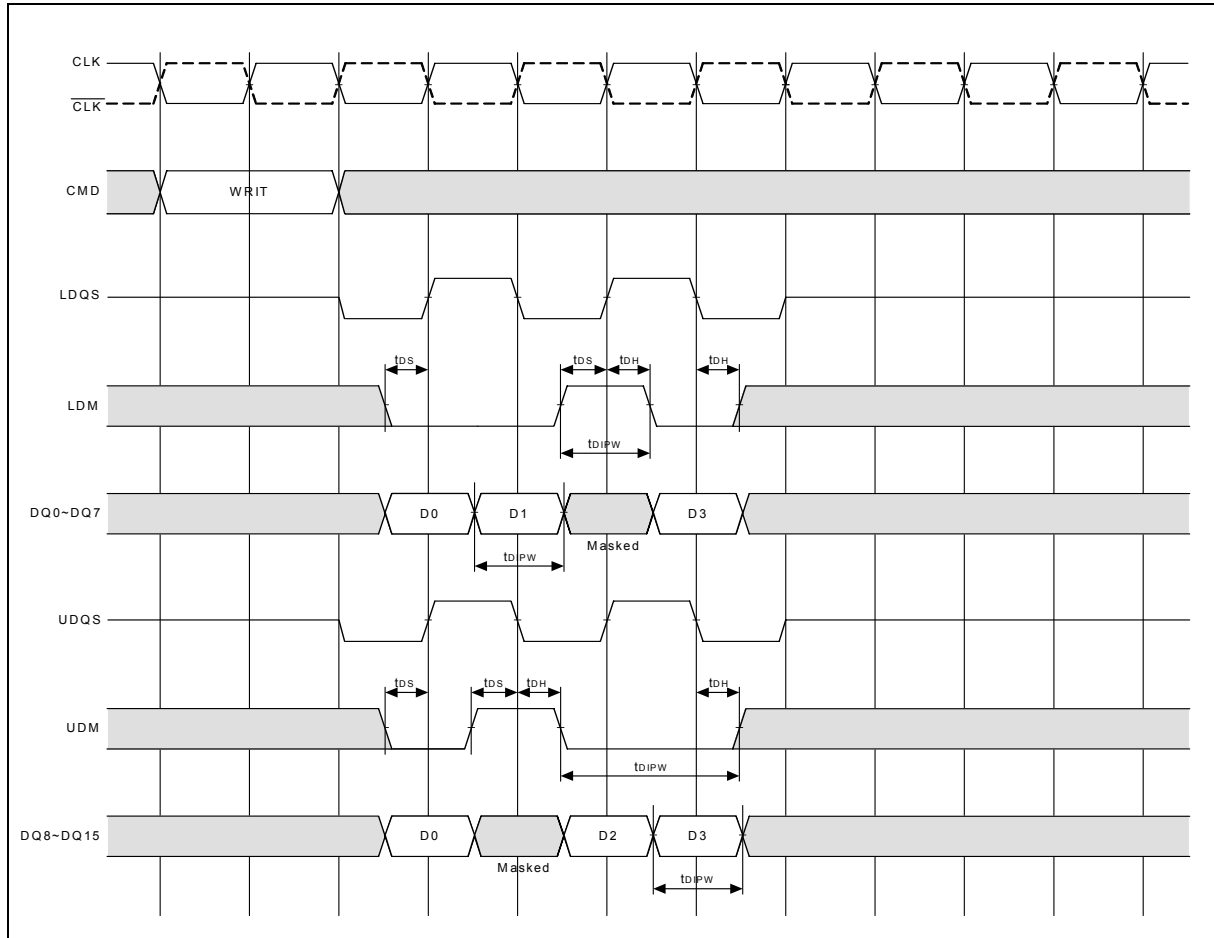
10.4 Write Timing (Burst Length = 4)



Note: x16 has two DQs (UDQS for upper byte and LDQS for lower byte). Even if one of the 2 bytes is not used, both UDQS and LDQS must be toggled.

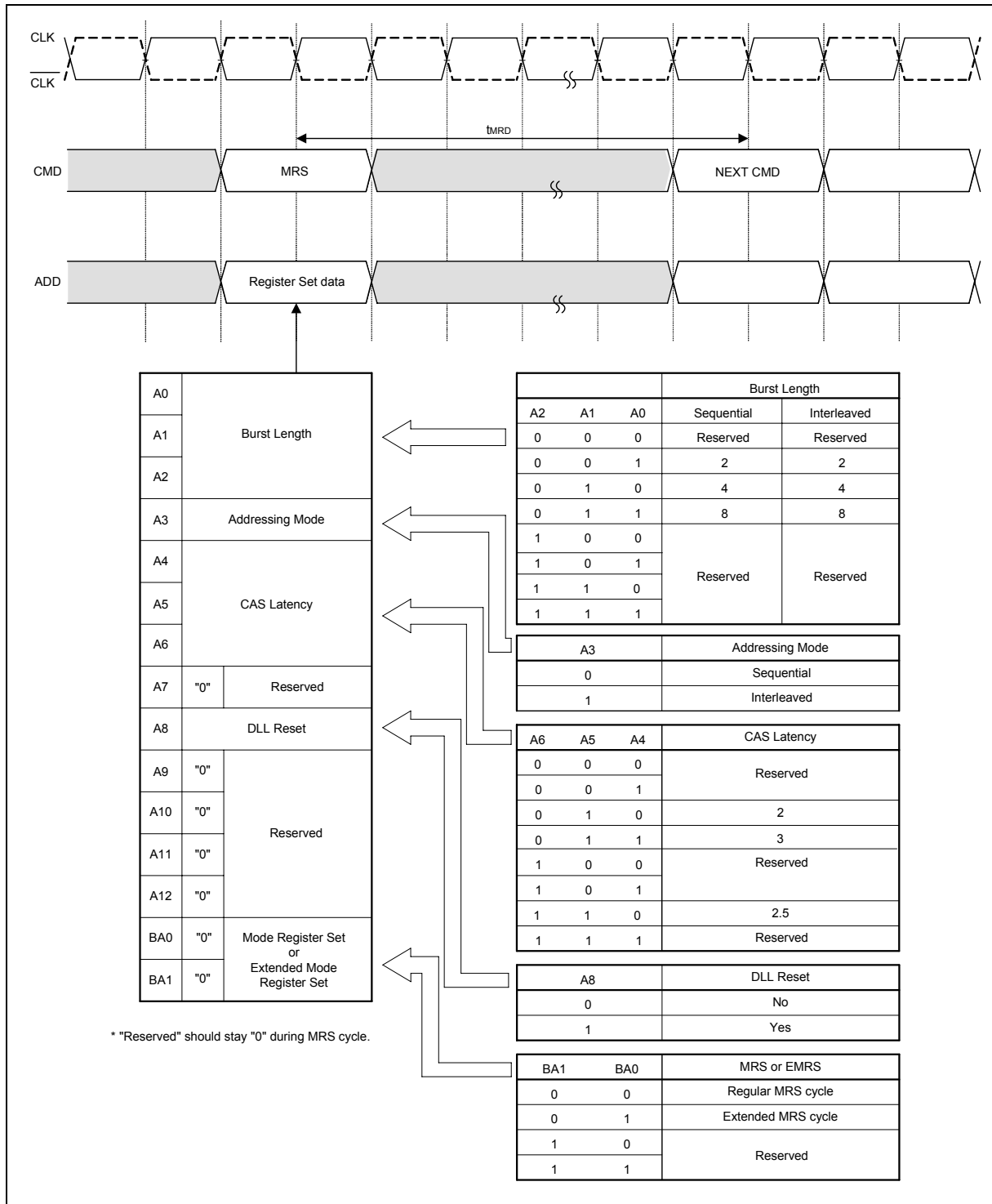


10.5 DM, DATA MASK (W9425G6EH)



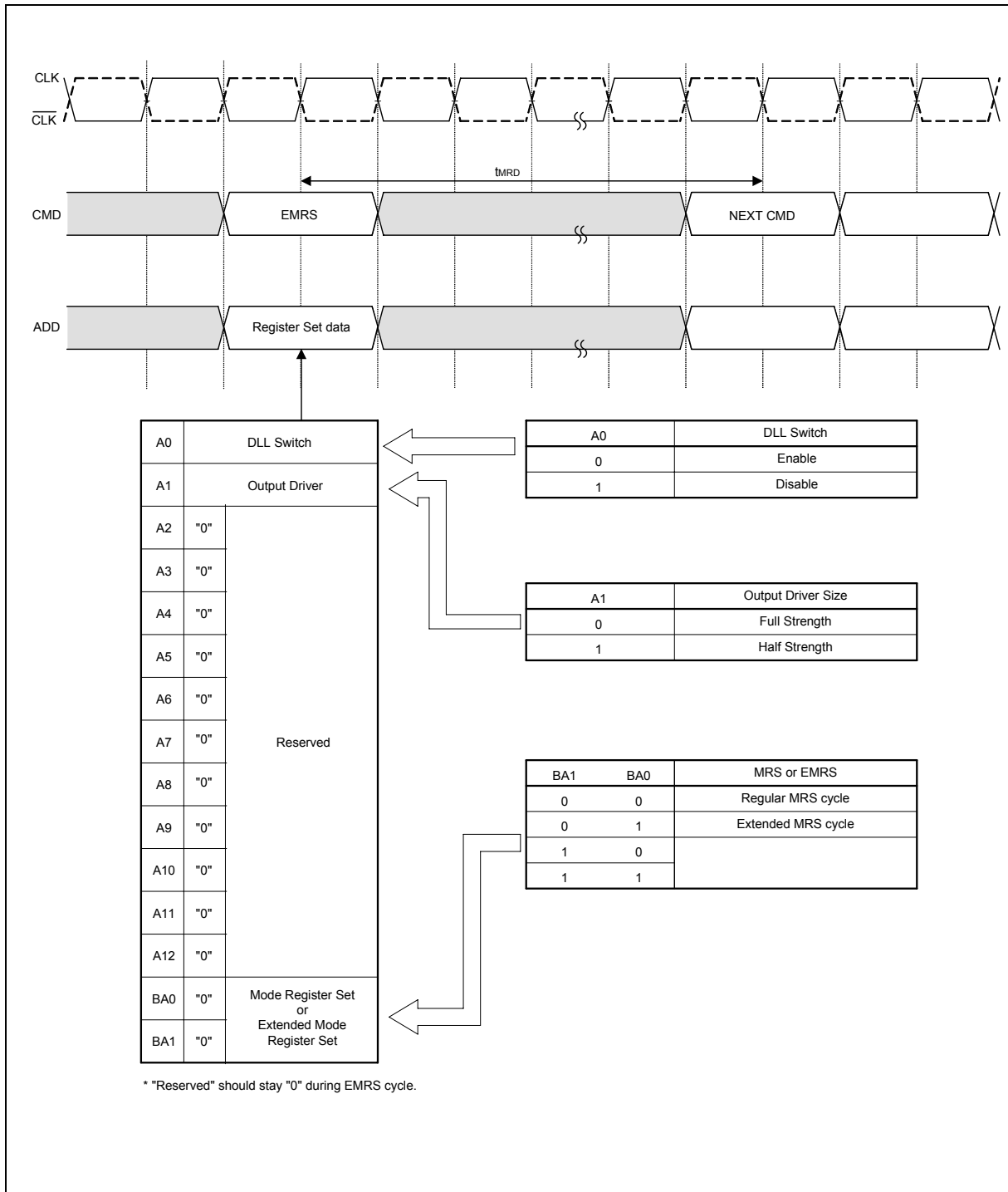


10.6 Mode Register Set (MRS) Timing





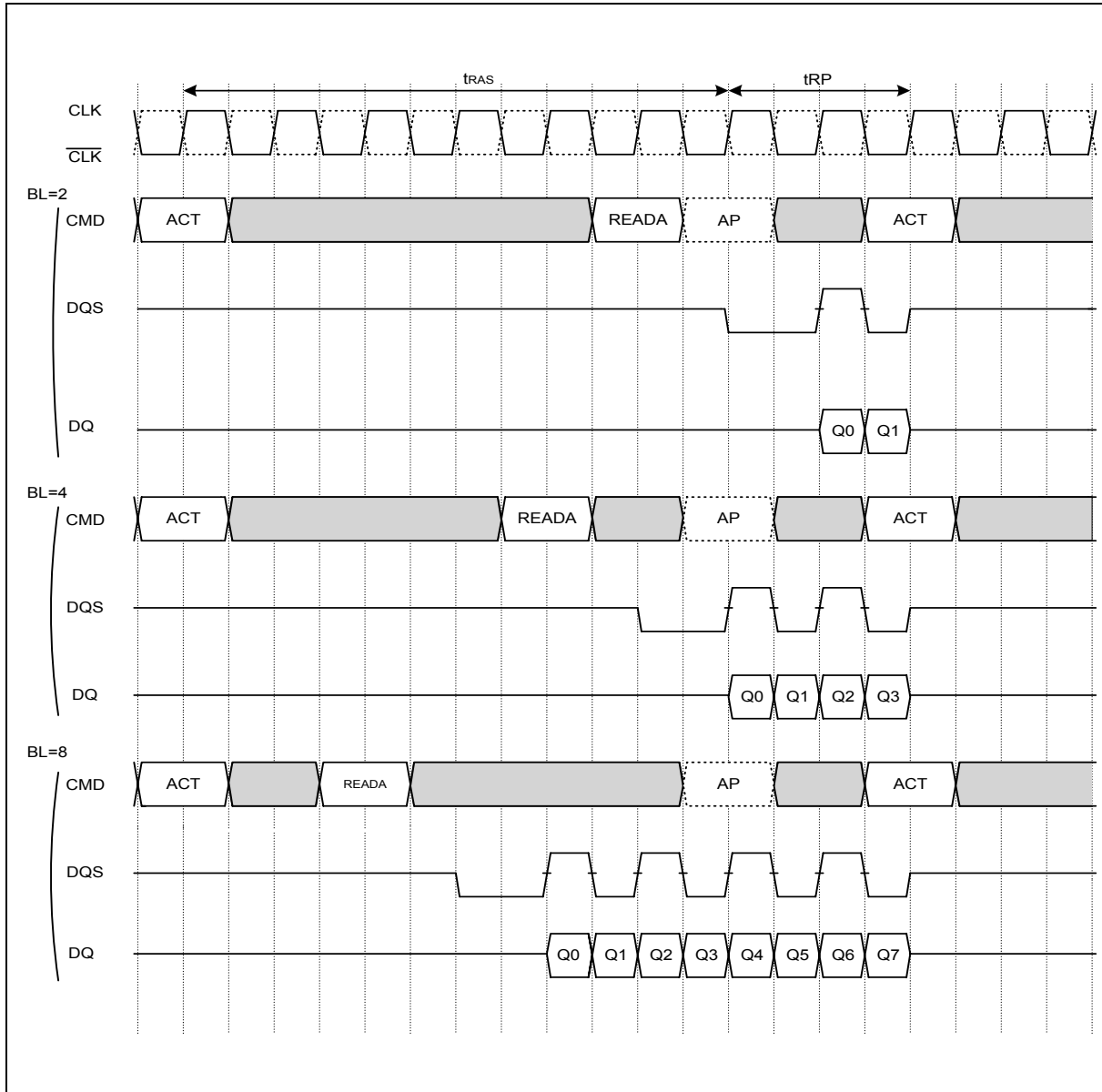
10.7 Extend Mode Register Set (EMRS) Timing






10.8 Auto-precharge Timing (Read Cycle, CL = 2)

1) $t_{RCD} (READA) \geq t_{RAS} (MIN) - (BL/2) \times t_{CK}$



Notes: CL=2 shown; same command operation timing with CL = 2,5 and CL=3

In this case, the internal precharge operation begin after BL/2 cycle from READA command.

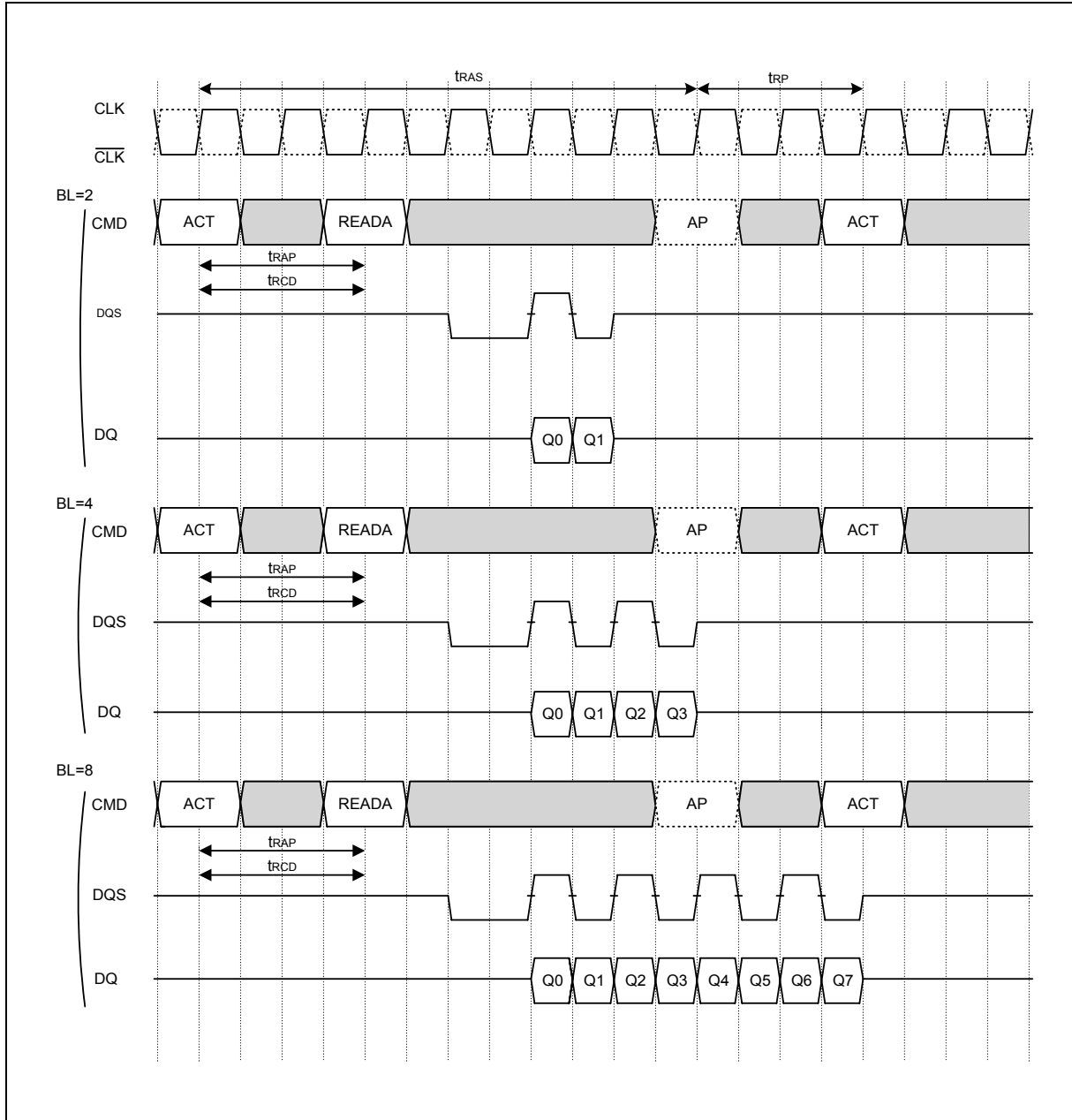
 Represents the start of internal precharging.

The Read with Auto-precharge command cannot be interrupted by any other command.



10.9 Auto-precharge Timing (Read cycle, CL = 2), continued

$$2) \text{trCD}/\text{RAP}(\text{min}) \leq \text{trCD} (\text{READA}) < \text{tRAS} (\text{min}) - (\text{BL}/2) \times \text{tCK}$$



Notes: CL2 shown; same command operation timing with CL = 2.5, CL=3.

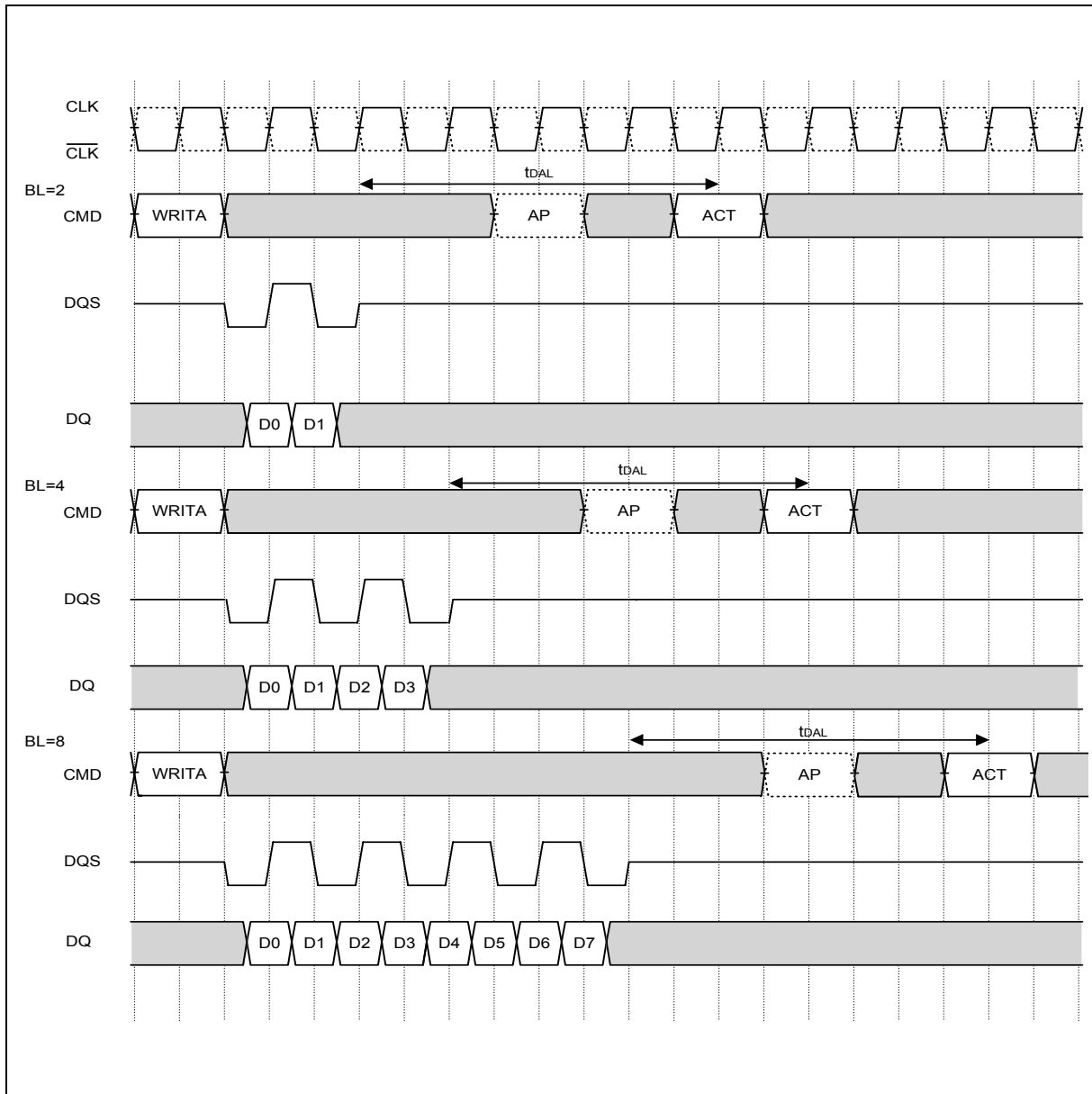
In this case, the internal precharge operation does not begin until after tRAS (min) has command.

AP Represents the start of internal precharging.

The Read with Auto-precharge command cannot be interrupted by any other command.



10.10 Auto-precharge Timing (Write Cycle)

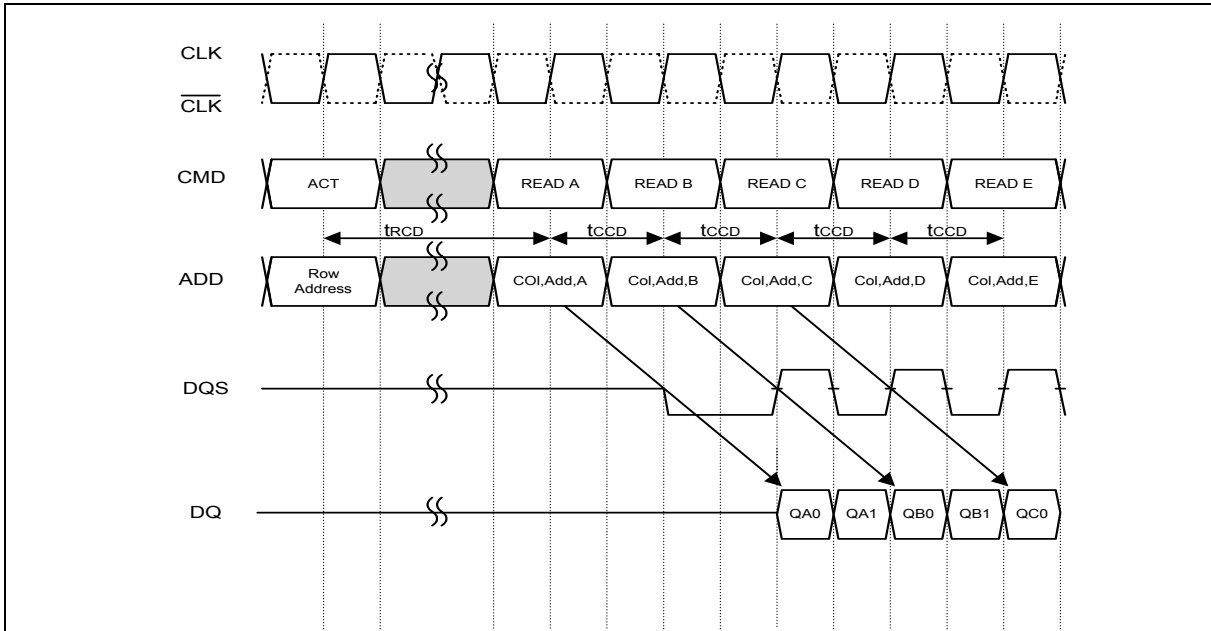


The Write with Auto-precharge command cannot be interrupted by any other command.

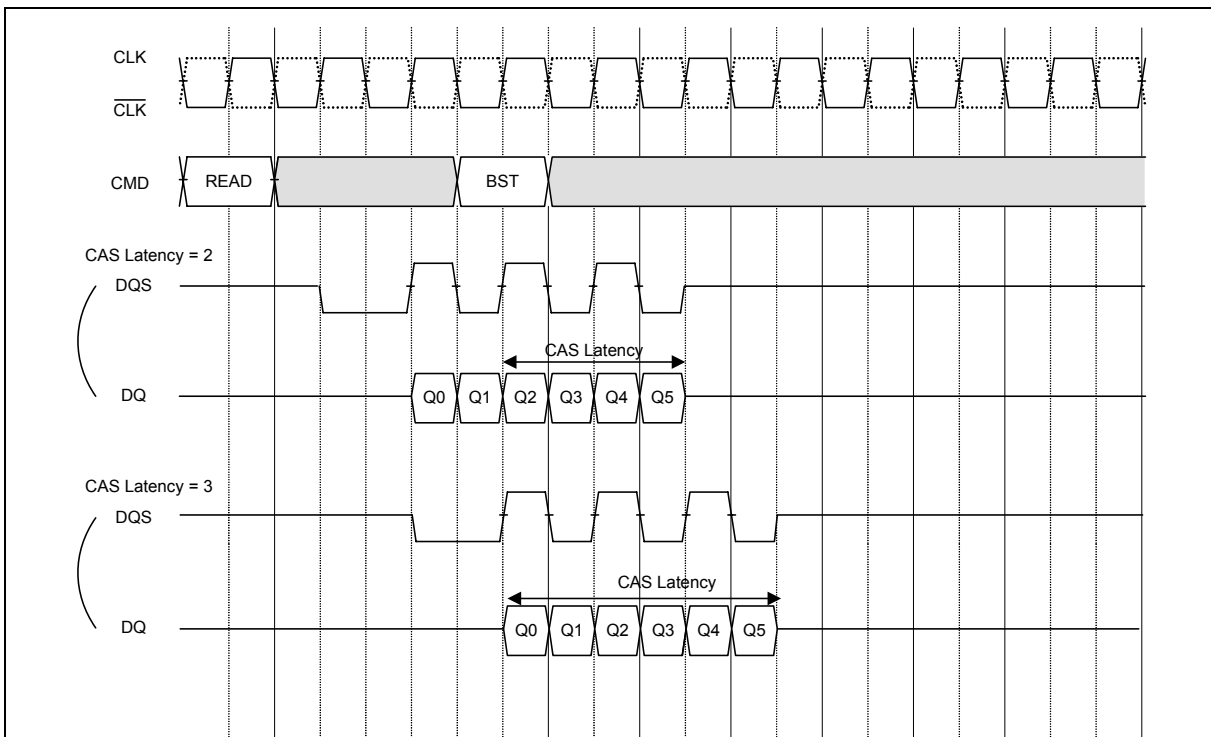
AP Represents the start of internal precharging .



10.11 Read Interrupted by Read (CL = 2, BL = 2, 4, 8)

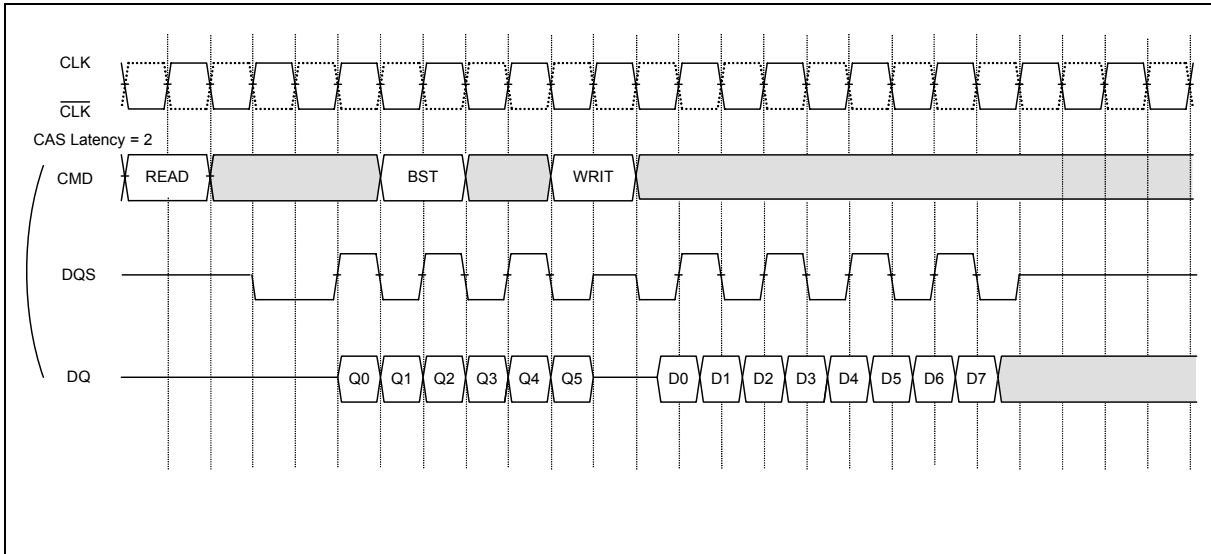


10.12 Burst Read Stop (BL = 8)



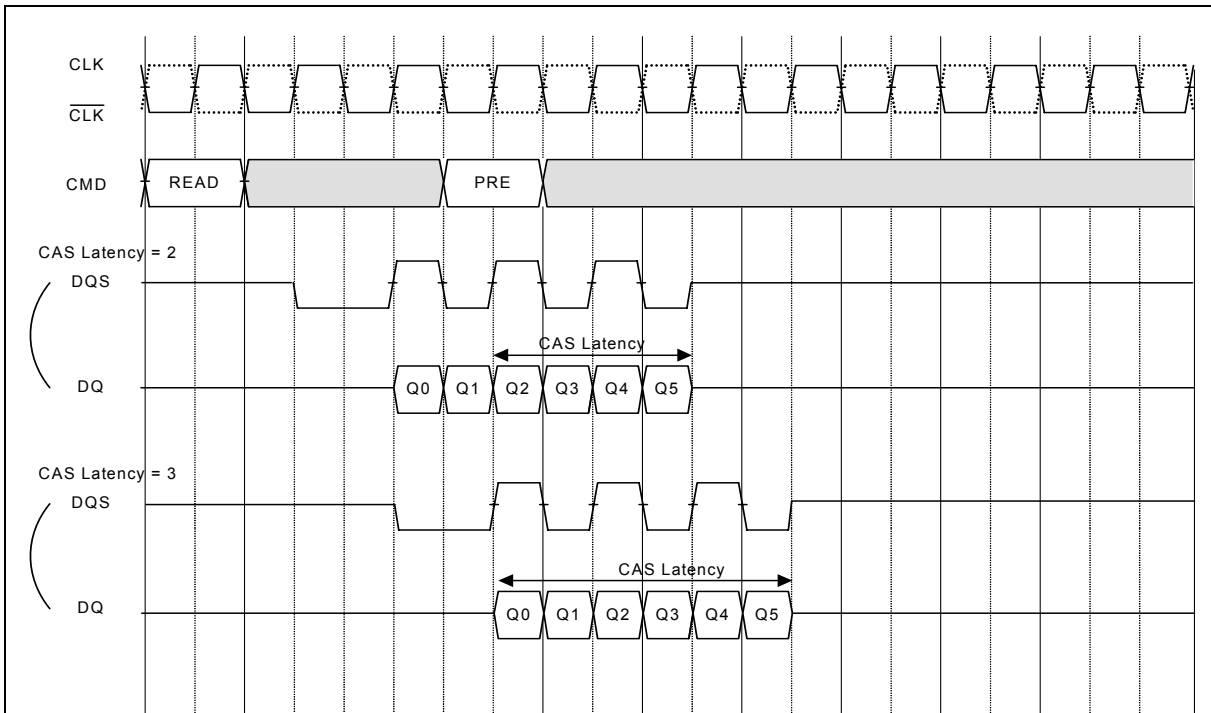


10.13 Read Interrupted by Write & BST (BL = 8)



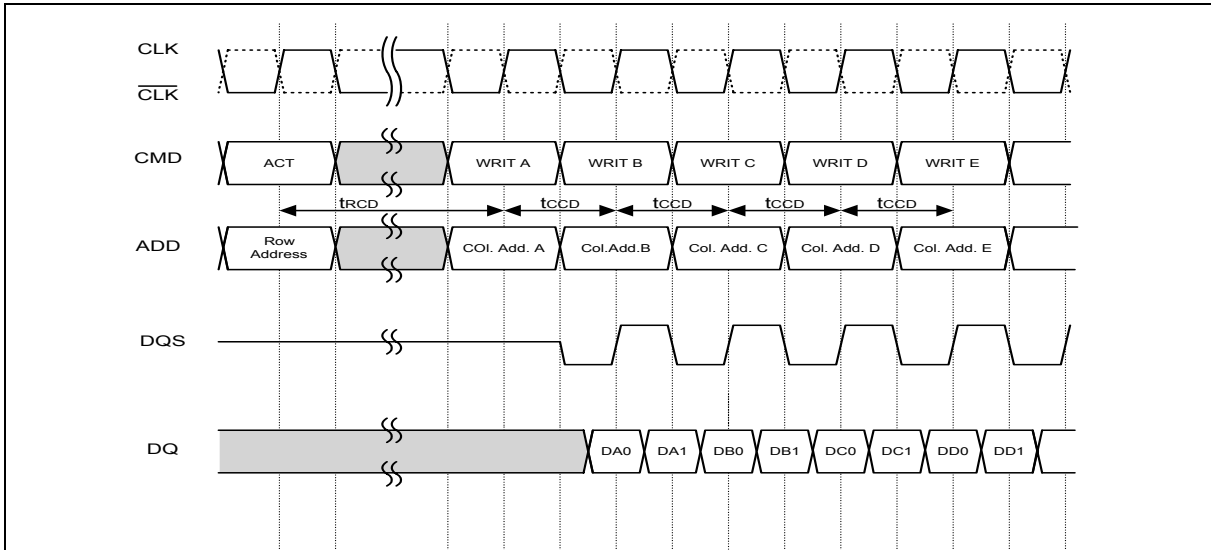
Burst Read cycle must be terminated by BST Command to avoid I/O conflict.

10.14 Read Interrupted by Precharge (BL = 8)

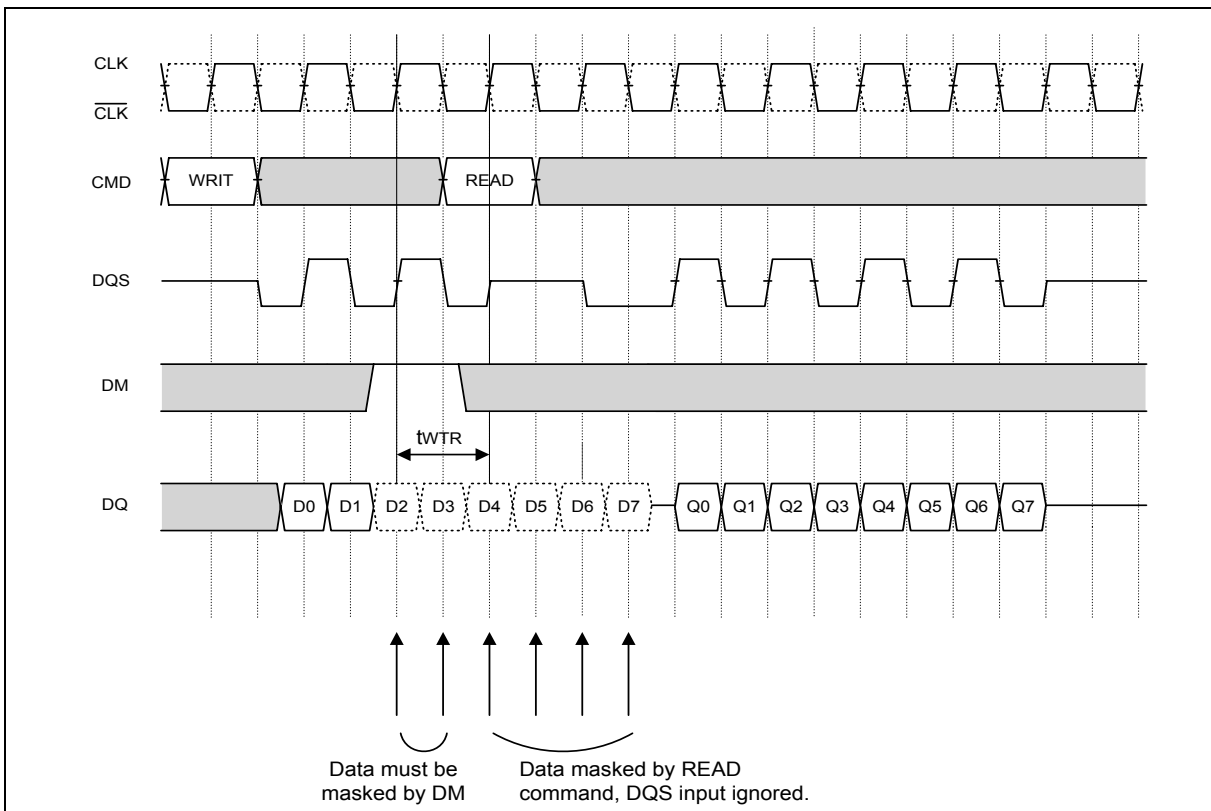




10.15 Write Interrupted by Write (BL = 2, 4, 8)

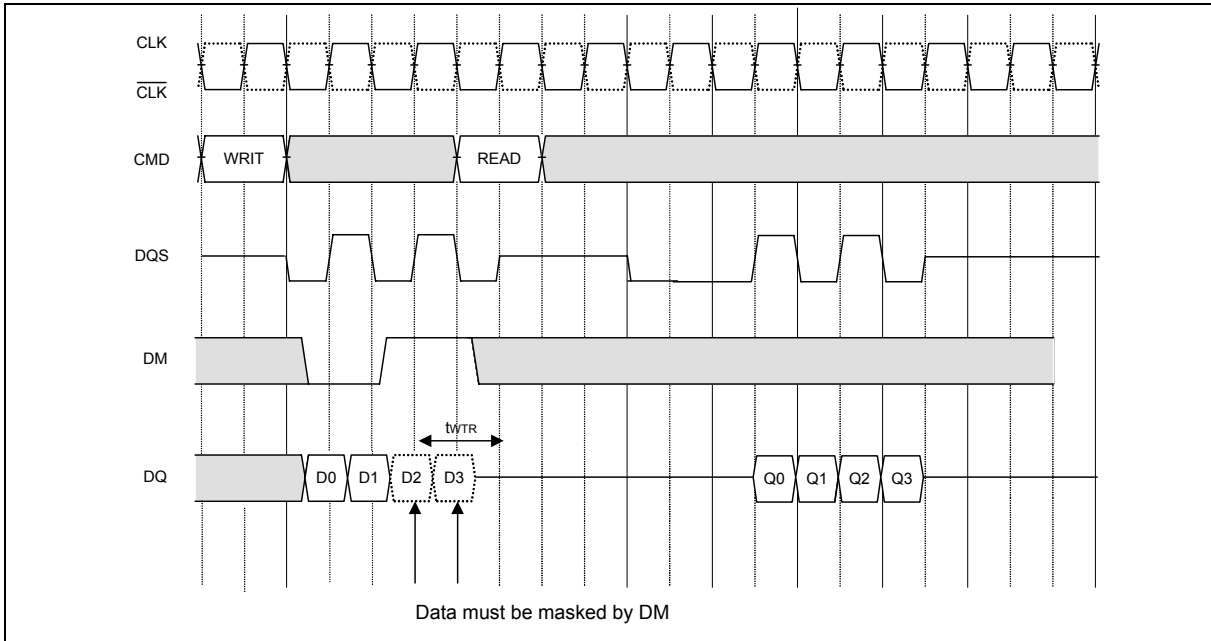


10.16 Write Interrupted by Read (CL = 2, BL = 8)

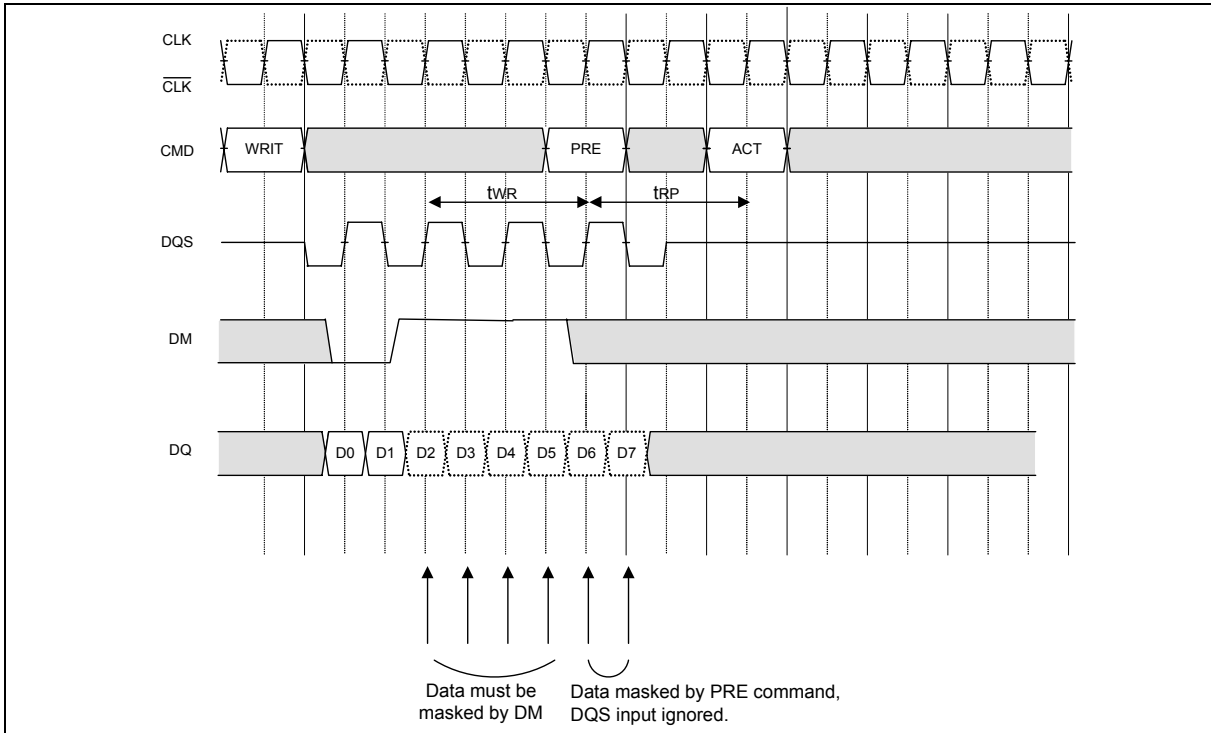




10.17 Write Interrupted by Read (CL = 3, BL = 4)



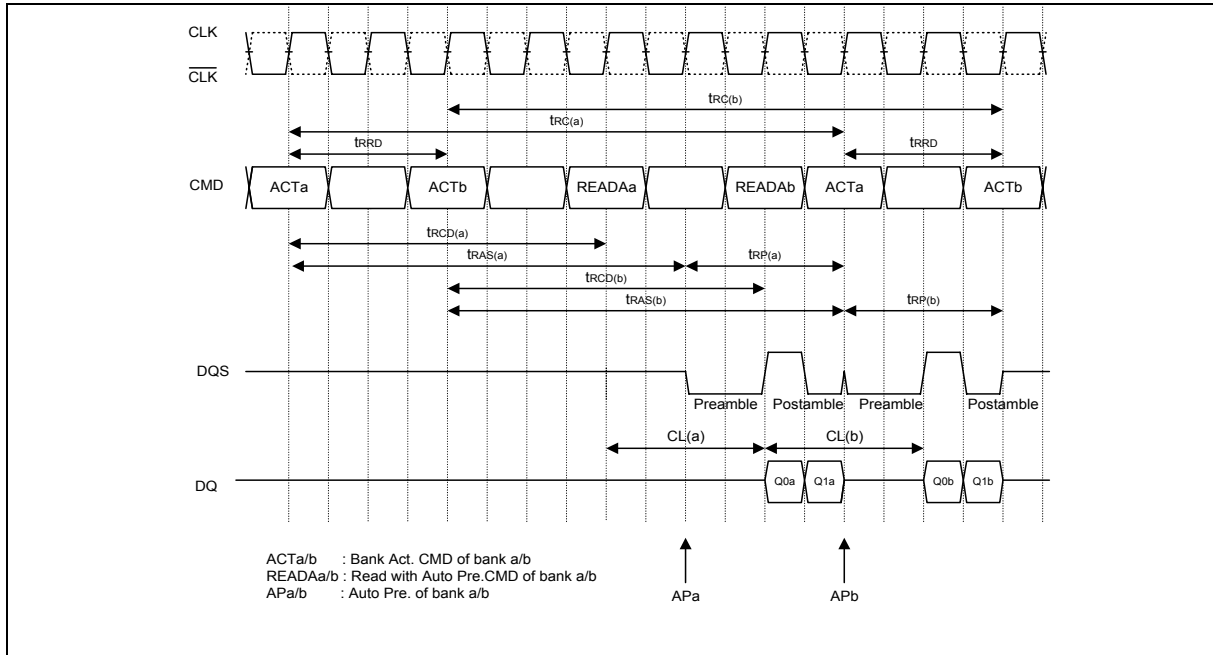
10.18 Write Interrupted by Precharge (BL = 8)



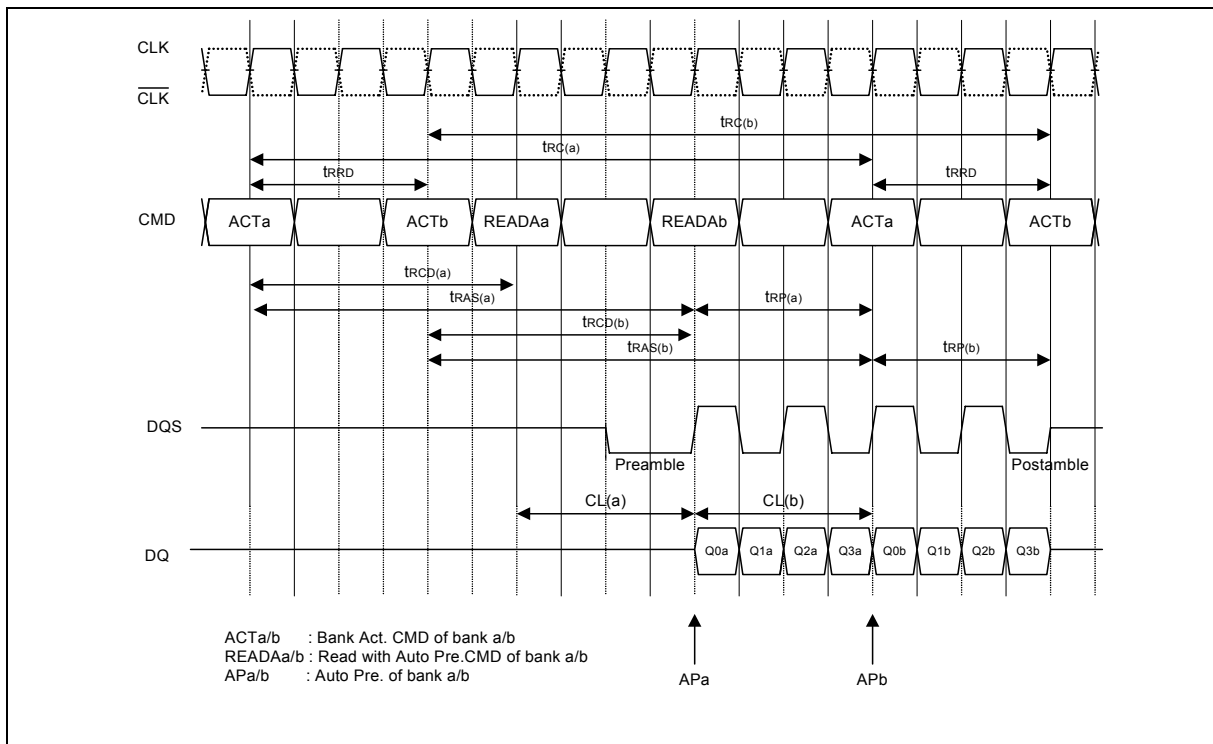


10.19 2 Bank Interleave Read Operation (CL = 2, BL = 2)

* t_{CK} = 100 MHz

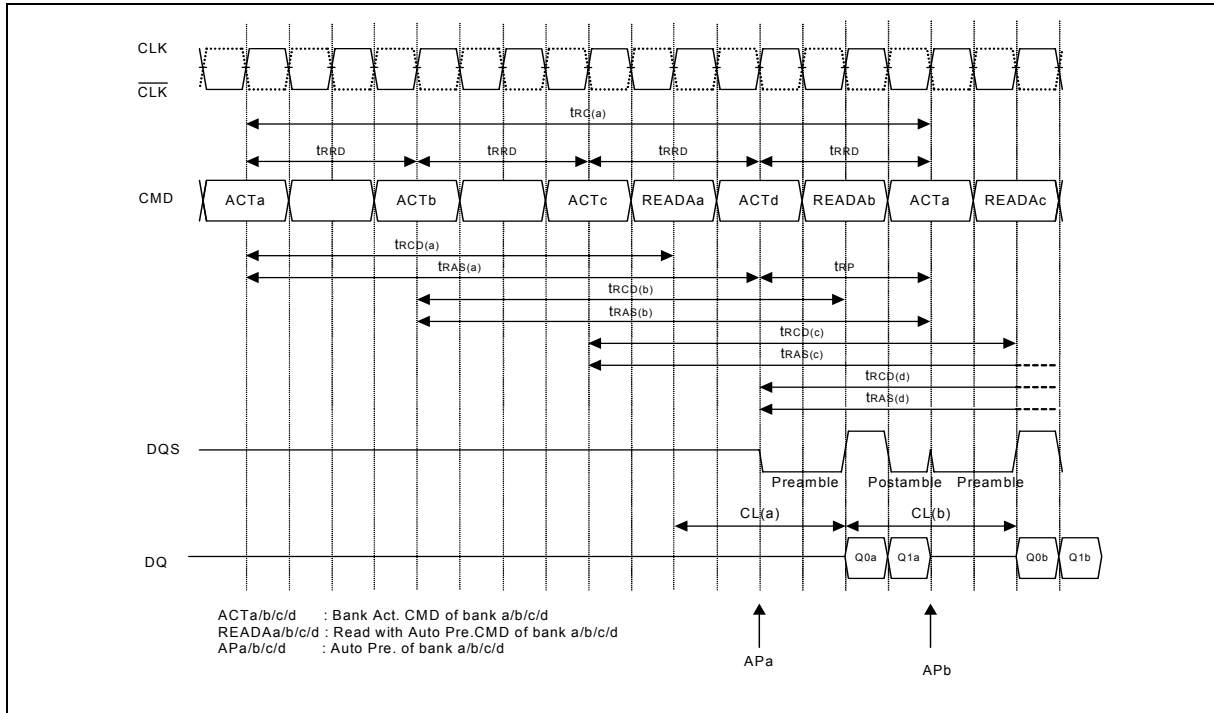


10.20 2 Bank Interleave Read Operation (CL = 2, BL = 4)

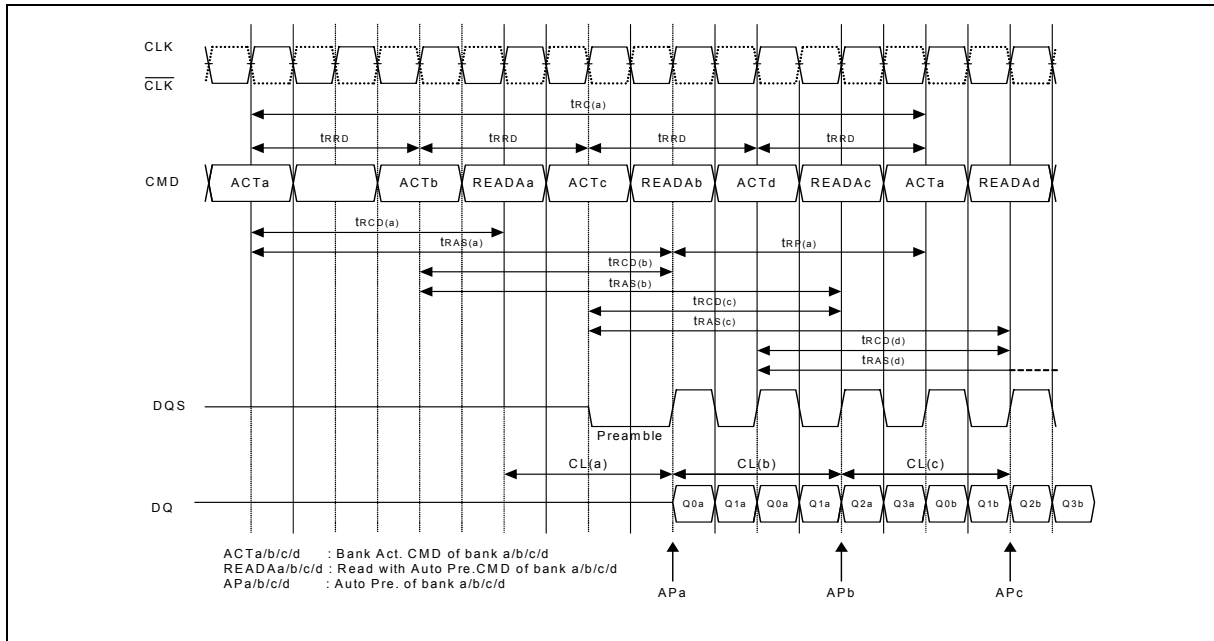




10.21 4 Bank Interleave Read Operation (CL = 2, BL = 2)

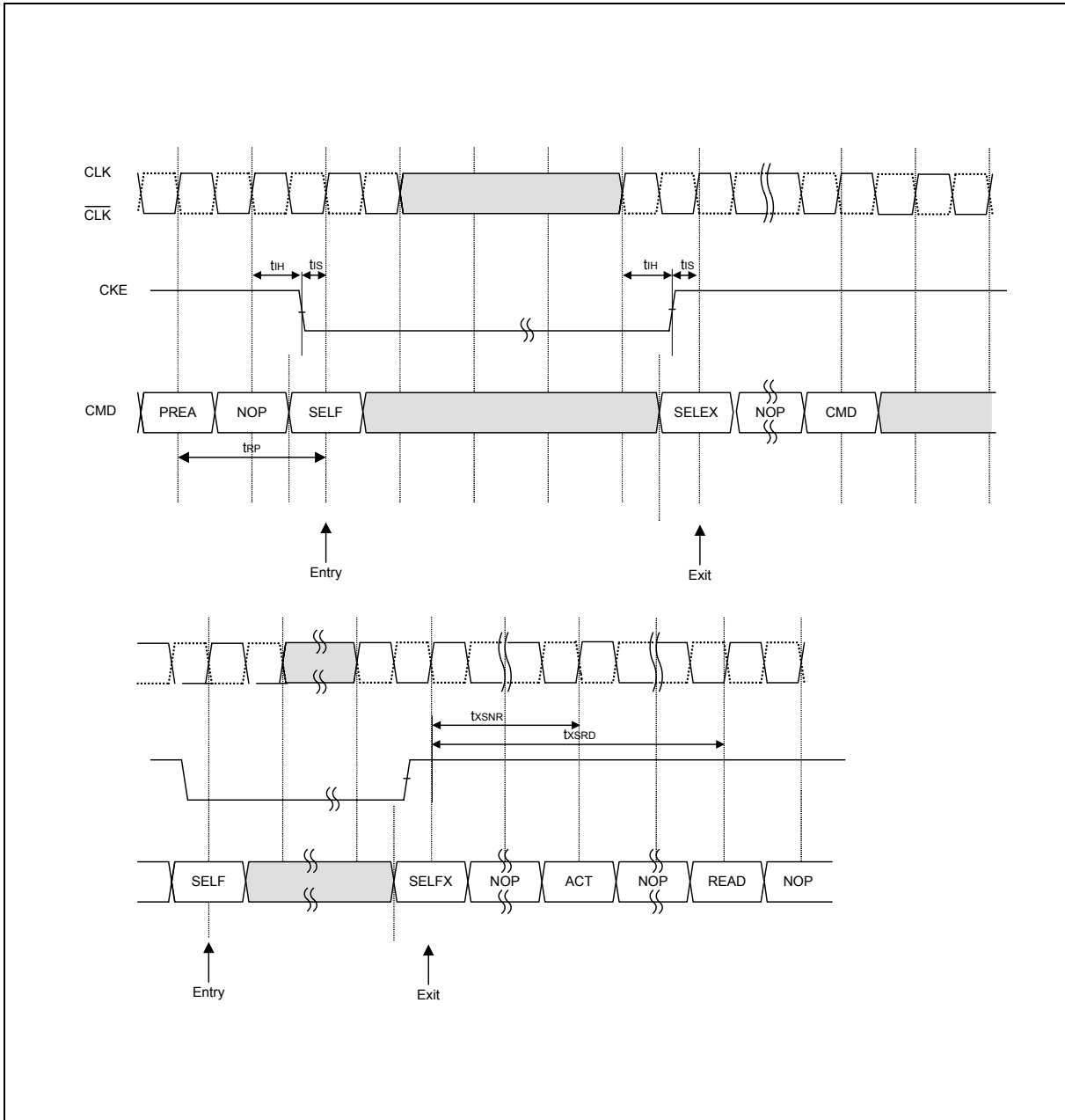


10.22 4 Bank Interleave Read Operation (CL = 2, BL = 4)





10.26 Self Refresh Entry and Exit Timing

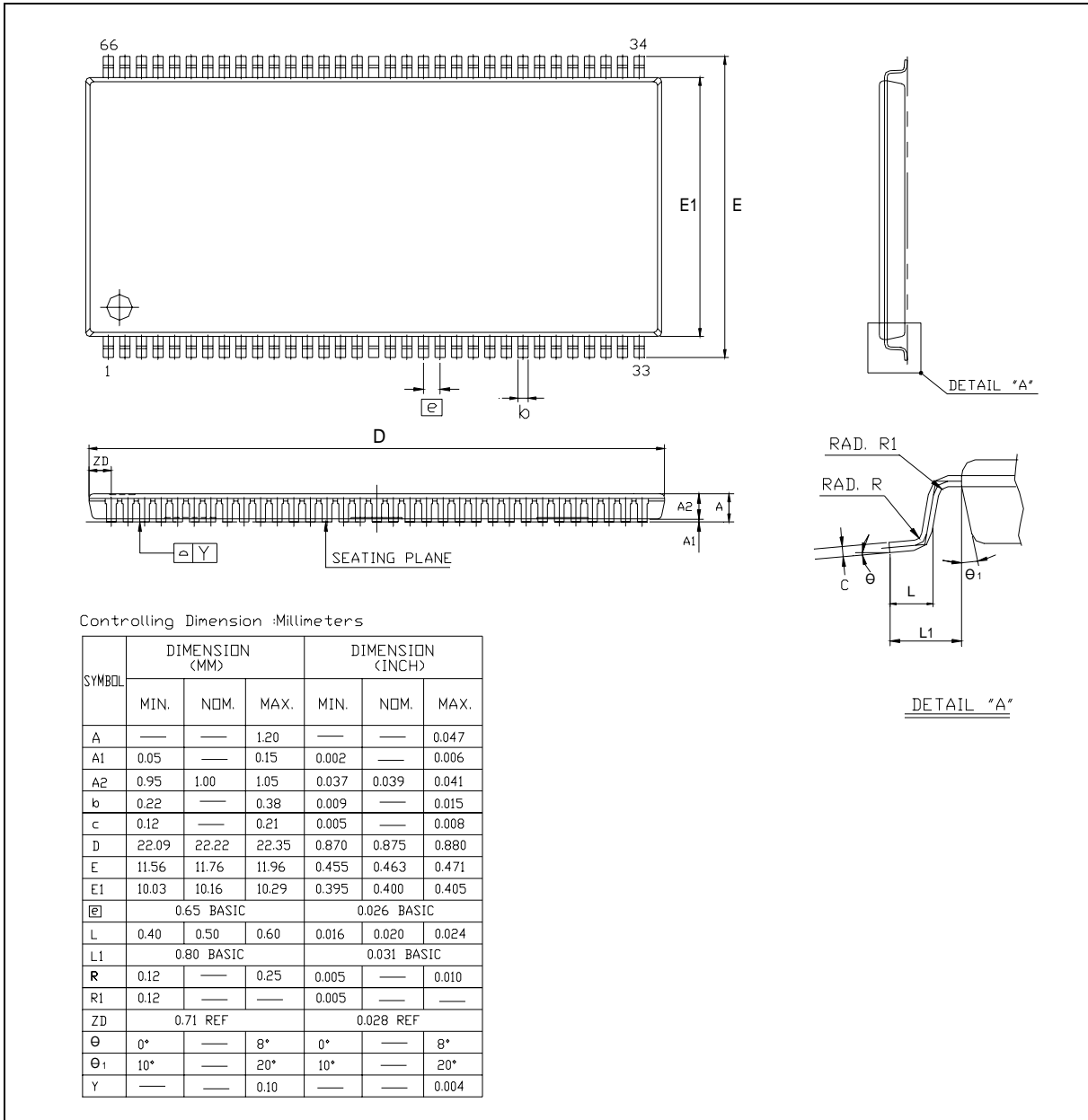


Note: If the clock frequency is changed during self refresh mode, a DLL reset is required upon exit.



11. PACKAGE SPECIFICATION

11.1 TSOP 66 II – 400 mil





12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	Dec. 12, 2007	All	Formally data sheet
A02	Jan. 04, 2008	5, 25	Revise -4 speed grade Max.IDD4R/IDD4W value from 190mA to 210mA
A03	Feb. 21, 2008	5, 26	Revise -5 speed grade Max. CLK cycle time tck value from 10nS to 12nS
		23	Change VDDQ max from VDD to 2.7V
A04	Apr. 11, 2008	5, 25	Modify -4 speed grade DC Characteristics IDD6 parameter value from 5mA to 3mA
		9	Add figure to illustrate Initialization sequence after power-up
		23	Revise overshoot/undershoot pulse width Before VIH (max.) = -1.2V with a pulse width ≤ 3 nS After VIH (max.) = -1.5V with a pulse width ≤ 5 nS Before VIL (min.) = VDDQ +1.2V with a pulse width ≤ 3 nS After VIL (min.) = VDDQ +1.5V with a pulse width ≤ 5 nS
		26, 27, 29	Revise input setup/hold time tIS/tIH parameters with skew rate dependency of AC characteristics table

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.

Publication Release Date: Apr. 11, 2008
Revision A04