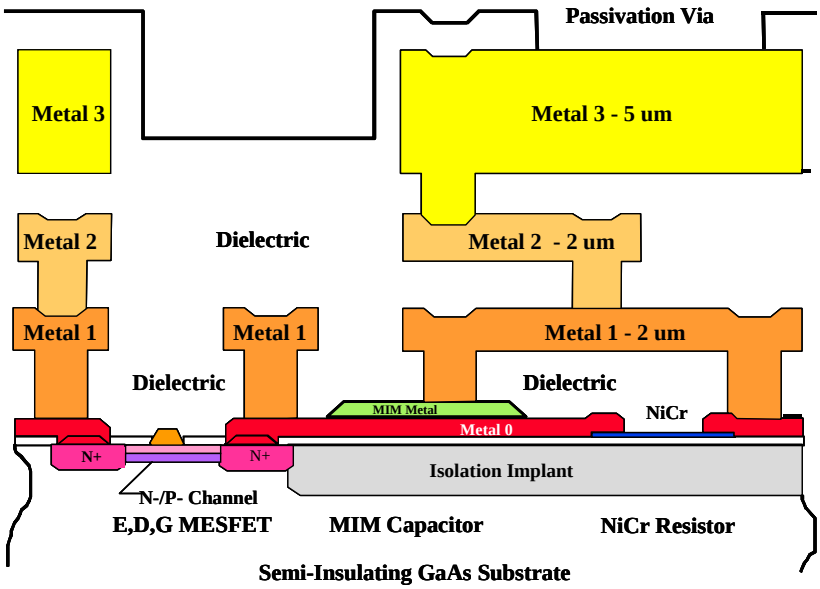
TQTRp

Advanced Passives & MESFET Foundry Service



TQTRp Process Cross-Section

General Description

TriQuint's TQTRp process has advanced metal systems and MESFET devices. It is targeted at high performance, small size passive-only or passive/active circuits and utilizes over 9 µm of gold metal. High density interconnections are accomplished with three thick global and one surface metal interconnect layers. The four metal layers are encapsulated in a high performance dielectric that allows wiring flexibility and plastic packaging simplicity. Precision NiCr resistors, implanted resistors, and high value MIM capacitors are included. Advanced 0.6 µm enhancement/depletion mode MESFET devices include an integrated power MESFET, general purpose D-Mode MESFET, and Enhancement Mode MESFET and are based on the TQTRx process, currently TriQuint's highest volume process. The TQTRp process is available on 150-mm (6 inch) wafers.

Features

- High Density Interconnects:
  - 3 Global
  - 1 Local
  - 9 µm Total Thickness
- High-Q Passives; >50 @ 2 GHz
- 0.6 µm Gate Length MESFET Optional: Power & General Purpose D-FETs; E-FET
- Schottky-Barrier Diodes
- Bulk & Thin Film Resistors
- High Value Capacitors
- Dielectric Encapsulated Metals
- Planarized Surface; simplified plastic packaging
- Substrate Vias Available
- Volume Production Processes
- Low Cost Passives-Only Option

Applications

- Active and/or Passive Components
- Circuits Requiring High Q Passive Elements
- Ideal for Mixers, Converters, and Phase-Shifters with Baluns, Transformers, E-M Structures
- Mobile Phone Front End Blocks
- RF Module Front-Ends

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TQTRp Process Details

Element	Parameter	Value	Units
Interconnects	Metal Layers	Four: 0.5,2,2,5	um
MIM Caps	Values	1200	pF/mm2
Resistors	NiCr	50	Ohms/sq
	Bulk	700	Ohms/sq
Gate Length	(All FETs)	0.6	um
N+ Diode	Vforward	0.55	V
E-FET;	Threshold Voltage	+0.15	Vth—V
	Imax	90	mA/mm
	Ft @ Idss	18	GHz
	Gm	225	mS/mm
	Breakdown, Vgd	22	V
	Fmin, 6 GHz	0.90	dB
D-FET	Pinchoff Voltage	-0.6	Vp—V
	Idss	70	mA/mm
	Gm	200	mS/mm
	Breakdown, Vgd	18.5	V
	Fmin, 6 GHz	0.54	dB
G-FET	Pinchoff Voltage	-2.2	Vp—V
	Idss	270	mA/mm
	Imax	365	mA/mm
	Gm	170	mS/mm
	Breakdown, Vgd	19	V
Vias		Yes	
Mask Layers	No Vias	18	
	With Vias	20	

Maximum Ratings

FET Operating Channel Temp		-55 to +150	°C
Capacitor Breakdown Voltage	- Design	10	V
	- Typical	20	V

Specifications Subject to Change

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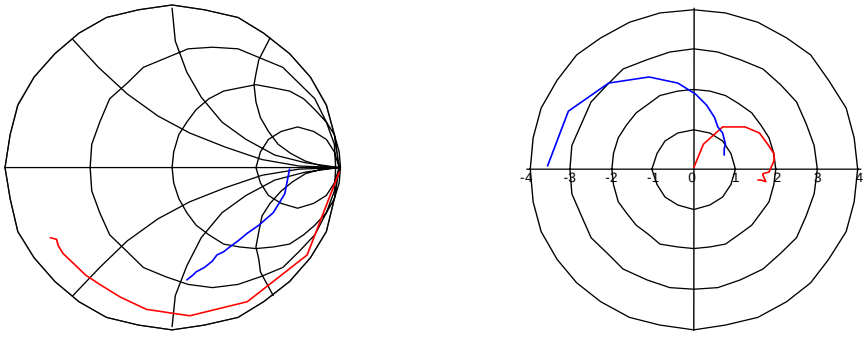
GFET
300 um
Vds=3V
50% Idss

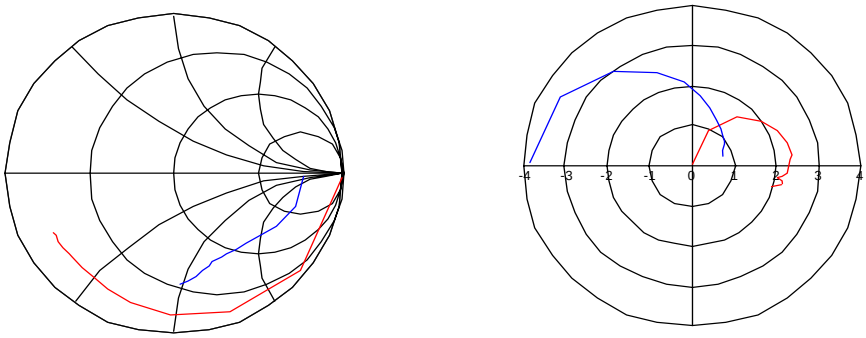


S11
S22

Freq (0.1GHz to 26.1GHz)

S12 / .05
S21

DFET
300 um
Vds=3V
50% Idss

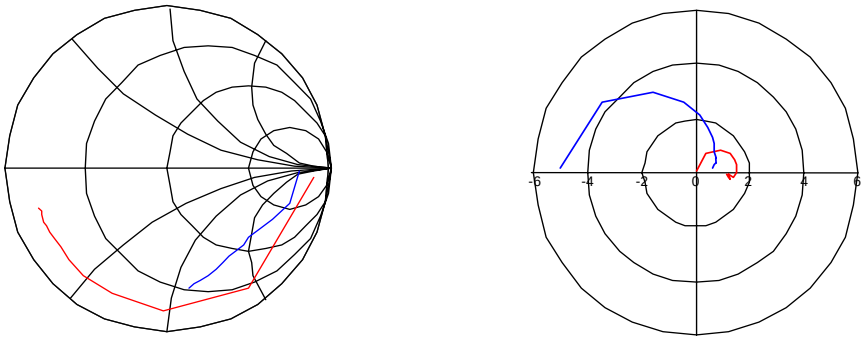


S11
S22

Freq (0.1GHz to 26.1GHz)

S12 / .05
S21

EFET
300 um
Vds=3V
50% Idmax



S11
S22

Freq (0.1GHz to 26.1GHz)

S12 / .05
S21

TQTRp

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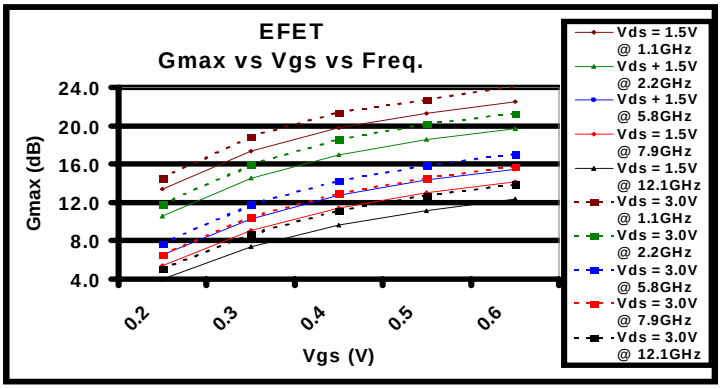
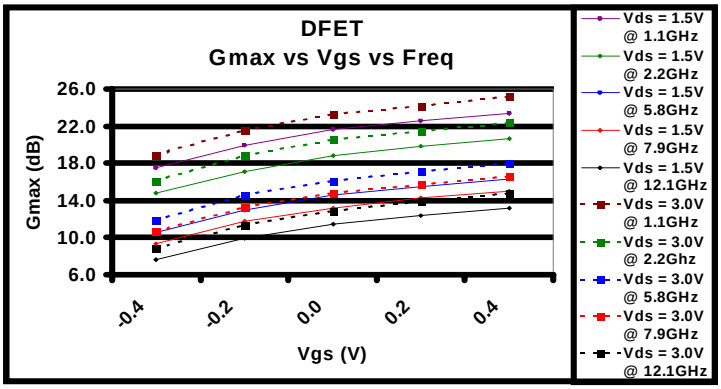
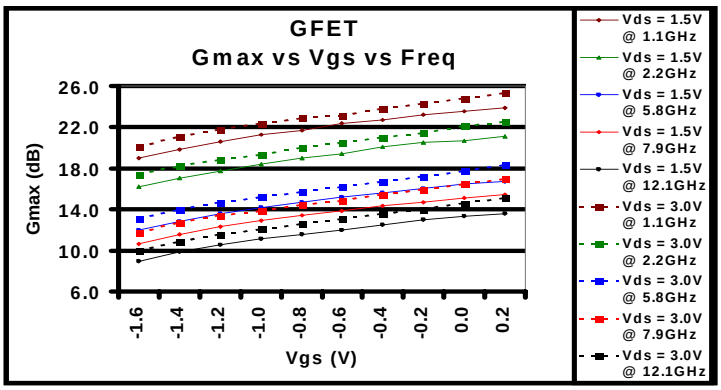
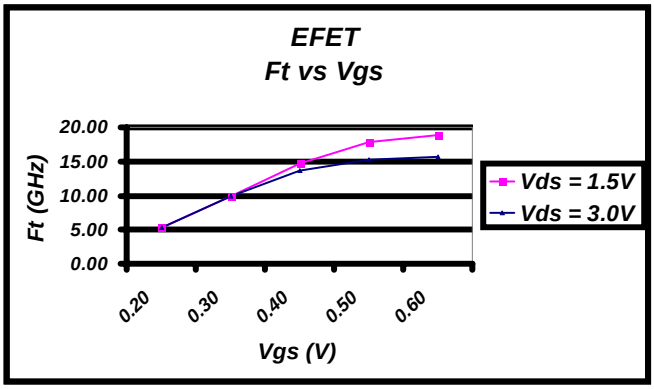
Gmax vs Vgs vs Frequency
300 um FETs; Three Types
Vds = 1.5 & 3.0 V; T=27°C

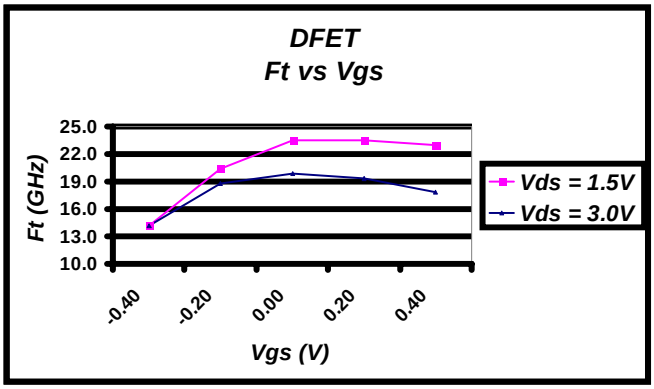


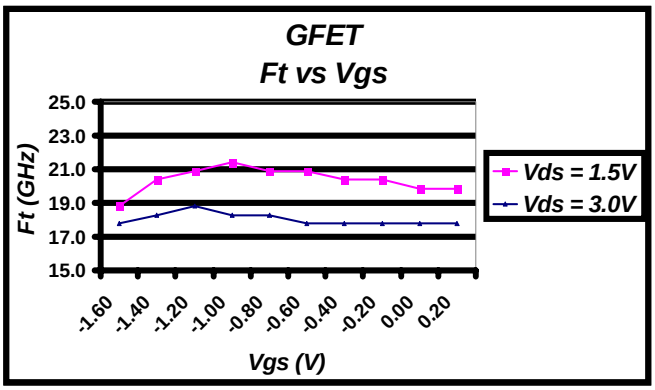




Ft versus Vgs;
300 um FETs; Three Types;
Vds = 1.5 & 3.0 V; T=27°C







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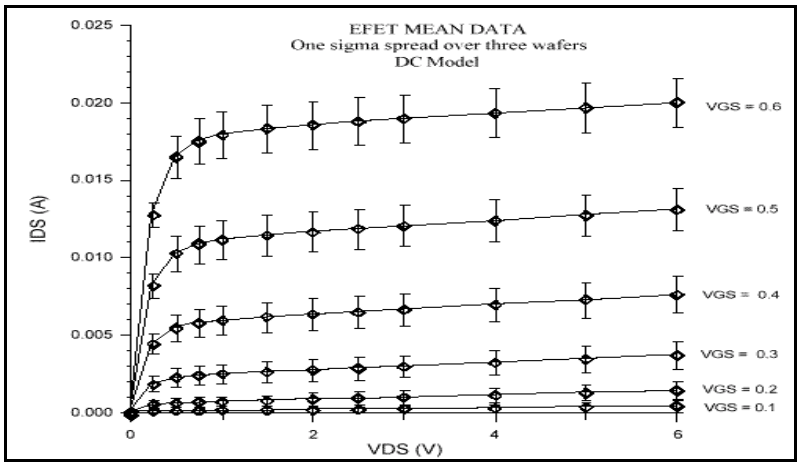
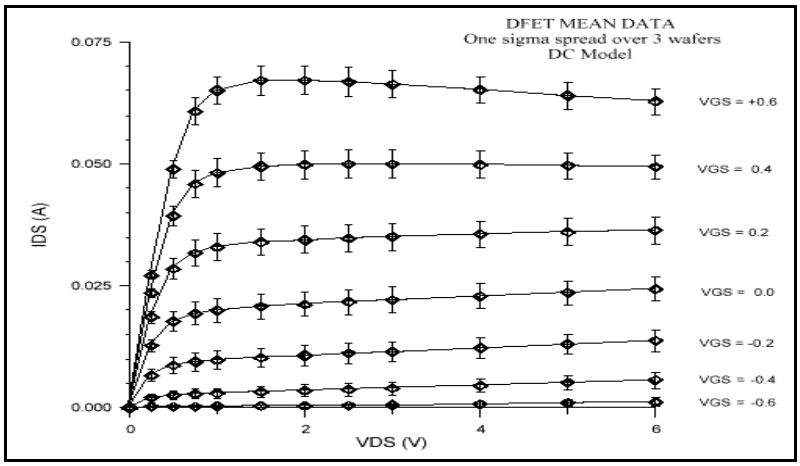
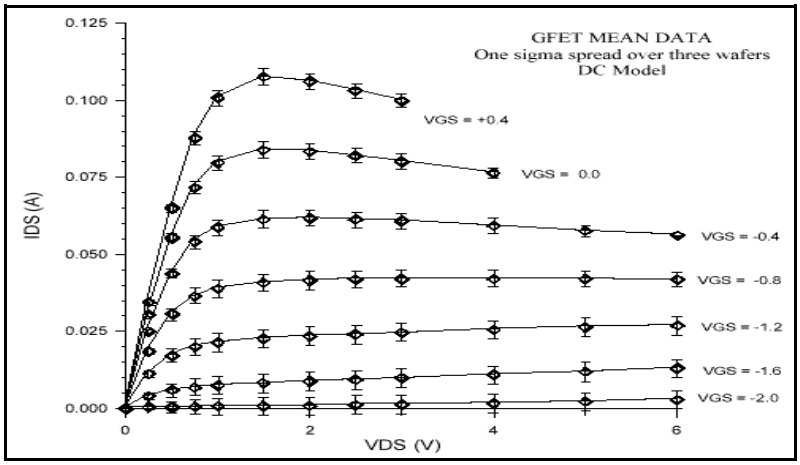
EFET
IV Curves
300 um



DFET
IV Curves
300 um



GFET
IV Curves
300 um



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Prototyping and Development

- Prototype Development Quickturn (PDQ):
  - Shared Mask Set;
  - Run Monthly;
  - Hot Lot Cycle;
  - Via and Non-Via Options.
- Prototype Wafer Option (PWO):
  - Customer-specific Masks, Customer Schedule
  - 2 wafers delivered
  - Hot Lot Cycle Time
  - With thinning and sawing; optional backside vias
- Design Sensitivity Test (DST) Wafer Run
  - Yield Analysis
  - Design Sensitivity to Process Variation
  - 14 Wafer Start; Spread of Vp Values

Design Tool Status

- Design Manual Available Now
- Device Library of Circuit Elements: FETs, Diodes, Thin Film and Implanted Resistors, Capacitors, Inductors
- Parameters for "TriQuint's Own Model" (TOM)
- Agilent ADS Design Kit Available Now
- PSPICE Models Available Q2'02
- Cadence Layout Library Available Now
- Layout/Verification Kit for ICEditors in Q4'02

Training

- GaAs Design Classes:
  - Half Day Introduction; Upon Request
  - Four Day Technical Training; Fall & Spring at TriQuint Oregon facility
- For Training Schedules please visit: www.triquint.com/foundry

Process Qualification Status

- TQTRp is a fully released qualified process
- Reliability Reports
  - TQTRp Process Qualification
  - TQTRx Element Qualification Report (for FETs)
- For more information on Quality and Reliability, contact TriQuint or visit www.tqs.com/Manufacturing/QR/bdy_qr-pubs.htm.

Applications Support Services

- Tiling of GDSII Stream Files including PCM on 15 x 15 mm maximum Tile Size
- Design Rule Check Services
- Layout versus Schematic Check Services
- Engineering Services:
  - Packaging Development
  - On-Wafer Test Development
  - Packaged Parts
  - Thermal Analysis
  - Yield Enhancement
- Part Qualification Services
- Failure Analysis

Manufacturing Services

- Mask Making
- Production 150 mm Wafer Fab
- Wafer Thinning
- Wafer Sawing
- Substrate Vias
- DC Die Sort Testing
- RF On-Wafer Testing
- Plastic Packaging
- RF Packaged Part Testing

Please contact your local TriQuint Semiconductor Representative or Foundry Services Staff for additional information:
E-mail: sales@triquint.com Phone: (503) 615-9000 Fax: (503) 615-8905