1/3-Inch Megapixel CMOS Active-Pixel Digital Image Sensor

MT9M011

For the latest data sheet revision, please refer to Micron's Web site: www.micron.com/imaging

Features

- DigitalClarity ™ CMOS Imaging Technology
- High frame rate
- Superior low-light performance
- Low dark current
- Simple two-wire serial interface
- Auto black level calibration
- Operating Modes:
  Snapshot and flash control, high frame rate preview, electronic panning
- Programmable Controls:
  Gain, frame size/rate, exposure, left-right and top-bottom image reversal, window size, and panning

Applications

- Cellular phones
- PDAs
- Toys
- Other battery-powered products

General Description

The Micron® Imaging MT9M011 is an SXGA-format, 1/3-inch CMOS active-pixel digital image sensor with an active imaging pixel array of 1,280H x 1,024V. It incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface and has low power consumption.

The megapixel CMOS image sensor features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs an SXGA image at 13.9 frames per second (fps).

Table 1: Key Performance Parameters

Parameter		Typical Value
Optical Format		1/3-inch (5:4)
Active Imager Size		4.6mm(H) x 3.7mm(V), 5.9mm (diagonal)
Active Pixels		1,280H x 1,024V
Pixel Size		3.6µm x 3.6µm
Color Filter Array		RGB Bayer Pattern
Shutter Type		Electronic Rolling Shutter (ERS)
Maximum Data Rate/ Master Clock		25 MPS/25 MHz
Frame Rate	SXGA (1280 x 1024)	Programmable up to 15 fps
	VGA (640 x 480)	Programmable up to 60 fps
	CIF (352 x 288)	Programmable up to 150 fps
ADC Resolution		10-bit, on-chip
Responsivity		1.0 V/lux-sec (550nm)
Dynamic Range		>71dB
SNR_{MAX}		44dB
Supply Voltage	I/O Digital	1.7V–3.6V
	Core Digital	2.5V–3.1V (2.8V nominal)
	Analog	2.5V–3.1V (2.8V nominal)
Power Consumption		129mW (full resolution mode)
		70mW (preview mode)
Operating Temperature		-30°C to +70°C

An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data. A flash output signal is also available to synchronize external light sources with sensor exposure time.

Table of Contents

List of Figures

List of Tables

Figure 1: Block Diagram

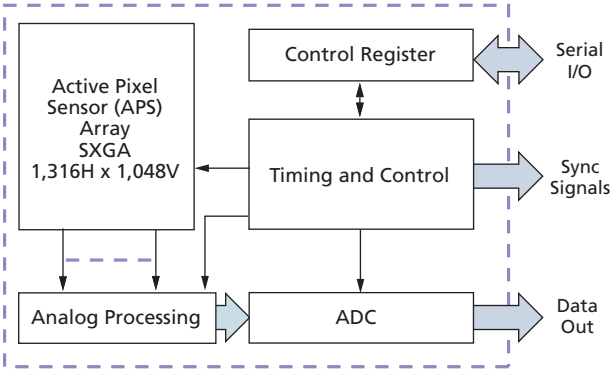
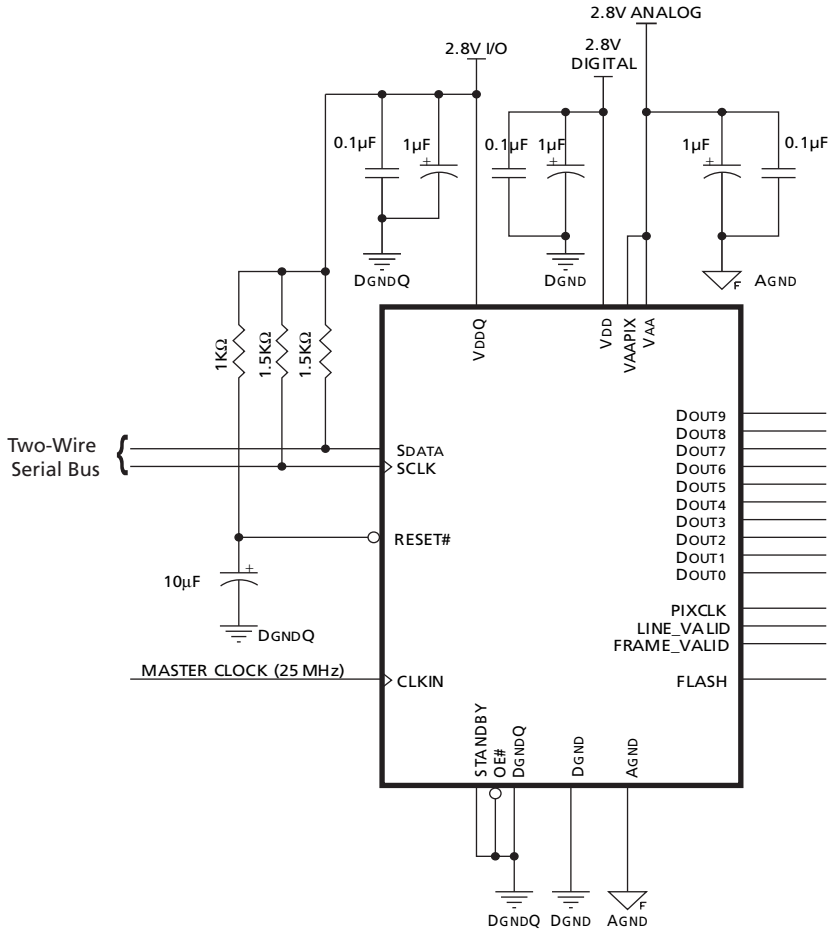


Figure 2: Typical Configuration (Connection)



Notes: 1. Resistor value 1.5KΩ is recommended, but may be greater for slower two-wire speed.
2. VDD and VAA supplies must be at same potential to avoid excess current draw. Care must be taken to avoid noise injection in the analog supply is cases where a single supply is used.

Table 2: Signal Description

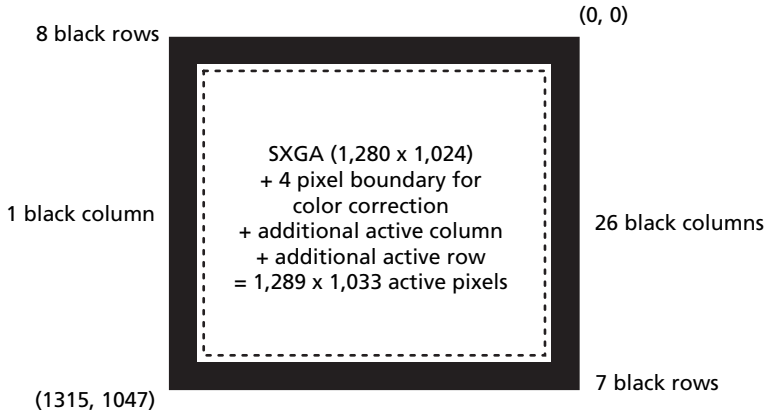
Name	Type	Description
RESET#	Input	Asynchronous reset of sensor when LOW. All registers reset to factory defaults.
STANDBY	Input	Enables low power standby mode when = 1.
OE#	Input	Enables output drivers when = 0.
SCLK	Input	Serial Clock.
CLKIN	Input	Master Clock into sensor (25 MHz maximum).
SDATA	I/O	Serial Data.
LINE_VALID	Output	Line Valid: Active HIGH during line of selectable valid pixel data (see Reg0x20 for options).
FRAME_VALID	Output	Frame Valid: Active HIGH during frame of valid pixel data.
FLASH	Output	Synchronization pulse for external light source.
PIXCLK	Output	Pixel Clock Output. Pixel data outputs are valid during rising edge of this clock.
DOUT0	Output	Pixel Data Output Bit 0 (LSB).
DOUT1	Output	Pixel Data Output Bit 1.
DOUT2	Output	Pixel Data Output Bit 2.
DOUT3	Output	Pixel Data Output Bit 3.
DOUT4	Output	Pixel Data Output Bit 4.
DOUT5	Output	Pixel Data Output Bit 5.
DOUT6	Output	Pixel Data Output Bit 6.
DOUT7	Output	Pixel Data Output Bit 7.
DOUT8	Output	Pixel Data Output Bit 8.
DOUT9	Output	Pixel Data Output Bit 9 (MSB).
VDDQ	Power	Digital I/O Power.
VAA	Power	Analog Power.
VAAPIX	Power	Pixel Array Power.
VDD	Power	Digital Core Power.
AGND	Ground	Analog Ground.
DGND	Ground	Digital Core Ground.
DGNDQ	Ground	Digital I/O Ground.
NC	–	No Connect.

Pixel Data Format

Pixel Array Structure

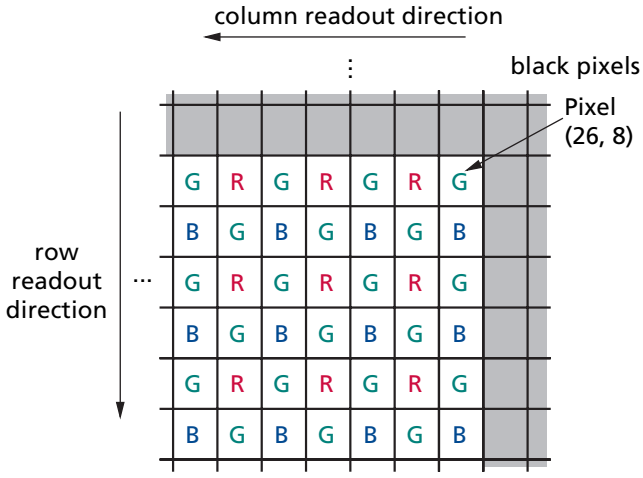
The MT9M011 pixel array is configured as 1,316 columns by 1,048 rows (shown in Figure 3). The first 26 columns and the first eight rows of pixels are optically black, and can be used to monitor the black level. The last column and the last seven rows of pixels are also optically black. The black row data is used internally for the automatic black level adjustment. However, the first eight black rows can also be read out by setting the sensor to raw data output mode (Reg0x22). There are 1,289 columns by 1,033 rows of optically active pixels, which provides a four-pixel boundary around the SXGA (1,280 x 1,024) image to avoid boundary effects during color interpolation and correction. The additional active column and additional active row are used to allow horizontally and vertically mirrored readout to also start on the same color pixel.

Figure 3: Pixel Array Description



The MT9M011 uses a Bayer color pattern, shown in Figure 4. The even-numbered rows contain green and red color pixels, and odd-numbered rows contain blue and green color pixels. Even-numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels.

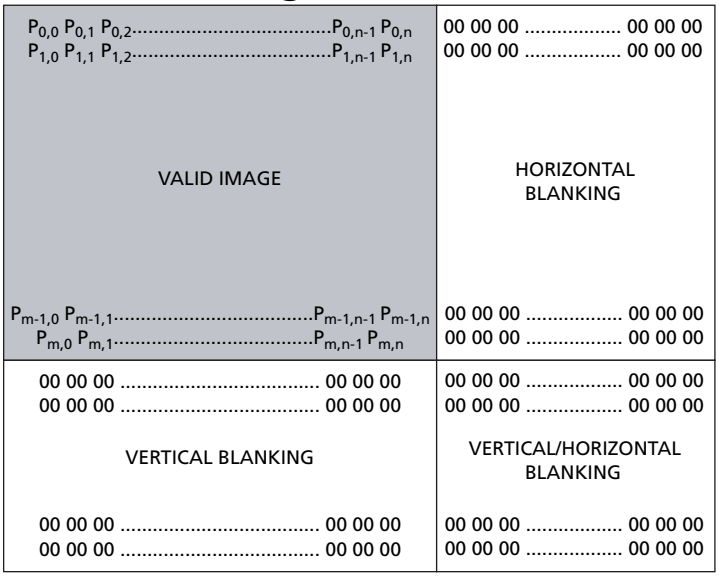
Figure 4: Pixel Color Pattern Detail (Top Right Corner)



Output Data Format

The MT9M011 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 5. The amount of horizontal blanking is programmable through Reg0x05 and Reg0x07; while vertical blanking is programmable through Reg0x06 and Reg0x08, respectively. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in "Output Data Timing" on page 9.

Figure 5: Spatial Illustration of Image Readout



Output Data Timing

The data output of the MT9M011 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period. The PIXCLK signal is nominally the inverted of the master clock, allowing PIXCLK to be used as a clock to latch the data. It is continuously enabled, even during the blanking period. The MT9M011 can be programmed to delay the PIXCLK edge relative to the DOUT transitions from 0 to 3.5 master clocks, in steps of one-half of a master clock. This is achieved by programming the corresponding bits in Reg0x0A. The parameters P, A, and Q in Figure 7 are defined in Table 3 on page 10. The high time is defined as parameter A = (Reg0x04 x PIXCLK_PERIOD).

Figure 6: Timing Example of Pixel Data

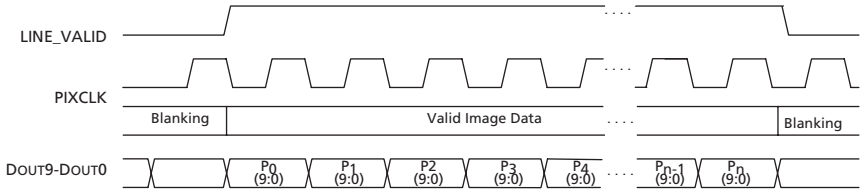


Figure 7: Row Timing and FRAME_VALID/LINE_VALID Signals

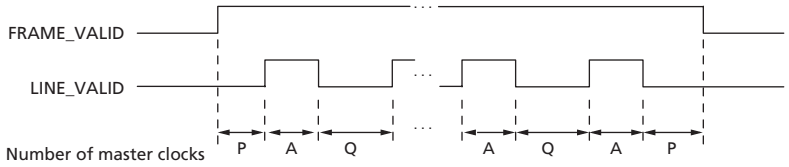


Table 3: Frame Time

Parameter	Name	Equation (master clocks units)	Default Timing at 25 MHZ
A	Active Data Time	Reg0x04 x PIXCLK_PERIOD (For skip 2x mode: divide Reg0x04 by 2, For skip 4x mode: divide Reg0x04 by 4)	1,280 pixel clocks = 1,280 master = 51.2µs
P	Frame Start/End Blanking	6 x PIXCLK_PERIOD	6 pixel clocks = 6 master = 0.24µs
Q	Horizontal Blanking	HBLANK_REG x PIXCLK_PERIOD	396 pixel clocks = 396 master = 15.84µs
A+Q	RowTime	(Reg0x04 + HBLANK_REG) x PIXCLK_PERIOD	1,676 pixel clocks = 1,676 master = 67.04µs
V	Vertical Blanking	VBLANK_REG x (A + Q) + (Q - 2 x P)	84,184 pixel clocks = 84,184 master = 3.37ms
Nrows x (A + Q)	Frame Valid Time	Reg0x03 x (A + Q) - (Q - 2 x P) (For skip 2x mode: divide Reg0x03 by 2, For skip 4x mode: divide Reg0x03 by 4)	1,715,840 pixel clocks = 1,715,840 master = 68.63ms
F	Total Frame Time	(Reg0x03 + VBLANK_REG) x (A + Q)	1,800,024 pixel clocks = 1,800,024 master = 72.0ms

1ADC_MODE:

Reg0xC8, bit 3 = 1: Reg0x20, bit 10
Reg0xC8, bit 3 = 0: Reg0x21, bit 10 (0 = 2 ADC mode, 1 = 1 ADC mode)
Default = 0

HBLANK_REG:

Reg0xC8, bit 0 = 1: Reg0x05
Reg0xC8, bit 0 = 0: Reg0x07
1ADC_MODE = 0: Minimum value is 202, 1ADC_MODE = 1: Minimum value is 114
Default = 396 (13.9 fps)

Note: For frame rate of 15 fps, set Reg0x05 to 272

VBLANK_REG:

Reg0xC8, bit 1 = 1: Reg0x06
Reg0xC8, bit 1 = 0: Reg0x08
Minimum value: sum of dark and extra rows enabled in Reg0x22 and Reg0x24
Default = 50

PIXCLK_PERIOD:

1ADC_MODE = 0: Reg0x0A, bit 3 - 0
1ADC_MODE = 1: (Reg0x0A, bit 3 - 0) x 2
A value of 0 in the register is not allowed.
Default = 1

The sensor timing is shown in terms of pixel clock and master clock cycles (please refer to Figure 6 on page 9). The recommended master clock frequency is 25 MHz. The vertical blank and total frame time equations assume that the number of integration rows (Reg0x09) is less than or equal to the number of active rows plus blanking rows (Reg0x03 + VBLANK_REG). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 4.

Table 4: Frame Time—Long Integration Time

Parameter	Name	Equation (master clock)	Default Timing
V′	Vertical Blanking (long integration time)	(Reg0x09 – Reg0x03) x (A + Q) + (Q - 2 x P)	84,184 pixel clocks = 3.37ms
F′	Total Frame Time (long integration time)	(Reg0x09) x (A + Q)	1,800,024 pixel clocks = 72.0ms

Serial Bus Description

Registers are written to and read from the MT9M011 through the two-wire serial interface bus. The sensor is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9M011 through the serial data (SDATA) line. The SDATA line is pulled up to 2.8V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address
- a(an) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a “0” indicates a write and a “1” indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9M011 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A “0” (0xBA) in the LSB (least significant bit) of the address indicates write mode, and a “1” (0xBB) indicates read mode.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

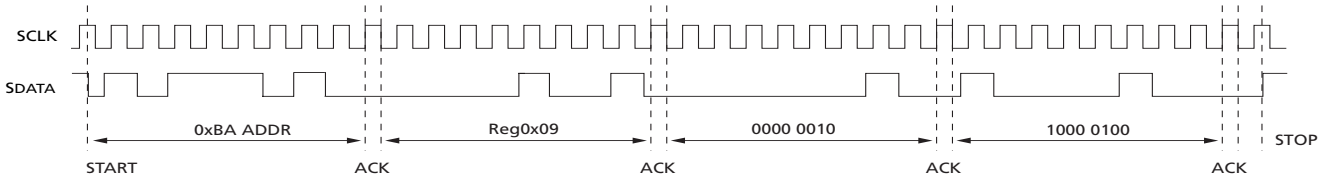
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-wire Serial Interface Sample Write and Read Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 8. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit transfer, the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

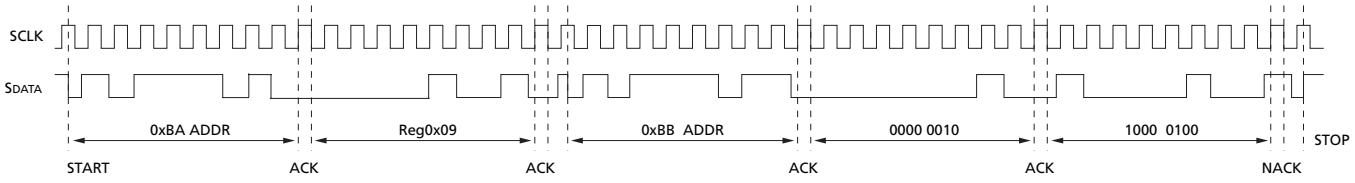
Figure 8: Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 9. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

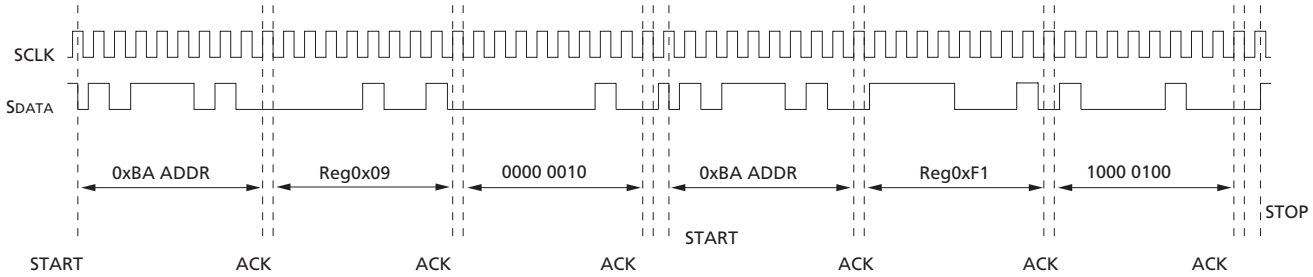
Figure 9: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284



Eight-Bit Write Sequence

To be able to write one byte at a time to the register a special register address is added. The 8-bit write is done by first writing the upper 8 bits to the desired register and then writing the lower 8 bits to the special register address (Reg0xF1). The register is not updated until all 16 bits have been written. It is not possible to just update half of a register. In Figure 10 a typical sequence for 8-bit writing is shown. The second byte is written to the special register (Reg0xF1).

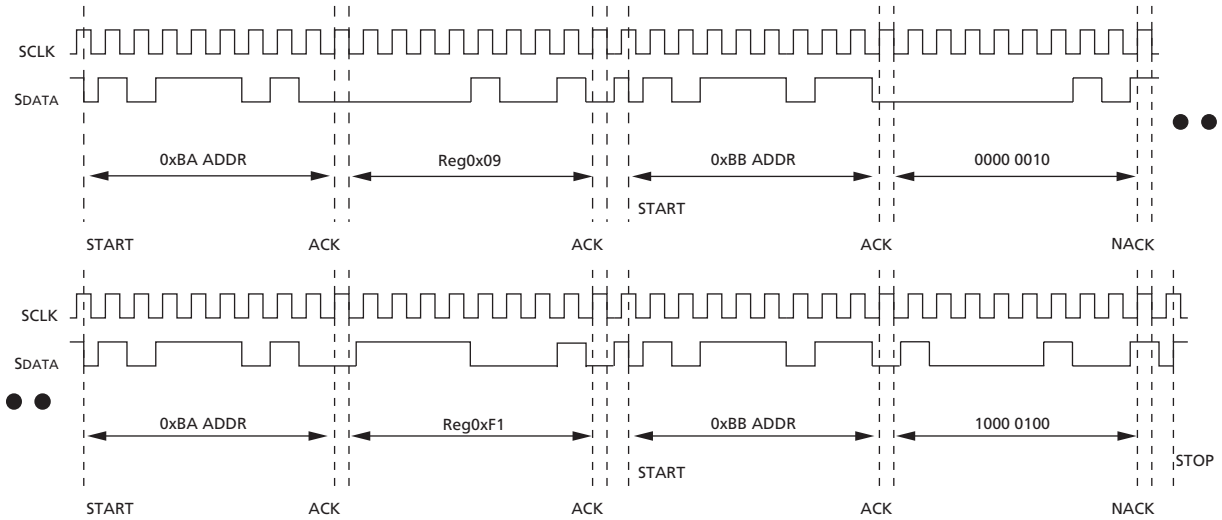
Figure 10: Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284



Eight-Bit Read Sequence

To read one byte at a time the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (Reg0xF1) the lower 8 bits are accessed (Figure 11). The master sets the no-acknowledge bits.

Figure 11: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284



Registers

Table 5: Register List and Default Value

Register Number (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0x00/0xFF	Chip Version	0001 0100 0010 0010 (LSB)	0x1433
0x01	Row Start	0000 0ddd dddd dddd	0x000C
0x02	Column Start	0000 0ddd dddd dddd	0x001E
0x03	Row Width	0000 0ddd dddd dddd	0x0400
0x04	Column Width	0000 0ddd dddd dddd	0x0500
0x05	Horizontal Blanking B	00dd dddd dddd dddd	0x018C
0x06	Vertical Blanking B	0ddd dddd dddd dddd	0x0032
0x07	Horizontal Blanking A	00dd dddd dddd dddd	0x00C6
0x08	Vertical Blanking A	0ddd dddd dddd dddd	0x0019
0x09	Shutter Width	dddd dddd dddd dddd	0x0432
0x0A	Row Speed	ddd0 000d dddd dddd	0x0011
0x0B	Extra Delay	00dd dddd dddd dddd	0x0000
0x0C	Shutter Delay	00dd dddd dddd dddd	0x0000
0x0D	Reset	d000 00dd 00dd dddd	0x0008
0x1F	Frame Valid Control	dddd dddd dddd dddd	0x0000
0x20	Read Mode B	dd00 0ddd dddd dddd	0x0200
0x21	Read Mode A	0000 0d00 0000 dd00	0x040C
0x22	Dark Col/Rows	0000 00dd dddd dddd	0x0129
0x23	Flash	??dd dddd dddd dddd	0x0608
0x2B	Green1 Gain	0000 0ddd dddd dddd	0x0020
0x2C	Blue Gain	0000 0ddd dddd dddd	0x0020
0x2D	Red Gain	0000 0ddd dddd dddd	0x0020
0x2E	Green2 Gain	0000 0ddd dddd dddd	0x0020
0x2F	Global Gain	0000 0ddd dddd dddd	0x0020
0xC8	Context Control	d000 0000 d000 dddd	0x000B

Note: 1 = always 1
0 = always 0
d = programmable
? = read only

Table 6: Reserved Register List and Default Value

Register Number (Hex)	Description	Default Value (Hex)
0x24	Reserved	0x806F
0x30	Reserved	0x042A
0x31	Reserved	0x1C00
0x32	Reserved	0x0000
0x33	Reserved	0x0349
0x34	Reserved	0xC019
0x36	Reserved	0xF0F0
0x37	Reserved	0x0000
0x3B	Reserved	0x0021
0x3C	Reserved	0x1A20
0x3D	Reserved	0x201E
0x3E	Reserved	0x2020
0x3F	Reserved	0x2020
0x40	Reserved	0x201C
0x41	Reserved	0x00D7
0x42	Reserved	0x0777
0x59	Reserved	0x000C
0x5A	Reserved	0xC00F
0x5B	Reserved	RO
0x5C	Reserved	RO
0x5D	Reserved	RO
0x5E	Reserved	RO
0x5F	Reserved	0x231D
0x60	Reserved	0x0080
0x61	Reserved	0x0000
0x62	Reserved	0x0000
0x63	Reserved	0x0000
0x64	Reserved	0x0000
0x65	Reserved	0x0000
0x70	Reserved	0x7B0A
0x71	Reserved	0x7B0A
0x72	Reserved	0x190E
0x73	Reserved	0x180F
0x74	Reserved	0x5732
0x75	Reserved	0x5634
0x76	Reserved	0x7335
0x77	Reserved	0x3012
0x78	Reserved	0x7902
0x79	Reserved	0x7506
0x7A	Reserved	0x770A
0x7B	Reserved	0x7809
0x7C	Reserved	0x7D06
0x7D	Reserved	0x3110
0x7E	Reserved	0x007E
0x80	Reserved	0x007F

Table 6: Reserved Register List and Default Value

Register Number (Hex)	Description	Default Value (Hex)
0x81	Reserved	0x007F
0x82	Reserved	0x570A
0x83	Reserved	0x580B
0x84	Reserved	0x470B
0x85	Reserved	0x480E
0x86	Reserved	0x5B02
0x87	Reserved	0x005C
0xF0	Reserved	0x0000
0xF5	Reserved	0x07FF
0xF6	Reserved	0x07FF
0xF7	Reserved	0x0000
0xF8	Reserved	0x0000
0xF9	Reserved	0x007C
0xFA	Reserved	0x0000
0xFB	Reserved	0x0000
0xFC	Reserved	0x0000
0xFD	Reserved	0x0000

Note: Writing to these registers may cause the part to go into an unknown state.

Table 7: Register Description

Bit	Bit Description		Default (Hex)	Sync'd to Frame Start	Bad Frame	Read/ write
0x00/0xFF (0/255) Chip Version						
15:0	Chip Version	Chip version - read-only.	1433			R
0x01 (1) Row Start						
10:0	Row Start	The first row to be read out (not counting any dark rows that may be read). To window the image down, set this register to the starting Y value. Setting a value less than 8 is not recommended since the dark rows should be read using Reg0x22.	0C	Y	YM	W
0x02 (2) Column Start						
10:0	Column Start	The first column to be read out (not counting dark columns that may be read). To window the image down, set this register to the starting X value. Setting a value below 24 decimals (0x18) is not recommended since readout of dark columns should be controlled by Reg0x22.	1E	Y	YM	W
0x03 (3) Row Width						
10:0	Row Width	Number of rows in the image to be read out (not counting any dark rows or border rows that may be read).	400	Y	YM	W
0x04 (4) Column Width						
10:0	Column Width	Number of columns in image to be read out (not counting any dark columns or border columns that may be read).	500	Y	YM	W
0x05 (5) Horizontal Blanking B						
10:0	Horizontal Blanking B	Number of blank columns in a row when context B is chosen (Reg0xC8, bit 0 = 1). If set smaller than the minimum value the minimum value will be used. With default settings the minimum horizontal blanking will be 202 columns when using two ADCs and 114 columns when using one ADC. Default of 0x18C = 13.9 fps @ 25 MHz Setting of 0x110 = 15 fps @ 25 MHz	18C	Y	YM	W
0x06 (6) Vertical Blanking B						
14:0	Vertical Blanking B	Number of blank rows in a frame when context B is chosen (Reg0xC8, bit 1 = 1). This number must be equal to or larger than the number of dark rows read out in a frame specified by Reg0x22.	32	Y	N	W
0x07 (7) Horizontal Blanking A						
10:0	Horizontal Blanking A	Number of blank columns in a row when context A is chosen (Reg0xC8, bit 0 = 0). The extra columns will be added at the beginning of a row. If set smaller than the minimum value the minimum value will be used. With default settings the minimum horizontal blanking will be 202 columns when using two ADCs and 114 columns when using one ADC. Default of 0xC6 = 27.8 fps @ 25 MHz Setting of 0x88 = 30 fps @ 25 MHz	C6	Y	YM	W

Table 7: Register Description (Continued)

Bit	Bit Description		Default (Hex)	Sync'd to Frame Start	Bad Frame	Read/ write
0x08 (8) Vertical Blanking A						
14:0	Vertical Blanking A	Number of blank rows in a frame when context A is chosen (Reg0xC8, bit 1 = 1). This number must be equal to or larger than the number of dark rows read out in a frame specified by Reg0x22.	19	Y	N	W
0x09 (9) Shutter Width						
15:0	Shutter Width	Integration time in number of rows. In addition to this register the shutter delay register (Reg0x0C) and the overhead time will influence the integration time for a given row time.	432	Y	N	W
0x0A (10) Row Speed						
3:0	Pixel Clock Period	Pixel clock period in master clocks when two ADCs are used (Reg0x20/0x21, bit 10 = 0). The ADC clock will always be half the programmed frequency. When only one ADC is used the pixel clock frequency will be halved as well, so in this case will be equal to the ADC clock frequency. The value "0" is not allowed, "1" will be used instead.	1	Y	YM	W
7:4	Delay Pixel Clock	Delay PIXCLK in half master clock cycles. When set the pixel clock can be delayed in increments of half master clock cycles compared to the synchronization of FRAME_VALID, LINE_VALID and DATA_OUT.	1	N		W
8	Invert Pixel Clock	Invert pixel clock. When set, LINE_VALID, FRAME _VALID, and DATA_OUT will be set up to the falling edge of PIXCLK. When clear, they are set up to the rising edge if there are no delay of the pixel clock.	0	N		W
15:14	Reserved	–	0	–	–	–
0x0B (11) Extra Delay						
13:0	Extra Delay	Extra blanking inserted between frames specified in pixel clocks. Can be used to get a more exact frame rate. It might affect the integration times of parts of the image when the integration time is less than one frame.	0	Y		W
0x0C (12) Shutter Delay						
10:0	Shutter Delay	The amount of time from the end of the sampling sequence to the beginning of the pixel reset sequence. This variable will automatically be halved when one ADC is used so the time in us will remain the same. This register has an upper value defined by the fact that the reset needs to finish before the readout of that row to prevent changes in the row time.	0	Y	N	W

Table 7: Register Description (Continued)

Bit	Bit Description		Default (Hex)	Sync'd to Frame Start	Bad Frame	Read/ write
0x0D (13) Reset						
0	Reset	Setting this bit will put the sensor into reset mode, which will set the sensor to its default power-up state. Clearing this bit will resume normal operation.	0	N	YM	W
1	Restart	Setting this bit will cause the sensor to abandon the current frame and start resetting the first row. The delay before the first valid frame is read out equals the integration time. This bit always reads "0."	0	N	YM	W
2	Analog standby	0 = normal operation (default). 1 = disable analog circuitry.	0	N	YM	W
3	Chip Enable	1 = normal operation. 0 = stop sensor readout. When this is returned to "1," sensor readout restarts and starts resetting the starting row in a new frame. To reduce the digital power further the master clock to the sensor can be disabled or the standby pin can be used.	1	N	YM	W
4	Reserved	–	0	–	–	–
5	Reserved	–	0	–	–	–
8	Show bad frames	1 = output all frames (including bad frames). 0 = only output good frames (default). A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, pixel clock speed, zoom, row or column skip, or mirroring.	0	N		W
9	Restart bad frames	When set a restart will be forced to take place when a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay when masking out a bad frame will be the integration time rather than the full frame time.	0	N		W
15	Synchronize changes	0 = normal operation, update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal and vertical blanking, window size, row/column skip, or row mirror) at the next frame boundary. 1 = do not update any changes to these settings until this bit is returned to "0." All registers that are frame synchronized will be affected by the setting of this bit.	0	N		W
0x1F (31) FRAME_VALID Control						
6:0	Early FRAME_VALID rise	When enabled, the FRAME_VALID rising edge will happen for the programmed number of rows before the first LINE_VALID: (bits 6:0) x row time + horiz blank + constant (constant = 3 in default mode).	0	N		W
7	Enable early FRAME_VALID rise	1 = Enables the early rise of FRAME_VALID as set in bits 6:0. 0 = default. FRAME_VALID will go HIGH six pixel clocks before first LINE_VALID.	0	N		W

Table 7: Register Description (Continued)

Bit	Bit Description		Default (Hex)	Sync'd to Frame Start	Bad Frame	Read/ write
14:8	Early FRAME_VALID fall	When enabled the FRAME_VALID falling edge will happen the programmed number of rows before the end of the last LINE_VALID: (1 + bits 14:8) x row time + constant (constant = 3 in default mode).	0	N		W
15	Enable early FRAME_VALID fall	1 = Enables the early disabling of FRAME_VALID as set in bits 14:8. Note that LINE_VALID will still be generated for all active rows. 0 = default. FRAME_VALID will go LOW six pixel clocks after last LINE_VALID.	0	N		W
0x20 (32) Read Mode - Context B						
0	Mirror rows	Read out rows from bottom to top (upside down). When set, row readout starts from row (Row Start + Row Size) and continues down to (Row Start + 1). When clear, readout starts at Row Start and continues to (Row Start + Row Size - 1). This ensures that the starting color is maintained.	0	Y	YM	W
1	Mirror columns	Read out columns from right to left (mirrored). When set, column readout starts from column (Col Start + Col Size) and continues down to (Col Start + 1). When clear, readout starts at Col Start and continues to (Col Start + Col Size - 1). This ensures that the starting color is maintained.	0	Y	YM	W
2	Row skip 2x - context B	When Read Mode context B is selected (Reg0xC8, bit 3 = 1): 1 = read out two rows, and then skip two rows (i.e. row 8, row 9, row 12, row 13…). 0 = normal readout.	0	Y	YM	W
3	Column skip 2x - context B	When Read Mode context B is selected (Reg0xC8, bit 3 = 1): 1 = read out two columns, and then skip two columns (as with rows). 0 = normal readout.	0	Y	YM	W
4	Row skip 4x	1 = read out two rows, and then skip six rows (i.e. row 8, row 9, row 16, row 17…). 0 = normal readout.	0	Y	YM	W
5	Column skip 4x	1 = read out two columns, and then skip six columns (as with rows). 0 = normal readout.	0	Y	YM	W

Table 7: Register Description (Continued)

Bit	Bit Description		Default (Hex)	Sync'd to Frame Start	Bad Frame	Read/ write
7:6	Zoom	In zoom mode, the pixel data rate is slowed down by a factor of either 2 or 4, and either 1 or 3 additional blank rows are added between each output row. This is designed to give the controller logic time to repeat data to fill in a window that is either 2 or 4 times larger with repeated data. The pixel clock speed is not affected by this operation, and the output data for each pixel is valid for either 2 or 4 pixel clocks. In 2X zoom mode, every row is followed by a blank row (with its own LINE_VALID, but all data bits = 0) of equal time. In 4X zoom mode, every row is followed by three blank rows. The combination of this register and an appropriate change to the window start registers allows the user to zoom to a region of interest without affecting the frame rate. 00 = no zoom (default) X1 = zoom 2X 10 = zoom 4X	0	Y	YM	W
8	Over Sized	When this bit is set a 4-pixel border will be output around the active image array independent of readout mode (skip, zoom, mirror, etc.). Setting this bit will therefore add eight to the number of rows and columns in the frame.	0	Y	YM	W
9	Show Border	This bit indicates whether to show the border enabled by bit 8. When bit 8 is 0 this bit has no meaning. When bit 8 is 1, this bit decides whether the border pixels should be treated as extra active pixels (1) or extra blanking pixels (0).	1	N		W
10	Use 1 ADC - Context B	0 = Use both ADCs to achieve maximum speed. 1 = Use one ADC to reduce power. Maximum readout frequency is now half of the master clock, and the pixel clock is automatically adjusted as described for the pixel clock speed register.	0	Y	YM	W
14	Continuous Line Valid	1 = "Continuous" Line_Valid (continue producing line valid during vertical blanking). 0 = Normal Line_Valid (default) no line valid during vertical blanking.	0	N		W
15	Xor Line Valid	1 = Line valid = "Continuous" Line_Valid XOR Frame Valid. 0 = Normal Line Valid. Ineffective if Continuous Line_Valid is set.	0	N		W

Table 7: Register Description (Continued)

Bit	Bit Description		Default (Hex)	Sync'd to Frame Start	Bad Frame	Read/ write
0x21 (33) Read Mode - Context A						
2	Row skip 2x - Context A	When Read Mode context A is selected (Reg0xC8, bit 3 = 0): 1 = read out two rows, and then skip two rows (i.e. row 8, row 9, row 12, row 13…). 0 = normal readout.	1	Y	YM	W
3	Column skip 2x - Context A	When Read Mode context A is selected (Reg0xC8, bit 3 = 0): 1 = read out two columns, and then skip two columns (as with rows). 0 = normal readout.	1	Y	YM	W
10	1 ADC mode - Context A	When Read Mode context A is selected (Reg0xC8, bit 3 = 0): 0 = Use both ADCs to achieve maximum speed. 1 = Use one ADC to reduce power. Maximum readout frequency is now half of the master clock, and the pixel clock is automatically adjusted as described for the pixel clock speed register.	1	Y	YM	W
0x22 (34) Show Control						
2:0	Number of dark rows	Specifies the number of dark rows to read out at the beginning of each frame when the dark row readout is enabled (bit 3). The programmed number is 1 less than the number of rows.	1	N	Y	W
3	Enable dark row readout	Enables the readout of the dark rows specified in bits 2:0.	1	N	Y	W
6:4	Dark start address	The start address for the dark rows. Must be set so all dark rows read out falls in the address space 0-7.	2	N	N	W
7	Show dark rows	When set, the programmed dark rows will be output before the active window. Frame valid will thus be asserted earlier than normal. This has no effect on integration time or frame rate. Whether the dark rows are shown in the image or not the definition frame start is before the dark rows are read out. All frame synced registers will be updated at this point.	0	N	N	W
8	Read dark columns	When disabled, an arbitrary number of dark columns can be read out by including them in the active image. Enabling the dark columns do not have an effect on the row time, but it will increase the minimum horizontal blanking value allowed.	1	N	Y	W
9	Show dark columns	When set, the programmed dark columns will be output before the active pixels in a line.	0	N	N	W
0x23 (35) Flash Control						
7:0	Xenon count	Length of FLASH_STROBE pulse when Xenon flash is enabled. The value specifies the length in 1,024 master clock cycle increments.	8	N	N	W
8	LED flash	Enable LED flash. When set, the FLASH_STROBE will go on prior to the start of the resetting of a frame. When disabled the FLASH_STROBE will remain high until the finish of the readout of the current frame.	0	Y	Y	W

Table 7: Register Description (Continued)

Bit	Bit Description		Default (Hex)	Sync'd to Frame Start	Bad Frame	Read/ write
9	Every frame	1 = Flash should be enabled every frame. 0 = Flash should be enabled for 1 frame only.	1	N	N	W
10	End of reset	1 = In Xenon mode the flash should be triggered after the resetting of a frame. 0 = In Xenon mode the flash should be enabled after the readout of a frame.	1	N	N	W
12:11	Frame delay	Delay of the flash pulse measured in frames.	0	N	N	W
13	Xenon flash	Enable Xenon flash. When set, the output pin FLASH_STROBE will be pulsed high for the programmed period during vertical blanking. This is achieved by keeping the integration time equal to one frame, and the pulse width less than the vertical blanking time.	0	Y	N	W
14	Reserved	–	0	–	–	–
15	FLASH_STROBE	Read-only bit that indicated whether the FLASH_STROBE pin is enabled.	0			W
0x2B (43) Green1 Gain						
6:0	Initial gain	Initial Gain = bits (6:0) x 0.03125.	20	Y	N	W
8:7	Analog gain	Analog Gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x Gain).	0	Y	N	W
10:9	Digital gain	Total Gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2x gain).	0	Y	N	W
0x2C (44) Blue Gain						
6:0	Initial gain	Initial Gain = bits (6:0) x 0.03125.	20	Y	N	W
8:7	Analog gain	Analog Gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain).	0	Y	N	W
10:9	Digital gain	Total Gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2x gain).	0	Y	N	W
0x2D (45) Red Gain						
6:0	Initial gain	Initial Gain = bits (6:0) x 0.03125.	20	Y	N	W
8:7	Analog gain	Analog Gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain).	0	Y	N	W
10:9	Digital gain	Total Gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2x gain).	0	Y	N	W
0x2E (46) Green2 Gain						
6:0	Initial gain	Initial Gain = bits (6:0) x 0.03125.	20	Y	N	W
8:7	Analog gain	Analog Gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain).	0	Y	N	W
10:9	Digital gain	Total Gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2x gain).	0	Y	N	W
0x2F (47) Global Gain						
10:0	Global Gain	This register can be used to set all four gains at once. When read, it will return the value stored in Reg0x2B.	20	Y	N	W

Table 7: Register Description (Continued)

Bit	Bit Description		Default (Hex)	Sync'd to Frame Start	Bad Frame	Read/ write
0xC8 (200) Context Control						
0	Horizontal blanking select	1 = Use Horizontal Blanking context B, Reg0x05. 0 = Use Horizontal Blanking context A, Reg0x07.	1	Y	YM	W
1	Vertical blanking select	1 = Use Vertical Blanking context B, Reg0x06. 0 = Use Vertical Blanking context A, Reg0x08.	1	Y	YM	W
2	LED flash enable	Enable LED flash. Same physical register as Reg0x23, bit 8.	0	Y	Y	W
3	Read mode select	1 = Use Read Mode context B, Reg0x20. 0 = Use Read Mode context A, Reg0x21. Note that bits only found in Read Mode context B register will always be taken from this register.	1	Y	YM	W
7	Xenon flash enable	Enable Xenon flash. Same physical register as Reg0x23, bit 13.	0	Y	N	W
15	Restart	Setting this bit will cause the sensor to abandon the current frame and start resetting the first row. Same physical register as Reg0x0D, bit 1.	0	N	YM	W

The following notation is used in Table 7:

Sync'd to frame start
N = No. The register value will be updated and used immediately.
Y = Yes. The register value will be updated at next frame start as long as the synchronize changes bit is 0. Note also that frame start is defined as when the first dark row is read out. By default this is eight rows before FRAME_VALID goes HIGH

Bad frame
A bad frame is a frame where all rows do not have the same integration time, or offsets to the pixel values changed during the frame.
N = No. Changing the register value will not produce a bad frame.
Y = Yes. Changing the register value might produce a bad frame.
YM = Yes, but the bad frame will be masked out unless the show bad frames feature is enabled.

Read/Write
R = Read-only register/bit.
W = Read/Write register/bit.

Feature Description

Window Control

Reg0x01 Row Start, Reg0x02 Column Start, Reg0x03 Row Width, and Reg0x04 Column Width These registers control the size and starting coordinates of the window. By changing these registers, any image format smaller than or equal to SXGA can be specified.

Border of Pixels

Reg0x20, bits 8 and 9 By setting these register bits, a four-pixel border will be added around the specified image. Since the border is independent of the readout mode, this border can then be used as extra pixels for image processing algorithms. This means that even in the skip modes, a four-pixel border will be output in the image. When enabled, eight rows and columns must be added to the settings in the row and column width to get the new window size. If the border is enabled but not shown in the image (bits 9-8 = 01), eight rows and columns should be added to the horizontal and vertical blanking numbers instead.

Readout Modes

Column Mirror Image

By setting bit 1 of Reg0x20, the readout order of the columns will be reversed as shown in Figure 12. The starting color will be preserved when mirroring the columns.

Row Mirror Image

By setting bit 0 of Reg0x20, the readout order of the rows will be reversed as shown in Figure 13. The starting color will be preserved when mirroring the rows.

Figure 12: Readout of 6 Pixels in Normal and Column Mirror Output Mode

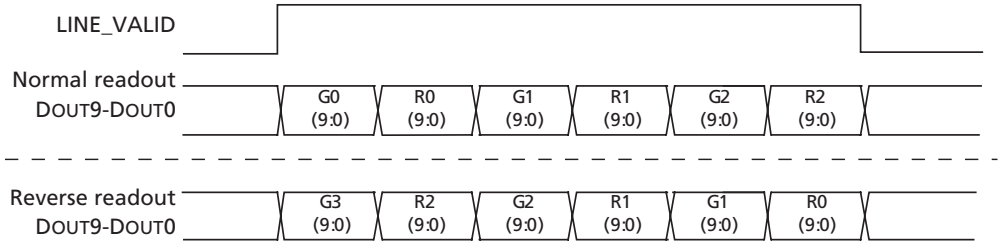
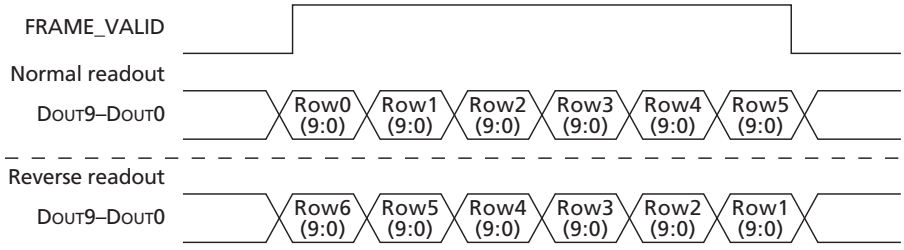


Figure 13: Readout of 6 Rows in Normal and Row Mirror Output Mode



Column and Row Skip

By setting bit 3 of Reg0x20 (Reg0x21), only half of the columns set will be read out, as shown in Figure 14. To preserve the Bayer pattern in the pixel array pair of columns are read out or skipped. The row skip mode works in the same way, and will read out two rows and then sip two. The row skip works in the same way and will only read out rows with bit 1 equal to "0." Row skip mode is enabled by setting bit 2 of Reg0x20. For both row and column skips, the number of rows or columns read out will be half of what is set in Reg0x03 or Reg0x04, respectively.

The sensor can also be programmed to only read out a sixteenth of the specified window size by setting bits 4 and 5 of Reg0x20, as shown in Figure 15 (Bayer pattern is preserved).

Figure 14: Readout of 8 Pixels in Normal and Column Skip 2X Output Mode

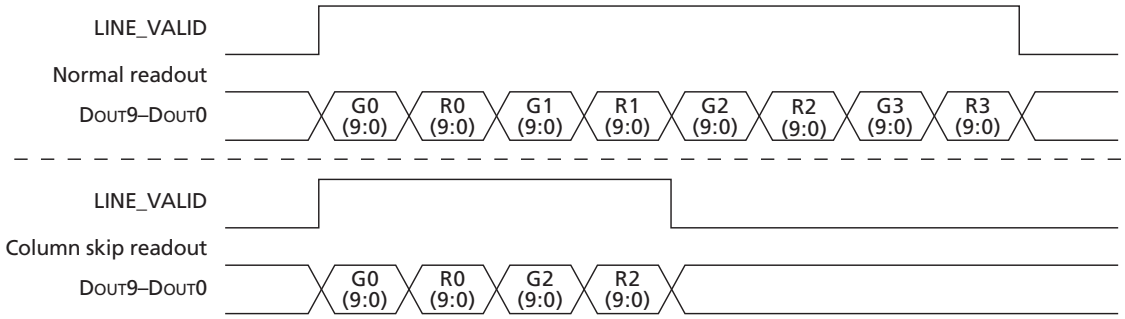
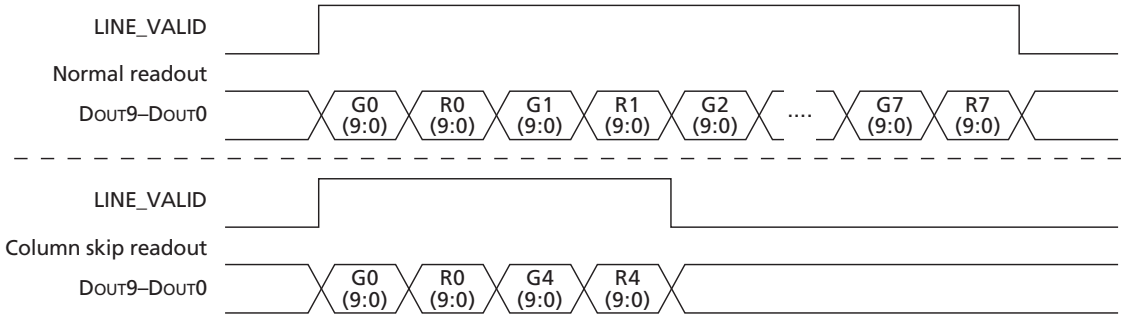


Figure 15: Readout of 16 Pixels in Normal and Column Skip 4X Output Mode

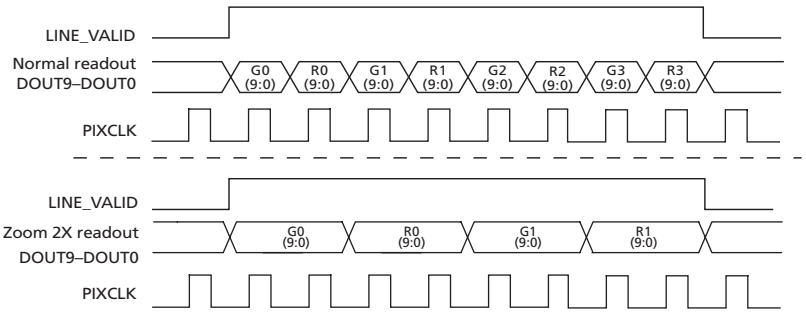


Digital Zoom

Reg0x20, bits 7:6 Digital Zoom In zoom mode, the pixel data rate is slowed down by a factor of either 2 or 4, and either 1 or 3 additional blank rows are added between each output row. This is designed to give the controller logic time to repeat data to fill in a window that is either 4 or 16 times larger with repeated data.

The pixel clock speed is not affected by this operation, and the output data for each pixel is valid for either 2 or 4 pixel clocks. In 2X zoom mode, every row is followed by a blank row (with its own line valid, but all data bits = 0) of equal time. In 4X zoom mode, every row is followed by three blank rows. In the zoom modes, Reg0x03 and Reg0x04 will still specify the window size out of the sensor including the extra blanking, so the active image read out will in effect be a quarter or a sixteenth of the output image.

Figure 16: Readout of 8 Pixels in Normal and Zoom 2X Output Mode



Frame Rate Control

When a window size is set, the blanking registers (Reg0x05-Reg0x08) along with the Row Speed Register (Reg0x0A) will let you program a desired frame rate. The frame timing equations at the beginning of this document shows you how to calculate the different timings. If these equations are turned around they can help you set the horizontal or vertical blanking values to achieve a desired frame rate:

HBLANK_REG = master clock freq / (frame rate x (Reg0x03 + VBLANK_REG) x PIXCLK_PERIOD) - Reg0x04

VBLANK_REG = master clock freq / (frame rate x (Reg0x04 + HBLANK_REG) x PIXCLK_PERIOD) - Reg0x03

Readout Speeds and Power Savings

The MT9M011 sensor has two ADCs to convert the pixel values to digital. Since the ADCs run at half the master clock frequency, this makes it possible to achieve a data rate equal to the master clock frequency. On the other hand, it also makes it an option for slower readout to turn one of the ADCs off in order to reduce the power consumption of the sensor. Reg0x20 (Reg0x21), bit 10, chooses between the two modes:

0 = Use both ADCs and read out at the set pixel clock frequency (Reg0x0A, bits 3:0)
1 = Use 1 ADC and read out at half the set pixel clock frequency (Reg0x0A, bits 3:0)

This can be used, for example, when the camera is in preview mode. To make the transitions between two sensor settings easier, some simple context switching is available in the MT9M011, as described below.

Context Switching

Reg0xC8 is designed to help switching between sensor modes easily. Some key registers and bits in the sensor have two physical register locations, called contexts. Bits 0, 1, and 3 of Reg0xC8 will decide which context of the register that is currently in use. A 1 in a bit will choose context B, while a 0 will select context A for that parameter. The select bits can be used in any combination, but by default it is set up to make switching between a preview mode to a full resolution mode easy:

Full resolution mode: (default)
Context B:

Reg0xC8 = 0x000B (Context B)
Reg0x05 = 0x018C (Horizontal Blanking)
Reg0x06 = 0x0032 (Vertical Blanking)
Reg0x20, bit 10 = 0, bit 3 = 0, bit 2 = 0 (2 ADCs, no column or row skip)

A full resolution SXGA picture will be output at the master clock frequency at 13.9 fps.

Context A:

Reg0xC8 = 0x0000 (Context A)
Reg0x07 = 0x00C6 (Horizontal Blanking)
Reg0x08 = 0x0019 (Vertical Blanking)
Reg0x21, bit 10 = 1, bit 3 = 1, bit 2 = 1 (1 ADC, column and row skip enabled)

A preview image (half SXGA size) will be output at half of the master clock frequency at 27.8 fps.

Note that the horizontal and vertical blanking values are set so the row time will be preserved in the two modes. This way, a switch between the modes will not affect the integration time. This is also the reason that the shutter delay register (Reg0x0C) is automatically halved in 1 ADC mode. A few more control bits are also available through the context register (Reg0xC8) so flash and restarting of the sensor can be done at the same time as changing the contexts. See Table 7, Register Description, on page 19 for more information.

Minimum Horizontal Blanking

The minimum horizontal blanking value is constrained by the time used for sampling a row of pixels and the overhead in the readout of a row. This can be expressed in an equation as:

min hblank = sampling time + dark col time + overhead

2 ADC Mode:

min hblank = 20 x (Reg0x22, bit 8) + 182 = 202 (default)

1 ADC Mode:

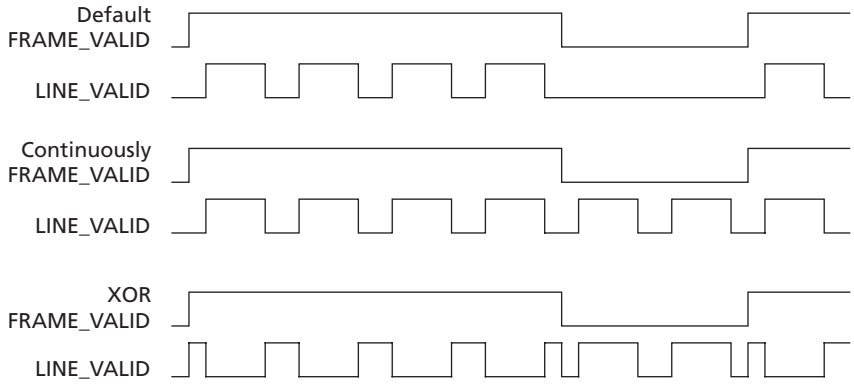
min hblank = 20 x (Reg0x22, bit 8) + 94 = 114 (default)

Valid Data Signals Options

LINE_VALID Signal

By setting Bit 9 and 10 of Reg0x20, the LINE_VALID signal can be programmed for three different output formats. The formats shown below illustrate reading out four rows and two vertical blanking rows (Figure 17). In the last format, the LINE_VALID signal is the XOR between the continuous LINE_VALID signal and the FRAME_VALID signal.

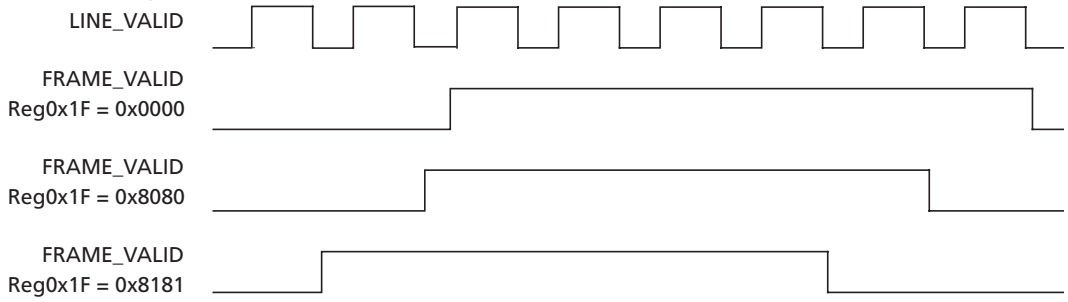
Figure 17: Different LINE_VALID Formats



FRAME_VALID Signal

Each edge of the FRAME_VALID signal can be programmed to occur earlier than the default time described in the frame timing equations. This is useful if a controller chip needs advanced notice that an image is ready and will be read out. Reg0x1F is used for this flexibility; Table 7, Register Description, on page 19 provides more information and equations concerning the time when the FRAME_VALID action will take place.

Figure 18: FRAME_VALID Signals



Note: The stippled LINE_VALID pulses are for illustration purposes only. The rising and falling edges can be programmed independently.

Integration Time

The following registers along with the row time control the integration time:

Register 0x09: number of rows of integration, default = 0x0432 (1074)

Register 0x0C: shutter delay, default = 0x0000 (0). This is the number of pixel clocks that the timing and control logic waits before asserting the reset for a given row

The actual total integration time, ^{t}INT, is:

^{t}INT = Reg0x09 x Row Time - Overhead Time - Shutter Delay

where:

Row Time = (Reg0x04 + HBLANK_REG) x PIXCLK_PERIOD master clock periods

Overhead Time = 64 master clock periods

Shutter Delay = Reg0x0C x PIXCLK_PERIOD master clock periods

In this expression, the row time term, Reg0x09 x row time, corresponds to the number of rows integrated. The overhead time (64 master clocks) is the overhead time between the READ cycle and the RESET cycle, and the final term is the effect of the shutter delay.

Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. If Reg0x09 is increased beyond the total number of rows per frame, MT9M011 will add additional blanking rows as needed. A second constraint is that ^{t}INT must be adjusted to avoid banding in the image from light flicker. Under 60Hz flicker, this means ^{t}INT must be a multiple of 1/120 of a second. Under 50Hz flicker, ^{t}INT must be a multiple of 1/100 of a second.

Maximum Shutter Delay

The maximum shutter delay is set by the reset cycle time and the overall row time available. It will differ for 1 and 2 ADC mode, as shown in the equations below:

2 ADC Mode:

max_shutter_delay = row time - 385
= row time - (365 + 20 x (Reg0x22, bit 8))
= row time - (sampling time + resetting time + dark cols + overhead)

1 ADC Mode:

max_shutter_delay = row time - 614
= row time - (574 + 2 x 20 (Reg0x22, bit 8))

Flash Description

Reg0x23 The MT9M011 supports both Xenon and LED flash through the FLASH_STROBE output pin. The timing of the FLASH_STROBE pin with the default settings are shown in Figure 19, Figure 20, and Figure 21. Additionally, the flash can be programmed to only be fired once, be delayed by a few frames when asserted, or programmed for other timing, as described in Table 7 on page 19.

Since enabling the LED flash will cause one bad frame, where several of the rows only had the flash on for part of their integration time, it is recommended to do a restart (Reg0x0D, bit 1) of the sensor when enabling the flash. The first bad frame will then be masked out as shown in Figure 21.

Figure 19: Xenon Flash Enabled

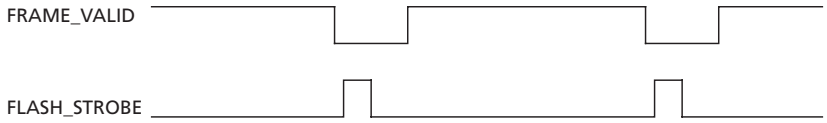


Figure 20: LED Flash Enabled (integration time = number of rows in a frame)

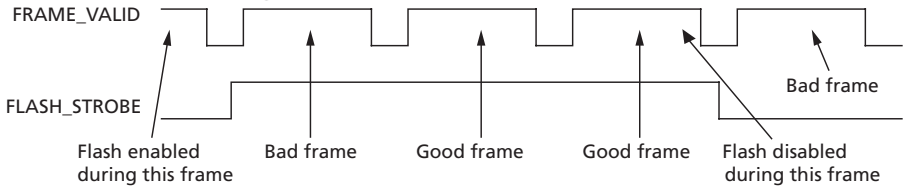
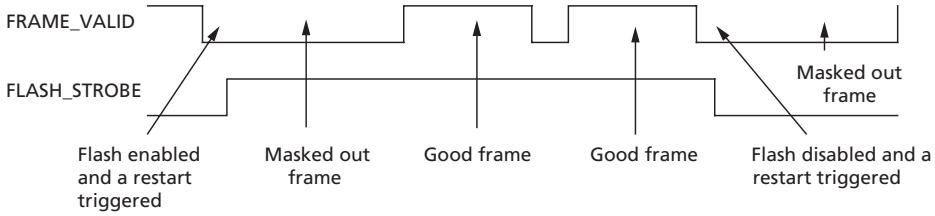


Figure 21: LED Flash Enabled with Restart (integration time = number of rows in a frame)



Recommended Gain Settings

The gains for green1, blue, red, and green2 pixels are set by registers Reg0x2B, Reg0x2C, Reg0x2D, and Reg0x2D, respectively. Gain can also be set globally by Reg0x2F. The analog gain is set by bits[8:0] of the corresponding register as following:

Gain = (Bit[8] + 1) x (Bit[7] + 1) x (Bit[6:0]/32)

Digital gain is set by bits 9 and 10 of the same registers.

The analog gain circuitry (pre-ADC) is designed to offer signal gains from 1 to 15.875.

The minimum gain of 1 (register set to 0x0020) corresponds to the lowest setting where the pixel signal is guaranteed to saturate the ADC under all specified operating conditions. Any reduction of the gain below this value may cause the sensor to saturate at ADC output values less than the maximum, under certain conditions. It is recommended that this guideline be followed at all times.

Since bits 7 and 8 of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, while the same overall gain. Table 8 lists the recommended gain settings.

Table 8: Recommended Gain Settings

Desired Gain	Recommended Settings (gain registers)	Conversion Formula (arithmetic)
1.000 to 1.969	0x020 to 0x03F	(Register value)/32
2.000 to 7.938	0x0A0 to 0x0FF	(Register value - 128)/16
8.000 to 15.875	0x1C0 to 0x1FF	(Register value - 384)/8

Electrical Specifications

Table 9: DC Electrical Characteristics

(V_{DD} = V_{AA} = $V_{DD}Q$ = 2.8V; T_A = 25°C; 13.9 fps at 25 MHz)

Symbol	Definition	Conditions	MIN	TYP	MAX	Units
V_{IH}	Input High Voltage		V_{DD} - 0.3		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} = V_{DD} or DGND	-15		15	µA
V_{OH}	Output High Voltage		$V_{DD}Q$			V
V_{OL}	Output Low Voltage		0		0.2	V
I_{OZ}	Tri-state Output Leakage Current				15	µA
I_{PWR}	Total Quiescent Supply Current[2]	CLKIN = 25 MHz; default settings; C_{LOAD} = 68.5pF		46	68	mA
I_{PWR} Standby	Total Standby Supply Current[2]	STANDBY = $V_{DD}Q$[1], CLKIN = 0 MHz		1	10	µA

Notes: 1. To place the chip in standby mode, first raise STANDBY to HIGH then wait ten master clock cycles before turning off the master clock. Ten master clock cycles are required to place the analog circuitry into standby, low-power mode.
2. Summation of currents for all power supplies.

Table 10: AC Electrical Characteristics

T_A = Ambient = 25°C; Load capacitance = 68.5pF; Master clock frequency = 25 MHz)

Symbol	Definition	MIN	TYP	MAX	Units
FCLK_IN	Input Clock Frequency Clock	1	25	25	MHz
^{t}DUTY_CYCLE	Input Duty Cycle		50		%
^{t}CLK_JITTER	Input Clock Jitter				%
^{t}R	Input Clock Rise Time				ns
^{t}F	Input Clock Fall Time				ns
 ^{t}PLHP ^{t}PHLP	CLKIN to PIXCLK propagation delay LOW-to-HIGH HIGH-to-LOW		 12 13		 ns ns
 ^{t}PLHD ^{t}PHLD	CLKIN to DOUT<:9:0> propagation delay LOW-to-HIGH HIGH-to-LOW		 18 15		 ns ns
^{t}FVSETUP	Setup time for FRAME_VALID before rising edge of PIXCLK		7		ns
^{t}FVHOLD	Hold time for FRAME_VALID after falling edge of PIXCLK		20		ns
^{t}LVSETUP	Setup time for LINE_VALID before rising edge of PIXCLK		8		ns
^{t}LVHOLD	Hold time for LINE_VALID after falling edge of PIXCLK		25		ns
^{t}DSETUP	Setup Time for DOUT before rising edge of PIXCLK		6		ns
^{t}DHOLD	Hold Time for DOUT after falling edge of PIXCLK				ns
^{t}FTOL	Time between rising edge of FRAME_VALID and LINE_VALID		240		ns
^{t}OUTR	DOUT Rise Time		12		ns
^{t}OUTF	DOUT Fall Time		11		ns
^{t}PLHF	CLKIN to FRAME_VALID propagation delay, LOW-to-HIGH		7		ns
^{t}PLHL	CLKIN to LINE_VALID propagation delay, LOW-to-HIGH		7		ns
^{t}PHLF	CLKIN to FRAME_VALID propagation delay, HIGH-to-LOW		4		ns
^{t}PHLL	CLKIN to LINE_VALID propagation delay, HIGH-to-LOW		5		ns

Propagation Delay for FRAME_VALID and LINE_VALID Signals

The LINE_VALID and FRAME_VALID signals change on the same rising master clock edge as the data output. The LINE_VALID goes HIGH on the same rising master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock rising edge as the end of the output of the last valid pixel's data.

As shown in the "Output Data Format" on page 8 and "Output Data Timing" on page 9, FRAME_VALID goes HIGH 6 pixel clocks prior to the time that the first LINE_VALID goes HIGH. It returns LOW 6 pixel clocks after the last LINE_VALID goes LOW.

Note that the data outputs change on the rising edge of the master clock.

Figure 22: Propagation Delays for FRAME_VALID and LINE_VALID Signals

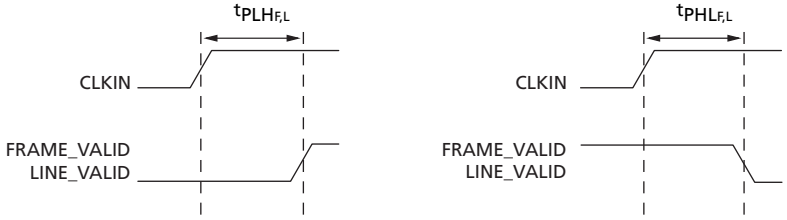


Figure 23: Propagation Delays for PIXCLK and Data Out Signals

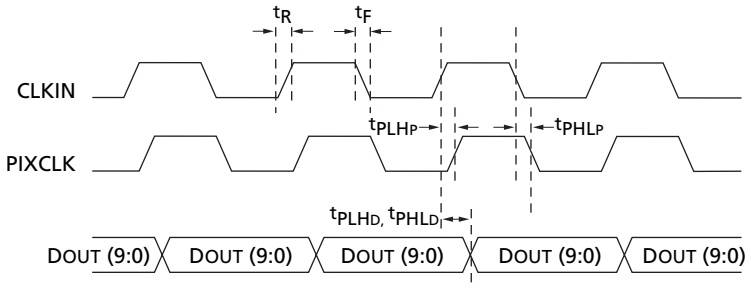
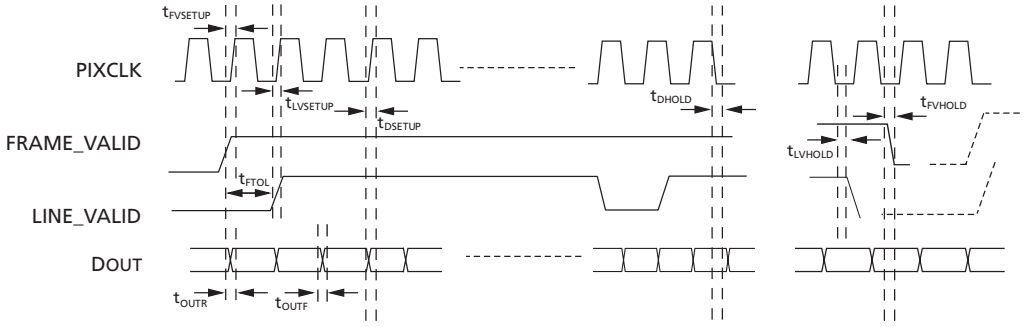


Figure 24: Data Output Timing Diagram



Two-wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

Figure 25: Serial Host Interface Start Condition Timing

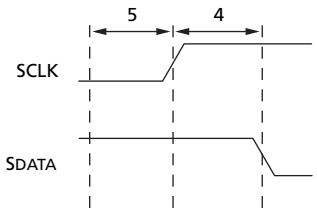
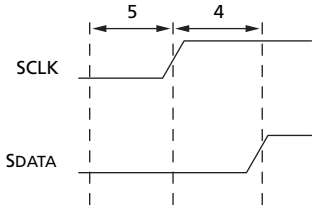
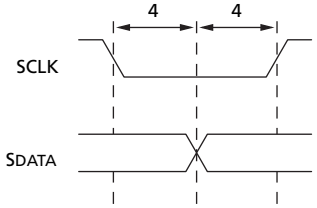


Figure 26: Serial Host Interface Stop Condition Timing



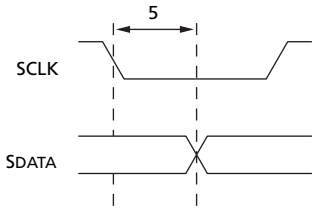
Note: All timing are in units of master clock cycle.

Figure 27: Serial Host Interface Data Timing for Write



Note: SDATA is driven by an off-chip transmitter.

Figure 28: Serial Host Interface Data Timing for Read



Note: SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 29: Acknowledge Signal Timing After an 8-Bit Write to the Sensor

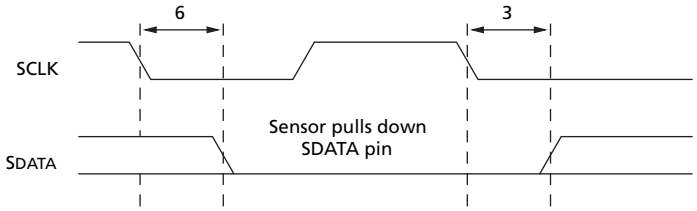
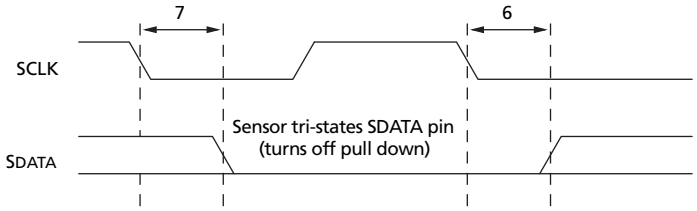


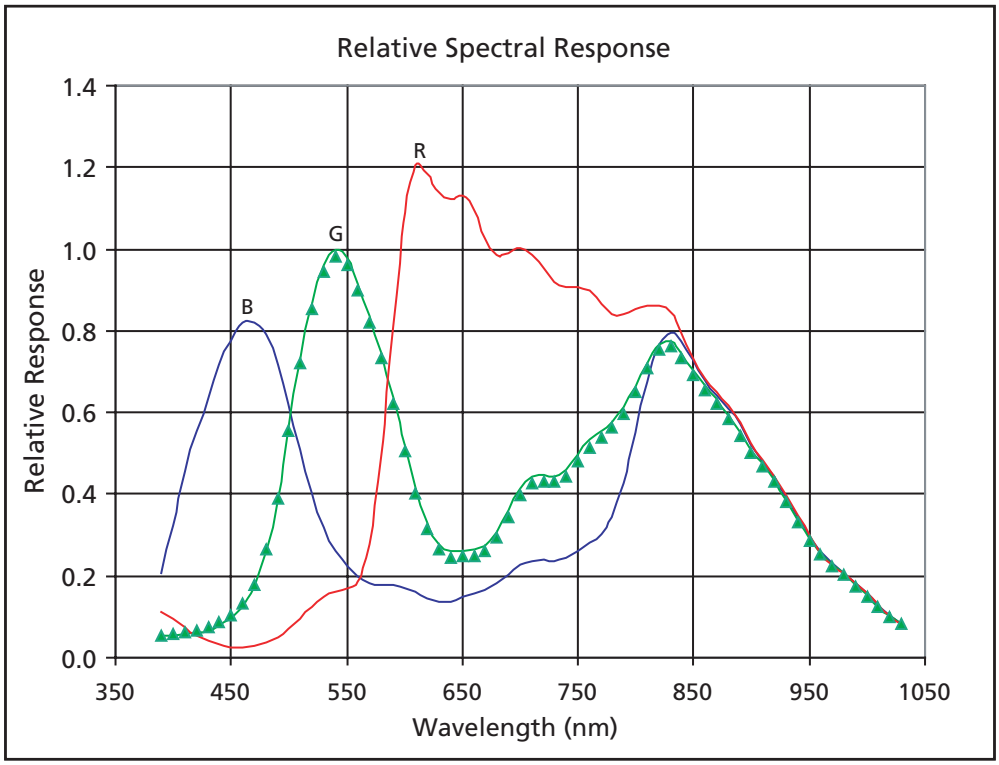
Figure 30: Acknowledge Signal Timing After an 8-Bit Read from the Sensor



Note: After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Spectral Response

Figure 31: Spectral Response



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

Revision History

- Rev. D, Preliminary 1/05
  - Changed master clock frequency to 25 MHz in Table 1, and updated related timings in Table 3
  - Added settings for maximum frame rate and updated description to Table 7, Register Description, on page 19—Reg0x05 and Reg0x07
  - Changed current values and conditions in Table 9, DC Electrical Characteristics, on page 35
  - Updated Table 10, AC Electrical Characteristics, on page 36
  - Removed ICSP package information and ball description

- Rev. C, Preliminary 8/04
  - Updated Table 5, Register List and Default Value, on page 16
  - Updated Table 7, Register Description, on page 19

- Rev. B, Preliminary 7/04
  - Updated Table 1, Key Performance Parameters, on page 1
  - Updated Figure 2 on page 5
  - Replaced Ballout drawing
  - Updated Table 5, Register List and Default Value, on page 16
  - Updated “Electrical Specifications” on page 35

- Rev. A, ... Preliminary3/04
  - Original release