# CYM1461

## 512K x 8 Static RAM Module

### Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 70 ns**
- **Low active power**
  - **825 mW (max.)**
- **Double-sided SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile version (PF)**
  - **Max. height of .315 in.**
- **Small footprint SIP version (PS)**
  - **PCB layout area of 1.5 sq. in.**
- **2V data retention (L version)**

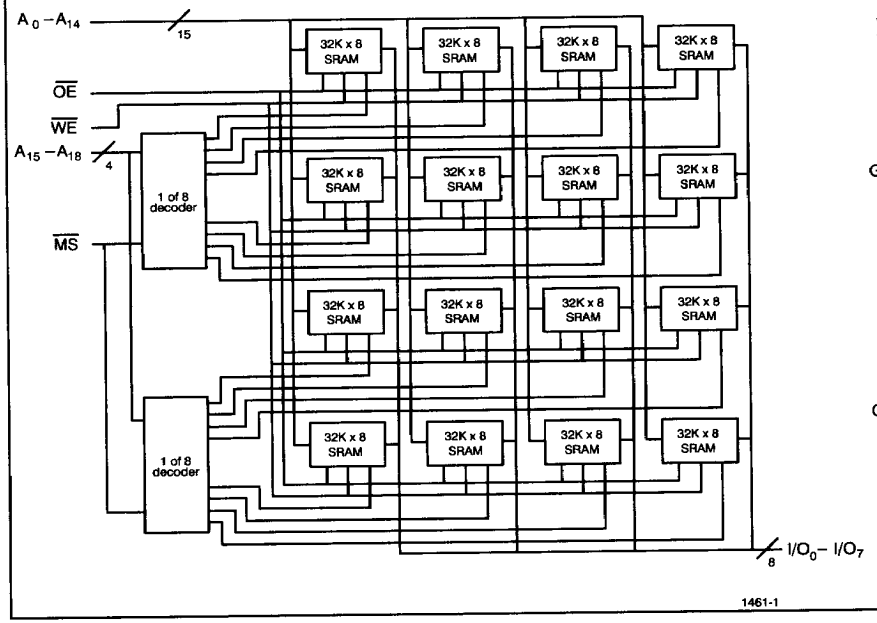
### Functional Description

The CYM1461 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed from sixteen 32K x 8 SRAMs in plastic surface mount packages on an epoxy laminate board with pins. Two choices of pins are available for vertical (PS) or horizontal (PF) through-hole mounting. On-board decoding selects one of the sixteen SRAMs from the high-order address lines keeping the remaining fifteen devices in standby mode for minimum power consumption.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{MS}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{MS}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

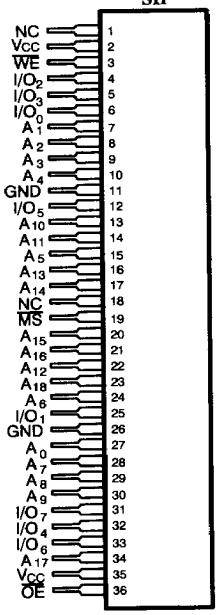
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

### Logic Block Diagram




### Pin Configuration

SIP




### Selection Guide

| | 1461–70 | 1461–85 | 1461–100 |
|---|---|---|---|
| Maximum Access Time (ns) | 70 | 85 | 100 |
| Maximum Operating Current (mA) | 150 | 150 | 150 |
| Maximum Standby Current (mA) | 50 | 50 | 50 |

## Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Supply Voltage to Ground Potential ..... −0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.3V to +7.0V

DC Input Voltage ..... −0.3V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameters | Description | Test Conditions | CYM1461 | | Units |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = −1.0 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 2.0 mA | 0.4 | V | |
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | $V_{CC}$ +0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | −0.3 | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | −20 | +20 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ Output Disabled | −20 | +20 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $\overline{MS}$ ≤ $V_{IL}$ $I_{OUT}$ = 0 mA | | 150 | mA |
| $I_{SB1}$ | Automatic $\overline{MS}$ Power-Down Current | Max. $V_{CC}$, $\overline{MS}$ ≥ $V_{IH}$ Min. Duty Cycle = 100% | | 50 | mA |
| $I_{SB2}$ | Automatic $\overline{MS}$ Power-Down Current | Max. $V_{CC}$ $\overline{MS}$ ≥ $V_{CC}$ − 0.2V, $V_{IN}$ ≥ $V_{CC}$ − 0.2V or $V_{IN}$ ≤ 0.2V | | 32 | mA |

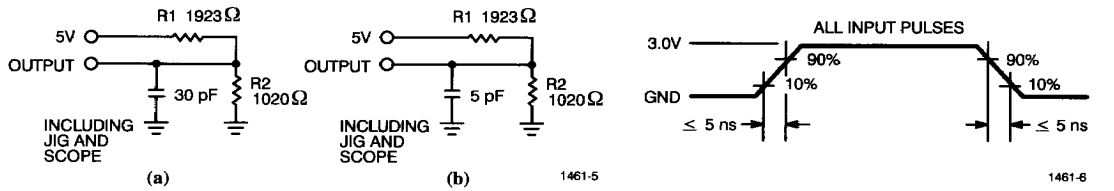
## Capacitance [1]

| Parameters | Description | Test Conditions | Max. | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz $V_{CC}$ = 5.0V | 100 | pF |
| $C_{OUT}$ | Output Capacitance | | 100 | pF |

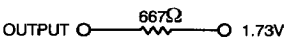
**Notes:**

1. Tested on a sample basis.

## AC Test Loads and Waveforms




Equivalent to: THEVENIN EQUIVALENT



## Switching Characteristics Over the Operating Range [2]

| Parameters | Description | 1461-70 | | 1461-85 | | 1461-100 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 70 | | 85 | | 100 | | ns |
| $t_{AA}$ | Address to Data Valid | | 70 | | 85 | | 100 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 20 | | 20 | | 20 | | ns |
| $t_{AMS}$ | $\overline{MS}$ LOW to Data Valid | | 70 | | 85 | | 100 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 40 | | 50 | | 55 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z | 5 | | 5 | | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [3] | | 35 | | 35 | | 40 | ns |
| $t_{LZMS}$ | $\overline{MS}$ LOW to Low Z [4] | 5 | | 5 | | 5 | | ns |
| $t_{HZMS}$ | $\overline{MS}$ HIGH to High Z [3,4] | | 35 | | 35 | | 40 | ns |
| **WRITE CYCLE** [5] | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 70 | | 85 | | 100 | | ns |
| $t_{SMS}$ | $\overline{MS}$ LOW to Write End | 70 | | 80 | | 85 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 70 | | 80 | | 85 | | ns |
| $t_{HA}$ | Address Hold from Write End | 5 | | 5 | | 5 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 5 | | 5 | | 5 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 60 | | 65 | | 65 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 35 | | 40 | | 45 | | ns |
| $t_{HD}$ | Data Hold from Write End | 5 | | 5 | | 5 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [3] | | 30 | | 35 | | 40 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z | 5 | | 5 | | 5 | | ns |

**Notes:**

2. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
3. $t_{HZOE}$, $t_{HZMS}$, and $t_{HZWE}$ are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
4. At any given temperature and voltage condition, $t_{HZMS}$ is less than $t_{LZMS}$ for any given device. These parameters are guaranteed and not 100% tested.
5. The internal write time of the memory is defined by the overlap of $\overline{MS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected. $\overline{OE}$, $\overline{MS} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{MS}$ transition LOW.
9. Data I/O is HIGH impedance if $\overline{OE} = V_{IH}$.

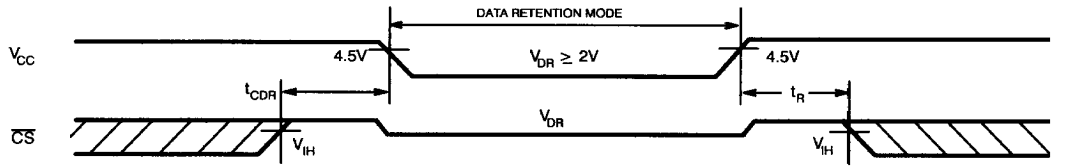
## Data Retention Characteristics (L Version Only)

| Parameter | Description | Test Conditions | CYM1461 | | Units |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $V_{DR}$ | $V_{CC}$ for Retention Data | $V_{CC}$ = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | 2.0 | | V |
| $I_{CCDR}$ | Data Retention Current | | | 300 | µA |
| $t_{CDR}$ [12] | Chip Deselect to Data Retention Time | | 0 | | ns |
| $t_R$ [12] | Operation Recovery Time | | $t_{RC}$ [10] | | ns |

**Notes:**

10. $t_{RC}$ = Read Cycle Time.
11. If $\overline{MS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
12. Guaranteed, not tested.

## Data Retention Waveform

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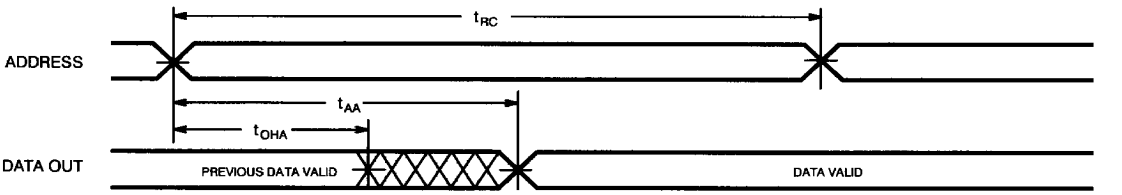
## Switching Waveforms

**Read Cycle No. 1** [7, 8]

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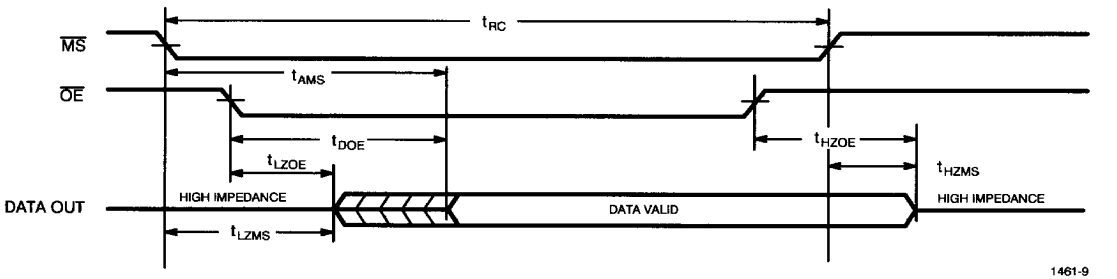
**Read Cycle No. 2** [8, 9, 10]

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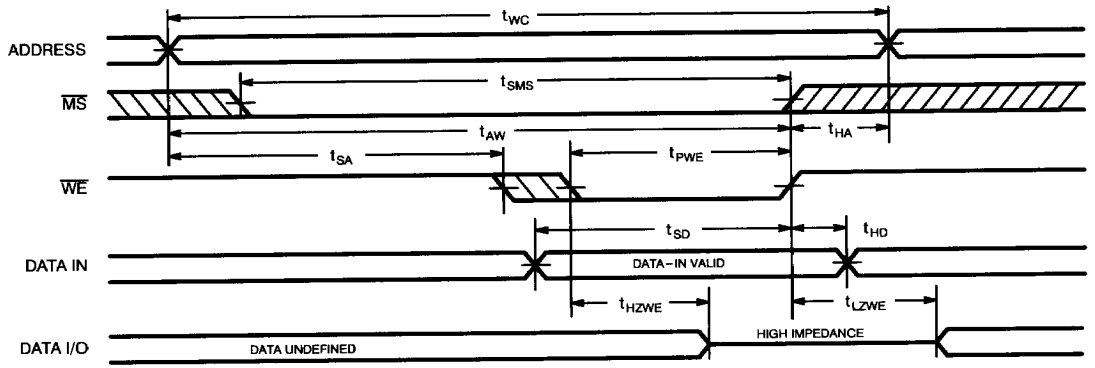
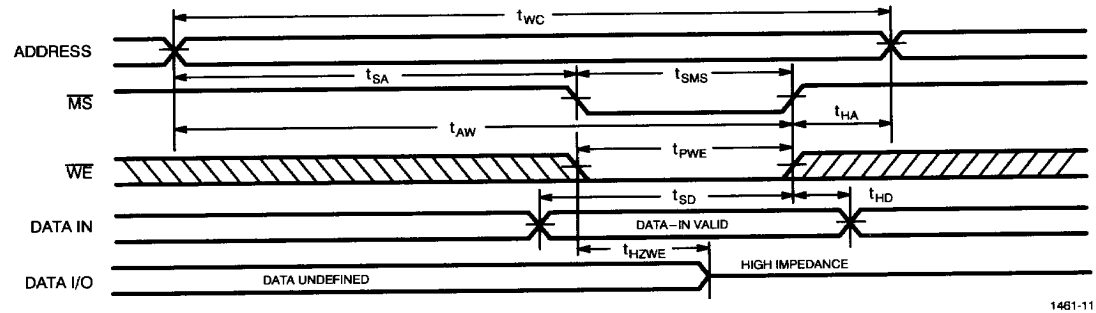
## Switching Waveforms (continued)

**Write Cycle No. 2** [8, 9]




**Write Cycle No. 2 ($\overline{MS}$ Controlled)** [11]




9 MODULES

## Truth Table

| $\overline{MS}$ | $\overline{WE}$ | $\overline{OE}$ | Input/Outputs | Mode |
|---|---|---|---|---|
| H | X | X | High Z | Deselect/Power-Down |
| L | H | L | Data Out | Read |
| L | L | X | Data In | Write |
| L | H | H | High Z | Deselect |

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## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|
| 70 | CYM1461PS-70C | PS01 | Commercial |
| | CYM1461LPS-70C | | |
| | CYM1461PF-70C | PF01 | |
| | CYM1461LPF-70C | | |
| 85 | CYM1461PS-85C | PS01 | Commercial |
| | CYM1461LPS-85C | | |
| | CYM1461PF-85C | PF01 | |
| | CYM1461LPF-85C | | |
| 100 | CYM1461PS-100C | PS01 | Commercial |
| | CYM1461LPS-100C | | |
| | CYM1461PF-100C | PF01 | |
| | CYM1461LPF-100C | | |