

CMM-2 2.0 to 6.0 GHz GaAs MMIC Amplifier

- ❑ High Gain: 12.5 dB
- ❑ Low Current: 35 mA @ 8V
- ❑ Small Size: 39 x 30 mils
- ❑ Directly Cascadable
- ❑ Self-Biased
- ❑ Single Power Supply

Celeritek CMM-2 GaAs MMIC Amplifier

The CMM-2 is a 2 to 6 GHz GaAs MMIC amplifier. It is a two-stage feedback design which draws low current from a single power supply. Applications include oscillator buffers, RF and IF gain blocks and isolation amplifiers.

The CMM-2 is a very small chip which provides 12 dB of gain and 10 dBm of power from an 8 volt supply. The chip is directly cascadable with no additional components. The circuit's self-biasing feature provides excellent performance from a 5 to 8 volt supply. Care must be taken to isolate the input and output from external DC voltages. Good performance is available up to 12 GHz.

Celeritek MMIC's are fabricated on ion-implanted GaAs material with gold-based metalization. The FET gates are sub-half micron, tee cross-section construction. Air bridges are used for top level interconnection. Silicon nitride serves as capacitor dielectric and surface passivation. Mesa resistors are used for feedback and bias functions.

The CMM-2 is available in chip form. It can be screened to meet commercial, military Hi-Rel or space grade reliability requirements. Custom wafer qualification for special electrical and/or reliability requirements is also available.



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Specifications ($T_A = 25^\circ\text{C}$, $V_{DD} = 8\text{V}$, 2-6 GHz)

Parameters	Units	Min	Typ	Max
Small Signal Gain	dB	11.0	12.5	
Gain Flatness	$\pm\text{dB}$		0.5	1.0
Input VSWR	—		1.7:1	2.0:1
Output VSWR	—		2.0:1	2.5:1
Reverse Isolation	dB	25	30	
Gain Variation Over Temperature (-55 to $+95^\circ\text{C}$)	$\pm\text{dB}$		0.75	1.00
Noise Figure	dB		5.5	7.0
1 dB Gain Compression Power Output	dBm	8	10	
Current	mA		35	50

Absolute Maximum Ratings

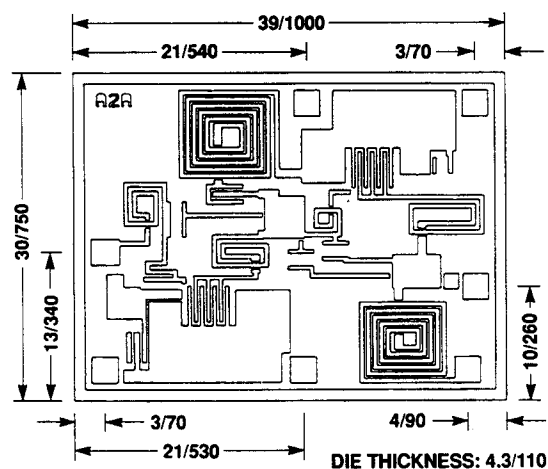
Parameter	Rating
Voltage	11V
Continuous Power Dissipation	1.25 W
Channel Temperature	$+175^\circ\text{C}$
Storage Temperature	-65°C to $+175^\circ\text{C}$
Mounting Temperature	$+320^\circ\text{C}$
Input Power	$+20\text{ dBm}$
θ_{JC}	60°C/W

Die Attach and Bonding Procedures

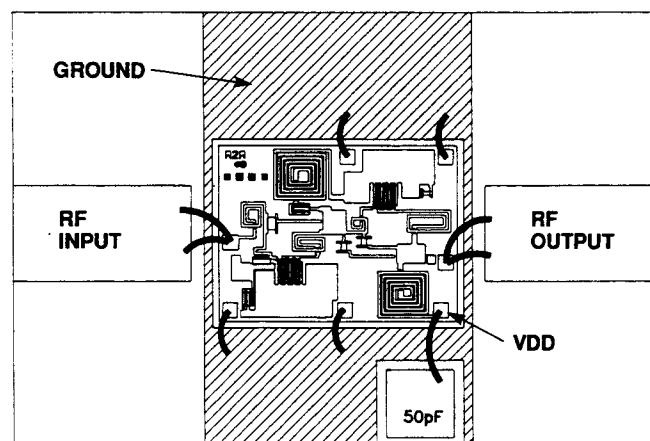
Die Attach: Conductive epoxy or preform die attach is recommended. For preform die attach: Preform: AuSn (80% Au, 20% Sn); Stage Temperature: 290°C , $\pm 5^\circ\text{C}$; Handling Tool: Tweezers; Time: 1 min or less.

Wire Bonding: Wire Size: 0.7 to 1.0 mil in diameter (pre-stressed); Thermocompression bonding is preferred over thermosonic bonding. For thermocompression bonding: Stage Temperature: 250°C ; Bond Tip Temperature: 150°C ; Bonding Tip Pressure: 18 to 40 gms depending on size of wire.

Chip Diagram (Dimensions in Mils/ μm)

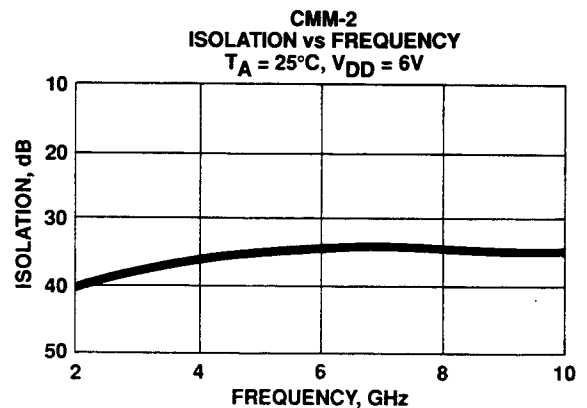
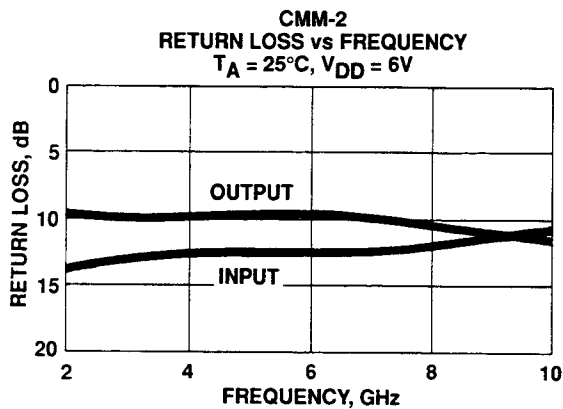
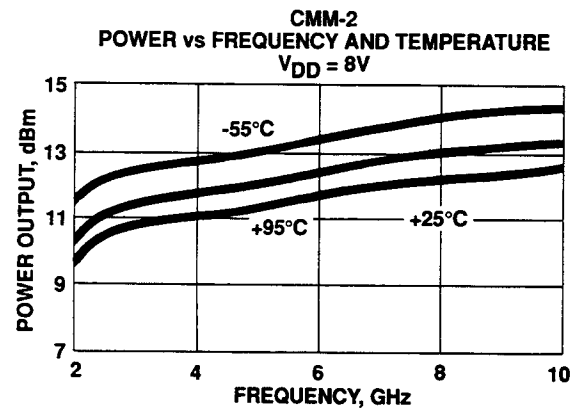
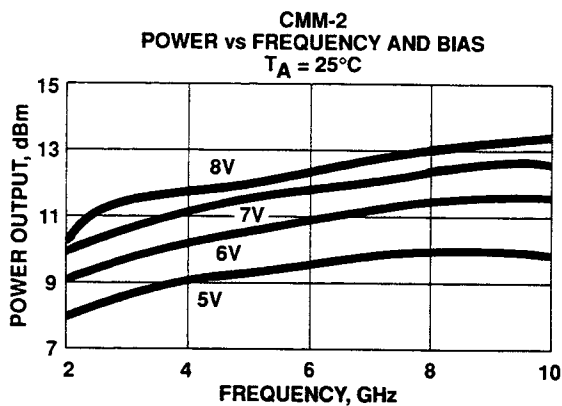
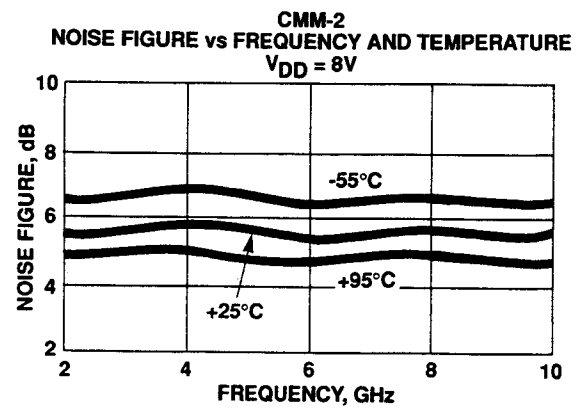
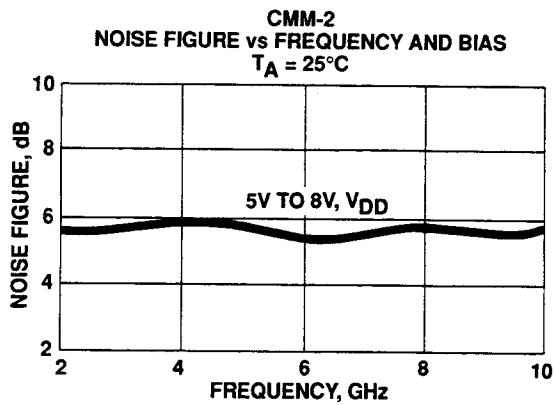
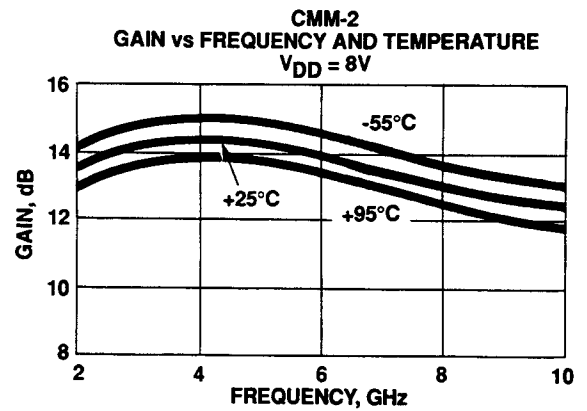
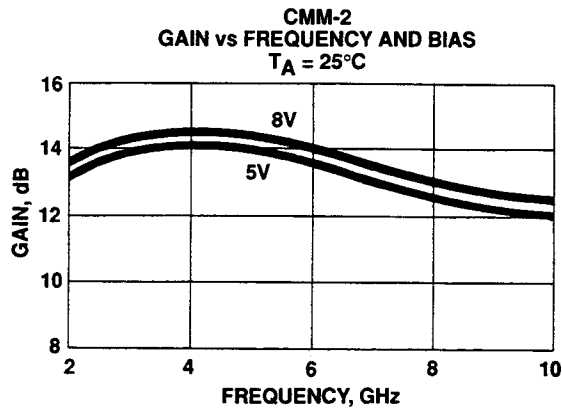


Bonding Diagram



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Typical Performance ($T_A = 25^\circ\text{C}$)



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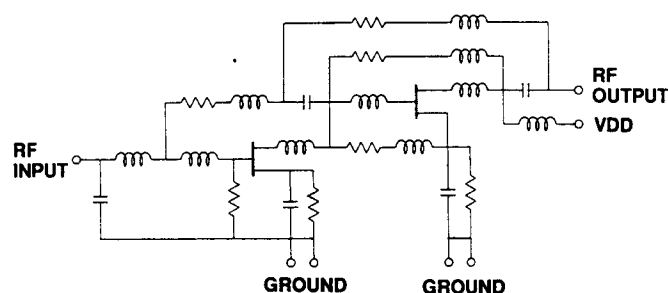
Typical Scattering Parameters, $T_A = 25^\circ\text{C}$ (S-Parameters Include Bonding Wire Parasitics)

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$V_{DD} = 8\text{V}$

Frequency (GHz)	S_{11} (dB)	S_{11} (Mag)	S_{11} (Ang)	S_{21} (dB)	S_{21} (Mag)	S_{21} (Ang)	S_{12} (dB)	S_{12} (Mag)	S_{12} (Ang)	S_{22} (dB)	S_{22} (Mag)	S_{22} (Ang)
2.0	-14.2	0.194	-147.7	13.4	4.677	23.2	-40.6	0.009	26.6	-9.8	0.323	-166.0
3.0	-13.4	0.223	-163.4	14.1	5.070	-34.5	-37.7	0.013	24.1	-10.8	0.290	178.1
4.0	-12.6	0.234	-176.2	14.2	5.129	-78.4	-36.2	0.015	30.0	-10.1	0.312	160.5
5.0	-12.6	0.228	176.6	14.1	5.070	-116.1	-35.9	0.016	19.8	-10.0	0.317	143.7
6.0	-12.7	0.232	169.6	13.9	4.955	-150.9	-35.8	0.016	19.1	-9.8	0.322	129.2
7.0	-12.5	0.238	163.5	13.4	4.677	177.5	-35.6	0.017	21.2	-10.0	0.316	116.0
8.0	-12.1	0.248	157.0	13.0	4.467	148.1	-35.2	0.017	17.0	-10.5	0.298	104.5
9.0	-11.8	0.258	149.4	12.7	4.315	120.5	-35.0	0.018	14.7	-11.3	0.272	94.4
10.0	-11.6	0.264	137.8	12.4	4.169	94.3	-35.0	0.018	9.9	-12.1	0.247	84.4

Equivalent Circuit



Wafer Qualification Procedure

100% DC Test
100% Visual Insp.

Sample Mechanical
Evaluation

Sample Circuit
Performance Tests*

NF, Gain, P_{-1} dB,
VSWR

Reliability
Assessment

*80% of tested samples must meet
specifications for wafer acceptance.

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Specifications subject to change.

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