EEPROM 128K x 8 EEPROM

AVAILABLE AS MILITARY SPECIFICATIONS

- MIL-STD-883 (Non-Compliant)

FEATURES

- High speed: 150, 200 and 250 ns
- Data Retention: 10 Years
- Low power Dissipation, active current (20mW/MHZ(typ)), standby current (100uW(max))
- Single +5V (±5%) power supply
- Data Polling and Ready/Busy Signals
- Erase/Write Endurance (100,000 cycles in page mode)
- Software Data protection Algorithm
- Data Protection Circuitry during power on/off
- Hardware Data Protection with RES pin
- Automatic Programming:
  Automatic Page Write: 10ms (max)
  128 Byte page size
  Automatic Page Write: 10ms (max)

OPTIONS MARKING

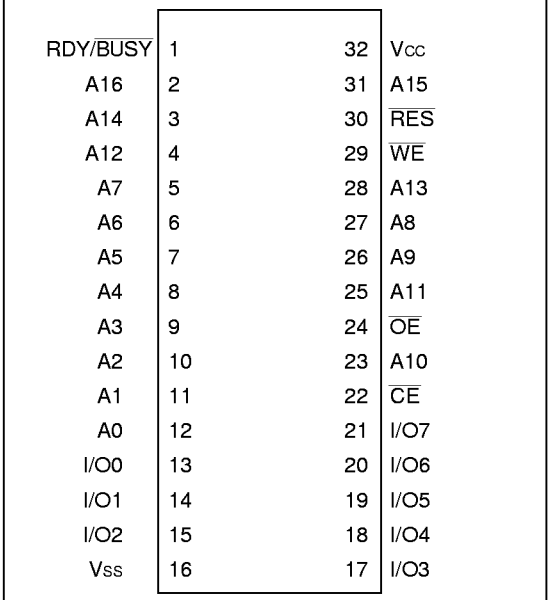
- Timing

150ns access	-15
200ns access	-20
250ns access	-25

- Packages

Ceramic Flat Pack	F	305
Radiation Tolerant Ceramic Flat Pack	SF	306

PIN ASSIGNMENT(Top View)
32-PIN FLATPACK



GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS58C1001 is a 1 Megabit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 131,072 x 8 bits. The AS58C1001 is capable of in system electrical Byte and Page reprogrammability.

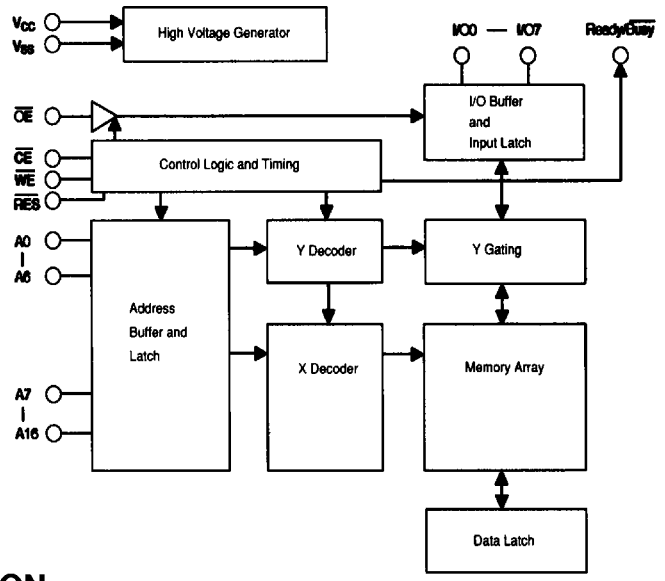
The AS58C1001 achieves high speed access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The AS58C1001 has a 128-Byte Page Programming function to make its erase and write operations faster. The AS58C1001 features Data Polling and a Ready/Busy signal to indicate completion of erase and programming operations.

The AS58C1001 provides several levels of data protection. Hardware data protection is provided with the RES pin, in addition to noise protection on the WE signal and write inhibit during power on and off. Software data protection is implemented using JEDEC Optional Standard algorithm.

The AS58C1001 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

FUNCTIONAL BLOCK DIAGRAM



MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/ $\overline{Busy}$	I/O
Read	Vil	Vil	Vih	Vh	High-Z	Dout
Standby	Vih	X	x	x	High-Z	High-z
Write	Vil	Vih	Vil	Vh	High-Z	Din
Deselect	Vil	Vih	vih	Vh	High-Z	High-Z
Write Inhibit	X	X	Vih	X	-	-
	X	Vil	X	X	-	-
Data Polling	Vil	Vil	Vih	Vh	Vol	Data Out (I/O7)
Program	X	X	X	Vil	High-Z	High-Z

FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 128 Bytes of data to be written into the EEPROM in a single cycle and allows the undefined data within 128 Bytes to be written corresponding to the undefined address (A_0 to A_6). Loading the first Byte of data, the data load window of 30 µs opens for the second. In the same manner each additional Byte of data can be loaded within 30 µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, the EEPROM enters erase and write automatically and only the input data can be written into the EEPROM. In Page mode the data can be written and accessed 10^5 times per page, and in Byte mode 10^4 times per Byte.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling allows the status of the EEPROM to be determined. If the EEprom is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is preforming a Write operation.

Write Protection

(1) Noise protection: Noise on a write cycle will not act as a trigger with a $\overline{WE}$ pulse of less than 20ns.

(2) Write inhibit: Holding $\overline{OE}$ low, $\overline{WE}$ high or $\overline{CE}$ high, inhibits a write cycle during power on/off.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

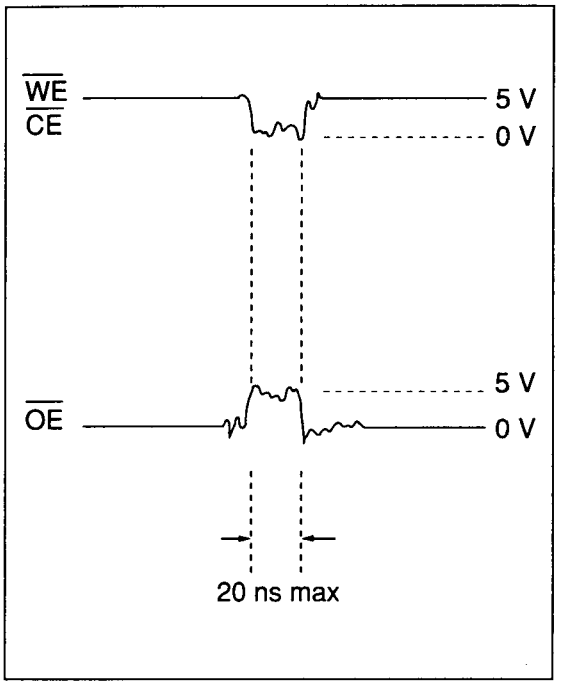
Write/Erase Endurance and Data Retention

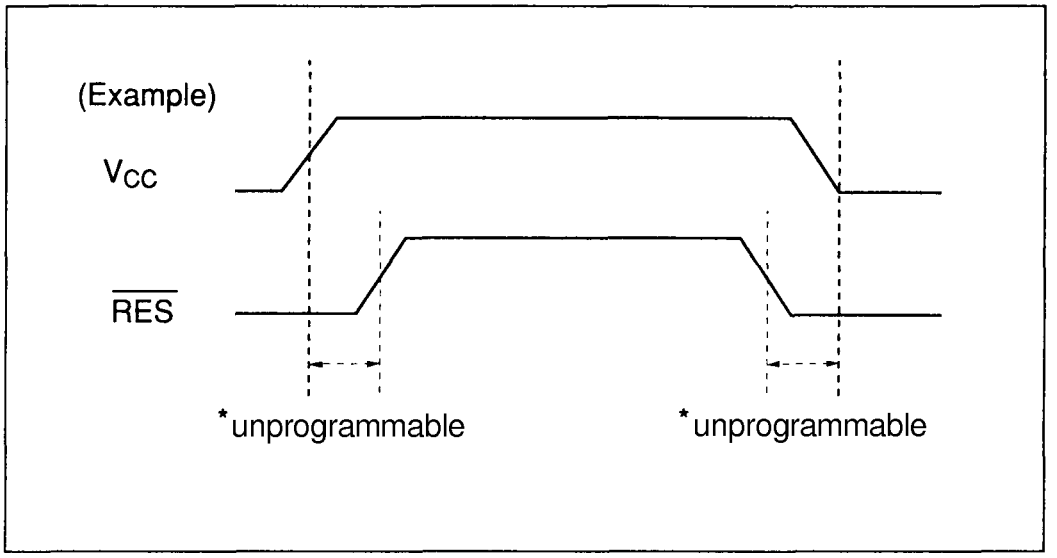
The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the AS58C1001 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the AS58C1001 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.





FUNCTIONAL DESCRIPTION (continued)

Data Protection (continued)

2. Data protection at V_{CC} on/off.
   When $\overline{RES}$ is low, the EEProm cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during programming because it does not provide a latch function.
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable, standby or readout state by using a CPU reset signal to $\overline{RES}$ pin.
   In addition, when $\overline{RES}$ is kept high at V_{CC} on/off timing, the input level of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}$ =VCC or $\overline{OE}$ =Low or $\overline{WE}$ =V_{CC} level.

3. **Software data protection**
   To protect unintentional programming caused by noise generated by external circuits, AS58C1001 has a Software data protection function. In Software data protection mode, 3 bytes of data must be input before the Write data. These Bytes can switch the Non-Protection mode to the Protection mode.

Address	Data
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	A0

Write Address Write Data (Normal Data Input)

The Software data protection mode can be cancelled by inputting the following 6 Bytes. This changes the AS58C100s to the Non-Protection mode and it can write data normally. When the data is input during the cancelling cycle, the data cannot be written.

Address	Data
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	80
⇓	⇓
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	20

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Input Relative to Vss ..... 0.6 to 7.0V[1]
Voltage on V_{CC} Supply Relative to V_{SS} ..... 0.5[2] to 7.0V[1]
Storage Temperature ..... -65 to +150°c
Operating Temperature ..... -55 to +125°c

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_C ≤ 125°C; V_{CC} = 5V ± 5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1.0	V	10
Input Low (Logic 0) Voltage[3]		V_{IL}	0.3	0.8	V	2
Input Volyage		VH	Vcc-0.5	Vcc+1.0	V	9
Input Leakage Current[4]	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}		2	µA	4
Output Leakage Current	Output Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}		2	µA	
Output High Voltage	I_{OH} = -400µA	V_{OH}	2.4		V	
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}		0.4	V	

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	Iout = 0mA Cycle=1µS, Duty=100%	I_{CC3}	15	12	10	mA	
	Iout = 0mA Cycle = 200 nS, Duty = 100%		60	50	45		
Power Supply Current: Standby	$\overline{CE}$ =V_{CC}	I_{CC1}	20	20	20	µA	
	$\overline{CE}$ =V_{IH}	I_{CC2}	1	1	1	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	Cin		6	pF	
Output Capacitance	V_{IN} = 0	Co		12	pF	

AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(-55°C ≤ T_C ≤ 125°C; V_{CC} = 5V ± 5%)

Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 1.5 V, 1.5 V

Item	Symbol	Test Condition	-15		-20		-25		Units
			Min.	Max.	Min	Max	Min	Max	
Address Access Time	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL} $\overline{WE}$=V_{IH}	-	150		200		250	ns
Chip Enable Access Time	t_{CE}	$\overline{OE}$=V_{IL} $\overline{WE}$=V_{IH}	-	150	—	200		250	ns
Output Enable Access Time	t_{OE}	$\overline{CE}$=V_{IL} $\overline{WE}$=V_{IH}	10	75	10	75	10	75	ns
Output Hold to Address Change	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL} $\overline{WE}$=V_{IH}	0	-	0		0		ns
Output Disable to High-Z	t_{DF}	$\overline{CE}$=V_{IL} $\overline{WE}$=V_{IH}	0	50	0	50	0	50	ns
	t_{DFR}	$\overline{CE}$=$\overline{OE}$=V_{IL} $\overline{WE}$=V_{IH}	0	350	0	350	0	350	ns
$\overline{RES}$ to Output Delay	t_{RR}	$\overline{CE}$=$\overline{OE}$=V_{IL} $\overline{WE}$=V_{IH}	0	450	0	450	0	450	ns

AC ELECTRICAL CHARACTERISTICS FOR SOFTWARE DATA PROTECTION CYCLE OPERATION

ITEM	SYMBOL	MIN	TYP.	MAX	UNITS
Byte Load Cycle Time	t_{BLC}	0.55	-	30	µs
Write Cycle Time	t_{WC}	10	-	-	ms

AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

ITEM	SYMBOL	MIN	TYP.	MAX	UNITS
Output Enable Hold Time	t_{OEH}	0	-	-	ns
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns
Write Start time	t_{DW}	150	-	-	ns
Write Cycle Time	t_{WC}	-	-	10	ms

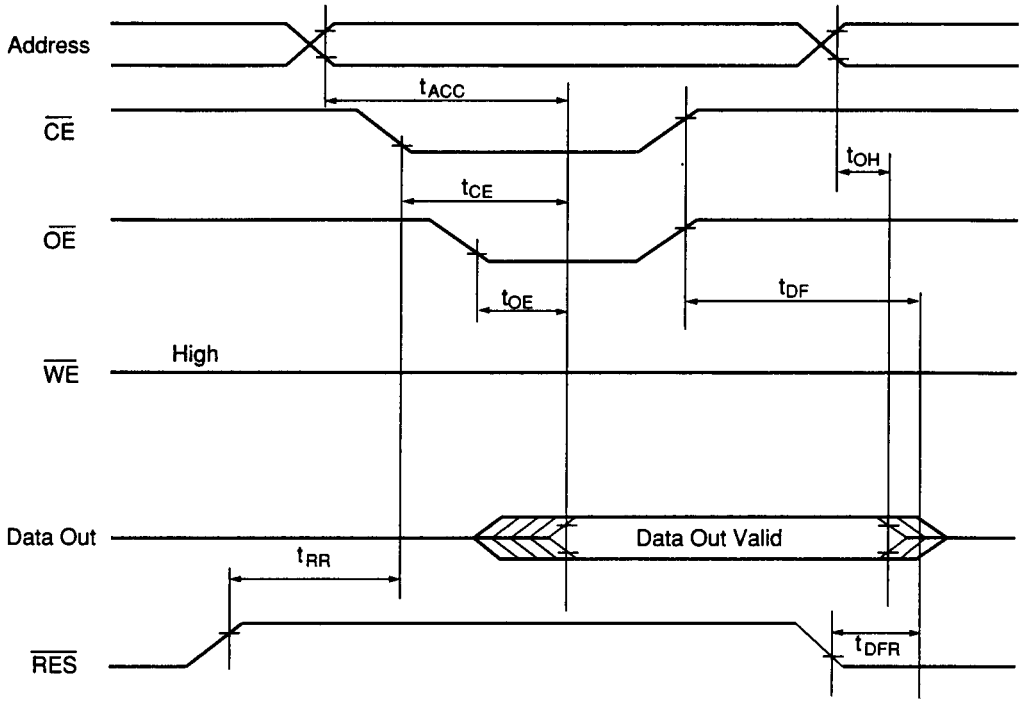
AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

ITEM	SYMBOL	MIN.[6]	TYP.	MAX	UNITS
Address Setup Time	t_{AS}	0	-	-	ns
Write Enable to Write Setup Time	t_{WS}[8]	0	-	-	ns
Chip Enable to Write Setup Time	t_{CS}[7]	0	-	-	ns
Write Pulse Width	t_{WP}[7]	250	-	-	ns
	t_{CW}[9]	250	-	-	ns
Address Hold Time	t_{AH}	150	-	-	ns
Data Setup Time	t_{DS}	100	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Write Enable Hold Time	t_{WH}[8]	0	-	-	ns
Chip Enable Hold Time	t_{CH}[7]	0	-	-	ns
Out Enable to Write Setup Time	t_{OES}	0	-	-	ns
Output Enable Hold Time	t_{OEH}	0	-	-	ns
Data Latch Time	t_{DL}	200	-	-	ns
Write Cycle Time	t_{WC}	10	-	-	ms
Byte Load Window	t_{BL}	100	-	-	µs
Byte Load Cycle	t_{BLC}	0.55	-	30	µs
Time to device Busy	t_{DB}	120	-	-	ns
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs
VCC to $\overline{RES}$ Setup Time	t_{RES}"	1	-	-	µs

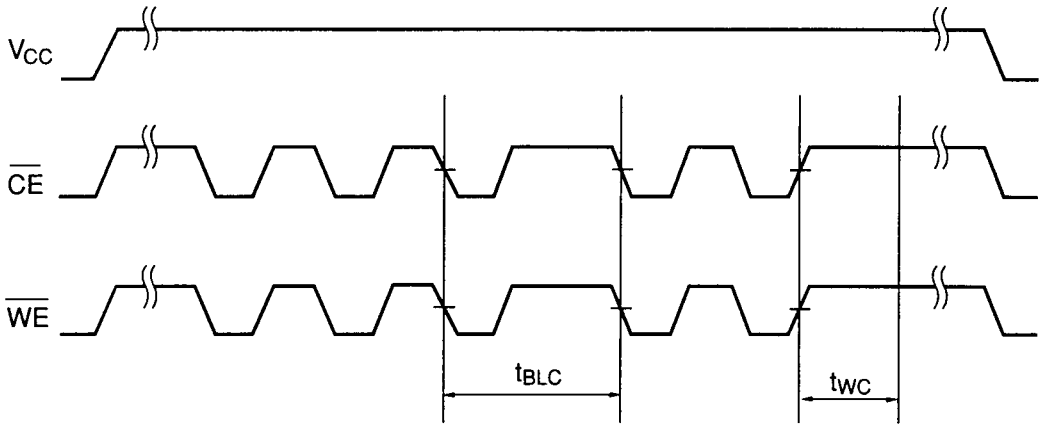
AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

ITEM	SYMBOL	MIN.[6]	TYP.	MAX	UNITS
Address Setup Time	t_{AS}	0	-	-	ns
Chip Enable to Write Setup Time	t_{CS}[7]	0	-	-	ns
Write Pulse Width	t_{CW}[8]	250	-	-	ns
	t_{WP}[7]	250	-	-	ns
Address Hold Time	t_{AH}	150	-	-	ns
Data Setup Time	t_{DS}	100	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Chip Enable Hold Time	t_{CH}[7]	0	-	-	ns
Out Enable to Write Setup Time	t_{OES}	0	-	-	ns
Output Enable Hold Time	t_{OEH}	0	-	-	ns
Write Cycle Time	t_{WC}	10	-	-	ms
Byte Load Window	t_{BL}	100	-	-	µs
Time to Device Busy	t_{DB}	120	-	-	ns
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs
Vcc to $\overline{RES}$ Setup Time	t_{RES}[11]	1	-	-	µs

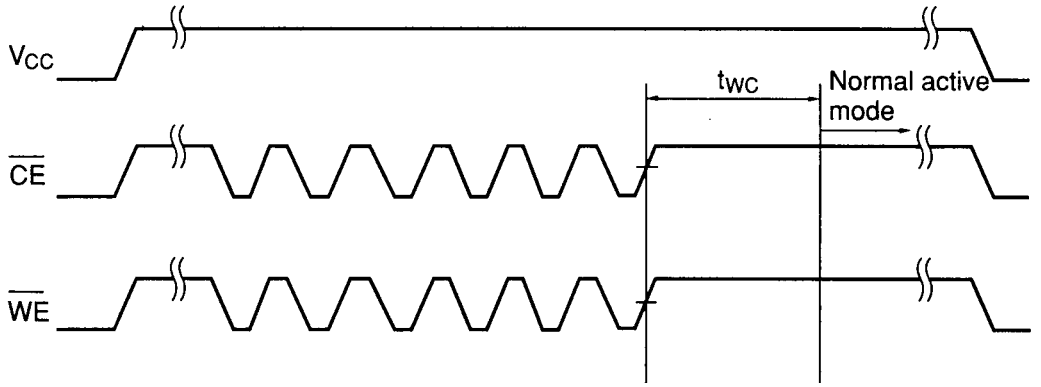
■ READ TIMING WAVEFORM



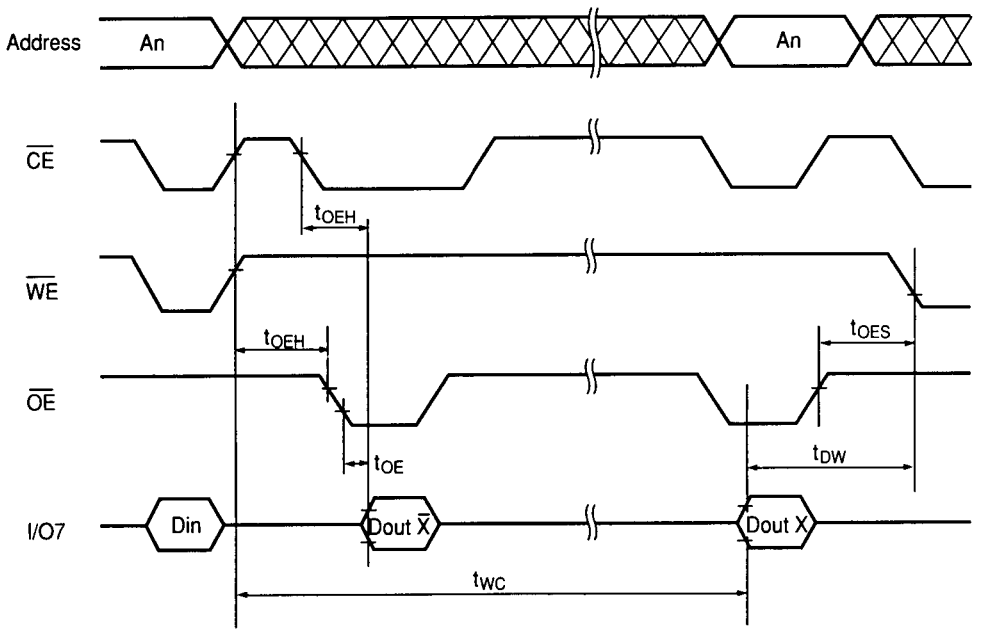
■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Protection Mode)



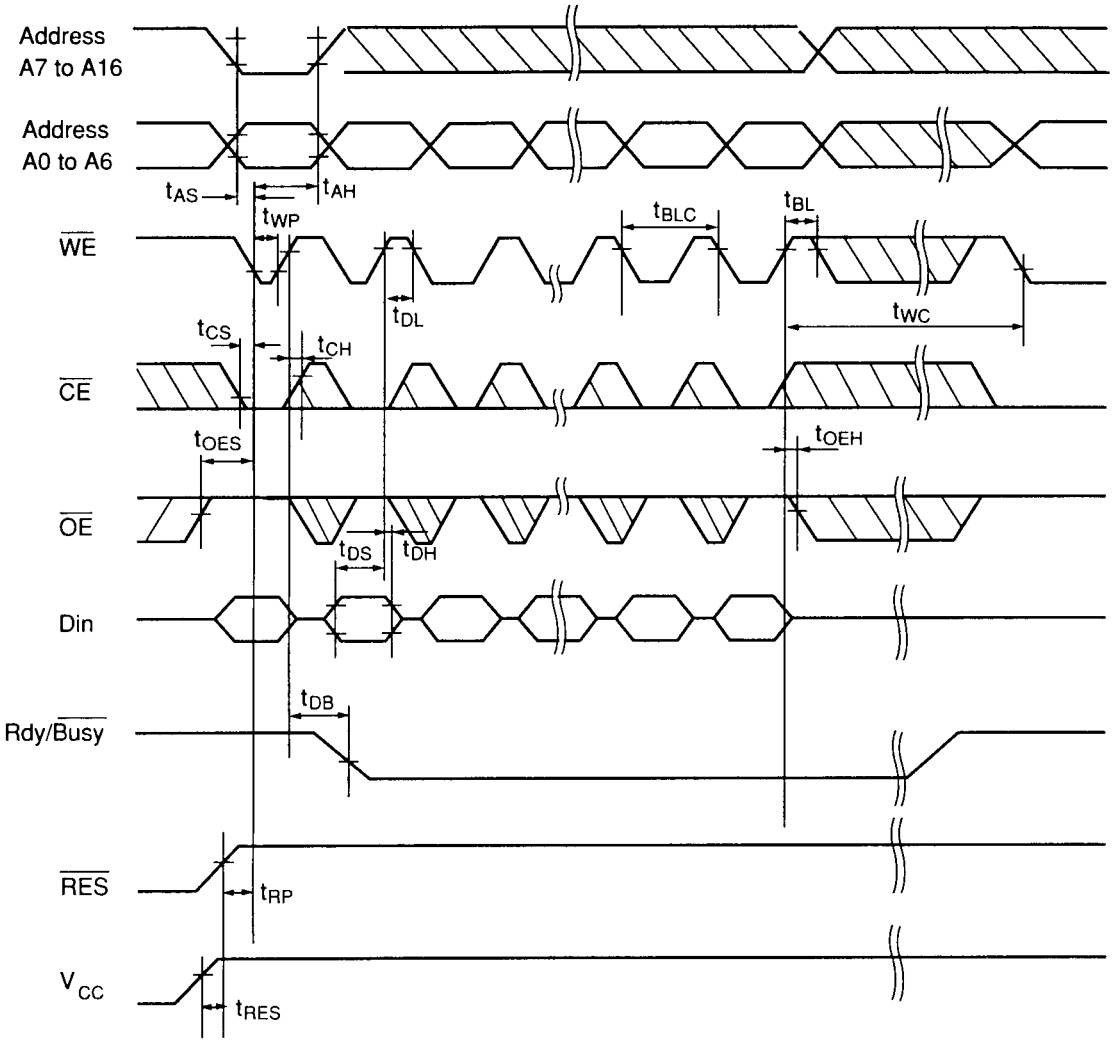
■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Non-Protection Mode)



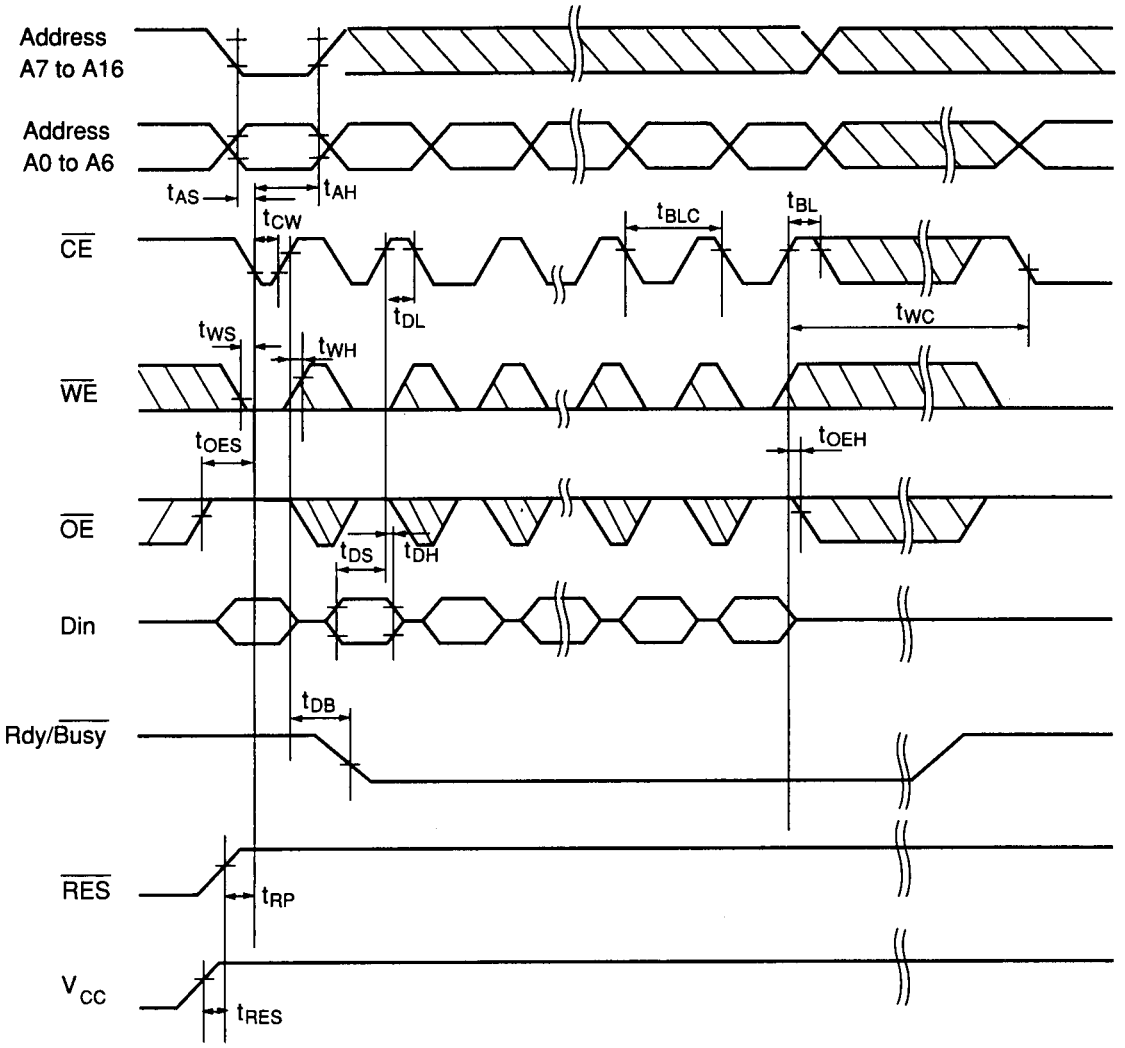
■ $\overline{\text{DATA}}$ POLLING TIMING WAVEFORM



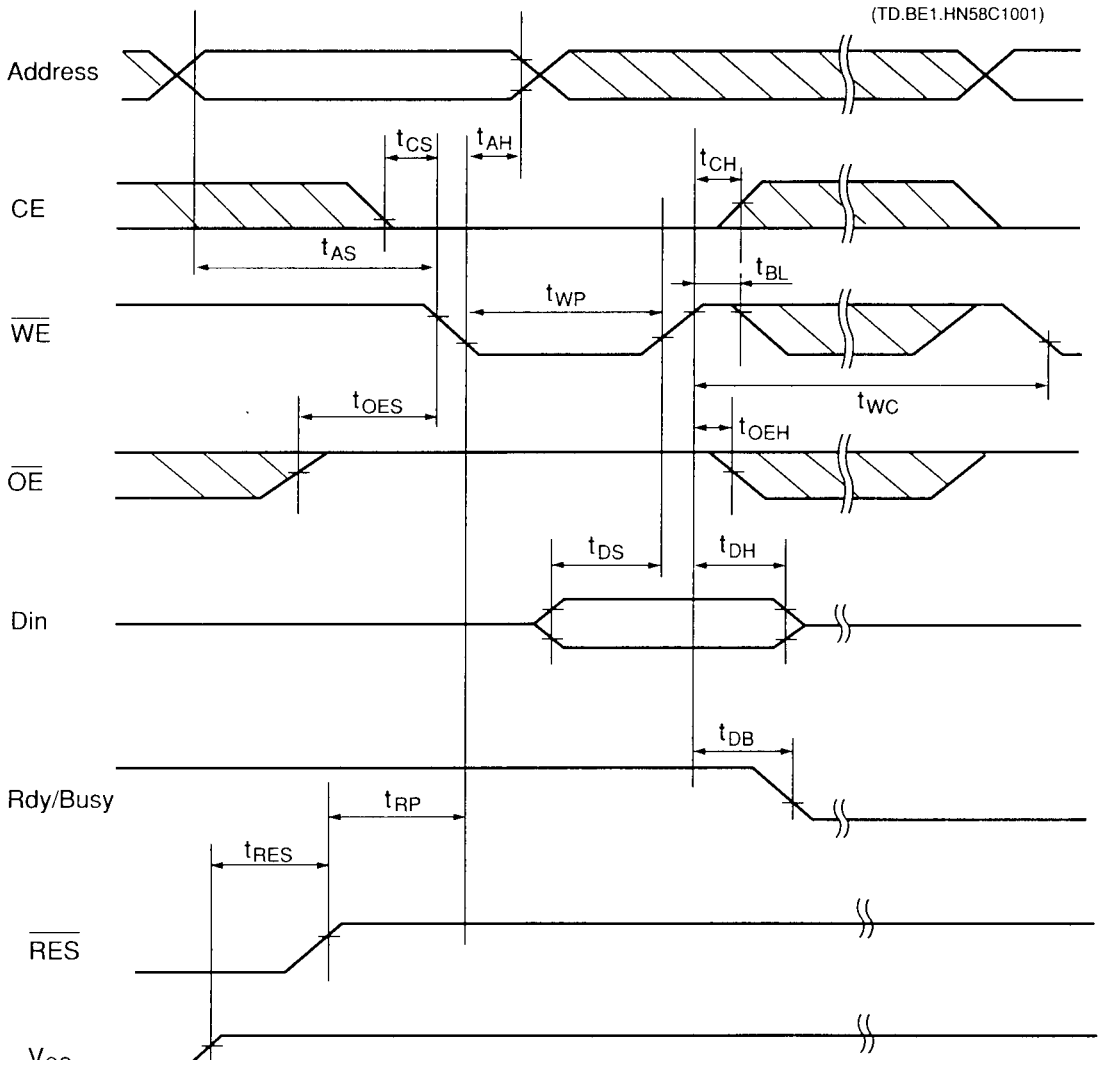
■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



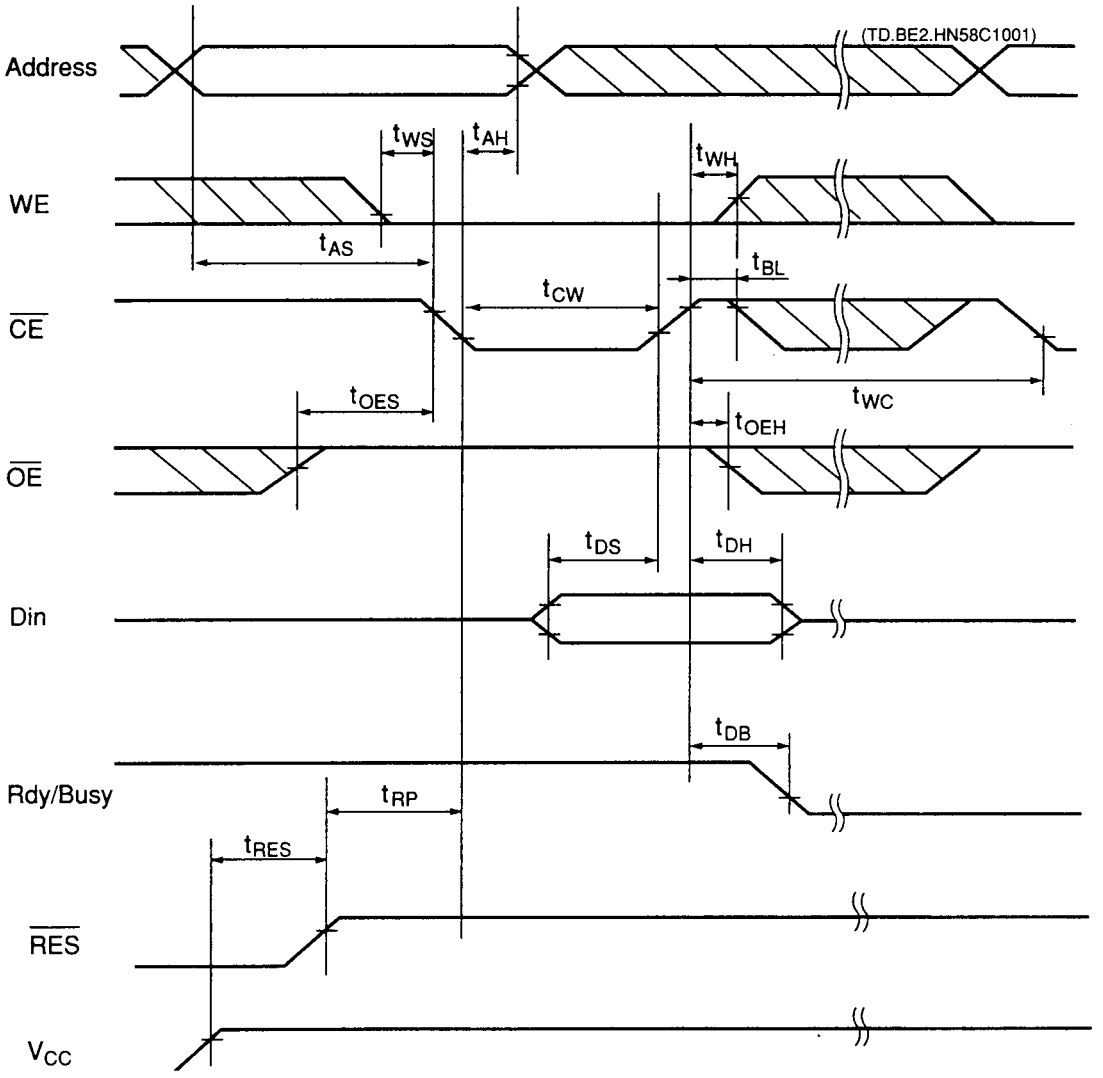
■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



AC TEST CONDITIONS

Input pulse levels	0v to 3v
Input rise and fall times	≤ 20ns
Input timing reference level	1.5v
Output reference level	1.5v
Output load	See figure 1

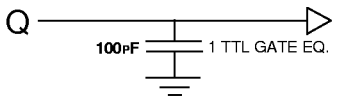


FIG. 1 OUTPUT LOAD EQUIVALENT

NOTES

1. Relative to V_{SS}
2. Vin min=-3.0v for pulse widths ≤50ns
3. V.L min=-1.0v for pulse widths ≤50ns
4. ILi on $\overline{RES}$=100ua MAX
5. t_{OF} is defined as the time at which E the output becomes an open circuit and data is no longer driven
6. Use this device in longer cycle than this value
7. $\overline{WE}$ controlled operation
8. $\overline{CE}$ controlled operation
9. $\overline{RES}$ pin
10. $\overline{RES}$ pin V_{IH} is V_H
11. Reference only, not tested

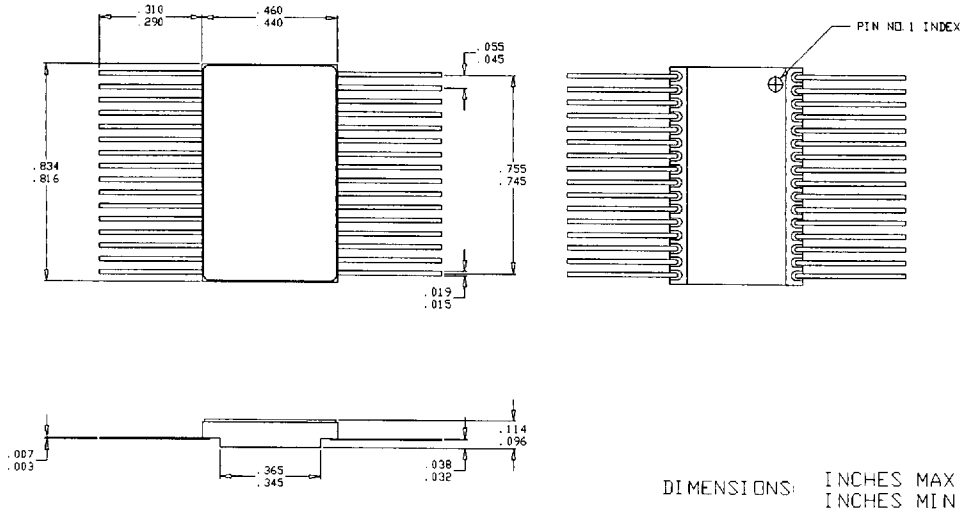
ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

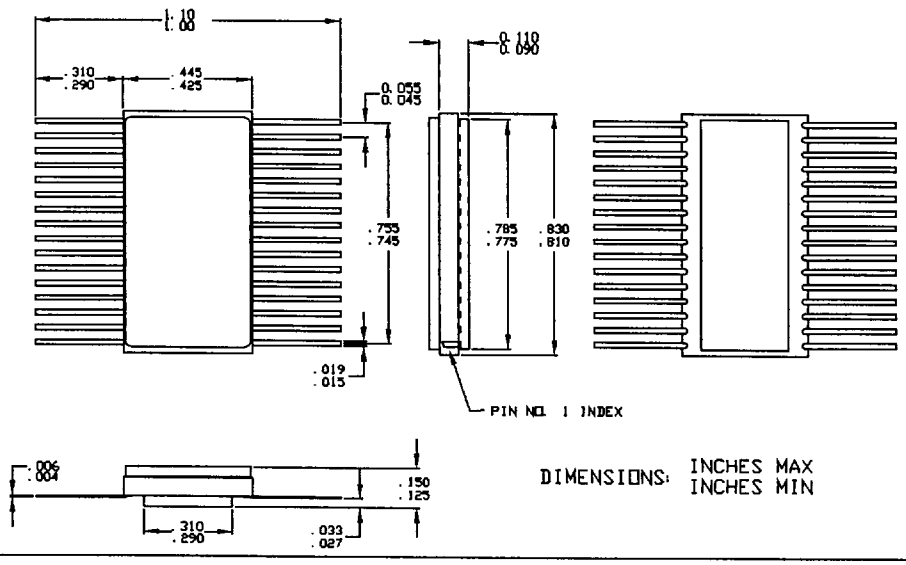
** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.

PACKAGE NO. 304
32 FP



DIMENSIONS: INCHES MAX
INCHES MIN

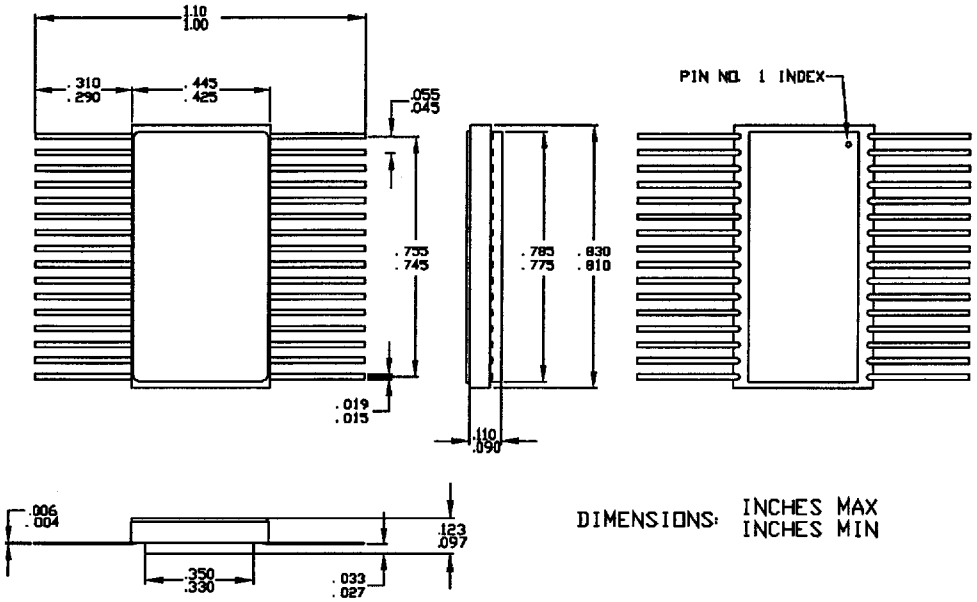
PACKAGE NO. 305
36 FP



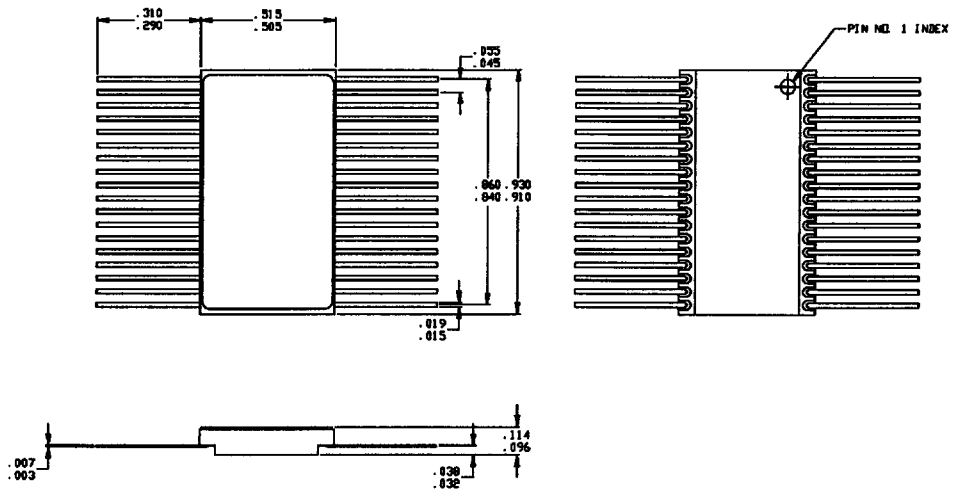
DIMENSIONS: INCHES MAX
INCHES MIN

PKG-17

PACKAGE NO. 306
36 FP



PACKAGE NO. 307
36 FP



PKG-18