

PNP switching transistor

2N4403

FEATURES

- High current (max. 600 mA)
- Low voltage (max. 40 V).

APPLICATIONS

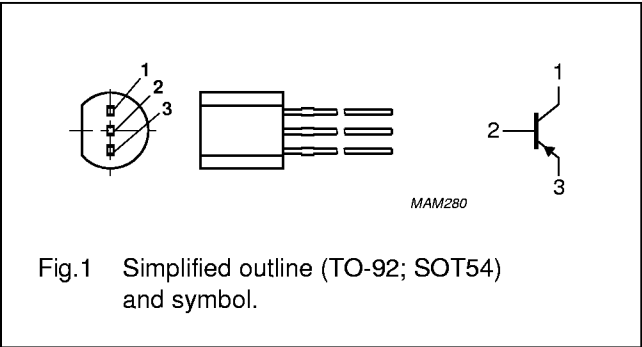
- Industrial and consumer switching applications.

DESCRIPTION

PNP switching transistor in a TO-92; SOT54 plastic package. NPN complement: 2N4401.

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	—	−40	V
V_{CEO}	collector-emitter voltage	open base	—	−40	V
V_{EBO}	emitter-base voltage	open collector	—	−5	V
I_C	collector current (DC)		—	−600	mA
I_{CM}	peak collector current		—	−800	mA
I_{BM}	peak base current		—	−200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	—	630	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		—	150	°C
T_{amb}	operating ambient temperature		−65	+150	°C

PNP switching transistor

2N4403

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	200	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

$T_j = 25\ ^\circ\text{C}$ unless otherwise specified.

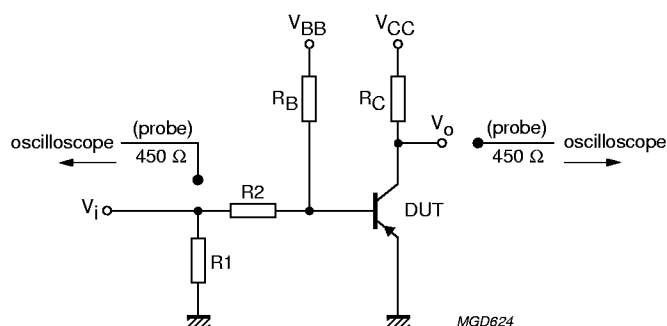
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0\ \text{mA}$; $V_{CB} = -40\ \text{V}$	—	—50	nA
I_{EBO}	emitter cut-off current	$I_C = 0\ \text{mA}$; $V_{EB} = -5\ \text{V}$	—	—50	nA
h_{FE}	DC current gain	$V_{CE} = -1\ \text{V}$; see Fig.2 $I_C = -0.1\ \text{mA}$	30	—	
		$I_C = -1\ \text{mA}$	60	—	
		$I_C = -10\ \text{mA}$	100	—	
		$V_{CE} = -2\ \text{V}$ $I_C = -150\ \text{mA}$ $I_C = -500\ \text{mA}$	100 20	300 —	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -150\ \text{mA}$; $I_B = -15\ \text{mA}$	—	—400	mV
		$I_C = -500\ \text{mA}$; $I_B = -50\ \text{mA}$	—	—750	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = -150\ \text{mA}$; $I_B = -15\ \text{mA}$	—	—950	mV
		$I_C = -500\ \text{mA}$; $I_B = -50\ \text{mA}$	—	—1.3	V
C_c	collector capacitance	$I_E = I_E = 0$; $V_{CB} = -10\ \text{V}$; $f = 1\ \text{MHz}$	—	8.5	pF
C_e	emitter capacitance	$I_C = I_C = 0$; $V_{EB} = -500\ \text{mV}$; $f = 1\ \text{MHz}$	—	30	pF
f_T	transition frequency	$I_C = -20\ \text{mA}$; $V_{CE} = -10\ \text{V}$; $f = 100\ \text{MHz}$	200	—	MHz
Switching times (between 10% and 90% levels); see Fig.3					
t_{on}	turn-on time	$I_{Con} = -150\ \text{mA}$; $I_{Bon} = -15\ \text{mA}$; $I_{Boff} = 15\ \text{mA}$	—	40	ns
t_d	delay time		—	15	ns
t_r	rise time		—	30	ns
t_{off}	turn-off time		—	350	ns
t_s	storage time		—	300	ns
t_f	fall time		—	50	ns

PNP switching transistor

2N4403



Fig.2 DC current gain; typical values.



$V_i = -9.5 \text{ V}$; $T = 500 \mu\text{s}$; $t_p = 10 \mu\text{s}$; $t_r = t_f \leq 3 \text{ ns}$.
 $R_1 = 68 \Omega$; $R_2 = 325 \Omega$; $R_B = 325 \Omega$; $R_C = 160 \Omega$.
 $V_{BB} = 3.5 \text{ V}$; $V_{CC} = -29.5 \text{ V}$.
 Oscilloscope: input impedance $Z_i = 50 \Omega$.

Fig.3 Test circuit for switching times.

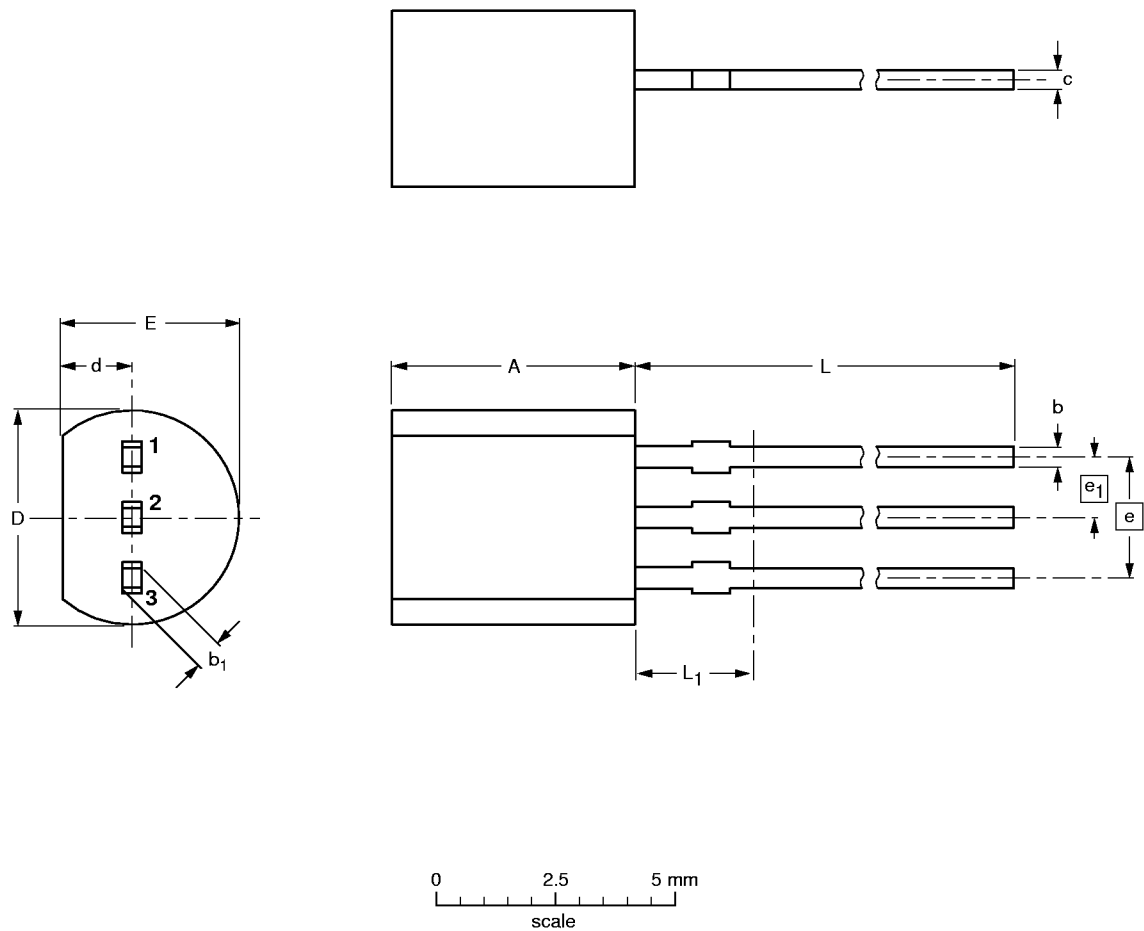
PNP switching transistor

2N4403

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28