PCI 9656 Blue Book Revision 0.90b Corrections

This document details several corrections to the PCI 9656 Blue Book, revision 0.90b. Please review these corrections before proceeding with your design.

1. Toggling IDDQEN# At Power On Time

When using the PCI 9656AD, external logic is required on the IDDQEN# pin to configure the PCI buffers for proper operation. This external logic is *not* required when using the PCI 9656BA. The requirement for this logic is not included in the Blue Book.

PCI 9656AD IDDQEN#

To put the PCI 9656AD into its IDDQ state, hold the IDDQEN# input signal (ball A10) in its asserted state.

To configure the PCI 9656AD for normal operation, during initialization the IDDQEN# input signal must transition from its asserted state to its de-asserted state prior to PCI RST# de-assertion. This causes the silicon to configure its PCI I/O buffers for proper bus operation. After this transition completes, hold IDDQEN# in its de-asserted state.

Note. For CompactPCI Hot Swap applications, IDDQEN# must be held in its de-asserted state during pre-charge. As a result, CompactPCI Hot Swap applications require that IDDQEN# transition from its de-asserted state to its asserted state after pre-charge completes, and then transition back to its de-asserted state prior to Local PCI RST# de-assertion.

PCI 9656BA IDDQEN#

To put the PCI 9656BA into its IDDQ state, hold the IDDQEN# input signal (ball A10) in its asserted state.

To configure the PCI 9656BA for normal operation, hold IDDQEN# in its de-asserted state.

Note. For applications that use the PCI 9656BA's PCI Power Management D3cold PME Generation feature, de-assert IDDQEN# by tying it directly to the 2.5V power source for Vcore. The PCI 9656BA uses IDDQEN# to sense both when Vcore is going away to prepare to enter the D3cold state and when Vcore is coming back to prepare to leave the D3cold state. Do not tie IDDQEN# to the 2.5V power source for 2.5Vaux, and do not tie it to the 3.3V power source for either Vring or Card_Vaux.

Even though the PCI 9656BA does not require any transitioning of its IDDQEN# input signal for proper PCI bus operation, transitioning the PCI 9656BA's IDDQEN# in accordance with the PCI 9656AD IDDQEN# requirements, above, will have no effect on PCI 9656BA operation. As a result, the PCI 9656BA can be substituted for the PCI 9656AD in existing designs without needing to remove the external IDDQEN# transitioning logic.

Sample Circuit Designs Supporting All Silicon Versions

The following circuit diagrams come directly from the schematics of two PLX hardware reference design boards that have been validated empirically. The first is an example circuit for designs that

do not need to support CompactPCI Hot Swap. The second is an example for designs that do need to support CompactPCI Hot Swap.

Note. These circuit diagrams are provided as examples only. It is the designer's responsibility to create circuitry that meets the above stated IDDQEN# toggling requirements for their particular design.

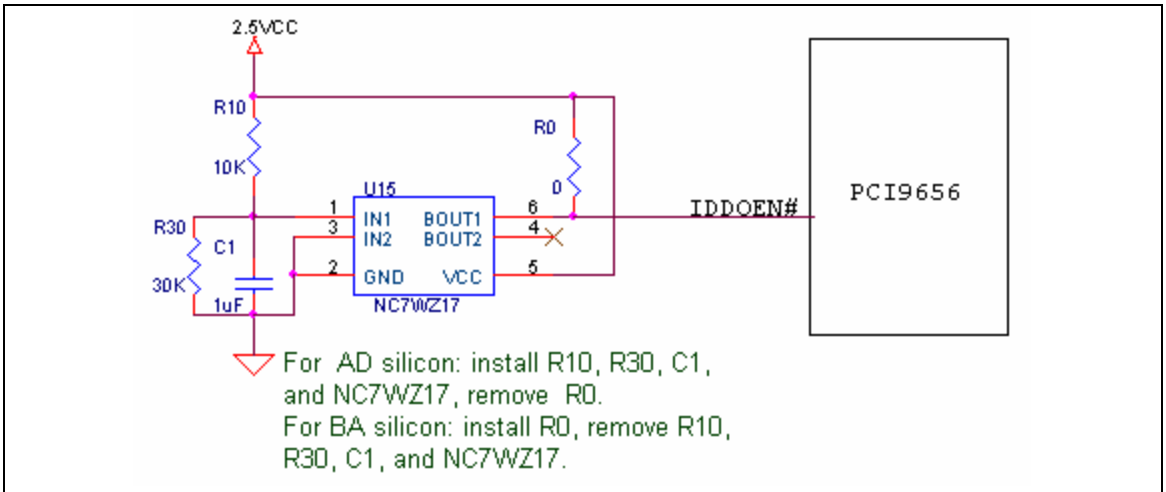

Figure 1. IDDQEN# Toggling Circuitry Example For Non-CompactPCI Hot Swap Designs

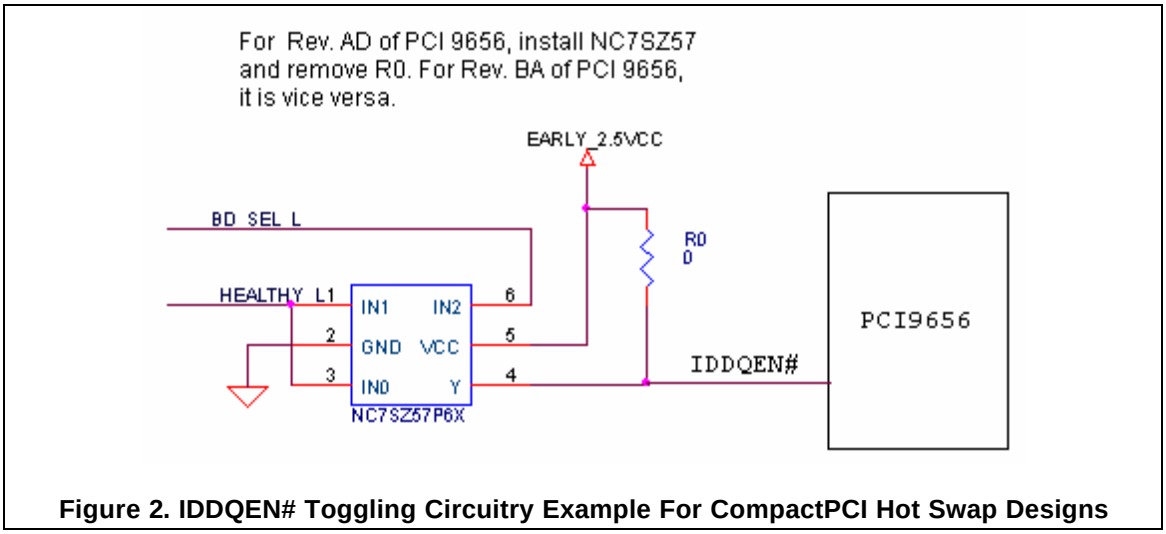

Figure 2. IDDQEN# Toggling Circuitry Example For CompactPCI Hot Swap Designs

2. USERi Pull-Up/Pull-Down At Power Up Time

When using the PCI 9656, an external pull-up or pull-down resistor is required on the USERi pin to configure the chip for the desired PCI bus behavior during chip initialization. A pull-up resistor configures the chip to issue PCI Retries during initialization [high = retry], and a pull-down resistor configures the chip to do nothing on the PCI bus during initialization. This is true for both the PCI 9656AD and the PCI 9656BA. The description in the Blue Book regarding this is incorrect for these chip revisions.

The following text replaces sections 2.4.1.2 and 4.4.1.2 of the Blue Book. Note that these sections of the Blue Book look very similar to what is below. The key difference is that the polarity of USERi is incorrectly reversed in the Blue Book descriptions. Follow the polarity in the description below. Changes from the Blue Book are underlined.

2.4.1.2/4.4.1.2 Local Initialization

As stated in *PCI r2.*2, Section 3.5.1.1:

"If the target is accessed during initialization-time, it is allowed to do any of the following:

1. Ignore the request (except if it is a boot device). This results in a Master Abort.

2. Claim the access and hold in wait sates until it can complete the request, not to exceed the end of initialization-time.

3. Claim the access and terminate with [PCI] Retry."

The PCI 9656 supports Option 1 (*Initially Not Respond*), and Option 3 (*Initially Retry*), above. For CompactPCI Hot Swap live insertion systems, the preferred method for the silicon is usually not to respond to PCI Configuration accesses during initialization. For legacy systems, Retries are usually preferred for compatibility reasons. However, it is ultimately the designer's choice of which option to use.

The PCI 9656 determines the option to use as follows:

The USERi pin is sampled at the rising edge RST# to determine the selected PCI Bus response mode during local initialization. <u>If USERi is low (through an external 1K ohm pull-down resistor), the PCI 9656 does not respond to PCI activity until the device's Local Bus initialization is complete.</u> This results in a Master Abort (the preferred method for CompactPCI Hot Swap systems). <u>If USERi is high (through an external 1K—4.7K ohm pull-up resistor), the PCI 9656 responds to PCI accesses with PCI Retry cycles until the device's Local Bus initialization is complete.</u> Local Bus initialization is complete when the Local Init Status bit is set (LMISC1[2]=1).

The LMISC1[2] bit can be programmed in one of three ways:

1. By a Local Bus master writing a 1 directly to LMISC1[2].

2. By the serial EEPROM specifying a value of 1 for LMISC1[2] during a serial EEPROM load.

3. If a Local Bus Master is not present and either a serial EEPROM is not present or a blank serial EEPROM is present, the PCI 9656 reverts to its power on/reset default register values and sets this bit. (Refer to Table 2-18 on page 2-9.)

During run time, USERi can be used as a general purpose input as described in the Tables 12-10, 12-11, and 12-12, for the M, C, and J mode Local Bus pins.

Refer to Section 9, "CompactPCI Hot Swap" for specifics on using this feature in *PICMG 2.1, R2.0* systems.

3. EEDI/EEDO Pull-Up When Local Processor Present But EEPROM Not Present

When using the PCI 9656, if initialization is to be performed by a Local Bus master and no serial EEPROM is present, the EEDI/EEDO pin must *not* be pulled down. This is true for both the PCI 9656AD and the PCI 9656BA. The description in the Blue Book regarding this is vague.

Tables 2-18 and 4-18 of the Blue Book make no mention of a pull-up or pull-down resistor on the EEDI/EEDO pin when a Local Processor is present but an EEPROM is not present. The correct requirement is that the EEDI/EEDO pin must be either be left floating or pulled up with a 1K-ohm or greater value resistor when an EEPROM is not present. In any case, the pin must *not* be pulled down.

The following shows the corrected entry of Tables 2-18 and 4-18:

Table 1. Serial EEPROM Guidelines

Local Processor	Serial EEPROM	System Boot Condition
		...
Present	None	The Local Processor programs the PCI 9656 registers, then sets the Local Init Status bit (LMISC1[2] = 1). A 1K ohm or greater pull-up resistor on EEDI/EEDO is recommended, but not required. The EEDI/EEDO pin already has an internal pull-up (ref. Table 12-1). ***Note:*** *Some systems may avoid configuring devices that do not complete configuration accesses within 2^{25} PCI clocks after RST# has been de-asserted. In addition, some systems may hang if Direct Slave reads and writes are immediately retried. The value of the Direct Slave Retry Delay Clocks (LBRD0[31:28]) may resolve the hang by delaying assertion of the STOP# signal by the PCI 9656.*
		...

4. Updated Electrical Specifications

The following table updates Blue Book Table 13-5 for both the PCI 9656AD and the PCI 9656BA. Changes from the Blue Book are underlined.

Table 2. Electrical Characteristics Over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}[1]	Output High Voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12.0 mA	2.4	-	V
V_{OL}[1]	Output Low Voltage		I_{OL} = 12.0 mA	-	0.4	V
V_{OH}[2]	Output High Voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0 mA	2.4	-	V
V_{OL}[2]	Output Low Voltage		I_{OL} = 24.0 mA	-	0.4	V
V_{IH}	Input High Level	-	-	2.0	5.5	V
V_{IL}	Input Low Level	-	-	-0.5	0.8	V
V_{OH3}	PCI 3.3V Output High Voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -500 µA	0.9 V_{DD}	-	V
V_{OL3}	PCI 3.3V Output Low Voltage		I_{OL} = 1500 µA	-	0.1 V_{DD}	V
V_{IH3}	PCI 3.3V Input High Level	-	-	0.5 V_{DD}	V_{DD}+0.5	V
V_{IL3}	PCI 3.3V Input Low Level	-	-	-0.5	0.3 V_{DD}	V
I_{II}	Input Leakage Current	V_{SS} = V_{IN} = V_{DD}, V_{DD} = Max		-10	+10	µA
I_{LPC}[3]	DC Current Per Pin During Pre-charge	V_P = 0.8 to 1.2V		-	1.0	mA
I_{OZ}	Three-State Output Leakage Current	V_{DD} = Max		-10	+10	µA
I_{DD}[4] (I/O Ring)	Power Supply Current for I/O Ring	I/O Ring V_{DD} = 3.6V, PCLK = 66MHz, LCLK = 66MHz		-	95	mA
I_{DD} (Core)	Power Supply Current for Core	Core V_{DD} = 2.63V, PCLK = 66MHz, LCLK = 66MHz		-	185	mA
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max, V_{IN} = GND or V_{CC}		-	50	µA

Notes:

1. For 12 mA I/O or output cells (Local Bus side).
2. For 24 mA I/O or output cells (Local Bus side).
3. I_{LPC} is the DC current flowing from VDD to Ground during pre-charge, as both PMOS and NMOS devices remain on during pre-charge. It is not the leakage current flowing into or out of the pin under pre-charge.
4. 40 Local Bus side I/Os switching simultaneously and 76 PCI side I/Os switching simultaneously.

5. PCI Arbiter Enable/Disable

When using the PCI 9656, the configuration register bit that is used to enable or disable the PCI 9656's PCI Arbiter can only be written by the EEPROM or a Local Bus master. A PCI master cannot be write this bit. This is true for both the PCI 9656AD and the PCI 9656BA. The description in the Blue Book regarding this is incorrect.

Register 11-57 of the Blue Book incorrectly states that the PCI Arbiter Enable bit (PCIARB[0]) can be written by a PCI master. In fact, a PCI master cannot write the PCI Arbiter Enable bit.

The following shows the corrected entry of Register 11-57:

Table 3. (PCIARB; PCI:100h, LOC:1A0h) PCI Arbiter Control

Bit	Description	Read	Write	Value after Reset
0	**PCI Arbiter Enable.** Value of 0 indicates the PCI arbiter is disabled and REQ0# and GNT0# are used by the PCI 9656 to acquire PCI Bus use. Value of 1 indicates the PCI arbiter is enabled.	Yes	Local/ Serial EEPROM	0
...				

6. PCI BAR's 4 & 5 Unused

For Direct Slave data transfers, the PCI 9656 supports mapping two PCI address spaces to the Local Bus using PCI Base Address Registers (BAR's) 2 and 3. This is true for both the PCI 9656AD and the PCI 9656BA. The Blue Book PCI Configuration Register table regarding this is potentially confusing.

Table 11-2 of the Blue Book could be interpreted to indicate that the PCI 9656 supports mapping four PCI address spaces to the Local Bus for Direct Slave data transfers. The PCI 9656 in fact only supports mapping two PCI address spaces.

The following shows the corrected entries of Table 11-2.

Table 4. PCI Configuration Registers

PCI Configuration Register Address	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9656 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI/ Local Writeable	Serial EEPROM Writeable
...				
20h	20h	PCI Base Address 4; unused	Y	N
24h	24h	PCI Base Address 5; unused	Y	N
...				

7. Big Endian/Little Endian/Byte Lane Mode

The Blue Book descriptions of Big Endian and Little Endian conversion are potentially confusing.

PCI 9656 Big Endian and Little Endian conversion are detailed in Blue Book Sections 2.3 and 4.3. The following tables provide further clarification by detailing precisely PCI 9656 signal mappings between the PCI bus and the Local Bus during Big Endian and Little Endian conversion.

Table 5. C Mode Endian Mapping For Byte Lane Mode 0

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	C Mode Local Bus Pin Byte Lane Mode = 0 (BIGEND[4] = 0)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LD0	1-LD0	1-LD0	1-LD24	1-LD8	1-LD0
AD33	AD1	1-LD1	1-LD1	1-LD1	1-LD25	1-LD9	1-LD1
AD34	AD2	1-LD2	1-LD2	1-LD2	1-LD26	1-LD10	1-LD2
AD35	AD3	1-LD3	1-LD3	1-LD3	1-LD27	1-LD11	1-LD3
AD36	AD4	1-LD4	1-LD4	1-LD4	1-LD28	1-LD12	1-LD4
AD37	AD5	1-LD5	1-LD5	1-LD5	1-LD29	1-LD13	1-LD5
AD38	AD6	1-LD6	1-LD6	1-LD6	1-LD30	1-LD14	1-LD6
AD39	AD7	1-LD7	1-LD7	1-LD7	1-LD31	1-LD15	1-LD7
AD40	AD8	1-LD8	1-LD8	2-LD0	1-LD16	1-LD0	2-LD0
AD41	AD9	1-LD9	1-LD9	2-LD1	1-LD17	1-LD1	2-LD1
AD42	AD10	1-LD10	1-LD10	2-LD2	1-LD18	1-LD2	2-LD2
AD43	AD11	1-LD11	1-LD11	2-LD3	1-LD19	1-LD3	2-LD3
AD44	AD12	1-LD12	1-LD12	2-LD4	1-LD20	1-LD4	2-LD4
AD45	AD13	1-LD13	1-LD13	2-LD5	1-LD21	1-LD5	2-LD5
AD46	AD14	1-LD14	1-LD14	2-LD6	1-LD22	1-LD6	2-LD6
AD47	AD15	1-LD15	1-LD15	2-LD7	1-LD23	1-LD7	2-LD7
AD48	AD16	1-LD16	2-LD0	3-LD0	1-LD8	2-LD8	3-LD0
AD48	AD17	1-LD17	2-LD1	3-LD1	1-LD9	2-LD9	3-LD1
AD50	AD18	1-LD18	2-LD2	3-LD2	1-LD10	2-LD10	3-LD2
AD51	AD19	1-LD19	2-LD3	3-LD3	1-LD11	2-LD11	3-LD3
AD52	AD20	1-LD20	2-LD4	3-LD4	1-LD12	2-LD12	3-LD4
AD53	AD21	1-LD21	2-LD5	3-LD5	1-LD13	2-LD13	3-LD5
AD54	AD22	1-LD22	2-LD6	3-LD6	1-LD14	2-LD14	3-LD6
AD55	AD23	1-LD23	2-LD7	3-LD7	1-LD15	2-LD15	3-LD7
AD56	AD24	1-LD24	2-LD8	4-LD0	1-LD0	2-LD0	4-LD0
AD57	AD25	1-LD25	2-LD9	4-LD1	1-LD1	2-LD1	4-LD1
AD58	AD26	1-LD26	2-LD10	4-LD2	1-LD2	2-LD2	4-LD2
AD59	AD27	1-LD27	2-LD11	4-LD3	1-LD3	2-LD3	4-LD3
AD60	AD28	1-LD28	2-LD12	4-LD4	1-LD4	2-LD4	4-LD4
AD61	AD29	1-LD29	2-LD13	4-LD5	1-LD5	2-LD5	4-LD5
AD62	AD30	1-LD30	2-LD14	4-LD6	1-LD6	2-LD6	4-LD6
AD63	AD31	1-LD31	2-LD15	4-LD7	1-LD7	2-LD7	4-LD7

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.

2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LD5" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LD5 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LD5 during the second 16-bit Local Bus transfer.

3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.

4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

Table 6. C Mode Endian Mapping For Byte Lane Mode 1

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	C Mode Local Bus Pin Byte Lane Mode = 1 (BIGEND[4] = 1)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LD0	1-LD16	1-LD24	1-LD24	1-LD24	1-LD24
AD33	AD1	1-LD1	1-LD17	1-LD25	1-LD25	1-LD25	1-LD25
AD34	AD2	1-LD2	1-LD18	1-LD26	1-LD26	1-LD26	1-LD26
AD35	AD3	1-LD3	1-LD19	1-LD27	1-LD27	1-LD27	1-LD27
AD36	AD4	1-LD4	1-LD20	1-LD28	1-LD28	1-LD28	1-LD28
AD37	AD5	1-LD5	1-LD21	1-LD29	1-LD29	1-LD29	1-LD29
AD38	AD6	1-LD6	1-LD22	1-LD30	1-LD30	1-LD30	1-LD30
AD39	AD7	1-LD7	1-LD23	1-LD31	1-LD31	1-LD31	1-LD31
AD40	AD8	1-LD8	1-LD24	2-LD24	1-LD16	1-LD16	2-LD24
AD41	AD9	1-LD9	1-LD25	2-LD25	1-LD17	1-LD17	2-LD25
AD42	AD10	1-LD10	1-LD26	2-LD26	1-LD18	1-LD18	2-LD26
AD43	AD11	1-LD11	1-LD27	2-LD27	1-LD19	1-LD19	2-LD27
AD44	AD12	1-LD12	1-LD28	2-LD28	1-LD20	1-LD20	2-LD28
AD45	AD13	1-LD13	1-LD29	2-LD29	1-LD21	1-LD21	2-LD29
AD46	AD14	1-LD14	1-LD30	2-LD30	1-LD22	1-LD22	2-LD30
AD47	AD15	1-LD15	1-LD31	2-LD31	1-LD23	1-LD23	2-LD31
AD48	AD16	1-LD16	2-LD16	3-LD24	1-LD8	2-LD24	3-LD24
AD48	AD17	1-LD17	2-LD17	3-LD25	1-LD9	2-LD25	3-LD25
AD50	AD18	1-LD18	2-LD18	3-LD26	1-LD10	2-LD26	3-LD26
AD51	AD19	1-LD19	2-LD19	3-LD27	1-LD11	2-LD27	3-LD27
AD52	AD20	1-LD20	2-LD20	3-LD28	1-LD12	2-LD28	3-LD28
AD53	AD21	1-LD21	2-LD21	3-LD29	1-LD13	2-LD29	3-LD29
AD54	AD22	1-LD22	2-LD22	3-LD30	1-LD14	2-LD30	3-LD30
AD55	AD23	1-LD23	2-LD23	3-LD31	1-LD15	2-LD31	3-LD31
AD56	AD24	1-LD24	2-LD24	4-LD24	1-LD0	2-LD16	4-LD24
AD57	AD25	1-LD25	2-LD25	4-LD25	1-LD1	2-LD17	4-LD25
AD58	AD26	1-LD26	2-LD26	4-LD26	1-LD2	2-LD18	4-LD26
AD59	AD27	1-LD27	2-LD27	4-LD27	1-LD3	2-LD19	4-LD27
AD60	AD28	1-LD28	2-LD28	4-LD28	1-LD4	2-LD20	4-LD28
AD61	AD29	1-LD29	2-LD29	4-LD29	1-LD5	2-LD21	4-LD29
AD62	AD30	1-LD30	2-LD30	4-LD30	1-LD6	2-LD22	4-LD30
AD63	AD31	1-LD31	2-LD31	4-LD31	1-LD7	2-LD23	4-LD31

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.

2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LD21" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LD21 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LD21 during the second 16-bit Local Bus transfer.

3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.

4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

Table 7. J Mode Endian Mapping For Byte Lane Mode 0

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	J Mode Local Bus Pin Byte Lane Mode = 0 (BIGEND[4] = 0)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LAD0	1-LAD0	1-LAD0	1-LAD24	1-LAD8	1-LAD0
AD33	AD1	1-LAD1	1-LAD1	1-LAD1	1-LAD25	1-LAD9	1-LAD1
AD34	AD2	1-LAD2	1-LAD2	1-LAD2	1-LAD26	1-LAD10	1-LAD2
AD35	AD3	1-LAD3	1-LAD3	1-LAD3	1-LAD27	1-LAD11	1-LAD3
AD36	AD4	1-LAD4	1-LAD4	1-LAD4	1-LAD28	1-LAD12	1-LAD4
AD37	AD5	1-LAD5	1-LAD5	1-LAD5	1-LAD29	1-LAD13	1-LAD5
AD38	AD6	1-LAD6	1-LAD6	1-LAD6	1-LAD30	1-LAD14	1-LAD6
AD39	AD7	1-LAD7	1-LAD7	1-LAD7	1-LAD31	1-LAD15	1-LAD7
AD40	AD8	1-LAD8	1-LAD8	2-LAD0	1-LAD16	1-LAD0	2-LAD0
AD41	AD9	1-LAD9	1-LAD9	2-LAD1	1-LAD17	1-LAD1	2-LAD1
AD42	AD10	1-LAD10	1-LAD10	2-LAD2	1-LAD18	1-LAD2	2-LAD2
AD43	AD11	1-LAD11	1-LAD11	2-LAD3	1-LAD19	1-LAD3	2-LAD3
AD44	AD12	1-LAD12	1-LAD12	2-LAD4	1-LAD20	1-LAD4	2-LAD4
AD45	AD13	1-LAD13	1-LAD13	2-LAD5	1-LAD21	1-LAD5	2-LAD5
AD46	AD14	1-LAD14	1-LAD14	2-LAD6	1-LAD22	1-LAD6	2-LAD6
AD47	AD15	1-LAD15	1-LAD15	2-LAD7	1-LAD23	1-LAD7	2-LAD7
AD48	AD16	1-LAD16	2-LAD0	3-LAD0	1-LAD8	2-LAD8	3-LAD0
AD48	AD17	1-LAD17	2-LAD1	3-LAD1	1-LAD9	2-LAD9	3-LAD1
AD50	AD18	1-LAD18	2-LAD2	3-LAD2	1-LAD10	2-LAD10	3-LAD2
AD51	AD19	1-LAD19	2-LAD3	3-LAD3	1-LAD11	2-LAD11	3-LAD3
AD52	AD20	1-LAD20	2-LAD4	3-LAD4	1-LAD12	2-LAD12	3-LAD4
AD53	AD21	1-LAD21	2-LAD5	3-LAD5	1-LAD13	2-LAD13	3-LAD5
AD54	AD22	1-LAD22	2-LAD6	3-LAD6	1-LAD14	2-LAD14	3-LAD6
AD55	AD23	1-LAD23	2-LAD7	3-LAD7	1-LAD15	2-LAD15	3-LAD7
AD56	AD24	1-LAD24	2-LAD8	4-LAD0	1-LAD0	2-LAD0	4-LAD0
AD57	AD25	1-LAD25	2-LAD9	4-LAD1	1-LAD1	2-LAD1	4-LAD1
AD58	AD26	1-LAD26	2-LAD10	4-LAD2	1-LAD2	2-LAD2	4-LAD2
AD59	AD27	1-LAD27	2-LAD11	4-LAD3	1-LAD3	2-LAD3	4-LAD3
AD60	AD28	1-LAD28	2-LAD12	4-LAD4	1-LAD4	2-LAD4	4-LAD4
AD61	AD29	1-LAD29	2-LAD13	4-LAD5	1-LAD5	2-LAD5	4-LAD5
AD62	AD30	1-LAD30	2-LAD14	4-LAD6	1-LAD6	2-LAD6	4-LAD6
AD63	AD31	1-LAD31	2-LAD15	4-LAD7	1-LAD7	2-LAD7	4-LAD7

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.
2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LAD5" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LAD5 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LAD5 during the second 16-bit Local Bus transfer.
3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.
4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

Table 8. J Mode Endian Mapping For Byte Lane Mode 1

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	J Mode Local Bus Pin Byte Lane Mode = 1 (BIGEND[4] = 1)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LAD0	1-LAD16	1-LAD24	1-LAD24	1-LAD24	1-LAD24
AD33	AD1	1-LAD1	1-LAD17	1-LAD25	1-LAD25	1-LAD25	1-LAD25
AD34	AD2	1-LAD2	1-LAD18	1-LAD26	1-LAD26	1-LAD26	1-LAD26
AD35	AD3	1-LAD3	1-LAD19	1-LAD27	1-LAD27	1-LAD27	1-LAD27
AD36	AD4	1-LAD4	1-LAD20	1-LAD28	1-LAD28	1-LAD28	1-LAD28
AD37	AD5	1-LAD5	1-LAD21	1-LAD29	1-LAD29	1-LAD29	1-LAD29
AD38	AD6	1-LAD6	1-LAD22	1-LAD30	1-LAD30	1-LAD30	1-LAD30
AD39	AD7	1-LAD7	1-LAD23	1-LAD31	1-LAD31	1-LAD31	1-LAD31
AD40	AD8	1-LAD8	1-LAD24	2-LAD24	1-LAD16	1-LAD16	2-LAD24
AD41	AD9	1-LAD9	1-LAD25	2-LAD25	1-LAD17	1-LAD17	2-LAD25
AD42	AD10	1-LAD10	1-LAD26	2-LAD26	1-LAD18	1-LAD18	2-LAD26
AD43	AD11	1-LAD11	1-LAD27	2-LAD27	1-LAD19	1-LAD19	2-LAD27
AD44	AD12	1-LAD12	1-LAD28	2-LAD28	1-LAD20	1-LAD20	2-LAD28
AD45	AD13	1-LAD13	1-LAD29	2-LAD29	1-LAD21	1-LAD21	2-LAD29
AD46	AD14	1-LAD14	1-LAD30	2-LAD30	1-LAD22	1-LAD22	2-LAD30
AD47	AD15	1-LAD15	1-LAD31	2-LAD31	1-LAD23	1-LAD23	2-LAD31
AD48	AD16	1-LAD16	2-LAD16	3-LAD24	1-LAD8	2-LAD24	3-LAD24
AD48	AD17	1-LAD17	2-LAD17	3-LAD25	1-LAD9	2-LAD25	3-LAD25
AD50	AD18	1-LAD18	2-LAD18	3-LAD26	1-LAD10	2-LAD26	3-LAD26
AD51	AD19	1-LAD19	2-LAD19	3-LAD27	1-LAD11	2-LAD27	3-LAD27
AD52	AD20	1-LAD20	2-LAD20	3-LAD28	1-LAD12	2-LAD28	3-LAD28
AD53	AD21	1-LAD21	2-LAD21	3-LAD29	1-LAD13	2-LAD29	3-LAD29
AD54	AD22	1-LAD22	2-LAD22	3-LAD30	1-LAD14	2-LAD30	3-LAD30
AD55	AD23	1-LAD23	2-LAD23	3-LAD31	1-LAD15	2-LAD31	3-LAD31
AD56	AD24	1-LAD24	2-LAD24	4-LAD24	1-LAD0	2-LAD16	4-LAD24
AD57	AD25	1-LAD25	2-LAD25	4-LAD25	1-LAD1	2-LAD17	4-LAD25
AD58	AD26	1-LAD26	2-LAD26	4-LAD26	1-LAD2	2-LAD18	4-LAD26
AD59	AD27	1-LAD27	2-LAD27	4-LAD27	1-LAD3	2-LAD19	4-LAD27
AD60	AD28	1-LAD28	2-LAD28	4-LAD28	1-LAD4	2-LAD20	4-LAD28
AD61	AD29	1-LAD29	2-LAD29	4-LAD29	1-LAD5	2-LAD21	4-LAD29
AD62	AD30	1-LAD30	2-LAD30	4-LAD30	1-LAD6	2-LAD22	4-LAD30
AD63	AD31	1-LAD31	2-LAD31	4-LAD31	1-LAD7	2-LAD23	4-LAD31

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.
2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LAD21" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LAD21 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LAD21 during the second 16-bit Local Bus transfer.
3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.
4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

Table 9. M Mode Endian Mapping For Byte Lane Mode 0

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	M Mode Local Bus Pin Byte Lane Mode = 0 (BIGEND[4] = 0)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LD31	1-LD31	1-LD31	1-LD7	1-LD23	1-LD31
AD33	AD1	1-LD30	1-LD30	1-LD30	1-LD6	1-LD22	1-LD30
AD34	AD2	1-LD29	1-LD29	1-LD29	1-LD5	1-LD21	1-LD29
AD35	AD3	1-LD28	1-LD28	1-LD28	1-LD4	1-LD20	1-LD28
AD36	AD4	1-LD27	1-LD27	1-LD27	1-LD3	1-LD19	1-LD27
AD37	AD5	1-LD26	1-LD26	1-LD26	1-LD2	1-LD18	1-LD26
AD38	AD6	1-LD25	1-LD25	1-LD25	1-LD1	1-LD17	1-LD25
AD39	AD7	1-LD24	1-LD24	1-LD24	1-LD0	1-LD16	1-LD24
AD40	AD8	1-LD23	1-LD23	2-LD31	1-LD15	1-LD31	2-LD31
AD41	AD9	1-LD22	1-LD22	2-LD30	1-LD14	1-LD30	2-LD30
AD42	AD10	1-LD21	1-LD21	2-LD29	1-LD13	1-LD29	2-LD29
AD43	AD11	1-LD20	1-LD20	2-LD28	1-LD12	1-LD28	2-LD28
AD44	AD12	1-LD19	1-LD19	2-LD27	1-LD11	1-LD27	2-LD27
AD45	AD13	1-LD18	1-LD18	2-LD26	1-LD10	1-LD26	2-LD26
AD46	AD14	1-LD17	1-LD17	2-LD25	1-LD9	1-LD25	2-LD25
AD47	AD15	1-LD16	1-LD16	2-LD24	1-LD8	1-LD24	2-LD24
AD48	AD16	1-LD15	2-LD31	3-LD31	1-LD23	2-LD23	3-LD31
AD48	AD17	1-LD14	2-LD30	3-LD30	1-LD22	2-LD22	3-LD30
AD50	AD18	1-LD13	2-LD29	3-LD29	1-LD21	2-LD21	3-LD29
AD51	AD19	1-LD12	2-LD28	3-LD28	1-LD20	2-LD20	3-LD28
AD52	AD20	1-LD11	2-LD27	3-LD27	1-LD19	2-LD19	3-LD27
AD53	AD21	1-LD10	2-LD26	3-LD26	1-LD18	2-LD18	3-LD26
AD54	AD22	1-LD9	2-LD25	3-LD25	1-LD17	2-LD17	3-LD25
AD55	AD23	1-LD8	2-LD24	3-LD24	1-LD16	2-LD16	3-LD24
AD56	AD24	1-LD7	2-LD23	4-LD31	1-LD31	2-LD31	4-LD31
AD57	AD25	1-LD6	2-LD22	4-LD30	1-LD30	2-LD30	4-LD30
AD58	AD26	1-LD5	2-LD21	4-LD29	1-LD29	2-LD29	4-LD29
AD59	AD27	1-LD4	2-LD20	4-LD28	1-LD28	2-LD28	4-LD28
AD60	AD28	1-LD3	2-LD19	4-LD27	1-LD27	2-LD27	4-LD27
AD61	AD29	1-LD2	2-LD18	4-LD26	1-LD26	2-LD26	4-LD26
AD62	AD30	1-LD1	2-LD17	4-LD25	1-LD25	2-LD25	4-LD25
AD63	AD31	1-LD0	2-LD16	4-LD24	1-LD24	2-LD24	4-LD24

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.
2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LD26" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LD26 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LD26 during the second 16-bit Local Bus transfer.
3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.
4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

Table 10. M Mode Endian Mapping For Byte Lane Mode 1

PCI Pins Mapped 2nd (64-bit Transfers Only)	PCI Pins Mapped 1st	M Mode Local Bus Pin Byte Lane Mode = 1 (BIGEND[4] = 1)					
		Little Endian			Big Endian		
		32-bit	16-bit	8-bit	32-bit	16-bit	8-bit
AD32	AD0	1-LD31	1-LD15	1-LD7	1-LD7	1-LD7	1-LD7
AD33	AD1	1-LD30	1-LD14	1-LD6	1-LD6	1-LD6	1-LD6
AD34	AD2	1-LD29	1-LD13	1-LD5	1-LD5	1-LD5	1-LD5
AD35	AD3	1-LD28	1-LD12	1-LD4	1-LD4	1-LD4	1-LD4
AD36	AD4	1-LD27	1-LD11	1-LD3	1-LD3	1-LD3	1-LD3
AD37	AD5	1-LD26	1-LD10	1-LD2	1-LD2	1-LD2	1-LD2
AD38	AD6	1-LD25	1-LD9	1-LD1	1-LD1	1-LD1	1-LD1
AD39	AD7	1-LD24	1-LD8	1-LD0	1-LD0	1-LD0	1-LD0
AD40	AD8	1-LD23	1-LD7	2-LD7	1-LD15	1-LD15	2-LD7
AD41	AD9	1-LD22	1-LD6	2-LD6	1-LD14	1-LD14	2-LD6
AD42	AD10	1-LD21	1-LD5	2-LD5	1-LD13	1-LD13	2-LD5
AD43	AD11	1-LD20	1-LD4	2-LD4	1-LD12	1-LD12	2-LD4
AD44	AD12	1-LD19	1-LD3	2-LD3	1-LD11	1-LD11	2-LD3
AD45	AD13	1-LD18	1-LD2	2-LD2	1-LD10	1-LD10	2-LD2
AD46	AD14	1-LD17	1-LD1	2-LD1	1-LD9	1-LD9	2-LD1
AD47	AD15	1-LD16	1-LD0	2-LD0	1-LD8	1-LD8	2-LD0
AD48	AD16	1-LD15	2-LD15	3-LD7	1-LD23	2-LD7	3-LD7
AD48	AD17	1-LD14	2-LD14	3-LD6	1-LD22	2-LD6	3-LD6
AD50	AD18	1-LD13	2-LD13	3-LD5	1-LD21	2-LD5	3-LD5
AD51	AD19	1-LD12	2-LD12	3-LD4	1-LD20	2-LD4	3-LD4
AD52	AD20	1-LD11	2-LD11	3-LD3	1-LD19	2-LD3	3-LD3
AD53	AD21	1-LD10	2-LD10	3-LD2	1-LD18	2-LD2	3-LD2
AD54	AD22	1-LD9	2-LD9	3-LD1	1-LD17	2-LD1	3-LD1
AD55	AD23	1-LD8	2-LD8	3-LD0	1-LD16	2-LD0	3-LD0
AD56	AD24	1-LD7	2-LD7	4-LD7	1-LD31	2-LD15	4-LD7
AD57	AD25	1-LD6	2-LD6	4-LD6	1-LD30	2-LD14	4-LD6
AD58	AD26	1-LD5	2-LD5	4-LD5	1-LD29	2-LD13	4-LD5
AD59	AD27	1-LD4	2-LD4	4-LD4	1-LD28	2-LD12	4-LD4
AD60	AD28	1-LD3	2-LD3	4-LD3	1-LD27	2-LD11	4-LD3
AD61	AD29	1-LD2	2-LD2	4-LD2	1-LD26	2-LD10	4-LD2
AD62	AD30	1-LD1	2-LD1	4-LD1	1-LD25	2-LD9	4-LD1
AD63	AD31	1-LD0	2-LD0	4-LD0	1-LD24	2-LD8	4-LD0

Notes

1. During 64-bit PCI transfers, the lower 32 bits of the PCI bus (AD[31:0]) are always mapped first.

2. For each Local Bus Pin table entry, *n-m* means that row's PCI pin maps to Local Bus pin *m* during Local Bus cycle *n* that either results from the PCI cycle (PCI-to-Local Bus transfers) or results in the PCI cycle (Local Bus-to-PCI transfers). For example, a Local Bus Pin of "2-LD10" for PCI Pin AD21 during 16–bit Little Endian Local Bus transfers (ref. the darkest shaded entry) means that during a PCI-to-Local Bus transfer, the value of PCI Pin AD21 during each 32-bit PCI transfer will occur on Local Bus pin LD10 of the second resulting 16-bit Local Bus transfer. During a Local Bus-to-PCI transfer, this means that the value of PCI Pin AD21 will result from the value of Local Bus pin LD10 during the second 16-bit Local Bus transfer.

3. The mappings in the table only occur during data phases. Addresses always map to/from PCI AD[31:0] as indicated in the 32-bit Little Endian column after the address translation specified in the configuration registers is performed.

4. Little and Big Endian Modes are selected by both register bits and pin signals, depending on the data phase type: Direct Master Read/Write, Direct Slave Read/Write, DMA PCI-to-Local Bus / Local Bus-to-PCI, and Configuration Register Read/Write. See the BIGEND register description in Table 11-41 and the BIGEND# pin description in Table 12-11 for details.

8. Local Bus Pause Timer Count Must Be Even (MARBR[8] = 0)

The Blue Book includes a description of the Local Bus Pause Timer in the MARBR register (Register Description 11-40). For the PCI 9656AD, the Local Bus Pause Timer count must be even (MARBR[8] = 0). This restriction is not included in the Blue Book description. For the PCI 9056BA, this count may be odd or even (MARBR[8] = 0 or 1).

The PCI 9656 includes a Local Bus Pause Timer (MARBR[15:8]) for specifying how long to stay off of the Local Bus between transfers to/from the Local Bus during DMA.

For the PCI 9656AD, this count must be even (MARBR[8] = 0). Note that this counter is 0 after reset, so the only time this correction is of concern is if the Local Bus Pause Timer count is ever changed from its reset value.

For the PCI 9056BA, this count may be odd or even (MARBR[8] = 0 or 1).

9. ALE Output Delay Timing For Any Local Bus Clock Rate

The Blue Book includes Figure 13-3 that shows the ALE output delay timing to the Processor/Local Bus clock for a clock rate of 33MHz. It does not show the output delay timing for other clock rates.

The following figure shows the PCI 9656AD ALE output delay timing for any Processor/Local Bus clock rate. It replaces Figure 13-3 in the Blue Book for the PCI 9656AD silicon. LC_{HIGH} is the time in ns that the Processor/Local Bus clock is high. (**Note.** When two times are given like x/y ns, x ns is the minimum value and y ns is the maximum value.)

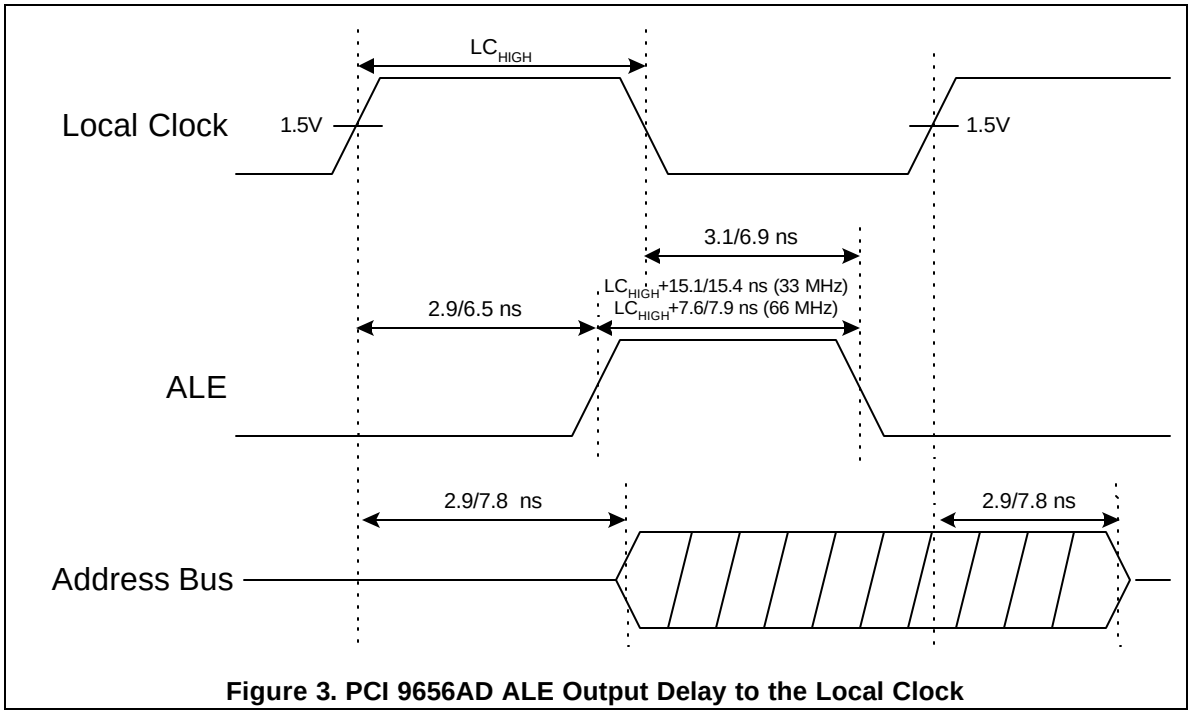

Figure 3. PCI 9656AD ALE Output Delay to the Local Clock

The following figure shows the PCI 9656BA ALE output delay timing for any Processor/Local Bus clock rate. It replaces Figure 13-3 in the Blue Book for the PCI 9656BA silicon. LC_{HIGH} is the time in ns that the Processor/Local Bus clock is high. (**Note.** When two times are given like x/y ns, x ns is the minimum value and y ns is the maximum value.)

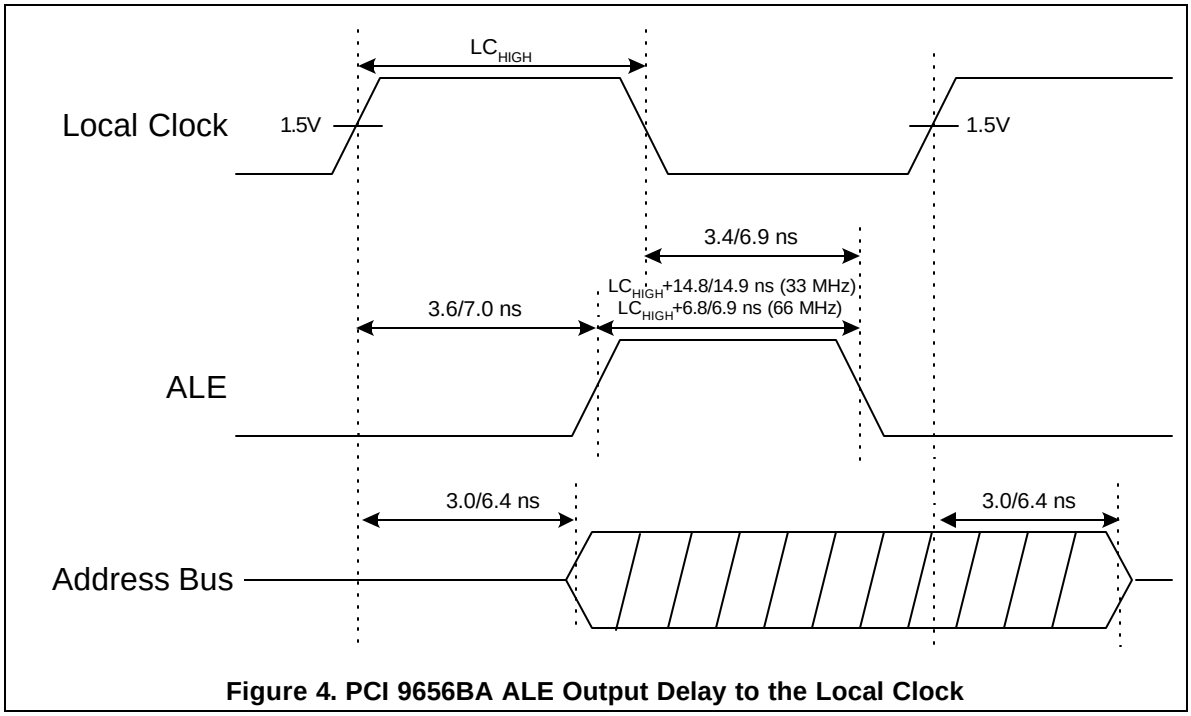

Figure 4. PCI 9656BA ALE Output Delay to the Local Clock

10. M Mode LA30 & LA 31 Pin Outs

Description:

The Blue Book Table 14-3 pin outs for pins P19 and P20 are indicated incorrectly. The M Mode LA31 and LA30 signals are swapped. This is true for both the PCI 9656AD and the PCI 9656BA.

Blue Book Table 14-3 indicates that pin P19 is “LA31 (M), LBE1# (C, J)” and pin P20 is “LA30 (M), LBE0# (C, J)”. This is incorrect.

For the PCI 9656AD and PCI 9656BA, pin P19 is “LA30 (M), LBE1# (C, J)” and pin P20 is “LA31 (M), LBE0# (C, J)”.

Note that in Table 12-10 the pin numbers for LA30 and LA31 are indicated correctly.

11. AC Timing

Description:

PLX had conducted exhaustive static timing analysis (STA) of the PCI 9656AD and PCI 9656BA silicon. The following six tables contain the results of that analysis and replace tables 13-6, 13-7, 13-8, and 13-9 in the Blue Book.

Table 11. C Mode Local Bus Input AC Timing Specifications

Signals (Synchronous Inputs)	T_{SETUP} (V_{CC} = 3.0V, T_a = 85°C)			T_{HOLD} (V_{CC} = 3.0V, T_a = 85°C)		
	Blue Book	AD STA	BA STA	Blue Book	AD STA	BA STA
ADS#	4.5 ns	4.8 ns	2.1 ns	1 ns	1 ns	1 ns
BIGEND#	4.5 ns	4.8 ns	4.0 ns	1 ns	1 ns	1 ns
BLAST#	4.5 ns	4.0 ns	3.4 ns	1 ns	1 ns	1 ns
BREQi	4.5 ns	1.7 ns	0.3 ns	1 ns	1 ns	1 ns
BTERM#	4.5 ns	4.8 ns	4.0 ns	1 ns	1 ns	1 ns
CCS#	4.5 ns	1.7 ns	2.9 ns	1 ns	1 ns	1 ns
DMPAF/**EOT#**	4.5 ns	4.7 ns	4.2 ns	1 ns	1 ns	1 ns
DP[3:0]	4.5 ns	2.0 ns	2.9 ns	1 ns	1 ns	1 ns
DREQ[1:0]#	4.5 ns	4.4 ns	3.3 ns	1 ns	1 ns	1 ns
LA[31:2]	4.5 ns	4.0 ns	3.4 ns	1 ns	1 ns	1 ns
LBE[3:0]#	4.5 ns	4.6 ns	3.6 ns	1 ns	1 ns	1 ns
LD[31:0]	4.5 ns	4.9 ns	3.1 ns	1 ns	1 ns	1 ns
LHOLDA	4.5 ns	4.2 ns	2.5 ns	1 ns	1 ns	1 ns
LW/R#	4.5 ns	5.0 ns	3.5 ns	1 ns	1 ns	1 ns
READY#	4.5 ns	4.7 ns	4.0 ns	1 ns	1 ns	1 ns
USERi/LLOCKi#	4.5 ns	2.4 ns	2.9 ns	1 ns	1 ns	1 ns
WAIT#	4.5 ns	4.7 ns	4.0 ns	1 ns	1 ns	1 ns
Input Clocks	**Min**			**Max**		
Local Clock Input Frequency	0 MHz			66 MHz		
PCI Clock Input Frequency	0 MHz			66 MHz		

Table 12. C Mode Local Bus Output AC Timing Specifications

Signals (Synchronous Outputs)	Output T_{VALID} (C_L = 50pF, V_{CC} = 3.0V, T_a = 85°C)		
	Blue Book	AD[1] STA	BA[2] STA
ADS#	9ns	7.6 ns	6.3 ns
BLAST#	9ns	7.6 ns	6.3 ns
BREQo	9ns	9.5 ns	6.8 ns
BTERM#	9ns	8.3 ns	6.8 ns
DACK[1:0]#	9ns	7.6 ns	6.3 ns
DMPAF/EOT#	9ns	8.5 ns	6.6 ns
DP[3:0]	9ns	7.9 ns	6.8 ns
LA[31:2]	9ns	8.0 ns	6.8 ns
LBE[3:0]#	9ns	7.6 ns	6.3 ns
LD[31:0]	9ns	7.8 ns	6.4 ns
LHOLD	9ns	7.5 ns	6.8 ns
LSERR#	9ns	10.2 ns	7.5 ns
LW/R#	9ns	7.6 ns	6.3 ns
READY#	9ns	9.0 ns	7.2 ns
USERo/LLOCKo#	9ns	7.6 ns	6.3 ns
WAIT#	9ns	7.6 ns	6.4 ns

1. On high-to-low transitions, output T_{VALID} values increase/decrease by 23 ps for each increase/decrease of 1pF.
   On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

2. On high-to-low transitions, output T_{VALID} values increase/decrease by 16 ps for each increase/decrease of 1pF.
   On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

   On high-to-low transitions, the slew rate at 50 pF loading is 1.93 V/ns typical; .94 V/ns worst case.
   On low-to-high transitions, the slew rate at 50 pF loading is 1.15 V/ns typical; .70 V/ns worst case.

Table 13. J Mode Local Bus Input AC Timing Specifications

Signals (Synchronous Inputs)	T_{SETUP} (V_{CC} = 3.0V, T_a = 85°C)			T_{HOLD} (V_{CC} = 3.0V, T_a = 85°C)		
	Blue Book	AD STA	BA STA	Blue Book	AD STA	BA STA
ADS#	4.5 ns	4.9 ns	2.1 ns	1 ns	1 ns	1 ns
ALE	4.5 ns	4.5 ns	1.7 ns	1 ns	1 ns	1 ns
BIGEND#	4.5 ns	4.8 ns	4.0 ns	1 ns	1 ns	1 ns
BLAST#	4.5 ns	4.0 ns	3.4 ns	1 ns	1 ns	1 ns
BREQi	4.5 ns	1.7 ns	0.3 ns	1 ns	1 ns	1 ns
BTERM#	4.5 ns	4.8 ns	4.2 ns	1 ns	1 ns	1 ns
CCS#	4.5 ns	1.7 ns	2.9 ns	1 ns	1 ns	1 ns
DMPAF/**EOT#**	4.5 ns	4.7 ns	4.2 ns	1 ns	1 ns	1 ns
DP[3:0]	4.5 ns	2.0 ns	2.9 ns	1 ns	1 ns	1 ns
DREQ[1:0]#	4.5 ns	4.4 ns	3.3 ns	1 ns	1 ns	1 ns
LA [28:2]	4.5 ns	4.0 ns	3.4 ns	1 ns	1 ns	1 ns
LAD[31:0]	4.5 ns	4.9 ns	3.1 ns	1 ns	1 ns	1 ns
LBE[3:0]#	4.5 ns	4.6 ns	3.6 ns	1 ns	1 ns	1 ns
LHOLDA	4.5 ns	4.2 ns	2.5 ns	1 ns	1 ns	1 ns
LW/R#	4.5 ns	5.0 ns	3.5 ns	1 ns	1 ns	1 ns
READY#	4.5 ns	4.7 ns	4.2 ns	1 ns	1 ns	1 ns
USERi/LLOCKi#	4.5 ns	2.4 ns	2.9 ns	1 ns	1 ns	1 ns
WAIT#	4.5 ns	4.7 ns	4.0 ns	1 ns	1 ns	1 ns
Input Clocks	**Min**			**Max**		
Local Clock Input Frequency	0 MHz			66 MHz		
PCI Clock Input Frequency	0 MHz			66 MHz		

Table 14. J Mode Local Bus Output AC Timing Specifications

Signals (Synchronous Outputs)	Output T_{VALID} (C_L = 50pF, V_{CC} = 3.0V, T_a = 85°C)		
	Blue Book	AD[1] STA	BA[2] STA
ADS#	9 ns	7.6 ns	6.3 ns
ALE	9 ns	8.0 ns	See item 9, above.
BLAST#	9 ns	7.6 ns	6.3 ns
BREQo	9 ns	9.5 ns	6.8 ns
BTERM#	9 ns	8.3 ns	6.8 ns
DACK[1:0]#	9 ns	7.6 ns	6.3 ns
DEN#	9 ns	7.9 ns	6.4 ns
DMPAF/EOT#	9 ns	8.5 ns	6.6 ns
DP[3:0]	9 ns	7.9 ns	6.8 ns
DT/R#	9 ns	7.9 ns	6.3 ns
LA[28:2]	9 ns	8.0 ns	6.4 ns
LAD[31:0]	9 ns	7.8 ns	6.4 ns
LBE[3:0]#	9 ns	7.6 ns	6.3 ns
LHOLD	9 ns	7.5 ns	6.8 ns
LSERR#	9 ns	10.2 ns	7.5 ns
LW/R#	9 ns	7.6 ns	6.3 ns
READY#	9 ns	9.0 ns	7.2 ns
USERo/LLOCKo#	9 ns	7.6 ns	6.3 ns
WAIT#	9 ns	7.6 ns	6.4 ns

1 On high-to-low transitions, output T_{VALID} values increase/decrease by 23 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

2 On high-to-low transitions, output T_{VALID} values increase/decrease by 16 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

On high-to-low transitions, the slew rate at 50 pF loading is 1.93 V/ns typical; .94 V/ns worst case.
On low-to-high transitions, the slew rate at 50 pF loading is 1.15 V/ns typical; .70 V/ns worst case.

Table 15. M Mode Local Bus Input AC Timing Specifications

Signals (Synchronous Inputs)	T_{SETUP} (V_{CC} = 3.0V, T_a = 85°C)			T_{HOLD}		
	Blue Book	AD STA	BA STA	Blue Book	AD STA	BA STA
BB#	4.5 ns	4.9 ns	2.7 ns	1 ns	1 ns	1 ns
BDIP#	4.5 ns	4.5 ns	3.8 ns	1 ns	1 ns	1 ns
BG#	4.5 ns	4.4 ns	2.9 ns	1 ns	1 ns	1 ns
BI#	4.5 ns	5.3 ns	4.0 ns	1 ns	1 ns	1 ns
BIGEND#/WAIT#	4.5 ns	4.8 ns	3.8 ns	1 ns	1 ns	1 ns
BURST#	4.5 ns	4.8 ns	4.1 ns	1 ns	1 ns	1 ns
CCS#	4.5 ns	1.7 ns	2.9 ns	1 ns	1 ns	1 ns
DP[0:3]	4.5 ns	2.0 ns	2.9 ns	1 ns	1 ns	1 ns
DREQ[1:0]#	4.5 ns	4.4 ns	3.3 ns	1 ns	1 ns	1 ns
LA[0:31]	4.5 ns	5.2 ns	3.6 ns	1 ns	1 ns	1 ns
LD[0:31]	4.5 ns	4.9 ns	3.1 ns	1 ns	1 ns	1 ns
MDREQ#/DMPAF/ **EOT#**	4.5 ns	4.7 ns	4.2 ns	1 ns	1 ns	1 ns
RD/WR#	4.5 ns	5.3 ns	3.5 ns	1 ns	1 ns	1 ns
TA#	4.5 ns	5.3 ns	4.1 ns	1 ns	1 ns	1 ns
TEA#	4.5 ns	5.2 ns	4.4 ns	1 ns	1 ns	1 ns
TS#	4.5 ns	4.8 ns	2.1 ns	1 ns	1 ns	1 ns
TSIZ[0:1]#	4.5 ns	5.0 ns	3.6 ns	1 ns	1 ns	1 ns
USERi/LLOCK#	4.5 ns	1.9 ns	3.2 ns	1 ns	1 ns	1 ns
Input Clocks	**Min**			**Max**		
Local Clock Input Frequency	0 MHz			66 MHz		
PCI Clock Input Frequency	0 MHz			66 MHz		

Table 16. M Mode Local Bus Output AC Timing Specifications

Signals (Synchronous Outputs)	Output T_{VALID} (C_L = 50pF, V_{CC} = 3.0V, T_a = 85°C)		
	Blue Book	AD[1] STA	BA[2] STA
BB#	9 ns	9.4 ns	6.8 ns
BDIP#	9 ns	7.7 ns	6.4 ns
BIGEND#/**WAIT#**	9 ns	7.6 ns	6.3 ns
BR#	9 ns	7.5 ns	6.8 ns
BURST#	9 ns	7.6 ns	6.3 ns
DACK[1:0]#	9 ns	7.6 ns	6.3 ns
DP[0:3]	9 ns	7.9 ns	6.8 ns
LA[0:31]	9 ns	8.0 ns	6.8 ns
LD[0:31]	9 ns	7.8 ns	6.3 ns
MDREQ#/DMPAF/ EOT#	9 ns	8.5 ns	6.6 ns
RD/WR#	9 ns	7.6 ns	6.3 ns
RETRY#	9 ns	9.5 ns	6.8 ns
TA#	9 ns	9.0 ns	7.2 ns
TEA#	9 ns	9.6 ns	7.5 ns
TS#	9 ns	7.6 ns	6.3 ns
TSIZ[0:1]#	9 ns	7.6 ns	6.3 ns
USERo/LLOCKo#	9 ns	7.6 ns	6.3 ns

1 On high-to-low transitions, output T_{VALID} values increase/decrease by 23 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

2 On high-to-low transitions, output T_{VALID} values increase/decrease by 16 ps for each increase/decrease of 1pF.
On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1pF.

On high-to-low transitions, the slew rate at 50 pF loading is 1.93 V/ns typical; .94 V/ns worst case.
On low-to-high transitions, the slew rate at 50 pF loading is 1.15 V/ns typical; .70 V/ns worst case.

12. Pin Types

Description:

The following tables detail the pin types of the PCI 9656AD and PCI 9656BA silicon. The information in these tables is intended to replace the Pin Type columns of Blue Book Tables 12-4 through 12-12.

Each table includes 5 columns for each pin:

1. Each entry in the leftmost column contains the name of the signal (or signals, in the case of multiplexed pins) connected to that pin.

2. Each entry in the next column contains the pin number (or pin numbers in the case of address buses, data buses, etc. that share the same pin type).

3. Each entry in the next column contains the pin type in the Blue Book.

4. Each entry in the next column contains the actual pin type for the AD silicon revision. Shaded entries in this column indicate where the actual pin type of the AD silicon differs from the pin type given in the Blue Book. While these changes should not effect designs that follow the Blue Book pin types, for designs that use the AD version of silicon, the designers should look carefully at the shaded entries in this column.

5. Each entry in the rightmost column contains the actual pin type for the BA silicon revision. Shaded entries in this column indicate where the actual pin type of the BA silicon differs from the actual pin type of the AD silicon. While these changes should not effect designs intended to use both AD and BA silicon revisions, for AD designs that are intended to use the BA as a drop-in replacement for the AD, the designers should look carefully at the shaded entries in this column.

Table 17. PCI 9656AD/PCI 9656BA PCI Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
ACK64#	N1	I/O STS PCI	I/O STS PCI	I/O STS PCI
AD[63:0]	T4, U3, W1, V3, Y2, W4, V4, U5, Y3, Y4, V5, W5, Y5, V6, U7, W6, Y6, V7, W7, Y7, V8, W8, Y8, V9, W9, Y9, W10, V10, Y10, Y11, W11, V11, A5, D7, C6, B5, A4, C5, B4, A3, B3, B2, A2, C3, B1, C2, D2, D3, H3, H2, H1, J4, J3, J2, J1, K2, K1, L2, L3, L4, M1, M2, M3, M4	I/O TS PCI	I/O TS PCI	I/O TS PCI
C/BE[7:0]#	T2, U1, T3, U2, D5, E4, G1, K3	I/O TS PCI	I/O TS PCI	I/O TS PCI
DEVSEL#	E1	I/O STS PCI	I/O STS PCI	I/O STS PCI
FRAME#	C1	I/O STS PCI	I/O STS PCI	I/O STS PCI
GNT0# **REQ#**	C7	**GNT0#** O **REQ#** O STS PCI	O TP PCI **Note:** *If ((RST# asserted) or (BD_SEL# not asserted))* Pin goes Hi-Z.	O TP PCI **Note:** *If ((RST# asserted) or (BD_SEL# not asserted))* Pin goes Hi-Z.
GNT[6:1]#	W12, U11, P4, R2, R1, N3	O TP	O TP PCI **Note:** *If ((RST# asserted) or (BD_SEL# not asserted) or PCARB[0]=0))* Pins go Hi-Z.	O TP PCI **Note:** *If ((RST# asserted) or (BD_SEL# not asserted) or PCARB[0]=0))* Pins go Hi-Z.
IDSEL	C4	I	I	I
INTA#	B7	I/O OC PCI	I/O OC PCI	I/O OC PCI
IRDY#	D1	I/O STS PCI	I/O STS PCI	I/O STS PCI
LOCK#	G4	I/O STS PCI	I/O STS PCI	I/O STS PCI
PAR	G2	I/O TS PCI	I/O TS PCI	I/O TS PCI
PAR64	V1	I/O TS PCI	I/O TS PCI	I/O TS PCI
PCLK	L1	I	I	I
PERR#	F2	I/O STS PCI	I/O STS PCI	I/O STS PCI

Table 17. PCI 9656AD/PCI 9656BA PCI Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
PME#	B9	O OC PCI	O OC PCI	O OC PCI
REQ0# **GNT#**	B6	**REQ0#** I **GNT#** I	I	I
REQ[6:1]#	V12, Y12, R3, T1, P2, P1	I	I	I
REQ64#	N2	I/O STS PCI	I/O STS PCI	I/O STS PCI
RST#	A6	I/O	*If (HOSTEN# asserted)* O TP PCI *else* I	*If (HOSTEN# asserted)* O TP PCI *else* I
SERR#	G3	I/O OC PCI	I/O OC PCI	I/O OC PCI
STOP#	F3	I/O STS PCI	I/O STS PCI	I/O STS PCI
TRDY#	E3	I/O STS PCI	I/O STS PCI	I/O STS PCI

Table 18. PCI 9656AD/PCI 9656BA C Mode Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
ADS#	C17	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
BIGEND#	C12	I	I	I
BLAST#	A18	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
BREQi	C16	I	I	I
BREQo	A17	O OC 24 mA	O DTS 24 mA	O DTS 24 mA
BTERM#	C20	I/O DTS 24 mA	I/O DTS 24 mA	I/O DTS 24 mA
CCS#	D12	I	I	I
DACK[1:0]#	C13, A13	O TP 24 mA	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pins go Hi-Z.	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pins go Hi-Z.
DMPAF **EOT#**	D14	**DMPAF** O TS 24 mA **EOT#** I	*If ((DMAMODE0[14]=1)* *or* *(DMAMODE1[14]=1))* I *else* O TP 24 mA	*If ((DMAMODE0[14]=1)* *or* *(DMAMODE1[14]=1))* I *else* O TP 24 mA **Note for 2nd case:** *If ((HOSTEN# not asserted & RST# asserted* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
DP[3:0]	D18, B20, C18, B19	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
DREQ[1:0]#	A14, B13	I	I	I
LA[31:2]	W14, Y15, V14, W15, Y16, U14, V15, W16, Y17, V16, W17, Y18, U16, V17, W18, Y19, V18, W19, Y20, W20, V19, U18, T17, V20, U20, T18, T19, T20, R18, P17	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
LBE[3:0]#	R20, P18, P19, P20	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
LCLK	D20	I	I	I

Table 18. PCI 9656AD/PCI 9656BA C Mode Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
LD[31:0]	N18, N19, N20, M17, M18, M19, M20, L19, L18, L20, K20, K19, K18, K17, J20, J19, J18, J17, H20, H19, H18, G20, G19, F20, G18, F19, E20, G17, F18, E19, E18, D19	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
LHOLD	B18	O TP 24 mA	O TP 24 mA	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
LHOLDA	B17	I	I	I
LINTi#	B15	I	I	I
LINTo#	A15	O OC 24 mA	O OC 24 mA	O OC 24 mA
LRESET#	A16	I/O TP 24 mA	*If (HOSTEN# asserted)* I *else* O TP 24 mA	*If (HOSTEN# asserted)* I *else* O TP 24 mA
LSERR#	D16	O OC 24 mA	O OC 24 mA	O OC 24 mA
LW/R#	R19	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
PMEREQ#	B10	I	I	I
READY#	E17	I/O DTS 24 mA	I/O DTS 24 mA	I/O DTS 24 mA
USERi **LLOCKi#**	B14	**USERi** I **LLOCKi#** I	I	I
USERo **LLOCKo#**	C14	**USERo** O TS 24 mA **LLOCKo#** O	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
WAIT#	B16	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA

Table 19. PCI 9656AD/PCI 9656BA J Mode Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
ADS#	C17	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
ALE	V14	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
BIGEND#	C12	I	I	I
BLAST#	A18	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
BREQi	C16	I	I	I
BREQo	A17	O OC 24 mA	O DTS 24 mA	O DTS 24 mA
BTERM#	C20	I/O DTS 24 mA	I/O DTS 24 mA	I/O DTS 24 mA
CCS#	D12	I	I	I
DACK[1:0]#	C13, A13	O TP 24 mA	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pins go Hi-Z.	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pins go Hi-Z.
DEN#	Y15	O TS 24 mA	O TS 24 mA	O TS 24 mA
DMPAF **EOT#**	D14	**DMPAF** O TS 24 mA **EOT#** I	*If ((DMAMODE0[14]=1)* *or* *(DMAMODE1[14]=1))* I *else* O TP 24 mA	*If ((DMAMODE0[14]=1)* *or* *(DMAMODE1[14]=1))* I *else* O TP 24 mA **Note for 2nd case:** *If ((HOSTEN# not asserted & RST# asserted* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
DP[3:0]	D18, B20, C18, B19	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
DREQ[1:0]#	A14, B13	I	I	I
DT/R#	W14	O TS 24 mA	O TS 24 mA	O TS 24 mA
LA[28:2]	W15, Y16, U14, V15, W16, Y17, V16, W17, Y18, U16, V17, W18, Y19, V18, W19, Y20, W20, V19, U18, T17, V20, U20, T18, T19, T20, R18, P17	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA

Table 19. PCI 9656AD/PCI 9656BA J Mode Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
LAD[31:0]	N18, N19, N20, M17, M18, M19, M20, L19, L18, L20, K20, K19, K18, K17, J20, J19, J18, J17, H20, H19, H18, G20, G19, F20, G18, F19, E20, G17, F18, E19, E18, D19	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
LBE[3:0]#	R20, P18, P19, P20	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
LCLK	D20	I	I	I
LHOLD	B18	O TP 24 mA	O TP 24 mA	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
LHOLDA	B17	I	I	I
LINTi#	B15	I	I	I
LINTo#	A15	O OC 24 mA	O OC 24 mA	O OC 24 mA
LRESET#	A16	I/O TP 24 mA	*If (HOSTEN# asserted)* I *else* O TP 24 mA	*If (HOSTEN# asserted)* I *else* O TP 24 mA
LSERR#	D16	O OC 24 mA	O OC 24 mA	O OC 24 mA
LW/R#	R19	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
PMEREQ#	B10	I	I	I
READY#	E17	I/O DTS 24 mA	I/O DTS 24 mA	I/O DTS 24 mA
USERi **LLOCKi#**	B14	**USERi** I **LLOCKi#** I	I	I
USERo **LLOCKo#**	C14	**USERo** O TS 24 mA **LLOCKo#** O	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
WAIT#	B16	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA

Table 20. PCI 9656AD/PCI 9656BA M Mode Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
BB#	C16	I/O OC 24 mA	I/O DTS 24 mA	I/O DTS 24 mA
BDIP#	B16	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
BG#	B17	I	I	I
BI#	C20	I	I	I
BIGEND# **WAIT#**	C12	**BIGEND#** I **WAIT#** I/O TS 24 mA	*If(MARBR(31)=0)* I *else* I/O TS 24 mA	*If(MARBR(31)=0)* I *else* I/O TS 24 mA
BR#	B18	O TP 24 mA	O TP 24 mA	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
BURST#	A18	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
CCS#	D12	I	I	I
DACK[1:0]#	C13, A13	O TP 24 mA	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pins go Hi-Z.	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pins go Hi-Z.
DP[0:3]	D18, B20, C18, B19	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
DREQ[1:0]#	A14, B13	I	I	I
LA[0:31]	W14, Y15, V14, W15, Y16, U14, V15, W16, Y17, V16, W17, Y18, U16, V17, W18, Y19, V18, W19, Y20, W20, V19, U18, T17, V20, U20, T18, T19, T20, R18, P17, P19, P20	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
LCLK	D20	I	I	I
LD[0:31]	N18, N19, N20, M17, M18, M19, M20, L19, L18, L20, K20, K19, K18, K17, J20, J19, J18, J17, H20, H19, H18, G20, G19, F20, G18, F19, E20, G17, F18, E19, E18, D19	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
LINTi#	B15	I	I	I

Table 20. PCI 9656AD/PCI 9656BA M Mode Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
LINTo#	A15	O OC 24 mA	O OC 24 mA	O OC 24 mA
LRESET#	A16	I/O TP 24 mA	*If (HOSTEN# asserted)* I *else* O TP 24 mA	*If (HOSTEN# asserted)* I *else* O TP 24 mA
MDREQ# **DMPAF** **EOT#**	D14	**MDREQ#** O TS 24 mA **DMPAF** O TS 24 mA **EOT#** I	*If ((DMAMODE0[14]=1)* *or* *(DMAMODE1[14]=1))* I *else* O TP 24 mA	*If ((DMAMODE0[14]=1)* *or* *(DMAMODE1[14]=1))* I *else* O TP 24 mA **Note for 2nd case:** *If ((HOSTEN# not asserted & RST# asserted* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.
PMEREQ#	B10	I	I	I
RD/WR#	R19	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
RETRY#	A17	O OC 24 mA	O DTS 24 mA	O DTS 24 mA
TA#	E17	I/O DTS 24 mA	I/O DTS 24 mA	I/O DTS 24 mA
TEA#	D16	I/O OC 24 mA	I/O OC 24 mA	I/O OC 24 mA
TS#	C17	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
TSIZ[0:1]	R20, P18	I/O TS 24 mA	I/O TS 24 mA	I/O TS 24 mA
USERi **LLOCKi#**	B14	**USERi** I **LLOCKi#** I	I	I
USERo **LLOCKo#**	C14	**USERo** O TS 24 mA **LLOCKo#** O	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.	O TP 24 mA **Note:** *If ((HOSTEN# not asserted & RST# asserted)* *or* *(HOSTEN# asserted & LRESET# asserted)* *or* *(BD_SEL# not asserted))* Pin goes Hi-Z.

Table 21. PCI 9656AD/PCI 9656BA JTAG Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
TCK	A8	I	I	I
TDI	A7	I	I	I
TDO	C8	O TS PCI	O TS PCI	O TS PCI
TMS	B8	I	I	I
TRST#	D9	I	I	I

Table 22. PCI 9656AD/PCI 9656BA Hot Swap Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
64EN#	U12	I	I	I
BD_SEL#	C9	I	I	I
CPCISW	Y14	I	I	I
ENUM#	Y13	O OC PCI	O OC PCI	O OC PCI
LEDon#	V13	O TP 24 mA	O OC 24 mA	O OC 24 mA

Table 23. PCI 9656AD/PCI 9656BA System Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
IDDQEN#	A10	I	I	I
MODE[1:0]	A19, A20	I	I	I
HOSTEN#	C15	I	I	I

Table 24. PCI 9656AD/PCI 9656BA EEPROM Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
EECS	B12	O TP 12 mA	O TP 12 mA **Note:** *If (BD_SEL# not asserted)* Pin goes Hi-Z.	O TP 12 mA **Note:** *If (BD_SEL# not asserted)* Pin goes Hi-Z.
EEDI/EEDO	B11	I/O TP 12 mA	I/O TS 12 mA **Note:** *If (CNTRL[31]=1)* Pin goes Hi-Z.	I/O TS 12 mA **Note:** *If (CNTRL[31]=1)* Pin goes Hi-Z.
EESK	A12	O TP 12 mA	O TP 12 mA **Note:** *If (BD_SEL# not asserted)* Pin goes Hi-Z.	O TP 12 mA **Note:** *If (BD_SEL# not asserted)* Pin goes Hi-Z.

Table 25. PCI 9656AD/PCI 9656BA Power & Ground Pin Types

Symbol	Pin Number	Blue Book r.90b Pin Type	True AD Pin Type	True BA Pin Type
$2.5V_{AUX}$	D10	I	I	I
$Card\_V_{AUX}$	C10	I	I	I
PRESENT_DET	A11	I	I	I
V_{BB}	W3	I	I	I **Note:** Changes from V_{BB} to V_{SS}.
V_{CORE}	C11, C19, E2, P3, U9, U19	I	I	I
V_{DDA}	W2	I	I	I **Note:** Changes from V_{DDA} to V_{RING}.
V_{IO}	A9, F1, V2, W13	I	I	I
V_{RING}	A1, D4, D6, D8, D11, D13, D15, D17, F4, F17, H4, H17, K4, L17, N4, N17, R4, R17, U4, U6, U8, U10, U13, U15, U17	I	I	I
V_{SS}	J9-J12, K9-K12, L9-L12, M9-M12	I	I	I
V_{SSA}	Y1	I	I	I **Note:** Changes from V_{SSA} to V_{SS}.