PLX 448

High Drive Current, Programmable Logic Device for Bus Interface Applications

February 1990

Distinctive Features

- Eight high current programmable I/Os and 11 inputs with logic architecture similar to industry standard PLDs.
- Integrated 48mA and 24mA drivers programmable to open collector or three-state configurations
- Buried register and combinatorial feedback capability
- Metastable hardened registers
- Two independent clock inputs
- On board drivers and Schmitt triggers allow direct connection to noisy backplanes
- Military temperature and reliability tested parts available in DIP and surface mountable packages

Applications

- Bus Control Logic
  - Bus Master and Slave Controllers
  - Intelligent Transceivers
  - Interrupt Generators and Handlers
  - Bus Arbiters
- General purpose high density, high drive current logic

General Description

The PLX 448 is a CMOS, UV erasable programmable logic device that can be easily programmed with industry standard hardware and software. With its on-board high current drivers and Schmitt triggers, metastable hardened registers and input hysteresis, it is ideally suited for designs in which direct connection to a bus backplane or other noisy environment is required. The high current drivers meet most of the specifications of VME, VSB, MBI*, MBII*, Micro Channel**, NuBus*** and other leading bus signal specifications. In addition, the PLX 448 has dynamic, bi-directional I/Os, buried register capability for building state machines and two clock inputs to handle asynchronous inputs.

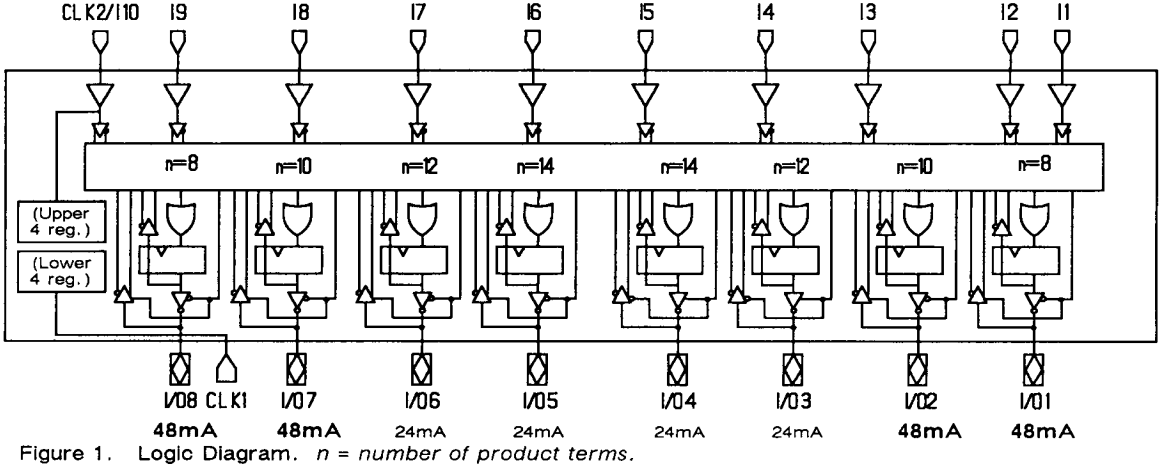

Figure 1. Logic Diagram. *n = number of product terms.*

Patent No. 4,833,349

* *Multibus I and Multibus II are registered trademarks of Intel Corporation*

** *Micro Channel is a registered trademark of IBM Corporation*

*** *NuBus is a registered trademark of Texas Instruments, Inc.*

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Detailed Description

Programmable Output Macrocell

The PLX 448 programmable output macrocell configuration is determined by the architecture bits C_0, C_1, C_2 and the output enable ($\overline{OE}$) product term (see Figures 2, 3 and table below).

The user can program each macrocell to a registered or combinatorial configuration with bit C_0.

C_1 determines the output polarity (Active High or Active Low).

With C_2 the user can individually program the 48mA Quad-state outputs (I/O1, 2, 7, 8) to open collector or three-state configurations. *(Continued on page 4.)*

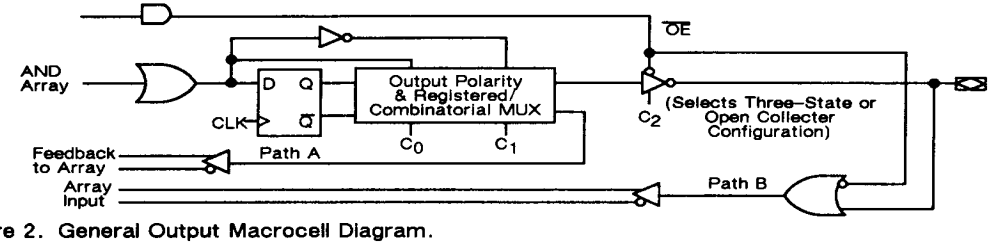
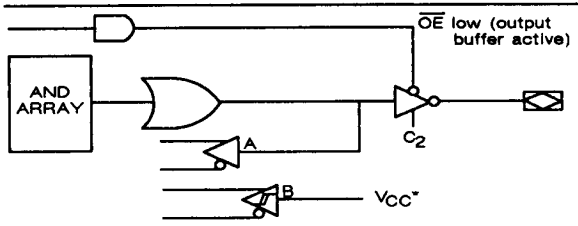


Figure 2. General Output Macrocell Diagram.
Applies to macrocells with 48mA outputs. 24mA output macrocells are three-state regardless of the state of C_2.

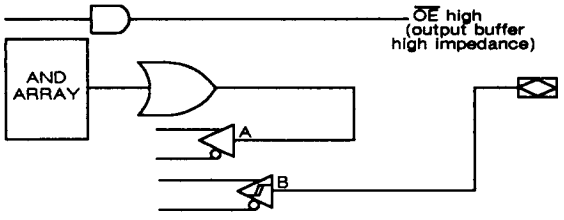
Architecture Bit and OE Term Definitions

Signal Name	Definition	Signal Name	Definition
$\overline{OE}$	High is high impedance, low is active.	C2	Level can be selected dynamically. Determines output state of 48mA outputs. If C2 is high and $\overline{OE}$ is low then the output is open collector. If C2 is low and $\overline{OE}$ is low, then the output is totem-pole. NOTE: 24mA outputs are always totem-pole when $\overline{OE}$ is low, regardless of the state of C2.
C0	High is registered mode, low is combinatorial.		
C1	High is active high, low is active low.		

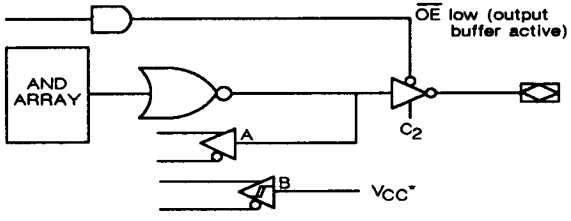
C0	C1	C2	$\overline{OE}$	Configuration Description	Schematic
0	0	0	0	Combinatorial, active low, totem pole output enabled	Configuration 1
0	0	0	1	Combinatorial, active low, totem pole output disabled	Configuration 2
0	0	1	0	Combinatorial, active low, open collector output enabled	Configuration 1
0	0	1	1	Combinatorial, active low, open collector output disabled	Configuration 2
0	1	0	0	Combinatorial, active high, totem pole output enabled	Configuration 3
0	1	0	1	Combinatorial, active high, totem pole output disabled	Configuration 4
0	1	1	0	Combinatorial, active high, open collector output enabled	Configuration 3
0	1	1	1	Combinatorial, active high, open collector output disabled	Configuration 4
1	0	0	0	Registered, active low, totem pole output enabled	Configuration 5
1	0	0	1	Registered, active low, totem pole output disabled	Configuration 6
1	0	1	0	Registered, active low, open collector output enabled	Configuration 5
1	0	1	1	Registered, active low, open collector output disabled	Configuration 6
1	1	0	0	Registered, active high, totem pole output enabled	Configuration 7
1	1	0	1	Registered, active high, totem pole output disabled	Configuration 8
1	1	1	0	Registered, active high, open collector output enabled	Configuration 7
1	1	1	1	Registered, active high, open collector output disabled	Configuration 8



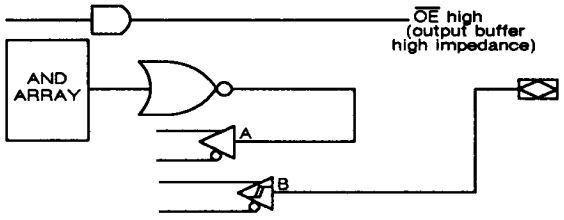
Configuration 1. Combinatorial Active Low.
Note that path A is same polarity as output of OR gate.



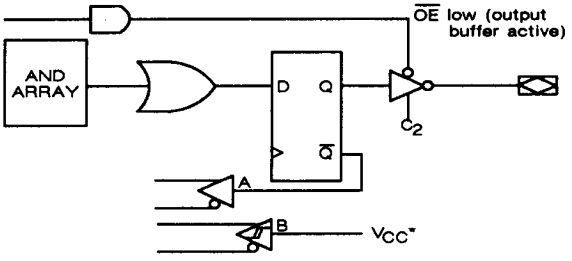
Configuration 2. Output disabled.
Path A is combinatorial Feedback. Path B is an input.



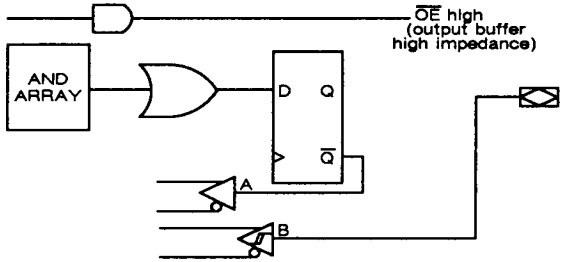
Configuration 3. Combinatorial Active High.
Note inverter on output of OR gate.



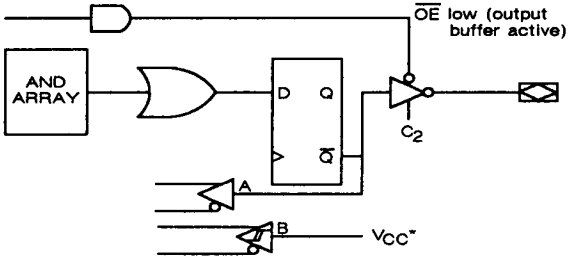
Configuration 4. Output disabled. Path A is combinatorial Feedback (note inverter on OR output). Path B is an input.



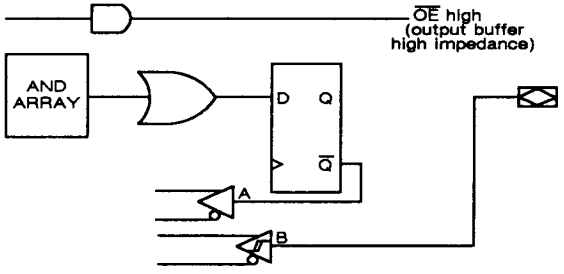
Configuration 5. Registered active low.
Note that path A comes from $\overline{Q}$.



Configuration 6. Output disabled. Path A is Registered feedback (from $\overline{Q}$). Path B is an input.



Configuration 7. Registered Active High.
Note that $\overline{Q}$ drives output buffer.



Configuration 8. Output disabled. Path A is registered feedback (from $\overline{Q}$). Path B is an input.

Figure 3. Specific Output Macrocell Configurations.
48 mA pins may be configured to open collector mode by programming C_2

*** When $\overline{OE}$ is enabled, Path B input becomes logical level high (goes to V_{CC})**

Programmable Output Macrocell (Continued)

The $\overline{OE}$ disables and enables both the output buffer and the input path (path B). When one is enabled, the other is disabled and vice versa. The $\overline{OE}$ state may be selected permanently or dynamically. The operation of the output buffer and the path B buffer are similar to that of a bi-directional transceiver.

When $\overline{OE}$ is low, the output buffer is enabled and the path B input is disconnected from the I/O pin and driven to V_{CC} (logic one).

When $\overline{OE}$ is high, the output buffer is disabled and the path B input is connected to the I/O pin acting as an input to the array.

In a typical application, the user can monitor $\overline{OE}$ to determine if path B is enabled or tied to V_{CC}. If the user wishes to monitor an I/O pin which can be driven by the macrocell output or another device (open collector or three state signal), the user can monitor both the internal feedback (Path A) and the input path (Path B).

Note that the $\overline{OE}$ is enabled by the "OR" of the inputs in the $\overline{OE}$ product term.

Preset and Reset

The PLX 448 includes synchronous preset and asynchronous reset product terms which are common to all output macrocells (see Figure 4.) The device automatically resets on power up. ("Preset" means Q output at register is set to 1. "Reset" means Q is set to 0.)

Testing

PLX 100 percent tests the windowed devices for full AC specifications before shipment. After test they are erased by exposure to Ultraviolet Light.

PLX tests the non-windowed one time programmable (OTP) devices for full AC specifications through the phantom array (Ph0-Ph3) and top test and bottom test rows. The device can be tested at incoming inspection the same way. Programmed devices can be tested by using preload to load initial values into the registers. Contact PLX for detailed programming information.

Clocks

The PLX 448 has two clock inputs. The dedicated clock pin clocks the registers in macrocells 1-4. The shared clock/input pin clocks registers in macrocells 5-8 (see Figure 4.)

Erasure

To erase the device, apply a minimum dose of 2537 Angstroms, 1800 mW x min/cm², (20 minutes under direct UV light, typically).

Metastability

Registers in the device have been specifically designed to minimize the metastable recovery time. For example, an MTBF requirement of 10 years at a clock frequency of 10MHz and a data frequency of 5MHz requires only 4ns of recovery time. (See page 11.) A detailed report on metastability is available from PLX on request.

Hysteresis

All inputs, including output macrocell inputs, have 200 mV typical hysteresis. (See pages 7 and 11.)

Ground Bounce

Three ground pins are provided to ensure minimal ground bounce in the device. I/O1-4 grounds are electrically isolated from I/O5-8 grounds. All I/O grounds are isolated from the internal logic ground. A detailed report on ground bounce and other bus specific device characteristics is available from PLX on request.

Device Programming

The following PLD programming software and hardware supports the PLX 448 device. Designers may use the software products below to edit source files, perform simulations and create JEDEC fuse map files.

Manufacturer (Software)	Product	Phone No. (In U.S.)
Data I/O, Redmond, WA	ABEL™ (version 3.0)	1-800-247-5700
Logical Devices, Fort Lauderdale, FL	CUPL™ (version 2.5)	1-800-331-7766 (305-974-0967 FL)
PistoHI™ Tools, Cupertino, CA	PET100™	1-800-274-7864
—Others are in development; contact PLX for an update.		

Manufacturer (Programmers)	Model No.	Phone No. (in U.S.)
Advin Systems, Sunnyvale, CA	Sailor-PAL	408-736-1622
Data I/O, Redmond, WA	29B	1-800-247-5700
Data I/O	Unisite 40™	1-800-247-5700
Digelec, Canoga Park, CA	860	1-800-367-8750 (818-887-3755 CA)
InLab, Broomfield, CO	28 A/U	1-800-237-6759 (303-460-0103 CO)
Logical Devices, Fort Lauderdale, FL	Allpro™	(305-974-0967 FL) 1-800-331-7766
OAE, Glendale, CA	(Omni 28, 40, 64 in development)	1-800-828-0080, (1-800-423-8874)
PistoHI™ Tools, Cupertino, CA	PET100™	408-255-2422
Stag Microsystems, Santa Clara, CA	ZL30, ZL30A	408-988-1118
Sunrise, Glendora, CA	ZL1000B, Z2500B	818-914-1926
—Others in Development; contact PLX for an update.		

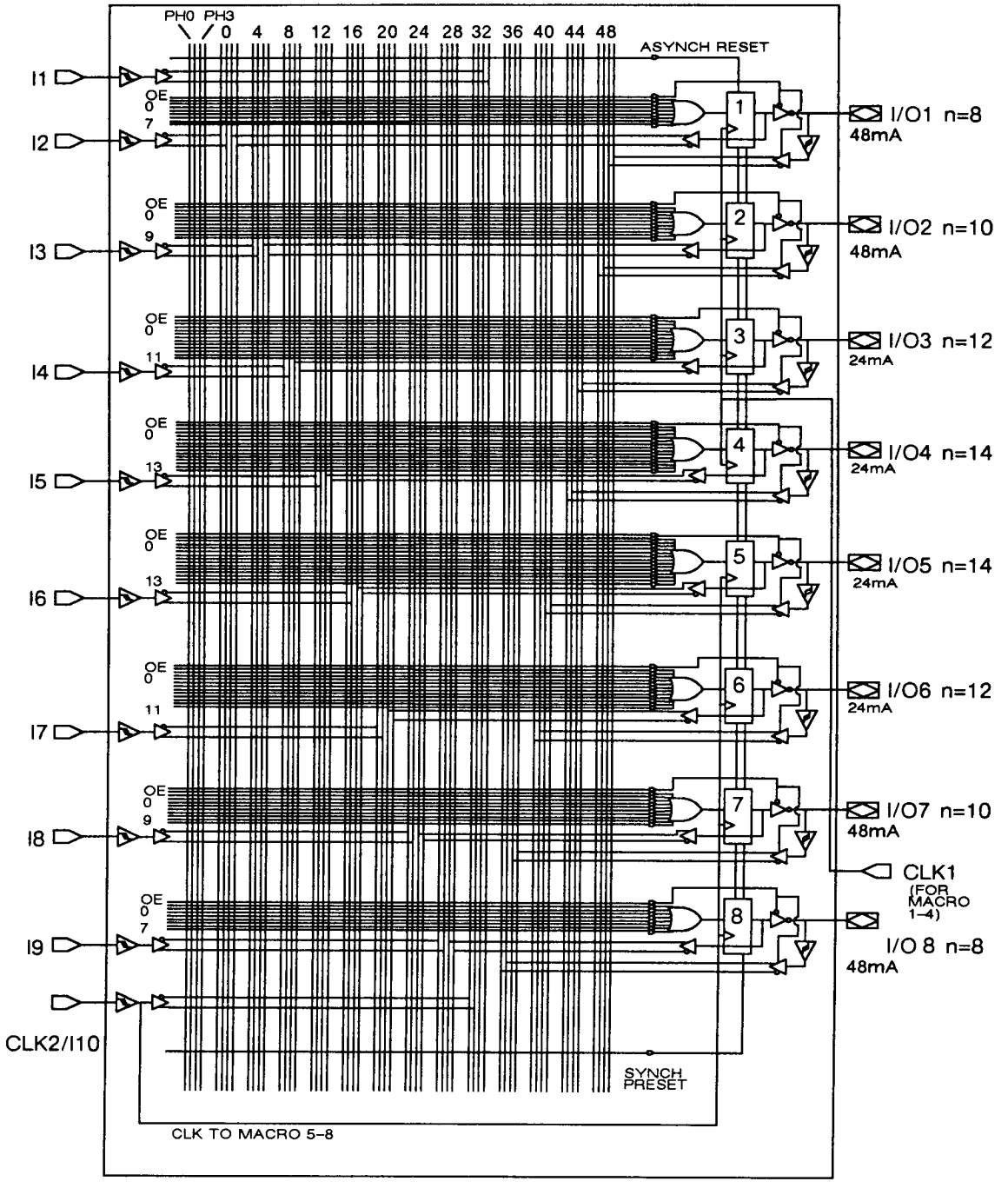
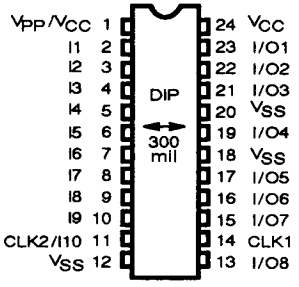
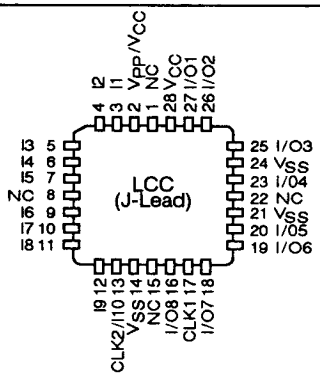


Figure 4. Logic Diagram *(n = # of product terms)*

Packages and Connection Diagrams





Pin Description (DIP and LCC Packages)

Pin No.		Description	Pin No.		Description
LCC	DIP		LCC	DIP	
28	24	V_{CC}	14, 21, 24	12, 18, 20	V_{SS} (Ground)
3-7, 9-12	2-10	Dedicated Inputs	16, 18, 19, 20, 23, 25, 26, 27	13, 15,16, 17, 19, 21, 22, 23	Bidirectional Input/Output pins
13	11	Dedicated Input and/or Clock Input to registers 4-8 (CLK2)			
17	14	Clock Input to registers 1-4 (CLK1)	1, 8, 15, 22		No Connect
2	1	V_{PP} /V_{CC}			

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -55°C to +125°C
Supply Voltage to Ground ..... -0.5V to +7.0V
DC Voltage to Outputs in High Z State ..... -0.5V to +7.0V
UV Exposure ..... 7000 Wsec/cm²
DC Programming Voltage 14.0V

Operating Ranges

	Ambient Temperature	Supply Voltage (V_{CC})
Commercial (C)	0°C to +70°C	5V ± 5%
Military (M)	-55°C to +125°C	5V ± 10%

Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I/O3, 4, 5, 6 I_{OL} = 24 (Com'l)		0.5	V
			I_{OL} = 24 (MIL)		0.6	V
			I/O1, 2, 7, 8 I_{OL} = 48 (Com'l)		0.5	V
			I_{OL} = 48 (MIL)		0.6	V
V_{IH}	Input HIGH Level			2.0		V
V_{IL}	Input LOW Level				0.8	V
I_{IX}	Input Leakage Current	V_{SS} <= V_{IN} <= V_{CC}, V_{CC} = Max		-10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{SS} <= V_{OUT} <= V_{CC}		-40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.5V		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, V_{IN} = GND Outputs Open (Com'l)			80	mA
		V_{CC} = Max, V_{IN} = GND Outputs Open (MIL)			90	mA

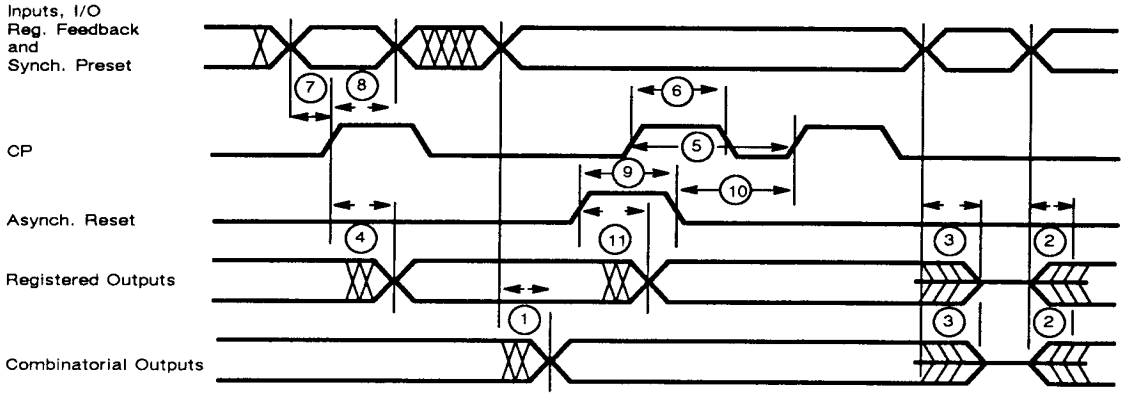
Capacitance (sample tested only)

Parameter	Test Conditions	Pins	Typ	Units
C_{IN}	V_{IN} = 2.0V @ f = 1MHz	Inputs and CLK1	5	pF
		I/Os	10	pF
C_{OUT}	V_{IN} = 2.0V @ f = 1MHz	I/Os	10	pF

Hysteresis

Parameter Symbol	Description	Typ	Units
V_{T+}	Positive-going threshold	1.5	V
V_{T-}	Negative-going threshold	1.3	V
nV_T	Hysteresis ($V_{T+} - V_{T-}$)	0.2	V

Switching Waveform



Switching Characteristics (Commercial Temperature Range)

	Parameter Symbol	Description	-45		Units
			Min	Max	
1.	t_{PD}	Input/feedback to nonreg. output		45	ns
2.	t_{EA}	Input to Output Enable		45	ns
3.	t_{ER}	Input to Output Disable		45	ns
4.	t_{CO}	Clock to Output		30	ns
5.	t_P	Clock Period (t_S + tCO)	60		ns
6.	t_W	Clock Width	35		ns
7.	t_S	Setup time (input or feedback)	30		ns
8.	t_H	Hold time	0		ns
9.	t_{AW}	Asynchronous reset width	45		ns
10.	t_{AR}	Recovery time, Asynch. reset	45		ns
11.	t_{AP}	Asynch reset to reg. output reset	45		ns
12.	f_{MAX}	Maximum frequency	16.7		MHz

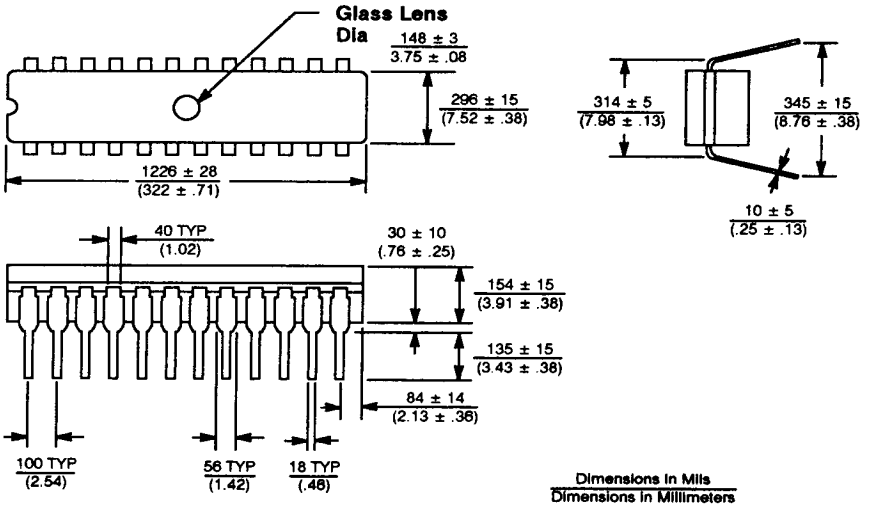
Note: Devices are tested with a 50 pF load. Derate speed by 10ns for a 300 pF load.

Switching Characteristics (Military Temperature Range)

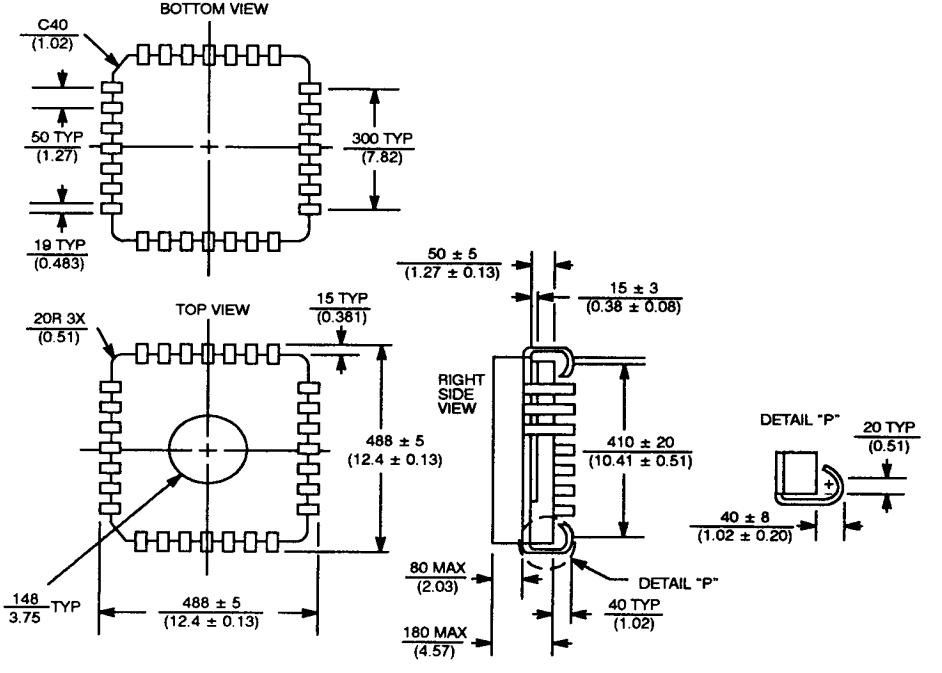
	Parameter Symbol	Description	M-65		Units
			Min	Max	
1.	t_{PD}	Input/feedback to nonreg. output		65	ns
2.	t_{EA}	Input to Output Enable		65	ns
3.	t_{ER}	Input to Output Disable		65	ns
4.	t_{CO}	Clock to Output		50	ns
5.	t_P	Clock Period (t_S + tCO)	90		ns
6.	t_W	Clock Width	55		ns
7.	t_S	Setup time (input or feedback)	40		ns
8.	t_H	Hold time	0		ns
9.	t_{AW}	Asynchronous reset width	65		ns
10.	t_{AR}	Recovery time, Asynch. reset	65		ns
11.	t_{AP}	Asynch reset to reg. output reset	65		ns
12.	f_{MAX}	Maximum frequency	11.1		MHz

Note: Devices are tested with a 50 pF load. Derate speed by 10ns for a 300 pF load.

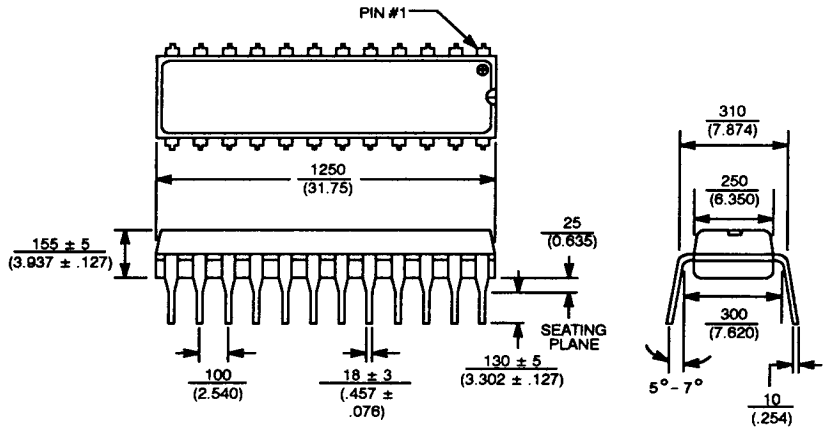
24-Lead Ceramic Dual In-line Package (CERDIP)



28-Pin J Lead Ceramic Chip Carrier



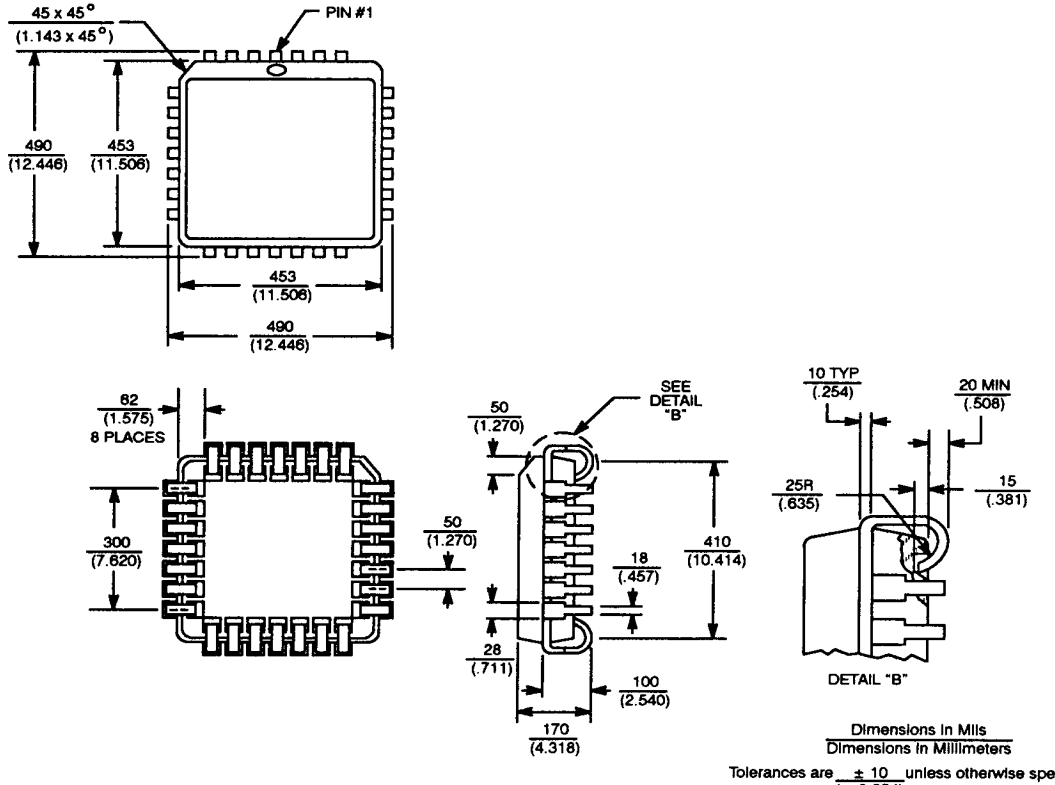
24-Pin DIP Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified

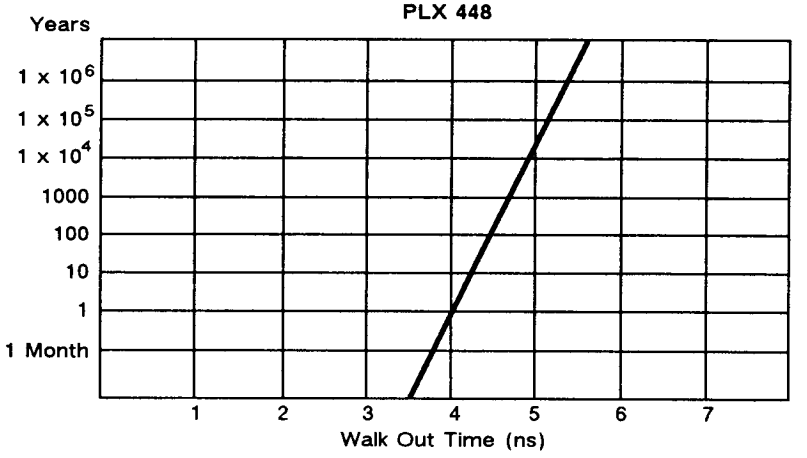
28-Pin LCC Plastic



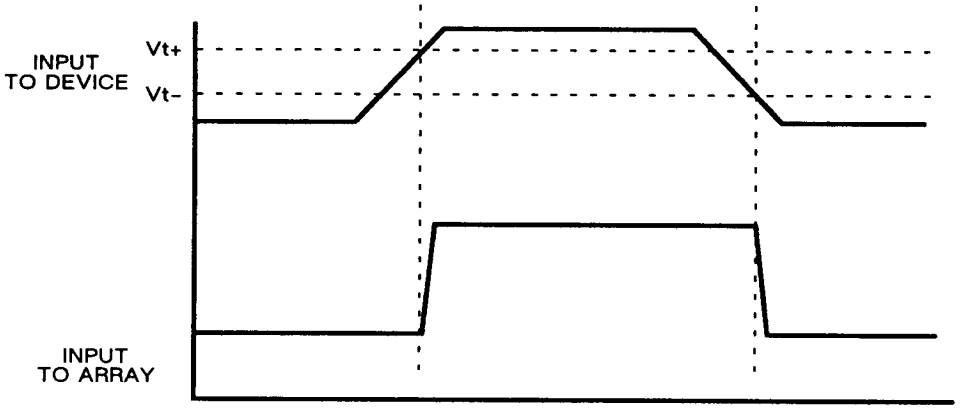
Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified

METASTABILITY INFORMATION
MTBF vs. Walk Out Time
PLX 448



INPUT HYSTERESIS (SCHMITT TRIGGER INPUTS)



Ordering Information

Package	Temperature Range	
	Commercial	Military
	0°C to +70°C	-55°C to +125°C
Package Material	Ceramic/Plastic	Ceramic
Package Type	24 Pin 300mil DIP	24 Pin 300mil DIP
	28 Pin J-Lead LCC	28 Pin J-Lead LCC
Drive Current (I_{OL})	4 @ 48mA, 4 @ 24mA	4 @ 48mA, 4 @ 24mA

Part Number Designations

PLX 448 XXX-YY

Speed Category -45 or -65

Package Type
- D = 24 Pin, windowed ceramic DIP, 300mil
- P = 24 Pin, plastic DIP, 300mil
- WJC = 28 Pin, windowed J-lead ceramic LCC
- JC = 28 Pin, J-lead ceramic LCC
- JP = 28 Pin, J-lead plastic LCC
- HR = 24 Pin, windowed ceramic DIP, 300mil, High Reliability Tested
- M = 24 Pin, windowed ceramic DIP, 300mil, Military Temperature (-55°C to +125°C)