PC100 Registered DIMM(168pin) Intel Type Rev1.2 SPD Specification(128Mb A-die base)

Rev. 0.0 August 1999



M377S1723AT3-C1H/C1L (1.2ver)

Organization: 16MX72Composition: 16MX8 *9

• Used component part #: K4S280832A-TC1H/C1L

of rows in module : 1 Row# of banks in component : 4 banks

• Feature: 1,500 mil height & double sided component

• Refresh : 4K/64ms

Byte #	Function described	Function Supported		Hex	Note	
Буш #	runction described	-1H	-1L	-1H	-1L	Note
0	# of bytes written into serial memory at module manufacturer	128	oytes	8	30h	
1	Total # of bytes of SPD memory device	256bytes	s (2K-bit)	(08h	
2	Fundamental memory type	SDF	RAM	()4h	
3	# of row address on this assembly	1	2	()Ch	1
4	# of column address on this assembly	1	0	()Ah	1
5	# of module Rows on this assembly	1 F	Row	()1h	
6	Data width of this assembly	72	bits	4	18h	
7	Data width of this assembly		-	(00h	
8	Voltage interface standard of this assembly	LV	ΓΤL	()1h	
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	EC	cc	()2h	
12	Refresh rate & type	15.625us, supp	oort self refresh		30h	
13	Primary SDRAM width	x	8	()8h	
14	Error checking SDRAM width	х	8	()8h	
15	Minimum clock dealy for back-to-back random column address	tCCD =	= 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 , 8 a	nd full page	8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 ba	anks	04h		
18	SDRAM device attributes : CAS latency	2	& 3	06h		
19	SDRAM device attributes : CS latency	0.0	CLK	01h		
20	SDRAM device attributes : Write latency	0.0	CLK	()1h	
21	SDRAM module attributes	address & con	uffered DQM, itrol inputs and rd PLL	1Fh		
22	SDRAM device attributes : General	Burst Read S	ige tolerance, ingle bit Write auto precharge	(0Eh	
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row o	f 128MB	2	20h	
32	Command and Address signal input setup time	21	ns	2	20h	
33	Command and Address signal input hold time	11	ns		10h	
34	Data signal input setup time	21	ns	2	20h	



Byte #	Function described	Function	Function Supported		Function Supported		Hex value	
Буш #	Function described	-1H	-1L	-1H	-1L	- Note		
35	Data signal input hold time	1	Ins	1	0h			
36~61	Superset information (maybe used in future)	-		00h				
62	SPD data revision code	Current releas	se Intel spd 1.2A	1:	2h			
63	Checksum for bytes 0 ~ 62		-	47h	77h			
64	Manufacturer JEDEC ID code	San	nsung	С	Eh			
65~71	Manufacturer JEDEC ID code	San	nsung	0	0h			
72	Manufacturing location	Onyar	ng Korea	0	1h			
73	Manufacturer part # (Memory module)		М	41	Dh			
74	Manufacturer part # (DIMM configuration)		3	3	3h			
75	Manufacturer part # (Data bits)	В	lank	2	0h			
76	Manufacturer part # (Data bits)		7	3	7h			
77	Manufacturer part # (Data bits)		7	3	7h			
78	Manufacturer part # (Mode & operating voltage)	S		53h				
79	Manufacturer part # (Module depth)	1		31h				
80	Manufacturer part # (Module depth)	7		3	37h			
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h				
82	Manufacturer part # (Composition component)		3	33h				
83	Manufacturer part # (Component revision)		A	41h				
84	Manufacturer part # (Package type)		Т	54h				
85	Manufacturer part # (PCB revision & type)		3	33h				
86	Manufacturer part # (Hyphen)	"	- "	21	Dh			
87	Manufacturer part # (Power)		С	4	3h			
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h			
89	Manufacturer part # (Minimum cycle time)	Н	L	48h	4Ch			
90	Manufacturer part # (TBD)	В	lank	2	0h			
91	Manufacturer revision code (For PCB)		3	3	3h			
92	Manufacturer revision code (For component)	A-die (2	2nd Gen.)	4	1h			
93	Manufacturing date (Week)	-		-		3		
94	Manufacturing date (Year)	-		-		3		
95~98	Assembly serial #		-		-	4		
99~125	Manufacturer specific data (may be used in future)	Und	efined		-	5		
126	System frequency for 100MHz	100)MHz	6	4h			
127	Intel Specification details	Detailed 100N	MHz Information	8Fh	8Dh			
128+	Unused storage locations	Und	efined		-	5		

- 2. This value is based on the component specification.
- 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
- 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
- 5. These bytes are Undefined and can be used for Samsung's own purpose.



M377S3320AT3-C1H/C1L (1.2ver)

Organization : 32MX72Composition : 32MX4 *18

• Used component part #: K4S280432A-TC1H/C1L

of rows in module : 1 Row# of banks in component : 4 banks

• Feature: 1,700 mil height & double sided component

• Refresh : 4K/64ms

Byte #	Function described	Function Supported		Hex	Note	
Byte #	r unction described	-1H	-1L	-1H	-1L	Note
0	# of bytes written into serial memory at module manufacturer	1281	oytes	8	30h	
1	Total # of bytes of SPD memory device	256bytes	s (2K-bit)	()8h	
2	Fundamental memory type	SDF	RAM	04h		
3	# of row address on this assembly	1	2	C)Ch	1
4	# of column address on this assembly	1	1	0Bh		1
5	# of module Rows on this assembly	1 R	low	01h		
6	Data width of this assembly	72	bits	4	48h	
7	Data width of this assembly		-	00h		
8	Voltage interface standard of this assembly	LV	ΓTL	()1h	
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	EC	CC	()2h	
12	Refresh rate & type	15.625us, supp	oort self refresh	8	30h	
13	Primary SDRAM width	х	4	()4h	
14	Error checking SDRAM width	х	4	04h		
15	Minimum clock dealy for back-to-back random column address	tCCD =	: 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 8	8 page	0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 ba	anks	04h		
18	SDRAM device attributes : CAS latency	2	& 3	06h		
19	SDRAM device attributes : CS latency	0 0	CLK	01h		
20	SDRAM device attributes : Write latency	0.0	CLK	()1h	
21	SDRAM module attributes	address & con	uffered DQM, trol inputs and rd PLL	1Fh		
22	SDRAM device attributes : General	Burst Read S	ge tolerance, ingle bit Write auto precharge	C	0Eh	
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	1 Row o	f 256MB	4	10h	
32	Command and Address signal input setup time	21	าร	2	20h	
33	Command and Address signal input hold time	11	าร	1	I0h	
34	Data signal input setup time	21	าร	2	20h	



Byte #	Function described	Function	Supported	Hex value		Note
Буш #	Function described	-1H	-1L	-1H	-1L	Note
35	Data signal input hold time	1	ns	10)h	
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current releas	e Intel spd 1.2A	12	2h	
63	Checksum for bytes 0 ~ 62		-	E0h	10h	
64	Manufacturer JEDEC ID code	Samsung		CI	Ēh	
65~71	Manufacturer JEDEC ID code	Samsung		00)h	
72	Manufacturing location	Onyan	g Korea	01	lh	
73	Manufacturer part # (Memory module)	ı	М	40	Dh	
74	Manufacturer part # (DIMM configuration)		3	33	3h	
75	Manufacturer part # (Data bits)	Bla	ank	20)h	
76	Manufacturer part # (Data bits)		7	37	7 h	
77	Manufacturer part # (Data bits)		7	37	7h	
78	Manufacturer part # (Mode & operating voltage)	:	S	53h		
79	Manufacturer part # (Module depth)		3	33h		
80	Manufacturer part # (Module depth)	3 33h		3h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32	2h	
82	Manufacturer part # (Composition component)		0	30h		
83	Manufacturer part # (Component revision)		A	41h		
84	Manufacturer part # (Package type)		Т	54h		
85	Manufacturer part # (PCB revision & type)		3	33	3h	
86	Manufacturer part # (Hyphen)	"	- "	20	Dh	
87	Manufacturer part # (Power)	С		33h 33h 32h 30h 41h		
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	Н	L	48h	4Ch	
90	Manufacturer part # (TBD)	Bl	ank	20)h	
91	Manufacturer revision code (For PCB)		3	33	Bh	
92	Manufacturer revision code (For component)	A-die (2	2ndGen.)	41h		
93	Manufacturing date (Week)		-	-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #		-		•	4
99~125	Manufacturer specific data (may be used in future)	Unde	efined		•	5
126	System frequency for 100MHz	100	MHz	64	1h	
127	Intel Specification details	Detailed 100M	1Hz Information	8Fh	8Dh	
128+	Unused storage locations	Unde	efined	-		5

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- 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
- 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
- 5. These bytes are Undefined and can be used for Samsung's own purpose.



M377S3323AT0-C1H/C1L

Organization: 32MX72Composition: 16MX8 *18

• Used component part #: K4S280832A-TC1H/C1L

of banks in module : 2 Rows# of banks in component : 4 banks

• Feature: 1,700 mil height & double sided component

• Refresh : 4K/64ms

Duto #	Function described	Function	Supported	Hex	value	Note
Byte #	runction described	-1H	-1L	-1H	-1L	Note
0	# of bytes written into serial memory at module manufacturer	128	oytes	8	0h	
1	Total # of bytes of SPD memory device	256byte	s (2K-bit)	C	8h	
2	Fundamental memory type	SDI	RAM	04h		
3	# of row address on this assembly	1	2	0	Ch	1
4	# of column address on this assembly	1	0	0	0Ah	
5	# of module Rows on this assembly	2 R	ows	C	2h	
6	Data width of this assembly	72	bits	4	-8h	
7	Data width of this assembly		-	00h		
8	Voltage interface standard of this assembly	LV	TTL	01h		
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	E	CC	C	2h	
12	Refresh rate & type	15.625us, supp	port self refresh	8	0h	
13	Primary SDRAM width	Х	8	C	8h	
14	Error checking SDRAM width	Х	8	C	8h	
15	Minimum clock dealy for back-to-back random column address	tCCD =	= 1CLK	C	11h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8	& full page	8Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 ba	anks	04h		
18	SDRAM device attributes : CAS latency	2	& 3	06h		
19	SDRAM device attributes : CS latency	0.0	CLK	01h		
20	SDRAM device attributes : Write latency	0.0	CLK	C	1h	
21	SDRAM module attributes	address & contro	uffered DQM, ol inputs and On- I PLL	1Fh		
22	SDRAM device attributes : General	Burst Read S	age tolerance, single bit Write auto precharge	0	Eh	
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows	of 128MB	2	0h	
32	Command and Address signal input setup time	2	ns	2	0h	
33	Command and Address signal input hold time	1	ns	1	0h	
34	Data signal input setup time	2	ns	2	10h	



Byte #	Function described	Function S	upported	Hex	/alue	Note
Буш #	Function described	-1H	-1L	-1H	-1L	Note
35	Data signal input hold time	1ns	3	10)h	
36~61	Superset information (maybe used in future)	-		00)h	
62	SPD data revision code	Current release	Intel spd 1.2A	12	2h	
63	Checksum for bytes 0 ~ 62	-		48h	78h	
64	Manufacturer JEDEC ID code	Sams	ung	CE	h	
65~71	Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang	Korea	01	lh	
73	Manufacturer part # (Memory module)	M		40	Dh	
74	Manufacturer part # (DIMM configuration)	3		33	3h	
75	Manufacturer part # (Data bits)	Blan	ık	20)h	
76	Manufacturer part # (Data bits)	7		37	7 h	
77	Manufacturer part # (Data bits)	7		37	7 h	
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	3		33h		
80	Manufacturer part # (Module depth)	3		33h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)	3		33h		
83	Manufacturer part # (Component revision)	A		41h		
84	Manufacturer part # (Package type)	Т		54h		
85	Manufacturer part # (PCB revision & type)	0		30h		
86	Manufacturer part # (Hyphen)	"-"	•	20	Dh	
87	Manufacturer part # (Power)	С		43	3h	
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	Н	L	48h	4Ch	
90	Manufacturer part # (TBD)	Blan	ık	20)h	
91	Manufacturer revision code (For PCB)	0		30)h	
92	Manufacturer revision code (For component)	A-die (2nd	d Gen.)	41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95~98	Assembly serial #	-		-		4
99~125	Manufacturer specific data (may be used in future)	Undefi	ned	-		5
126	System frequency for 100MHz	100M	Hz	64	1h	
127	Intel Specification details	Detailed 100MH	z Information	8Fh	8Dh	
128+	Unused storage locations	Undefi	ned	-		5

- 2. This value is based on the component specification.
- 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
- 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
- 5. These bytes are Undefined and can be used for Samsung's own purpose.



M377S6428AT3-C1H/C1L (1.2ver)

Organization: 64MX72Composition: 64MX4 *18

• Used component part #: K4S560632A-TC1H/C1L

of rows in module : 2 Rows# of banks in component : 4 banks

• Feature: 1,700 mil height & double sided component

• Refresh : 4K/64ms

Byte #	Function described	Function Supported		Hex	Note	
Byte #	r unction described	-1H	-1L	-1H	-1L	Note
0	# of bytes written into serial memory at module manufacturer	1281	oytes	8	30h	
1	Total # of bytes of SPD memory device	256bytes	s (2K-bit)	()8h	
2	Fundamental memory type	SDF	RAM	(04h	
3	# of row address on this assembly	1	2	C)Ch	1
4	# of column address on this assembly	1	1	0Bh		1
5	# of module Rows on this assembly	2 R	ows	02h		
6	Data width of this assembly	72	bits	4	48h	
7	Data width of this assembly		-	00h		
8	Voltage interface standard of this assembly	LV	ΓTL	()1h	
9	SDRAM cycle time from clock @CAS latency of 3	10ns	10ns	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	6ns	60h	60h	2
11	DIMM configuraion type	EC	CC	()2h	
12	Refresh rate & type	15.625us, supp	oort self refresh	8	30h	
13	Primary SDRAM width	х	4	()4h	
14	Error checking SDRAM width	х	4	04h		
15	Minimum clock dealy for back-to-back random column address	tCCD =	: 1CLK	01h		
16	SDRAM device attributes : Burst lengths supported	1, 2, 4 8	8 page	0Fh		
17	SDRAM device attributes : # of banks on SDRAM device	4 ba	anks	04h		
18	SDRAM device attributes : CAS latency	2	& 3	06h		
19	SDRAM device attributes : CS latency	0 0	CLK	01h		
20	SDRAM device attributes : Write latency	0.0	CLK	()1h	
21	SDRAM module attributes	address & con	uffered DQM, trol inputs and rd PLL	1Fh		
22	SDRAM device attributes : General	Burst Read S	ge tolerance, ingle bit Write auto precharge	C	0Eh	
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-	-	00h	00h	2
26	SDRAM access time @CAS latency of 1	-	-	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	20ns	14h	14h	
28	Minimum row active to row active delay (tRRD)	20ns	20ns	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	20ns	14h	14h	
30	Minimum activate precharge time (=tRAS)	50ns	50ns	32h	32h	
31	Module Row density	2 Rows o	of 256MB	4	10h	
32	Command and Address signal input setup time	21	าร	2	20h	
33	Command and Address signal input hold time	11	าร	1	I0h	
34	Data signal input setup time	21	าร	2	20h	



Byte #	Function described	Function	Supported	Hex value		Note
Бую #	r unction described	-1H	-1L	-1H	-1L	Note
35	Data signal input hold time	1	ns	10	Oh	
36~61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Current releas	e Intel spd 1.2A	1:	2h	
63	Checksum for bytes 0 ~ 62		-	E1h	11h	
64	Manufacturer JEDEC ID code	Sam	nsung	С	Eh	
65~71	Manufacturer JEDEC ID code	Sam	nsung	00h		
72	Manufacturing location	Onyan	g Korea	0	1h	
73	Manufacturer part # (Memory module)		M	41	Oh	
74	Manufacturer part # (DIMM configuration)		3	3:	3h	
75	Manufacturer part # (Data bits)	BI	ank	20	Oh	
76	Manufacturer part # (Data bits)		7	3	7h	
77	Manufacturer part # (Data bits)		7	3	7h	
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	6		36h		
80	Manufacturer part # (Module depth)	4		34h		
81	Manufacturer part # (Refresh, # of banks in Comp. & inter-	2		32h		
82	Manufacturer part # (Composition component)		8	38h		
83	Manufacturer part # (Component revision)		A	4	1h	
84	Manufacturer part # (Package type)		Т	54h		
85	Manufacturer part # (PCB revision & type)		3	33h		
86	Manufacturer part # (Hyphen)	"	- "	21	Oh	
87	Manufacturer part # (Power)		С	4:	3h	
88	Manufacturer part # (Minimum cycle time)	1	1	31h	31h	
89	Manufacturer part # (Minimum cycle time)	Н	L	48h	4Ch	
90	Manufacturer part # (TBD)	BI	ank	20	Oh	
91	Manufacturer revision code (For PCB)		3	3:	3h	
92	Manufacturer revision code (For component)	A-die (2	nd Gen.)	41h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-			-	3
95~98	Assembly serial #		-		-	4
99~125	Manufacturer specific data (may be used in future)	Und	efined		-	5
126	System frequency for 100MHz	100	MHz	6	4h	
127	Intel Specification details	Detailed 100N	/IHz Information	8Fh	8Dh	
128+	Unused storage locations	Und	efined		-	5

- 2. This value is based on the component specification.
- 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
- 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
- 5. These bytes are Undefined and can be used for Samsung's own purpose.

