

### 3.3 V 64M × 64/72-Bit SDRAM Modules

#### 168-pin Unbuffered DIMM Modules

- 168-pin unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications
- PC100-222 and PC133-333 versions
- Two bank 64M × 64 and 64M × 72 organization
- Optimized for byte-write non-parity or ECC applications
- Fully PC board layout compatible to INTEL's Rev. 1.0 module specification
- JEDEC standard Synchronous DRAMs (SDRAM)
- Programmed Latencies:
- Programmable  $\overline{\text{CAS}}$  Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs and outputs are LVTTTL compatible
- Serial Presence Detect with E<sup>2</sup>PROM
- Uses Infineon 256 Mbit SDRAM components in 32M × 8 organization and TSOPII-54 packages
- Gold contact pad, card size:  
133.35 mm × 31.75 mm × 4.00 mm (JEDEC MO-161-BA)

| Product Speed |       | CL | $t_{\text{RCD}}$ | $t_{\text{RP}}$ |
|---------------|-------|----|------------------|-----------------|
| -7.5          | PC133 | 3  | 3                | 3               |
| -8            | PC100 | 2  | 2                | 2               |

- Single + 3.3 V (± 0.3 V) power supply

- SDRAM Performance:

|                 |                        | -7.5  | -8    | Unit |
|-----------------|------------------------|-------|-------|------|
|                 |                        | PC133 | PC100 |      |
| $f_{\text{CK}}$ | Clock Frequency (max.) | 133   | 100   | MHz  |
| $t_{\text{AC}}$ | Clock Access time      | 5.4   | 6     | ns   |

The HYS 64V64220GU and HYS 72V64220GU are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organized as 64M × 64 and 64M × 72 in two banks high speed memory arrays designed with 256M Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use 7-5 speed sorted 256 Mbit Synchronous DRAMs (SDRAMs) to meet the PC133-333 requirements and -8 components for the standard PC100 applications. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL's PC100 module specification. The DIMMs have a serial presence detect, implemented with a serial E<sup>2</sup>PROM using the 2-pin I<sup>2</sup>C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All Infineon 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint, with 1.25" (31.75 mm) height.

**Ordering Information**

| Type                  | Code          | Package      | Descriptions                       | Module Height |
|-----------------------|---------------|--------------|------------------------------------|---------------|
| HYS 64V64220GU-7.5-C2 | PC133-333-520 | L-DIM-168-30 | PC133 64M × 64 2 bank SDRAM module | 1.25"         |
| HYS 72V64220GU-7.5-C2 | PC133-333-520 | L-DIM-168-30 | PC133 64M × 72 2 bank SDRAM module | 1.25"         |
| HYS 64V64220GU-8-C2   | PC100-222-620 | L-DIM-168-30 | PC100 64M × 64 2 bank SDRAM module | 1.25"         |
| HYS 72V64220GU-8-C2   | PC100-222-620 | L-DIM-168-30 | PC100 64M × 72 2 bank SDRAM module | 1.25"         |

*Note: All part numbers end with a place code, designating the die revision. Consult factory for current revision. Example: HYS 64V64220GU-8-C2, indicating Rev.C2 dies are used for SDRAM components.*

**Pin Definitions and Functions**

|                  |                                    |                                   |                                     |
|------------------|------------------------------------|-----------------------------------|-------------------------------------|
| A0 - A12         | Address Inputs                     | CLK0 - CLK3                       | Clock Input                         |
| BA0, BA1         | Bank Selects                       | DQMB0 - DQMB7                     | Data Mask                           |
| DQ0 - DQ63       | Data Input/Output                  | $\overline{CS0} - \overline{CS3}$ | Chip Select                         |
| CB0 - CB7        | Check Bits (x72 organization only) | $V_{DD}$                          | Power (+ 3.3 V)                     |
| $\overline{RAS}$ | Row Address Strobe                 | $V_{SS}$                          | Ground                              |
| $\overline{CAS}$ | Column Address Strobe              | SCL                               | Clock for Presence Detect           |
| $\overline{WE}$  | Read/Write Input                   | SDA                               | Serial Data Out for Presence Detect |
| CKE0, CKE1       | Clock Enable                       | N.C./DU                           | No Connection                       |

**Address Format**

|             | Part Number      | Rows | Columns | Bank Select | Refresh | Period | Interval |
|-------------|------------------|------|---------|-------------|---------|--------|----------|
| 64M × 64/72 | HYS64/72V64220GU | 13   | 10      | 2           | 8k      | 64 ms  | 7.8 μs   |

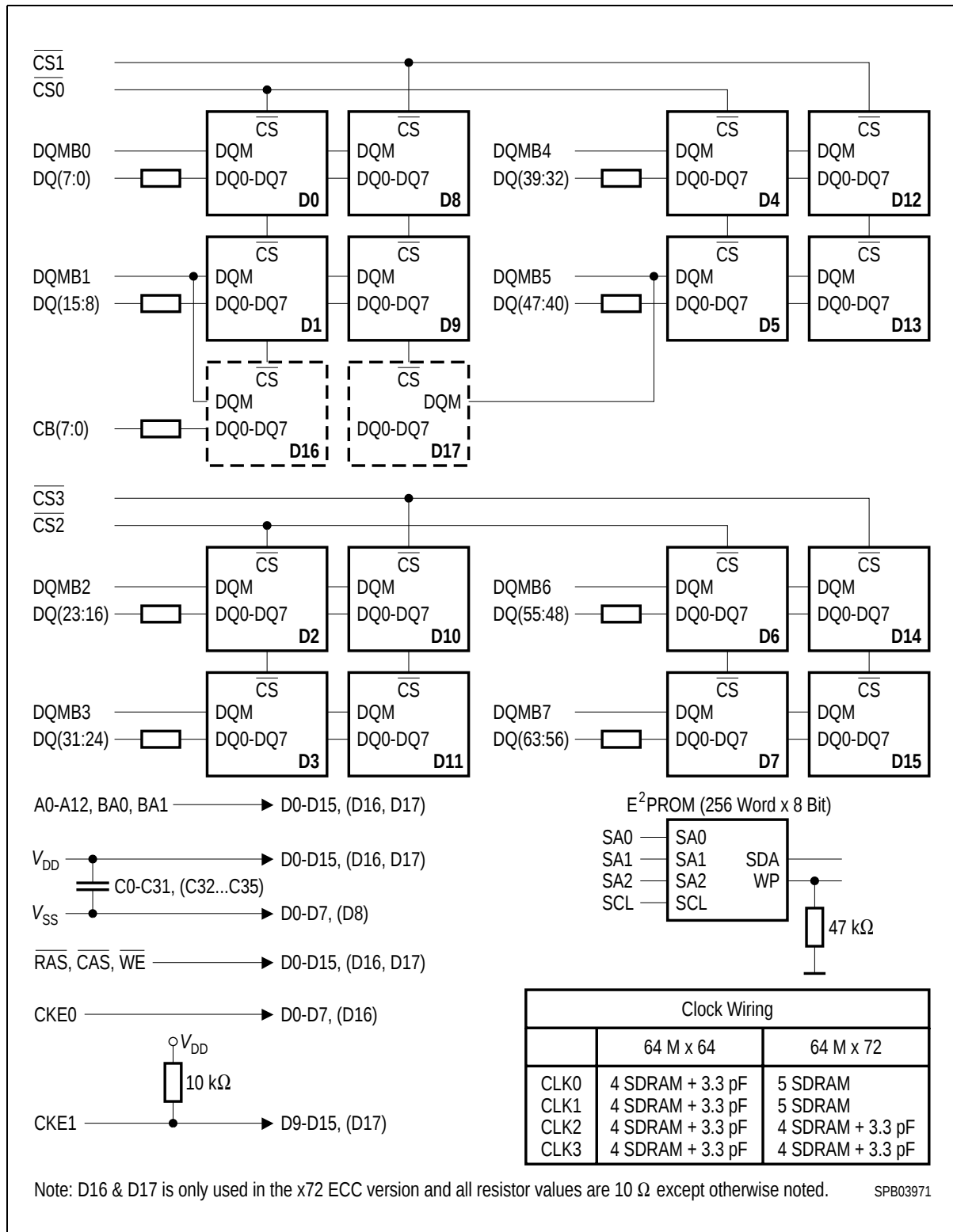
**Pin Configuration**

| PIN# | Symbol   | PIN# | Symbol           | PIN# | Symbol   | PIN# | Symbol           |
|------|----------|------|------------------|------|----------|------|------------------|
| 1    | $V_{SS}$ | 43   | $V_{SS}$         | 85   | $V_{SS}$ | 127  | $V_{SS}$         |
| 2    | DQ0      | 44   | DU               | 86   | DQ32     | 128  | CKE0             |
| 3    | DQ1      | 45   | $\overline{CS2}$ | 87   | DQ33     | 129  | $\overline{CS3}$ |
| 4    | DQ2      | 46   | DQMB2            | 88   | DQ34     | 130  | DQMB6            |
| 5    | DQ3      | 47   | DQMB3            | 89   | DQ35     | 131  | DQMB7            |
| 6    | $V_{DD}$ | 48   | DU               | 90   | $V_{DD}$ | 132  | N.C.             |
| 7    | DQ4      | 49   | $V_{DD}$         | 91   | DQ36     | 133  | $V_{DD}$         |
| 8    | DQ5      | 50   | N.C.             | 92   | DQ37     | 134  | N.C.             |
| 9    | DQ6      | 51   | N.C.             | 93   | DQ38     | 135  | N.C.             |
| 10   | DQ7      | 52   | N.C. (CB2)       | 94   | DQ39     | 136  | CB6              |
| 11   | DQ8      | 53   | N.C. (CB3)       | 95   | DQ40     | 137  | CB7              |
| 12   | $V_{SS}$ | 54   | $V_{SS}$         | 96   | $V_{SS}$ | 138  | $V_{SS}$         |
| 13   | DQ9      | 55   | DQ16             | 97   | DQ41     | 139  | DQ48             |
| 14   | DQ10     | 56   | DQ17             | 98   | DQ42     | 140  | DQ49             |
| 15   | DQ11     | 57   | DQ18             | 99   | DQ43     | 141  | DQ50             |
| 16   | DQ12     | 58   | DQ19             | 100  | DQ44     | 142  | DQ51             |
| 17   | DQ13     | 59   | $V_{DD}$         | 101  | DQ45     | 143  | $V_{DD}$         |
| 18   | $V_{DD}$ | 60   | DQ20             | 102  | $V_{DD}$ | 144  | DQ52             |

**Pin Configuration (cont'd)**

| PIN# | Symbol                  | PIN# | Symbol          | PIN# | Symbol                  | PIN# | Symbol          |
|------|-------------------------|------|-----------------|------|-------------------------|------|-----------------|
| 19   | DQ14                    | 61   | N.C.            | 103  | DQ46                    | 145  | N.C.            |
| 20   | DQ15                    | 62   | DU              | 104  | DQ47                    | 146  | DU              |
| 21   | N.C. (CB0)              | 63   | CKE1            | 105  | N.C. (CB4)              | 147  | N.C.            |
| 22   | N.C. (CB1)              | 64   | V <sub>SS</sub> | 106  | N.C. (CB5)              | 148  | V <sub>SS</sub> |
| 23   | V <sub>SS</sub>         | 65   | DQ21            | 107  | V <sub>SS</sub>         | 149  | DQ53            |
| 24   | N.C.                    | 66   | DQ22            | 108  | N.C.                    | 150  | DQ54            |
| 25   | N.C.                    | 67   | DQ23            | 109  | N.C.                    | 151  | DQ55            |
| 26   | V <sub>DD</sub>         | 68   | V <sub>SS</sub> | 110  | V <sub>DD</sub>         | 152  | V <sub>SS</sub> |
| 27   | $\overline{\text{WE}}$  | 69   | DQ24            | 111  | $\overline{\text{CAS}}$ | 153  | DQ56            |
| 28   | DQMB0                   | 70   | DQ25            | 112  | DQMB4                   | 154  | DQ57            |
| 29   | DQMB1                   | 71   | DQ26            | 113  | DQMB5                   | 155  | DQ58            |
| 30   | $\overline{\text{CS0}}$ | 72   | DQ27            | 114  | $\overline{\text{CS1}}$ | 156  | DQ59            |
| 31   | DU                      | 73   | V <sub>DD</sub> | 115  | $\overline{\text{RAS}}$ | 157  | V <sub>DD</sub> |
| 32   | V <sub>SS</sub>         | 74   | DQ28            | 116  | V <sub>SS</sub>         | 158  | DQ60            |
| 33   | A0                      | 75   | DQ29            | 117  | A1                      | 159  | DQ61            |
| 34   | A2                      | 76   | DQ30            | 118  | A3                      | 160  | DQ62            |
| 35   | A4                      | 77   | DQ31            | 119  | A5                      | 161  | DQ63            |
| 36   | A6                      | 78   | V <sub>SS</sub> | 120  | A7                      | 162  | V <sub>SS</sub> |
| 37   | A8                      | 79   | CLK2            | 121  | A9                      | 163  | CLK3            |
| 38   | A10                     | 80   | N.C.            | 122  | BA0                     | 164  | N.C.            |
| 39   | BA1                     | 81   | WP              | 123  | A11                     | 165  | SA0             |
| 40   | V <sub>DD</sub>         | 82   | SDA             | 124  | V <sub>DD</sub>         | 166  | SA1             |
| 41   | V <sub>DD</sub>         | 83   | SCL             | 125  | CLK1                    | 167  | SA2             |
| 42   | CLK0                    | 84   | V <sub>DD</sub> | 126  | A12                     | 168  | V <sub>DD</sub> |

Note: Pin names in paranthese are for the x72 ECC versions; example: Pin 106 = (CB5)



**Block Diagram: 64M × 64/72 Two Bank SDRAM DIMM Modules**

**DC Characteristics**
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{SS} = 0 \text{ V}; V_{DD}, V_{DDQ} = 3.3 \text{ V} \pm 0.3 \text{ V}$ 

| Parameter                                                                                              | Symbol     | Limit Values |                | Unit          |
|--------------------------------------------------------------------------------------------------------|------------|--------------|----------------|---------------|
|                                                                                                        |            | min.         | max.           |               |
| Input High Voltage                                                                                     | $V_{IH}$   | 2.0          | $V_{DD} + 0.3$ | V             |
| Input Low Voltage                                                                                      | $V_{IL}$   | - 0.5        | 0.8            | V             |
| Output High Voltage ( $I_{OUT} = - 4.0 \text{ mA}$ )                                                   | $V_{OH}$   | 2.4          | -              | V             |
| Output Low Voltage ( $I_{OUT} = 4.0 \text{ mA}$ )                                                      | $V_{OL}$   | -            | 0.4            | V             |
| Input Leakage Current, any input<br>( $0 \text{ V} < V_{IN} < 3.6 \text{ V}$ , all other inputs = 0 V) | $I_{I(L)}$ | - 40         | 40             | $\mu\text{A}$ |
| Output Leakage Current<br>(DQ is disabled, $0 \text{ V} < V_{OUT} < V_{DD}$ )                          | $I_{O(L)}$ | - 40         | 40             | $\mu\text{A}$ |

**Capacitance**
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}, f = 1 \text{ MHz}$ 

| Parameter                                                                                                               | Symbol    | Limit Values            |                         | Unit |
|-------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------|-------------------------|------|
|                                                                                                                         |           | max.<br>64M $\times$ 64 | max.<br>64M $\times$ 72 |      |
| Input Capacitance<br>(A0 to A11, BA0, BA1, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ ) | $C_{I1}$  | 105                     | 144                     | pF   |
| Input Capacitance ( $\overline{\text{CS0}}$ - $\overline{\text{CS3}}$ )                                                 | $C_{I2}$  | 32                      | 40                      | pF   |
| Input Capacitance (CLK0 - CLK3)                                                                                         | $C_{ICL}$ | 40                      | 43                      | pF   |
| Input Capacitance (CKE0, CKE1)                                                                                          | $C_{I3}$  | 65                      | 72                      | pF   |
| Input Capacitance (DQMB0 - DQMB7)                                                                                       | $C_{I4}$  | 20                      | 25                      | pF   |
| Input/Output Capacitance<br>(DQ0 - DQ63, CB0 - CB7)                                                                     | $C_{IO}$  | 17                      | 17                      | pF   |
| Input Capacitance (SCL, SA0-2)                                                                                          | $C_{SC}$  | 8                       | 8                       | pF   |
| Input/Output Capacitance                                                                                                | $C_{SD}$  | 8                       | 8                       | pF   |

**Operating Currents per SDRAM Component <sup>1)</sup>**
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ 

(Recommended Operating Conditions unless otherwise noted)

| Parameter                                                                                                                                                                                                                                 | Test Condition          | Symbol     | -7.5 | -8  | Unit | Note   |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|------------|------|-----|------|--------|
|                                                                                                                                                                                                                                           |                         |            | max. |     |      |        |
| Operating current<br><br>$t_{RC} = t_{RC(MIN.)}$ , $t_{CK} = t_{CK(MIN.)}$<br>Outputs open, Burst Length = 4, CL = 3<br>All banks operated in random access,<br>all banks operated in ping-pong manner<br>to maximize gapless data access | —                       | $I_{CC1}$  | 230  | 170 | mA   | 1)     |
| Precharge stand-by current<br>in Power Down Mode<br><br>$\overline{CS} = V_{IH(MIN.)}$ , $CKE \leq V_{IL(MAX.)}$                                                                                                                          | $t_{CK} = \text{min.}$  | $I_{CC2P}$ | 2    | 2   | mA   | 1)     |
| Precharge Stand-by Current<br>in Non-Power Down Mode<br><br>$\overline{CS} = V_{IH(MIN.)}$ , $CKE \geq V_{IH(MIN.)}$                                                                                                                      | $t_{CK} = \text{min.}$  | $I_{CC2N}$ | 40   | 30  | mA   | 1)     |
| No operating current<br><br>$t_{CK} = \text{min.}$ , $\overline{CS} = V_{IH(MIN.)}$ ,<br>active state (max. 4 banks)                                                                                                                      | $CKE \geq V_{IH(MIN.)}$ | $I_{CC3N}$ | 50   | 45  | mA   | 1)     |
|                                                                                                                                                                                                                                           | $CKE \leq V_{IL(MAX.)}$ | $I_{CC3P}$ | 10   | 10  | mA   | 1)     |
| Burst operating current<br>$t_{CK} = \text{min.}$ ,<br>Read command cycling                                                                                                                                                               | —                       | $I_{CC4}$  | 150  | 100 | mA   | 1), 2) |
| Auto refresh current<br>$t_{CK} = \text{min.}$ ,<br>Auto Refresh command cycling                                                                                                                                                          | —                       | $I_{CC5}$  | 240  | 220 | mA   | 1)     |
| Self refresh current<br>Self Refresh Mode, $CKE = 0.2 \text{ V}$                                                                                                                                                                          |                         | $I_{CC6}$  | 3    | 3   | mA   | 1)     |

**AC Characteristics** <sup>3), 4)</sup>
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{SS} = 0 \text{ V}; V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 1 \text{ ns}$ 

| Parameter | Symbol | Limit Values      |      |                 |      | Unit | Note |
|-----------|--------|-------------------|------|-----------------|------|------|------|
|           |        | -7.5<br>PC133-333 |      | -8<br>PC100-222 |      |      |      |
|           |        | min.              | max. | min.            | max. |      |      |

**Clock**

|                                     |          |     |     |    |     |     |        |
|-------------------------------------|----------|-----|-----|----|-----|-----|--------|
| Clock Cycle Time                    | $t_{CK}$ |     |     |    |     |     | —      |
| $\overline{\text{CAS}}$ Latency = 3 |          | 7.5 | —   | 10 | —   | ns  |        |
| $\overline{\text{CAS}}$ Latency = 2 |          | 12  | —   | 10 | —   | ns  |        |
| System Frequency                    | $f_{CK}$ |     |     |    |     |     | —      |
| $\overline{\text{CAS}}$ Latency = 3 |          | —   | 133 | —  | 100 | MHz |        |
| $\overline{\text{CAS}}$ Latency = 2 |          | —   | 100 | —  | 100 | MHz | *)     |
| for HYS64/72V64220GU-7.5-C2         |          |     |     |    |     |     |        |
| Clock Access Time                   | $t_{AC}$ |     |     |    |     |     | 4), 5) |
| $\overline{\text{CAS}}$ Latency = 3 |          | —   | 5.4 | —  | 6   | ns  |        |
| $\overline{\text{CAS}}$ Latency = 2 |          | —   | 6   | —  | 6   | ns  |        |
| Clock High Pulse Width              | $t_{CH}$ | 2.5 | —   | 3  | —   | ns  | 6)     |
| Clock Low Pulse Width               | $t_{CL}$ | 2.5 | —   | 3  | —   | ns  | 6)     |

**Setup and Hold Times**

|                                 |           |     |   |   |   |     |    |
|---------------------------------|-----------|-----|---|---|---|-----|----|
| Input Setup Time                | $t_{CS}$  | 1.5 | — | 2 | — | ns  | 7) |
| Input Hold Time                 | $t_{CH}$  | 0.8 | — | 1 | — | ns  | 7) |
| Power Down Mode Entry Time      | $t_{SB}$  | —   | 1 | — | 1 | CLK | 8) |
| Power Down Mode Exit Setup Time | $t_{PDE}$ | 1   | — | 1 | — | CLK | 9) |
| Mode Register Setup Time        | $t_{RSC}$ | 2   | — | 2 | — | CLK |    |
| Transition Time (rise and fall) | $t_T$     | 1   | — | 1 | — | ns  | —  |

**Common Parameters**

|                                                                           |           |      |      |    |      |     |   |
|---------------------------------------------------------------------------|-----------|------|------|----|------|-----|---|
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay                  | $t_{RCD}$ | 20   | —    | 20 | —    | ns  | — |
| Precharge Time                                                            | $t_{RP}$  | 20   | —    | 20 | —    | ns  | — |
| Active Command Period                                                     | $t_{RAS}$ | 45   | 100k | 50 | 100k | ns  | — |
| Cycle Time                                                                | $t_{RC}$  | 67.5 | —    | 70 | —    | ns  | — |
| Bank to Bank Delay Time                                                   | $t_{RRD}$ | 15   | —    | 16 | —    | ns  | — |
| $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay Time (same bank) | $t_{CCD}$ | 1    | —    | 1  | —    | CLK | — |

**AC Characteristics (cont'd)** <sup>3), 4)</sup>
 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{SS} = 0 \text{ V}; V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 1 \text{ ns}$ 

| Parameter | Symbol | Limit Values      |      |                 |      | Unit | Note |
|-----------|--------|-------------------|------|-----------------|------|------|------|
|           |        | -7.5<br>PC133-333 |      | -8<br>PC100-222 |      |      |      |
|           |        | min.              | max. | min.            | max. |      |      |

**Refresh Cycle**

|                              |            |   |    |   |    |     |                |
|------------------------------|------------|---|----|---|----|-----|----------------|
| Refresh Period (8192 cycles) | $t_{REF}$  | — | 64 | — | 64 | ms  | <sup>8)</sup>  |
| Self Refresh Exit Time       | $t_{SREX}$ | 1 | —  | 1 | —  | CLK | <sup>10)</sup> |

**Read Cycle**

|                              |           |   |   |   |   |     |                |
|------------------------------|-----------|---|---|---|---|-----|----------------|
| Data Out Hold Time           | $t_{OH}$  | 3 | — | 3 | — | ns  | <sup>4)</sup>  |
| Data Out to Low Impedance    | $t_{LZ}$  | 0 | — | 0 | — | ns  | —              |
| Data Out to High Impedance   | $t_{HZ}$  | 3 | 7 | 3 | 8 | ns  | <sup>11)</sup> |
| DQM Data Out Disable Latency | $t_{DQZ}$ | — | 2 | — | 2 | CLK | —              |

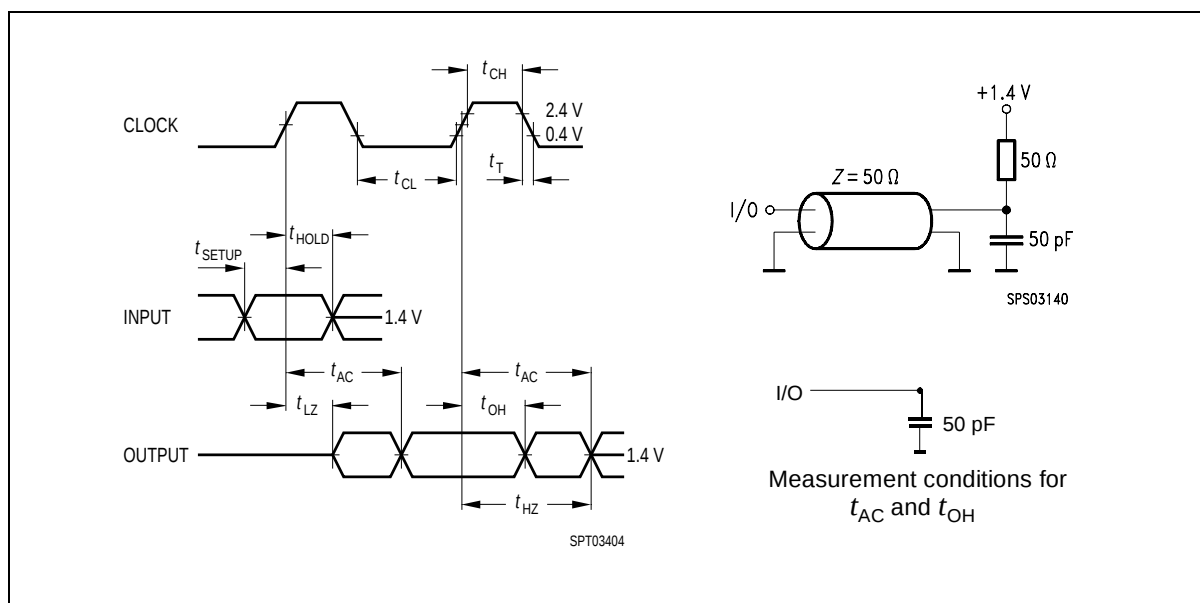
**Write Cycle**

|                                             |           |   |   |   |   |     |   |
|---------------------------------------------|-----------|---|---|---|---|-----|---|
| Data Input to Precharge<br>(write recovery) | $t_{WR}$  | 2 | — | 2 | — | CLK | — |
| DQM Write Mask Latency                      | $t_{DQW}$ | 0 | — | 0 | — | CLK | — |

**Notes**

- These parameters depend on the cycle rate. These values are measured at 133 MHz for -7.5 modules and at 100 Mhz for -8 modules. Input signals are changed once during  $t_{CK}$ , except for  $I_{CC6}$  and for standby currents when  $t_{CK} = \text{infinity}$ . All values are shown per memory component.
- These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 assumed and the  $V_{DDQ}$  current is excluded.
- All AC characteristics are shown on SDRAM component level.  
An initial pause of 100  $\mu\text{s}$  is required after power-up, then a Precharge All Banks command must be given followed by eight Auto-Refresh (CBR) cycles before the Mode Register Set Operation can begin.
- AC timing tests have  $V_{IL} = 0.4 \text{ V}$  and  $V_{IH} = 2.4 \text{ V}$  with the timing referenced to the 1.4 V crossover point. The transition time is measured between  $V_{IH}$  and  $V_{IL}$ . All AC measurements assume  $t_T = 1 \text{ ns}$  with the AC output load circuit show. Specified  $t_{AC}$  and  $t_{OH}$  parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.
- If clock rising time is longer than 1 ns, a time  $(t_T/2 - 0.5) \text{ ns}$  must be added to this parameter.

6. Rated at 1.4 V
7. If  $t_T$  is longer than 1 ns, a time  $(t_T - 1)$  ns has to be added to this parameter.
8. Anytime the Refresh Period has been exceeded, a minimum of two Auto-Refresh (CBR) commands must be given to "wake-up" the device.
9. Timing is asynchronous. If setup time is not met by rising edge of the clock then the CKE signal is assumed latched on the next cycle.
10. Self-Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self-Refresh Exit is not complete until a time period equal to  $t_{RC}$  is satisfied after the Self Refresh Exit command is registered.
11. This is referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.



**Note: \*)** 256MByte PC133 modules with place codes earlier than "-C2" (f.e. "A" and "B") are only backward compatible to PC100 3-2-2 when operating on a 100 Mhz memory bus.

A serial presence detect storage device - E<sup>2</sup>PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E<sup>2</sup>PROM device during module production using a serial presence detect protocol (I<sup>2</sup>C synchronous 2-wire bus).

**SPD-Table for PC133 Modules**

| Byte# | Description                                                           | SPD Entry Value                | Hex              |                  |
|-------|-----------------------------------------------------------------------|--------------------------------|------------------|------------------|
|       |                                                                       |                                | 64M × 64<br>-7.5 | 64M × 72<br>-7.5 |
| 0     | Number of SPD Bytes                                                   | 128                            | 80               | 80               |
| 1     | Total Bytes in Serial PD                                              | 256                            | 08               | 08               |
| 2     | Memory Type                                                           | SDRAM                          | 04               | 04               |
| 3     | Number of Row Addresses (without BS bits)                             | 13                             | 0D               | 0D               |
| 4     | Number of Column Addresses                                            | 10                             | 0A               | 0A               |
| 5     | Number of DIMM Banks                                                  | 2                              | 02               | 02               |
| 6     | Module Data Width                                                     | 64 /72                         | 40               | 48               |
| 7     | Module Data Width (cont'd)                                            | 0                              | 00               | 00               |
| 8     | Module Interface Levels                                               | LVTTL                          | 01               | 01               |
| 9     | SDRAM Cycle Time at CL = 3                                            | 7.5 ns                         | 75               | 75               |
| 10    | SDRAM Access Time from Clock at CL = 3                                | 5.4 ns                         | 54               | 54               |
| 11    | DIMM Config                                                           | none/ECC                       | 00               | 02               |
| 12    | Refresh Rate/Type                                                     | Self-Refresh, 7.8 μs           | 82               | 82               |
| 13    | SDRAM Width, Primary                                                  | x8                             | 08               | 08               |
| 14    | Error Checking SDRAM Data Width                                       | na / x8                        | 00               | 08               |
| 15    | Minimum Clock Delay for Back-to-Back Random Column Address            | $t_{CCD} = 1 \text{ CLK}$      | 01               | 01               |
| 16    | Burst Length Supported                                                | 1, 2, 4 & 8                    | 0F               | 0F               |
| 17    | Number of SDRAM Banks                                                 | 4                              | 04               | 04               |
| 18    | Supported CAS Latencies                                               | CAS latency = 2 & 3            | 06               | 06               |
| 19    | CS Latencies                                                          | CS latency = 0                 | 01               | 01               |
| 20    | WE Latencies                                                          | Write latency = 0              | 01               | 01               |
| 21    | SDRAM DIMM Module Attributes                                          | non buffered/non reg.          | 00               | 00               |
| 22    | SDRAM Device Attributes: General                                      | $V_{DD} \text{ tol } \pm 10\%$ | 0E               | 0E               |
| 23    | Min. Clock Cycle Time at CAS Latency = 2 for HYS64//72V64220GU-7.5-C2 | 10.0 ns                        | A0               | A0               |
| 24    | Max. Data Access Time from Clock for CL = 2                           | 6.0 ns                         | 60               | 60               |
| 25    | Minimum Clock Cycle Time at CL = 1                                    | not supported                  | FF               | FF               |
| 26    | Maximum Data Access Time from Clock at CL = 1                         | not supported                  | FF               | FF               |
| 27    | Minimum Row Precharge Time                                            | 20 ns                          | 14               | 14               |
| 28    | Minimum Row Active to Row Active Delay $t_{RRD}$                      | 15                             | 0F               | 0F               |
| 29    | Minimum RAS to CAS Delay $t_{RCD}$                                    | 20 ns                          | 14               | 14               |
| 30    | Minimum RAS Pulse Width $t_{RAS}$                                     | 45 ns                          | 2D               | 2D               |
| 31    | Module Bank Density (per bank)                                        | 256 MByte                      | 40               | 40               |
| 32    | SDRAM Input Setup Time                                                | 1.5 ns                         | 15               | 15               |

**SPD-Table for PC133 Modules (cont'd)**

| Byte#  | Description                                                | SPD Entry Value | Hex              |                  |
|--------|------------------------------------------------------------|-----------------|------------------|------------------|
|        |                                                            |                 | 64M × 64<br>-7.5 | 64M × 72<br>-7.5 |
| 33     | SDRAM Input Hold Time                                      | 0.8 ns          | 08               | 08               |
| 34     | SDRAM Data Input Hold Time                                 | 1.5 ns          | 15               | 15               |
| 35     | SDRAM Data Input Setup Time                                | 0.8 ns          | 08               | 08               |
| 36-61  | Superset Information (may be used in future)               | –               | FF               | FF               |
| 62     | SPD Revision                                               | Revision 1.2    | 12               | 12               |
| 63     | Checksum for Bytes 0 - 62<br>for HYS64/72V64220GU-7.5-C2   | –               | 37               | 49               |
| 64-125 | Manufacturers Information<br>(FF <sub>H</sub> if not used) | –               | XX               | XX               |
| 126    | Frequency Specification                                    |                 | 64               | 64               |
| 127    | 100 MHz Support Details<br>for HYS64/72V64220GU-7.5-C2     | –               | FF               | FF               |
| 128+   | Unused Storage Locations                                   | –               | FF               | FF               |

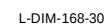
**SPD-Table for PC100 Modules**

| Byte# | Description                                                | SPD Entry Value           | Hex            |                |
|-------|------------------------------------------------------------|---------------------------|----------------|----------------|
|       |                                                            |                           | 64M × 64<br>-8 | 64M × 72<br>-8 |
| 0     | Number of SPD Bytes                                        | 128                       | 80             | 80             |
| 1     | Total Bytes in Serial PD                                   | 256                       | 08             | 08             |
| 2     | Memory Type                                                | SDRAM                     | 04             | 04             |
| 3     | Number of Row Addresses (without BS bits)                  | 13                        | 0D             | 0D             |
| 4     | Number of Column Addresses                                 | 10                        | 0A             | 0A             |
| 5     | Number of DIMM Banks                                       | 2                         | 02             | 02             |
| 6     | Module Data Width                                          | 64 / 72                   | 40             | 48             |
| 7     | Module Data Width (cont'd)                                 | 0                         | 00             | 00             |
| 8     | Module Interface Levels                                    | LVTTL                     | 01             | 01             |
| 9     | SDRAM Cycle Time at CL = 3                                 | 10.0 ns                   | A0             | A0             |
| 10    | SDRAM Access Time from Clock at CL = 3                     | 6.0 ns                    | 60             | 60             |
| 11    | DIMM Config                                                | none/ECC                  | 00             | 02             |
| 12    | Refresh Rate/Type                                          | Self-Refresh, 7.8 $\mu$ s | 82             | 82             |
| 13    | SDRAM Width, Primary                                       | x8                        | 08             | 08             |
| 14    | Error Checking SDRAM Data Width                            | na / x8                   | 00             | 08             |
| 15    | Minimum Clock Delay for Back-to-Back Random Column Address | $t_{CCD} = 1 \text{ CLK}$ | 01             | 01             |
| 16    | Burst Length Supported                                     | 1, 2, 4 & 8               | 0F             | 0F             |
| 17    | Number of SDRAM Banks                                      | 4                         | 04             | 04             |
| 18    | Supported CAS Latencies                                    | CAS latency = 2 & 3       | 06             | 06             |
| 19    | CS Latencies                                               | CS latency = 0            | 01             | 01             |
| 20    | WE Latencies                                               | Write latency = 0         | 01             | 01             |
| 21    | SDRAM DIMM Module Attributes                               | non buffered/non reg.     | 00             | 00             |
| 22    | SDRAM Device Attributes: General                           | $V_{DD}$ tol +/- 10%      | 0E             | 0E             |
| 23    | Min. Clock Cycle Time at CAS Latency = 2                   | 10.0ns                    | A0             | A0             |
| 24    | Max. Data Access Time from Clock for CL = 2                | 6.0 ns                    | 60             | 60             |
| 25    | Minimum Clock Cycle Time at CL = 1                         | not supported             | FF             | FF             |
| 26    | Maximum Data Access Time from Clock at CL = 1              | not supported             | FF             | FF             |
| 27    | Minimum Row Precharge Time                                 | 20 ns                     | 14             | 14             |
| 28    | Minimum Row Active to Row Active Delay $t_{RRD}$           | 16 ns                     | 10             | 10             |
| 29    | Minimum RAS to CAS Delay $t_{RCD}$                         | 20 ns                     | 14             | 14             |
| 30    | Minimum RAS Pulse Width $t_{RAS}$                          | 50 ns                     | 32             | 32             |
| 31    | Module Bank Density (per bank)                             | 256 MByte                 | 40             | 40             |
| 32    | SDRAM Input Setup Time                                     | 2 ns                      | 20             | 20             |
| 33    | SDRAM Input Hold Time                                      | 1 ns                      | 10             | 10             |

**SPD-Table for PC100 Modules**

| Byte#  | Description                                  | SPD Entry Value | Hex            |                |
|--------|----------------------------------------------|-----------------|----------------|----------------|
|        |                                              |                 | 64M × 64<br>-8 | 64M × 72<br>-8 |
| 34     | SDRAM Data Input Setup Time                  | 2 ns            | 20             | 20             |
| 35     | SDRAM Data Input Hold Time                   | 1 ns            | 10             | 10             |
| 36-61  | Superset Information (may be used in future) | –               | FF             | FF             |
| 62     | SPD Revision                                 | Revision 1.2    | 12             | 12             |
| 63     | Checksum for Bytes 0 - 62                    | –               | 9A             | AC             |
| 64-125 | Manufacturers Information                    | –               | XX             | XX             |
| 126    | Frequency Specification                      | 100 MHz         | 64             | 64             |
| 127    | 100 MHz Support Details                      | –               | FF             | FF             |
| 128+   | Unused Storage Locations                     | –               | FF             | FF             |

**L-DIM-168-30 (JEDEC MO-161-BA)  
SDRAM DIMM Module Package  
HYS 64/72V64220GU**



**Change List:**

|           |                                                                                                                                                                                                                                                                                                      |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14.1.1999 | Input capacitances adjusted                                                                                                                                                                                                                                                                          |
| 18.4.1999 | -8A speed sort added<br>Infineon logo added<br>SPD codes updated according to new 256M speedsorts                                                                                                                                                                                                    |
| 12.5.99   | Some ICC current values changed due to new inputs                                                                                                                                                                                                                                                    |
| 3.8.99    | PC133 merged into this datasheet                                                                                                                                                                                                                                                                     |
| 23.8.99   | Byte 126 changed to 64h for PC133 modules                                                                                                                                                                                                                                                            |
| 6.9.99    | Template from R&L                                                                                                                                                                                                                                                                                    |
| 20.10.99  | CL=2 max. frequency changed to 83 Mhz for -7.5 modules                                                                                                                                                                                                                                               |
| 2.12.99   | Some timing parameters adjusted according to INTELs PC133 specification                                                                                                                                                                                                                              |
| 20.1.2000 | Capacitance values for x72 adjusted (new measurements)                                                                                                                                                                                                                                               |
| 10.3.2000 | Implemented differences between 256Mbit S20 and S17 PC133 modules<br>256Mbit S20 based PC133 modules are backward compatible to PC100 3-2-2<br>256Mbit S17 based modules are backwards compatible to PC100-2-2-2<br>leading to changes in SPD code of bytes 23, 63 (checksum) and 126<br>TPCR issued |
| 10.5.2000 | Reference to JEDEC MO-161-BA added                                                                                                                                                                                                                                                                   |
| 5.03.2001 | -8A and -8B speed sorts removed<br>PC133 timing parameters only for 256M S17 and later versions<br>References to 256M S20 removed<br>ICC currents according to 256M S17 datasheet                                                                                                                    |