HY628100A Series

128K x 8-bit CMOS SRAM

PRELIMINARY

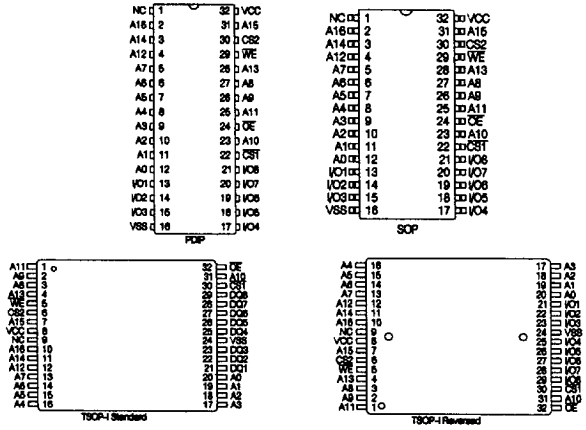
DESCRIPTION

The HY628100A is a high-speed, low power and 131,072 x 8-bits CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 55ns. The HY628100A has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY628100A Series.

FEATURES

- **High speed- 55/70/85/100ns (max.)**
- **Low power consumption**
  - **Operating : 25mW (typ.)**
  - **Standby (CMOS) : 5μw (typ.)**
- **Single 5V±10% power supply**
- **Battery backup (L/LL-part)**
  - **2.0V (min.) data retention**
- **Fully static operation**
  - **No clock or refresh required**
- **TTL compatible inputs and outputs**
- **Tri-state output**
- **Standard pin configuration**
  - **32 pin 600 mil PDIP**
  - **32 pin 525 mil SOP**
  - **32 pin 8x20 mm TSOP-I**

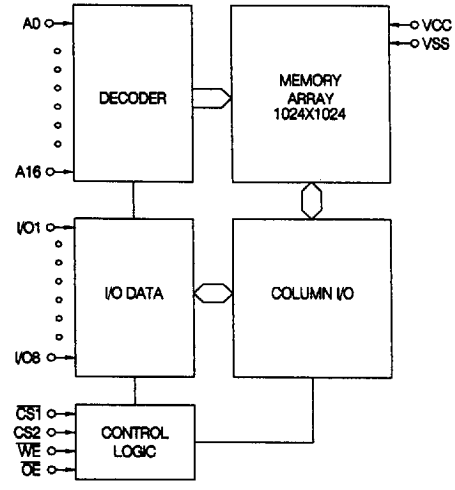
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
$\overline{CS1}$	Chip Select 1
CS2	Chip Select 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A16	Address Inputs
I/O1-I/O8	Data Input/Output
Vcc	Power(+5V)
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_{IN}, V_{OUT}	Power Supply,Input/Output Voltage	-0.5 to 7.0	V
T_A	Operating Temperature	0 to 70	°C
T_{BIAS}	Temperature Under Bias	-10 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260 • 10	°C • sec

Note:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.5	V
V_{IL}	Input Low Voltage	-0.5[1]	-	0.8	V

Note:
1. V_{IL} = -3.0V for pulse width less than 50ns.

TRUTH TABLE

MODE	I/O OPERATION	$\overline{CS1}$	CS2	WE	OE
Standby	High-Z	H	X	X	X
	High-Z	X	L	X	X
Output Disabled	High-Z	L	H	H	H
Read	Data Out	L	H	H	L
Write	Data in	L	H	L	X

Note:
1.H=V_{IH}, L=V_{IL}, X=Don't Care

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V± 10%, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	POWER	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		-1	-	1	μA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$ = V_{IL}		-1	-	1	μA
I_{CC}	Operating Power Supply Current	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0mA		-	5	10	mA
I_{CC1}	Average Operating Current	$\overline{CS1}$=V_{IL}, CS2=V_{IH} Min. Duty Cycle=100%, $I_{I/O}$=0mA		-	40	70	mA
I_{SB}	TTL Standby Current (TTL Inputs)	$\overline{CS1}$=V_{IH} or CS2=V_{IL}		-	1	2	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	$\overline{CS1}$ ≥ V_{CC}-0.2V, CS2 ≤ 0.2V or CS2 ≥ V_{CC}-0.2V		-	-	1	mA
			L	-	2	100	μA
			LL	-	1	20	μA
V_{OL}	Output Low Voltage	I_{OL} =2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA		2.4	-	-	V

Note:
1. Typical values are at V_{CC}=5.0V, T_A=25°C

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V ±10%, unless otherwise noted.)

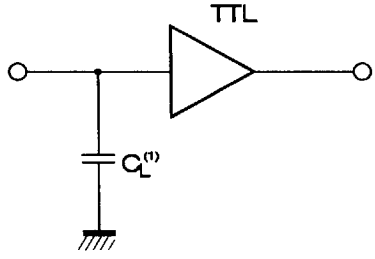
#	SYMBOL	PARAMETER	-55		-70		-85		-10		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	READ CYCLE										
1	t_{RC}	Read Cycle Time	55	-	70	-	85	-	100	-	ns
2	t_{AA}	Address Access Time	-	55	-	70	-	85	-	100	ns
3	t_{ACS}	Chip Select Access Time	-	55	-	60	-	85	-	100	ns
4	t_{OE}	Output Enable to Output Valid	-	25	-	35	-	45	-	50	ns
5	t_{CLZ}	Chip Select to Low -Z Output	10	-	10	-	10	-	10	-	ns
6	t_{OLZ}	Output Enable to Low-Z Output	5	-	5	-	5	-	5	-	ns
7	t_{CHZ}	Chip Disable to High -Z Output	0	20	0	25	0	30	0	30	ns
8	t_{OHZ}	Output Disable to High -Z Output	0	20	0	25	0	30	0	30	ns
9	t_{OH}	Output Hold from Address Change	10	-	10	-	10	-	10	-	ns
	WRITE CYCLE										
10	t_{WC}	Write Cycle Time	55	-	70	-	85	-	100	-	ns
11	t_{CW}	Chip Select to End of Write	45	-	60	-	70	-	80	-	ns
12	t_{AW}	Address Valid to End of Write	45	-	60	-	70	-	80	-	ns
13	t_{AS}	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	t_{WP}	Write Pluse Width	40	-	50	-	55	-	60	-	ns
15	t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	t_{WHZ}	Write to High-Z Output	0	20	0	25	0	30	0	30	ns
17	t_{DW}	Data to Write Time Overlap	25	-	30	-	35	-	40	-	ns
18	t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
19	t_{OW}	Output Active from End of Write	5	-	5	-	5	-	5	-	ns

AC TEST CONDITIONS

(T_A=0°C to 70°C, V_{CC}=5V ± 10%, unless otherwise specified.)

PARAMETER	VALUE
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference levels	1.5V
Output Load	C_L=100pF + 1TTL Load

AC TEST LOADS



Note:
1. Including jig and scope capacitance.

CAPACITANCE

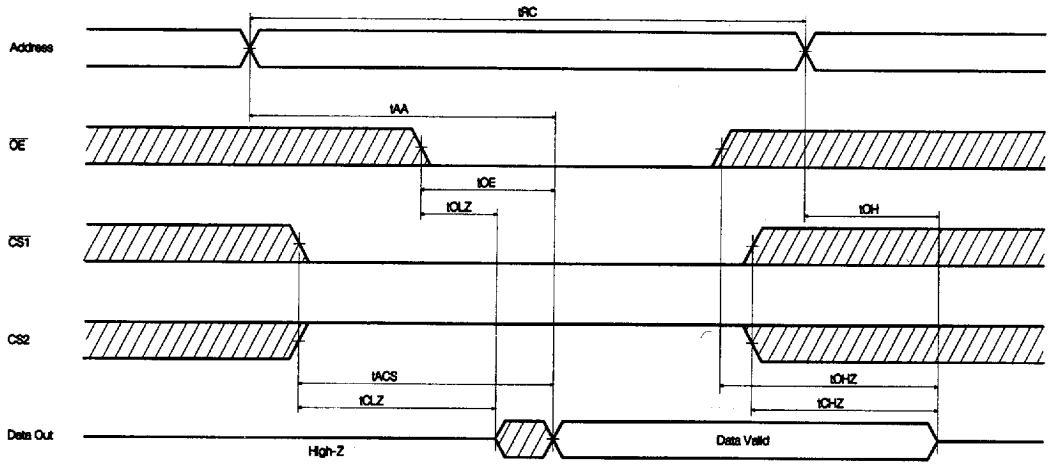
(T_A=25°C, f= 1MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

Note:
1. This parameter is sampled and not 100% tested.

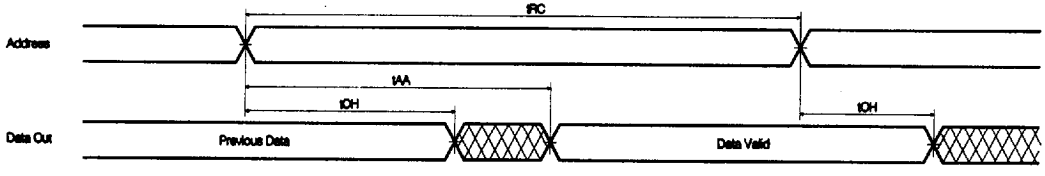
TIMING DIAGRAM

READ CYCLE 1



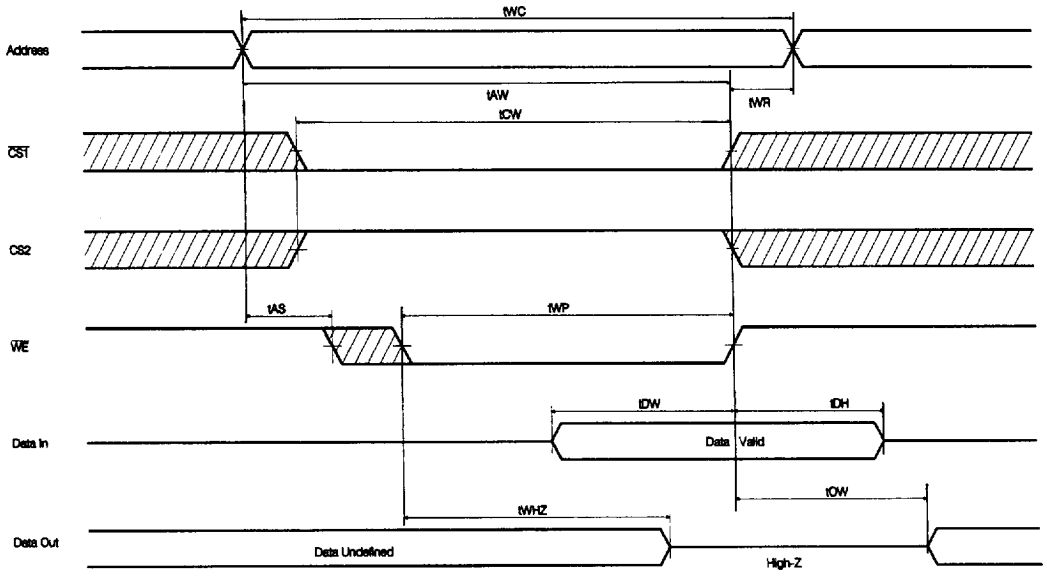
Note (READ CYCLE):
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.

READ CYCLE 2

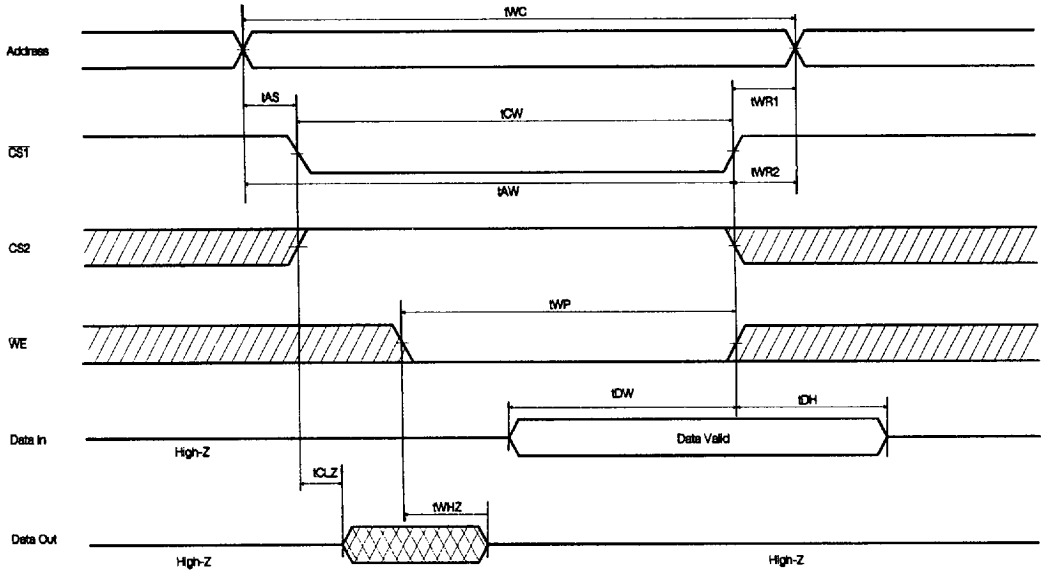


Note(READ CYCLE):
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CS1}$=V_{IL}, CS2=V_{IH}.
3. $\overline{OE}$=V_{IL}.

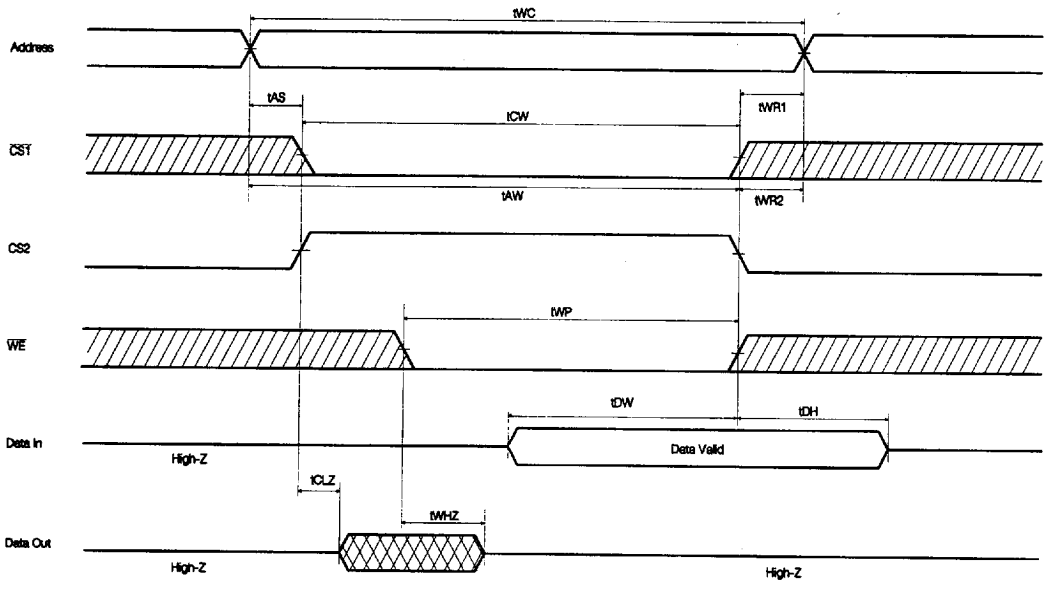
WRITE CYCLE 1 ($\overline{WE}$ Controlled)



WRITE CYCLE 2($\overline{CS1}$ Controlled)



WRITE CYCLE 3 (CS2 Controlled)



Note (WRITE CYCLE):

1. A write occurs during the overlap of a low $\overline{CS1}$ and high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

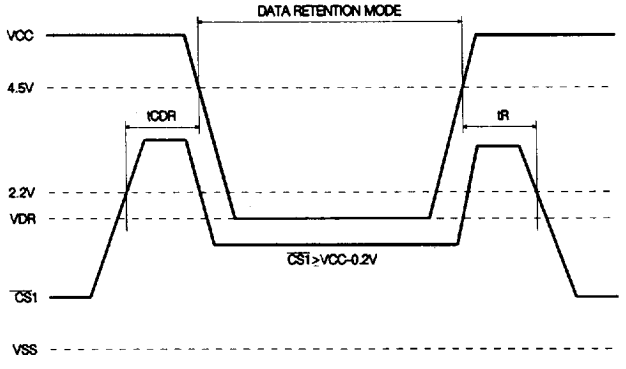
DATA RETENTION CHARACTERISTICS

(T_A=0°C to 70°C)

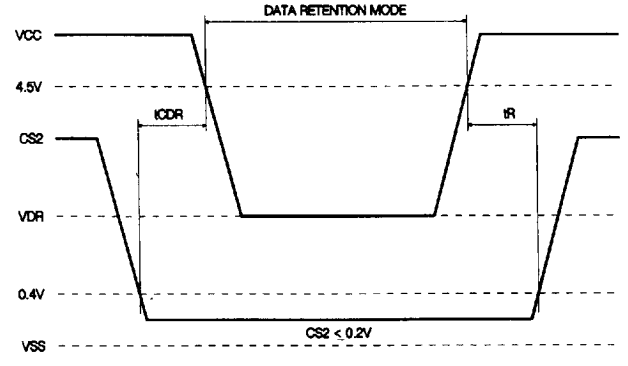
SYMBOL	PARAMETER	TEST CONDITION	POWER	MIN.	TYP.	MAX	UNIT
V_{DR}	V_{CC} for Data Retention	$\overline{CS1} \geq V_{CC}$-0.2V, CS2 ≤ 0.2V or ≥ V_{CC}-0.2V, $V_{SS} \leq V_{IN} \leq V_{CC}$		2.0	-	-	V
I_{CCDR}	Data Retention Current	V_{CC}=3.0V, $\overline{CS1} \geq V_{CC}$ -0.2V, CS2 ≤ 0.2V or ≥ V_{CC}-0.2V, $V_{SS} \leq V_{IN} \leq V_{CC}$	L	-	2	50	µA
			LL	-	1	10	µA
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
t_R	Operating Recovery Time			t_{RC}(2)	-	-	ns

Notes :
1. Typical values are at the condition of T_A=25°C.
2. t_{RC} is read cycle time.

DATA RETENTION TIMING DIAGRAM 1

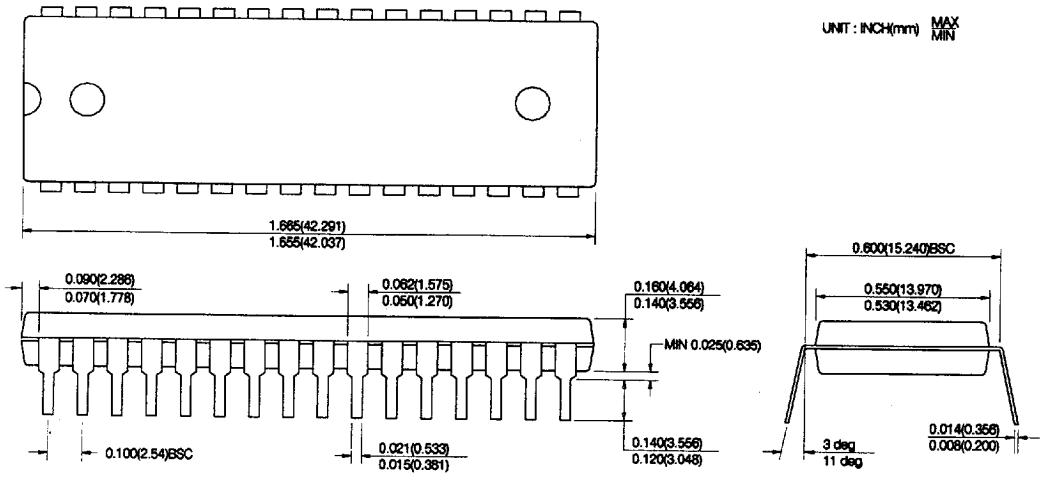


DATA RETENTION TIMING DIAGRAM 2

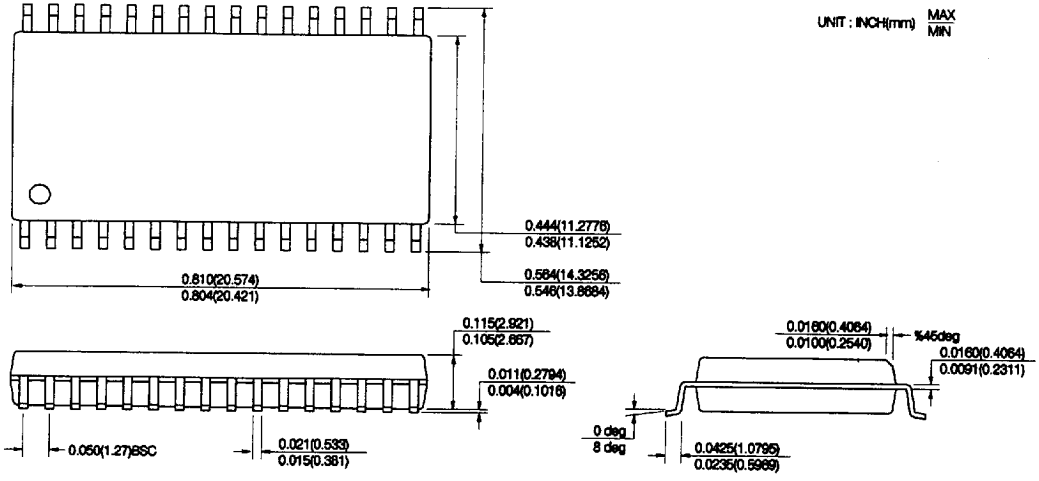


PACKAGE INFORMATION

600 mil 32 pin Plastic Dual In Line Package (P)

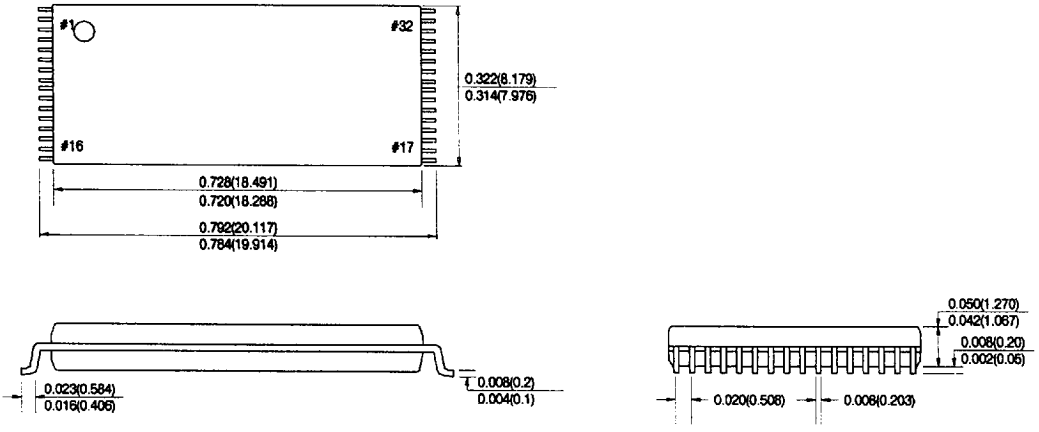


525mil 32 pin Small Outline Package (G)



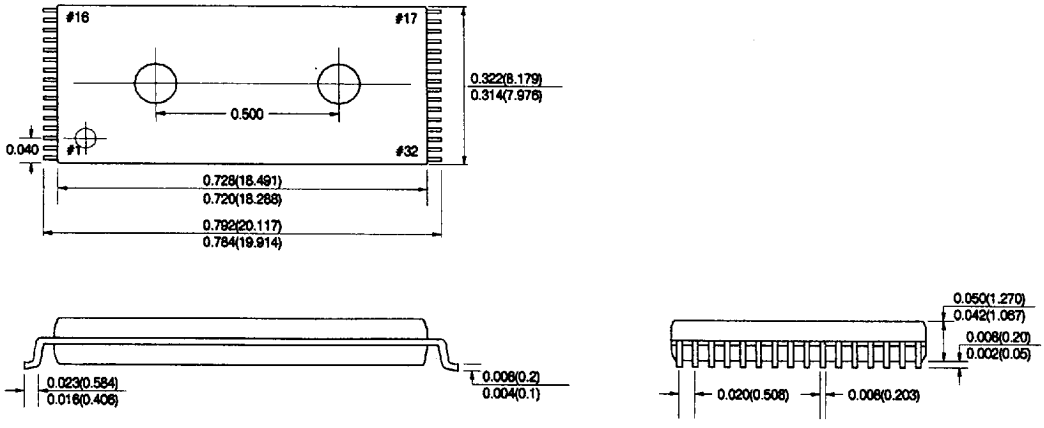
32 pin Thin Small Outline Package 8 x 20 mm Standard (T1)

UNIT : INCH(mm)



32 pin Thin Small Outline Package 8 x 20 mm Reversed (R1)

UNIT : INCH(mm)



ORDERING INFORMATION

PART NO.	SPEED	POWER	PACKAGE
HY628100AP	55/70/85/100		PDIP
HY628100ALP	55/70/85/100	L-Part	PDIP
HY628100ALLP	55/70/85/100	LL-part	PDIP
HY628100AG	55/70/85/100		SOP
HY628100ALG	55/70/85/100	L-Part	SOP
HY628100ALLG	55/70/85/100	LL-Part	SOP
HY628100AT1	55/70/85/100		TSOP-I Standard
HY628100ALT1	55/70/85/100	L-Part	TSOP-I Standard
HY628100ALLT1	55/70/85/100	LL-Part	TSOP-I Standard
HY628100AR1	55/70/85/100		TSOP-I Reversed
HY628100ALR1	55/70/85/100	L-Part	TSOP-I Reversed
HY628100ALLR1	55/70/85/100	LL-Part	TSOP-I Reversed