

FEATURES

- LOW BIAS CURRENT — FET Input
- PROTECTED OUTPUT STAGE — Thermal Shutoff
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — $\pm 12\text{V}$ TO $\pm 50\text{V}$
- HIGH OUTPUT CURRENT — $\pm 5\text{A}$ Peak

APPLICATIONS

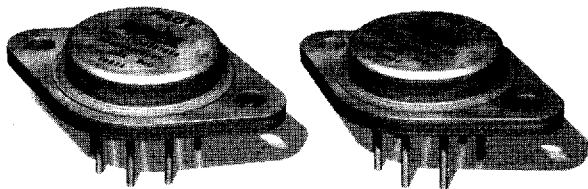
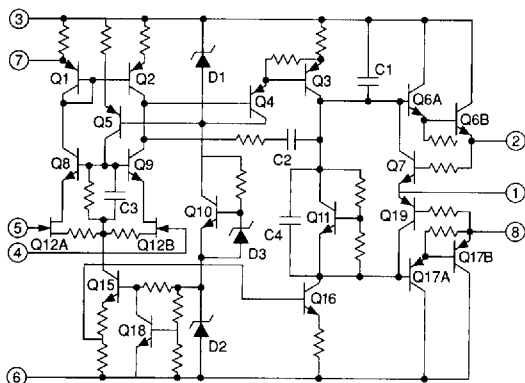
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

DESCRIPTION

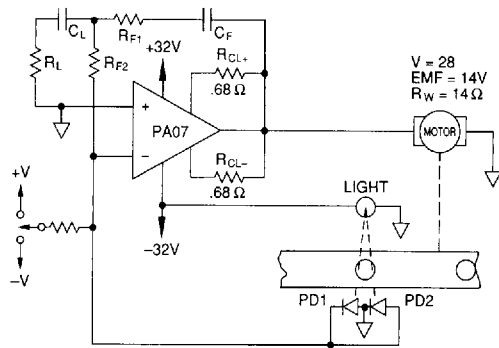
The PA07 is a high voltage, high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. A thermal shutoff circuit protects against overheating and minimizes heatsink requirements for abnormal operating conditions. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



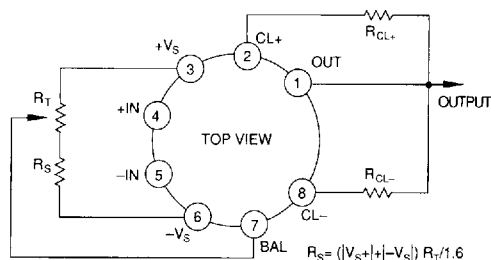
TYPICAL APPLICATION



Negates optoelectronic instabilities
Lead network minimizes overshoot
SEQUENTIAL POSITION CONTROL

Position is sensed by the differentially connected photo diodes, a method that negates the time and temperature variations of the optical components. Off center positions produce an error current which is integrated by the op amp circuit, driving the system back to center position. A momentary switch contact forces the system out of lock and then the integrating capacitor holds drive level while both diodes are in a dark state. When the next index point arrives, the lead network of C1 and R1 optimize system response by reducing overshoot. The very low bias current of the PA07 augments performance of the integrator circuit.

EXTERNAL CONNECTIONS



NOTE: Input offset voltage trim optional. $R_T = 10\text{K}\Omega$ MAX
 8-pin TO-3 package

PA07 • PA07A

ABSOLUTE MAXIMUM RATINGS SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal ¹	67W
INPUT VOLTAGE, differential	$\pm 50V$
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction ¹	200°C
TEMPERATURE RANGE, storage	-65 to +150°C
OPERATING TEMPERATURE RANGE, case	-55 to +125°C

SPECIFICATIONS

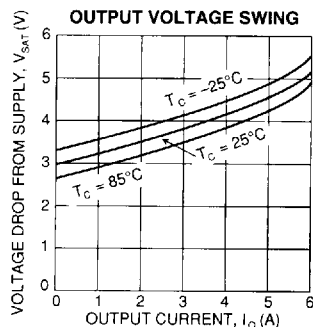
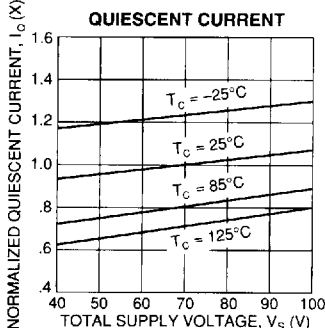
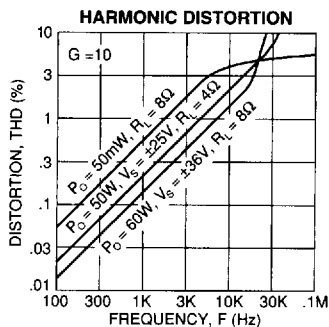
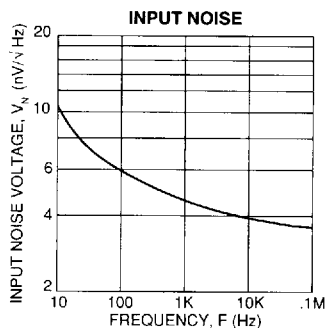
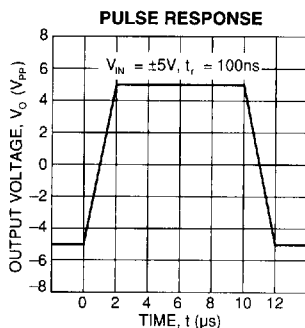
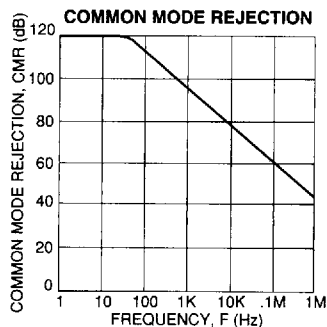
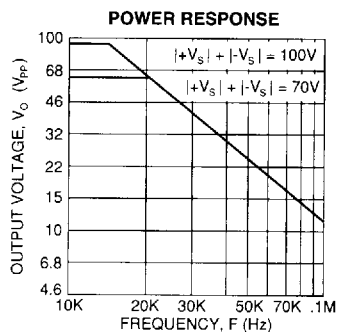
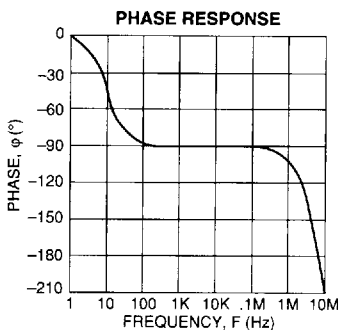
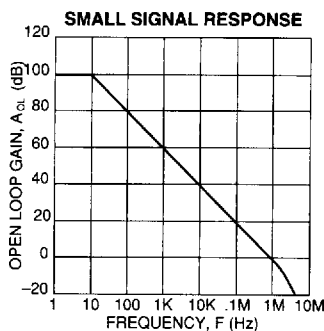
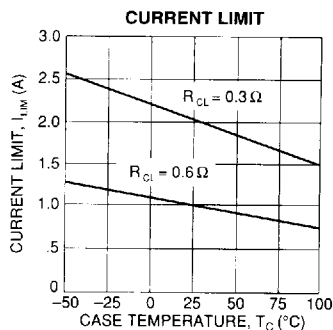
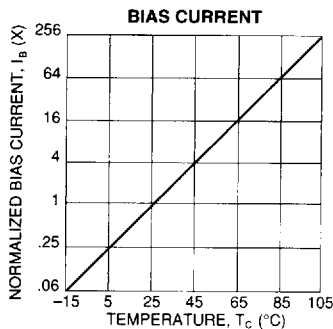
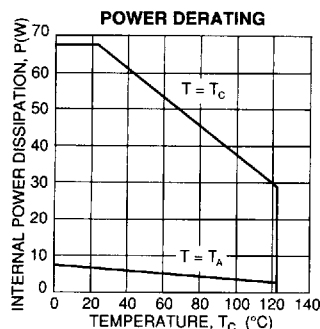
SPECIFICATIONS		PA07			PA07A			
PARAMETER	TEST CONDITIONS ²	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T _c = 25°C		.5	±2		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	μV/°C
OFFSET VOLTAGE, vs. supply	T _c = 25°C		8			*		μV/V
OFFSET VOLTAGE, vs. power	Full temperature range		20			10		μV/W
BIAS CURRENT, initial ³	T _c = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T _c = 25°C		.01			*		pA/V
OFFSET CURRENT, initial ³	T _c = 25°C		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	T _c = 25°C		10 ¹¹			*		Ω
INPUT CAPACITANCE	T _c = 25°C		4			*		pF
COMMON MODE VOLTAGE RANGE ⁴	Full temperature range	±V _s -10			*			V
COMMON MODE REJECTION, DC	Full temperature range, V _{CM} = ±20V		120			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T _c = 25°C, R _L = 15Ω	92	98		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T _c = 25°C, R _L = 15Ω		1.3			*		MHz
POWER BANDWIDTH	T _c = 25°C, R _L = 15Ω		18			*		kHz
PHASE MARGIN	Full temperature range, R _L = 15Ω		70			*		°
OUTPUT								
VOLTAGE SWING ⁴	Full temp. range, I _o = 5A	±V _s -5			*			V
VOLTAGE SWING ⁴	Full temp. range, I _o = 2A	±V _s -5			*			V
VOLTAGE SWING ⁴	Full temp. range, I _o = 90mA	±V _s -5			*			V
CURRENT, peak	T _c = 25°C	5			*			A
SETTLING TIME to .1%	T _c = 25°C, 2V step		1.5			*		μs
SLEW RATE	T _c = 25°C		5			*		V/μs
CAPACITIVE LOAD, unity gain	Full temperature range			10			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±12	±35	±50	*	*	*	V
CURRENT, quiescent	T _c = 25°C		18	30		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case ⁵	F>60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	F<60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*	*	°C/W
TEMPERATURE RANGE, case	Meets full range specifications	-25	25	+85	*	*	*	°C

NOTES: * The specification of PA07A is identical to the specification for PA07 in applicable column to the left.

- Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
- The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
- Doubles for every 10°C of temperature increase.
- $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
- Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



GENERAL

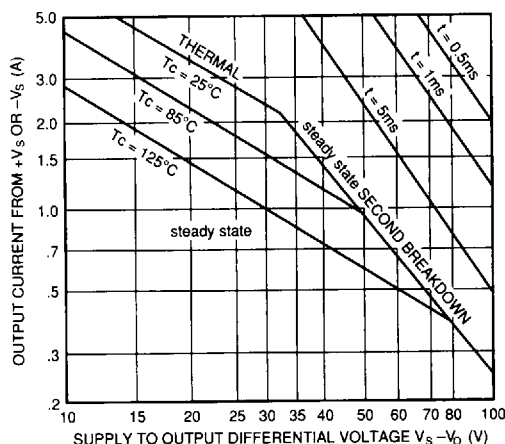
Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specified limits.
3. The junction temperature of the output transistors.

SAFE OPERATING AREA CURVES



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and inductive* loads up to the following maximum are safe:

$\pm V_S$	CAPACITIVE LOAD		INDUCTIVE LOAD	
	$I_{LIM} = 2A$	$I_{LIM} = 5A$	$I_{LIM} = 2A$	$I_{LIM} = 5A$
50V	80 μF	75 μF	55mH	7.5mH
40V	250 μF	150 μF	150mH	11mH
30V	1,200 μF	500 μF	250mH	24mH
20V	20mF	5mF	1.5H	75mH
15V	∞	25mF	∞	100mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 12V below the supply rail with $I_{LIM} = 5A$ or 32V below the supply rail with $I_{LIM} = 2A$ while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any reactive or EMF generating load and short circuits to the supply rail or common if the current limits are set as follows at $T_c = 85^\circ\text{C}$:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.25A	.82A
40V	.37A	1.4A
30V	.65A	2.1A
20V	1.4A	3.3A
15V	2.1A	4.5A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C . This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

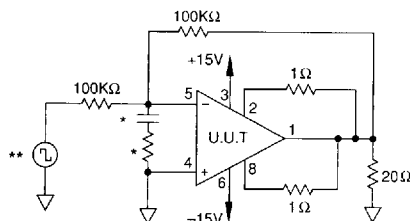
Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the $T_c = 25^\circ\text{C}$ boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, will destroy signal integrity and reduce the reliability of the device.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connections diagram. The minimum value for R_{CL} is $.12\Omega$, however, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_o	25°C	±35V	$V_{IN} = 0, A_v = 100$		30	mA
1	Input Offset Voltage	V_{OS}	25°C	±35V	$V_{IN} = 0, A_v = 100$		2	mV
1	Input Offset Voltage	V_{OS}	25°C	±12V	$V_{IN} = 0, A_v = 100$		4.3	mV
1	Input Offset Voltage	V_{OS}	25°C	±50V	$V_{IN} = 0, A_v = 100$		3.5	mV
1	Input Bias Current, +IN	$+I_b$	25°C	±35V	$V_{IN} = 0$		50	pA
1	Input Bias Current, -IN	$-I_b$	25°C	±35V	$V_{IN} = 0$		50	pA
1	Input Offset Current	I_{OS}	25°C	±35V	$V_{IN} = 0$		50	pA
3	Quiescent Current	I_o	-55°C	±35V	$V_{IN} = 0, A_v = 100$		46	mA
3	Input Offset Voltage	V_{OS}	-55°C	±35V	$V_{IN} = 0, A_v = 100$		4.4	mV
3	Input Offset Voltage	V_{OS}	-55°C	±12V	$V_{IN} = 0, A_v = 100$		6.7	mV
3	Input Offset Voltage	V_{OS}	-55°C	±50V	$V_{IN} = 0, A_v = 100$		5.9	mV
3	Input Bias Current, +IN	$+I_b$	-55°C	±35V	$V_{IN} = 0$		50	pA
3	Input Bias Current, -IN	$-I_b$	-55°C	±35V	$V_{IN} = 0$		50	pA
3	Input Offset Current	I_{OS}	-55°C	±35V	$V_{IN} = 0$		50	pA
2	Quiescent Current	I_o	125°C	±35V	$V_{IN} = 0, A_v = 100$		30	mA
2	Input Offset Voltage	V_{OS}	125°C	±35V	$V_{IN} = 0, A_v = 100$		5	mV
2	Input Offset Voltage	V_{OS}	125°C	±12V	$V_{IN} = 0, A_v = 100$		7.3	mV
2	Input Offset Voltage	V_{OS}	125°C	±50V	$V_{IN} = 0, A_v = 100$		6.5	mV
2	Input Bias Current, +IN	$+I_b$	125°C	±35V	$V_{IN} = 0$		10	nA
2	Input Bias Current, -IN	$-I_b$	125°C	±35V	$V_{IN} = 0$		10	nA
2	Input Offset Current	I_{OS}	125°C	±35V	$V_{IN} = 0$		10	nA
4	Output Voltage, $I_o = 5A$	V_o	25°C	±15.3V	$R_L = 2.07\Omega$	10.3		V
4	Output Voltage, $I_o = 90mA$	V_o	25°C	±50V	$R_L = 500\Omega$	45		V
4	Output Voltage, $I_o = 2A$	V_o	25°C	±29V	$R_L = 12\Omega$	24		V
4	Current Limits	I_{CL}	25°C	±19V	$R_L = 12\Omega, R_{CL} = 1\Omega$.54	.86	A
4	Stability/Noise	E_N	25°C	±35V	$R_L = 500\Omega, A_v = 1, C_L = 10nF$		1	mV
4	Slew Rate	SR	25°C	±35V	$R_L = 500\Omega$	2.5	10	V/ μ s
4	Open Loop Gain	A_{OL}	25°C	±35V	$R_L = 500\Omega, F = 10Hz$	92		dB
4	Common Mode Rejection	CMR	25°C	±34.5V	$R_L = 500\Omega, F = DC, V_{CM} = \pm 24.5V$	80		dB
6	Output Voltage, $I_o = 5A$	V_o	-55°C	±15.3V	$R_L = 2.07\Omega$	10.3		V
6	Output Voltage, $I_o = 90mA$	V_o	-55°C	±50V	$R_L = 500\Omega$	45		V
6	Output Voltage, $I_o = 2A$	V_o	-55°C	±29V	$R_L = 12\Omega$	24		V
6	Stability/Noise	EN	-55°C	±35V	$R_L = 500\Omega, A_v = 1, C_L = 10nF$		1	mV
6	Slew Rate	SR	-55°C	±35V	$R_L = 500\Omega$	2.5	10	V/ μ s
6	Open Loop Gain	A_{OL}	-55°C	±35V	$R_L = 500\Omega, F = 10Hz$	90		dB
6	Common Mode Rejection	CMR	-55°C	±34.5V	$R_L = 500\Omega, F = DC, V_{CM} = \pm 24.5V$	80		dB
5	Output Voltage, $I_o = 3A$	V_o	125°C	±11.3V	$R_L = 2.07\Omega$	6.3		V
5	Output Voltage, $I_o = 90mA$	V_o	125°C	±50V	$R_L = 500\Omega$	45		V
5	Output Voltage, $I_o = 2A$	V_o	125°C	±29V	$R_L = 12\Omega$	24		V
5	Stability/Noise	E_N	125°C	±35V	$R_L = 500\Omega, A_v = 1, C_L = 10nF$		1	mV
5	Slew Rate	SR	125°C	±35V	$R_L = 500\Omega$	1.25	10	V/ μ s
5	Open Loop Gain	A_{OL}	125°C	±35V	$R_L = 500\Omega, F = 10Hz$	92		dB
5	Common Mode Rejection	CMR	125°C	±34.5V	$R_L = 500\Omega, F = DC, V_{CM} = \pm 24.5V$	80		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.