MX•COM, INC.

MX803

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AUDIO SIGNALING PROCESSOR

DESCRIPTION

The MX803, a member of the DBS800 IC family, is an audio signaling processor that provides an inband tone signaling capability for LMR radio systems. Signaling systems supported include SelCall (CCIR, EEA, ZVEI I, II, and III) 2-Tone SelCall and DTMF encode.

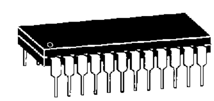
Using a non-predictive decoder and versatile encoder gives the MX803 the capability to work in any standard or non-standard tone system.

The MX803 is a full-duplex device for use with Single Tone or Selective Call systems. It consists of:

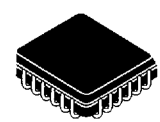
- A tone decoder with programmable NOTONE timer.
- Two individual tone encoders and a programmable TX period timer.
- An on-chip summing amplifier.

Under the control of the microcontroller (via C-BUS, the DBS800 serial interface) the MX803 will simultaneously encode and transmit 1 or 2 audio tones in the 208-3000Hz range. It also will detect, decode, and indicate the frequency of any non-predicted input tone in the frequency range of 313 to 6000Hz.

A general purpose logic input, interfacing directly with the Status Register, is provided. This could be used as an auxiliary method of routing digital information to the microcon-



MX803J
24-pin CDIP



MX803LH
24-pin PLCC

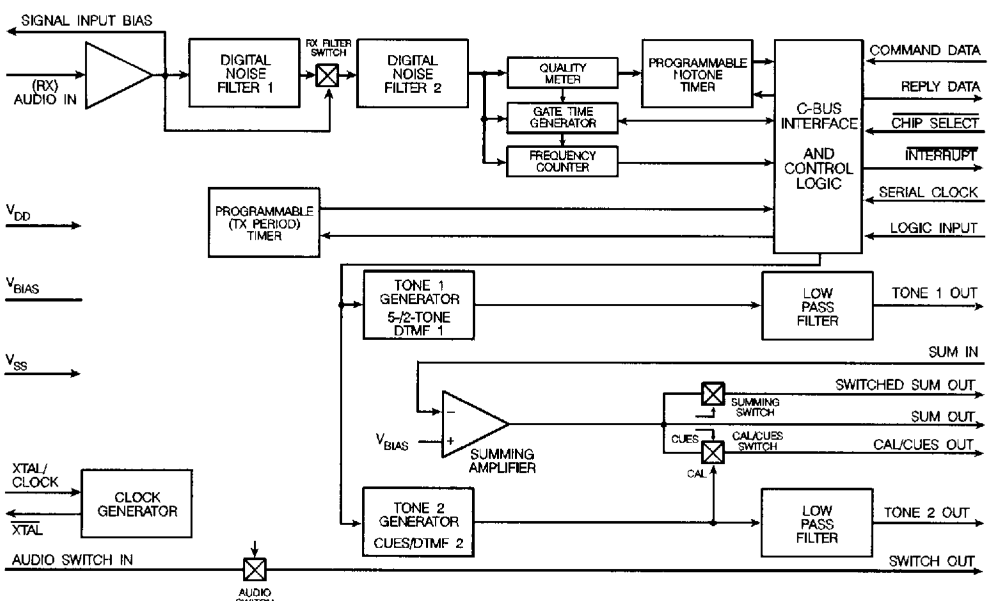


Figure 1 - MX803 Audio Signaling Processor

DESCRIPTION...

troller via the C-BUS. Output frequencies are produced from data loaded to the device. A programmable, general purpose, on-chip timer sets the tone transmit periods. A Dual-Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This process can also be used for level correction.

Tones produced by the MX803 can be used in the system as modulation calibration inputs and as "CUE" audio indications to the operator. Received tones are measured and their frequency indicated to the microcontroller in the form of a received data word. A poor quality or incoherent tone will indicate Notone.

The MX803 is a low-power 5-volt CMOS IC available in 24-pin CDIP and 24-lead plastic SMT packages.

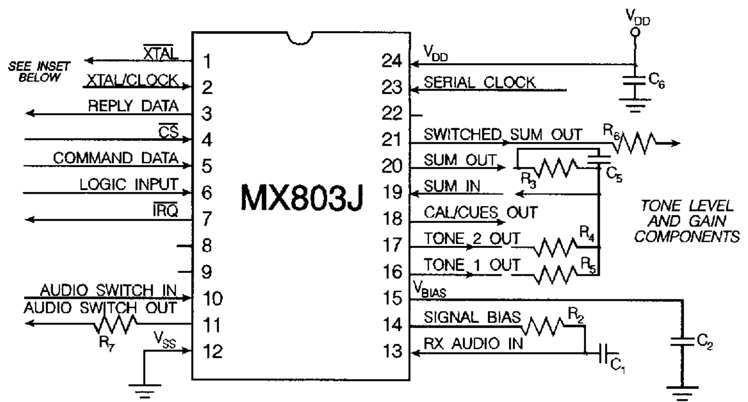
PIN FUNCTION CHART

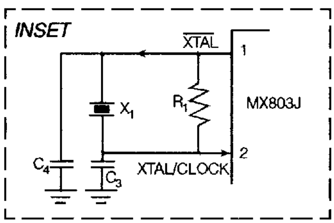
Pin	Function
1	**Xtal:** The output of the on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2.
3	**Reply Data:** This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the microcontroller. See Timing Diagrams.
4	**Chip Select ($\overline{CS}$):** The "C-BUS" data loading control function. This input is provided by the microcontroller. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Timing Diagrams.
5	**Command Data:** The "C-BUS" serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. See Timing diagrams.
6	**Logic Input:** This "real-time" input is available as a general purpose logic input port which can be read from the Status Register (see Table 3).
7	**Interrupt Request ($\overline{IRQ}$):** The output of this pin indicates an interrupt condition to the microcontroller by going to a logic "0." This is a "wire-or-able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The system $\overline{IRQ}$ line requires one pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register and are shown below: G/Purpose Timer Period Expired NOTONE Timer Period Expired RX Tone Measurement Complete These interrupts are inactive during relevant powersave conditions and can be disabled by bits 5 and 6 in the Control Register.
8	**N/C:** No internal connection.
9	**N/C:** No internal connection.
10	**Audio Switch In:** This is the input to the stand-alone on-chip Audio Switch. This function (Control Register bit 7) may be used to break the system transmitter modulation path when it is required to provide a CUE (beep) from Tone Generator 2 to the loudspeaker via the MX806A LMR Audio Processor.
11	**Audio Switch Out**: The output of the stand-alone on-chip Audio Switch.
12	V_{SS}**:** Negative supply (GND).

PIN FUNCTION CHART

Pin	Function
13	**RX Audio In:** The received audio tone signaling input. This input must be a.c. coupled and connected, using external components, to the Signal Input Bias pin (See Figure 2).
14	**Signal Input Bias:** External components are required between this input and the RX Audio In pin (See Figure 2).
15	V_{BIAS}: The internal circuitry bias line, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_2. See Figure 2.
16	**Tone 1 Out:** This is the Tone 1 Generator (2-/5-tone Selcall or DTMF 1) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 1 Register (Table 5). See Figure 2.
17	**Tone 2 Out:** This is the Tone 2 Generator (2-/5-tone Selcall, CUES or DTMF 2) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 2 Register (Table 5). See Figure 2.
18	**CAL/CUES Out:** An auxiliary, selectable tone frequency output, providing a square wave CALibration signal from the Tone 2 Generator or a sine wave CUES (beep) signal from the Summing Amplifier. The output mode (CAL or CUES) is selected by bit 14 in the TX Tone Generator 2 Register (Table 5). In a DBS 800 audio installation, this output should be connected to the Calibration Input of the MX806A LMR Audio Processor. When Tone Generator 2 is set to Notone, the CAL input is pulled to V_{BIAS}; during a powersave of Tone Generator 2 it is held at V_{SS}.
19	**Sum In:** The input to the on-chip Summing Amplifier. This amplifier is available for combining Tone 1 and Tone 2 outputs (DTMF). Gain and coupling components should be used at this input to provide the required system gains. See Figures 2 and 3.
20	**Sum Out:** The output of the on-chip summing amplifier. Combined tones (1 and 2) are available at this output. See Figures 2 and 3.
21	**Switched Sum Out:** This is the combined tone output available for transmitter modulation. The switch allows control of the MX803 final output to the MX806A. Control of this switch is by bit 4 of the Control Register. See Figures 2 and 3.
22	No internal connection.
23	**Serial Clock:** The "C-BUS" serial clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the Audio Signaling Processor. See Timing diagrams.
24	V_{DD}: Positive supply. A single +5 volt power supply is required. Levels and voltages within this Audio Signaling Processor are dependent upon this supply.
	NOTE: *1) Pins 8, 9, and 22 may be connected to V_{SS} to improve screening.* *2) A glossary of abbreviations used in this document can be found on page 12.* *C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a µController and DBS 800 ICs. It may be used with any µController, and can, if desired, take advantage of hardware serial I/O functions embodied into many types of µController. The C-BUS data rate is determined solely by the µController.*

Analog Application Information





Component	Value	Component	Value
R_1	1.0MΩ	C_1	0.1µF
R_2	2.0MΩ	C_2	1.0µF
*R_3	100kΩ	C_3	33.0pF
*R_4	82.0kΩ	C_4	33.0pF
*R_5	122kΩ	C_5	22.0pF
*R_6	100kΩ	C_6	1.0µF
*R_7	100kΩ	X_1	4.00MHz

Tolerances : R = ±10%, C = ±20%

Figure 2 - External Components

NOTES

1. Xtal/clock components described are recommended in accordance with MX-COM's Application Note on Standard and DBS 800 Crystal Oscillator Circuits (April 1990).

2. Resistors marked with an asterisk (*) are System Components whose values are calculated to allow the MX803 to operate with other DBS 800 microcircuits. Figure 3 shows these components used in the system signal paths.

3. R_3, R_4, R_5 and C_5 are tone mixing components calculated to provide a 3dB tone differential (twist) for use in a DTMF configuration. Single tone output levels are set independently or by the MX806 Modulator Drivers. R_7 provides modulation level and matching for inputs to the MX806.

4. To improve screening and reduce noise levels around the MX803, pins 8, 9 and 22 should be connected to V_{SS}.

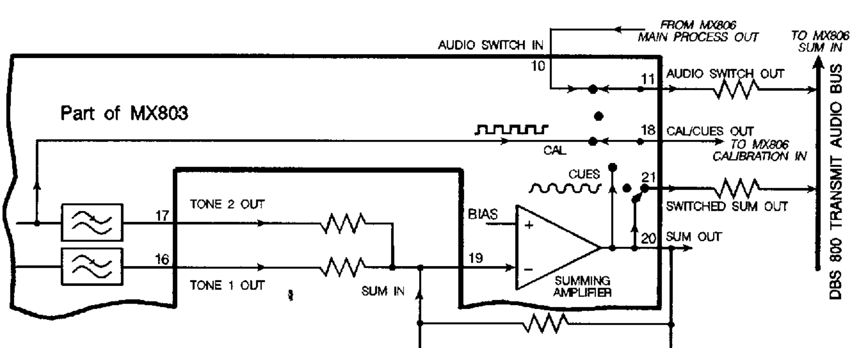


Figure 3 - Signal Switching

Controlling Protocol

Control of the MX803 Audio Signaling Processor's operation is by communication between the µController and the MX803 internal registers on the C-BUS using Address/Commands (A/Cs) and appended instructions or data (see Figure 7). The use and content of these instructions is detailed in the following pages.

MX803 Internal Registers

Control Register (30_H) -- Write only, control and configuration of the MX803.

Status Register (31_H) -- Read only, reporting of device functions.

RX Tone Frequency Register (32_H) -- Read only, indicates frequency of the last received input.

RX Notone Timer (33_H) -- Write only, setting of the RX Notone period.

TX Tone Generator 1 Register (34_H) -- Write only, setting the required output frequency from TX Tone Generator 1.

TX Tone Generator 2 Register (35_H) -- Write only, setting the required output frequency from TX Tone Generator 2.

General Purpose Timer Register (36_H) -- Write only, setting of a general purpose sequential time period.

Address/Commands

The first byte of a loaded data sequence is always recognized by the C-BUS as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an A/C byte followed by further instruction/data or a status/data reply.

Instructions and data are loaded and transferred via C-BUS in accordance with the timing information given in Figures 7 and 8.

Table 1 shows the list of A/C bytes relevant to the MX803.

Command Assignment	Address/Command (A/C) Byte Hex. MSB	Binary LSB	Data Byte(s)
General Reset	01	0 0 0 0 0 0 0 1	
Write to Control Register	30	0 0 1 1 0 0 0 0	+ 1 byte instruction to Control Register
Read Status Register	31	0 0 1 1 0 0 0 1	+ 1 byte reply from Status Register
Read RX Tone Frequency	32	0 0 1 1 0 0 1 0	+ 2 bytes reply from RX Tone Register
Write to Notone Timer	33	0 0 1 1 0 0 1 1	+ 1 byte instruction to Notone Register
Write to TX Tone Gen. 1	34	0 0 1 1 0 1 0 0	+ 2 bytes instruction to TX Tone Gen. 1
Write to TX Tone Gen. 2	35	0 0 1 1 0 1 0 1	+ 2 bytes instruction to TX Tone Gen. 2
Write to G/Purpose Timer	36	0 0 1 1 0 1 1 0	+ 1 byte instruction to G/Purpose Timer

Table 1 - C-BUS Address/Commands

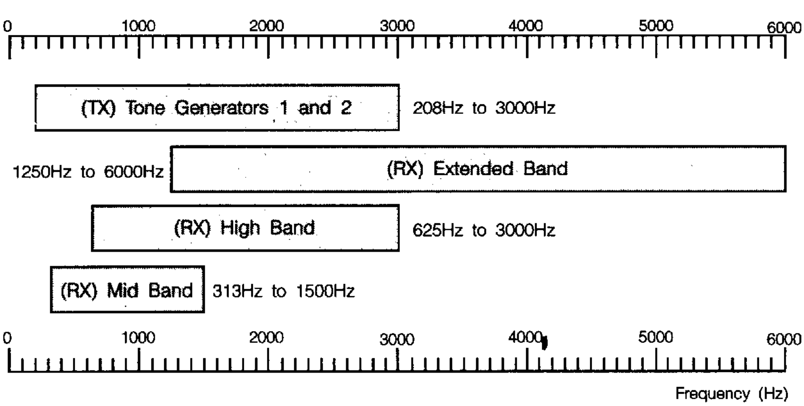


Figure 4 - MX803 Frequencies

Controlling Protocol...

"Write to Control Register" - A/C 30_H, followed by 1 byte of Command Data

Audio Switch
See the signal switching diagram (Figure 3) for application examples.

General Purpose Timer
This should be set up before interrupts are enabled since a General Reset command will set the timer period to 00_H - 0ms (permanent interrupt).

Interrupt Enable Instructions
Status bits 0, 1 and 2 are produced regardless of the state of these settings.

Band Selection
Bits 2 and 3 set the required frequency range. (See Figure 4, MX803 Frequencies.)

Summing Switch
Used to interrupt the MX803 drive to the MX806A Audio Processor (see Figure 3, Signal Switching).

Interrupt Designation
Decoder Interrupts:
Notone Timer and RX Tone Measurement
Transmitter Interrupt:
G/Purpose Timer Interrupt

Setting		Control Bits
MSB		***Transmitted First***
Bit 7		Audio Switch
1		Enable
0		Disable
6		***G/Purpose Timer Interrupt***
1		Enable
0		Disable
5		***Decoder Interrupts***
1		Enable
0		Disable
4		***Summing Switch***
1		Enable
0		Disable
3	***2***	***Band Selection***
0	0	High Band
0	1	Mid Band
1	0	Extended Band
1	1	Do not use this setting
1		Set to
0		"0"
0		Set to
0		"0"

Table 2 - Control Register

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"Read Status Register" - A/C 31_H, followed by 1 byte of Reply Data

Setting	Status Bits
MSB	***Received First***
Bit 7	Set to
0	"0"
6	Set to
0	"0"
5	Set to
0	"0"
4	Set to
0	"0"
3	***Logic Input Status***
1	"1"
0	"0"
2	***G/Purpose Timer Period***
1	Expired
	(Interrupt Generated)
1	***Notone Timer Period***
1	Expired
	(Interrupt Generated)
0	***RX Tone Measurement***
1	Complete
	(Interrupt Generated)

Table 3 - Status Register

Interrupt Requests ($\overline{IRQ}$)
Interrupts on this device are available to draw the attention of the microcontroller to a change in the condition of the bit in the status register. However, bits are set in the status register irrespective of the setting of interrupt enable bits (Table 2) and these changes may be recognized by polling the register.

General Purpose Timer Period
Set to a logic "1" when the timer period has expired.
Cleared to a logic "0" by:
a) Reading the Status Register, or
b) New G/Purpose Timer information, or
c) General Reset command

Notone Timer Period
Set to a logic "1" when the timer period has expired.
Cleared to a logic "0" by:
a) Reading the Status Register, or
b) New Notone Timer information, or
c) General Reset command

RX Tone Measurement
Set to a logic "1" when the RX Tone Measurement is complete. Cleared to a logic "0" by:
a) Reading the Status Register, or
b) General Reset command

Controlling Protocol...

TX Tone Generator Regsiters 1 and 2

Each TX Tone Generator is controlled individually by writing a two-byte command to the relevant TX Tone Generator Register. The format of this command word, which is different for each tone generator, is shown below with the calculations required for tone frequency (f_{TONE}) generation described in the following text.

"Write to TX Tone Generator 1 Register" - A/C 34_H, followed by 2 bytes of Command Data

MSB (loaded first) 15	14	13	Bit Numbers 12	11	10	9	8	7	6	5	4	3	2	1	LSB (loaded last) 0
0	0	Notone/ Enable	These 13 bits (0 to 12) are used to produce a binary number, designated "A." "A" is used in the formulas below to set the TX Tone 1 frequency (f_{TONE} 1).												

Table 4 - TX Tone Generator 1

SETTING TX TONE GENERATOR 1

The binary number produced by bits 0 to 12 (MSB) is designated "A." If "A" = all logic "0" TX Tone Generator 1 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at V_{BIAS} (NOTONE)
"0" = Tone 1 Output Enabled
Bits 14 and 15 (MSB) must be logic "0."

SETTING TX TONE GENERATOR 2

The binary number produced by bits o to 12 (MSB) is designated "B." If "B" = all logic "0" then TX Tone Generator 2 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at V (NOTONE)
"0" = Tone 1 Output Enabled.
Bit 14 at logic "1" = Squarewave CAL Output.
"0" = Sinewave CUES Output.
Bit 15 (MSB) must be a logic "0."

"Write to TX Tone Generator 2 Register" - A/C 35_H, followed by 2 bytes of Command Data

MSB (loaded first) 15	14	13	Bit Numbers 12	11	10	9	8	7	6	5	4	3	2	1	LSB (loaded last) 0
0	CAL/ CUES	Notone/ Enable	These 13 bits (0 to 12) are used to produce a binary number, designated "B." "B" is used in the formulas below to set the TX Tone 2 frequency (f_{TONE} 2).												

Table 5 - TX Tone Generator 2

Notes: (1) Programming Tone Generator 2 to Notone will place the CAL/CUES output at V_{BIAS} via a 40kΩ internal resistor.
(2) Programming Tone Generator 2 to Powersave will place the CAL/CUES output at V_{SS}.
(3) If both Tone Generators are Powersaved, the Input Amplifier is also Powersaved.

CALCULATIONS

As can be seen from Tables 4 and 5 (above), a binary number ("A" or "B" - bits 0 to 12) is loaded to the respective TX Tone Generator. The formulas described below are used to produce the required output frequency.

Required TX Tone output frequency = f_{TONE} 1 or 2
Xtal/clock frequency = f_{XTAL}
Input Data Word (bits 0 to 12) = "A" or "B"

Formula

$$f_{TONE} = \frac{f_{XTAL}}{4 \times \text{"A" or "B"}} \text{ (Hz)} \quad \text{or} \quad \text{input "A" or "B"} = \frac{f_{XTAL}}{4 \times f_{TONE}} \text{ (Hz)}$$

TX TONE FREQUENCIES

With reference to Tables 4 and 5 (above), while Input Data Words "A" or "B" can be programmed for frequencies outside the stated limits of 208Hz and 3000Hz, any output frequencies obtained may not be within specified parameters (see Specification page).

Controlling Protocol...

"Read RX Tone Frequency Register" - A/C 32_H, followed by 2 bytes of Reply Data

Measurement of RX Signal Frequency S_{INPUT}

The measurements on this and the following page are for a clock frequency of 4.032 MHz (see the bottom of the page for a scaling formula for other crystal values).

The input audio signal, S_{INPUT}, is measured in the Frequency Counter over a specified measurement period (9.125ms or 18.250ms).

The measuring function counts the number of complete input cycles occuring within the count period and then the number of measuring clock cycles necessary to make up the period.

When the count period of a successful decode is complete, the RX Tone Measurement bit in the Status Register and the Interrupt bit are set.

The RX Tone Frequency Register will now indicate the signal frequency S_{INPUT} in the form of 2 bytes (1 and 0) as illustrated in Figure 6 below.

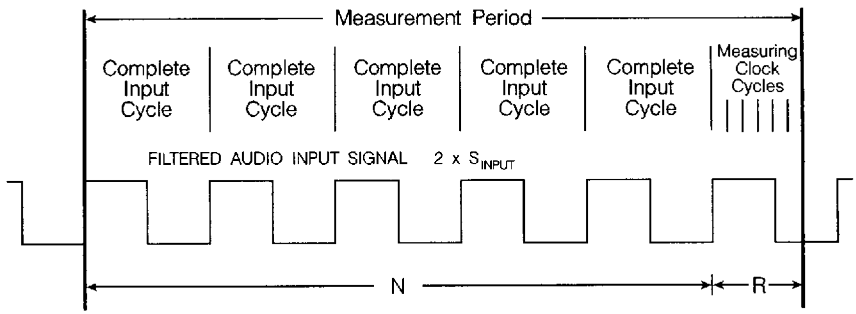

Figure 5 - Measurement of an RX Frequency

The Integer (N) - Byte 1

This is a binary number representing twice the number of complete input audio cycle periods. It is counted during the specified measurement period, which is:

High Band Decode	=	9.125 ms = "t"
Mid Band Decode	=	18.250 ms = "t"
Extended Band Decode	=	9.125 ms = "t"

See below for "t" and "f" scaling factors.

The Remainder (R) - Byte 0

This is a binary number representing the remainder part, R, of twice the Input Signal Frequency. R = "the number of specified measuring-clock cycles" required to complete the specified measurement period (See N). The clock cycle frequencies are:

High Band Decode	=	56.00 kHz = "f"
Mid Band Decode	=	28.00 kHz = "f"
Extended Band Decode	=	56.00 kHz = "f"

(Reply Data) (MSB) - Transmitted First — Byte 1 — Byte 0 — (Reply Data) (LSB) - Transmitted Last

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
"0"	"0"	← Integer (N) →						"0"	"0"	← Remainder (R) →					

CTCSS RX Frequency Register

Figure 6 - Format of the RX Tone Frequency Register

f_{XTAL} Scaling Factors

The calculations above are for a Xtal of 4.032 MHz. The following formulas allow calculation of these values using any Xtal value.

$$\text{"t" scaled} = t \times \left[\frac{4.032}{f_{XTAL}}\right]$$

$$\text{"f" scaled} = f \times \left[\frac{f_{XTAL}}{4.032}\right]$$

Controlling Protocol...

Frequency Measurement: The following formulas show the derivation of the RX frequency S_{INPUT} from the measured data bytes (N and R).

High Band Measurement

S_{INPUT} - High Band

In the measurement period of 9.125ms, there are N cycles at $2S_{INPUT}$ and R clock cycles at 56.000kHz.

So $$\frac{N}{2S_{INPUT}} + \frac{R}{56000} = 9.125ms$$

from which $$S_{INPUT} = \frac{28000 \times N}{(511-R)} \text{ Hz} \quad [1]$$

N and R - High Band

The measurement period = 9.125ms

Clock frequency = 56.000kHz

The measured frequency = $2S_{INPUT}$ Hz

In the measurement period there are:

$2S_{INPUT} \times 9.125 \times 10^{-3}$ cycles

Nh is the lower integer value of this decimal number:

$$N = INT(9.125 \times 10^{-3} \times 2S_{INPUT}) \quad [4]$$

Rh is the lower integer value of this decimal number:

$$R = INT(9.125 \times 10^{-3} - \frac{N)}{2S_{INPUT}} \times 56000 \quad [5]$$

Mid Band Measurement

S_{INPUT} - Mid Band

In the measurement period of 18.250ms, there are N cycles at $2S_{INPUT}$ and R clock cycles at 28.000kHz.

So $$\frac{N}{2S_{INPUT}} + \frac{R}{28000} = 18.250ms$$

from which $$S_{INPUT} = \frac{14000 \times N}{(511-R)} \text{ Hz} \quad [2]$$

N and R - Mid Band

The measurement period = 18.250ms

Clock frequency = 28.000kHz

The measured frequency = $2S_{INPUT}$Hz

In the measurement period there are:

$2S_{INPUT} \times 18.250 \times 10^{-3}$ cycles

Nm is the lower integer value of this decimal number:

$$N = INT(18.250 \times 10^{-3} \times 2S_{INPUT}) \quad [6]$$

Rm is the lower integer value of this decimal number:

$$R = INT(18.250 \times 10^{-3} - \frac{N)}{2S_{INPUT}} \times 28000 \quad [7]$$

Extended Band Measurement

S_{INPUT} - Extended Band

In the measurement period of 9.125ms, there are N cycles at S_{INPUT} and R clock cycles at 56.000kHz.

So $$\frac{N}{S_{INPUT}} + \frac{R}{56000} = 9.125ms$$

from which $$S_{INPUT} = \frac{56000 \times N}{(511-R)} \text{ Hz} \quad [3]$$

N and R - Extended Band

The measurement period = 9.125ms

Clock frequency = 56.000kHz

The measured frequency = S_{INPUT} Hz

In the measurement period there are:

$S_{INPUT} \times 9.125 \times 10^{-3}$ cycles

N is the lower integer value of this decimal number:

$$N = INT(9.125 \times 10^{-3} \times S_{INPUT}) \quad [8]$$

R is the lower integer value of this decimal number:

$$R = INT(9.125 \times 10^{-3} - \frac{N)}{S_{INPUT}} \times 56000 \quad [9]$$

Controlling Protocol...

"Write to RX Notone Timer Register" - A/C 33_H, followed by 1 byte of Command Data

Setting				Function/Period	
MSB					
7	*6*	*5*	*4*	***Transmitted Bit 7 First***	
0	0	0	0	These 4 bits must be "0"	
3	*2*	*1*	*0*	High Band	Mid Band
0	0	0	0	period (ms) 0	0
0	0	0	1	20 ±1%	40 ±1%
0	0	1	0	40 "	80 "
0	0	1	1	60 "	120 "
0	1	0	0	80 "	160 "
0	1	0	1	100 "	200 "
0	1	1	0	120 "	240 "
0	1	1	1	140 "	280 "
1	0	0	0	160 "	320 "
1	0	0	1	180 "	360 "
1	0	1	0	200 "	400 "
1	0	1	1	220 "	440 "
1	1	0	0	240 "	480 "
1	1	0	1	260 "	520 "
1	1	1	0	280 "	560 "
1	1	1	1	300 "	600 "

Table 6 - RX Notone Timer Settings

Operation of the RX Notone Timer

A NOTONE period is that period when no signal or a consistently bad quality signal is received. The NOTONE Timer is employed to indicate to the microcontroller that a NOTONE situation has existed for a predetermined period.

The NOTONE Timer period is "primed" by writing to the NOTONE Timer Register (33) using the instructions and information (1 data byte) given in Table 6. This timer register can be written-to and set in any mode of the MX803 except "Notone Timer Powersave." Priming the timer sets the timing period; this period will not be allowed to start until at least one frequency (tone) measurement has been sucessfully completed.

The NOTONE Timer is a one-shot timer that is reset only by successful tone measurements.

If the quality of the received signal drops to an unusable level the NOTONE Timer will start its run-down. On completion of this timer period, the NOTONE Timer Period Expired bit in the Status Register and an Interrupt are set.

Upon detection of the Interrupt, the Status Register should be read by the Controller to ascertain the source of the Interrupt.

The NOTONE Timer Period Expired bit is cleared:

i By a read of the Status Register
ii New NOTONE Timer Information
iii General Reset Command

The timer is set to 00_H by a General Reset command.

The following situations may be encountered by the NOTONE Timer circuitry:

NO SIGNAL

The NOTONE Timer can only start its run down on completion of a valid frequency measurement.

NO SIGNAL AFTER A VALID TONE MEASUREMENT

The timer will start to run down when the last RX Tone Measurement complete bit is set. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

SIGNAL FADES AFTER A VALID TONE MEASUREMENT

The timer will start to run down when the signal becomes unreadable to the device. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

SIGNAL APPEARS AFTER THE TIMER HAS STARTED

If the frequency measurement is more than 75% complete when the timer period expires, neither the NOTONE bit nor the Interrupt will be set unless that frequency measurement is subsequently aborted.

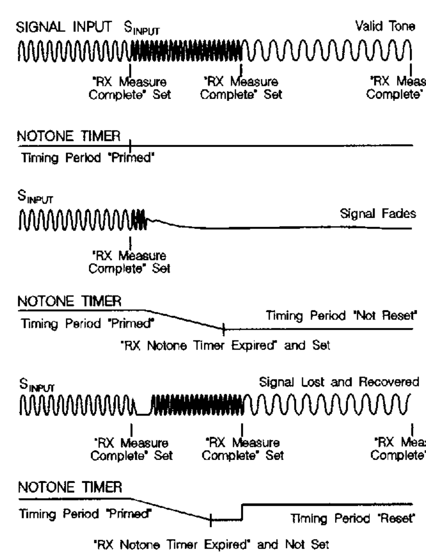

Figure 7 - Notone Timing

Controlling Protocol...

"Write to General Purpose Timer Register" - A/C 36_H, followed by 1 byte of Command Data

Setting				Function/Period	
MSB					
7	*6*	*5*	*4*	***Transmitted Bit 7 First***	
0	0	0	0	These 4 bits must be "0"	
3	*2*	*1*	*0*	High Band	Mid Band
				Reset Timer and Start Timing	
0	0	0	0	period of 0	0
0	0	0	1	10ms ±1%	20ms ±1%
0	0	1	0	20 "	40 "
0	0	1	1	30 "	60 "
0	1	0	0	40 "	80 "
0	1	0	1	50 "	100 "
0	1	1	0	60 "	120 "
0	1	1	1	70 "	140 "
1	0	0	0	80 "	160 "
1	0	0	1	90 "	180 "
1	0	1	0	100 "	200 "
1	0	1	1	110 "	220 "
1	1	0	0	120 "	240 "
1	1	0	1	130 "	260 "
1	1	1	0	140 "	280 "
1	1	1	1	150 "	300 "

Table 7 - General Purpose Timer Settings

Operation of the General Purpose Timer

This timer, which is not dedicated to any specific function within the MX803, can be used within the DBS 800 system to indicate time-elapsed periods of between 10-150ms in the High Band or 20-300ms in the Mid Band to the microcontroller. Setting of the timer is by loading a single byte data word via the C-BUS (see Table 7 at left) to the MX803 through the Command Data line.

The timer will be reset and the run-down started on completion of Timer Data Word loading.

When the programmed time period has expired, the General Purpose Timer Expired bit (bit 2) in the Status Register and the Interrupt are set.

The General Purpose Timer Expired bit is cleared:
- (i) By a read of the Status Register, or
- (ii) New G/P Timer information, or
- (iii) General Reset Command.

When the programmed time period has expired, this timer will reset, restart itself and continue sequencing until:
- (i) New G/P Timer information is written, or
- (ii) A General Reset Command is received.

The General Purpose Timer Expired bit and the interrupt will remain set until cleared.

The timer is set to 00_H (0ms) by a General Reset command.

Powersave

Various sections of the MX803 can be placed independently into a power-economical condition. Table 8 (below) gives a summary of these states available to the MX803.

Powersaved Section	Instruction Source		Table
Tone Encoder 1	TX Tone Gen. 1 Reg. (34_H)	All bits = "0"	4
Tone Encoder 2	TX Tone Gen. 2 Reg. (35_H)	All bits = "0"	5
Input Amplifier	This action is automatic when both Tone Encoders are in the Powersave condition.		

Table 8 - MX803 Powersave Functions

Powersave Conditions

Xtal/Clock and C-BUS: This circuitry is always active, on all DBS 800 ICs, under any depowered/powersaved conditions

Controlling Protocol...

Interrupt Requests

An Interrupt ($\overline{IRQ}$), when enabled, is provided by the MX803 to indicate the following conditions to the µController.

Notone Timer Period Expired

Enabled: By Control Register bit 5.
Set: When the preset Notone Flag is set.
Identified: By Status Register bit 1.
Cleared: By reading the Status Register.

G/Purpose Timer Period Expired

Enabled: By Control Register bit 6.
Set: When the General Purpose Timer has timed out.
Identified: By Status Register bit 2.
Cleared: By reading the Status Register.

RX Tone Measurement Complete

Enabled: By Control Register bit 5.
Set: When an RX Frequency Measurement has been successfully completed.
Identified: By Status Register bit 0.
Cleared: By reading the Status Register.

On recognition of the "Read Status" Command byte, the interrupt output is cleared, the Status bits are transferred to the µController via the C-BUS Reply Data line and the internal Status bits are cleared.

Operational Recommendations

Following initial system power-up, a General Reset command should be sent.

Receive Sequence

1. Send Control Command for RX: Select Midband/Highband and Digital Filter length.
2. Disable transmitters if desired by writing to Tone Frequency registers.
3. Prime the Notone timer by sending the required period byte.
4. Enable/disable interrupts as desired.
5. When a valid tone has been detected by a successfully completed measurement the Status Register is set to "Tone Measurement Complete" and an interrupt is set to the µC.
6. The µC examines the Status Register. If tone measurement is complete, it reads in the RX Tone Frequency in the form N + R (Fig. 6).
7. RX Tone Measurement Complete interrupts are periodically sent to the µC unless Notone is detected, in which case a Notone Interrupt is sent.

Transmit Sequence

1. Set Tone Frequency Generators to Notone during the transmitter initialization period.
2. Send Control Command for TX: Select Sum/Switched Sum o/p and Audio Switch states.
3. Send General Purpose (GP) Timer information for the Notone transmitter initialization period. This will initiate the timer.
4. Enable/disable interrupts as desired.
5. µC waits for "GP Timer Expired," reads the Status Register to check interrupts due to timer, and resets the Status Bit. If required, the µC sends the next timer period followed by the next tone(s) frequency information. A new timer period sent will reset the timer, otherwise the timer is self-resetting.
6. The µC monitors the interrupts and repeats 5 & 6 as required.
7. After last loaded tone, µC turns off Tone Generator(s).

General Reset

Upon power-up the bits in the MX803 registers will be random (either "0" or "1"). A General Reset Command 01_H) will be required to reset all microcircuits on the C-BUS. It has the following effect on the MX803:

Control Register	Set as 00_H
Status Register (bits 0, 1, 2)	Set as 00_H
Notone Timer	Set as 00_H
Tone Gen. 1 Reg. (2 bytes)	Set as 0000_H
Tone Gen. 2 Reg. (2 bytes)	Set as 0000_H
Gen. Purpose Reg.	Set as 00_H

This sets the MX803 to Encoder High Band (625Hz to 3000Hz) with interrupts disabled and both timers set to 00_H.

Both timers should be set up before interrupts are enabled to prevent initial, undesired interrupts.

Glossary of Abbreviations

Below is a list of abbreviations used in this Data Bulletin.

f_{XTAL} Xtal/Clock frequency.

S_{INPUT} Audio input signal.

f_{TONE} Tone frequency.

Timing Information

Figure 8 shows the timing parameters for two-way communication between the µController and the MX803 on the C-BUS.

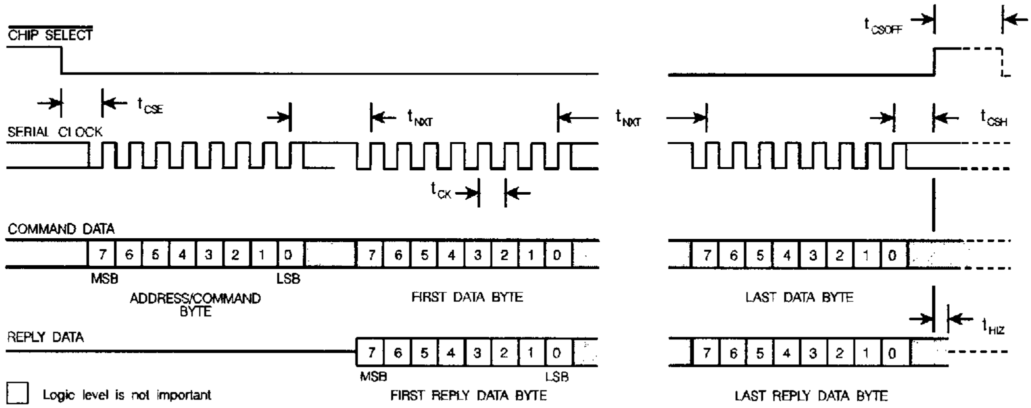

Figure 8 - C-BUS Timing

	Parameter	Min.	Typ.	Max.	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	-	-	µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0	-	-	µs
t_{CSOFF}	Chip Select High	2.0	-	-	µs
t_{NXT}	Command Data Inter-Byte Time	4.0	-	-	µs
t_{CK}	Serial Clock Period	2.0	-	-	µs
t_{CH}	Decoder or Encoder Clock High	500	-	-	ns
t_{CL}	Decoder or Encoder Clock Low	500	-	-	ns
t_{CDS}	Command Data Set-Up Time	250	-	-	ns
t_{CDH}	Command Data Hold Time	0	-	-	ns
t_{RDS}	Reply Data Set-Up Time	250	-	-	ns
t_{RDH}	Reply Data Hold Time	50.0	-	-	ns
t_{HIZ}	Chip Select High to Reply Data High - Z	-		2.0	µs

Notes:
1. Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the MX803 MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the MX803 and into the microcontroller on the rising Serial Clock edge.
3. Loaded data instructions are acted upon at the end of each individual, loaded byte.
4. To allow for differing microcontroller serial interface formats, the MX803 will work with either polarity Serial Clock pulses.

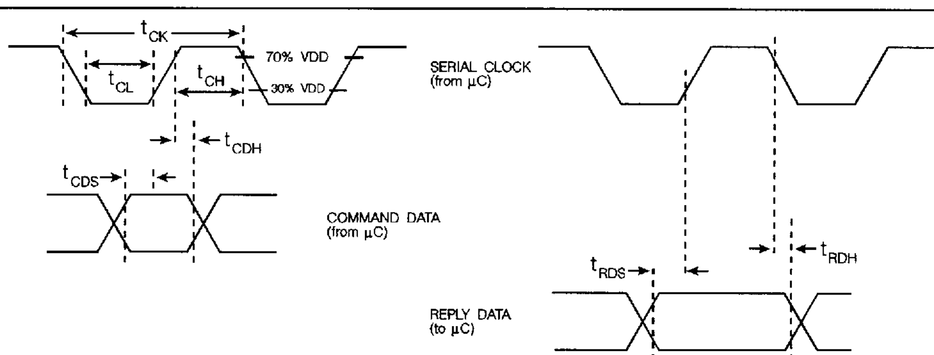

Figure 9 - Timing Relationships for C-BUS Information Transfer

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin	
(Ref V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Sink/source Current	
(Supply pins)	±30mA
(Other pins)	±20mA
Total Device Dissipation	
@T_{AMB} 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/clock f_{XTAL} = 4.0MHz

Audio level 0dB ref. = 308mVrms @ 1kHz *(60% deviation, FM)*

Noise Bandwidth = 5.0kHz Band-Limited Gaussian

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Decoder + Both Timers		-	2.0	-	mA
Decoder, Both Timers + One TX only		-	4.0	-	mA
All Functions Enabled		-	5.0	-	mA
Analog Impedances					
RX Audio Input		-	20.0	-	MΩ
Summing Amp Input		-	20.0	-	MΩ
Switch		-	1.0	-	kΩ
Tones 1 and 2 Outputs		-	10.0	-	kΩ
CAL/CUES Output		-	5.0	-	kΩ
Summing Outputs		-	10.0	-	kΩ
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5	-	-	V
Input Logic "0"	1	-	-	1.5	V
Output Logic "1" (IOH = -120µA)	2	4.6	-	-	V
Output Logic "0" (IOL = 360µA)	3	-	-	0.4	V
I_{OUT} Tristate (Logic "1" or "0")	3	-	-	4.0	µA
Input Capacitance	1	-	-	7.5	pF
IOX (V_{OUT} = 5V)	4	-	-	4.0	µA
Overall Performances					
RX - Decoding					
High Band					
Sensitivity		-	-20.0	-	dB
Tone Response Time					
Good Signal	5	-	-	20.0	ms
Tone-to-Noise Ratio = 0dB	5,6	-	-	40.0	ms
Frequency					
Band		625	-	3000	Hz
Measurement Resolution		-	0.2	-	%
Measurement Accuracy		-	0.5	-	%

Characteristics	See Note	Min.	Typ.	Max.	Unit
Mid-Band					
Sensitivity		-	-20.0	-	dB
Tone Response Time					
Good Signal	7	-	-	60.0	ms
Tone-to-Noise Ratio = 0dB	6,7	-	-	80.0	ms
Frequency					
Band		313	-	1500	Hz
Measurement Resolution		-	0.2	-	%
Measurement Accuracy		-	0.5	-	%
Extended Band					
Sensitivity		-	-20.0	-	dB
Tone Response Time					
Good Signal	5	-	-	20.0	ms
Frequency					
Band		1250	-	6000	Hz
Measurement Resolution		-	0.2	-	%
Measurement Accuracy		-	0.5	-	%
TX - Encoders 1 and 2					
Tone Frequency		208	-	3000	Hz
Period ($1/f_{TONE}$) Error		-	-	1.0	µS
Tone Amplitude		-1.0	-	1.0	dB
Total Harmonic Distortion		-	-	5.0	%
Rise Time to 90%	8	-	-	3.0	ms
Fall Time to 10%	8	-	-	5.0	ms
Frequency Change Time	8	-	2.0	-	ms
Timers					
General Purpose					
Timing Period Range					
High-Band		10.0	-	150	ms
Mid-Band		20.0	-	300	ms
RX Notone					
Timing Period Range					
Hi-Band		20.0	-	300	ms
Mid-Band		40.0	-	600	ms
Xtal/Clock Frequency (f_{XTAL})		3.9	-	4.1	MHz

Notes:
1. Device control pins: Serial Clock, Command Data, and $\overline{CS}$.
2. Reply Data output.
3. Reply Data and $\overline{IRQ}$ outputs.
4. Leakage current into the "Off" $\overline{IRQ}$ output.
5. Measurement period = 9.198ms.
6. Decode Probability = 0.993.
7. Measurement period = 18.396ms.
8. For f_{TONE}>625Hz, the time periods will double for Encoder frequencies below 625Hz.

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