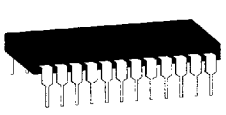
OCTAL DIGITALLY CONTROLLED AMPLIFIER ARRAY

Features

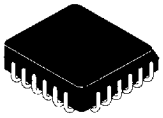
8 Digitally Controlled Amplifiers
15 Gain/Attenuation Steps + Mute
7 Trimmers with a ±3dB Range in 0.43dB Steps
1 "Volume" Control with a ±14dB Range in 2.0 dB Steps
Individual Control with an 8-Bit Serial Word
Output Mute/Powersave Function
Digitally Set Audio Control Levels

Applications

Cellular and LMR Radios, PABX's, Electronic Mail
Automatic Test Equipment, Remote Gain Adjustments



MX009J (CDIP)
MX009P (PDIP)
24 pins



MX009LH
(24 pin PLCC)

Description

The MX009 Digitally Controlled Amplifier Array replaces trimmers and one volume control in radio and wireline communications applications in which voice or data signals need adjusting. The MX009 is a single-chip LSI circuit comprised of eight discrete, digitally controlled amplifiers, each with 15 distinct gain/attenuation steps plus a MUTE. Control of each amplifier is by an 8-bit serial word.

Seven of the amplifiers have a ±3dB range stepped in 15 increments of 0.43dB each. The remaining amplifier has a ±14dB range in 15 steps of 2dB, and is intended for volume control applications. Each digitally controlled amplifier includes a sixteenth "Mute" state which sets the output to bias ($V_{DD}/2$) and powersaves the section addressed. Minimum current drain results from muting all eight sections.

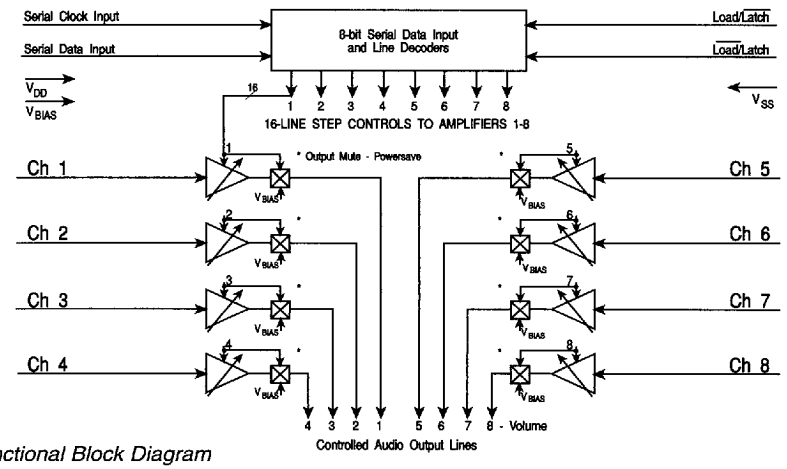
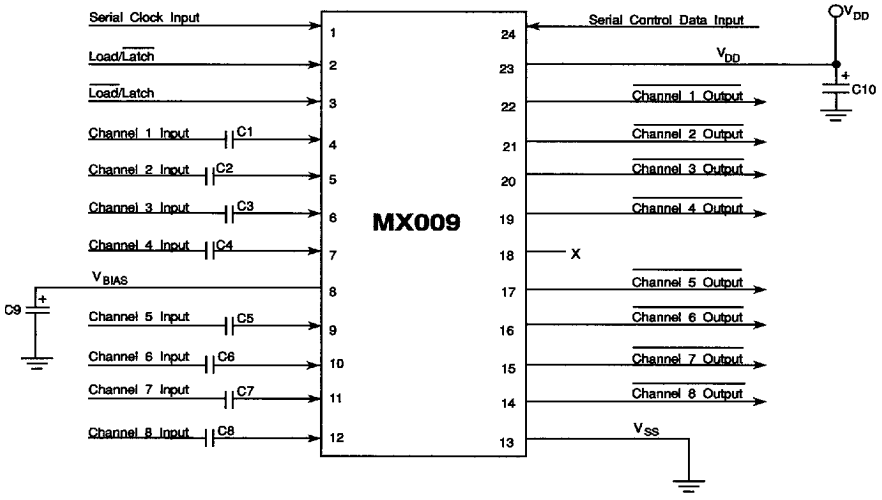


Figure 1 - Functional Block Diagram

Pin Function Table

Pin	Function
1	Serial Clock: This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Data Load timing. This input has an internal 1MΩ pullup resistor.
2	Load/$\overline{\text{Latch}}$: This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical "0" to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded this input should be $\overline{\text{strobed}}$ "0 -> 1 -> 0" to latch the new data in. Data is executed on the falling edge of the strobe. If the $\overline{\text{Load}}$/Latch input is used this pin should be left open circuit — This input has an internal 1MΩ pullup resistor.
3	$\overline{\text{Load}}$/Latch: This is the inverted Load/Latch input. This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical "1" to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded this input should be strobed "1 -> 0 -> 1" to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/$\overline{\text{Latch}}$ input is used this pin should be left open circuit — This input has an internal 1MΩ pulldown resistor.
4	Ch 1 Input: Analog Inputs: These individual amplifier inputs are self-biasing; input
5	Ch 2 Input: analog signals must be a.c. coupled to these pins, as shown in Figure 2. In the powersave modes the inputs are biased at
6	Ch 3 Input: $V_{DD}/2$. Ch1 to Ch7 range from -3dB to +3dB in 0.43dB steps. Ch8 could be utilized as a volume control ranging from -15dB
7	Ch 4 Input: to +15dB in 2.0 dB steps.
8	V_{BIAS}: The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{ss} as shown in Figure 2.
9	Ch 5 Input: Analog Inputs
10	Ch 6 Input:
11	Ch 7 Input:
12	Ch 8 Input:
13	V_{ss}: Negative supply rail (GND).
14	$\overline{\text{Ch 8}}$ Output: Analog Outputs: These are the individual "Gain Controlled" amplifier outputs.
15	$\overline{\text{Ch 7}}$ Output: Ch1 to Ch7 range from -3dB to +3dB in 0.43dB steps. Ch8 could be
16	$\overline{\text{Ch 6}}$ Output: used as a volume control, ranging from -14dB to +14dB in 2.0dB steps.
17	$\overline{\text{Ch 5}}$ Output: In the powersave modes the selected output is biased at $V_{DD}/2$.
18	No internal connection. Do not use.
19	$\overline{\text{Ch 4}}$ Output: Analog Outputs
20	$\overline{\text{Ch 3}}$ Output:
21	$\overline{\text{Ch 2}}$ Output: Note that amplifiers Ch1 to Ch8
22	$\overline{\text{Ch 1}}$ Output: are "inverting amplifiers."
23	V_{DD}: Positive supply. A single +5-volt power supply is required.
24	Control (Data) Input: Operation of the 8 amplifier channels (Ch1 - Ch8) is controlled by the 8 bits of data entered serially at this pin. The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1MΩ pullup resistor.

Application Notes



Notes

(1) Channel Amplifiers 1 to 8 are inverting amplifiers.

(2) Analog input capacitors C_1 to C_8 are only required for a.c. input signals; d.c. input signals do not require these components.

Component	Unit Value
C_1 to C_8	0.1µF
C_9	1.0µF
C_{10}	1.0µF

Tolerances ± 20%

Fig. 2 - External Component Connections

Application Recommendations

To avoid noise and instability the following practices are recommended:

(a) Use a clean, well-regulated power supply.

(b) Keep leads short.

(c) Inputs and outputs should be shielded wherever possible.

(d) Analog tracks should not run parallel to digital tracks.

(e) A "Ground Plane" connected to V_{ss} will assist in eliminating external pick-up on the channel input and output pins.

(f) Avoid running High Level Outputs adjacent to Low Level Inputs.

(g) Input signal amplitudes should be applied with regard to Figure 3.

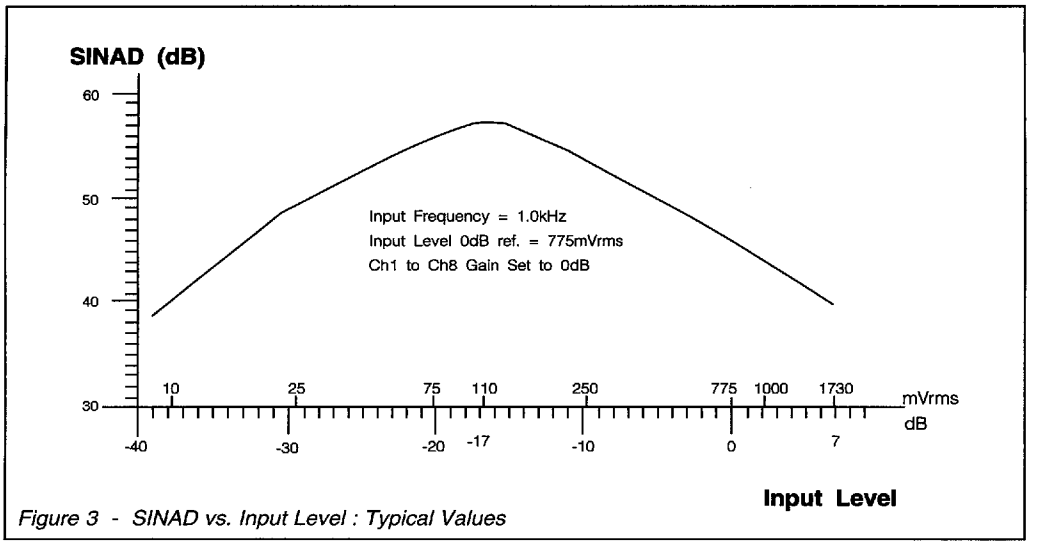


Figure 3 - SINAD vs. Input Level : Typical Values

Control Data and Timing

The gain of each amplifier block (Channels 1 to 8) in the MX009 is set individually by an 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0) is serially loaded to the Control Data Input using the external data clock. Data is loaded to the MX009 on the rising edge of the Serial Clock. Loaded data is executed on the falling edge of the Load/$\overline{\text{Latch}}$ pulse and on the rising edge of the Load/$\overline{\text{Latch}}$ pulse. Table 1 shows the format of each 4-bit Address word. Table 2 shows the format of each Gain Control word and Figure 4 shows the data loading operation and timing.

Table 1 Address Word Format

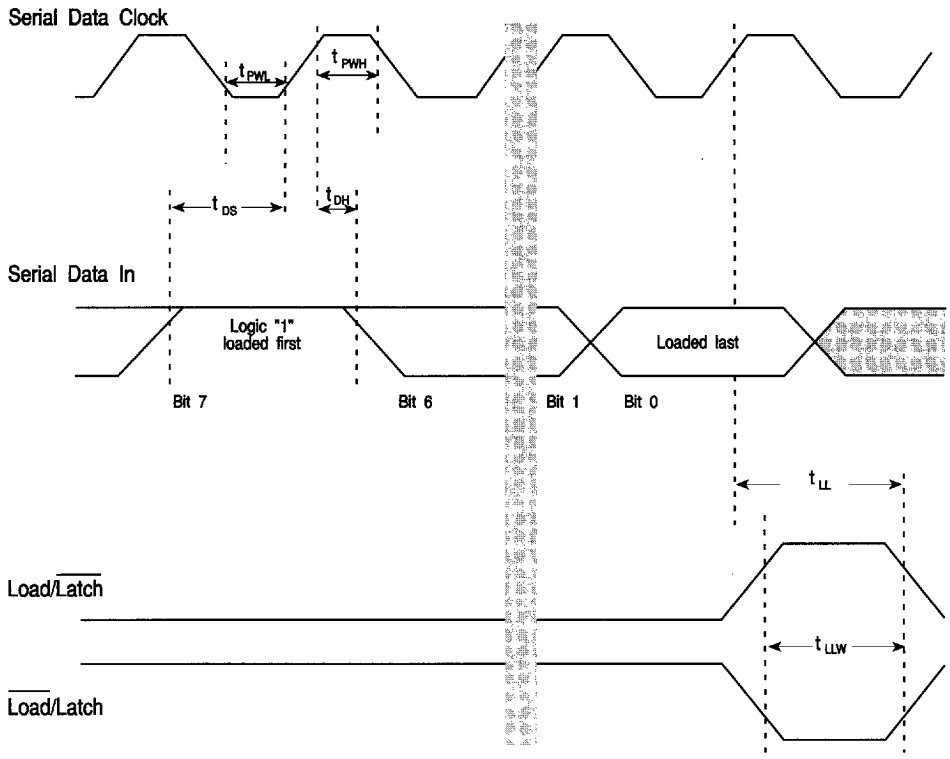
Bit 7 MSB	Bit 6	Bit 5	Bit 4 LSB	Channel Selected
1	0	0	0	1
1	0	0	1	2
1	0	1	0	3
1	0	1	1	4
1	1	0	0	5
1	1	0	1	6
1	1	1	0	7
1	1	1	1	8

Table 2 Gain Control Word Format

Bit 3 MSB	Bit 2	Bit 1	Bit 0 LSB	Stage 1 to 7 2dB	Stage 8 0.43dB
0	0	0	0	Powersave	Powersave
0	0	0	1	-3.0	-14.0dB
0	0	1	0	-2.571	-12.0dB
0	0	1	1	-2.143	-10.0dB
0	1	0	0	-1.714	-8.0dB
0	1	0	1	-1.286	-6.0dB
0	1	1	0	-0.857	-4.0dB
0	1	1	1	-0.428	-2.0dB
1	0	0	0	0	0.0dB
1	0	0	1	0.428	2.0dB
1	0	1	0	0.857	4.0dB
1	0	1	1	1.286	6.0dB
1	1	0	0	1.714	8.0dB
1	1	0	1	2.143	10.0dB
1	1	1	0	2.571	12.0dB
1	1	1	1	3.0	14.0dB

Data Loading

The 8-bit data word is loaded bit 7 first and bit 0 last. Bit 7 must be a logic "1" to address the chip. If bit 7 in the word is a logic "0" that 8-bit word will not be executed. Figure 4 (below) shows the timing information required to load and operate this device.



Timing

t_{PWH}	t_{DS}	t_{LL}
Serial Clock "High" Pulse Width	Data Set-up Time	Load/Latch Set-up Time
t_{PWL}	t_{DH}	t_{LLW}
Serial Clock "Low" Pulse Width	Data Hold Time	Load/Latch Pulse Width

Figure 4 - Serial Control Data Loading Diagram

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation (@T_{AMB} 25°C)	800mW Max.
Derating	10mW/°C
Operating temperature:	-40°C to + 85°C
Storage temperature:	-55°C to +125°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V

T_{AMB} = 25°C

Audio level 0dB ref = 775 mVrms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current -Powersave		—	0.16	1.0	mA
-All Stages Operating		—	4.0	8.0	mA
Dynamic Values					
Input Logic "1"		3.5	—	—	V
Input Logic "0"		—	—	1.5	V
Digital Input Impedances		0.5	1.0	—	MΩ
Amplifier Stages (General)					
Bandwidth (-3dB)		15.0	—	- -	kHz
Output Impedance		—	0.8	3.0	kΩ
Total Harmonic Distortion	1	—	0.35	0.5	%
Output Noise Level (per stage)	2	- -	65.0	- -	µVrms
Onset of Clipping	3	—	1.73	—	Vrms
Gain Variation	4	- -	- -	0.1	dB
Interstage Isolation		—	60.0	- -	dB
"Trimmer" Stages (Ch 1 - Ch 7)					
Gain		-3.0		+3.0	dB
Gain Steps (15 in No.)		—	0.43	—	dB
Step Error	5	—	—	±0.2	dB
Input Impedance		100.0	—	—	kΩ
"Volume" Stage (Ch 8)					
Gain		-14.0		+14.0	dB
Gain Steps (15 in No.)		—	2.0	—	dB
Step Error	5	—	—	±0.4	dB
Input Impedance		50.0	—	—	kΩ
Timing (See Figure 4)					
Serial Clock "High" Pulse Width (t_{PWH})		250	—	—	ns
Serial Clock "Low" Pulse Width (t_{PWL})		250	—	—	ns
Data Set-up Time (t_{DS})		150	—	—	ns
Data Hold Time (t_{DH})		50	—	—	ns
Load/Latch Set-up Time (t_{LL})		250	—	—	ns
Load/Latch Pulse Width (t_{LLW})		150	—	—	ns
Serial Data Clock Frequency		—	—	2.0	MHz

Notes

1. *Gain Set 0dB. Input Level 1kHz -3.0dB (549mVrms).*
2. *a.c. short-circuit input, measured in a 30 kHz bandwidth.*
3. *See Figure 3.*
4. *Over temperature and supply voltage range.*
5. *With reference to a 1.0 kHz signal.*