L64280
Complex FFT Processor (FFTP)

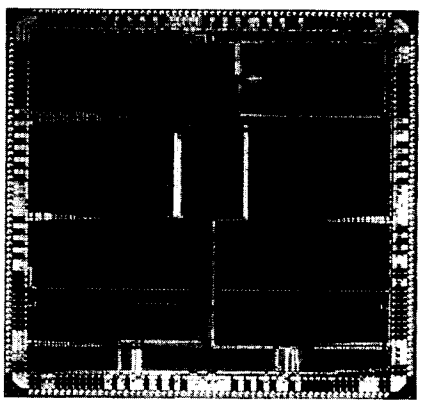
Description

The L64280 FFTP (Fast Fourier Transform Processor) is a floating-point complex FFT processor and is designed for primary use with the L64281 FFTSR (Fast Fourier Transform Video Shift Register) in real-time FFT systems. It can also be used in a single processor configuration in which system cost is reduced along with system performance. The FFTP includes the FFT controller and complex exponential ROM needed to compute transforms of 2048 points or less. For longer transforms, external controllers and coefficient storage devices are required.

The device performs both the forward and inverse transforms and can accept data in either normal order or bit-reversed order.

A variety of operating modes and data formats can be chosen. The input data can be either a floating-point or fixed-point number. Likewise, the output data can be either a floating-point or fixed-point number. For fixed-point outputs, a user supplied scale factor determines which internal bits are output.

In addition to performing FFTs, the device can be operated as a complex MAC, two real MACs or as a MAC with one complex and one real operand. The user can either input a complex or real coefficient or input the phase of a complex exponential or real sinusoid.



L64280 Chip

Features

- Computes FFT butterflies at 20 MHz rate
- Real or complex multiplication-accumulation
- Integer or floating-point data formats
- Internal FFT controller for up to 2K point FFT
- Internal complex exponential, real sinusoid ROM for up to 2K point FFT
- Forty-bit internal accumulation for high precision
- Applications in modulation and demodulation
- Internal controller for single processor systems
- High data rates

Commercial	Military
40 MHz	30 MHz
30 MHz	25 MHz

- Available in a 144-pin CPGA (Ceramic Pin Grid Array) package

Pin Listing and Description

(the Highest Numbered Bit is Always the Most Significant)

EDI.0:3
Four-bit input exponent set to constant for fixed-point data input.

RDI.0:19
Twenty-bit real data mantissa input.

IDI.0:19
Twenty-bit imaginary data mantissa input.

EDO.0:3/OVF.0:3
Four-bit output exponent and overflow flags. In floating-point output mode, the output data exponent appears on these pins. In fixed-point output mode, OVF.0 HIGH indicates overflow of the data on RDO, and OVF.1 is the sign of the data on RDO; OVF.2 HIGH indicates overflow of the data on IDO, and OVF.3 is the sign of the data on IDO.

RDO.0:19
Twenty-bit real data mantissa output.

IDO.0:19
Twenty-bit imaginary data mantissa output.

Pin Listing and Description (the Highest Numbered Bit is Always the Most Significant) (Continued)

RLOWBITS
Forces the output exponent to 15 to read the low 15 bits when HIGH. Should be LOW or left unconnected when output is floating-point format. Should be LOW to read fixed-point data bits specified by internal signals FOE.

W.0:19
Twenty-bit coefficient or phase data input bus. For complex coefficients, the real and imaginary coefficients are multiplexed over the W bus. When using the internal complex exponential, sinusoid ROM, (USEROM HIGH, FFTCOEFF LOW) the 11-bit unsigned phase value is input on the LSBs of this bus. If a real sinusoid is desired (COMPCOEFF LOW), the bit W.11 selects a sine wave when HIGH, and a cosine wave when LOW.

SYNCI
FFT synchronization input (FFT mode) or accumulator reset signal (MAC mode). SYNCI HIGH signifies the beginning of an input data block.

SYNCO
FFT synchronization output. In FFT mode SYNCO HIGH signifies the beginning of a transform data block.

CROSSO
FFT cross output used to control the cross-pass network of either the following L64280 or L64281. The data should be crossed if CROSSO is HIGH and passed if CROSSO is LOW.

CROSSI
FFT cross input CROSSI controls the internal crossing network. The data is crossed if CROSSI is HIGH and passed if CROSSI is LOW. In MAC mode or FFT cycles not using the internal cross network, CROSSI is tied LOW or left unconnected.

CLK
System clock, active at the rising edge.

CI.0:7
Control input bus. Data on this bus is latched into the internal control register specified by REGADR when $\overline{WE}$ is LOW.

$\overline{WE}$
Active-LOW write enable for the CI inputs. When $\overline{WE}$ is LOW, new data is written into the register specified by the address on the REGADR pins.

REGADR.0:1
Control register address. Determines which of the control registers will be loaded with the data on CI when WE goes LOW.

MP
Multipass mode pin. When HIGH, the device is assumed to be in a multipass or single processor system. When LOW, the device is in a pipelined or custom system.

ENDI
Synchronization signal used only in multipass FFT systems (MP HIGH). When HIGH, ENDI signifies the end of the input data block.

ENDO
Synchronization signal used only in multipass FFT systems (MP HIGH). When HIGH, ENDO signifies the end of the output data block.

MPSTARTI
FFT reset signal used only in multipass FFT systems. MPSTARTI goes HIGH to initialize the device for a new transform.

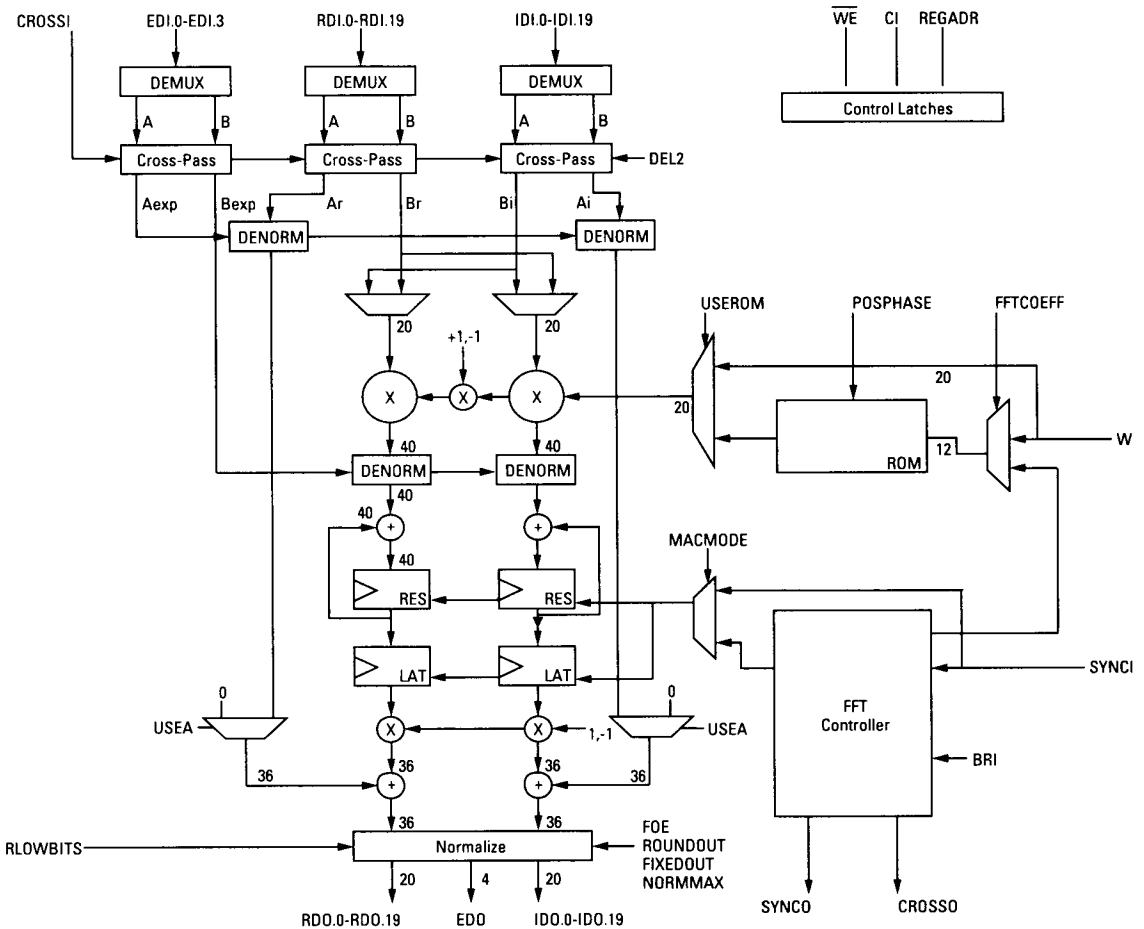
VDO
Valid data output flag (MP HIGH only). When HIGH, indicates that the output data is valid and not a partial result. Can be used to latch the final transform results.

CLKO
FFT delayed CLK. Intended for future use to reduce data output delay from CLK when connected to the following device CLK input. Currently not characterized and should be left unconnected.

Pin Description Summary

Pin	No. of Pins	I/O	Description
EDI.0-EDI.3	4	I	Exponent input
RDI.0-RDI.19	20	I	Real mantissa input
IDI.0-IDI.19	20	I	Imaginary mantissa input
EDO.0-EDO.3	4	O	Exponent output (overflow flags)
RDO.0-RDO.19	20	O	Real mantissa output
IDO.0-IDO.19	20	O	Imaginary mantissa output
RLOWBITS	1	I	Read low bits of result
W.0-W.19	20	I	Coefficient input
CI.0-CI.7	8	I	Control input
$\overline{WE}$	1	I	Write enable for CI bus
REGADR.0:1	2	I	Control register address
SYNCI	1	I	FFT synchronization input
SYNCO	1	O	FFT synchronization output
CROSSI	1	I	FFT cross input
CROSSO	1	O	FFT cross output
MP	1	I	Multipass mode pin
MPSTARTI	1	I	Multipass reset pin
ENDI	1	I	End data block input
ENDO	1	O	End data block output
VDO	1	O	Valid data output
CLK	1	I	System clock
CLKO	1	O	Delayed clock - no connect

Block Diagram



Architecture

FFT Mode

The L64280 has an architecture that is optimized for the computation of the butterfly operations required in the FFT. Two real multipliers compute the single complex product of the butterfly in two clock cycles. Because the butterfly has eight real additions but only four real multiplications, the L64280 has twice as many adders as multipliers. This makes it possible for all hardware to be fully utilized.

The complex exponential coefficients are generated internally via the FFT controller and ROM.

In general, the data storage and manipulation is not performed within the L64280. The L64281 performs these functions. However, for cycles 0 and 1 (1 and 2 if the data is in bit-reversed order) of the FFT, the data storage and manipulation functions are simple enough to implement within the L64280 (Cross-Pass circuit).

MAC Mode

In addition to computing FFT butterflies, the device can be operated in either complex or real MAC and multiplier modes. In complex MAC or multiplier mode, each product is computed in two clock cycles. In real mode, two

Architecture (Continued)

real products (two data streams with the same coefficient) are computed each clock cycle. If one operand is real and the other is complex, one complex product is generated every clock cycle. There is no performance penalty for accumulating the products.

In MAC mode, the SYNCI signal resets the internal accumulator and latches the last accumulated result in the following register. By buffering the accumulator, the final result is held on the output pins until a new result is valid.

In each mode of operation the user can input the unsigned phase, ϕ, and use the internal ROM to generate either the complex coefficient,

$$\cos\left(\frac{2\pi}{2048}\phi\right) + j\sin\left(\frac{2\pi}{2048}\phi\right),$$

or a real coefficient,

$$\cos\left(\frac{2\pi}{2048}\phi\right) \text{ or } \sin\left(\frac{2\pi}{2048}\phi\right).$$

Alternatively, the complex coefficient, W = Wr + jWi, or the real coefficient W can be input directly.

Data Format

The data format is a hybrid floating-point fixed-point scheme. The data inputs and outputs can be either fixed or floating-point numbers while the coefficients are always fixed-point. Although the exponents are only four bits wide, this provides the same dynamic range as a 36-bit fixed-point system. The denormalizers convert the incoming floating-point numbers to the internal fixed-point format. The normalizer at the output converts the fixed-point format back to floating-point. The accumulators are 40 bits wide.

Device Functions

The L64280 has three primary functional options: complex FFT mode, complex MAC mode and real MAC mode. The MAC modes degenerate into multiplier modes if only a single product is accumulated.

In complex FFT mode, the device continually performs the butterfly operation:

$A \leftarrow A + WB$
$B \leftarrow A - WB$

The complex input values, A followed by B, are multiplexed over the RDI, IDI and EDI buses, while the complex output values, A followed by B, are multiplexed over the RDO, IDO and EDO buses. For FFTs with length less than or equal to 2048 points, Wr and Wi are generated internally. For longer transforms, the values Wr and Wi are input sequentially on the W bus. Wr and Wi are input at the same times as A and B, respectively.

In MAC mode, the L64280 computes a sum of products. If the number of products is one, the device operates like a complex multiplier or two real multipliers. In either case, the user can supply the complex or real coefficients directly, or the phase of a sinusoid can be supplied.

Latency

The block diagram does not show any of the pipeline registers. The latency of the device (delay between first input and the first output) is 14 clock cycles in FFT and complex MAC modes and 12 clock cycles in real MAC mode. Therefore the delay from SYNCI to SYNCO is 14 clock cycles in FFT mode. See the functional waveforms for additional timing information, as well as exact timing relationships between input and output data samples.

SYNCO is used to indicate the beginning of the output data block in FFT mode and will always go HIGH 14 cycles after SYNCI is HIGH. If the CM bits are set to a value of 10 or less, SYNCO will go HIGH periodically with a period the same as the block length and synchronized to the last time SYNCI went HIGH. For this case, SYNCI does not need to go HIGH at the beginning of each block, only at the beginning of the first block. If the CM bits are set to 15, SYNCO will only go HIGH 14 cycles after SYNCI goes HIGH and will stay LOW until 14 cycles after the next time SYNCI goes HIGH.

Device Functions (Continued)

Table 1. Device Functions

Mode	Outputs
Complex MAC	$\sum_{i=1}^{N} B_i W_i$
Complex MAC	$\sum_{i=1}^{N} B_i e^{j\left(\frac{2\pi}{2048}\phi_i\right)}$
Complex Multiplier	BW
Complex Multplier	$Be^{j\left(\frac{2\pi}{2048}\phi_i\right)}$
Real MAC	$\sum_{i=1}^{N} A_i W_i, \sum_{i=1}^{N} B_i W_i$
Real MAC	$\sum_{i=1}^{N} A_i \cos\left(\frac{2\pi}{2048}\phi_i\right), \sum_{i=1}^{N} B_i \cos\left(\frac{2\pi}{2048}\phi_i\right)$
Real Multiplier	AW, BW
Real Multiplier	$A\cos\left(\frac{2\pi}{2048}\phi_i\right), B\cos\left(\frac{2\pi}{2048}\phi_i\right)$

Numerical Representations

Data Format

The data format options of the L64280 provide the user with a great deal of flexibility. The input data and output data are represented by two 20-bit two's complement fractional mantissas and a four-bit unsigned exponent. Because the mantissas are two's complement numbers, there is no "hidden bit"; denormalized numbers (including zero) are represented directly. The coefficients are always fixed-point two's complement fractional numbers. The input data value is:

$$(RDI + jIDI)2^{-EDI}$$

For floating-point outputs (FIXEDOUT = 0), the output data value is:

$$(RDO + jIDO)2^{-EDO + NORMMAX}$$

or, for fixed-point outputs (FIXEDOUT = 1), the output data value is:

$$(RDO + jIDO)2^{-FOE + NORMMAX}$$

Normalization

NORMMAX affects the interpretation of the output exponent. If NORMMAX = 0, the input and output exponents have the same significance. That is, the input and output data values will be the same if the input is multiplied by a "true" one. However, if NORMMAX = 1 and the input data is multiplied by a "true" one, the output exponent will be one larger than the input exponent. This mode is used to avoid overflow due to the normal growth (by 1-bit per cycle) in the FFT. If NORMMAX = 1, the output data is always normalized to the largest possible output at that cycle of the FFT. Care must be taken when performing forward FFTs if NORMMAX = 0. NORMMAX should be set LOW in MAC mode.

Fixed-Point Output

If the final FFT results are desired in a fixed-point format, the last processor in the system is set to output fixed-point results. For fixed-point outputs, the output exponent for all data values is set by the internal bits FOE. If FOE is chosen too large, overflow occurs. However, when FIXEDOUT = 1, the output exponent on the EDO pins is replaced by an overflow flag for each mantissa (IDO and RDO) and the sign of each mantissa. The user can easily detect in which direction, if any, each mantissa overflowed.

Fixed-Point Input

If the input data is in a fixed-point format, the input exponent should be used to prevent overflow in the accumulator. For FFTs, the exponents of fixed-point inputs to the first device should be set to 1. If NORMMAX = 1 in each L64280, no overflow will occur in any devices in the system. In MAC mode, larger input expo-

Numerical Representations (Continued)

nents are needed to prevent overflow when a larger number of products is accumulated. When accumulating N products, the input exponents should be set to $\log_2 M$ to prevent overflow for any data inputs, where M is a power of two and is greater than or equal to N.

Rounding

The output is rounded to the RDO.0 and IDO.0 if RNDOUT = 1.

Extended Precision Output

It is also possible to output a 35-bit word in MAC mode (FFT mode does not provide enough time to read the whole data word). To do this, FIXEDOUT should be set to 1, FOE set to 0 and RNDOUT set to 0. For each output word, the top 20 bits will be read when RLOWBITS is LOW and the low 20 bits will be read when RLOWBITS is HIGH. There will be three clock delays from the time RLOWBITS is asserted to the time when the relevant data appears at the output.

Fractional Number Format

In the fractional number system, the binary point is to the right of the most significant bit. This is in contrast to the integer number format in which the binary point is to the right of the least significant bit. In this system, + 1 (0.1111111111111111111) is the largest positive number and - 1 (1.0000000000000000001) is the most negative. Note that zero is represented by a mantissa of 0.00000000000000000000 regardless of the value of the exponent. More explicitly, when operating in a floating-point complex-data mode, the values on the data and coefficient inputs and the data outputs can be expressed as:

$$RDI = -RDI.19 + \sum_{i=0}^{18} RDI.i2^{i-19}$$

$$IDI = -IDI.19 + \sum_{i=0}^{18} IDI.i2^{i-19}$$

$$EDI = \sum_{i=0}^{3} EDI.i2^{i}$$

$$RDO = -RDO.19 + \sum_{i=0}^{18} RDO.i2^{i-19}$$

$$IDO = -IDO.19 + \sum_{i=0}^{18} IDO.i2^{i-19}$$

$$EDO = \sum_{i=0}^{3} EDO.i2^{i}$$

$$W = -W.19 + \sum_{i=0}^{18} W.i2^{i-19}$$

Control and Coefficients

Supplying Coefficients and Phase Values Over the W Bus

When the internal FFT controller is not being used to supply the complex coefficients to the multipliers, the user has a variety of options for generating these coefficients. The real or complex coefficients can be supplied directly via the W bus or a phase value can be supplied and the coefficients determined by the internal ROM. All bits of the W bus that are not specified in Table 2 may be left unconnected or tied to VDD or VSS.

Table 2. Coefficient Sources

Function	USEROM	FFTCOEFF	COMPCOEFF	W BUS
Complex FFT or MAC mode phase supplied	HIGH	LOW	HIGH	W.10-W.0 is phase
Real MAX mode phase supplied	HIGH	LOW	LOW	W.10-W.-0 is phase
Complex FFT or MAC mode coeff supplied	LOW	LOW	HIGH	Real and imaginary parts of coefficient are MUXED over W.19-W.0
Real MAC mode coeff supplied	LOW	LOW	LOW	W.19-W.0 is coefficient
Complex FFT mode phase generated internally	HIGH	HIGH	HIGH	Not used

Control and Coefficients (Continued)

Loading the Control Signals

The function of the device is controlled by two internally latched control words. The data on the 8-bit CI bus is latched into the register specified by REGADR when WE is LOW. The memory map for the device is given in Table 3.

If the length of the transform exceeds 2048 points, some devices will have cycle numbers greater than 10. In these cases and when operating in MAC mode, the internal FFT controller cannot be used and the C and CM bits can be set either HIGH or LOW.

The CM and C words are used to specify the FFT operation being performed. Each device in the 1-D transform system has the same value of CM but a different value of C. The CM bits specify the value of cycleMAX = $(\log_2 N) - 1$. The cycle of each L64280 in an FFT system is specified via the C.0-C.3 bits. For normal order input data (BRI = LOW), the C bits should be set to cycle. If the input data is bit-reversed (BRI = HIGH), then the C bits should be set to 10-cycle. Note that both CM and C must have a value between 0 and 10.

The FOE bits specify the value of the output exponent in fixed-point output mode (FIXEDOUT = 1). The other control bits have functions as shown in Table 4.

Table 3. Memory Map

REGADR	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
0	CM.3	CM.2	CM.1	CM.0	C.3	C.2	C.1	C.0
1	USEA	POSPHASE	NORMMAX	BRI	DEL.2	FFTCOEFF	ESEROM	—
2	MACMODE	COMPCOEFF	FIXEDOUT	RNDOUT	FOE.3	FOE.2	FOE.1	FOE.0

Control and Coefficients
(Continued)

Table 4. Function of Control Bits

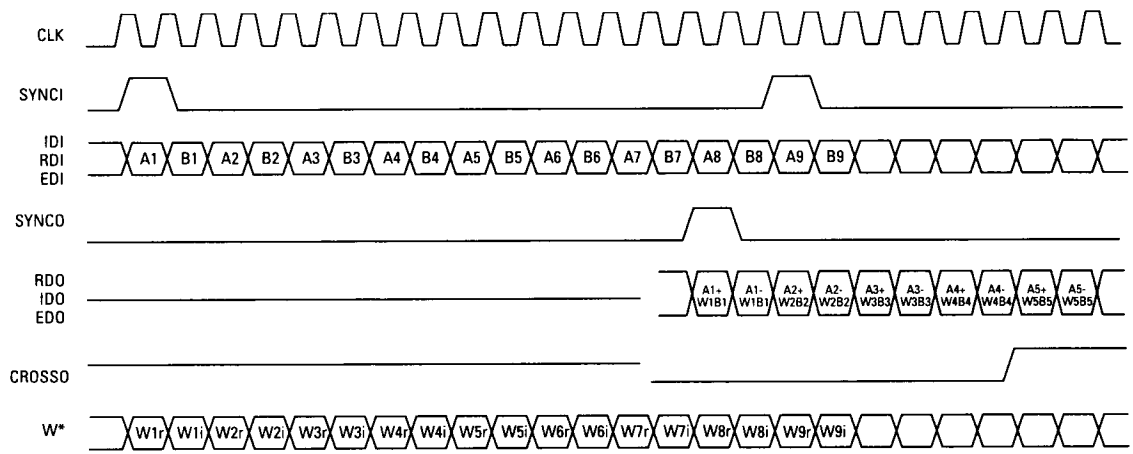
Bit	Value	Function
USEA	0 1	MAC, multiplier mode - compute $\sum W_i B_i$ FFT mode – compute A + WB and A - WB
POSPHASE	0 1	use negative phase, i.e., compute $e^{-j\frac{2\pi}{2048}\phi}$ use positive phase, i.e., compute $e^{j\frac{2\pi}{2048}\phi}$
NORMMAX	0 1	Don't scale output by 1/2 – MAC mode Scale output by 1/2 to prevent overflow in FFT
BRI	0 1	FFT input data in normal order FFT input data in bit-reversed order
DEL2	0 1	FFTP is not in cycle 1 – normal order input and not in cycle 2 – bit reversed order input FFTP is in cycle 1 – normal order input or in cycle 2 – bit-reversed order input
FFTCOEFF	0 1	Coefficients or phase supplied via W bus Phase supplied by internal FFT controller
USEROM	0 1	Multiplier coefficient comes from W Bus Multiplier coefficient comes from ROM
MACMODE	0 1	FFT mode Multiplication or MAC mode
COMPCOEFF	0 1	Coefficients are real – only for MAC mode Coefficients are complex
FIXEDOUT	0 1	Output data is floating-point – EDO is exponent Output data is fixed-point FOE.3-FOE.0 set output scale Overflow indicated on OVF pins
RNDOUT	0 1	Don't round output – used when reading 35-bit output Round output – used when reading only 20-bits of output

Table 5. Typical Control Word Values and CROSSI for Different Modes

Mode	REGADR = 1	REGADR = 2	CROSSI
Forward FFT, normal order input, cycle 0	10100110	0101XXXX	Active
Forward FFT, normal order input, cycle 1	10101110	0101XXXX	Active
Forward FFT, normal order input, cycle > 1	1010X110	0101XXXX	0
Inverse FFT, bit-reversed order input, cycle 0	1101X110	0101XXXX	0
Inverse FFT, bit-reversed order input, cycle 1	11010110	0101XXXX	Active
Inverse FFT, bit-reversed order input, cycle 2	11011110	0101XXXX	Active
Inverse FFT, bit-reversed order input, cycle > 2	1101X110	0101XXXX	0
Complex MAC-input phase, fixed-point out	010XX010	11110000	0
Complex MAC-input coefficient, fixed-point out	0X0XXX00	11110000	0
Real MAC-input coefficient, fixed-point out	0X0XXX00	10110000	0

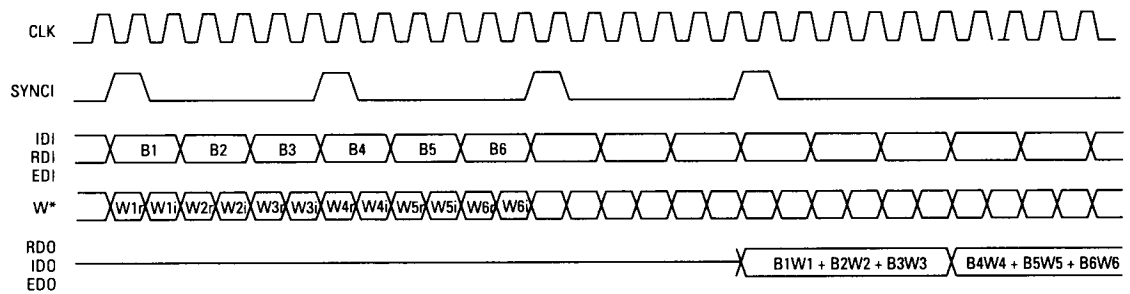
Functional Waveforms

FFT Example



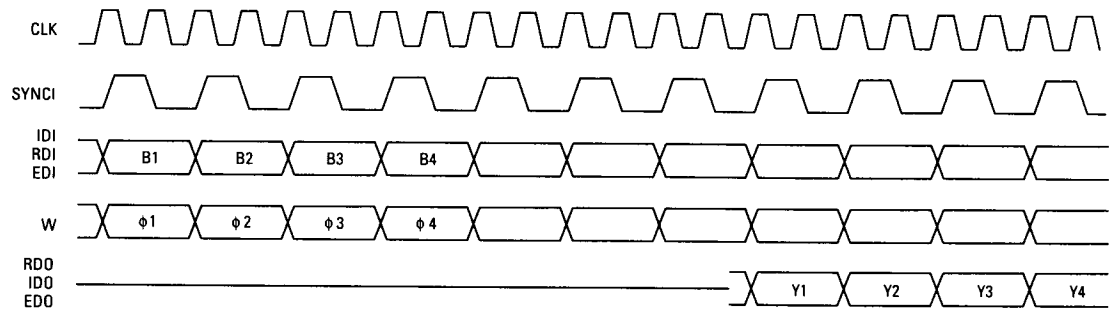
*- only used for FFT's with length > 2048 points and cycle > 10

Complex MAC Example



Functional Waveforms (Continued)

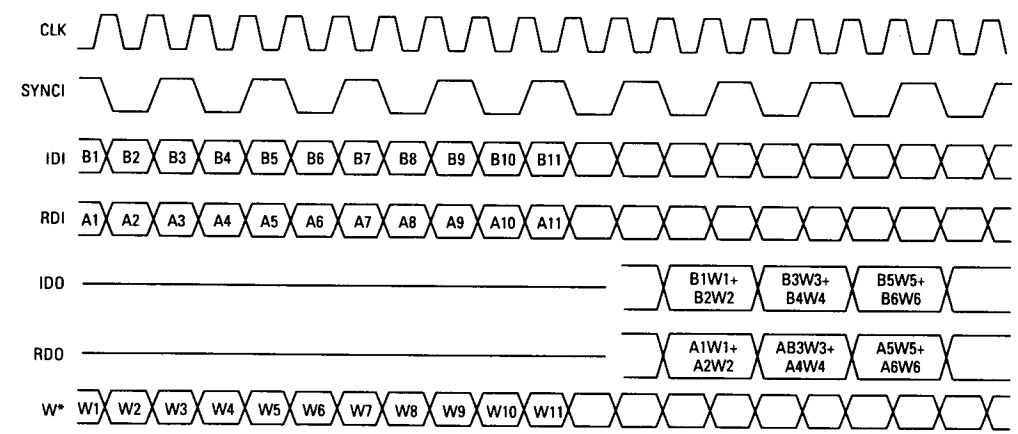
Complex Multiplier Example



$$Y1 = e^{\frac{j2\pi}{2048}\phi_1} B_1 \qquad Y2 = e^{\frac{j2\pi}{2048}\phi_2} B_2$$

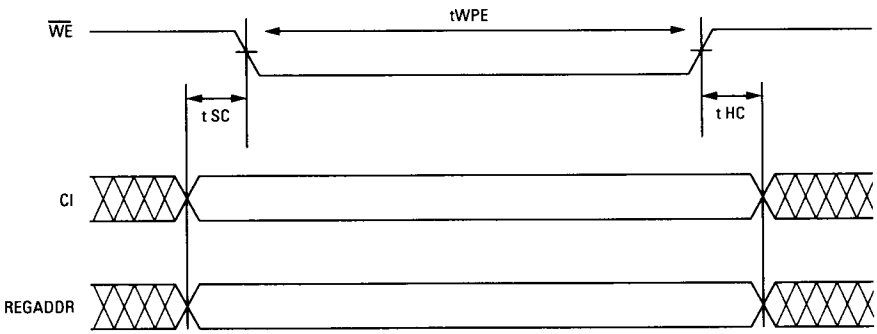
$$Y3 = e^{\frac{j2\pi}{2048}\phi_3} B_3 \qquad Y4 = e^{\frac{j2\pi}{2048}\phi_4} B_4$$

Real MAC Example

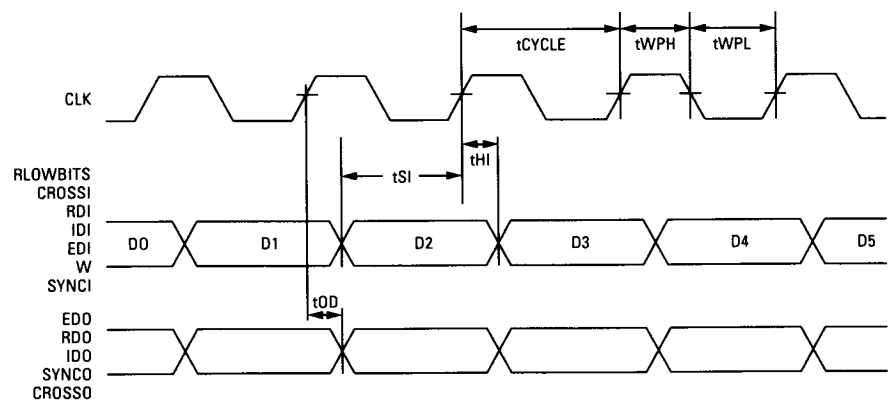


AC Timing Waveforms

Coefficient/Control Section



FFT and MAC Mode I/O Timing



Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD + 0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-4.5 to +5.5	V
Operating ambient temperature range			
Military range	TA	-55 to +125	°C
Commercial range	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5V over the specified temperature and voltage ranges [1]

Symbol	Parameter	Condition			Min	Typ	Max	Units
VIL	Low level input voltage						0.8	V
VIH	High level input voltage							
	Commercial temperature range				2.0			V
	Military temeperature range				2.25			V
IIN	Input current	VIN = VDD			-150		200	µA
VOH	High level output voltage		Comm	Mil				
		IOH=	-4 mA	-3.2 mA	2.4	4.5		V
VOL	Low level output voltage		Comm	Mil				
		IOL=	4 mA	3.2 mA		0.2	0.4	V
IOS	Output short circuit current[1]	VDD = Max, VO = VDD 15				130	mA	
		VDD = Max, VO = 0V			-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS					10	mA
IDQ	Operating supply current	tCYCLE = 25 ns			300		mA	
CIN	Input capacitance	Any input				5		pF
COUT	Output capacitance	Any output				10		pF

Notes:
1. Military temperature range is -55°C to +125°C, ±10% power supply; commercial temperature range is °C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.

AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64280-40		L64280-30	
		Min	Max	Min	Max
tCYCLE	CLK cycle time	25		33	
tPWH (min)	Min CLK pulse width, HIGH	10		14	
tPWL (min)	Min CLK pulse width, LOW	10		14	
tSI	Input setup time	7		10	
tHI	Input hold time	4		7	
tWPE	WE pulse width	15		20	
tSC	REGADDR, CI input setup time	10		15	
tHC	REGADDR, CI input hold time	10		15	
tOD*	Output delay time		18		25

Note: All times are in ns.

AC Switching Characteristics: Military (TA = -55°C to 125°C, VDD = 4.5 V to 5.5 V)

Symbol	Parameter	L64280-30		L64280-25	
		Min	Max	Min	Max
tCYCLE	CLK cycle time	33		40	
tPWH (min)	Min CLK pulse width, HIGH	14		16	
tPWL (min)	Min CLK pulse width, LOW	14		16	
tSI	Input setup time	10		12	
tHI	Input hold time	7		8	
tWPE	WE pulse width	20		24	
tSC	REGADDR, CI input setup time	15		17	
tHC	REGADDR, CI input hold time	15		17	
tOD	Output delay time		25		30

Notes:
1. All times are in ns.
* For the L64280GC-40, tOD is otherwise guaranteed for CLOAD = 35 pF CLOAD = 55 pF

L64280 Package Pin Information (144-Pin PGA, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	CLKO	C7	IDI.5	H13	VSS	N10	CI.2
A2	IDI.16	C8	IDI.4	H14	W.19	N11	IDO.0
A3	IDI.12	C9	CLK	H15	W.16	N12	IDO.3
A4	IDI.11	C10	MP	J1	RDI.13	N13	VSS
A5	IDI.9	C11	CROSSO	J2	RDI.15	N14	IDO.7
A6	VSS	C12	W.17	J3	VSS	N15	IDO.10
A7	VDD	C13	VSS	J13	IDO.17	P1	RDO.14
A8	IDI.3	C14	W.5	J14	IDO.16	P2	RDO.12
A9	IDI.1	C15	W.0	J15	IDO.19	P3	RDO.9
A10	IDI.0	D1	RDI.3	K1	RDI.14	P4	RDO.8
A11	ENDI	D2	EDI.0	K2	RDI.16	P5	RDO.5
A12	CROSSI	D3	EDI.3	K3	RDI.17	P6	RDO.2
A13	SYNCO	D13	W.11	K13	IDO.13	P7	RDO.0
A14	$\overline{WE}$	D14	W.1	K14	IDO.14	P8	EDO.0
A15	W.15	D15	W.2	K15	IDO.18	P9	CI.4
B1	EDI.1	E1	RDI.6	L1	RDI.18	P10	CI.3
B2	IDI.19	E2	RDI.2	L2	RDI.19	P11	CI.0
B3	IDI.15	E3	RDI.0	L3	RDO.16	P12	RLOWBITS
B4	IDI.13	E13	W.3	L13	IDO.9	P13	IDO.1
B5	IDI.10	E14	W.4	L14	IDO.11	P14	IDO.4
B6	IDI.7	E15	W.6	L15	IDO.15	P15	VDD
B7	IDI.6	F1	RDI.9	M1	RDO.19	R1	RDO.11
B8	IDI.2	F2	RDI.5	M2	RDO.17	R2	VDD
B9	SYNCI	F3	RDI.4	M3	RDO.13	R3	RDO.6
B10	MPSTARTI	F13	W.8	M13	IDO.6	R4	RDO.4
B11	ENDO	F14	W.9	M14	IDO.8	R5	RDO.1
B12	VDO	F15	W.12	M15	IDO.12	R6	EDO.2
B13	W.18	G1	RDI.10	N1	RDO.18	R7	EDO.1
B14	W.13	G2	RDI.7	N2	RDO.15	R8	CI.7
B15	W.7	G3	RDI.8	N3	VSS	R9	CI.6
C1	RDI.1	G13	VDD	N4	RDO.10	R10	CI.5
C2	EDI.2	G14	W.10	N5	RDO.7	R11	CI.1
C3	IDI.18	G15	W.14	N6	RDO.3	R12	REGADR.0
C4	IDI.17	H1	RDI.12	N7	EDO.3	R13	REGADR.1
C5	IDI.14	H2	RDI.11	N8	VSS	R14	IDO.2
C6	IDI.8	H3	VDD	N9	VDD	R15	IDO.5

L64280 Package Pin Information (144-Pin PGA, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
P11	CI.0	C5	IDI.14	G3	RDI.8	A13	SYNCO
R11	CI.1	B3	IDI.15	F1	RDI.9	A7	VDD
N10	CI.2	A2	IDI.16	G1	RDI.10	G13	VDD
P10	CI.3	C4	IDI.17	H2	RDI.11	H3	VDD
P9	CI.4	C3	IDI.18	H1	RDI.12	N9	VDD
R10	CI.5	B2	IDI.19	J1	RDI.13	P15	VDD
R9	CI.6	N11	IDO.0	K1	RDI.14	R2	VDD
R8	CI.7	P13	IDO.1	J2	RDI.15	B12	VDD
C9	CLK	R14	IDO.2	K2	RDI.16	A6	VSS
A1	CLKO	N12	IDO.3	K3	RDI.17	C13	VSS
A12	CROSSI	P14	IDO.4	L1	RDI.18	H13	VSS
C11	CROSSO	R15	IDO.5	L2	RDI.19	J3	VSS
A11	ENDI	M13	IDO.6	P7	RDO.0	N13	VSS
B11	ENDO	N14	IDO.7	R5	RDO.1	N3	VSS
D2	EDI.0	M14	IDO.8	P6	RDO.2	N8	VSS
B1	EDI.1	L13	IDO.9	N6	RDO.3	C15	W.0
C2	EDI.2	N15	IDO.10	R4	RDO.4	D14	W.1
D3	EDI.3	L14	IDO.11	P5	RDO.5	D15	W.2
P8	EDO.0	M15	IDO.12	R3	RDO.6	E13	W.3
R7	EDO.1	K13	IDO.13	N5	RDO.7	E14	W.4
R6	EDO.2	K14	IDO.14	P4	RDO.8	C14	W.5
N7	EDO.3	L15	IDO.15	P3	RDO.9	E15	W.6
A10	IDI.0	J14	IDO.16	N4	RDO.10	B15	W.7
A9	IDI.1	J13	IDO.17	R1	RDO.11	F13	W.8
B8	IDI.2	K15	IDO.18	P2	RDO.12	F14	W.9
A8	IDI.3	J15	IDO.19	M3	RDO.13	G14	W.10
C8	IDI.4	C10	MP	P1	RDO.14	D13	W.11
C7	IDI.5	B10	MPSTARTI	N2	RDO.15	F15	W.12
B7	IDI.6	E3	RDI.0	L3	RDO.16	B14	W.13
B6	IDI.7	C1	RDI.1	M2	RDO.17	G15	W.14
C6	IDI.8	E2	RDI.2	N1	RDO.18	A15	W.15
A5	IDI.9	D1	RDI.3	M1	RDO.19	H15	W.16
B5	IDI.10	F3	RDI.4	R12	REGADR.0	C12	W.17
A4	IDI.11	F2	RDI.5	R13	REGADR.1	B13	W.18
A3	IDI.12	E1	RDI.6	P12	RLOWBITS	H14	W.19
B4	IDI.13	G2	RDI.7	B9	SYNCI	A14	$\overline{WE}$

Packaging

144-Pin Ceramic Pin Grid Array: See FE Package in Package Selector Guide

Ordering Information

L64280 G M -XX

- **-XX** — Speed in MHz
- **M** — Temperature Range/Flow Option
  - C = Commercial (0°C to 70°C)
  - M = Military (-55°C to +125°C), Processed to MIL-STD-883C Level B
- **G** — Package Code
  - G = 144-Pin Ceramic Pin Grid Array
- **L64280** — Device Type
  - Complex FFT Processor