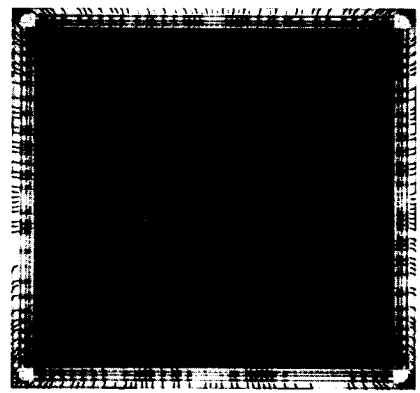
L64220
Rank-Value Filter (RVF)

Description

The L64220 computes a given rank of the input values in a moving window and outputs the rank value. The operation is similar to a linear transversal filter except that the output is chosen from a sorted list of the input values rather than a weighted sum of the input values. Some examples of useful rank values include the maximum, minimum and median. Median filtering has been shown to be effective in removing noise that has a probability density with long tails (i.e., spikey noise), while preserving monotonic changes in the input data. The maximum and minimum can also be used to suppress certain types of noise in a non-linear manner.

The Rank-Value Filter can be reconfigured for operation as an 8 x 8, 4 x 16, 2 x 32 filter or as a 1 x 64 1-D filter. Values can be masked from the computation, giving the user very general control over the window of the filter. Thus, the size and shape of the window can be varied for many applications.



L64220 Chip

Features

- 64-tap, 12-bit reconfigurable Rank-Value Filter processor (RVF)
- Sorts and selects output data value based upon input rank (000000 = min, 111111 = max)
- Configurable for 8 x 8, 4 x 16, 2 x 32 or 64-tap window size
- Operates on signed or unsigned data
- Eight separate 12-bit input buses
- Configurable window shape and size
- Double-buffered coefficient/control registers
- High-speed real-time operation

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

- Extremely useful as a median filter to remove impulse-like (salt and pepper) noise
- Fully compatible with other LSI Logic L64200 series devices

Architecture

The L64220 Rank-Value Filter (RVF) sorts all the values within a window and outputs the value of interest as determined by the RANK selector. Commonly used rank values are the maximum or minimum value within a set of inputs. The most common application of the device will be as a median filter which has excellent properties for removal of impulse-like noise. The device is a stand-alone filter which can operate on either one-dimensional or two-dimensional windows where each data point is up to 12 bits in length. The L64220 is easily reconfigurable to perform RVF operations with a variety of window sizes and shapes.

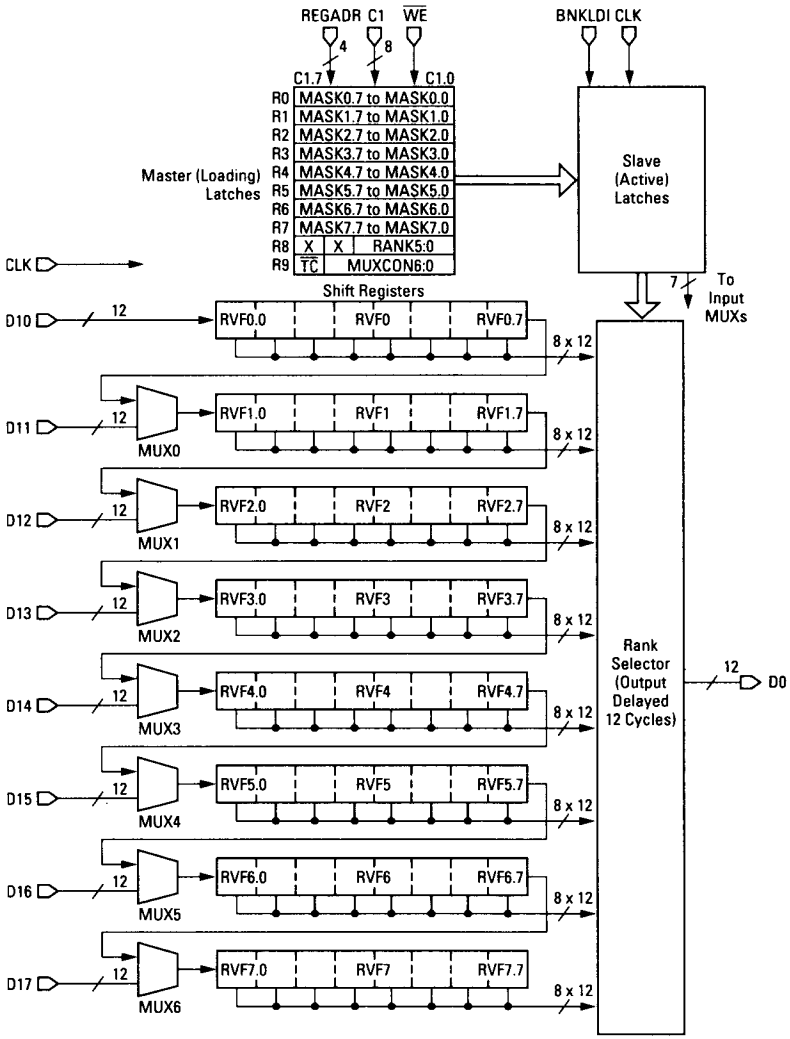
The Rank-Value Filter operates at very high speeds and is useful in high-end applications such as radar signal processing, image processing, high-speed data communications and other areas where performance and processing power are important.

The device contains eight individual 8-tap shift registers (RVF0–RVF7), each 12 bits wide. By controlling the input source to each 8-tap shift-register section, the Rank-Value Filter can be configured as a 64-tap 1-D Rank-Value, or as a 2-D filter with a 2 x 32, 4 x 16 or 8 x 8 window.

Architecture

Any element in the window can be masked by setting any of the 64 mask bits LOW. Masking is useful for reducing the size or changing the shape of the processing window. The N unmasked data values in the window are sent to the rank selector. The rank selector outputs the value with the rank that is stored in control register 8. The maximum value always has a rank of 63, while the minimum has a value of 64-N.

Block Diagram



Pin Listing and Description

DIX.Y
Data inputs where X represents one of eight individual 12-bit input buses and Y represents the individual bit location within the 12-bit bus. For example, DI3.11 is the MSB of the DI3 bus.

C1.0 to C1.7
Coefficient/control input data. Data is written into the master stage of the coefficient/control register (designated by address REGADR0:3) when $\overline{WE}$ is LOW.

REGADR.0 to REGADR.3
4-bit address designating the location into which data provided at CI will be written into the master section of the double-buffered coefficient/control register.

$\overline{WE}$
Active LOW write enable. Data provided at CI will be written into the master section of the double-buffered control register location designated by REGADR when $\overline{WE}$ is held LOW.

BNKLDI
Slave register BANK LOAD enable input. Enables data transfer from the master section of the double-buffered control registers into the slave section (where it becomes active) at the next rising edge of CLK.

CLK
System clock. Controls loading of all data shift registers. Also controls the loading of the slave section of the double-buffered coefficient/control (in conjunction with BNKLDI).

DO.0 to DO.11
12-bit output bus. Provides the sorted rank value based upon the rank held in register R8. DO.11 is the MSB.

$\overline{TEST}$
Reserved LSI Logic test input. Must be held HIGH or left unconnected by the user during normal operation of the device.

Data I/O

One-Dimensional Configuration:
The Rank-Value Filter accepts 12-bit data through the DI0 bus port. The data is fed into the first shift register tap RVF0.0, then shifted to shift register tap RVF0.1 in the next cycle, and so on, up to RVF0.7. For one-dimensional processing, the select line of MUX0 is set to pass data shifted out of RVF0.7 into RVF1.0. To implement a 64-tap 1-D filter, select lines of MUX1–MUX6 are set so that data out of the last shift register in one bank of 8 RVF taps is fed directly into the first shift register of the next bank. All unused inputs (DI1 through DI7) must be set to LOW (GND) or HIGH (VDD) for the device to operate properly.

Two-Dimensional Configuration:
A single Rank-Value Filter can be configured to process a 2 x 32, 4 x 16 or 8 x 8 window of video data. For 2-D video processing the L64220 should be used with one or more of the L64210/L64211 Variable-Length Video Shift Registers. For an 8 x 8 filter window with 12-bit data, the eight 12-bit data bus outputs (D0.0–D0.7) from two L64211s are input to the eight input bus ports (DI0–DI7) of the L64220. The select lines for MUX0 to MUX6 are set to pass data directly from the input bus pins DI1 to DI7 (not from the last taps of RVF0 to RVF6) into the first shift register taps of RVF1 to RVF7.

Control/Coefficient Input (CI) Bus

The L64220 provides a double-buffered mechanism for asynchronously loading control inputs. The storage registers for these control signals consist of two stages, a master and a slave section. Each of these stages contains a total of ten register locations (R0–R9). The master registers are addressed by the 4-bit REGADR input. There are eight bits in each register.

The first eight register locations (R0-R7) contain the mask inputs for each of the 64 window locations. R0 to R7 contain the eight mask bits for the eight shift register locations in RVF0 to RVF7, respectively. When a mask bit is a 1, the data at the corresponding position in the window is included in the rank computation. When a mask bit is a 0, that data value which corresponds to the mask bit is ignored or masked during the sorting process which leads to the rank value. Using the mask bits the user can have full control over the shape and size of the window. For example, to use the RVF to perform 5 x 5 median filtering, 25 window locations would be left unmasked.

The ninth register (R8) holds the 6-bit rank value. This value determines the rank of the output value. A rank of 63 always corresponds to the maximum. The minimum has a rank of 64–N, where N is the number of unmasked values in the window. The most significant two bits of this register are inactive.

Control/Coefficient Input (CI) Bus (Continued)

The tenth register (R9) serves the dual purpose of setting the input MUXs and determining the data type. The least significant 7-bit locations govern the input MUX controls which determine which input buses are active and therefore the shape of the window. When all bit locations are LOW, the Rank-Value Filter acts as a 1-D filter, accepting only data from DI0.

When a single control bit is set HIGH, the corresponding input MUX allows data to feed directly from the appropriate input bus into the Rank-Value Filter. When all bit locations are HIGH and all input buses active, the Rank-Value Filter window is 8 x 8. The final bit location in R9 sets the data type. A LOW value means that incoming data is two's complement type. A HIGH value indicates that the incoming data is unsigned.

The control register section consists of two separate stages, a master (loading) section and a slave (active) section. Data is loaded into the master registers in an asynchronous fashion, then passed on to the slave section under the control of BNKLDI (bank load input).

To load the master registers, control words are input on the 8-bit CI bus. These words are asynchronously loaded into one of the ten register locations indicated by the REGADR input as long as $\overline{WE}$ is LOW. Once all appropriate data have been loaded in the master latches, it is transferred to the slave latches by strobing BNKLDI HIGH. All new control words then become active simultaneously at the next rising edge of CLK.

There are three methods of loading and transferring control signals. The first and most common method is to load the control signals into the master latch asynchronously to the system CLK and transfer it to the slave latch synchronously to the CLK. When all master latches have been loaded, the control signals can be bank-loaded simultaneously into the Rank-Value Filter by enabling the slave latches (occurs when BNKLDI and CLK are HIGH). This transfer is done synchronously to CLK. This is illustrated in the diagram "AC Timing Waveforms–Bank Loading of Controls." This method provides the flexibility of loading new control signals into the processor, while continuing the processing of data with the previous set of control signals. When BNKLDI and CLK are both HIGH, the filter operation will change cleanly from the use of old control signals to the new.

The second method is to load and transfer control signals synchronously to the system clock. This can be done with BNKLDI tied HIGH. $\overline{WE}$ is pulsed LOW when CLK is LOW. During this time, a new control signal on the CI bus is loaded into the master latch whose location has been determined by REGADR.0–REGADR.3. On the next rising edge of CLK, the control signal is transferred to the slave latch, which provides the active control signal. In this manner, a new control signal can replace the current one within a single cycle. This can be done only with cycle times approaching 80 ns (COM) or more.

The third approach is to asynchronously load and transfer new control signals over several cycles. This technique is used when it is not convenient to supply BNKLDI or $\overline{WE}$ signals which are synchronous to CLK. BNKLDI can be tied HIGH and $\overline{WE}$ operated asynchronously. In this case, every time a new control signal is loaded, the processor output could be undefined for up to 100 cycles after the rising edge of $\overline{WE}$.

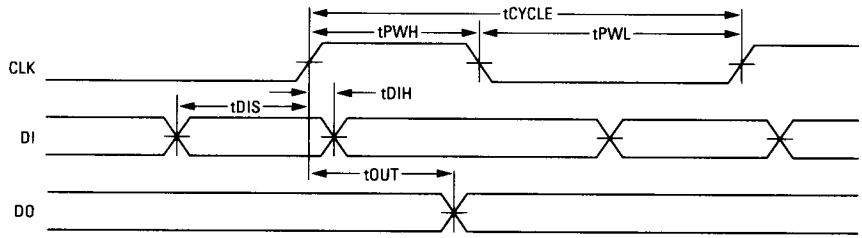
The internal signals MUXCON.0 to MUXCON.6 are select lines for MUX0 to MUX6. When any MUXCON is HIGH, the corresponding mux select line is set such that external data at the input bus pins in transferred to the corresponding 8-tap RVF block. When LOW, data is transferred from the previous RVF block to the output of the MUX. The following table summarizes some of the possible configurations of the L64220 window, which must be set during initialization of the processor.

MUXCON.0-MUXCON.6	Window Shape
0000000	1 x 64
0001000	2 x 32
0101010	4 x 16
1111111	8 x 8

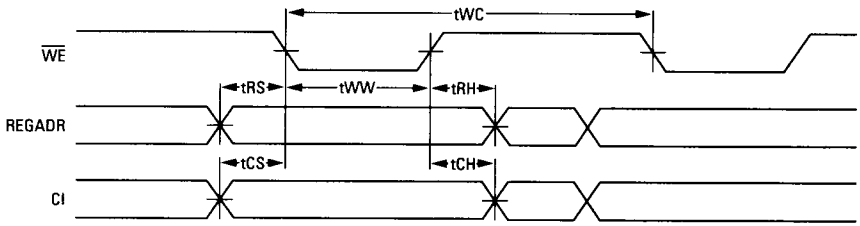
These are the most common configurations of the window shape. Other configurations are possible.

AC Timing Waveforms

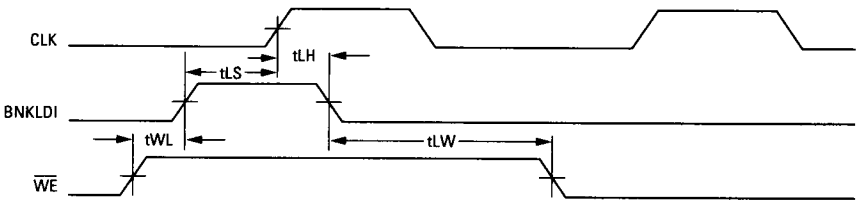
Normal Filter Operation



Normal Controls into Master Section (Methods I, II, III)

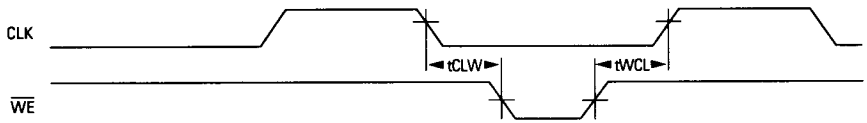


Bank Loading of Controls
Synchronous Transfer from Master to Slave Registers (Method I)

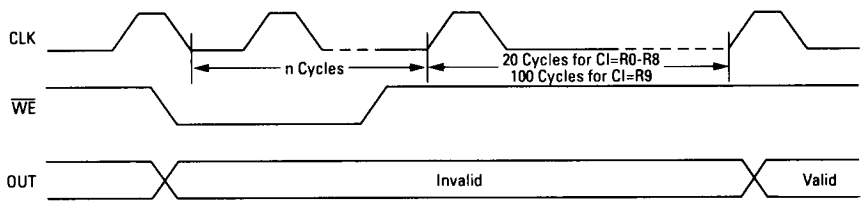


AC Timing Waveforms
(Continued)

Sychronous Loading of Master Section and Sychronous Transfer to Slave Section with Bank Load HIGH (Method II)



Sychronous Loading of Master Section and Sychronous Transfer to Slave Section with Bank Load HIGH (Method II)



AC Switching Characteristics: Commercial (TA=0°C to 70°C, VDD=4.75 V to 5.25 V)

Symbol	Parameter	L64220-20		L64220-15	
		Min	Max	Min	Max
tCYCLE	Minimum clock (CLK) cycle time	50		65	
tPWH	Minimum clock (CLK) pulse width HIGH	20		25	
tPWL	Minimum clock (CLK) pulse width LOW	20		25	
tDIS	Input data (DI) set-up time	15		20	
tDIH	Input data (DI) hold time	5		7	
tOUT	Output delay (DO) from CLK↑		30		40
tLS	BNKLDI set-up time with respect to CLK↑	15		20	
tLH	BNKLDI hold time with respect to CLK↑	5		7	
tWL	$\overline{WE}$ set-up time with respect to BNKLDI↑	5		7	
tLW	$\overline{WE}$ hold time with respect to BNKLDI↑	tPW+15		tPW+20	
tRS	REGADR set-up time with respect to $\overline{WE}$↓	10		15	
tRH	REGADR hold time with respect to $\overline{WE}$↑	10		15	
tCS	CI set-up time with respect to $\overline{WE}$↓	10		15	
tCH	CI hold time with respect to $\overline{WE}$↑	10		15	
tWW	Minimum $\overline{WE}$ pulse width LOW	20		25	
tWC	Minimum $\overline{WE}$ cycle time	50		65	
tCLW	CLK↓ before $\overline{WE}$↓	20		25	
tWCL	CLK↑ after $\overline{WE}$↑	20		25	

Note: All units in ns, output loading=50 pF.

AC Switching Characteristics: Military (TA=-55°C to 125°C, VDD=4.5 V to 5.5 V)

Symbol	Parameter	L64220-16		L64220-12	
		Min	Max	Min	Max
tCYCLE	Minimum clock (CLK) cycle time	60		75	
tPWH	Minimum clock (CLK) pulse width HIGH	25		30	
tPWL	Minimum clock (CLK) pulse width LOW	25		30	
tDIS	Input data (DI) set-up time	20		25	
tDIH	Input data (DI) hold time	7		15	
tOUT	Output delay (DO) from CLK↑		40		50
tLS	BNKLDI set-up time with respect to CLK↑	20		25	
tLH	BNKLDI hold time with respect to CLK↑	7		15	
tWL	$\overline{WE}$ set-up time with respect to BNKLDI↑	7		15	
tLW	$\overline{WE}$ hold time with respect to BNKLDI↓	tPW+20		tPW+25	
tRS	REGADR set-up time with respect to $\overline{WE}$↓	15		20	
tRH	REGADR hold time with respect to $\overline{WE}$↑	15		20	
tCS	CI set-up time with respect to $\overline{WE}$↓	15		20	
tCH	CI hold time with respect to $\overline{WE}$↑	15		20	
tWW	Minimum $\overline{WE}$ pulse width LOW	25		30	
tWC	Minimum $\overline{WE}$ cycle time	60		75	
tCLW	CLK↓ before $\overline{WE}$↓	25		30	
tWCL	CLK↑ after $\overline{WE}$↑	25		30	

Note: All units in ns, output loading=50 pF.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD +0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Operating ambient temperature range			
Military	TA	-55 to +125	°C
Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD=5 V over the specified temperature and voltage ranges (1)

Symbol	Parameter	Condition			Min	Typ	Max	Unit
VIL	Low level input voltage						0.8	V
VIH	High level input voltage Commercial temperature range Military temperature range				2.0 2.25			V V
IIN	Input current	VIN = VDD			-150		200	µA
VOH	High level output voltage		Comm	Mil				
		IOH =	-4 mA	-3.2 mA	2.4	4.5		V
VOL	Low level output voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOS	Output short circuit current(2)	VDD = Max, VO = VDD			15		130	mA
		VDD = Max, VO = OV			-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS					10	mA
IDD	Operating supply current	tCYCLE = 50 ns				300		mA
CIN	Input capacitance	Any input				5		pF
COUT	Output capacitance	Any output				10		pF

Notes:
1. Military temperature range is -55°C to +125°C, ±10% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.

Application Examples

Example No. 1: 8-Bit Unsigned Data Operation
System Configuration: Use the L64210 Variable-Length Video Shift Register as a front end. Set it for 512 pixel operation. Tie the three 8-bit output buses (DO0, DO1 and DO2) to the first three inputs of the L64220 Rank-Value Filter (DI0, DI1, DI2) tying the four LSBs and all other unused inputs to VDD or GND.

The rank value will appear in the eight most significant bits of DO delayed by 13 cycles relative to the input data.

Control Inputs: Shown below is the set-up for the Coefficient/control registers:

Mask locations are set up to configure the L64220 as a 3 x 3 window (all other locations are masked out).

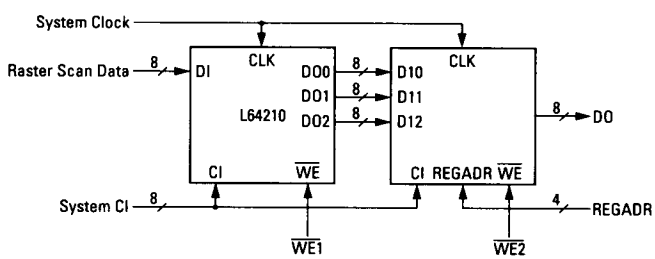
RANK is chosen to find the median in a 3 x 3 field:

RANK =64–window size+desired RANK (0=min)
=64–(3 x 3) + 4 (median)
=64–9 + 4
=59.

MUX controls are all set to 1 (all input lines active) and $\overline{TC}$ is set to 1 (unsigned data).

REGADR	CI7	CI6	CI5	CI4	CI3	CI2	CI1	CI0	
0	0	0	0	0	0	1	1	1	Mask0
1	0	0	0	0	0	1	1	1	Mask1
2	0	0	0	0	0	1	1	1	Mask2
3	0	0	0	0	0	0	0	0	Mask3
4	0	0	0	0	0	0	0	0	Mask4
5	0	0	0	0	0	0	0	0	Mask 5
6	0	0	0	0	0	0	0	0	Mask6
7	0	0	0	0	0	0	0	0	Mask7
8	X	X	1	1	1	0	1	1	RANK
9	1	1	1	1	1	1	1	1	$\overline{TC}$, MUXCON

3 x 3 Median Filter for a 512 x 512 Image



Application Examples
(Continued)

Example No. 2: 12-Bit Two's Complement Data Operation

System Configuration: Use two L64210 Variable-Length Video Shift Registers as a front end to the Rank-Value Filter. Set them both for 1024 pixel operation. One will format the eight most significant bits of the 12-bit data. The other will format the four least significant bits. The CLK, $\overline{WE}$, REGADR and CI are connected as before.

To configure the L64220 to operate on a 4 x 9 window, every other input bus is used (DI0, DI2, DI4, DI6).

RANK value will appear on the 12-bit output delayed by 13 cycles relative to the input data.

Control Inputs: Shown below is the set-up for the coefficient/control registers:

The filter is first configured for a 4 x 16 window. The last seven bits in each odd-numbered row are masked out to reduce the window size to 4 x 9. Here, data from DI0 feeds into RVF through RVF0.7 then to RVF1.0. All other locations in RVF1 are masked out. DI2, DI4, and DI6 are set up in a similar manner to DI0.

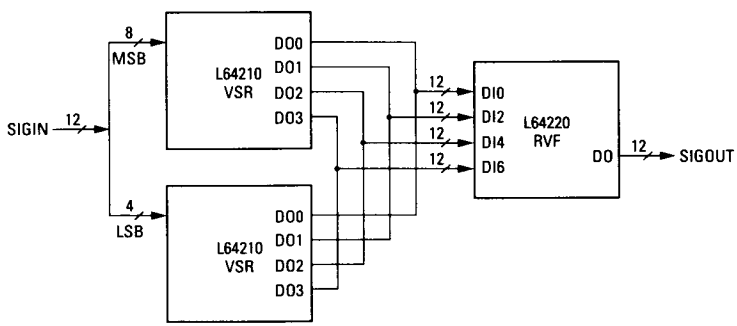
Rank Value =64– window size + desired RANK
=64–(4 x 9) + 0(min value)
=64– 36
=28.

MUX controls are set up to allow every other input bus to be used (nominally 4 x 16 filter). DI0, DI2, D14, and DI6 are all active. All other inputs must be tied to 0V or 5V.

$\overline{TC}$ is set to 0, data is two's complement.

REGADR	CI7	CI6	CI5	CI4	CI3	CI2	CI1	CI0	
0	1	1	1	1	1	1	1	1	Mask0
1	0	0	0	0	0	0	0	1	Mask1
2	1	1	1	1	1	1	1	1	Mask2
3	0	0	0	0	0	0	0	1	Mask3
4	1	1	1	1	1	1	1	1	Mask4
5	0	0	0	0	0	0	0	1	Mask 5
6	1	1	1	1	1	1	1	1	Mask6
7	0	0	0	0	0	0	0	1	Mask7
8	X	X	0	1	1	1	0	0	RANK
9	0	0	1	0	1	0	1	0	$\overline{TC}$, MUXCON

4 x 9 Minimum Filter on a 1K x 1K Image



Application Examples
(Continued)

Example No. 3: 12-Bit Unsigned Data Operation

System Configuration: 12-bit data feeds directly into DI0. All other inputs are held LOW.

12-bit median value will appear on D0 delayed by 13 cycles relative to the input data.

Control Inputs: Shown below is the set-up for the coefficient/control registers:

All mask locations are 1 since all filter locations are active.

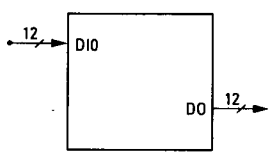
RANK is chosen to find the median of the 64 data points.

Mask Value=64–window size+desired RANK
=64–64 + 32
=32

MUX controls ae all set to 0 because only DI 0 is active. $\overline{TC}$ is set to 1 for unsigned data.

REGADR	CI7	CI6	CI5	CI4	CI3	CI2	CI1	CI0	
0	1	1	1	1	1	1	1	1	Mask0
1	1	1	1	1	1	1	1	1	Mask1
2	1	1	1	1	1	1	1	1	Mask2
3	1	1	1	1	1	1	1	1	Mask3
4	1	1	1	1	1	1	1	1	Mask4
5	1	1	1	1	1	1	1	1	Mask 5
6	1	1	1	1	1	1	1	1	Mask6
7	1	1	1	1	1	1	1	1	Mask7
8	X	X	1	0	0	0	0	0	RANK
9	1	0	0	0	0	0	0	0	$\overline{TC}$, MUXCON

1-D, 64-Tap Median Filter



Pinout Diagram

155-Pin Ceramic Pin Grid Array (CPGA)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A		GND	DI1.10	DI6.7	DI3.7	DI0.7	DI5.6	GND	VDD	DI1.6	NC	NC	DI5.3	DI2.3	VDD	GND
B	VDD	DI4.10	DI2.10	DI7.7	DI4.7	DI1.7	DI6.6	BNK-LDI	DI3.6	DI0.6	NC	DI7.3	DI4.3	DI1.3	DI0.3	VDD
C	DI6.10	DI5.10	DI3.10	DI0.10	DI5.7	DI2.7	DI7.6	DI4.6	DI2.6	NC	NC	DI6.3	DI3.3	DI7.2	DI6.2	DI5.2
D	DI1.11	DI0.11	DI7.10											DI4.2	DI3.2	DI2.2
E	DI4.11	DI3.11	DI2.11											DI1.2	DI0.2	DI1.7
F	DI7.11	DI6.11	DI5.11											DI6.1	DI5.1	DI4.7
G	REG-ADR.2	REG-ADR.3	$\overline{WE}$											DI3.1	DI2.1	DI1.1
H	GND	REG-ADR.0	REG-ADR.1					Top View Cavity Down						DI0.1	NC	GND
J	VDD	CI.0	CI.1											DI6.0	DI7.0	VDD
K	CI.2	CI.3	CI.4											DI3.0	DI4.0	DI5.0
L	CI.5	CI.6	CI.7											DI0.0	DI1.0	DI2.0
M	$\overline{TEST}$	DI0.9	DI1.9											NC	NC	NC
N	DI2.9	DI3.9	DI5.9											DI7.4	NC	NC
P	DI4.9	DI6.9	DI7.9	DI1.8	DI5.8	DO.11	DO.8	DO.6	DO.3	DO.0	DI2.5	DI5.5	DI0.4	CLK	DI5.4	DI6.4
R	GND	NC	DI0.8	DI3.8	DI6.8	DO.10	DO.7	DO.5	DO.4	DO.1	DI1.5	DI4.5	DI7.5	DI2.4	DI4.4	GND
T	VDD	GND	DI2.8	DI4.8	DI7.8	DO.9	GND	VDD	GND	DO.2	DI0.5	DI3.5	DI6.5	DI1.4	DI3.4	VDD

Packaging

155-Pin Grid Array Ceramic Cavity Down Package: See FR Package in Package Selector Guide.

Ordering Information

L64220 G M -XX

- -XX: Speed in MHz
- M: Temperature Range/Flow Option
  C=Commercial (0°C to 70°C)
  M=Military (-55°C to +125°C), Processed to MIL-STD-883C Level B.
- G: Package Code
  G=155 Pin Ceramic Pin Grid Array
- L64220: Device Type
  Rank-Value Filter