CMOS/MOS
INTEGRATED
CIRCUIT

HCC/HCF 40105B

FIFO REGISTER

- INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS
- 3-STATE OUTPUTS
- EXPANDABLE IN EITHER DIRECTION
- STATUS INDICATORS ON INPUT AND OUTPUT
- RESET CAPABILITY
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 40105B** (extended temperature range) and **HCF 40105B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.

The **HCC/HCF 40105B** is a low-power first-in-first-out (FIFO) "elastic" storage register that can store 16 4-bit words. It is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

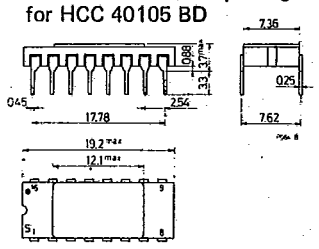
ORDERING NUMBERS:

HCC 40105 BD for dual in-line ceramic package
HCC 40105 BF for dual in-line ceramic package, frit seal
HCC 40105 BK for ceramic flat package
HCF 40105 BE for dual in-line plastic package
HCF 40105 BF for dual in-line ceramic package, frit seal

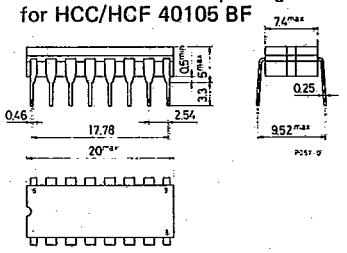
HCC/HCF 40105B

MECHANICAL DATA (dimensions in mm)

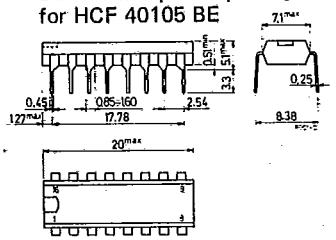
Dual in-line ceramic package for HCC 40105 BD



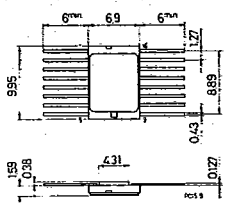
Dual in-line ceramic package for HCC/HCF 40105 BF



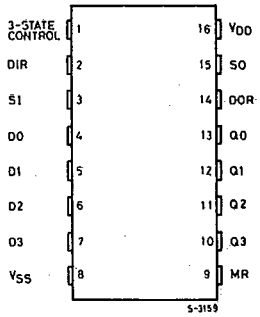
Dual in-line plastic package for HCF 40105 BE



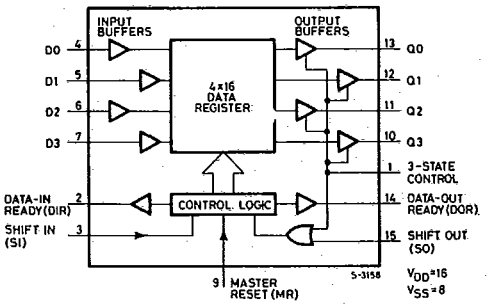
Ceramic flat package for HCC 40105 BK



PIN CONNECTIONS



FUNCTION DIAGRAM

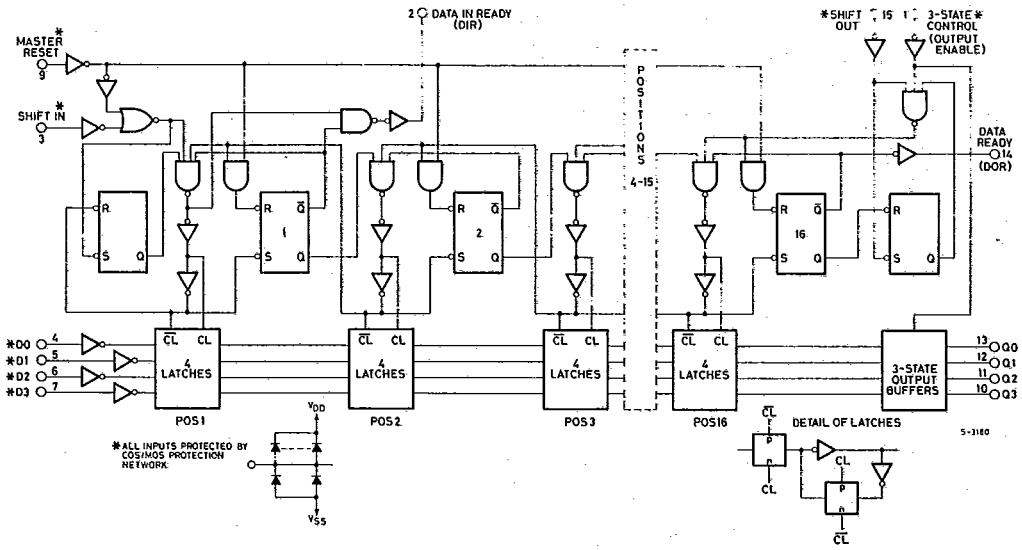


RECOMMENDED OPERATING CONDITIONS

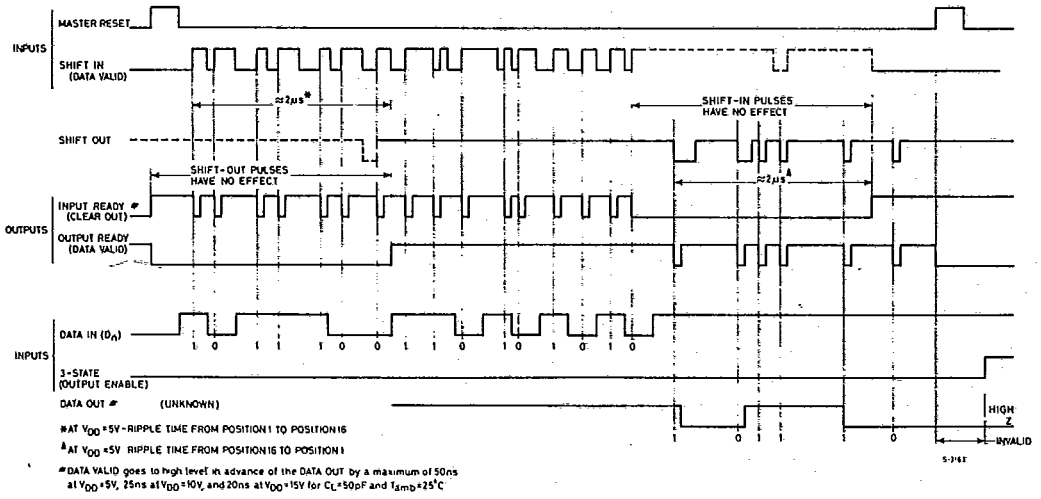
V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

HCC/HCF 40105B

LOGIC DIAGRAM



TIMING DIAGRAM



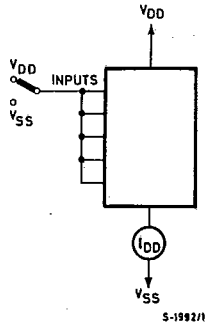
*AT V_{DD} =5V - RIPPLE TIME FROM POSITION 1 TO POSITION 16

▲AT V_{DD} =5V RIPPLE TIME FROM POSITION 16 TO POSITION 1

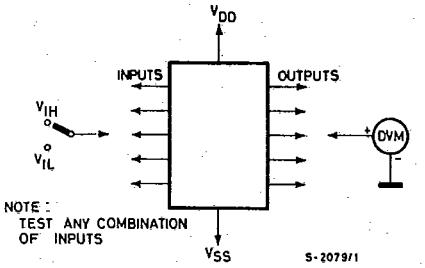
#DATA VALID goes to high level in advance of the DATA OUT by a maximum of 50ns at V_{DD} =5V, 25ns at V_{DD} =10V, and 20ns at V_{DD} =15V for C_L =50pF and T_{amb} =25°C

TEST CIRCUITS

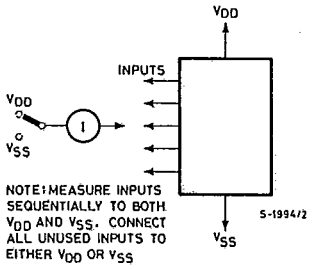
Quiescent device current



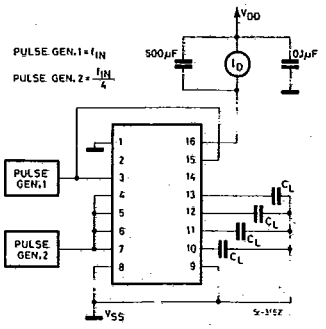
Input voltage



Input leakage current

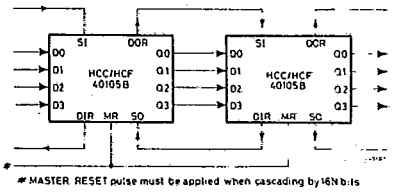


Dynamic power dissipation



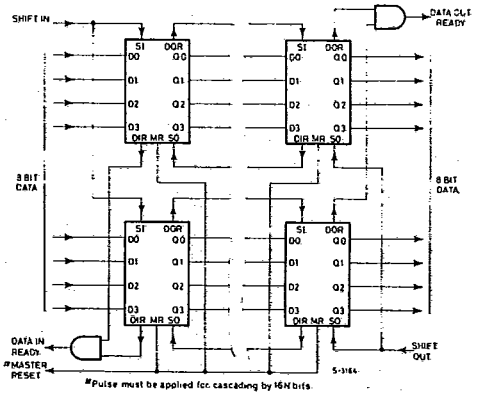
TYPICAL APPLICATIONS

Expansion, 4 bits-wide-by-16 N-bits long



MASTER RESET pulse must be applied when cascading by 16N bits

Expansion, 8 bits-wide-by-16 N-bits long



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	Values T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$±10^{-5}$	±0.3		± 1	
I_{OH}, I_{OL} **	3-state output leakage current	HCC types	0/18	0/18		18		±0.4		$±10^{-4}$	±0.4		±12	μA
		HCF types	0/15	0/15		15		±1.0		$±10^{-4}$	±1.0		±7.5	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

** Forced output disable.

DYNAMIC ELECTRICAL CHARACTERISTICS (T$_{amb}$= 25°C, C$_L$= 50 pF, R$_L$= 200 kΩ, typical temperature coefficient for all V$_{DD}$ values is 0.3%/°C, all input rise and fall time = 20 ns)

Parameter		Test conditions	Values			Unit
		V$_{DD}$ (V)	Min.	Typ.	Max.	
t_{PHL}	Propagation delay time Shift-Out or Reset to Data-Out Ready	5		185	370	ns
		10		90	180	
		15		65	130	
t_{PHL}	Propagation delay time Shift-In to Data-In Ready	5		160	320	ns
		10		65	130	
		15		45	90	
t_{PZH}, t_{PZL}	Propagation delay time 3-State Control to Data-Out	5		140	280	ns
		10		60	120	
		15		40	80	
t_{PHZ}, t_{PLZ}	Propagation delay time 3-State Control to Data-Out	5		100	200	ns
		10		50	100	
		15		40	80	
t_{PLH}	Ripple-Through Delay Input to Output	5		2	4	μs
		10		1	2	
		15		0.7	1.4	
t_{THL} t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_I	Shift-In or Shift-Out Rate	5		1.5	3	MHz
		10		3	6	
		15		4	8	
t_{WH}	Shift-In pulse width	5	200	100		ns
		10	80	40		
		15	60	30		
t_{WL}	Shift-Out pulse width	5	360	180		ns
		10	160	80		
		15	100	50		
t_r	Shift-In or Shift-Out Rise time	5			15	μs
		10			15	
		15			15	
t_f	Shift-In fall time	5			15	μs
		10			15	
		15			15	
t_f	Shift-Out fall time	5			15	μs
		10			5	
		15			5	
t_{setup}	Data setup time	5	0			ns
		10	0			
		15	0			
t_{hold}	Data hold time	5	350	175		ns
		10	150	75		
		15	120	60		

DINAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{WL}	Data-In Ready pulse width	5		260	520	ns
		10		100	200	
		15		70	140	
t_{WL}	Data-Out Ready pulse width	5		220	440	ns
		10		90	180	
		15		65	130	
t_{WH}	Master Reset pulse width	5	200	100		ns
		10	90	45		
		15	60	30		

APPLICATIONS INFORMATION

Loading Data – Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

Unloading Data – As soon as the first word has rippled to the output, DATA-OUT READY (DOR) goes high, and data can be removed by a falling edge on the SO input. This falling edge causes the DOR signal to go low while the word on the output is dumped and the next word moves to the output. As long as valid data are available in the FIFO, the DOR signal will go high again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain low, and any further commands will be ignored until a "1" marker ripples down to the last control register, when DOR goes high. Unloading of data is inhibited while the 3-state control input is high. The 3-state control signal should not be shifted from high to low (data outputs turned on) while the SHIFT-OUT is at logic 0. This level change would cause the first word to be shifted out (unloaded) immediately and the data to be lost.

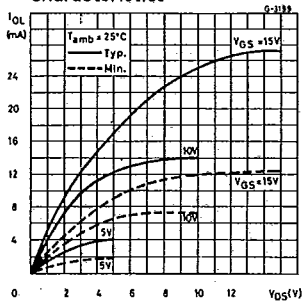
Cascading – The **HCC/HCF 40105B** can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than 4 bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions.

3-State Outputs – In order to facilitate data busing, 3-state outputs are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output.

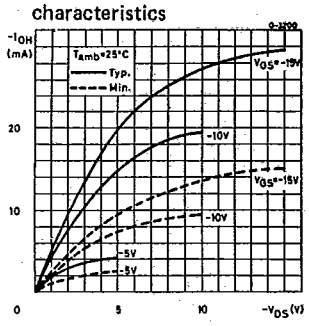
Master Reset – A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded.

HCC/HCF 40105B

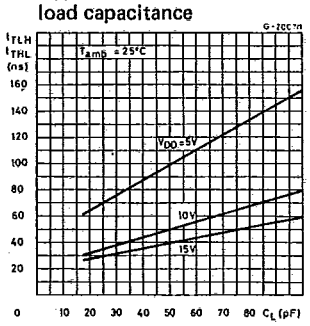
Output low (sink) current characteristics



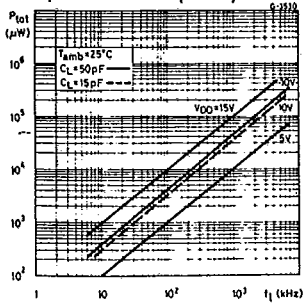
Output high (source) current characteristics

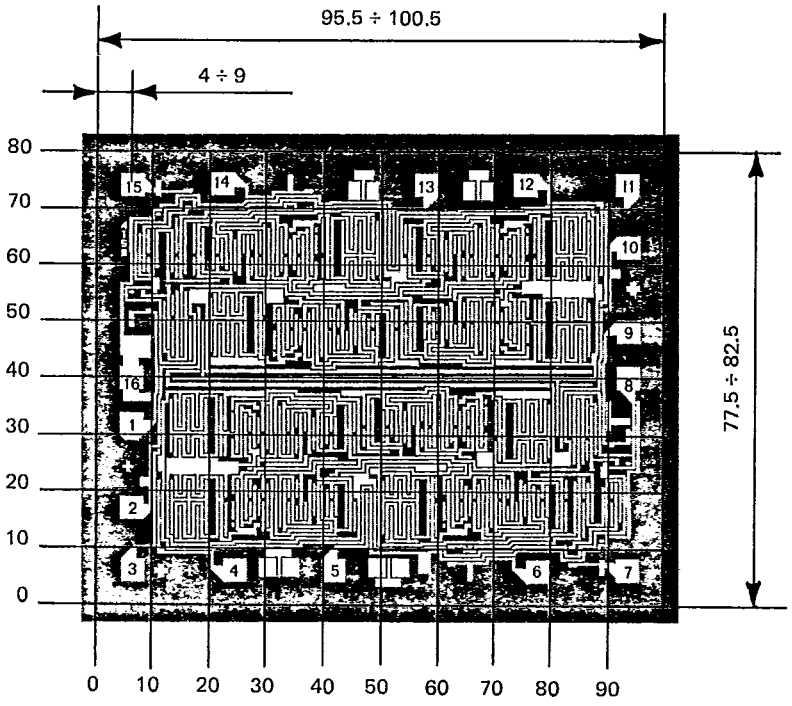


Typical transition time vs. load capacitance

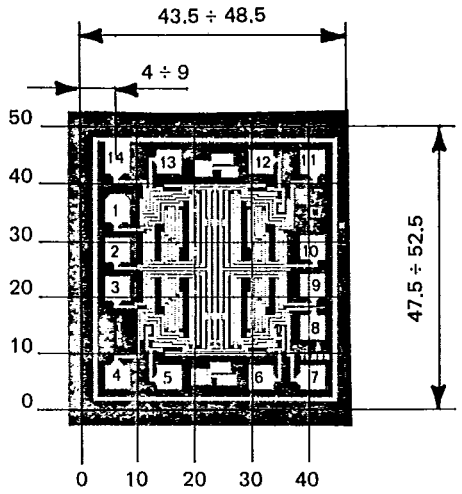


Typical dynamic power dissipation vs. frequency




95.5 ÷ 100.5
4 ÷ 9
77.5 ÷ 82.5
80
70
60
50
40
30
20
10
0
0 10 20 30 40 50 60 70 80 90
15 14 13 12 11 10 9 8 16 1 2 3 4 5 6 7

4015B


43.5 ÷ 48.5
4 ÷ 9
47.5 ÷ 52.5
50
40
30
20
10
0
0 10 20 30 40
14 13 12 11 1 2 3 10 9 8 4 5 6 7

4016B