H3108A

1024 x 8
CMOS EEPROM

HUGHES AIRCRAFT COMPANY

MICROELECTRONICS CENTER

DESCRIPTION

Hughes H3108A is a CMOS Electrically Erasable Programmable ROM (EEPROM) organized 1024 x 8. It is an improved version of the H3108, featuring both lower power dissipation and latched data and addresses during programming. Also, Chip Select (CS) now provides for significantly reduced power to unselected devices in the Program Mode.

Data modification is accomplished by first raising the power voltage, V_{DD}, to + V_{PP} and selecting the device with CS high (+5V). Then, erasing or writing is controlled with T^2L level signals to appropriate control inputs $\overline{OE}$ (Erase) and $\overline{CE}$ (Write).

All read operations are performed with V_{DD} at 5 volts. With CS at a high level, the falling edge of the Chip Enable signal ($\overline{CE}$) latches a valid address input and initiates the accessing of data. The information is enabled on the bus when Output Enable ($\overline{OE}$) is a low level.

The Chip Select (CS) input for this device is functional in all modes, allowing for chip selection in the Read, Erase, or Write modes independent of $\overline{OE}$ and $\overline{CE}$ inputs.

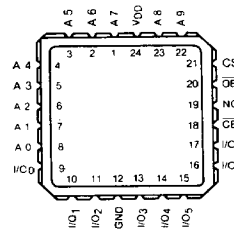
Hughes H3108A is available in a 24 lead dual-in-line ceramic package (D suffix), plastic package (P suffix), or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available on request. Commercial (HC3108A), Industrial (HI3108A), and Military (HB3108A) versions are available.

FEATURES

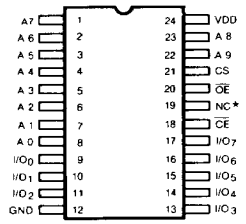
- 1K x 8 CMOS E^2PROM
- T^2L Level Chip Erase/Byte Write Controls
- 1 ms Erase/Write times
- 10,000 Erase/Write cycles (Endurance)[3]
- 10 year Data Retention[4]
- Latched Data & Addresses in Program Mode
- 3-line Control Architecture
- 10 μW Typical Quiescent Power Dissipation
- JEDEC Approved 24 pin DIP

PIN CONFIGURATIONS

Leadless Chip Carrier

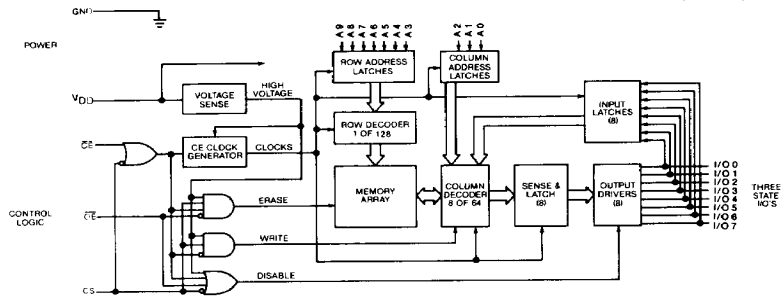


Dual-In-Line Package



*No connection to this pin allowed (internal pull-up to V_{DD}).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range . . . . . – 0.3 to + 18 Volts
(All voltage referenced to GND terminal)
Input Voltage Range. . . . . V_{SS} –0.3V to V_{DD} + 0.3V
Storage Temperature Range . . . . – 65 °C to + 150 °C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Erase/Write functions above 17 V V_{DD} will adversely affect endurance[3].

RECOMMENDED OPERATING CONDITIONS

		Read Mode	Write or Erase Mode
V_{DD} Supply Voltage		5 ± 1 Volts	16 ± 1 Volts
Temperature Range	Plastic Package	– 40 °C to + 85 °C	– 40 °C to + 85 °C
	Ceramic Package	– 55 °C to + 125 °C	– 55 °C to + 125 °C

DC OPERATING CHARACTERISTICS

Read: V_{DD} = 6 Unless Otherwise Specified

Symbol	Parameter	+25 °C Min.	+25 °C Typ.	+25 °C Max.	–40 °C to +85 °C Min.	–40 °C to +85 °C Max.	–55 °C to +125 °C Min.	–55 °C to +125 °C Max.	Units	Test Conditions
I_{DDS}	V_{DD} Standby Current	—	2	100	—	100	—	200	µA	$\overline{CE}$ = $\overline{OE}$ = 6 V, CS = 0
I_{DDA}	V_{DD} Active Current[1]	—	2	100	—	100	—	200	µA	$\overline{CE}$ = $\overline{OE}$ = 0, CS = 6 V
V_{OL}	Output Low Voltage	—	0.25	0.45	—	0.45	—	0.45	V	V_{DD} = 4.75 V, I_O = 2.1mA
V_{OH}	Output High Voltage	2.4	4.5	—	2.4	—	2.4	—	V	V_{DD} = 4.75V, $\|I_O\|$ = – 400µA
V_{IL}	Input Low Voltage	—	—	0.8	—	0.76	—	0.76	V	V_{DD} = 4.75 V
V_{IH}	Input High Voltage	3.08	—	—	3.18	—	3.18	—	V	V_{DD} = 5.25 V
I_{LI}	Input Leakage Current	—	±1	±5	—	± 10	—	± 10	µA	V_{IN} = 0 or V_{DD}
I_{LO}	Output Leakage Current	—	±1	±5	—	± 10	—	± 10	µA	V_O = 0 or V_{DD}

Erase or Write: V_{DD} = 17 V Unless Otherwise Specified

Symbol	Parameter	+25 °C Min.	+25 °C Typ.	+25 °C Max.	–40 °C to +85 °C Min.	–40 °C to +85 °C Max.	–55 °C to +125 °C Min.	–55 °C to +125 °C Max.	Units	Test Conditions
I_{DPP}	V_{DD} Program Current	—	1	3	—	5	—	5	mA	CS = 0 V
I_{DPP}	V_{DD} Program Current	—	2.5	5	—	7	—	7	mA	CS = 5 V
V_{IL}	Input Low Voltage	—	—	0.8	—	0.76	—	0.76	V	—
V_{IH}	Input High Voltage	3.08	—	—	3.18	—	3.18	—	V	—
I_{LI}	Input Leakage Current	—	±1	±5	—	± 10	—	± 10	µA	V_{IN} = 0 or V_{DD}
I_{LO}	Output Leakage Current	—	±1	±5	—	± 10	—	± 10	µA	V_O = 0 or V_{DD}

Notes:
1. This parameter is only sampled and is not 100% tested.
2. Erase and Write time is a function of + V_{PP}. See characteristic curve.
3. Endurance is the maximum number of erase/write cycles per byte.
4. Retention is the amount of time the data is retained in memory without power being supplied.

AC OPERATING CHARACTERISTICS

H3108A

Read: V_{DD} = 5 V ±5% Unless Otherwise Specified

Symbol	Parameter	T = +25°C			0°C to +70°C		−40°C to +85°C		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
t_{ASU}	Address Set Up Time	350	—	—	500	—	500	—	ns	CS = V_H
t_{AH}	Address Hold Time	150	50	—	200	—	200	—	ns	CS = V_H
t_{ACE}	Access Time from $\overline{CE}$	—	500	700	—	925	—	925	ns	CS = V_H, $\overline{OE}$ = V_L
t_{OE}	Output Enable Time	—	200	325	—	475	—	475	ns	CS = V_H, $\overline{OE}$ = V_L
t_{ACS}	Access Time from CS	-	—	500	-	700	-	700	ns	—
t_{DOE}	Time Disable to $\overline{OE}$	—	—	525	—	650	—	650	ns	$\overline{CE}$ = V_L, CS = V_H
t_{DCE}	Time Disable to $\overline{CE}$			525		650		650	ns	$\overline{OE}$ = V_L, CS = V_H
t_{DCS}	Time Disable to CS			600		750		750	ns	$\overline{OE}$ = V_L, $\overline{CE}$ = V_L
t_{CEH}	$\overline{CE}$ High Time	1.1	0.5	—	1.4	—	1.4	—	µs	—
I_{DYN}	V_{DD} Dynamic Current	—	0.5	1.0	—	1.2	—	1.2	mA	f = 100 KHz

Read Test Conditions
Output Load: C_L = 50pF
Input Levels: V_H = 3.18 Volts, V_L = 0.45 Volts

Timing Measurement Reference Levels: Input = Output = 50%

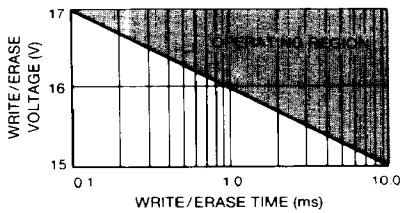
Erase and Write, V_{DD} = 16V Unless Otherwise Specified

Symbol	Parameter	T = +25°C			0°C to +70°C		−40°C to +85°C		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
t_{VPS}	Program Set Up Time[1]	5	—	—	5	—	5	—	µs	—
t_{EP}	Erase Pulse Width[2]	1	—	10	1	10	1	10	ms	CS = V_H, $\overline{CE}$ = V_H
t_{WP}	Write Pulse Width[2]	1	—	10	1	10	1	10	ms	CS = V_H, $\overline{OE}$ = V_H
t_{DS}	Data Set Up Time[1]	200	—	—	260	—	260	—	ns	CS = V_H, $\overline{OE}$ = V_H
t_{DH}	Data Hold Time[1]	750	—	—	900	—	1000	—	ns	CS = V_H, $\overline{OE}$ = V_H
t_{ASP}	Address Set Up Time[1]	350	—	—	450	—	500	—	ns	CS = V_H
t_{AHP}	Address Hold Time[1]	200	—	—	260	—	260	—	ns	CS = V_H
t_{CSP}	CS Set Up Time Program	500	—	—	625	—	700	—	ns	—

Programming Test Conditions
Input Levels: V_H = 3.18 Volts, V_L = 0.45 Volts

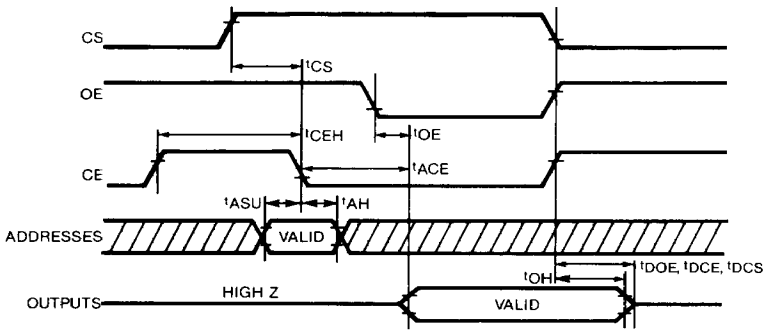
Timing Measurement Reference Levels: Input = Output = 50%

PROGRAM TIME VS. SUPPLY VOLTAGE

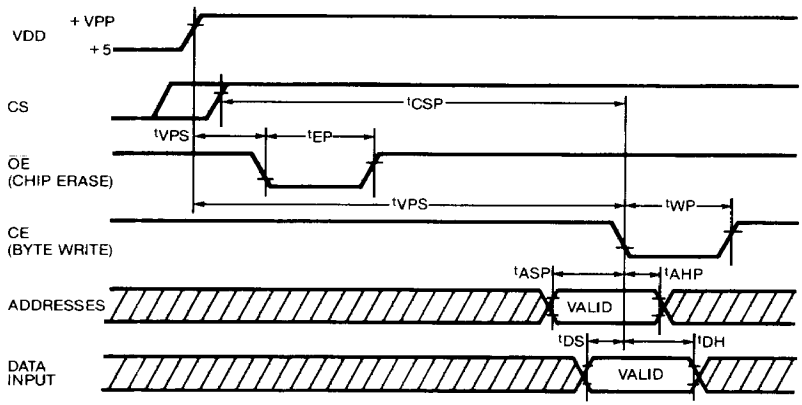


TIMING DIAGRAM

READ



CHIP ERASE / BYTE WRITE



OPERATING MODES

The H3108A has three modes of operation: Read, Chip Erase and Byte Write, all enabled when the chip is selected (CS = high). In the Read Mode the H3108A functions as a normal CMOS ROM. When the power input (V_{DD}) is raised to +V_{PP} the Erase or Write Mode is enabled. In the Erase Mode, all bytes are reset to a logic low (GND). In the Write Mode, bits of the addressed byte may be programmed to a logic high. An Erase Operation is required before re-writing over previously Programmed data. Detailed procedures for each mode follow:

READ MODE: The circuit reads addresses on the falling edge of $\overline{CE}$ and latches the accessed data until $\overline{CE}$ goes high again. The latched data will appear at the outputs whenever $\overline{CE}$ is low, CS is high, and $\overline{OE}$ is low.

ERASE MODE: A Chip Erase (all 0's in memory) is accomplished by setting $\overline{CE}$ and $\overline{OE}$ high, raising the positive supply to + V_{PP} and then pulsing $\overline{OE}$ low. When the circuit internally senses the +V_{PP} voltage, it floats the outputs preventing + V_{PP} level signals from appearing on the data I/O bus.

WRITE MODE: A Write consists of programming 1's into bits that contain a 0. A byte is written by setting $\overline{CE}$ and $\overline{OE}$ high, raising the positive supply to + V_{PP}, and pulsing $\overline{CE}$ low. The address and data lines must be valid when $\overline{CE}$ falls. Data and addresses are latched while $\overline{CE}$ is low. A Write operation can follow an Erase while holding +V_{DD} at +V_{PP}, and several or all the bytes can be programmed with +V_{DD} held at +V_{PP}.

SUMMARY OF OPERATING MODES

Logic 1 = High, Logic 0 = Low, X = Do not care

STATE	$\overline{CE}$	CS	$\overline{OE}$	V_{DD}	I/O BUS
Standby (unselected)*	X	0	X	+5 or +V_{PP}	Floating
Standby (selected)*	1	1	1	+5 or +V_{PP}	Floating
Standby (selected)	1	1	0	+5	Floating
Read	0	1	1	+5	Floating
Read	0	1	0	+5	Data Output
Erase	1	1	0	+V_{PP}	Floating
Write	0	1	1	+V_{PP}	Data Input
Prohibited State	0	1	0	+V_{PP}	Data Input

* Recommended modes for V_{DD} transition to and from +V_{PP}. V_{DD} should not fall below input levels during transition.

PIN DESCRIPTIONS

A 0 - A 9: Address inputs which select one of 1024 bytes of memory for either Read or Program. The addresses need to be valid during the falling edge of $\overline{CE}$.

I/O_0 - I/O_7: Bidirectional three-state data lines that are Data outputs during a Read operation and Data inputs during a Write operation.

GND: Negative supply terminal and V = 0 reference.

V_{DD}: Positive supply terminal. It is raised to + V_{PP} for Erase and Write operations.

CS: Chip Select. A Logic Low disables all control inputs in all modes.

$\overline{OE}$: Output Enable. A Logic High disables the Data Output Drivers in normal operation. If V_{DD} = + VPP, a Logic Low causes a chip erase. This input is active only when CS is high.

$\overline{CE}$: Chip Enable. A Logic Low at this input latches the input address during a Read operation and latches both addresses and data inputs during a Write operation. For the Read operation, accessed data is latched and valid as long as $\overline{CE}$ is held at a Logic Low. If V_{DD} = + V_{PP}, a Logic Low causes a byte Write operation. This input is active only when CS is high.