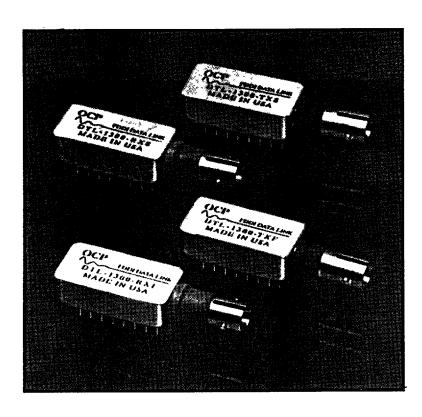
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Preliminary



DTL-1300-F/S

Data Link Modules for FDDI



Feat	ures
	Full FDDI Compliance
	High Temperature and SAFENET Applications
	Minimum of 18 dB Link Budget
	Wide Receiver Dynamic Range, 25 dB minimum
	LED Disable Control Input
	Integral ST™ Optical Connector
	Single Supply Voltage (+5 V or -5.2 V)
	Standard 16 Pin Footprint
	Dual-in-Line Hermetically Sealed Metal Package
	-40°C to +110°C Case Temperature Range

Descriptions

The DTL-1300-F/S Fiber Optic Transmitter and Receiver Data Link is designed to meet or exceed all the requirements of the Physical Layer Medium Dependent (PMD) specification for the Fiber Distributed Data Interface (FDDI) over an extremely wide temperature range from -40°C to +110°C. Highly reliable 1300 nm surface-emitting LEDs selected for proper rise/fall time, center wavelength and spectral width are utilized in the transmitters. The receivers incorporate an InGaAs/InP PIN photodiode and a high speed transimpedance amplifier to exceed the sensitivity

and dynamic range requirements of FDDI. The receiver post-amplifier features the specified Signal Detect function and differential emitter coupled logic (ECL) outputs. Both the transmitter and receiver are housed in a 16-pin dual-in-line hermetically sealed metal package with integral ST™ connector and operate on standard +5 volt or -5.2 volt power supply.

The DTL-1300-S modules are designed for use with 62.5/125 μ m fiber. The DTL-1300-F modules are designed for use with 100/140 μ m fiber.

Optical Communication Products, Inc.

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Absolute Maximum Ratings

Parameter	DTL-	1300-F	DTL-	Units	
	Minimum	Maximum	Minimum	Maximum	00
Storage Temperature	- 55	+110	- 55	+110	°C
Operating Temperature	- 40	+110	0	+ 85	.€
Supply Voltage	0	+6.0	0	+6.0	V
Input Voltage	0	+6.0	0	+6.0	V
Lead Soldering	-	240°C, 10 sec	-	240°C, 10 sec	_

Transmitter Electrical Interface

Parameter		Symbol	Minimum	Typical	Maximum	Units	
Supply Voltage	+5 V	Vcc	4.5	5.0	5.5	٧	
oupply voilage	-5.2 V	VEE	- 5.5	- 5.2	- 4.5	V	
Supply Current		1	-	130	160	mA	
Power Dissipation		Р	•	650	900	mW	
Input HIGH Voltage (Data/Data)		VIHS	Vcc - 1.15	+	Vcc - 0.73	V	
Input LOW Voltage (Data/Data)		VILS	Vcc - 1.87	-	Vcc - 1.45	V	
Differential Input Voltage		V _{DIF}	0.3	- 1.1		V	
Input Common Mode Voltage ¹		VICM	-	-	1.0	V	
Reference Voltage	V _{BB}	V _{CC} - 1.39	V _{CC} - 1.29	V _{CC} - 1.17	V		
1 Permissible ± V _{ICM} w	ith respect to V _{BB}	·	4		I		

Receiver Electrical Interface

Paramet	Symbol	Minimum	Typical	Maximum	Units		
Supply Voltage	+5 V	Vcc	4.5	5.0	5.5	V	
——————————————————————————————————————	- 5.2 V	VEE	- 5.5	- 5.2	- 4.5	٧	
Supply Current	1	-	80	100	mA		
Power Dissipation	Р	-	400	550	mW		
Output HIGH Voltage		VoH	Vcc - 1.035	-	Vcc - 0.88	٧	
Output LOW Voltage		VoL	Vcc - 1.83	-	V _{CC} - 1.62	V	

Transmitter Operation

The transmitter behaves logically as a differential input gate which controls a 1300 nm LED. When the DATA input voltage is greater than the DATA input voltage, the LED is ON; and vice versa. For single-ended applications, the unused input pin

should be connected to VBB . The DISABLE control input turns the LED off when forced to ECL logic "high" independent of the input data. For normal operation, the DISABLE input should be left open or forced to ECL logic "low".

Transmitter Performance (Over Specified Operating Temperature Range)

Symbol	DTL-1300-F			DTL-1300-S			Units
- Cymber	Min	Тур	Max	Min	Тур	Max	Ormo
В	DC	125	160	DC	125	160	Mb/s
Po	- 15.7	- 12.0	- 9.0	- 16.0	- 12.0	- 9.0	dBm
λο	1270	1320	1380	1270	1320	1380	nm
tr & tr	0.6	-	3.5	0.6	-	2.7	ns
RJ	0	-	0.7	0	-	0.7	ns
DCD	0	-	0.6	0	-	0.6	ns
DDJ	0	-	0.6	0	-	0.6	ns
-	-	-	10	-	-	10	%
Poff	-	-	- 50			- 50	dBm
Δλ	-	130	160	-	130	160	nm
	P̄ _o λ _c t _r & t _f RJ DCD DDJ - Poff	Min B DC Po -15.7 λc 1270 tr & tr 0.6 RJ 0 DDJ 0 DDJ 0 C Poff -	Min Typ B DC 125 P̄o -15.7 -12.0 λc 1270 1320 t _r & t _f 0.6 - RJ 0 - DCD 0 - DDJ 0 - Poff - -	Min Typ Max B DC 125 160 Po -15.7 -12.0 -9.0 λc 1270 1320 1380 tr & tr 0.6 - 3.5 RJ 0 - 0.7 DCD 0 - 0.6 DDJ 0 - 0.6 - - 10 - Poff - - -50	Min Typ Max Min B DC 125 160 DC P̄₀ -15.7 -12.0 -9.0 -16.0 λ̄₀ 1270 1320 1380 1270 tr & tf 0.6 - 3.5 0.6 RJ 0 - 0.7 0 DCD 0 - 0.6 0 DDJ 0 - 0.6 0 - - - 10 - Poff - - - -	Min Typ Max Min Typ B DC 125 160 DC 125 P̄₀ -15.7 -12.0 -9.0 -16.0 -12.0 λ̄₀ 1270 1320 1380 1270 1320 tr & tf 0.6 - 3.5 0.6 - RJ 0 - 0.7 0 - DCD 0 - 0.6 0 - DDJ 0 - 0.6 0 - - - - 10 - - Poff - - - - -	Symbol Min Typ Max Min Typ Max B DC 125 160 DC 125 160 Po -15.7 -12.0 -9.0 -16.0 -12.0 -9.0 λc 1270 1320 1380 1270 1320 1380 tr & tf 0.6 - 3.5 0.6 - 2.7 RJ 0 - 0.7 0 - 0.7 DCD 0 - 0.6 0 - 0.6 DDJ 0 - 0.6 0 - 0.6 - - - 10 - - 10 Poff - - - - - - -

Measured with 100/140 μ m fiber for DTL-1300-F and 62.5/125 μ m fiber for DTL-1300-S.

Receiver Performance (Over Specified Operating Temperature Range)

							<u> </u>		
Parameter		Symbol	DTL-1300-F			DTL-1300-S			Units
			Min	Тур	Max	Min	Тур	Max	
Data Rate		В	1	125	160	1	125	160	Mb/s
Optical Input Power ¹ (BER = 2.5 x 10 ⁻¹⁰)	FDDI Test ²	- P _{in}	- 34.0	-	- 9.0	- 35.0	-	- 9.0	dBm
	Sensitivity ³	T IN	- 35.5	-		- 36.5	-		
Signal Detect	Assertion	P _{sd}	•	-	- 34.0	- '	-	- 35.0 -	dBm
Thresholds ¹	Deassertion		- 45.0	-	-	- 45.0	-		
Signal Detect Hysteresis ¹			1.5	-	-	1.5	-	-	dB
Signal Detect Timing	Assertion	T _{sd}	•	én	100	-	-	50	
olgital Detect Hilling	Deassertion	i su	-	-	350	-	-	50	μs
Wavelength of Operation		λ	1100	1320	1600	1100	1320	1600	nm
Output Duty Cycle Distortion (p-p)		DCD	-	•	0.4	-	-	0.4	ns

 $^{^{1}}$ Measured with 100/140 μm fiber for DTL-1300-F and 62.5/125 μm fiber for DTL-1300-S. 2 FDDI Test Conditions.

² Center wavelength, spectral width, and rise/fall time are compliant with Figure 5.1 of the FDDI PMD.

When tested with 2⁷-1 PRBS at 125 Mbaud, input optical rise/fall time of 2.5 nsec at 1300 nm wavelength, and optimum sampling point.

Receiver Operation

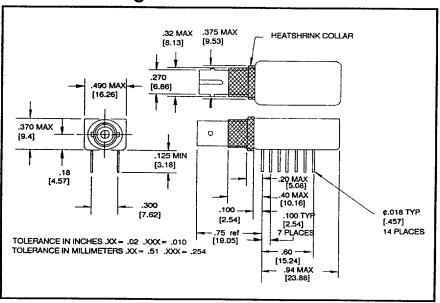
The receiver converts the incident optical power to a photocurrent using a high performance PIN photodiode. The photocurrent is converted to a analog voltage by a transimpedance amplifier. This analog signal is then amplified by additional gain stages and processed through a shaping filter and a comparator to generate the differential ECL output signals. Both outputs (DATA and \overline{DATA}) are open emitters requiring termination to VCC -2 volts with 50 Ω or to VEE with 510 Ω . For optimum performance both outputs should be terminated identically, even if only one output is used.

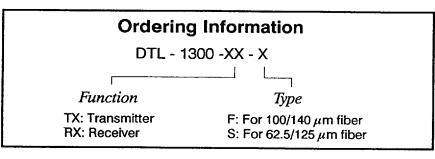
The Signal Detect circuit monitors the level of incoming optical signal and generates a logic LOW

signal when insufficient photocurrent is produced to ensure proper operation. The Signal Detect can be used to control an external squelch circuit to gate off spurious outputs generated by the receiver when no optical input is available. The outputs are open emitter ECL requiring termination (510 $\,\Omega$ to VEE is recommended).

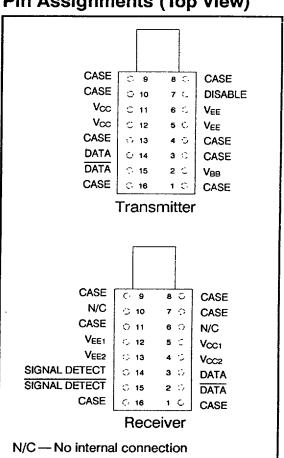
Special care should be taken with the receiver PCB layout. A solid ground plane and low impedance, well-bypassed power supply traces are highly recommended. If the receiver outputs drive long traces or multiple loads, the use of an ECL buffer gate to isolate the receiver from transmission line reflections is recommended.

Outline Drawing





Pin Assignments (Top View)



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