# 8-BIT 200KSPS ADC AL1209H

## GENERAL DESCRIPTION

The AL1209H is a CMOS 8-bit A/D converter for micom applications. It is a SAR (Successive Approximation Register) A/D converter which consists of SAR, R_string DAC, 11bit resolution comparator and output register buffer.
The maximum conversion rate of AL1209H is 200KSPS and supply voltage is 5V single.

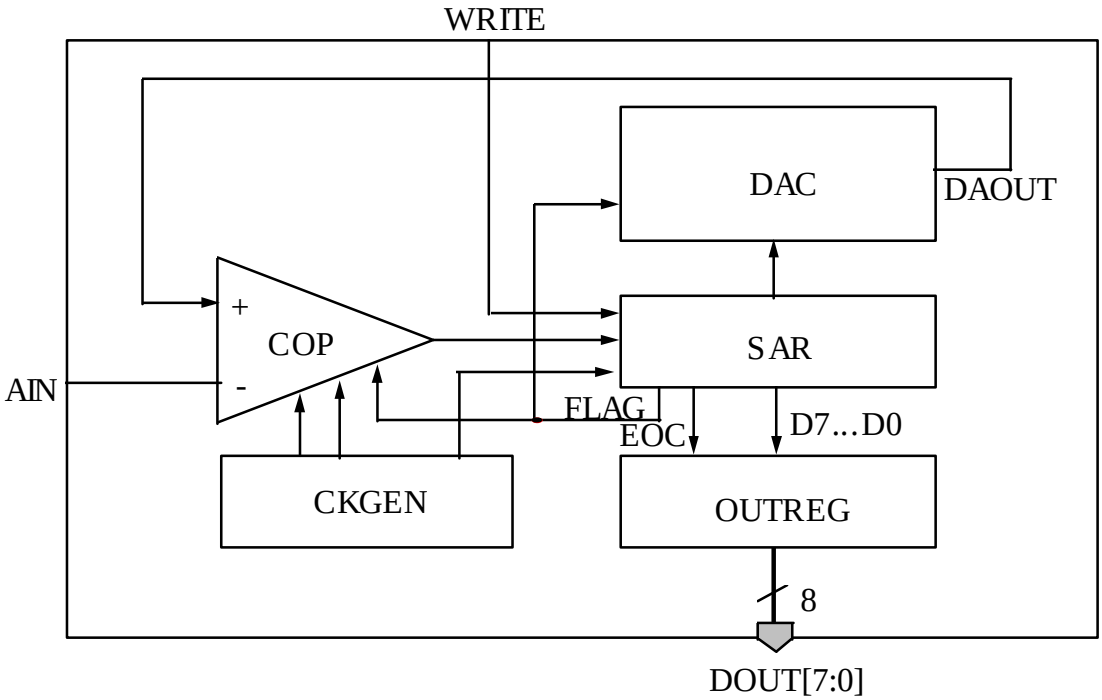
## FEATURES

- **Resolution : 8-bit**
- **Differential Linearity Error : ±0.3 LSB(typ)**
- **Integral Linearity Error : ±0.5 LSB(typ)**
- **Maximum Conversion Rate : 200KSPS**
- **Low Power Consumption : 4mW(typ.)**
- **Power Supply : 5V Single**

## TYPICAL APPLICATIONS

- MICOM
- Battery Charger
- Game Pack
- Digital Still Camera
- Other Low power equipments.

## FUNCTIONAL BLOCK DIAGRAM



## CORE PIN DESCRIPTION

| NAME | I/O TYPE | I/O PAD | PIN DESCRIPTION |
|---|---|---|---|
| REFP | AI | pia_bb | Internal Reference Top Bias. +5.0V |
| REFN | AI | pia_bb | Internal Reference Bottom Bias |
| VDDA | AP | vdda | Analog Power (+5.0V) |
| VSSA | AG | vssa | Analog Ground |
| AIN | AI | pia_bb | Analog Input<br>Input Span : REFN ~ REFP |
| CLK | DI | pic_bb | Clock Input |
| DOUT[7:0] | DO | pic_bb | Digital Output |
| WRITE | DI | pic_bb | A/D Conversion Start Signal |
| STOP | DI | pic_bb | Power Down |
| RESET | DI | pic_bb | System Reset |
| VBB | AG/DG | vbba | Analog/Digital Sub Bias |
| VSS | DG | vsst | Digital Ground |
| VDD | DP | vdd5t | Digital Power (+5.0V) |

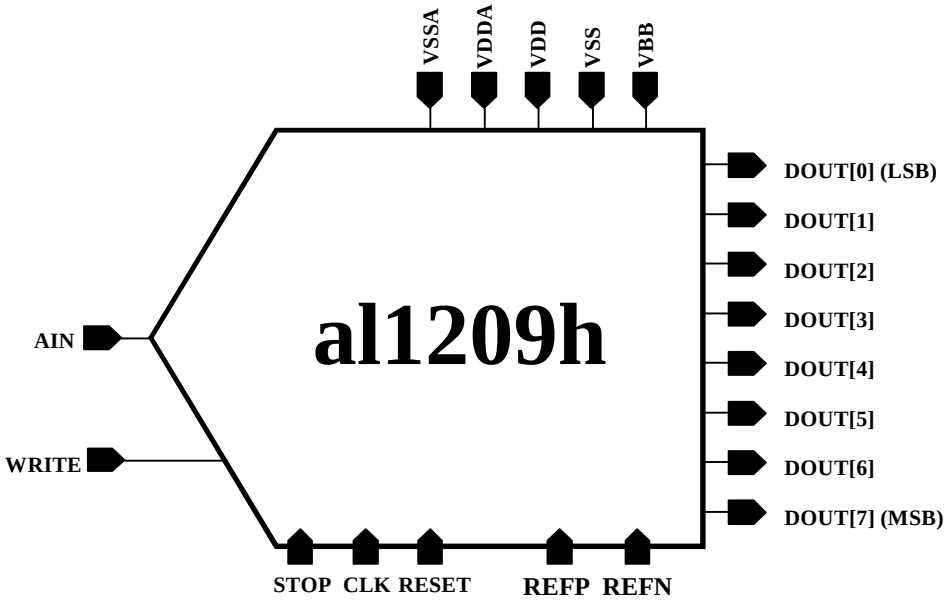
**I/O TYPE ABBR.**

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output

- AP : Analog Power
- AG : Analog Ground
- DP : Digital Power
- DG : Digital Ground

- AB : Analog Bidirection
- DB : Digital Bidirection

## CORE CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | VDD | 5.0 | V |
| Analog Input Voltage | AIN | REFN to REFP | V |
| Digital Input Voltage | CLK | VSS to VDD | V |
| Digital Output Voltage | $V_{OH}$, $V_{OL}$ | VSS to VDD | V |
| Reference Voltage | REFN/REFP | VSS to VDD | V |
| Storage Temperature Range | Tstg | -45 to 150 | °C |
| Operating Temperature Range | Topr | 0 to 70 | °C |

NOTES

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

## RECOMMENDED OPERATING CONDITIONS

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | VDDA - VSSA<br>VDD - VSS | 4.75 | 5.0 | 5.25 | V |
| Supply Voltage Difference | VDDA - VDD | -0.1 | 0.0 | 0.1 | V |
| Reference Input Voltage | REFP<br>REFN | -<br>- | VDD<br>VSS | -<br>- | V |
| Analog Input Voltage | AIN | REFN | - | REFP | V |
| Clock High Time<br>Clock Low Time | Tpwh<br>Tpwl | -<br>- | 49<br>49 | -<br>- | ns |
| Digital Input 'L' Voltage<br>Digital Input 'H' Voltage | $V_{IL}$<br>$V_{IH}$ | -<br>4.5 | -<br>- | 0.5<br>- | V |
| Operating Temperature | Topr | 0 | - | 70 | °C |

NOTES

1. It is strongly recommended that all the supply pins (VDDA, VDD) be powered from the same source to avoid power latch-up.

## DC ELECTRICAL CHARACTERISTICS

| Characteristics | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Resolution | - | - | 8 | - | bits | |
| Reference Current | IREF | - | 195 | 220 | uA | REFP : 5.0V<br>REFN : 0.0V |
| Differential Linearity Error | DLE | - | ±0.3 | ±0.5 | LSB | AIN : REFN ~ REFP<br>(Ramp Input) |
| Integral Linearity Error | ILE | - | ±0.5 | ±1.0 | LSB | Fck : 2KHz<br>12MHz |
| Bottom Offset Voltage Error | EOB | - | 6 | 19.5 | mV | EOB = AIN(0,1) - REFN |
| Top Offset Voltage Error | EOT | - | 19.5 | 39 | mV | EOT = REFP - AIN(254,255) |

NOTES

1. Converter Specifications (unless otherwise specified)
   VDDA=5.0V VDD=5.0V
   VSSA=GND VSS=GND VBB=GND
   REFP=5.0V REFN=0.0V
   Ta=25 °C
2. TBD : To Be Determined
3. Because of inserting the power down mode, EOT is over 1-LSB. If you don't use, REFP can be located at dot-line and EOT is the same as EOB. See fig1.

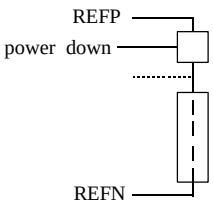


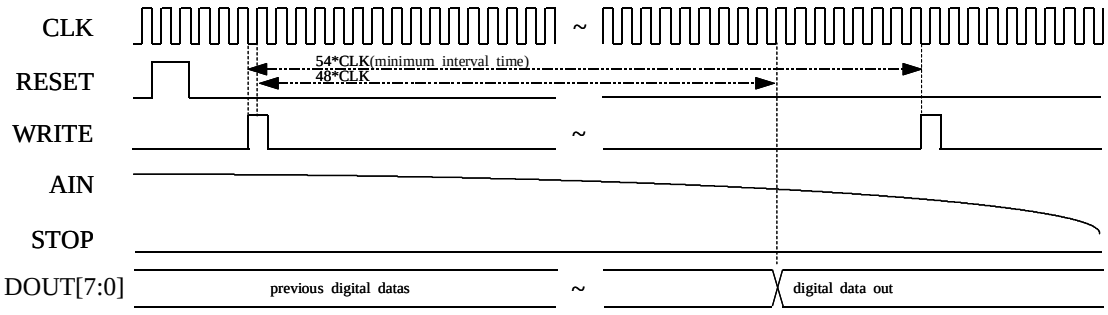
fig1.

## AC ELECTRICAL CHARACTERISTICS

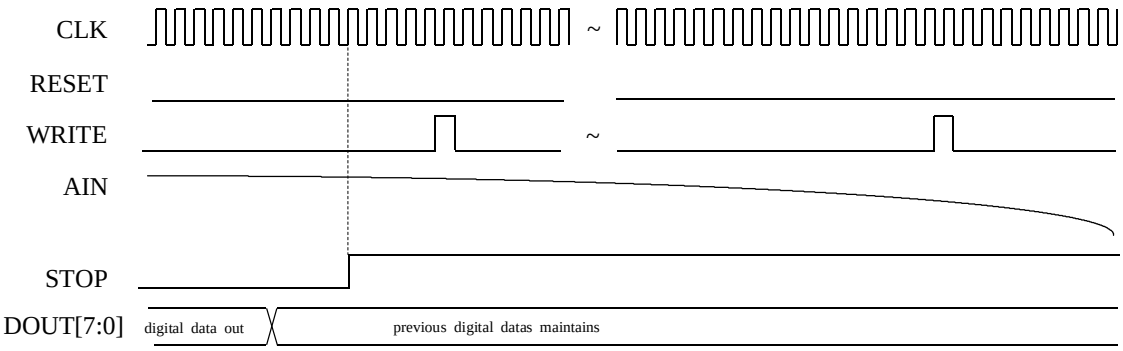
| Characteristics | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Clock High Time | Tpwh | - | 49 | - | ns | AIN : 1, 4KHz<br>(Sine Input) |
| Clock Low Time | Tpwl | - | 49 | - | ns | |
| Conversion Rate | Fs | - | 200 | 300 | KSPS | fCK=12MHz. |
| Dynamic Supply Current | Is | - | 0.8 | 1.2 | mA | about the CORE |
| | | - | 1.9 | 2 | mA | output load=50pF, testpins are not envolved. |
| | | - | 5.1 | 5.8 | mA | output load=50pF, testpins are envolved. |
| | | 100 | - | - | nA | Power Down Mode |
| Power Dissipation | PD | - | 4 | 6.5 | mW | at A/D operating. about the CORE |
| | | 500 | - | - | nW | Power Down Mode. about the CORE |

## TIMING DIAGRAM

1. A/D operation




2. at STOP mode.



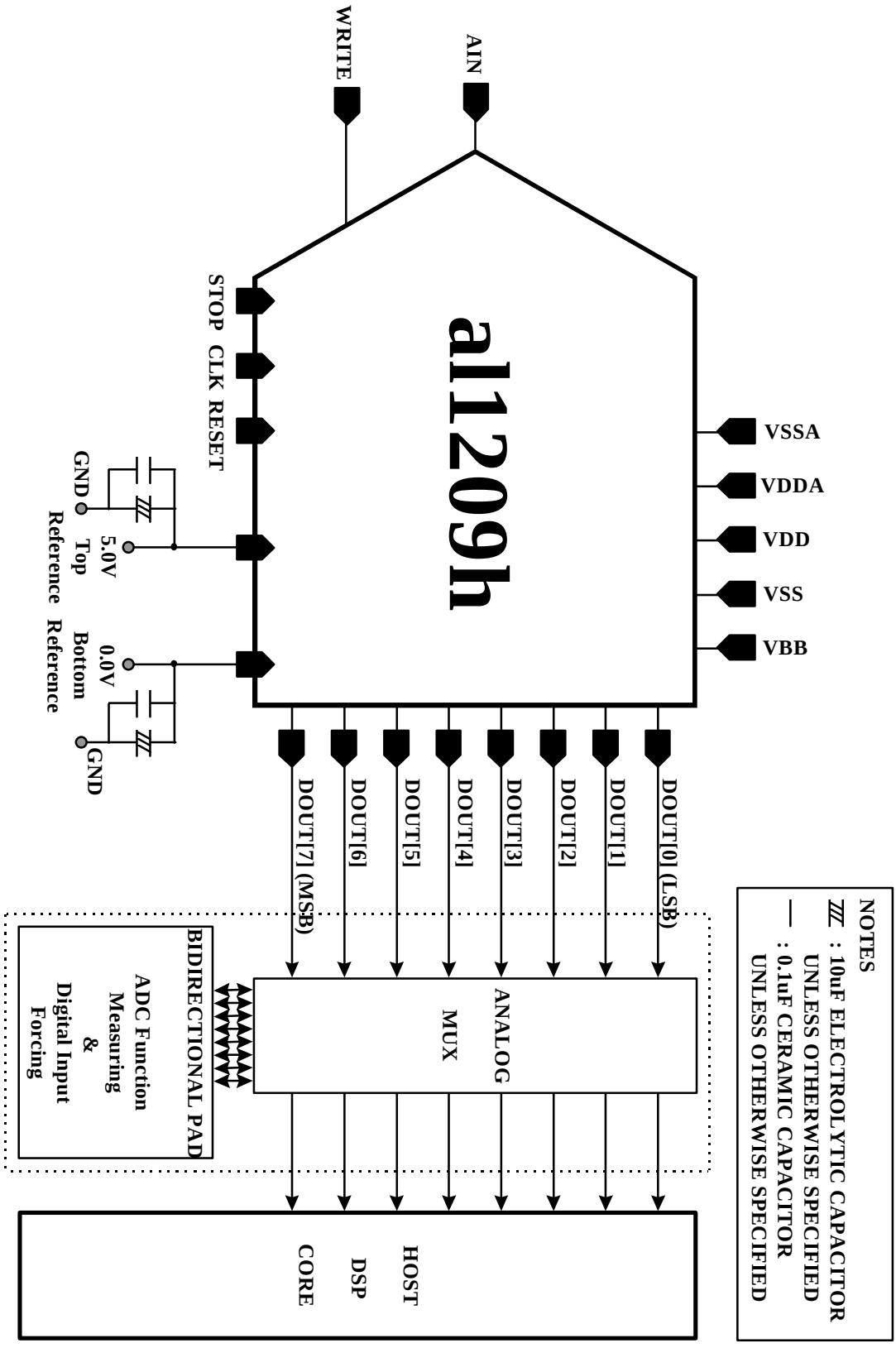
## FUNCTIONAL DESCRIPTION

1. AL1209H is a SAR(Successive Approximation Register)-Type A/D converter. The ADC is composed of Offset-Auto-Calibration comparators, and R-string DAC for generation of $2^8$ Analog Level, and Clock Generator to devide with internal clocks from 12MHz CPU clock, SAR and Output Buffer Registers.

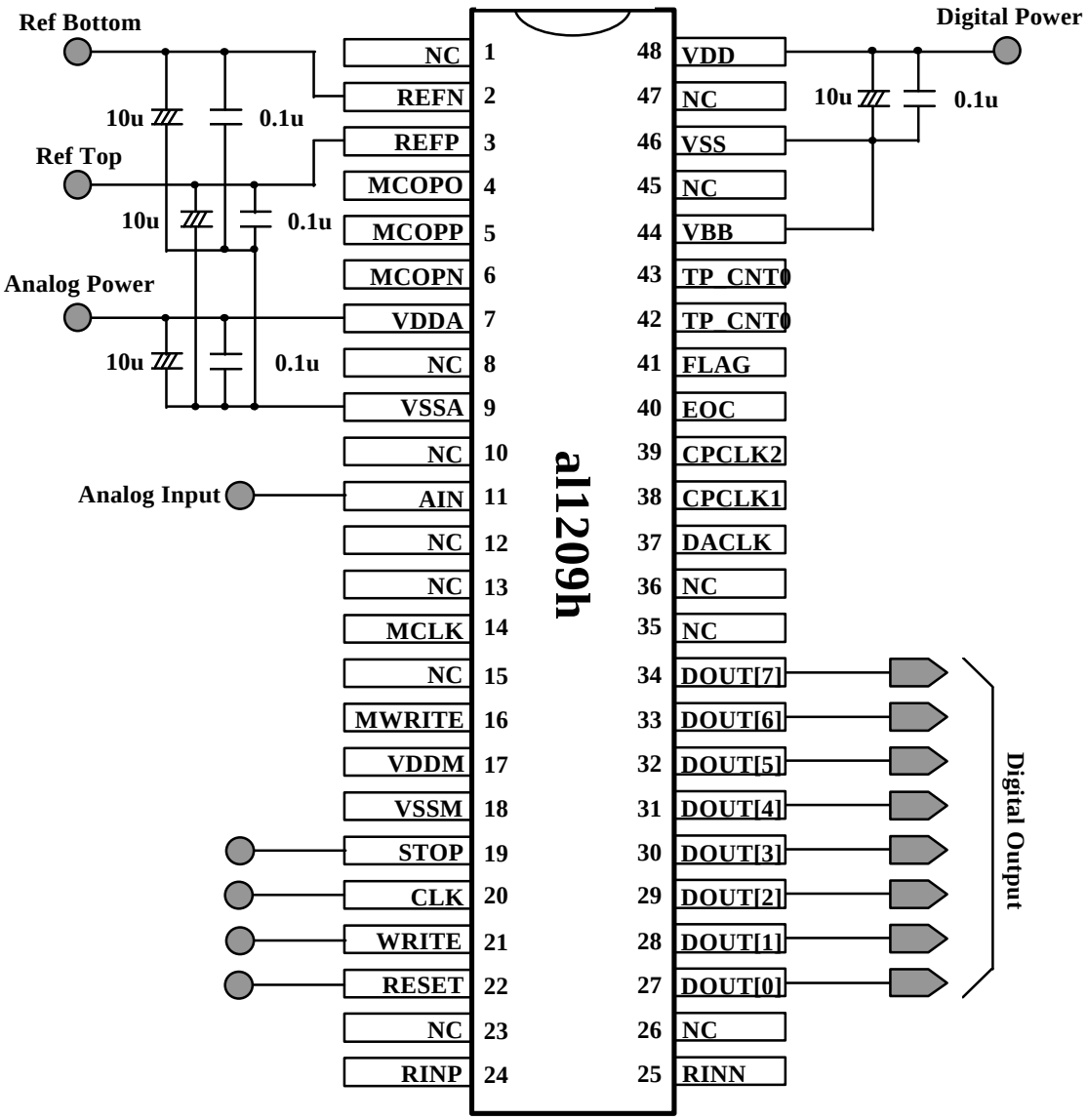
2. AL1209H operates as follows. When Main system clock 12MHz is supplied to operate ADC, The WRITE signal, A/D conversion enable signal, is supplied main clock's falling edge with 1-clock period as active HIGH and it come down to Low state the FLAG, and CKGEN generate the internal clocks, DACLK, CPCLK1, CPCLK2. The 1-period of DACLK is 1BIT A/D conversion time. After 8BIT A/D conversion is completed, the EOC clock is pulsed and the FLAG state comes to HIGH. This is the A/D conversion DATA capture region.

## CORE EVALUATION GUIDE

1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.
2. The reference voltages may be biased externally through REFN and REFP pins



## PACKAGE CONFIGURATION




**NOTES**
**: 10uF ELECTROLYTIC CAPACITOR UNLESS OTHERWISE SPECIFIED**
**: 0.1uF CERAMIC CAPACITOR UNLESS OTHERWISE SPECIFIED**

NOTES

1. You can test ADC function by checking external bidirectional pad connected to internal signal path.
2. ESD (ElectroStatic Discharge) sensitive device. Although the digital control inputs are diode protected, permanent damage may occur on devices subjected to high electrostatic discharges. It is recommended that unused devices be stored in conductive foam or shunts to avoid performance degradation or loss of functionality. The protective foam should be discharged to the destination socket before devices are inserted.
3. NC denotes "No Connection".

## PACKAGE PIN DESCRIPTION

| NAME | PIN NO. | I/O TYPE | PIN DESCRIPTION |
|---|---|---|---|
| REFN | 2 | AI | 0.0V External Reference Bottom Bias. |
| REFP | 3 | AI | Internal Reference Top Bias. +5.0V<br>(Short to VRTS for Self-Bias.) |
| VDDA | 7 | AP | +5.0V Analog Power. |
| VSSA | 9 | AG | Analog Ground. |
| AIN | 11 | AI | Analog Input.<br>Input Span = REFN - REFP |
| STOP | 19 | DI | Power Down |
| CLK | 20 | DI | Clock Input. |
| WRITE | 21 | DI | A/D Conversion Start Signal |
| RESET | 22 | DI | Reset |
| DOUT[0:7] | 27~34 | DO | Digital Output. |
| VBB | 44 | AG/DG | Analog/Digital Sub Bias. |
| VSS | 46 | DG | Digital Ground. |
| VDD | 48 | DP | Digital Power. |
| pin# 4,5,6,14,16,17,18,24,25,37,38,39,40,41,42,43 | | | **Testpins.** |

NOTES

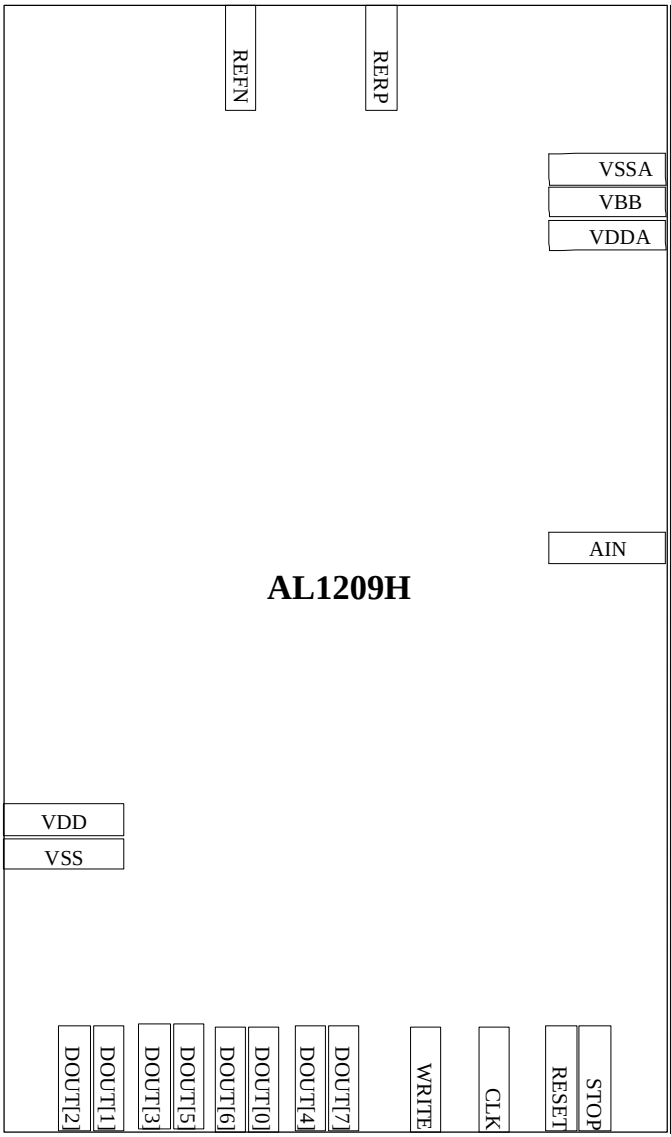
1. Speed Up
   - The Conversion Rate of AL1209H is 200KSPS, but it proved to operates well at 300KSPS or more because of a lot of design margin.

2. Input Range Variation.
   -The analog input voltage (AIN) of this ADC is single. The default range is from REFN to REFP. Therefore, if you want to change the AIN range, it should be changed the values of REFN and REFP.
   The minimum range is 2.5V.

3. Note that this ADC has not the sample and hold circuit. Therefore during the A/D conversion, the analog input voltage variation should be less than 1 LSB.

## PHANTOM CELL INFORMATION

- Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
  The term "External" implies that the pins should be assigned externally like power pins.
  The term "External/internal" implies that the applications of these pins depend on the user.




| Pin Name | Pin Usage | Pin Layout Guide |
|---|---|---|
| VDDA | External | - Do not merge the analog powers with another power from other blocks.<br>- Use good power and ground source on board. |
| VSSA | External | |
| VBB | External | |
| VDD | External | |
| VSS | External | |
| AIN | External/Internal | - Do not overlap with digital lines.<br>- Maintain the shortest path to pads. |
| REFP | External | - Maintain the larger width and the shorter length as far as the pads.<br>- Separate from all other digital lines. |
| REFN | External | |
| CLK | External/Internal | - Separate from all other analog signals |
| STOP | External/Internal | |
| RESET | External/Internal | |
| WRITE | External/Internal | |
| DOOT[7] | External/Internal | - Separated from the analog clean signals if possible. |
| DOUT[6] | External/Internal | |
| DOUT[5] | External/Internal | |
| DOUT[4] | External/Internal | |
| DOUT[3] | External/Internal | |
| DOUT[2] | External/Internal | |
| DOUT[1] | External/Internal | |
| DOUT[0] | External/Internal | |

## FEEDBACK REQUEST

It should be quite helpful to our ADC core development if you specify your system requirements on ADC in the following characteristic cheking table and fill out the additional questions.
We appreciate your interest in our products. Thank you very much.

| Characteristic | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|
| Analog Power Supply Voltage | | | | V | |
| Digital Power Supply Voltage | | | | V | |
| Bit Resolution | | | | bit | |
| Reference Input Voltage | | | | V | |
| Analog Input Voltage | | | | Vpp | |
| Operating Temperature | | | | °C | |
| Integral Non-linearity Error | | | | LSB | |
| Differential Non-linearity Error | | | | LSB | |
| Bottom Offset Voltage Error | | | | mV | |
| Top Offset Voltage Error | | | | mV | |
| Maximum Conversion Rate | | | | MSPS | |
| Dynamic Supply Current | | | | mA | |
| Power Dissipation | | | | mW | |
| Digital Output Format (Provide detailed description & timing diagram) | | | | | |

1. Between single input-output and differential input-output configurations, which one is suitable for your system and why?

2. Please comment on the internal/external pin configurations you want our ADC to have, if you have any reason to prefer some type of configuration.

3. Freely list those functions you want to be implemented in our ADC, if you have any.

## HISTORY CARD

| Version | Date | Modified Items | Comments |
|---|---|---|---|
| ver 1.0 | | Original version published (preliminary) | |
| ver 1.1 | | | |
| ver 1.2 | 1999.10 | Release the formal datasheet | |
| ver 1.3 | 02.04.27 | Add the phantom cell information | |
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