MINGSTAR ELECTRONIC CORPORATION

Spec. No.	233-220-053

Version : 0
Total pages: 21
Date : 1998/07/20

TFT-LCD CONTROLLER LSI (UPS015)
PRELIMINARY SPECIFICATION

MODEL NAME: UPS015

The content of this technical information is subject to change without notice. Please contact Mingstar or its agent for further information.

Approved by	Checked by	Prepared by
T. P. Chiang	H. Y. Chou 7.22.'98	Asir Chang

Contents:

A.General description:

This timing controller is a synchronizing signal controlling CMOS array LSI for Mingstar LCD module. It provides all the necessary control timing signals to the LCD source and gate drivers. With external VCO as the master clock, the controller has built-in phase locked loop system which can synchronize the master clock with the horizontal and vertical Sync. signals from a classical TV system.
The applicable Mingstar TFT-LCD modules are SM261D series, MTL020D01,MTL025D01, MTL040D01 , MTL068D01, MTL070W01.

B. Feature:

* Programmable resolution mode.
* Low Power Consumption.
* Single Supply : +5.0 Volts.
* 48 pins TQFP.
* Shift Clocks Signal for the Source Driver. (3 - ϕClock)
* Line Inversion Driving Scheme.
* NTSC TV Standard System .
* Master Clock Frequency : 26 MHz max.
* Provides Timing Scan Signals for Left / Right and Up / Down Shift Control.
* Display Timing Range = 49.6μs

C.Pin description:

Pin no	Symbol	I/O	Description	Remark
1	INV/O	O	Inverter output	
2	INV/I	I	Inverter input	
3	OEH	O	Output enable control signal for source driver	
4	OEV	O	Output enable control signal for source driver	
5	TEST			Note 1
6	TEST			Note 1
7	GND		Ground	
8	Q1HA	O	Sample & hold sequence control signal for source driver	
9	A18	I	Resolution mode selecting pin I	Note 2
10	STV1	O	Gate driver start pulse. when (1).UDC=H, STV1 is output pin of start pulse. (2).UDC=L, STV1 is in high impedance state.	
11	STV2	O	Gate driver start pulse. when (1).UDC=H, STV2 is in high impedance state. (2).UDC=L, STV2 is output pin of start pulse.	
12	VCC			
13	STHL	O	Source driver start pulse. when (1).LRC=H, STHL is in high impedance state. (2).LRC=L, STHL is output pin of start pulse.	
14	STHR	O	Source driver start pulse. when (1).LRC=H, STHR is output pin of start pulse. (2).LRC=L, STHR is in high impedance state.	
15	NPD	O	Negative polarity phase detector output.	
16	CKV	O	Gate driver shift clock.	
17	CK1A	O	Source driver shift clock ϕ1 .	
18	CK2A	O	Source driver shift clock ϕ2 .	
19	CK3A	O	Source driver shift clock ϕ3 .	
20	TEST			Note 1
21	TEST			Note 1
22	RC1	I	Resolution mode selecting pin LI	Note 2
23	GND		Ground	
24	VCC			
25	OSC/O	O	Inverted OSC signal output	
26	OSC/I	I	Master system clock input. This input pin is connected to the external VCO output for system clock timing & synchronization to the TV sync. signals through the phase locked loop block.	

Pin no	Symbol	I/O	Description	Remark
27	VSY / O	O	Negative polarity vertical sync. output	
28	TEST			Note 1
29	GR	I	Global reset. It should be connected to V_{CC} in normal operation. If connected to GND, the controller is in reset state.	
30	VSY/I	I	Vertical synchronization signal input from the sync. separator of a TV system. It should be a negative polarity.	
31	UD	O	Inverted UDC signal output.	
32	GND		Ground	
33	RC2	I	Resolution mode selecting pin III .	
34	HSY/O	O	Negative polarity horizontal sync. output.	
35	Csync	I	Positive polarity composite sync. input.	
36	GND		Ground	
37	UDC	I	Up / Down scan control pin.	
38	TEST			Note 1
39	LRC	I	Left / Right scan control pin.	
40	LRA	O	Inverted LRC signal output.	
41	TEST			Note 1
42	TEST			Note 1
43	NPC	I	It should be pulled to Vcc in normal operation.	
44	PFRP	O	Polarity alternating signal for V_{com}	
45	TEST			
46	CP/O	O	Compare pulse output.	
47	CP/I	I	Compare pulse input.	
48	VCC			

Note 1 : All the test pins should be electrically opened.
Note 2 : Resolution setting :

A18	RC1	RC2	Resolutiion mode (VXH)	Appicable Mingstar LCD
L	L	H	220 X 528	MTL020D01
L	H	H	220 X 280	SM261D series
H	L	H	234 X 960	
H	H	H	234 X 480	MTL025D01 , MTL040D01
H	L	L	234 X 1152	MTL068D01, MTL070W01

This chip can drive different Mingstar's LCD according to the above table.

D.DC characteristics

1.Absolute maximum ratings:

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power supply	-0.3 to 6.0	V
V_{IN}	Input voltage	-0.3 to VCC + 0.3	V
V_{OUT}	Output voltage	-0.3 to VCC + 0.3	V
T_{STG}	Storage temperature	-40 to 125	°C

2.Recommended operating conditions:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power supply	4.5	5.0	5.5	V
V_{IN}	Input voltage	0	-	V_{CC}	V
T_{OPR}	Operating temperature	-20	-	85	°C

3.General DC characteristics:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	Remark
I_{IL}	Input low current	no pull-up or pull-down	-1	-	1	μA	
I_{IH}	Input high current	no pull-up or pull-down	-1	-	1	μA	
I_{OZ}	Tri-state leakage current		-10	-	10	μA	
C_{IN}	Input capacitance		-	3	-	pF	
C_{OUT}	Output capacitance		3	-	6	pF	
V_{IL}	Input low voltage	CMOS	-	-	0.3Vcc	V	
V_{SIL}	Schmitt input low voltage	CMOS	-	1.76	-	V	Note 1
V_{IH}	Input high voltage	CMOS	0.7Vcc	-	-	V	
V_{SIH}	Schmitt input high voltage	CMOS	-	3.2	-	V	Note 1
V_{OL}	Output low voltage	I_{OL}=4mA	-	-	0.4	V	
V_{OH}	Output high voltage	I_{OH}=4mA	3.5	-	-	V	
R_I	Input pull up/down resistance	V_{IL}=0V or V_{IH}=V_{CC}	-	50	-	KΩ	

Note 1: The applicable pins are A18, OSC/I, GR, VSY/I, Csync, CP/I.

4.Current consumption for 5 volts operating:

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Loading
I_{IN}	Current consumption	Vcc=5V	3	5	7	mA	SM261D series
			5	8	11	mA	MTL020D01
			4	7	10	mA	MTL025D01
			4	7	10	mA	MTL040D01
			8	13	18	mA	234 X 960 mode
			9	15	21	mA	MTL068D01

E. AC characteristics

1.Timing condition

(i) 220 X 280 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	150	166	183	ns	
Csync period	t_H	61.5	63.5	65.5	μS	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μS	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	9	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	2	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	16	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	10	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	11	-	t_{CPH}	
CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	5	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	4	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	3	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	6	-	t_{CPH}	

STV setup time	t_{SUV}	-	2	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(ii) 234 X 480 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	94	104	114	ns	
Csync period	t_H	61.5	63.5	65.5	μ_S	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μ_S	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	15	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	3	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	27	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	13	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	20	-	t_{CPH}	

CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	8	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	6	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	2	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	10	-	t_{CPH}	
STV setup time	t_{SUV}	-	3	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(iii) 220 X 528 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	85	94	103	ns	
Csync period	t_H	61.5	63.5	65.5	μs	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μs	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	

STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	18	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	5	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	27	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	14	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	24	-	t_{CPH}	
CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	8	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	7	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	1	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	12	-	t_{CPH}	
STV setup time	t_{SUV}	-	4	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(iv) 234 X 960 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	47	52	57	ns	
Csync period	t_H	61.5	63.5	65.5	μS	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μS	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	30	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	7	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	54	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	26	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	40	-	t_{CPH}	
CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	14	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	12	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	4	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	20	-	t_{CPH}	
STV setup time	t_{SUV}	-	6	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(v) 234 X 1152 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	39	43	47	ns	
Csync period	t_H	61.5	63.5	65.5	μs	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μs	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	36	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	9	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	62	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	40	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	50	-	t_{CPH}	
CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	18	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	14	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	12	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	26	-	t_{CPH}	
STV setup time	t_{SUV}	-	8	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	

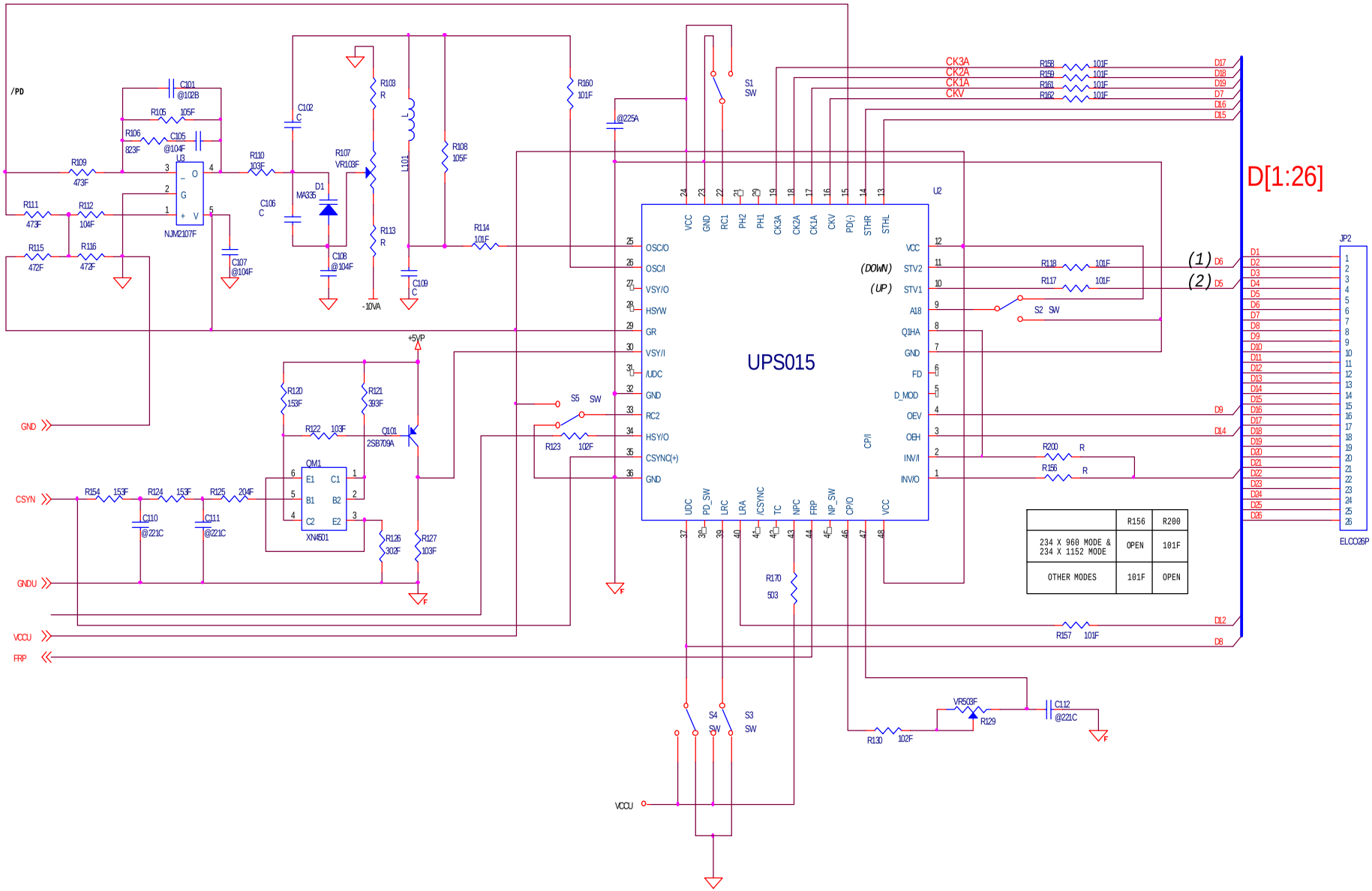
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

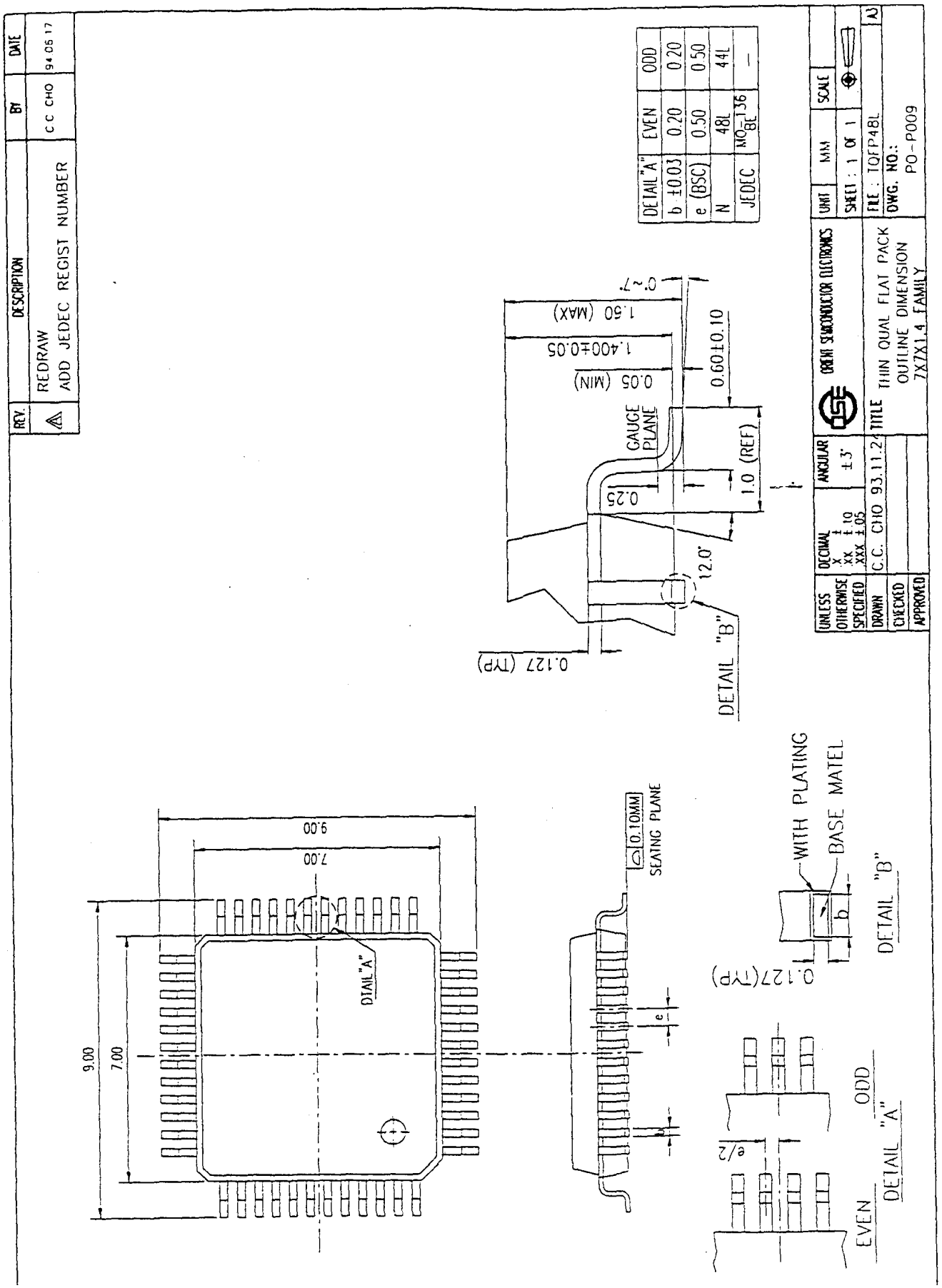
2.Timing diagram

Please refer to the attached drawing. from Fig.1 to Fig.4-(b).

F. Test circuit



G. Package information



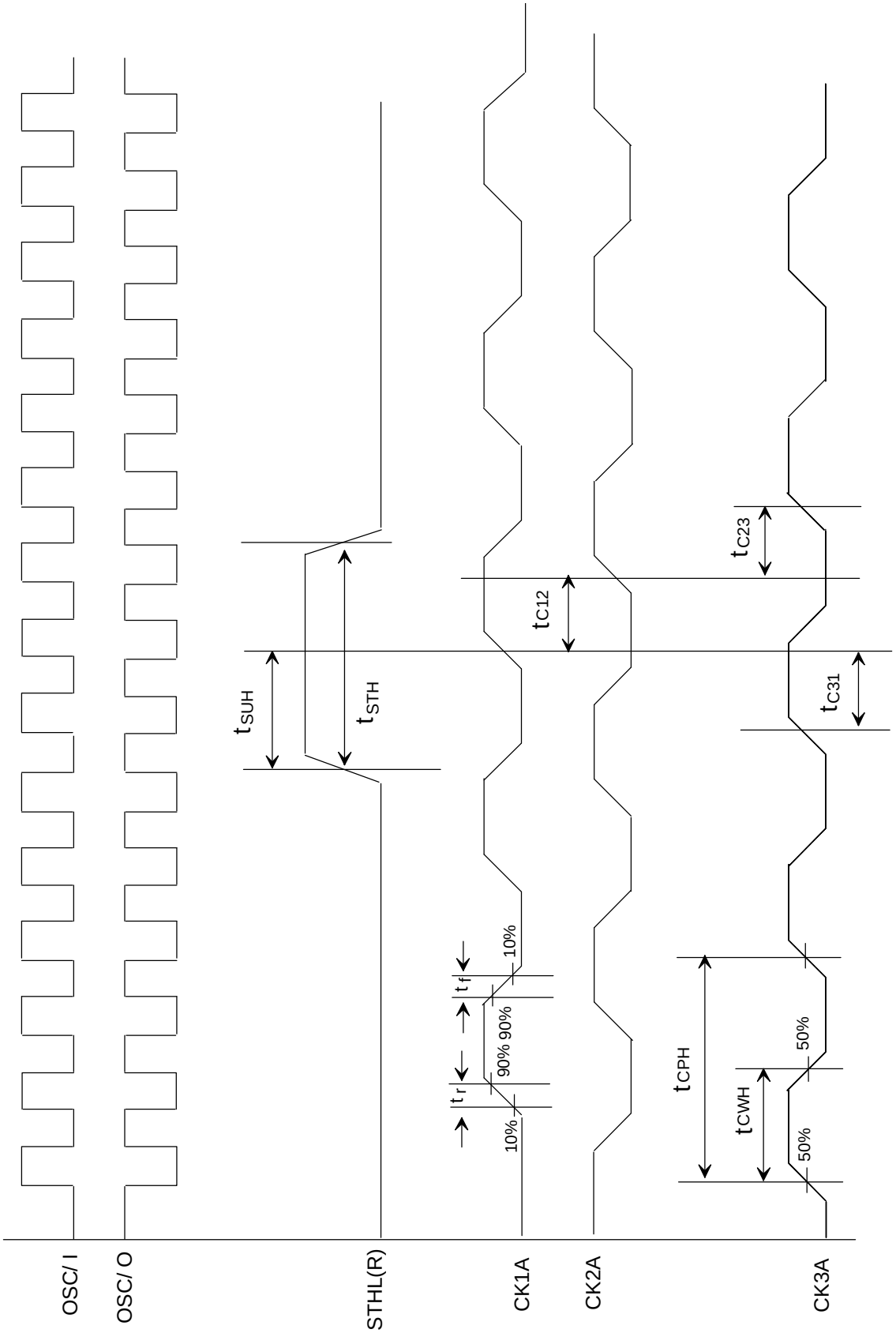
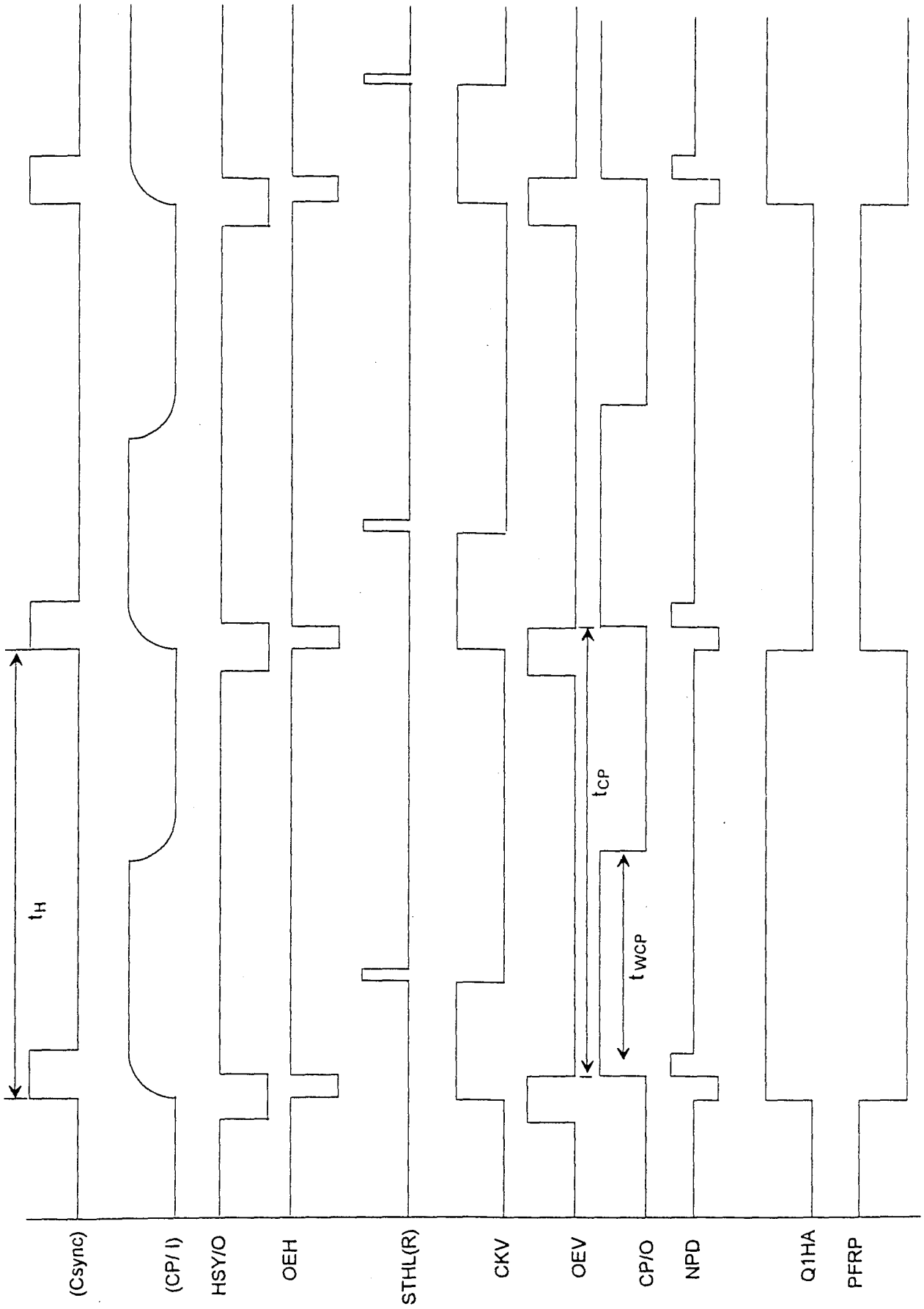
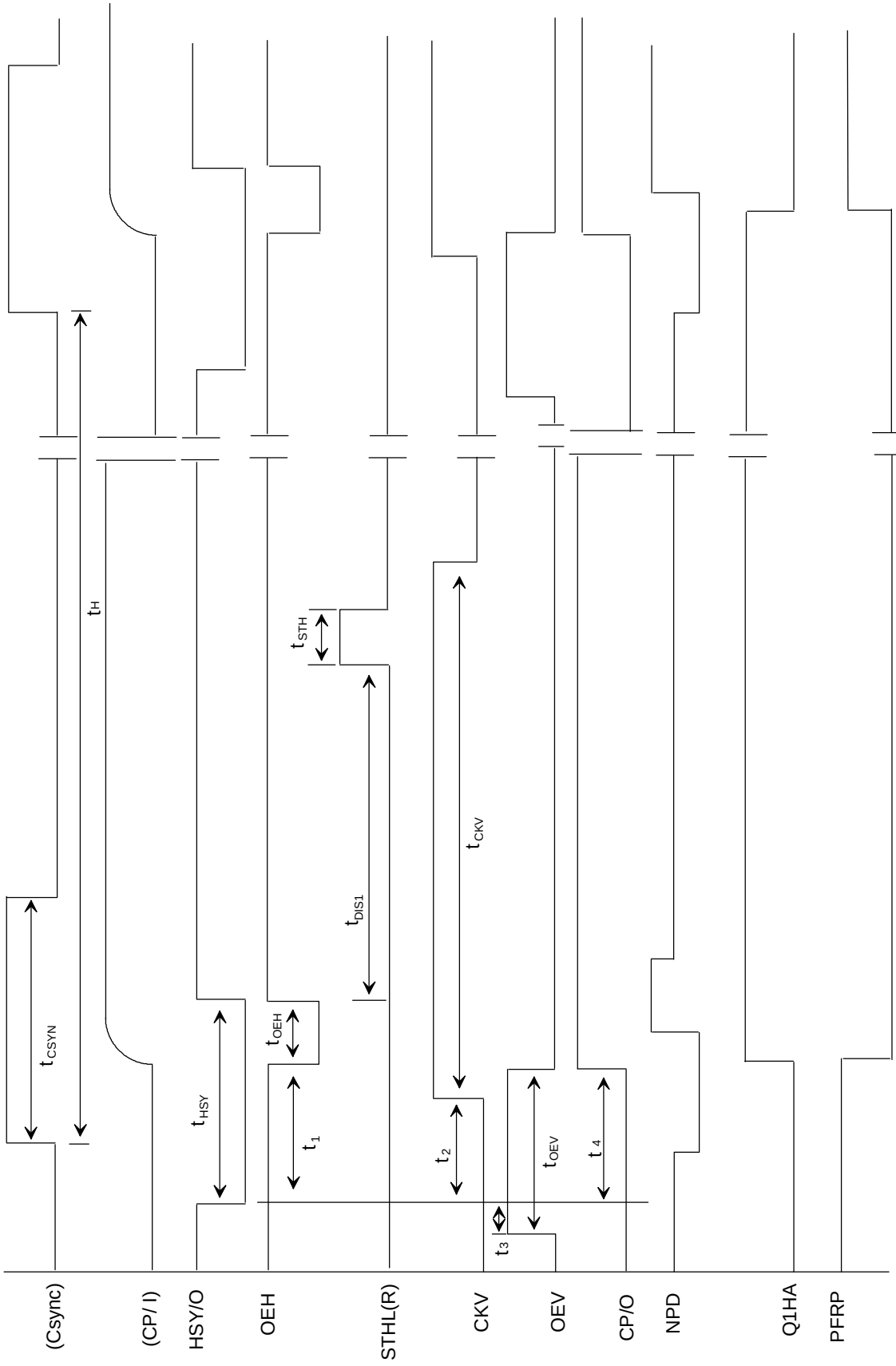


Fig.1 Sampling clock timing



※ In 234 X 960 & 234 X 1152 resolution mode , Q1HA always keeps low.

Fig.2-(a) Horizontal timing



i ° In 234 x 960 & 234 x 1152 resolution mode , Q1HA always keeps low.

Fig.2-(b) Detail horizontal timing

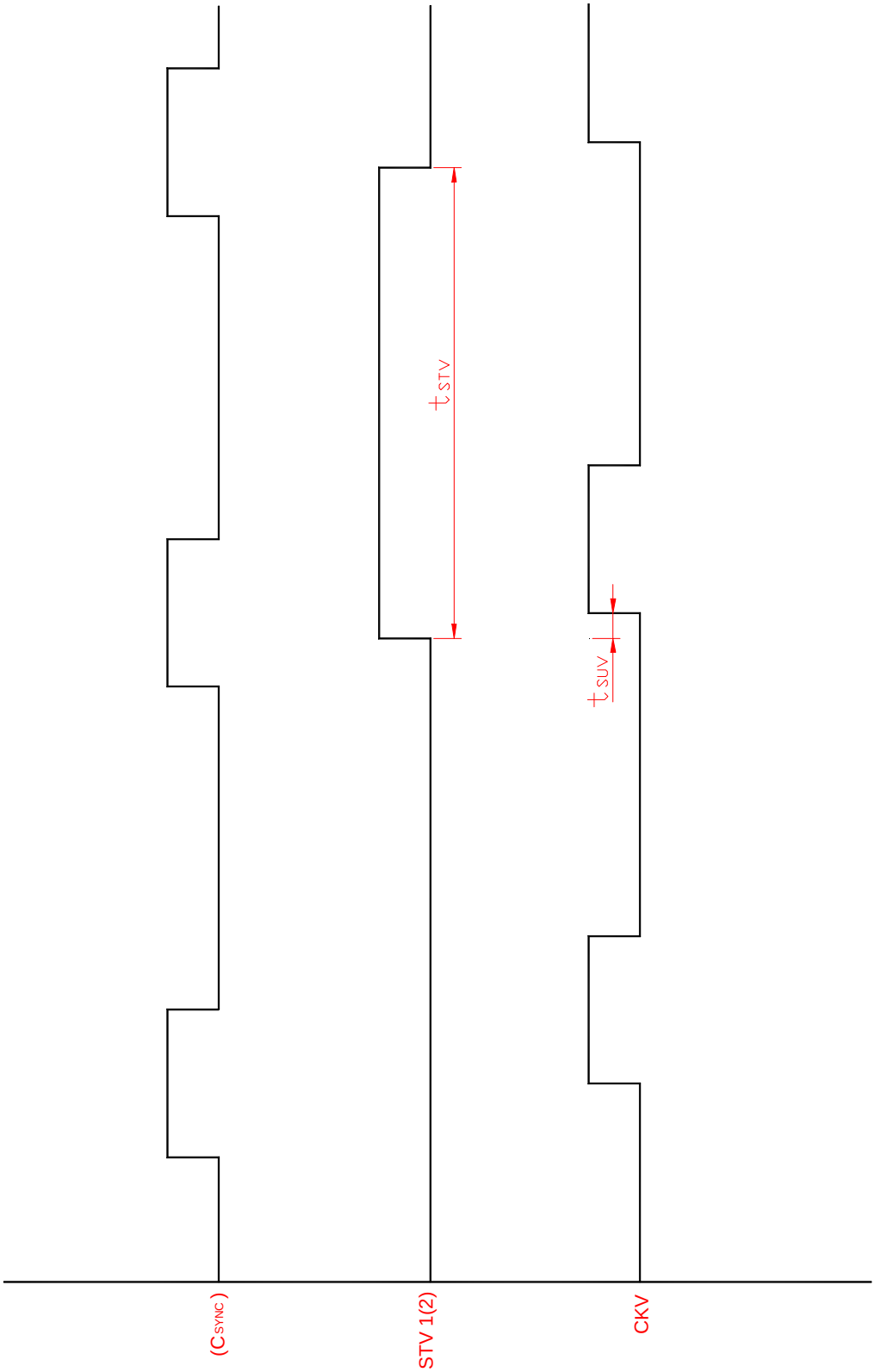
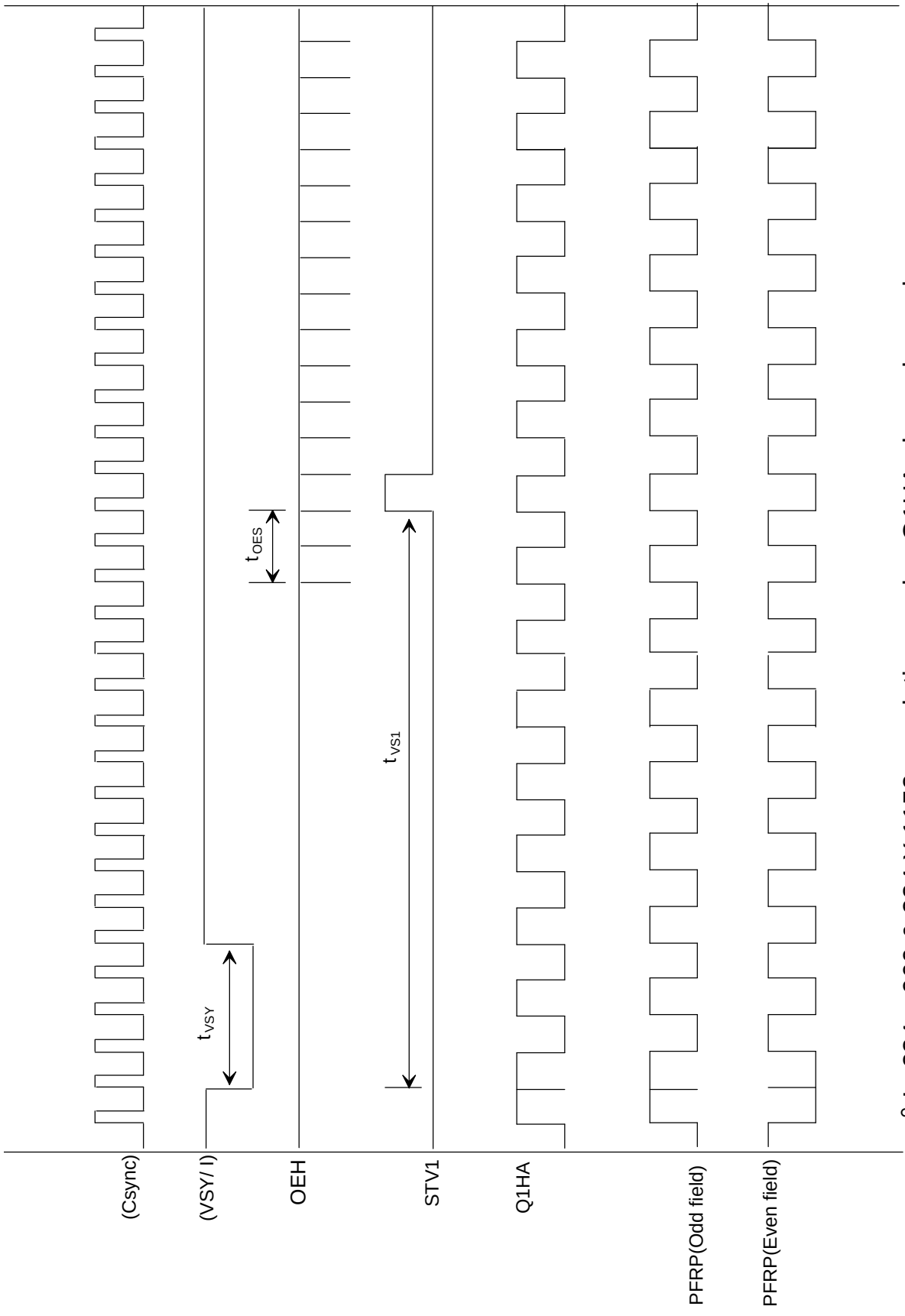
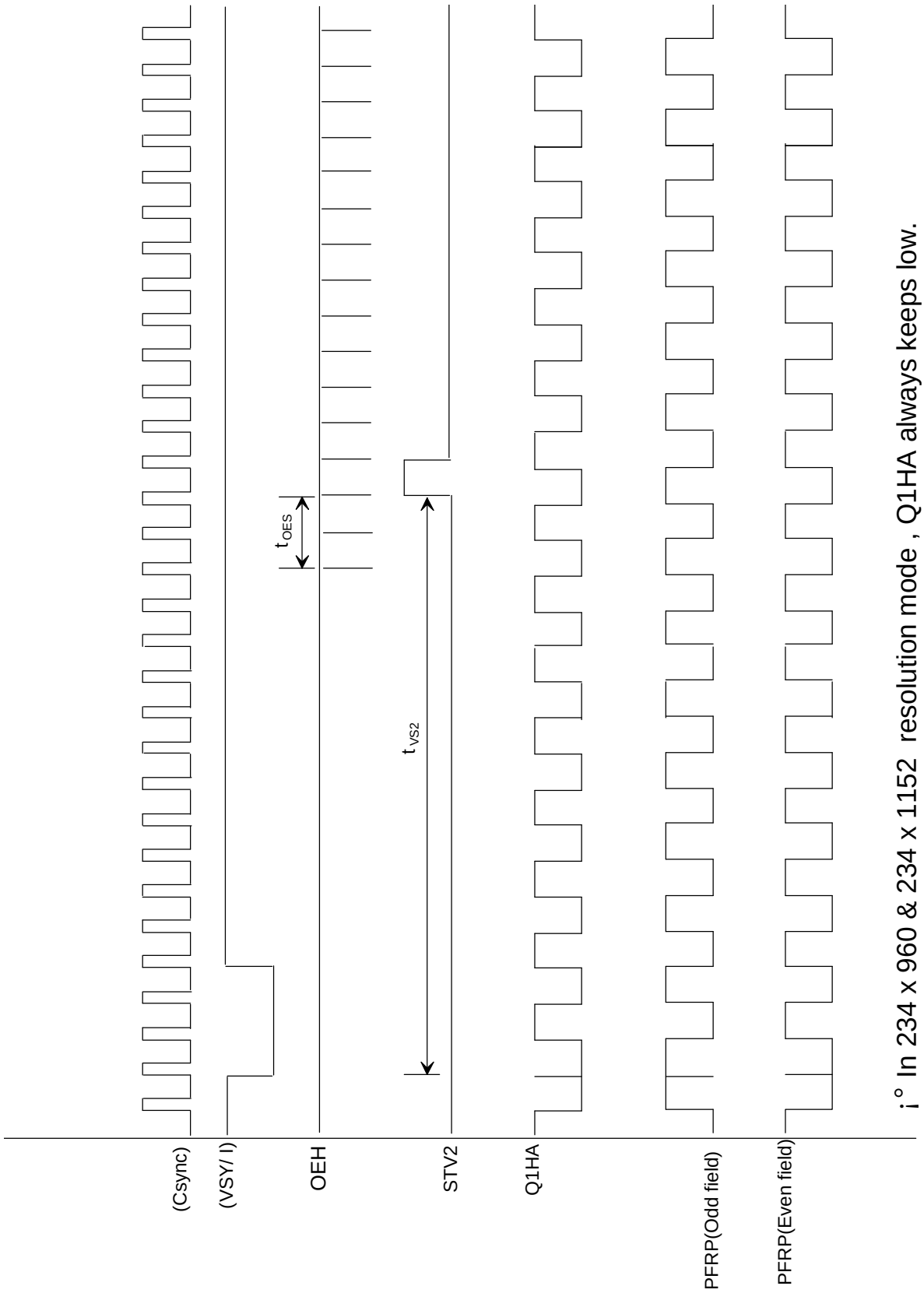


Fig.3 Vertical shift clock timing



i° In 234 x 960 & 234 X 1152 resolution mode , Q1HA always keeps low.

Fig.4-(a) Vertical timing (UDC="H")



¡° In 234 x 960 & 234 x 1152 resolution mode , Q1HA always keeps low.

Fig.4-(b) Vertical timing (UDC="L")

MINGSTAR ELECTRONIC CORP.

365-A Cloverleaf Drive
Baldwin Park, CA 91706

Fax:626-369-1655
Tel :888-314-1126