CY10E470
CY100E470

4K x 1 ECL Static RAM

Features

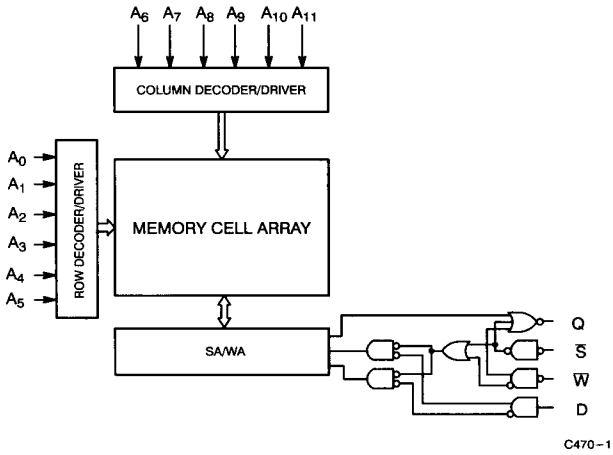
- **4096 x 1−bit organization**
- **High speed/low power**
  - **t_{AA} = 5 ns**
  - **I_{EE} = 200 mA**
- **Both 10K- and 100K-compatible versions**
- **On-chip voltage compensation for improved noise margin**
- **Open emitter output for ease of memory expansion**
- **Industry-standard pinout**

Functional Description

The Cypress CY10E470 and CY100E470 are ECL RAMs designed for scratch pad, control, and buffer storage applications. Both parts are fully decoded random access memories organized as 4096 words by 1 bit. The CY10E470 is 10K-compatible. The CY100E470 is 100K-compatible.

The active LOW chip select ($\overline{S}$) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ LOW, the data at D is written into the addressed location. To read, $\overline{W}$ is held HIGH, while $\overline{S}$ is held LOW. Open emitter outputs allow for wired-OR connection in order to expand the memory.

Logic Block Diagram



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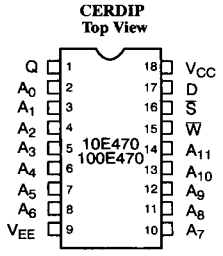
Pin Configuration



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Selection Guide

	10E470-5 100E470-5	10E470-7 100E470-7
Maximum Access Time (ns)	5	7
I_{EE} Max. (mA)	200	200

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage V_{EE} to V_{CC} ..... −7.0V to +0.5V

Input Voltage ..... V_{EE} to +0.5V

Output Current ..... −50 mA

Operating Range referenced to V_{CC}

Range	Version	Ambient Temperature	V_{EE}
Commercial	10E	0°C to + 75°C	−5.2V ± 5%
Commercial	100E	0°C to + 85°C	−4.5V ± 0.3V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Temperature[1]	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	10E R_L = 50Ω to −2V V_{EE} = −5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	−1000	−840	mV
			T_A = +25°C	−960	−810	mV
			T_A = +75°C	−900	−720	mV
		100K R_L = 50Ω to −2V V_{EE} = −4.5V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1025	−880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50Ω to −2V V_{EE} = −5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	−1870	−1665	mV
			T_A = +25°C	−1850	−1650	mV
			T_A = +75°C	−1830	−1625	mV
		100K R_L = 50Ω to −2V V_{EE} −4.5V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1810	−1620	mV
V_{IH}	Input HIGH Voltage	10E V_{EE} = −5.2V	T_A = 0°C	−1145	−840	mV
			T_A = +25°C	−1105	−810	mV
			T_A = +75°C	−1045	−720	mV
		100K V_{EE} = −4.5V	T_A = 0°C to 85°C	−1165	−880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = −5.2V	T_A = 0°C	−1870	−1490	mV
			T_A = +25°C	−1850	−1475	mV
			T_A = +75°C	−1830	−1450	mV
		100K V_{EE} = −4.5V	T_A = 0°C to 85°C	−1810	−1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{S}$ inputs	0.5	170	µA
			All other inputs	−50		µA
I_{EE}	Supply Current (All inputs and outputs open)	Commercial		−200		mA

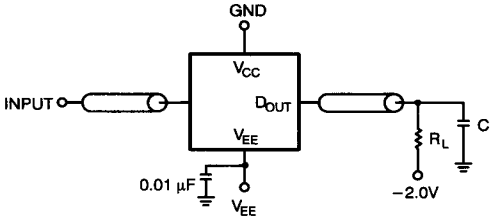
Capacitance[2]

Parameter	Description	Min.	Typ.	Max.	Unit
C_{IN}	Input Pin Capacitance		4		pF
C_{OUT}	Output Pin Capacitance		6		pF

Notes:

1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[3, 4, 5, 6, 7, 8]



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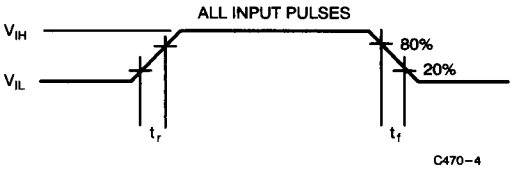

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Switching Characteristics Over the Operating Range

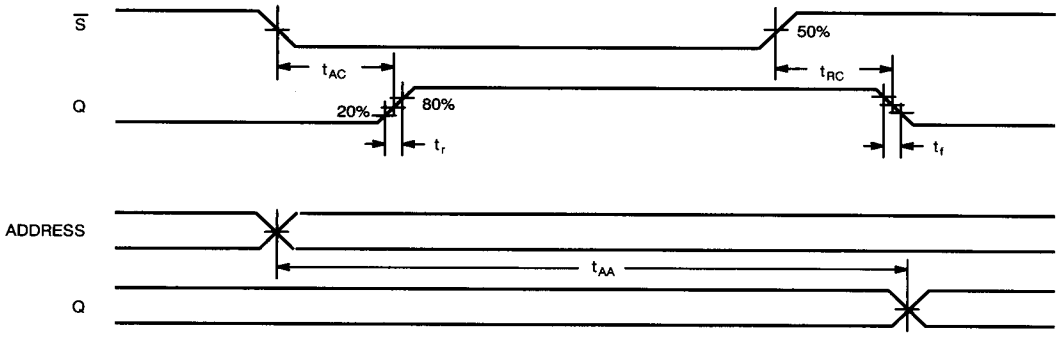
Parameter	Description	10E470–5 100E470–5		10E470–7 100E470–7		Unit
		Min.	Max.	Min.	Max.	
t_{AC}	Input to Output Delay		3.0		3.5	ns
t_{RC}	Chip Select Recovery		3.0		3.5	ns
t_{AA}	Address Access Time		5.0		7.0	ns
t_{WW}	Write Pulse Width	5.0		7.0		ns
t_{SD}	Data Set-Up to Write	0		0		ns
t_{HD}	Data Hold to Write	0		0		ns
t_{SA}	Address Set-Up/Write	0		1.0		ns
t_{HA}	Address Hold/Write	0		1.0		ns
t_{SC}	Chip Select Set-Up/Write	0		0		ns
t_{HC}	Chip Select Hold/Write	0		0		ns
t_{WS}	Write Disable		3.0		3.5	ns
t_{WR}	Write Recovery		5.0		8.0	ns
t_r	Output Rise Time	1.0	2.5	1.0	2.5	ns
t_f	Output Fall Time	1.0	2.5	1.0	2.5	ns

Notes:

3. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10E version.
4. V_{IL} = −1.7V, V_{IH} = −0.9V on 100K version.
5. R_L = 50Ω, C < 30 pF (includes fixture and stray capacitance).
6. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
7. t_r = t_f = 0.7 ns.
8. All timing measurements are made from the 50% point of all waveforms.

Switching Waveforms

Read Mode



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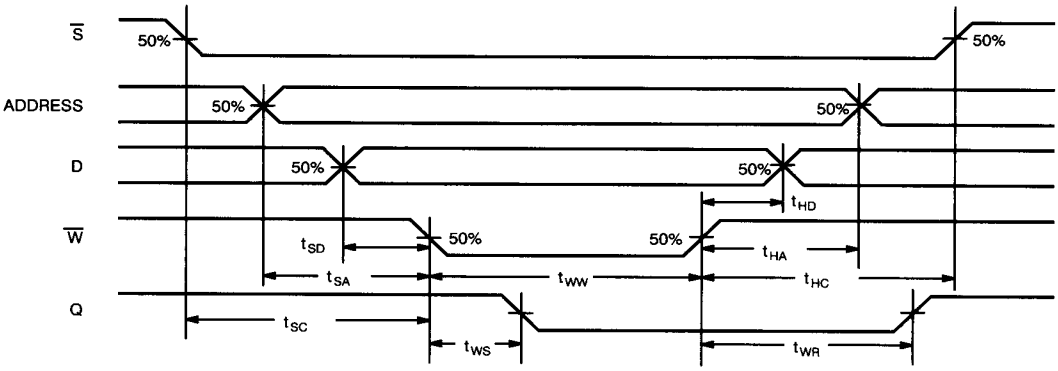
Write Mode



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Truth Table

Inputs			Output	
$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Ordering Information

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Name	Package Type	Operating Range
10K	200	5.0	CY10E470–5DC	D4	18-Lead (300-Mil) CerDIP	Commercial
		7.0	CY10E470–7DC	D4	18-Lead (300-Mil) CerDIP	
100K	200	5.0	CY100E470–5DC	D4	18-Lead (300-Mil) CerDIP	Commercial
		7.0	CY100E470–7DC	D4	18-Lead (300-Mil) CerDIP	

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