Signetics

5485, 54LS85, 54S85
Comparators

4-Bit Magnitude Comparators

Product Specification

Military Logic Products

FEATURES

- **Magnitude comparison of any binary words**
- **Serial or parallel expansion without extra gating**
- **Use 54S85 for very high-speed comparisons**

DESCRIPTION

The '85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0 - A_3) and (B_0 - B_3), where A_3 and B_3 are the most significant bits.

The operation of the '85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme.

ORDERING INFORMATION

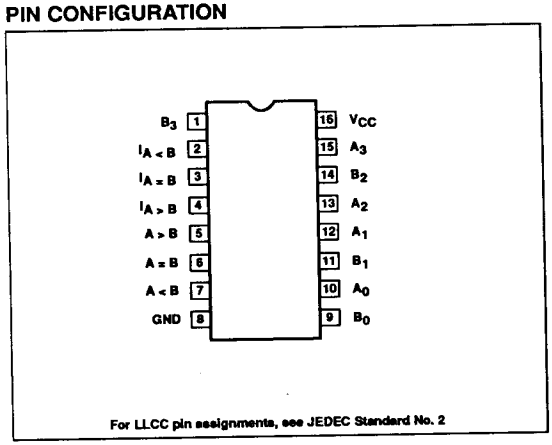
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS85/BEA 54S85/BEA 5485/BEA
16-Pin Ceramic FlatPack	54LS85/BFA 5485/BFA
16-Pin Ceramic LLCC	54LS85/B2A 54S85/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54S	54LS
A_0 - A_3, B_0 - B_3, $I_{A=B}$	Inputs	3UL	3SUL	3LSUL
$I_{A<B}$, $I_{A>B}$	Inputs	1UL	1SUL	1LSUL
A = B, A < B, A > B	Outputs	10UL	10SUL	10LSUL

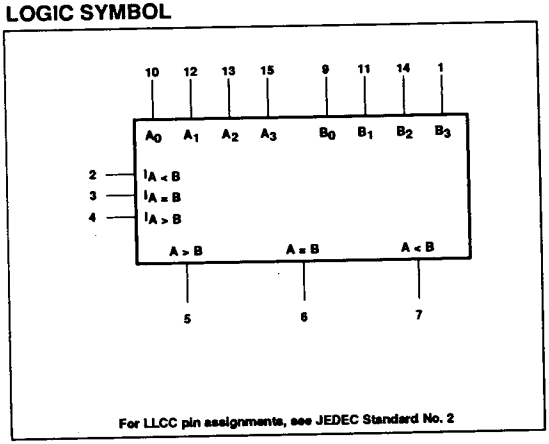
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}, a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



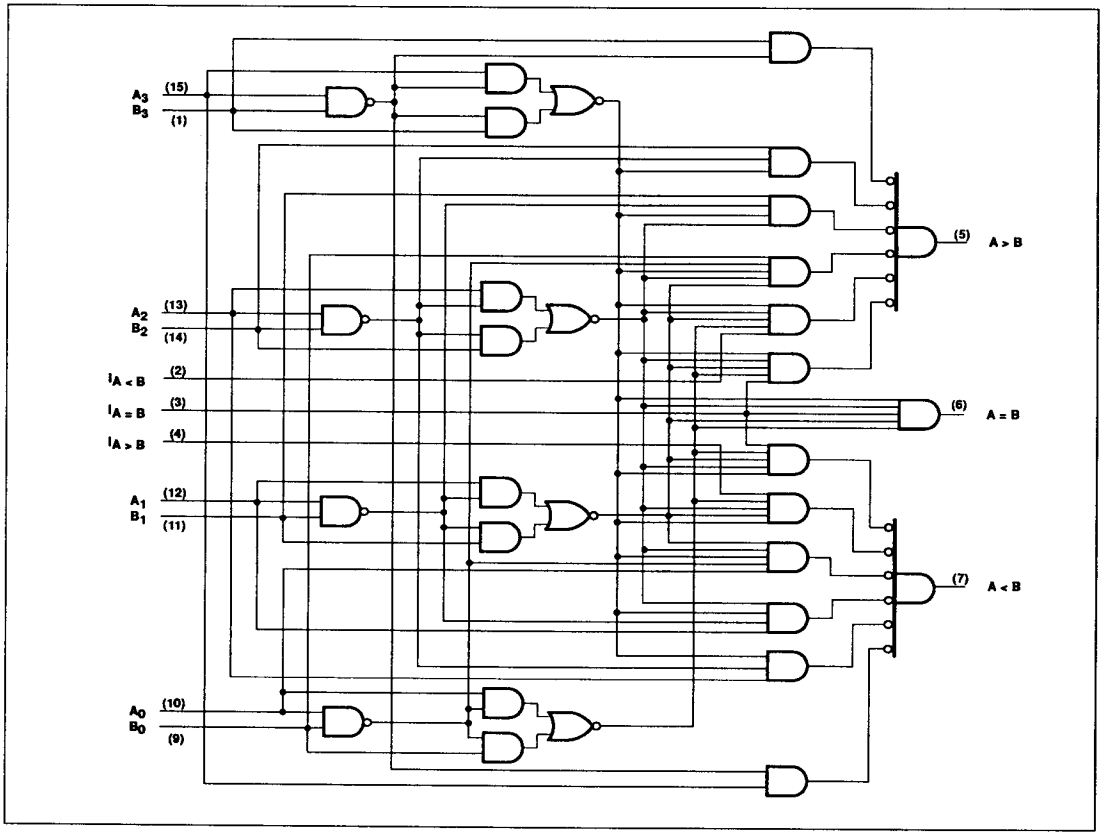
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A > B, A = B and A < B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = Low, $I_{A=B}$ = High, and $I_{A<B}$ = Low.

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ Low. The '85 can be used as a 5-bit comparator only when the outputs are used to drive the (A_0 - A_3) and (B_0 - B_3) inputs of another '85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A > B	A < B	A = B
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

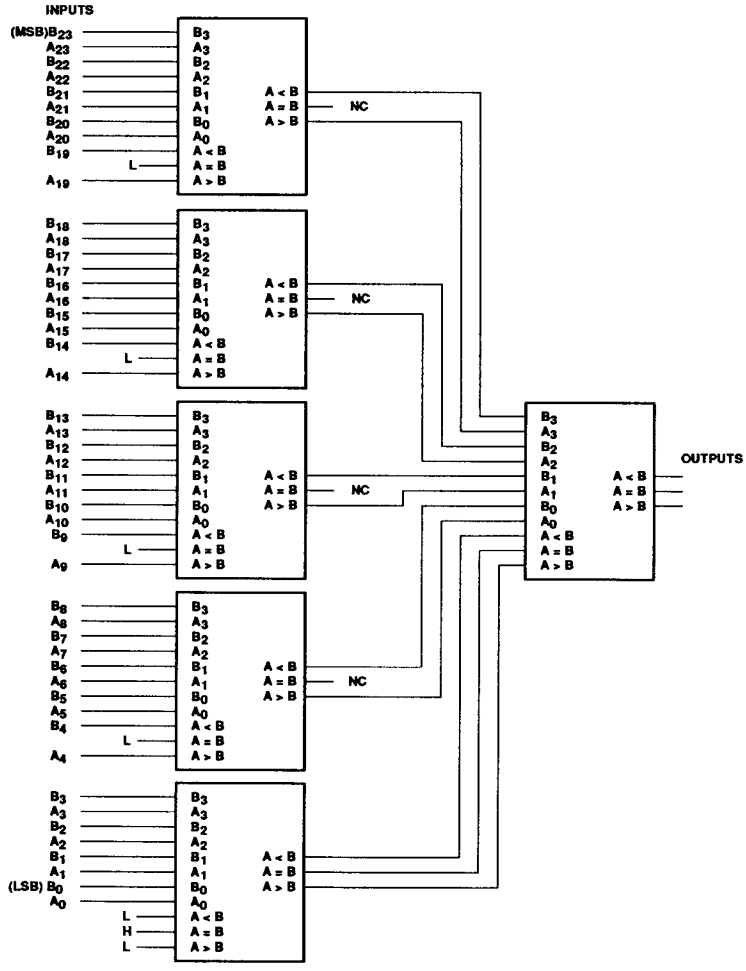


Figure 1. Comparison of Two 24-Bit Words

Table 1.

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS		
		54	54S	54LS
1 - 4 Bits	1	23ns	12ns	23ns
5 - 25 Bits	2 - 6	40ns	22ns	46ns
25 - 120 Bits	8 - 31	63ns	34ns	69ns

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150			°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		54			54LS			54S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			2.0			2.0			V
V_{IL}	Low-level input voltage				+0.8			+0.7			+0.8	V
		+125°C			+0.8			+0.7			+0.7	V
I_{IK}	Input clamp current				-12			-18			-18	mA
I_{OH}	High-level output current				-400			-400			-1000	µA
I_{OL}	Low-level output current				16			4			20	mA
T_A	Operating free-air temperature range		-55		+125	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			5485			54LS85			54S85			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max			2.4	3.4		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max				0.2	0.4		0.25	0.4			0.5	V
				+125°C			0.4			0.4			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V	$I_{A<B}$, $I_{A>B}$						0.1				mA
				Other inputs						0.3				mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V	$I_{A<B}$, $I_{A>B}$			40							µA
				Other inputs			120							µA
			V_I = 2.7V	$I_{A<B}$, $I_{A>B}$						20			50	µA
				Other inputs						60			150	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V	$I_{A<B}$, $I_{A>B}$			-1.6			-0.4				mA
				Other inputs			-4.8			-1.2				mA
			V_I = 0.5V	$I_{A<B}$, $I_{A>B}$									-2.0	mA
				Other inputs									-6.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-18		-55	-20		-100	-40		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max				55	88		10.4	20		73	115	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS[5]		54S[5]		UNIT
			C_L = 15pF		C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output	Waveform 1 3 logic levels		26 30		36 30		16 16.5	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 2 4 logic levels		35 30		45 45		18 16.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A > B output	Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 2 2 logic levels		20 17		20 26		10.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A < B output	Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

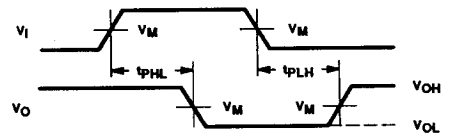
SYMBOL	PARAMETER	TEST CONDITIONS	54[5]		54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output	Waveform 1 3 logic levels		30 34		41 35		19.0 19.5	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 2 4 logic levels		39 34		50 50		19.5 19.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A > B output	Waveform 1 1 logic level		15 21		27 22		9.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 2 2 logic levels		24 21		25 31		13.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A < B output	Waveform 1 1 logic level		15 21		27 22		9.5 10.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V

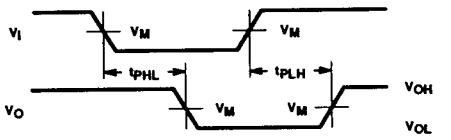
SYMBOL	PARAMETER	TEST CONDITIONS	54[5]		54LS[5]		54S[5]		UNIT
			C_L = 50pF		C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output	Waveform 1 3 logic levels		39 44		53 46		23 24	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 2 4 logic levels		51 44		65 65		25 24	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A > B output	Waveform 1 1 logic level		20 27		35 29		11.5 13	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 2 2 logic levels		31 27		33 40		16 12	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A < B output	Waveform 1 1 logic level		20 27		35 29		11.5 13	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open, A = B grounded, and all other inputs at ≥ 4.0V.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



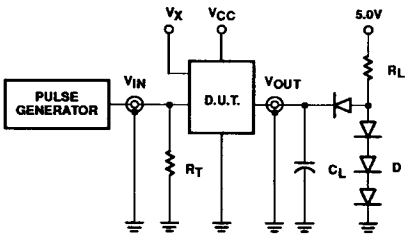
Waveform 1. Waveform for Inverting Outputs



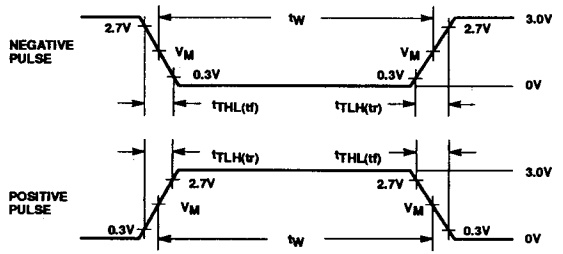
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.3V for 54LS, V_M = 1.5V for all other TTL families.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.