

Features

- 8192 x 8 bit static CMOS RAM
- 250 and 500 ns Access Times
- Common data inputs and data outputs
- Three-state outputs
- Typ. operating supply current:
250 ns: 12 mA
500 ns: 7 mA
- Standby current < 5 μ A
- Standby current at 25 °C and 3.3 V: typ. 50 nA
- TTL/CMOS-compatible
- Automatic reduction of power dissipation in long Read or Write cycles
- Power supply voltage 3.3 V
- Operating temperature ranges
0 to 70 °C
-25 to 85 °C
-40 to 85 °C
- Quality assessment according to CECC 90000, CECC 90100 and CECC 90111
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity > 100 mA

- Packages: PDIP28(600 mil)
SOP28 (330 mil)

Description

The UL6264A is a static RAM manufactured using a CMOS process technology with the following operating modes:

- Read - Standby
- Write - Data Retention

The memory array is based on a 6-transistor cell.

The circuit is activated by the rising edge of E2 (at $\overline{E1} = L$) or the falling edge of $\overline{E1}$ (at E2 = H). The address and control inputs open simultaneously. According to the information of $\overline{W}$ and $\overline{G}$ the data inputs, or outputs, are active. In the active state $\overline{E1} = L$ and E2 = H, each address change leads to a new Read or Write cycle. In a Read cycle, the data outputs are activated by the falling edge of $\overline{G}$, afterwards the data word read will be available at the outputs

DQ0 - DQ7. After the address

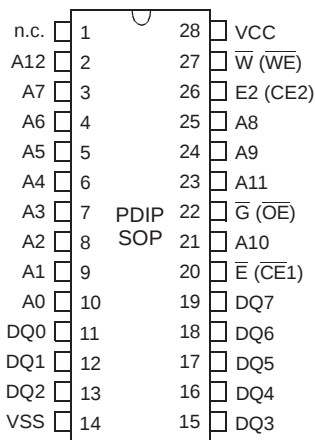
change, the data outputs go High-Z until the new read information is available. The data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no change of the address, data input and control signals $\overline{W}$ or $\overline{G}$, the operating current (at $I_O = 0$ mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of E2 or $\overline{W}$, or by the rising edge of $\overline{E1}$, respectively.

Data retention is guaranteed down to 2 V.

With the exception of E2, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required. This gate circuit allows to achieve low power standby requirements by activation with TTL-levels too.

If the circuit is inactivated by E2 = L, the standby current (TTL) drops to 100 μ A typ.

Pin Configuration

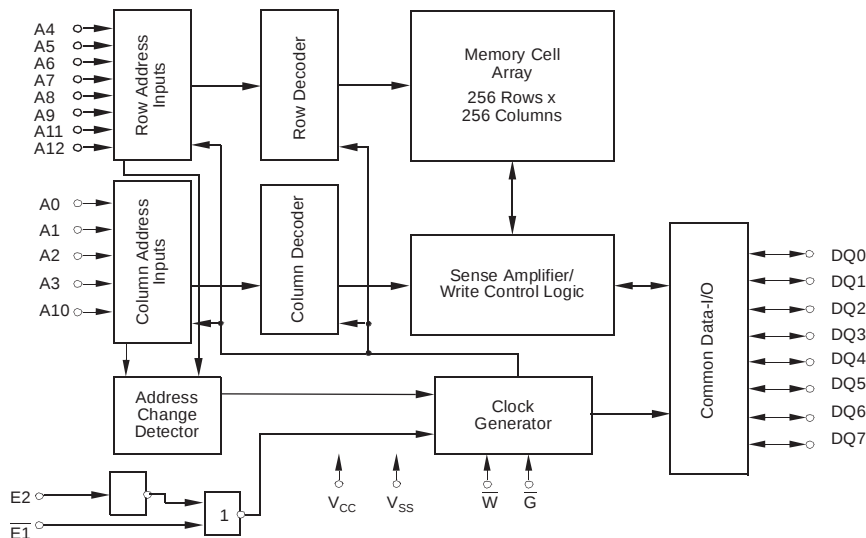


Top View

Pin Description

Signal Name	Signal Description
A0 - A12	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground
n.c.	not connected

Block Diagram



Truth Table

Operating Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	*	L	*	*	High-Z
	H	*	*	*	High-Z
Internal Read	L	H	H	H	High-Z
Read	L	H	H	L	Data Outputs Low-Z
Write	L	H	L	*	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to $V_{SS} = 0$ V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I , as well as input levels of $V_{IL} = 0$ V and $V_{IH} = 3$ V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis} -times, in which cases transition is measured ± 200 mV from steady-state voltage.

Maximum Ratings		Symbol	Min.	Max.	Unit
Power Supply Voltage		V_{CC}	-0.3	7	V
Input Voltage		V_I	-0.3	$V_{CC} + 0.5$	V
Output Voltage		V_O	-0.3	$V_{CC} + 0.5$	V
Power Dissipation		P_D		1	W
Operating Temperature	C-Type	T_a	0	70	$^{\circ}\text{C}$
	G-Type		-25	85	$^{\circ}\text{C}$
	K-Type		-40	85	$^{\circ}\text{C}$
Storage Temperature		T_{stg}	-55	125	$^{\circ}\text{C}$

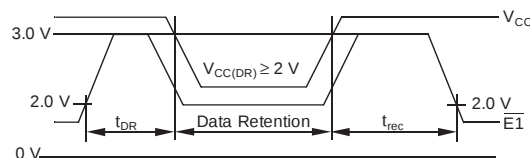
Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		3.0	3.6	V
Data Retention Voltage	$V_{CC(DR)}$		2.0		V
Input Low Voltage*	V_{IL}		-0.3	0.8	V
Input High Voltage	V_{IH}		2.0	$V_{CC} + 0.3$	V

* -2 V at Pulse Width 10 ns

Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	$V_{CC} = 3.6\text{ V}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.0\text{ V}$ $t_{cW} = 500\text{ ns}$ $t_{cW} = 250\text{ ns}$		20 30	mA mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	$V_{CC} = 3.6\text{ V}$ $V_{E1} = V_{E2} = V_{CC} - 0.2\text{ V}$		5	μA
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	$V_{CC} = 3.6\text{ V}$ $V_{E1} = V_{E2} = 2.0\text{ V}$		2 (typ. 0.7)	mA
Output High Voltage	V_{OH}	$V_{CC} = 3.0\text{ V}$ $I_{OH} = -1.0\text{ mA}$	2.4		V
Output Low Voltage	V_{OL}	$V_{CC} = 3.0\text{ V}$ $I_{OL} = 2.0\text{ mA}$		0.4	V
Input High Leakage Current	I_{IH}	$V_{CC} = 3.6\text{ V}$ $V_{IH} = 3.6\text{ V}$		1	μA
Input Low Leakage Current	I_{IL}	$V_{CC} = 3.6\text{ V}$ $V_{IL} = 0\text{ V}$	-1		μA
Output High Current	I_{OH}	$V_{CC} = 3.0\text{ V}$ $V_{OH} = 2.4\text{ V}$		-1	mA
Output Low Current	I_{OL}	$V_{CC} = 3.0\text{ V}$ $V_{OL} = 0.4\text{ V}$	2.0		mA
Output Leakage Current High at Three-State Outputs	I_{OHZ}	$V_{CC} = 3.6\text{ V}$ $V_{OH} = 3.6\text{ V}$		1	μA
Low at Three-State Outputs	I_{OLZ}	$V_{CC} = 3.6\text{ V}$ $V_{OL} = 0\text{ V}$	-1		μA

Switching Characteristics	Symbol		Min.		Max.		Unit
	Alt.	IEC	25	50	25	50	
Time to Output in Low-Z	t_{LZ}	$t_{t(QX)}$	20	20			ns
$\overline{G}$ LOW to Output in Low-Z	t_{OLZ}	$t_{tG(QX)}$	10	10			ns
Cycle Time							
Write Cycle Time	t_{WC}	t_{cW}	250	500			ns
Read Cycle Time	t_{RC}	t_{cR}	250	500			ns
Access Time							
$\overline{E1}$ LOW or E2 HIGH to Data Valid	t_{ACE}	$t_{a(E)}$	-	-	250	500	ns
$\overline{G}$ LOW to Data Valid	t_{OE}	$t_{a(G)}$	-	-	100	100	ns
Address to Data Valid	t_{AA}	$t_{a(A)}$	-	-	250	500	ns
Pulse Widths							
Write Pulse Width	t_{WP}	$t_{w(W)}$	120	150			ns
Chip Enable to End of Write	t_{CW}	$t_{w(E)}$	180	210			ns
Setup Times							
Address Setup Time	t_{AS}	$t_{su(A)}$	0	0			ns
Chip Enable to End of Write	t_{CW}	$t_{su(E)}$	180	210			ns
Write Pulse Width	t_{WP}	$t_{su(W)}$	120	150			ns
Data Setup Time	t_{DS}	$t_{su(D)}$	80	100			ns
Data Hold Time							
Address Hold Time from End of Write	t_{DH}	$t_{h(D)}$	0	0			ns
	t_{AH}	$t_{h(A)}$	0	0			ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	20	20			ns
$\overline{E1}$ HIGH or E2 LOW to Output in High-Z	t_{HZCE}	$t_{dis(E)}$	0	0	60	60	ns
$\overline{W}$ LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$	0	0	60	60	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$	0	0	40	40	ns

Data Retention Mode $\overline{E1}$ -Controlled



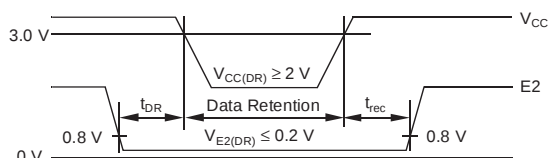
$$V_{E2(DR)} \geq V_{CC(DR)} - 0.2 \text{ V or } V_{E2(DR)} \leq 0.2 \text{ V}$$

$$V_{CC(DR)} - 0.2 \text{ V} \leq V_{\overline{E1}(DR)} \leq V_{CC(DR)} + 0.3 \text{ V}$$

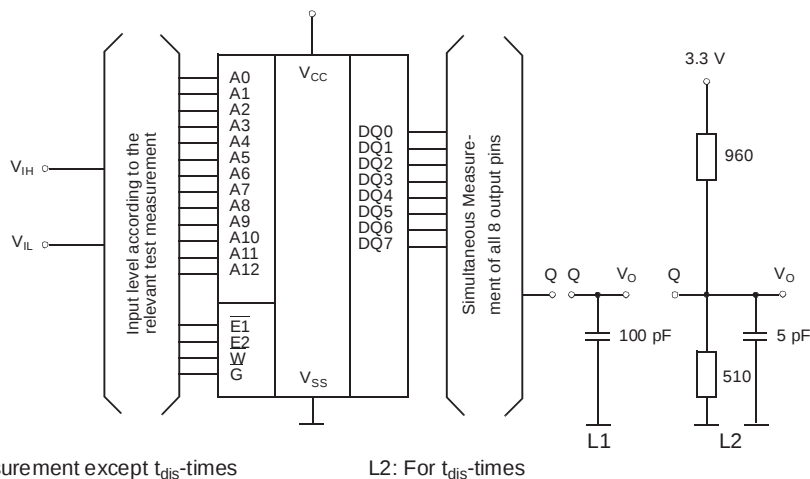
Chip Deselect to Data Retention Time
Operating Recovery Time

t_{DR} : min 0 ns
 t_{rec} : min t_{cR}

Data Retention Mode E2-Controlled



Test Configuration for Functional Check



L1: For dynamic measurement except t_{dis} -times

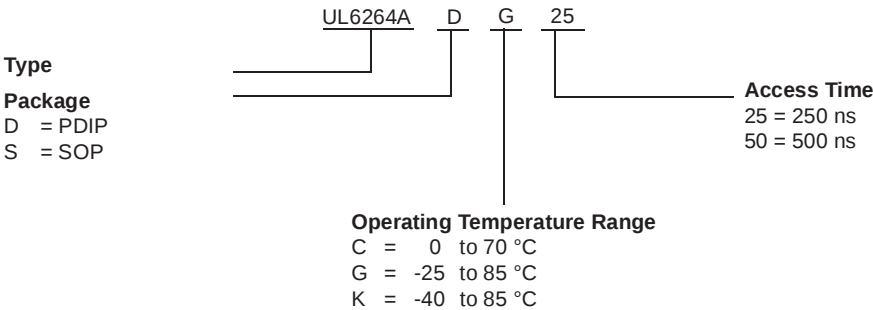
L2: For t_{dis} -times

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	$V_{CC} = 3.3\text{ V}$ $V_I = V_{SS}$	C_I		8	pF
Output Capacitance	$f = 1\text{ MHz}$ $T_a = 25\text{ }^{\circ}\text{C}$	C_O		10	pF

All pins not under test must be connected with ground by capacitors.

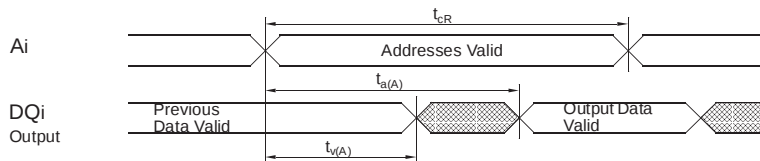
IC Code Numbers

Example

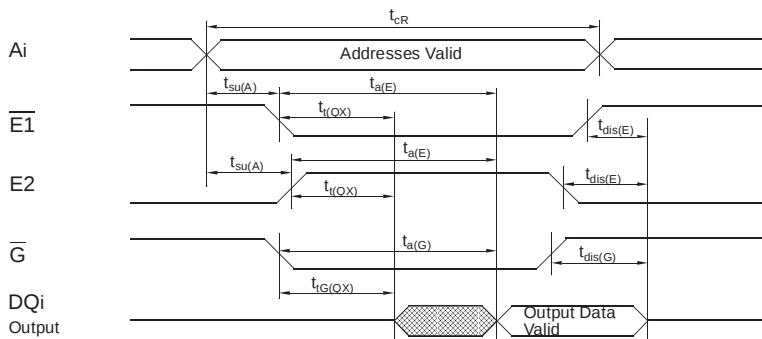


The date of manufacture is given by the 4 last digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

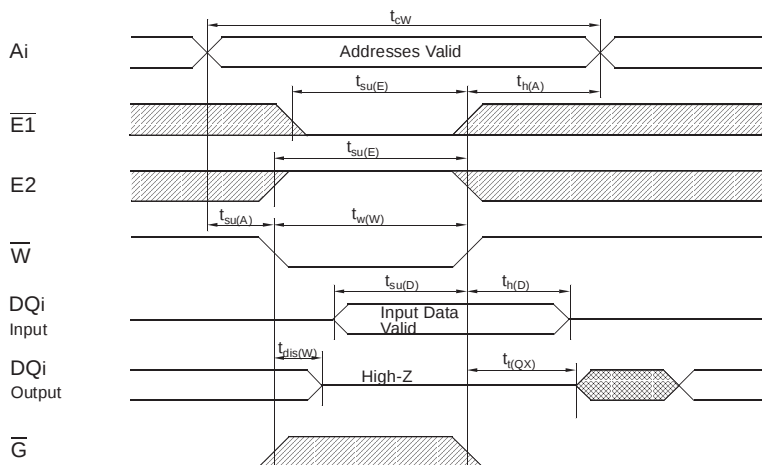
Read Cycle 1 (during Read Cycle: $\overline{E1} = \overline{G} = V_{IL}$, $E2 = \overline{W} = V_{IH}$)



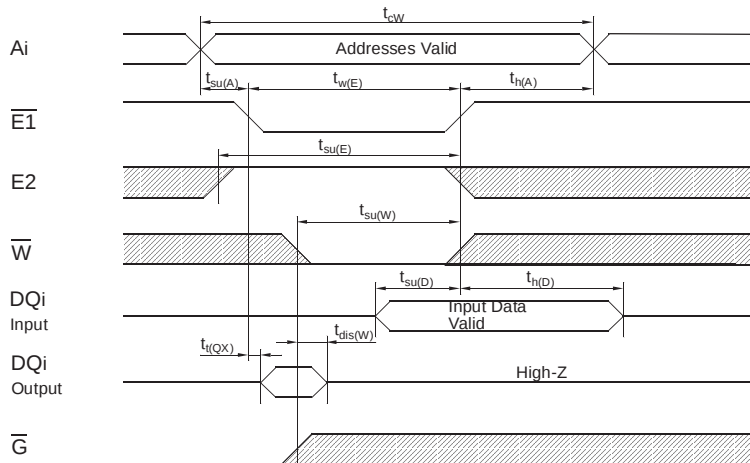
Read Cycle 2 (during Read Cycle: $\overline{W} = V_{IH}$)



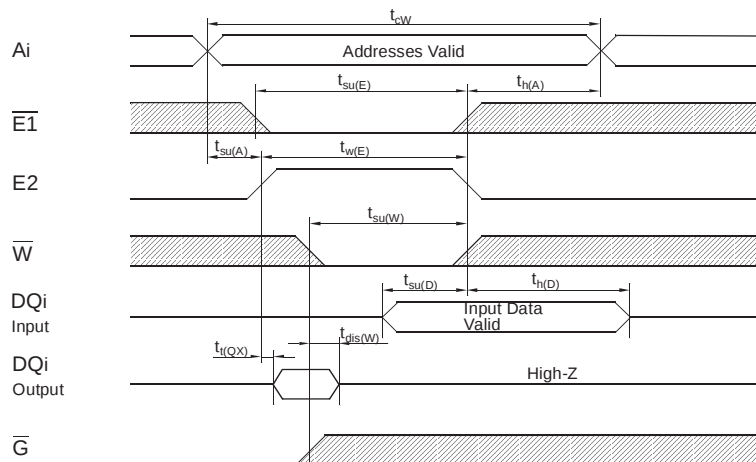
Write Cycle 1 ($\overline{W}$ -controlled)



Write Cycle 2 ($\overline{E1}$ -controlled)



Write Cycle 3 (E2-controlled)



undefined



L- or H-Level





Zentrum Mikroelektronik Dresden

Memory Products 1998

Low Voltage 8K x 8 SRAM UL6264A

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