DIGITAL SIGNAL PROCESSOR

- 160ns INSTRUCTION CYCLE TIME
- PARALLEL HARVARD ARCHITECTURE
- SEPARATED PROGRAM AND DATA BUSES
- THREE DATA BUSES STRUCTURE
- DUAL EXTERNAL BUSES
- ONE CYCLE 16-BIT R/W OPERATION ON EXTERNAL DATA MEMORY
- THREE DATA TYPES : 16-BIT REAL, 32-BIT REAL, 16 + 16-BIT COMPLEX
- EXTERNAL MASKABLE INTERRUPT
- COMPLEX MULTIPLIER
- 256 x 16-BIT INTERNAL RAMs, 512 x 16-BIT INTERNAL COEFFICIENT ROM
- 1.28K x 32-BIT WORDS OF INTERNAL PROGRAM ROM
- NO FUNCTIONAL DIFFERENCES BETWEEN TS68930 ROM VERSION AND TS68931 ROMLESS VERSION

DESCRIPTION

The TS68930/31 HMOS digital signal processors are members of SGS-THOMSON family of general purpose DSP's fully software and hardware compatible with other members of the family.

By virtue of their highly parallel architecture, these digital signal processors are well suited to a wide range of applications including those requiring operations on complex numbers.

Typical examples are found in telecommunications, modems, image and speech processing, high speed control, digital filtering, sonar and radar applications.

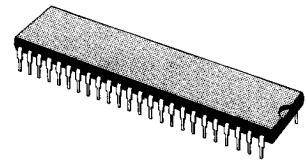
They are able to execute simultaneously within 160 ns an ALU function, a Multiplication, two Read and one Write operations with associated address calculation.

The on-chip large memory resources and multiprocessor direct interface allows the development at the lowest cost/complexity of high performance applications. The TS68931 is the ROMless version of the TS68930. In addition of the TS68930 features, it provides the capability of addressing up to 64K x 32 external instruction memory and allows a total realtime emulation of the TS68930. It is also particularly well adapted for applications where large program is required or for low quantities.

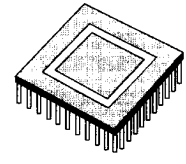
DEVELOPMENT SYSTEMS

The TS68930 is supported by a complete set of hardware and software tools for applications development. Software packages include assembler, linker and simulator on VAX and PC as well as a high level "C" compiler and optimizer.

Hardware tools include a stand-alone emulator, eprom emulation module and a powerful multiprocessor development station.



TS68930
P
DIP 48
(Plastic Package)



TS68931
R
PGA84
(Pin Grid Array Ceramic)

For pin connections and order codes, please see inside

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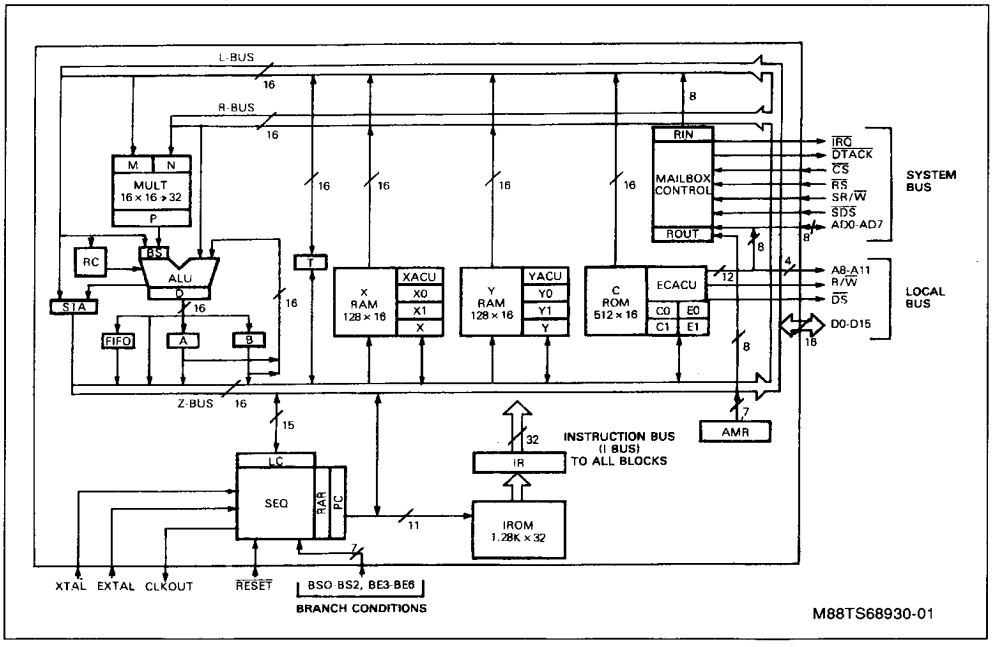
1. BLOCK DIAGRAM (TS68930)

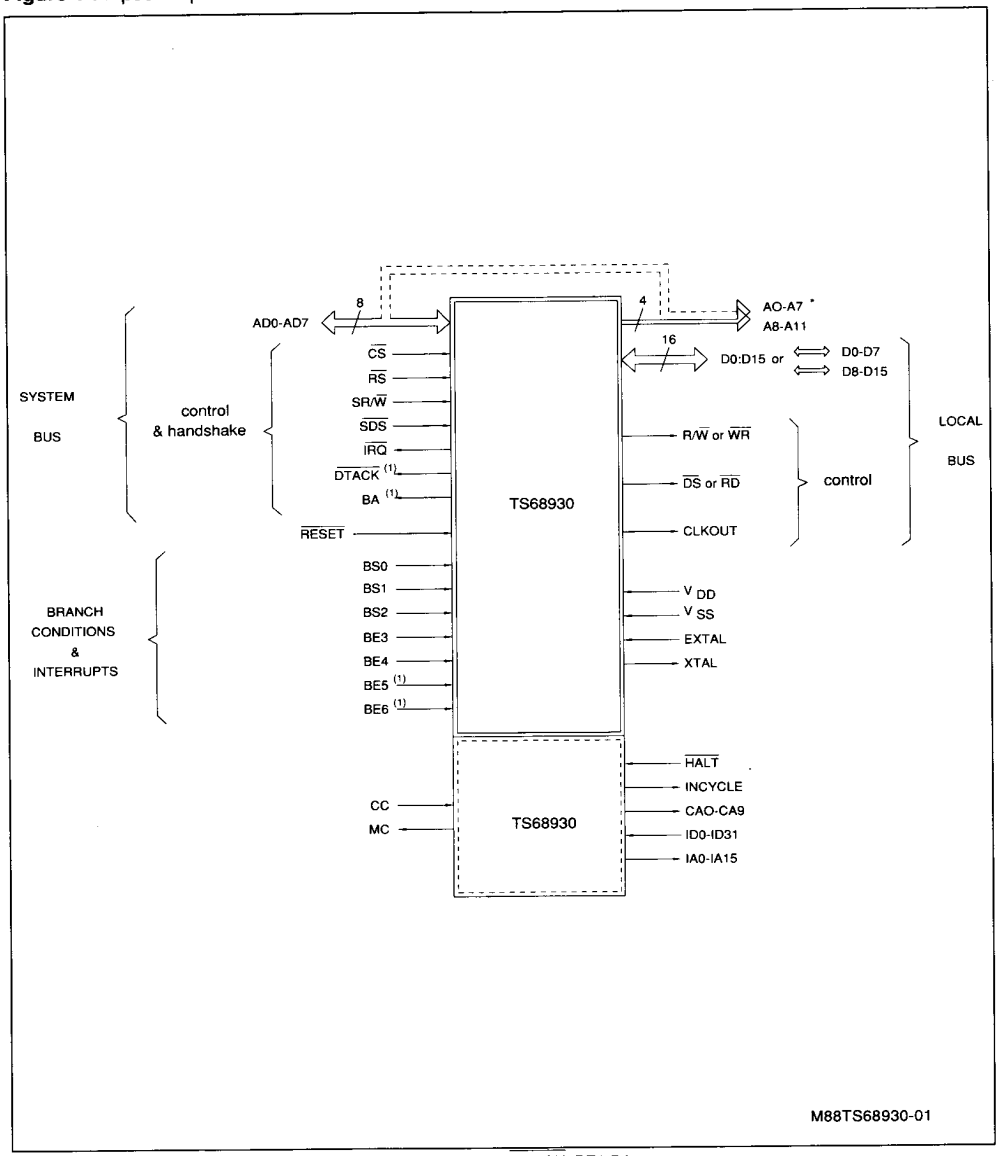


DEFINITION OF ACRONYMS

L-bus	: Left data bus	CROM	: Coefficient ROM
R-bus	: Right data bus	X0, X1, X	: Addressing registers XRAM
M	: Multiplier input register	Y0, Y1, Y	: Addressing registers YRAM
N	: Multiplier input register	C0, C1	: Addressing registers CROM
P	: Multiplier output register	E0, E1	: Addressing registers ERAM
BS	: Barrel Shifter	XACU	: Address calculation unit XRAM
ALU	: Arithmetic and Logic Unit	YACU	: Address calculation unit YRAM
D	: ALU output register	ECACU	: Address calculation unit CROM & ERAM
RC	: Replace Code register	RIN	: Input register of mailbox
STA	: Status register	ROUT	: Output register of mailbox
FIFO	: ALU output FIFO	AMR	: Access mode register
A	: ALU accumulator	IR	: Instruction register
B	: ALU accumulator	PC	: Program counter
Z- bus	: Result data bus	RAR	: Return address register
T	: Transfer register	SEQ	: Sequencer
XRAM	: X Data RAM	LC	: Loop Counter
YRAM	: Y Data RAM	IROM	: Instruction ROM

2. PIN DESCRIPTION

Figure 1 : Input/Output Pins.



Notes : 1. these pins are shared and software programmable : BE5/DTACK, BE6/BA
2. A0-A7 and AD0-AD7 may be multiplexed.

LOCAL INTERFACE

Name	Pin Type	Function	Description
D (0:15)	I/O	Data Bus	Can be concatenated or separate D (0:7), D (8:15).
A (8:11)	O	Address Bus	High order addresses for local interface.
$\overline{DS}/\overline{RD}$	O	Data Strobe/read	Synchronizes the transfer on local bus/read cycle.
$R/\overline{W}/\overline{WR}$	O	Read/write/write	Indicates the current bus cycle state/write cycle.
CLKOUT	O	Clock Output	CLKOUT Frequency is half input clock frequency.

SYSTEM INTERFACE

Name	Pin Type	Function	Description
AD (0:7)	I/O	System Data Bus or Local Address Bus	System data bus for exchanges between the processor and a host via an internal mailbox or local address bus for external RAM.
$\overline{CS}$	I	Chip Select	Used by a host to gain access to the mailbox and system bus.
$\overline{RS}$	I	Register Select	Used by a host to gain access to the mailbox and system bus.
$\overline{SDS}$	I	Data Strobe	Synchronizes the transfer on the system bus.
$SR/\overline{W}$	I	Read/write	Indicates the current system bus cycle state.
$\overline{DTACK}$	O	Data Transfer Acknowledge	Indicates that the processor has recognized it is being accessed.
BA	O	Bus Available	Indicates availability of the sytem bus to host.
$\overline{IRQ}$	O	Interrupt Request	Handshake signal sent to the master to gain access to the mailbox.

EXTERNAL BRANCH CONDITIONS

Name	Pin Type	Function	Description
BS (0:2)	I	Branch on State	External Conditions
BE (3:4)	I I	Branch on Edge	External Conditions. Falling edge is memorised and reset when tested.
BE5/BA	I/O		BE5 shares pin with BA.
BE6/DTACK	I/O		BE6 shares pin with DTACK.

OTHER PINS

Name	Pin Type	Function	Description
EXTAL	I	Clock	Crystal input pin for internal oscillator or input pin for external oscillator.
XTAL	I	Clock	Together with EXTAL it is used for crystal oscillator. If external oscillator is used, pin XTAL is not connected.
V_{DD}	I	Power Supply	
V_{SS}	I	Ground	
$\overline{RESET}$	I	Reset	

INSTRUCTION INTERFACE AND SYSTEM CONTROL INTERFACE (ST18931 only)

Name	Pin Type	Function	Description
ID (0:31) IA (0:15) CA (0:9)	I/O O O	Instruction Data Instruction Address Coef. ROM Address or External RAM Address	Instruction Bus. 32 Bit Data Instruction Address External Coefficient ROM Address 10 Bit OR External RAM Address (9-bit address – output enable signal) (8-bit address)
$\overline{HALT}$	I	Halt Signal	Halts the processor. This signal freezes the program and loop counters.
INCYCLE	O	Instruction Cycle Clock	A transition from low to high indicates that a new instruction is processed.

3. FUNCTIONAL DESCRIPTION

3.1. GENERAL ARCHITECTURE

The TS68930/31 architecture is based on an innovative architectural concep developped by SGS-THOMSON Microelectronics.

The TS68930 is compatible with the ST18930 and ST18940 other members of SGS-THOMSON digital signal processors family.

The TS68930 confirms the efficiency of a highly parallel and pipelined operation using a true Harvard memory space and bus structure.

The block diagram shows four main blocks :

. The sequencer block

. The operating unit (ALU, Multiplier and Barrel Shifter)

. The data memories

. The inputs/outputs

These four blocks can be considered as four independent units working in parallel and communicating through a network of 16/32 - bit buses.

By taking advantage of the 32 - bit wide instruction bus, the TS68930/31 are able to execute simultaneously the following operations during each machine cycle :

Read two operands from internal or external memory

. Execute a multiplication

. Perform an ALU operation

. Write a result into internal or external memory

. Post modify three pointers independently

. Store data into the transfer register

In addition, data exchanges through mailbox occur concurrently and independently of internal operations.

All instructions are executed in a single cycle time except branch instructions.

Some additional features give the TS68930/31 extremely powerful performances. They provide three operating modes (real, complex and double precision) dynamically set by software and user transparent.

In complex mode, the hardware multiplier provides (16 + 16 - bit) results from 2 x (16 + 16 - bit) inputs each machine cycle.

(12.5 - million multiplications per second).

The ALU, reinforced by a barrel shifter, provides 27 basic arithmetic and logic functions.

Three dedicated calculation units control the four data memory spaces.

A 1.28K x 32 program ROM (for the TS68930) allows most of digital signal processor applications possibilities, using the efficiency of the code and architecture. The following sections will detail all the hardware blocks of the TS68930/31 and demonstrate its software performances provided by the high level of parallelism in the operations.

3.2. OPERATING UNIT

One of the most useful features of the TS68930 is to provide the user three operating modes which can be dynamically set by software.

These three modes are :

. REAL 16-bit

. COMPLEX 16-bit real + 16-bit imaginary

. DOUBLE PRECISION 32-bit

Thus, the DSP is seen by the user as a standard 16 - bit real or complex machine or a 32-bit real machine. All operating units and working registers are automatically adjusted by the processor to the right length. In real mode, all instructions are executed in

a single machine cycle. In complex and double precision mode, the instruction time is doubled.

In all modes, the number representation used is signed 2's complement.

3.2.1. 16/32 - Bit ALU/Accumulator (fig. 2). The ALU can be seen either as a 16 or 32 - bit ALU. The ALU is loaded on the right side by the R - bus or by the A or B accumulators.

On the left side, the operands always access the ALU through the barrel shifter, coming either for the L (left) - bus or the hardware multiplier output register P.

The result of an ALU operation is automatically written in the D register and, if required into the Accumulator or FIFO. The ALU provides a range of 27 codes for operations which execute in a single machine cycle. They include arithmetic and logic operations, shift and rotate operations.

The high degree of parallelism of the TS68930/31 processor allows more combinations than previous generation DSP devices which require a more complex instruction set.

The complete list of ALU codes and description is given in 3.8.2.

3.2.2. Barrel Shifter. The 16-bit barrel shifter located on the left side of the ALU performs all logic/arithmetic shifts and rotations. It is used for normalization and formatting of data in floating point operations and bit or byte manipulations. Two types of operations are allowed in the barrel shifter.

- Operations defined by ALU codes (shifts of 1 or 8 bits) see 3.8.2
- Operations defined by specific dedicated instructions :

ASR ($0 \rightarrow 15$) arithmetic shift right by N ($0 < N \leq 15$)

LSR ($0 \rightarrow 15$) logical shift right by N ($0 < N \leq 15$)

LSL ($0 \rightarrow 15$) logical shift left by N ($0 \leq N \leq 15$)

ROR ($0 \rightarrow 15$) rotation right by N ($0 < N \leq 15$)

These codes allow all types of shifts from 0 to 15 bits.

3.2.3. Multiplier. The multiplier executes a 16 x 16-bit multiplication with a 32-bit result at each machine cycle. The operands are loaded into the M and N registers and the result of a previous multiplication is written in the P register during the same cycle.

The pipeline structure makes the multiplication result available with a delay of two instruction cycles.

The multiplier provides a multiplier overflow flag OVFM which is memorized in the status register in complex mode only (see 3.2.4).

The efficiency of the parallel pipeline operation of the multiplier is shown in fig. 3.

3.2.4. Associated registers. Registers A and B store the results from the ALU. They are sized according to the mode of operation. They also provide capability to feedback the ALU for a new operation with the ALU result of a previous operation.

Register FIFO.

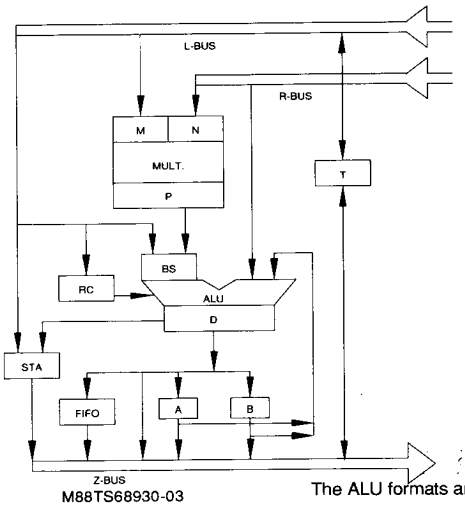
The 4 x 16-bit FIFO is used for intermediate storages. Initialization of the FIFO (empty FIFO) can be made by an INI instruction.

A result loaded in FIFO at instruction N is available at least at instruction N+2 in real mode and N+1 in complex and double precision modes.

Register RC (Replace Code register).

This register can dynamically load an ALU code to be executed by the processor from the data memories. It allows data control program sequencing without the use of a systematic test instruction. For instance, in FFT calculation, scanning may or may not be necessary during a pass.

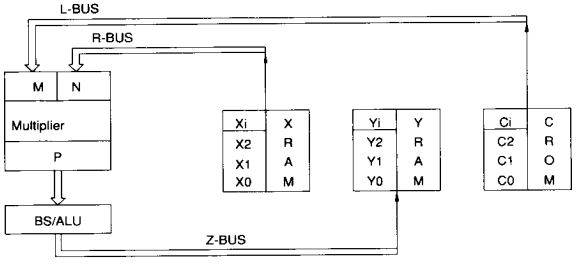
Figure 2 : Alu Block Diagram.



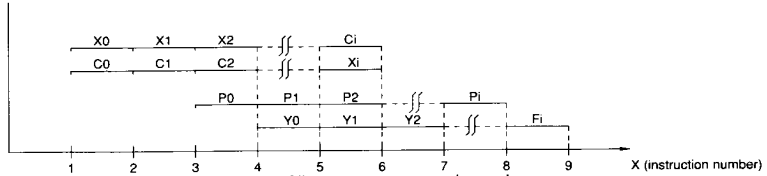
- 4 Inputs
  giving access to 10 possible sources :
  XRAM, YRAM,CROM, ERAM,
  P, T, RIN, A, B, FIFO
- 5 Destinations : A, B, D, FIFO, Z BUS
- R side by Accumulators
  L side by T registers
- 27 operations : including Arithmetic,
  Logic, Shifts,
  With 3 modes of execution :
  Real
  Complex
  Double precision
- Saturation mode to prevent overflow
- The status register gives information
  on the results of operations.
- The Replace Code Register allows dynamically changing the ALU operation code with a data.

The ALU formats are : 16-bit in Real mode
16 + 16-bit in Complex mode
32-bit in Double Precision mode

Figure 3 : Multiplier Efficiency.



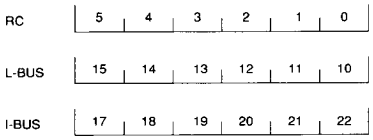
Yi=Xi.Ci



All components are always busy

M88TS68930-04

This register is 6-bit wide and is loaded by the 6 MSB of L-bus :



Bit 1 to 5 contain the executable ALU code corresponding to the bits I21-I17. Bit 0 allows the choice of ALU output destination (A or B register).

Its contents is defined by three ALU codes : (see 5.2.)

ALU Code	Function
RCR	Load ALU control code in register RC.
RCE	Execute ALU code contained in register RC.
RCER	Execute ALU code contained in RC and load new ALU code in RC.

Status register (STA).

This register provides a status of the ALU, operating and addressing modes, and multiplier. It is divided into two sub-registers :

CCR (Condition Code Register)
STR (State Register)

A detailed description of this register is given in δ 5.4.

Transfer register T.

The transfer register provides a direct transfer capability between L-bus and Z-bus.

It can either be source or destination for the two buses.

Its various uses include :

* Loop back to the multiplier in one cycle
* Temporary register between memory and ALU
* Temporary register between memory and multiplier
* Operation between two accumulators in the same instruction
* Memory to memory transfer
* Saving program counter (in a branch instruction)

The status register content can be saved using instruction SVR.

The condition code register CCR can be read in OPIN instruction and it can be loaded via L-bus (ALU code LCCR).

The state register STR can be programmed by an INI instruction or an SVR instruction (except EF bit).

3.3. DATA MEMORY BLOCKS.

3.3.1. Available spaces. The TS68930 provides four separated memory spaces (see fig. 4)

. two internal RAMs of 128 x 16-bit (YRAM and XRAM)

. one internal data ROM (independent from the program ROM) of 512 x 16-bit (CROM) (ST18930 only)

. one optional external memory (ERAM) of 4K x 16-bit accessible in one single instruction cycle in exactly the same way as internal memories.

This external memory is controlled by an Intel or Motorola type control interface and offers full speed, fully transparent, Read and Write operations.

Slower external memories or peripherals can be accessed by using slow exchanges modes.

However slower external memories or peripherals can be accessed by using slow exchanges mode.

The powerful instruction set and the Harvard architecture allows many combinations of simultaneous memory accesses. The only forbidden situations are :

- read and write access is the same RAM within the same instruction
- simultaneous access to CROM and ERAM

3.3.2. Address Calculation Units. Three different Addresses Calculation Units are available.

XACU is associated with XRAM

YACU is associated with YRAM

ECACU is associated with the ERAM and the CROM

3.3.3. Addressing modes. The TS68930 provides four addressing modes :

- Direct addressing
- Immediate operand
- Indirect addressing with or without post modification of the pointers
- Circular addressing (also called virtual shift mode) for XACU and YACU.

The circular addressing mode is of particular interest in digital signal processing typical operations like convolution algorithms used in FIR filters. It has the same function as a shift register but does not move the data stored.

For this feature, three pointers are used in the memory space chosen (X or Y). The current address is given by a specific X pointer shifting repetitively between two limits X0 and X1 (respectively Y, Y0 and Y1).

The circular mode is declared in the status register STA (see 3.2.4) by an INI instruction.

3.3.4. Pointers. The TS68930 offers a large number of address pointers for each memory space :

- X0, X1 and X for XRAM
- Y0, Y1 and Y for YRAM
- C0, C1 for CROM
- E0, E1 for ERAM

The pointers Xi, Yi, Ci and Ei can be independently incremented, decremented or maintained. The two pointers X and Y are specific to the circular addressing mode. The pointers can be loaded with new addresses (constant or computed values) through Z-bus. In this case, the value of unused Z-bus MSBs are irrelevant. The unused bits are set to 1.

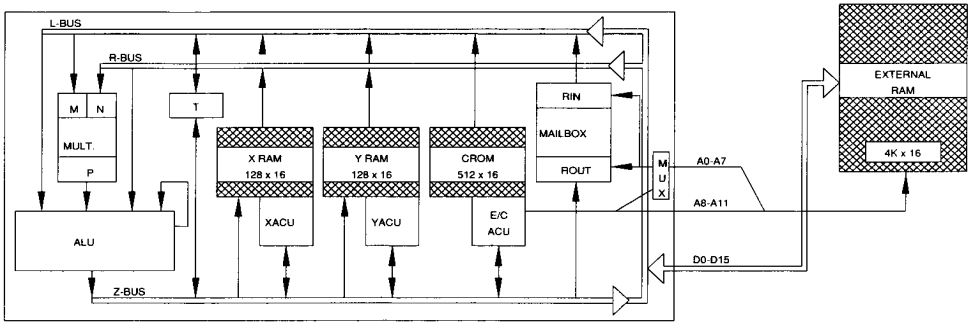
3.3.5 Odd/Even addresses. In complex and double precision modes, the processor automatically generates the two addresses necessary to store

one data word (even first, then odd addresses).

The user can reverse this order by setting to 1 the ADOF bit with the INI instruction (refer to OPCODE). This feature is available independently for XRAM and YRAM.

	COMPLEX WORD	DOUBLE PR. WORD
Even Address	Real Part	Lower Part
Odd Address	Imaginary Part	Upper Part

Figure 4 : Data Memory Blocks.



3.4. SEQUENCER BLOCKS

3.4.1. Sequencer. The purpose of the sequencer is to generate the next instruction address.

The sequencer takes into account the current operating mode of the TS68930/31 to execute this task. The instruction is executed in one cycle time in real mode and two cycles time in complex or double precision mode.

The linear address program generation may be interrupted by several means hereunder described.

A. Execution of a branch instruction
- unconditional branch always.
- seven ALU conditions flagged from the status register :

SR	Sign real
SI	Sign Imaginary
CR	Carry Real
CI	Carry Imaginary
Z	Zero
OVF	Overflow
MOVF	Memorized overflow MOVF is reset when tested by branch instruction.

- three external conditions on state of pins BS0, BS1, BS2 (the pins BS0, BS1, BS2 can also be used as interrupt pins if enable interrupt is programmed).
- four edge sensitive external conditions on pins BE3, BE4, BE5, BE6. The falling edges of BE3-BE6 are memorized internally and reset when tested by the branch instruction. The external test conditions are used to synchronize different processes.
- The mailbox flag RDYOIN indicating mailbox availability.

All the branch conditions can be tested on true or false conditions.

B. Subroutine call

C. Loop execution

One of the most powerful features of the TS68930/31 is its ability to repeat the execution of several instructions with very straightforward commands. The loop execution is set with the instructions : REPEAT, BEGIN, END which respectively define the number of loops, the beginning of loop and its end. The DSP will then manage all the necessary pointers to execute the loop with no overhead time (see 3.4.4.).

3.4.2. Instruction ROM. The TS68930 instruction ROM has a capacity of 1280 words of 32-bit available for the user. The ROM code is defined following the user's information (see appendix C for masking information). The TS68931 does not provide an on-chip ROM memory, but can address an external 64K program memory space in a single cycle.

3.4.3. Program Counter. The program counter is a 16-bit wide Register ; 12 bits are used in the TS68930 (ROM version).

3.4.4. Loop Counter. The loop counter does considerably increase the efficiency of the processor in repeated calculations, very commonly used in digital signal processing.

Three counters define a hardware loop :

- LCI Instruction Loop Counter (4-bit). Counts the number of instructions to be executed in the loop.
- LCR Repeat Loop Counter (8-bit). Gives the number of times the loop will be repeated (can be loaded by a calculated value).
- LCD Delay Loop Counter (3-bit). Gives the delay between the declaration and the start of a loop.

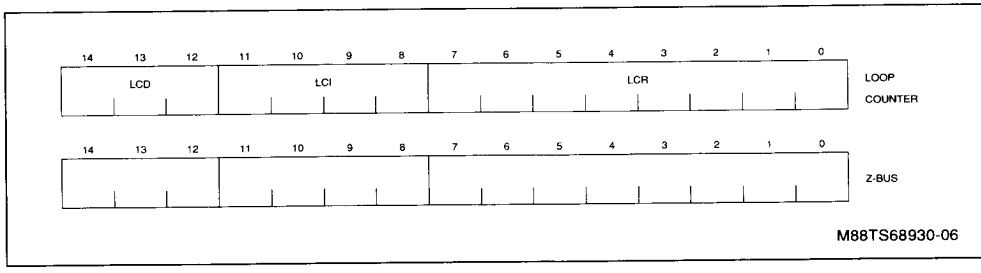
The loop counter content can be saved (SVR instruction) with the format shown in table below :

The loop counter is set by the three pseudo-instructions Begin, Repeat and End in the Macroassembler.

The loop counter is frozen during an interrupt routine.

On the TS68931, a HALT freezes the state of the loop counter. A RESET signal resets the loop counter.

3.4.5. Return Address Register. The JSR instruction allows one level of subroutine nesting with automatic saving of the PC on to the Return Address Register. Multiple Level of subroutine nesting can be implemented in RAM using either of the two pointers as stack pointer.



3.5. INPUTS/OUTPUTS

A very important feature of a signal processor is its ability to be inserted in a complete system including memories, other processes, analog interface circuits.

Basically, the external world seen by a TS68930/31 can be divided in two main sections : communications with its own local resources (peripheral, memories, converters) and communications with control processor, either microcontroller or master DSP in a multiprocessor application.

To communicate with its local resources, the TS68930/31 uses its local bus.

To interface with a host, the TS68930/31 uses its system bus and branch capabilities.

However, the local and system bus configuration is flexible and allows many combinations for the architecture of a system based around a TS68930/31.

3.5.2. Dual bus interface. In order to provide the maximum flexibility, the TS68930/31 provides two buses. One is called the system bus and is found on pins AD0-AD7, the other one called local bus is situated on pins D0-D15. The system bus provides a very straightforward interface to a host controller, while the local bus allows the TS68930/31 to make an efficient use of external resources such as memories, analog interface circuits etc... This dual bus structure allows many combinations of circuits where the TS68930/31 can act in different ways :

Fig. 6A as a microprocessor peripheral

Fig. 6B as a processor with its associated memory

Fig. 6C as an intelligent peripheral having its own external memory and connected to a microprocessor.

It must be emphasized that, in most configurations, the connections are absolutely direct and do not use any external additional logic.

Furthermore, thanks to the dual bus structure, several TS68930/31 can be very simply combined together in multiprocessor applications, thereby directly increasing the processing power.

Figure 6 A : HOST/TS68930.

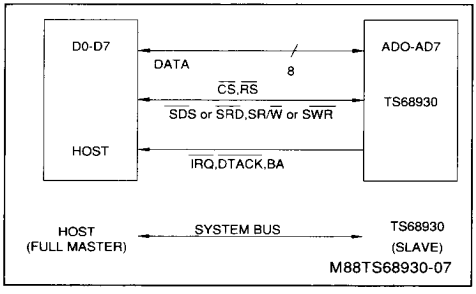


Figure 6 B : TS68930/RAM.

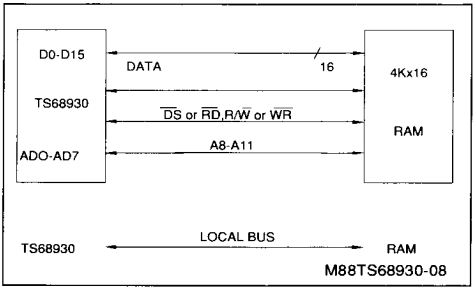
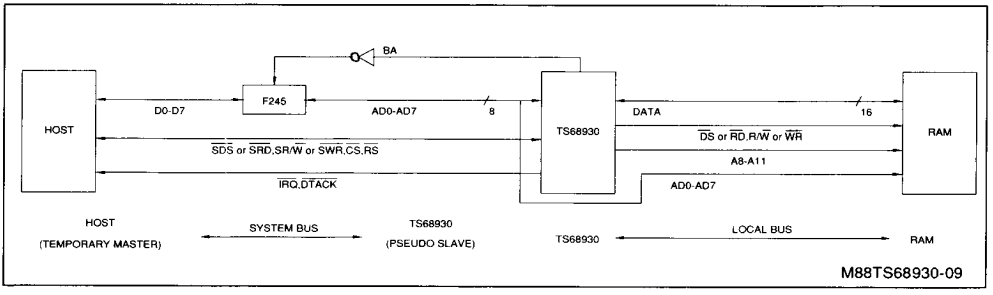


Figure 6 C : HOST/TS68930/RAM.



3.5.3. Host/slave configuration. The processor acts as a host on its local bus and as a slave on its system bus.

In configurations in which the TS68930 accesses external RAMS on its local bus, pins AD0-AD7 can be used to provide 8 LSB addresses, while A8-A11 provides 4 MSB addresses to the RAM.

In this case, the TS68930/31 prevents the host from using the system bus and is then called a pseudo-slave.

Since the host can only temporarily access the system bus it is defined as a temporary master. That mode of operation is software controlled through the Access Mode Register (AMR) (see 3.5.7.).

On the TS68931 the pins CA0-CA7, which present the least significant bits of external ERAM/CROM addresses can be connected to that RAM in place of system bus pins AD0-AD7.

3.5.4. Local bus. The local bus uses two software programmable signals to control the data on D0-D15.

$\overline{DS}$: Data Strobe. Synchronizes the transfer on local bus.

R/$\overline{W}$: Read/Write. Indicates the direction of the data.

These signals are used for Motorola-like bus compatibility.

$\overline{RD}$: Read. Read clock pulse.

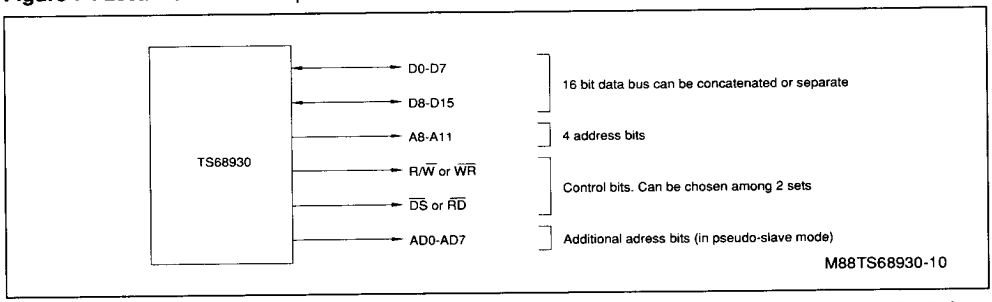
$\overline{WR}$: Write. Write clock pulse.

These signals are used for Intel-like bus compatibility.

A8-A11 : Address bits (4)

AD0-AD7 : Optional additional address bits (8)

Figure 7 : Local Bus Pin Description.



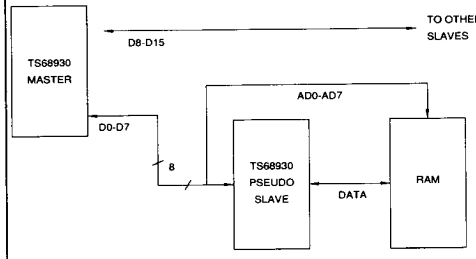
The four address bits of the local bus are usually sufficient to address peripherals. When an access to external RAM is necessary with the TS68930/31, the address bus can then be extended by using the AD0-AD7 pins of the system bus as address lines.

If an external peripheral or external memories are too slow to answer in one machine cycle, the TS68930/31 can be programmed to execute an external access in 2 cycles using the bits ES0 and ES1 of Access Mode Register (see 3.5.7.).

This mode is particularly useful for peripherals such as data converters, or dedicated interface like the MAFE chip set (Modem Analog Front End) from SGS-THOMSON.

The local data bus can also be splitted into two independent 8-bit buses. This is used in a multiprocessor architecture when a pseudo-slave uses the system bus to transfer its own RAM addresses on D0-D7 (fig. 8). By dividing its local bus, the temporary master can remain a full-master on bus D8-D15 and does not require a bus transceiver on D0-D7. The selection between the two buses is then made by the addresses A10-A11 as indicated in fig. 8.

Figure 8 : Separate Local Buses.



A_{11}	A_{10}	$D_0 - D_7$	$D_8 - D_{15}$
0	0	Selection	High Impedance
0	1	High Impedance	Selection
1	0	High Impedance	Selection
1	1	High Impedance	Selection

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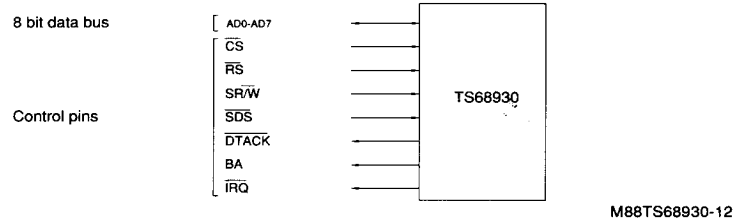
3.5.5. System Bus : The system bus uses two signals to control the data on AD0-AD7. The system bus mode of operation is Motorola like.

$\overline{CS}/\overline{RS}$	Mailbox Control Signal. Also used by a host to gain access to the bus.
$R/\overline{W}$ $\overline{SDS}$	System Read/Write System Data Strobe } Generated by an external processor (host).
$\overline{IRQ}$	Handshake Signal (see 3.5.6)
$\overline{DTACK}$	Data Transfer Acknowledge. Compatibility with 68000 family. Is programmed by Access Mode Register.
BA	Bus Available. The TS68930/31 is not currently using the system data bus to generate addresses. BA is also programmable by the Access Mode Register.

Figure 9 : System Bus Description.



protocol signal description.

RDYOIN.
Internal flag indicating the status of the mailbox
0 = DSP has access to the mailbox
1 = host has access to the mailbox

a. RDYOIN is set by the DSP and reset by the host. That means that the DSP gives the mailbox to the host when it finishes using it and vice-versa. In no case can the host or the DSP take possession of the mailbox, it can only wait for the other to give it back.

b. The TS68930/31 sees RDYOIN as a flag :
   - tested by a branch instruction
   - set to 1 by an initialization instruction in order to give the availability of the mailbox to the host.

$\overline{IRQ}$.
Handshake signal enabling the host to gain access to the mailbox.

a. $\overline{IRQ}$ is asserted low by the DSP to indicate the availability of the mailbox (at the same time as RDYOIN).

b. The host after testing $\overline{IRQ}$, knows that it can access the mailbox. The access to the bus (which can be currently used by the DSP as a local address bus) must be requested by reading the address $\overline{CS} = 0$, $\overline{RS} = 0$.

c. The DSP then answers back by asserting $\overline{IRQ}$ high. (In pseudo-slave mode, the DSP is halted). The host now has full control of the bus and mailbox.

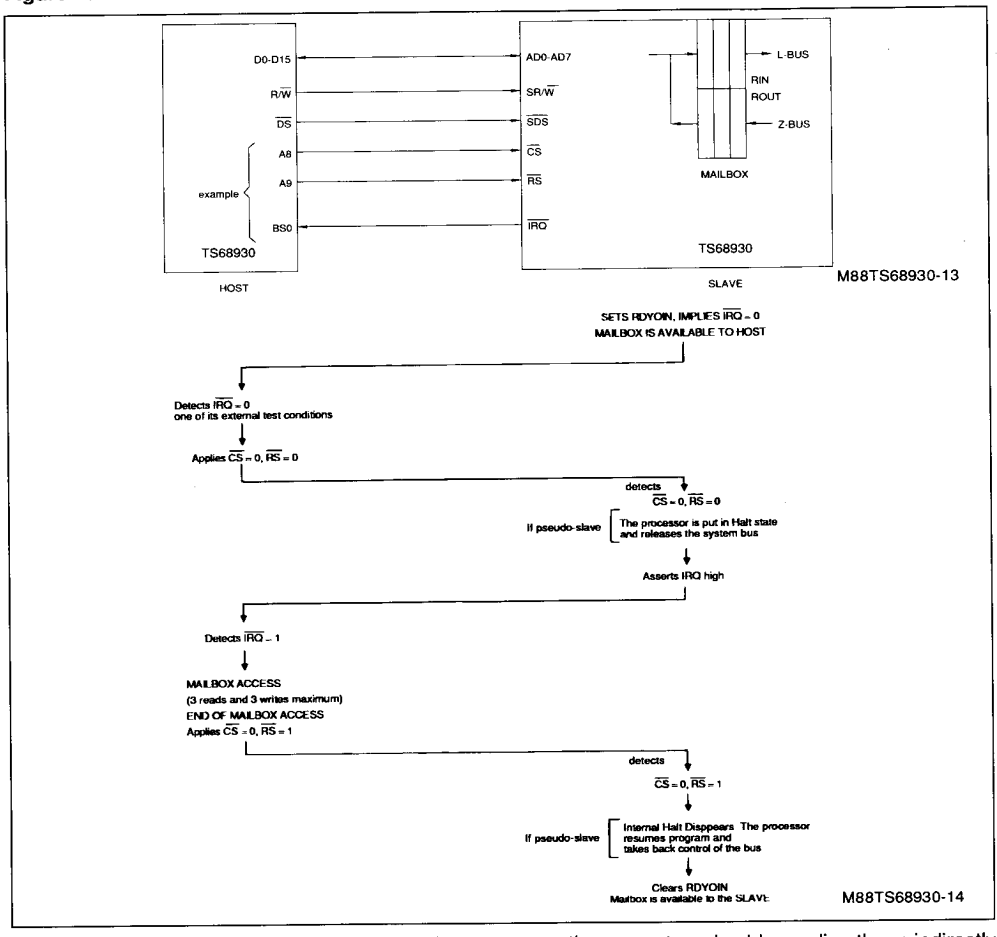
   When the host has completed the exchange it generates the address $\overline{CS} = 0$, $\overline{RS} = 1$ and the DSP resets RDYOIN.

HALT (internal).
The internal halt has the following effect on the circuit :
- the program is stopped at the end of the current instruction, the program and loop counter are frozen
- a NOP is executed
- no more addresses are generated on the system bus

3.5.6. Mailbox. The mailbox is a set of registers which interface with the system data bus. The mailbox is divided in two parts :

- RIN (3 x 8 bit register) : This register is read internally by the TS68930/31 on the upper byte of L-bus (L8-L15) and written externally from the system bus. After each write or read operation the data is shifted by one byte.
- ROUT (3 x 8 bit register) : This register is written internally with the upper byte of the Z-bus (Z8-Z15) and read externally on the system bus. After each operation (read or write), the data is shifted by one byte.

Figure 10 : Mailbox Connection and Protocol.



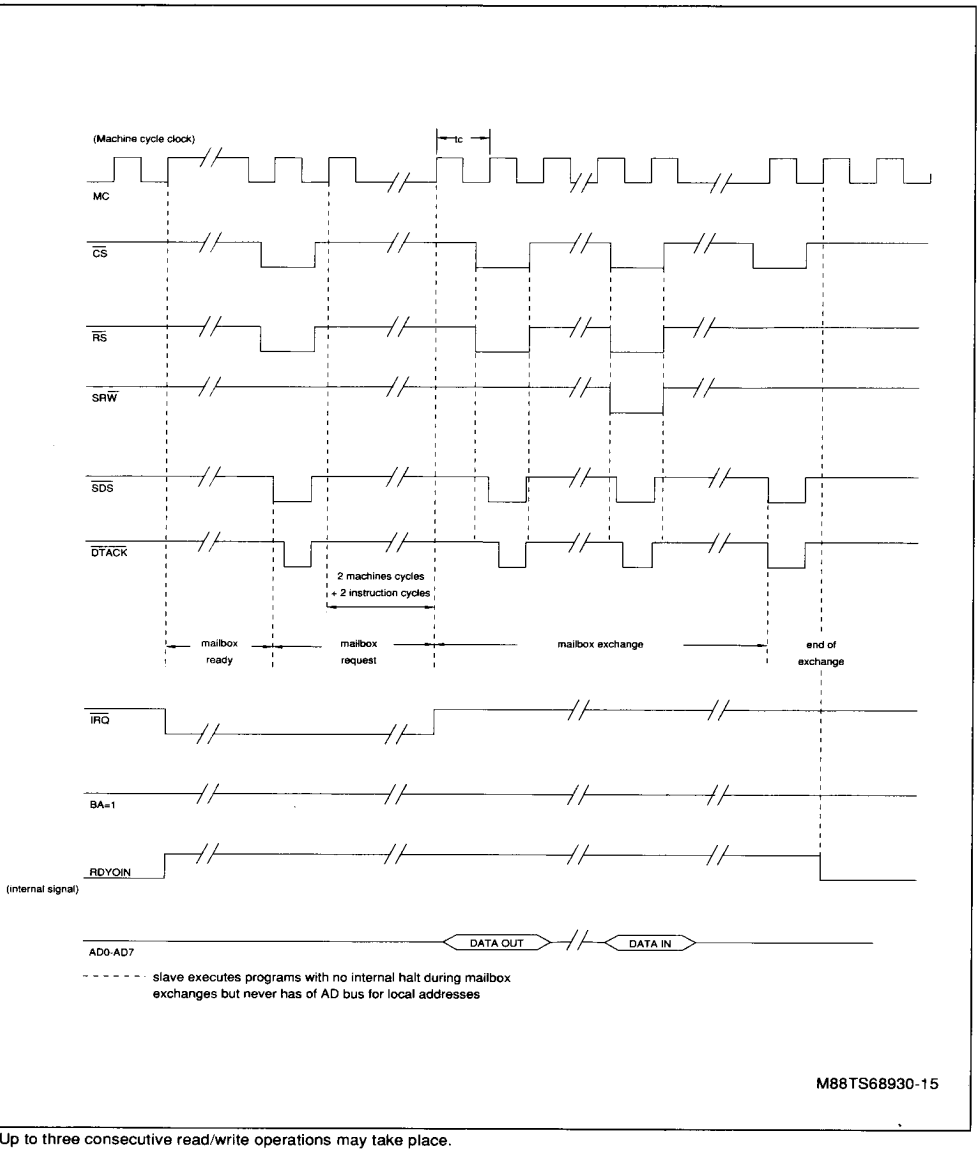
This protocol is hardwired on the slave side and programmed on the host side. The mailbox is included in the slave. The two slave address pins (CS, RS) are directly connected to two host address lines.

Therefore, the slave is seen as two external memory locations by the host which will address it by generating an external address directly or indirectly (pointer E0 or E1).

By addressing the location 00 the host echoes the IRQ to the slave and accesses the mailbox.

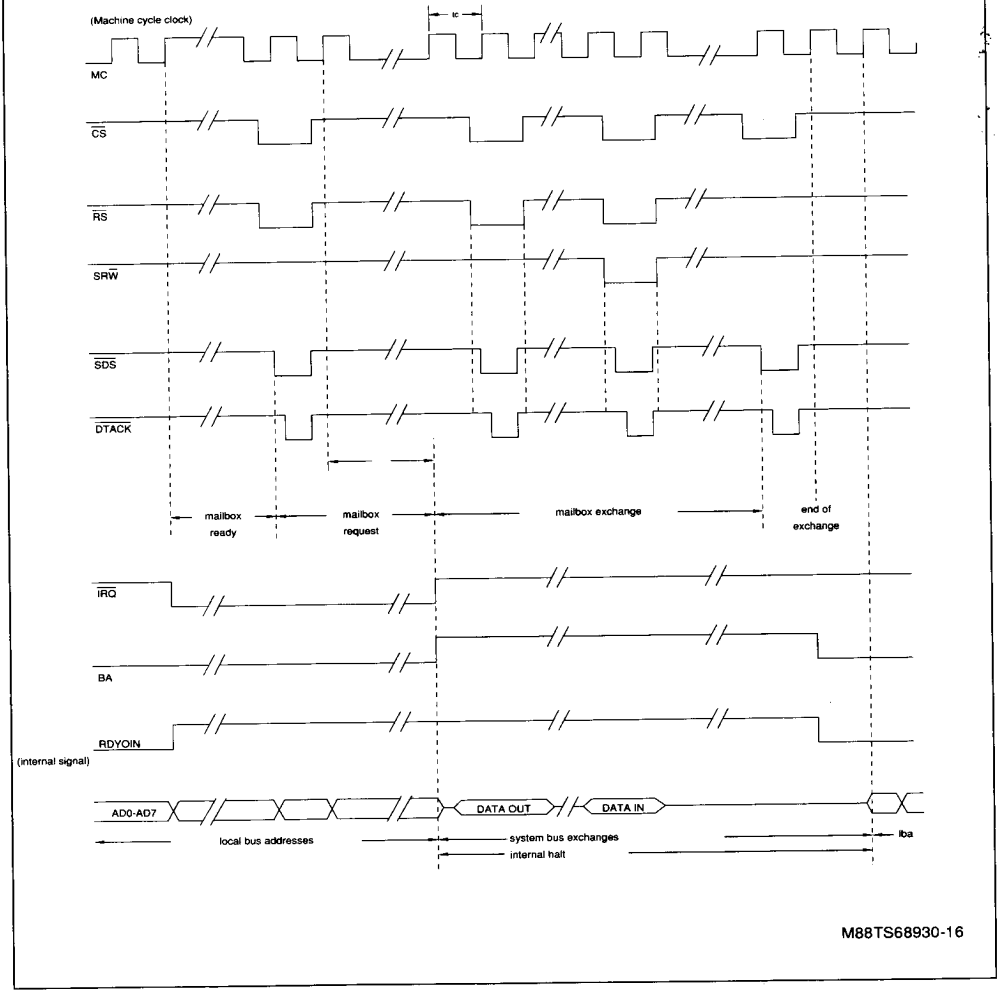
By addressing the location 01 the host releases the bus.

Figure 11.A : TS68930/31 Mailbox Exchange, Slave Mode.



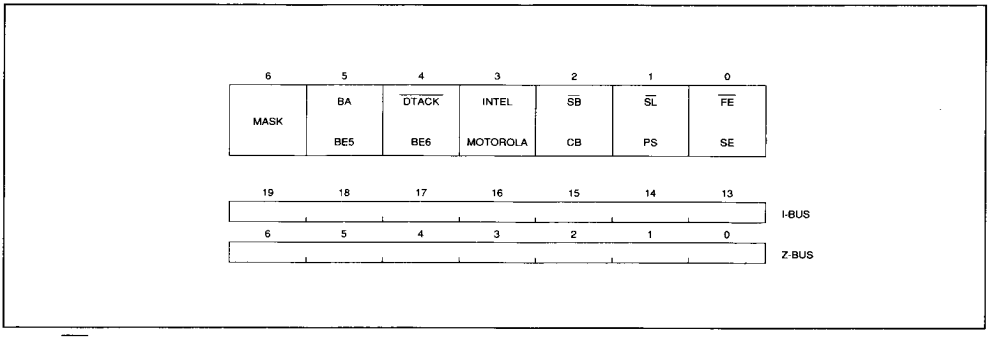
* Up to three consecutive read/write operations may take place.

Figure 11.B : TS68930/31 Mailbox Exchange, Pseudo Slave Mode.



3.5.7. Access Mode Register (AMR). The AMR is a 7-bit register which defines the processor external access modes.

It is loaded by an INI or SVR instruction and saved by an SVR instruction. Its fields are defined as follows :



Bit 0 : FE/SE

This bit defines Fast Exchange in one cycle to access external resources when low. Or slow exchange in two cycles when high. The slow exchange mode can only be used in the real mode. The circuit automatically repeats the instruction which defines the external transfer. The control of the multiplier, ALU, ACU, loop counter is the responsibility of the programmer who must take into account the repetition of the instruction.

Bit 1 : SL/PS.

0 = Slave.
1 = Pseudo-slave.

This bit defines the behaviour of the TS68930/31 regarding the system bus (AD0-AD7). In slave mode, the processor will never use the system bus as local bus address.

In pseudo-slave, the processor uses address bus (AD0-AD7) for local resources. These bits will be concatenated with A8-A11 bits of the local bus to form a 12-bit address bus for larger external memory spaces. The pseudo-slave will then address an external RAM with LSB's address on AD0-AD7 and MSB's on A8-A11. After an exchange the TS68930 in pseudo-slave mode must relinquish the master (see 3.5.3. - Master/slave configuration).

Bit 2 : SB/CB.

0 = Separated bus.
1 = Concatenated bus.
This bit indicates whether the local bus is used as a 16-bit concatenated bus or as 2 independent 8-bit buses.
(see 3.5.4. - local bus description).

Bit 3 : I/M.

0 = Control pulses Read (RD) and Write (WR) are generated. This is the case with an Intel type peripheral or a standard byte-wide RAM.
1 = Control pulses data strobe (DS) and Read/Write (R/W) are generated.

This is the case for exchanges with a slave processor, a 68000 type peripheral, a data converter such as TS7542 or the M.A.F.E. chip set (TS68950/51/52).

Bit 4 : DTACK/BE6.

The TS68930 does acknowledge correct access by generation of a DTACK output. In this case, the BE6 pin is not available for an external test condition.

Bit 5 : BA/BE5.

This bit low configurates the pin BA/BE5 as bus available output (BA) indicating to the master that the pseudo-slave is not using the system bus for generating addresses on the local bus. When high, it is used as an external test condition (BE5).

Bit 6 : MASK (TS68931 only).

When this bit is low, an external Halt applied to the processor will not change the values in the ARM register. When high, an external Halt applied to the processor will reset the ARM register with following configuration :

ONE CYCLE EXCHANGE, PSEUDO-SLAVE, CONCATENATED BUS, RD AND WR CONTROL PULSES.

This bit can be modified by the programmer even while the HALT is asserted.

3.5.8. Instruction interface and system control (TS68931 only). On the TS68931, the coefficient ROM and the instruction ROM (CROM & IROM) are external. The device provides the necessary buses to access these data. Instructions are read on ID0 : ID31 using IA0-IA15 for addressing. Coefficients are read on local address bus D0-D15 using CA0-CA8 for addressing. CA9 is at low level for address validation. CA0 : CA7 also contains external RAM addresses (if necessary) associated with a high level for CA9.

So, for the TS68931, there is no need of a pseudo slave mode as AD0:AD7 remain available for data transfer on the system bus. Clock signals are also provided for interfacing purposes (3.6.1.).

3.5.9. Halt (TS68931 only). The external $\overline{\text{HALT}}$ signal will freeze the program counter, the loop counter. The instruction register can then be loaded from an external source. This signal is used for system development. If the MASK bit = 1 then it will force the AMR into the following configuration :

ONE CYCLE EXCHANGE, PSEUDO SLAVE, SEPARATE BUS, RD AND WR CONTROL PULSES.

3.6. OTHER RESOURCES

3.6.1. Clock generators. Different clock outputs are available on the TS68931 and on the TS68930.

CLKOUT : available on TS68930 and TS68931.

INCYCLE : available on TS68931 only.

The CLKOUT output period is function of the EXTAL period and is half the frequency of the input clock.

The INCYCLE output is equal to machine cycle in real mode and half of machine cycle in complex and double precision mode.

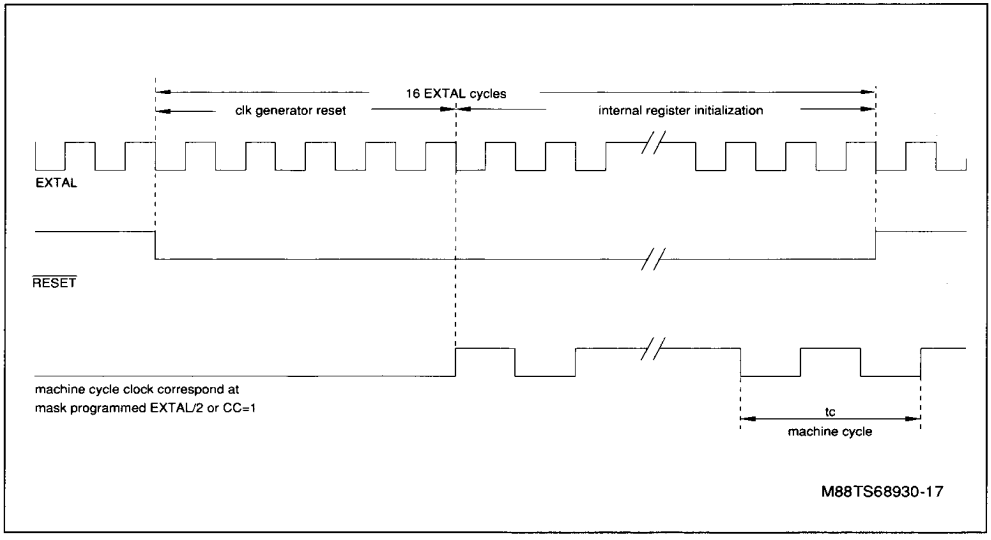
3.6.2. Reset. The reset signal acts on several processors blocks as follows :

- Sequencer : the program counter (PC) and the loop counter (LC) are cleared to zero. The instruction register is loaded with NOP instruction.
- Status register : set in real mode, no saturation, empty FIFO (EF = 1), memorized overflows (MOVF = 0), and XRAM and YRAM in non circular addressing mode.
- Access Mode Register (AMR) : set for one cycle external exchange, slave mode, concatenated bus, RD and WR, BE5 and BE6, SDS and SR/W.

The reset signal must be maintained for a minimum of 16 cycles of EXTAL signal .

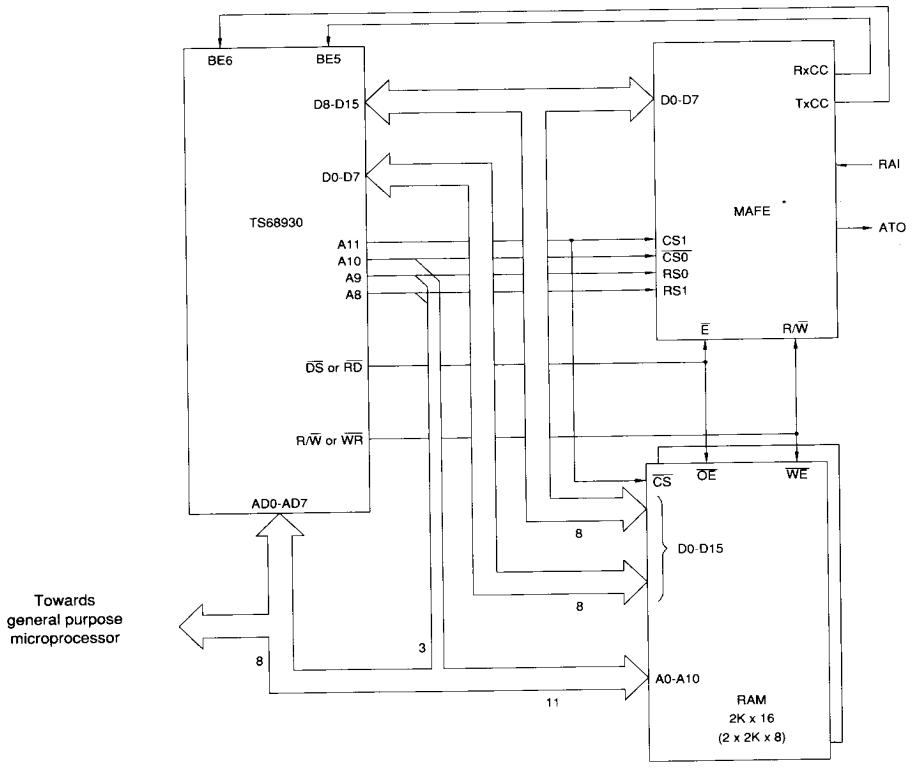
3.6.3. Watchdog capability. The watchdog prevents the processor from staying locked in an undesired state or internal loop caused by adverse conditions such as high-voltage transients. The circuitry includes a 2-bit counter which is incremented by each falling edge on BE3 input and reset by software testing of any of the BE3 conditions. If three falling edges of BE3 input occurs without a test of the condition, the TS68930 is reset by the watchdog circuit. This capability is a mask option of the TS68930 which is chosen (or not) by the user.

Figure 12 : Reset Timing.



4. TYPICAL APPLICATION CONFIGURATIONS

Figure 13 : Configuration Example with TS68930 + RAM + MAFE*.



A_{11}	A_{10}	A_9	A_8	
1	0	X	X	**MAFE**
0	X	X	X	**RAM**

* MAFE is the TS68950/51/52 Modem Analog Front – End Chip Set.

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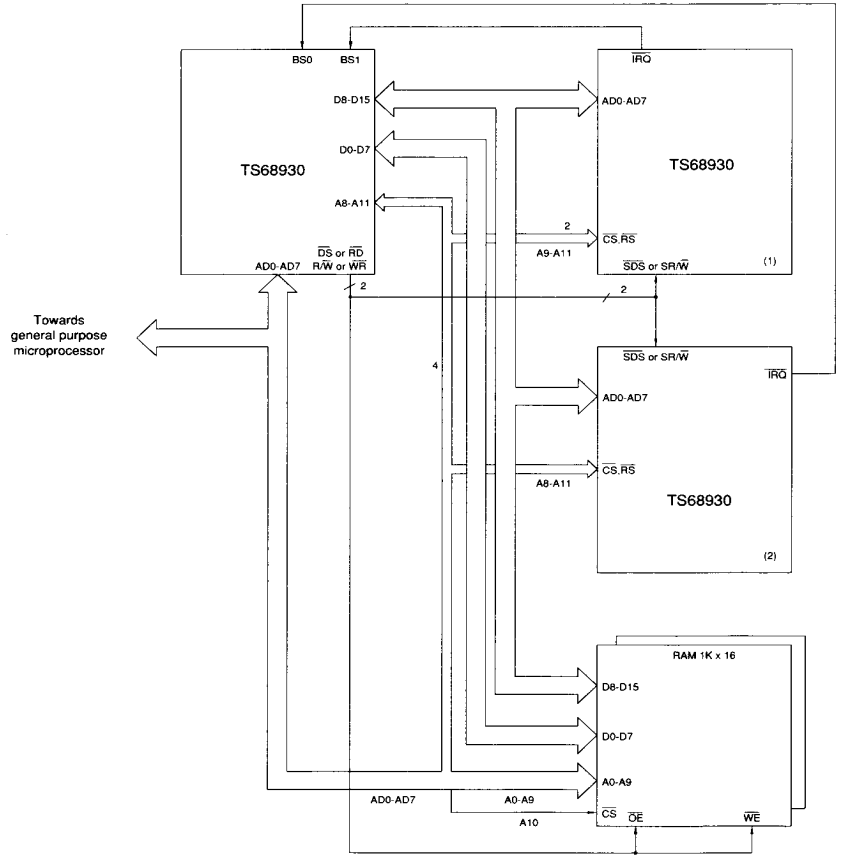
Figure 14 : Configuration Example : 3 TS68930 + RAM.



A_{11}	A_{10}	A_9	A_8	
0	1	0/1	1	**TS68930** (1)
0	1	1	0/1	**TS68930** (2)
1	0	X	X	**RAM**

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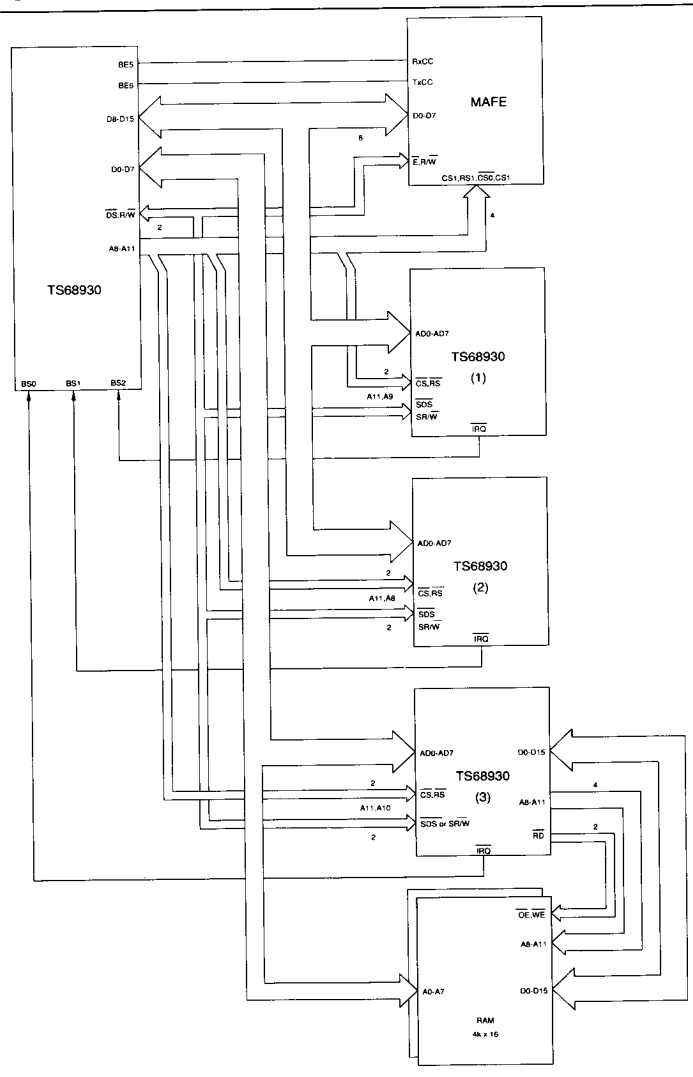
Figure 15 : Configuration Example 4 TS68930 + MAFE + RAM.



A_{11}	A_{10}	A_9	A_8	
1	0	X	X	**MAFE**
0	1	0/1	1	**TS68930** (1)
0	1	1	0/1	**TS68930** (2)
0	0/1	1	1	**TS68930** (3)

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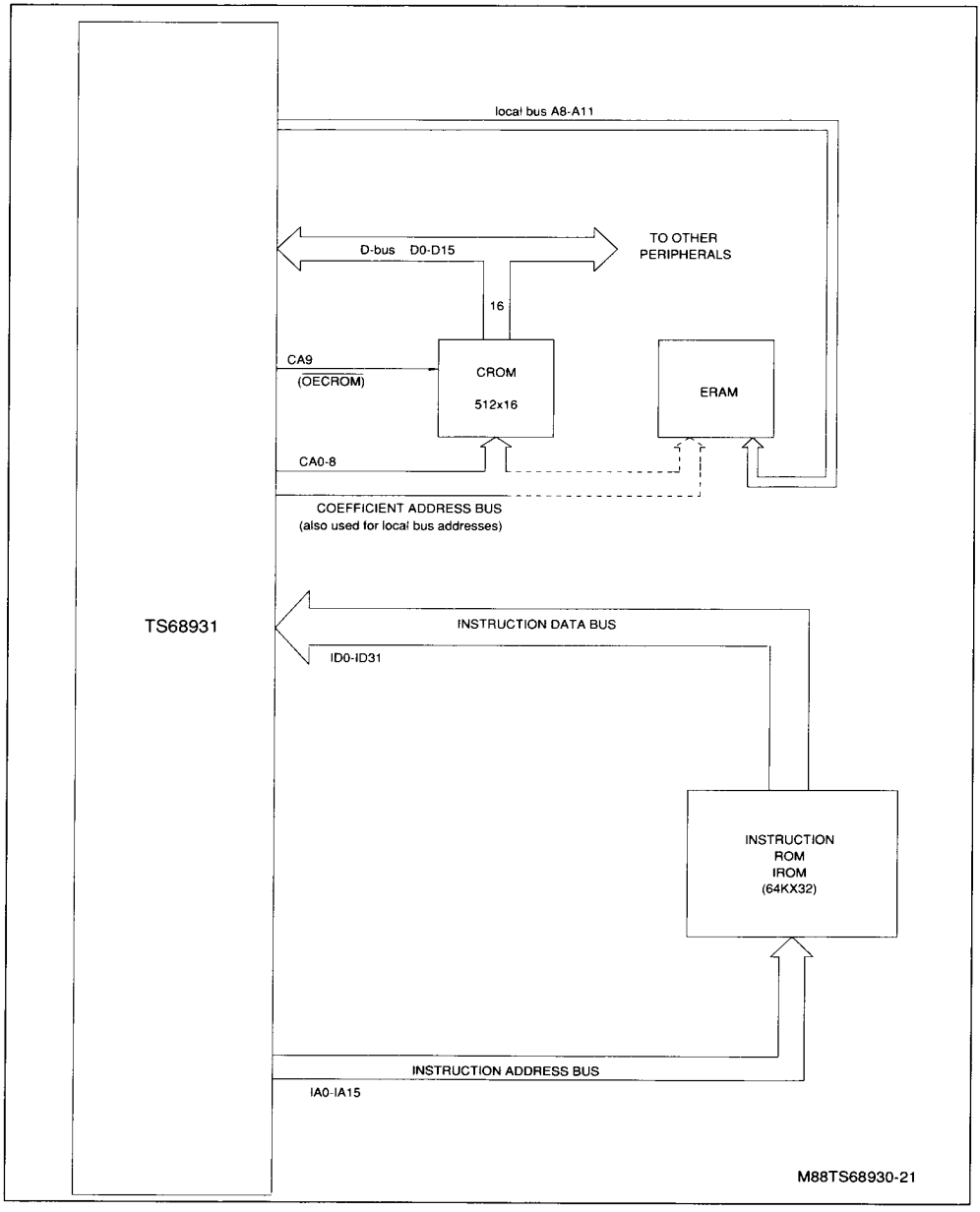
Figure 16 : Interfacing CROM, IROM to ST18931.



5. INSTRUCTION SET

Symbol	Type	Operation	Number of Cycles	
			REAL	CPLX DBPR
OPIN	Calculation Instruction with Indirect Addressing	This instruction refers to operands indirectly addressed.	1	2
OPDI	Calculation Instruction with Direct Addressing	The operand sourcing the L-BUS is directly addressed.	1	2
OPIM	Calculation Instruction with Immediate Operand	An immediate operand is read on R-BUS.	1	2
ASR ASL LSR ROR	General Shift Instruction	The operand sourcing the L-BUS can be shifted/rotated by 0 → 15 bits.	1	2
BRI	Immediate Branch Instruction	Conditional/unconditionnal branch to direct address.	2	2
BRC	Computed Branch Instruction	Conditional/unconditional branch to computed address.	2	2
SVR TFR	Data Transfer Instruction	This instruction is used to save register contents in external or internal RAM.	1	2
INI	Initialization and Control Instruction	Pointers, acces mode register, loop counter, mode initialization.	1	2

INSTRUCTION SET LANGUAGE DEFINITIONS

LDT	Load L-BUS source into Transfer Register T
R SRC	R-BUS Source
L SRC	L-BUS Source
SL	ALU Input Selection Left Side
SR	ALU Input Selection Right Side
ALU DST	ALU Output Destination
ALU CODE	ALU Codes
LDM	Load L-BUS Source into Multiplier Input M
LDN	Load R-BUS Source into Multiplier Input N
Z SRC	Z-BUS SOURCE
Z DST	Z-BUS DESTINATION
ZT	Load Z-BUS into Transfer Register T
ACE	Post Incrementation Pointers CROM or ERAM
AY	Post Incrementation Pointers YRAM
AX	Post Incrementation Pointers XRAM
BRA	Branch Address Source
FT	False/true Condition
SVPC	Save Program Counter
JDST	Destination Register for J Constant
KDST	Destination Register for K Constant
MODE	Operating Mode
SAT	Saturation Flag
ADOF	Ever add Flag
J Constant	8-bit Constant used to initialize registers
K Constant	12-bit constant used to initialize registers

5.1 OPERATING CODE FORMATS

Fig. 17 : OPIN : Calculation Instruction with Indirect Addressing.

Bit	Field	Operations and Codes
31 30	OP CODE	00
29	LDT	0-NO LOAD, 1-LBUS → T
28 27	R SRC	00 01 10 11 (X0) (E0) (Y0) (Y1)
26 25 24	L SRC	000 001 010 011 100 101 110 111 (X0) (X1) (Y0) RIN T (E1) (C0) (C1)
23	SL	0-LBUS / 1-P
22	SR	0-RBUS / 1-A/B (refer to ALU DST)
21 20 19 18 17	ALU CODE	cf. Special Table
16 15	ALU DST	00 01 10 11 D F A B
14 13 12	Z SRC	000 001 010 011 100 101 110 111 D F A B T CCR – –
11	LDM	0-NO LOAD / 1-LBUS → M
10	LDN	0-NO LOAD / 1-RBUS → N
9 8	ACE	00 01 10 11 + 0 + 1 – – 1
7 6	AY	00 01 10 11 + 0 + 1 – – 1
5 4	AX	00 01 10 11 + 0 + 1 – – 1
3 2 1	Z DST	000 001 010 011 100 101 110 111 NONE ROUT (Y0) (Y1) (E0) (E1) (X0) (X1)
0	ZT	0-NO LOAD / 1 ZBUS → T

Fig. 18 : OPDI : Calculation Instruction with Direct Addressing.

Bit	Field	Operations and Codes
31 30 29	OP CODE	010
28 27	R SRC	00 (X0) 01 (E0) 10 (Y0) 11 (Y1)
26 25 24	L SRC	000 X 001 – 010 Y 011 RIN 100 T 101 E 110 – 111 C
23	Z SRC	0-D / 1-F
22	SR	0-RBUS / 1-A
21 20 19 18 17	ALU CODE	cf. Special Table
16	ALU DST	0-F / 1-A
15 14 13 12 11 10 9 8 7 6 5 4	LBUS DIRECT ADDRESS	MSB LSB
3 2 1 0	Z DST	0000 NONE 0010 ROUT 0100 (Y0) 0110 (Y1) 1000 (E0) 1010 (E1) 1100 (X0) 1110 LCR 0001 X0 0011 X1 0101 Y0 0111 Y1 1001 E0 1011 E1 1101 C0 1111 C1

Fig. 19 : OPIM : Calculation Instruction with Immediate Operand.

Bit	Field	Operations and Codes
31 30 29 28 27	OP CODE	01110
26 25 24	L SRC	000 (X0) 001 (X1) 010 (Y0) 011 RIN 100 T 101 (E1) 110 (C0) 111 (C1)
23	SL	0-LBUS / 1-P
22	SR	0-RBUS / 1-A
21 20 19 18 17	ALU.CODE	cf. Special Table
16	ALU DST	0-F / 1-A
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	IMMEDIATE VALUE	MSB LSB

Fig. 20 : ASR, LSL, LSR, ROR, Shift Instructions.

Bit	Field	Operations and Codes	
31 30 29 28 27	OP CODE	01111	
26 25 24	L SRC	000 001 010 011 100 101 110 111 X – Y RIN T E – C	
23	SL	0-LBUS / 1-P	
22 21	ALU CODE	00 01 10 11 ASR LSL LSR ROR	**NOTE** : When LSR, ASR, ROR shift value is complemented to 2.
20 19 18 17	SHIFT VALUE	0000 0001 ..... 1111 0 1 15	
16	ALU DST	0-F / 1-A	
15 14 13 12 11 10 9 8 7 6 5 4	LBUS DIRECT ADDRESS	MSB LSB	
3 2 1 0			

Fig. 21 : BRI : Branch Immediate Instruction.

Bit	Field	Operations and Codes
31 30 29	OP CODE	100
28	BRA	0-IR, 1-RAS
27	FT	0-FALSE, 1-TRUE
26 25 24 23	COND	CF Special Table
22	SVPC	0-NO SVPC, 1-PC → RAS*
21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	BRANCH ADDRESS	MSB LSB
5 4	AX	00 01 10 11 + 0 + 1 – – 1
3 2 1	Z DST	000 001 010 011 100 101 110 111 NONE – [Y0] [Y1] – – [X0] [X1]
0	ZT	0 NO LOAD, 1-ZBUS → T

* The PC write operation in X or YRAM (defined by Z DST) is realized if the branching is really executed.

Fig. 22 : BRC : Branch Computed Instruction.

Bit	Field	Operations and Codes
31 30 29 28	OP CODE	1010
27	FT	0-FALSE, 1-TRUE
26 25 24 23	COND	CF Special Table
22	SVPC	0-NO SVPC, 1-PC → RAS*
21 20		
19	RTI	0-NO RTI, 1-RAS → PC
18 17 16		
15 14 13 12	BRANCH SOURCE	000 001 010 011 100 101 110 111 NONE F A B T – – –
11 10 9 8 7 6		
5 4	AX	00 01 10 11 + 0 + 1 – – 1
3 2 1	Z DST	000 0001 010 011 100 101 110 111 NONE – [Y0] [Y1] – – [X0] [X1]
0	ZT	0-NO LOAD, 1-ZBUS → T

* See BRI.

Fig. 23 : SVR : Data Transfer Instruction.

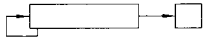
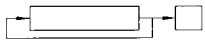
Bit	Field	Operations and Codes
31 30 29 28 27 26	OP CODE	011000
25 24 23 22	Z SRC	0000 0001 0010 0011 0100 0101 0110 0111 X0 X1 Y0 Y1 E0 E1 C0 C1 1000 1001 1010 1011 1100 1101 1110 1111 AMR LC A F D STA B –
21 20 19 18 17 16		
15 14 13 12 11 10 9 8 7 6 5 4	ZBUS DIRECT ADDRESS	MSB LSB
3 2 1	Z DST	000 001 010 011 100 101 110 111 NONE ROUT Y AMR E STR X –
0	ZT	0-NO LOAD, 1-ZBUS → T

Fig. 24 : INI : Initialization and Control Instruction.

Bit	Field	Operations and Codes			
31 30	OP CODE	11			
29 28 27	J DST	000 001 010 011 100 101 110 111 AMR LCD Y0 Y1 CRR EN* EF NONE			
26 25 24	K DST	000 001 010 011 100 101 110 111 X0 X1 LCI-LCR NONE E0 E1 C0 C1			
23 22	MODE	00 01 10 11 – REAL DBPR CPLX			
21	SAT	0 NO SATURATION MODE		1 SATURATION MODE	
20	AD0F	0 NO INVERSION		1 INVERSION LSB ADDRESS X/Y RAM	
19	J7	J7 0 YRAM NORMAL MODE		1 YRAM CIRCULAR ADDRESSING MODE	
18 17 16 15 14 13 12	J6 J5 J4 J CONSTANT J3 J2 J1 J0	(if EN) (if EN) (if EN)	0X EI = N/C 10 EI = 0 11 EI = 1	OX SIM = N/C 10 SIM = 0 (INTEL) 11 SM = 1 (MOTOROLA)	0 RDY O/N = N/C 1 RDY O/N = 1
11 10 9 8 7 6 5 4 3 2 1 0	K11 K CONSTANT K0	K7 0 XRAM Normal Mode		1 XRAM Circular Addressing Mode	

* EN (Enable) code (101) is a multi–function condition permitting independant programming of RDYOIN and SIM flags, and STA register bit EI in J field of the INI instruction.

5.2 ALU CODES

MNEMO	Function	SR	SI	CR	CI	Z	OV F	MO VF	AO VF	Code (I17-I21)
ADD	A + B	*	*	*	*	*	*	*	*	00010
ADDC	A + B + CARRY	*	*	*	*	*	*	*	*	00011
ADDS	B + A/16	*	*	*	*	*	*	*	*	00001
ADDX	B + A* (COMPLEX CONJUGATE)	*	*	*	*	*	*	*	*	01010
AND	A • B	*	*	0	0	*	0		*	01110
ASL	CARRY  0	*	*	*	*	*	*		*	01011
ASR	 CARRY	*	*	*	*	*	0		*	01111
CLR	CLEAR	0	0	0	0	1	0		0	10011
COM	COMPLEMENT A	*	*	0	0	*	0		*	10110
COM	COMPLEMENT B	*	*	0	0	*	0		*	11000
LCCR	LBUS –> CCR	*	*	*	*	*	*	*	*	01001
LSL	CARRY  0	*	*	*	*	*	0		*	11011
LSLB	LSL BYTE	*	*	*	*	*	0		*	11001
LSR	0  CARRY	*	*	*	*	*	0		*	00111
LSRB	LSR BYTE	*	*	*	*	*	0		*	11010
NOP										00000
OR	A ∧ B	*	*	0	0	*	0		*	01101
RCE	EXECUTE RC	*	*	*	*	*	*	*	*	10001
RCER	EXECUTE RC / LOAD NEW CODE	*	*	*	*	*	*	*	*	10000
RCR	LOAD RC									10010
ROR	 CARRY	*	*	*	*	*	0		*	10111
SBC	A + $\overline{B}$ + CARRY	*	*	*	*	*	*	*	*	00101
SBCR	$\overline{A}$ + B + CARRY	*	*	*	*	*	*	*	*	01000
SET		*	*	0	0	0	0		0	11100
SUB	A + $\overline{B}$ + 1	*	*	*	*	*	*	*	*	00100
SUBR	$\overline{A}$ + B + 1	*	*	*	*	*	*	*	*	00110
TRA	TRANSFER A	*	*	0	0	*	0		*	10100
TRA	TRANSFER B	*	*	0	0	*	0		*	10101
XOR	A ⊕ B	*	*	0	0	*	0		*	01100
SUBS	B + $\overline{A}$/16 + 1	*	*	*	*	*	*	*	*	11101

Notes : 1. A B refer to ALU inputs (respectively LSIDE, RSIDE) not to accumulators A/B.
2. In ASL the OVF bit is equivalent to exclusive OR of bit 14 and 15.

5.3. TEST CONDITIONS

True Condition	False Condition	Code
BE3	No BE3	0100
BE4	No BE4	0010
BE5	No BE5	0011
BE6	No BE6	0001
Branch Always	Branch Never	0000
BS0	No BS0	1100
BS1	No BS1	1101
BS2	No BS2	1110
CI	No CI	1010
CR	No CR	0110
MOVF	No MOVF	1011
OVF	No OVF	0111
RDYOIN	No RDYOIN	1111
SI	No SI	1001
SR	No SR	0101
Z	No Z	1000

5.4. AMR AND STA REGISTERS

AMR (Access Mode Register)

6	5	4	3	2	1	0
MASK	BA BE5	$\overline{\text{DTACK}}$ BE6	T M	$\overline{\text{SB}}$ CB	$\overline{\text{SL}}$ PS	SE0

STA (Status Register)

15	14	13	12	11	10	9	8	7	6	5	4 3	2	1	0
SR	SI	CR	CI	Z	OVF	MOVF	AOVF	OVFM	EF	SAT	MODE	XC	YC	
CCR									STR					

CONDITION CODE REGISTER (CCR)

Name	Function	Description
SR	Sign Real	Set if the MSB of the ALU result is 1. Cleared otherwise.
SI	Sign Imaginary	Set if the MSB of the ALU imaginary result is 1 (in complex mode). Cleared otherwise.
CR	Carry Real	Set if a carry is generated out of the MSB of the result for arithmetic and shift operations. Cleared otherwise.
CI	Carry Imaginary	Set if a carry is generated out of the MSB of the imaginary part of the result for complex arithmetic and shift operations. Cleared otherwise.
Z	Zero	Set if the ALU result equals zero. In complex mode it is set if both real and imaginary parts are equal to zero.
OVF	Overflow	Set if there was an arithmetic overflow. This implies that the result cannot be represented in the operand size. In complex mode it is set for an overflow of either real or imaginary part. Cleared otherwise.
MOVF	Memorized Overflow	Set in the same conditions as overflow. Is cleared only when tested by a branch instruction.
AOVF	Advanced Overflow	Exclusive OR of bit 14 and 15 of the ALU. If there was an arithmetic overflow on half capacity (15 bits in real/complex mode, 31 bits in double precision mode). Is memorized and cleared by LCCR ALU instruction.
OVFM	Overflow Multiplier	Set if the multiplier has overflowed. Only meaningful for complex multiplication. Is memorized and cleared by LCCR ALU instruction.

STATE REGISTER (STR)

Name	Function	Description
EF	Empty FIFO	Set if FIFO is empty. Cleared otherwise.
SAT	Saturation Flag	Set if the TS68930 is programmed in saturation mode. In this configuration, the processor will behave as follows : Positive overflow : ALU result forced to 7FFF. Negative overflow : ALU result forced to 8000. This feature does not apply to double precision mode. This bit is cleared otherwise.
MODE (2bits)	Operating Mode	Define a real (01), complex (11) or double precision (10) mode.
XC	XRAM Circular	Circular addressing mode flag for XRAM. (see 3.3.3)
YC	YRAM Circular	Circular addressing mode flag for YRAM. (see 3.3.3)

6. ELECTRICAL SPECIFICATIONS

6.1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	– 0.3 to 7.0	V
V_{in}*	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
P_{Dmax}	Maximum Power Dissipation	3	W

With respect to Vss

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

6.2. DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 °C to + 70 °C (unless otherwise specified)

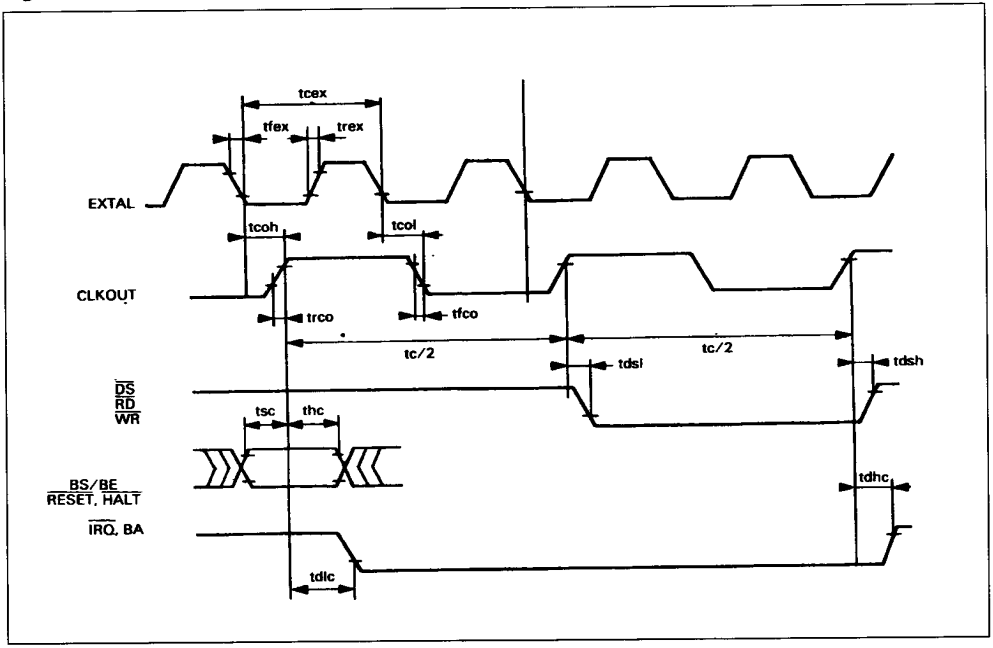
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	– 0.3		0.8	V
V_{IH}	Input High Voltage	2.4		V_{CC}	V
I_{in}	Input Leakage Current			10	µA
V_{OH}	Output High Voltage (I_{load} = – 300 µA)	2.7			V
V_{OL}	Output Low Voltage (I_{load} = 3.2 mA)			0.5	V
P_D	Power Dissipation		1.5		W
C_{in}	Input Capacitance		10		pF
I_{TSI}	Three State (off state) Input Current			10	µA

6.3. AC ELECTRICAL SPECIFICATIONS - CLOCK AND CONTROL PINS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C, see figure 6.1.)
OUTPUT LOAD = 50 pF + DC Characteristics I load
REFERENCE LEVELS : V_{IL} : 0.8 V V_{IH} : 2.4 V
V_{OL} : 0.8 V V_{OH} : 2.4 V tr, tf ≤ 5 ns for input signals

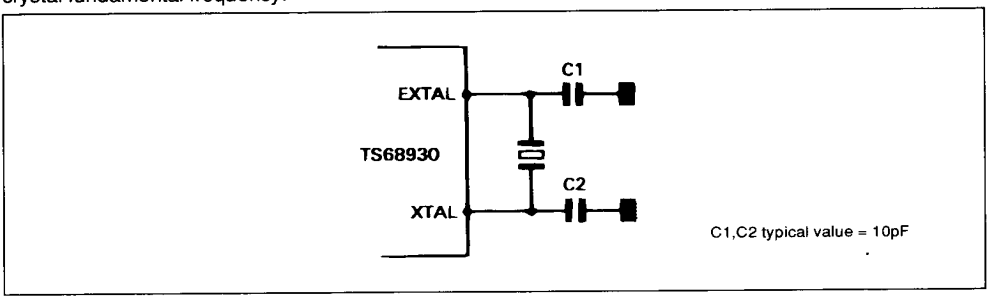
Symbol	Parameter	Min.	Typ.	Max.	Unit
tcex	External Clock Cycle Time	40		160	ns
tfex	External Clock Fall Time			5	ns
trex	External Clock Rise Time			5	ns
tcoh	EXTAL to CLKOUT High Delay		25		ns
tcol	EXTAL to CLKOUT Low Delay		25		ns
tcor	CLKOUT Rise Time			10	ns
tcof	CLKOUT Fall Time			10	ns
tdsl	CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Low		5		ns
tdsh	CLKOUT to DS, RD, WR High		5		ns
tsc	Control Inputs Set-up Time (BS0...BS2, BE3...BE6, Reset, halt)	20			ns
thc	Control Inputs Hold Time (BS0...BS2, BE3...BE6, $\overline{Reset}$, $\overline{halt}$)	10			ns
tdlc	CLKOUT to Control Output Low ($\overline{IRQ}$, BA)			50	ns
tdhc	CLKOUT to Control Output High (BA)			50	ns

Figure 25 : Clock and Control Pins Timing.



INTERNAL CLOCK OPTION

A crystal oscillator can be connected across XTAL and EXTAL. The frequency of CLKOUT : tc/2 is half the crystal fundamental frequency.

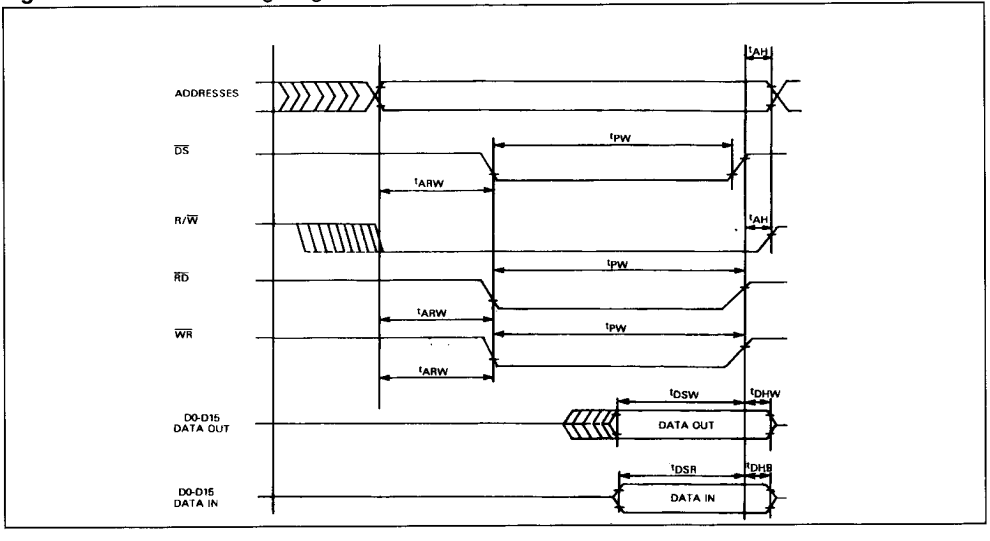


6.4. AC ELECTRICAL SPECIFICATIONS - LOCAL BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C ; see figure 6. 2.)

Symbol	Parameter	Min.	Max.	Unit
t_{PW}	$\overline{RD}$, $\overline{WR}$, $\overline{AS}$ Pulse Width	1/2 tc – 15	1/2 tc	ns
t_{AH}	Address Hold Time	10		ns
t_{DSW}	Data Set-up Time, Write Cycle	25		ns
t_{DHW}	Data Hold Time, Write Cycle	10		ns
t_{DSR}	Data Set-up Time, Read Cycle	20		ns
t_{DHR}	Data Hold Time, Read Cycle	5		ns
t_{ARW}	Address Valid to $\overline{WR}$, $\overline{AS}$, $\overline{RD}$ Low	1/2 tc – 40		ns

Figure 26 : Local Bus Timing Diagram.



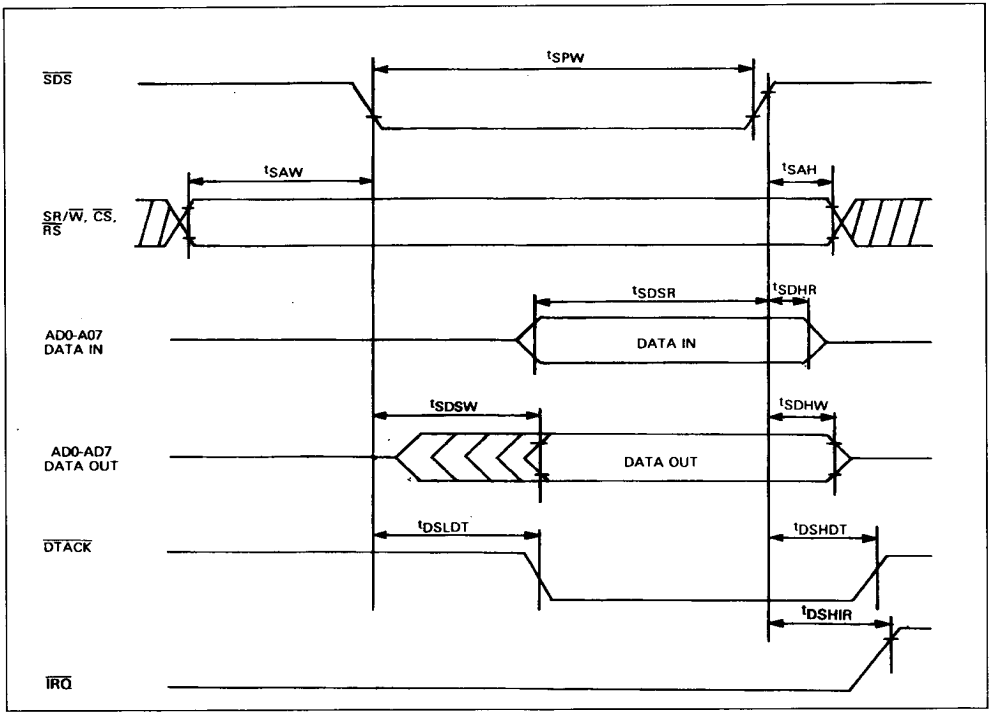
6.5. AC ELECTRICAL SPECIFICATIONS - SYSTEM BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C ; see figure 6. 3.)

Symbol	Parameter	Min.	Max.	Unit
t_{SPW}	$\overline{SDS}$ Pulse Width	60		ns
t_{SAW}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Set-up Time	20		ns
t_{SAH}	SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ Hold after $\overline{SDS}$ High	5		ns
t_{SDSR}	Data Set-up Time, Read Cycle	20		ns
t_{SDHR}	Data Hold Time, Read Cycle	5		ns
t_{SDSW}	Data Set-up Time, Write Cycle		35	ns
t_{SDHW}	Data Hold Time, Write Cycle	10	50	ns
t_{DSLDT}	$\overline{SDS}$ Low to $\overline{DTACK}$ Low		50	ns
t_{DSHDT}	$\overline{SDS}$ High to $\overline{DTACK}$ High*		50	ns
t_{DSHIR}	$\overline{SDS}$ High to $\overline{IRQ}$ High		50	ns

* DTACK is an open drain output test load include RL = 820Ω at Vcc

Figure 27 : System Bus Timing Diagram.

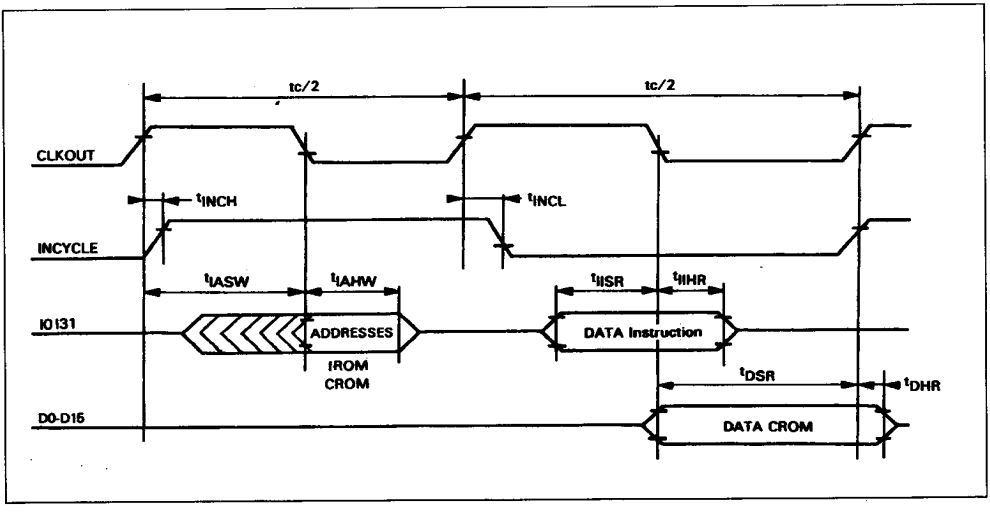


6.6. AC ELECTRICAL SPECIFICATIONS - INSTRUCTION BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0 °C to + 70 °C ; see figure 6. 4.)

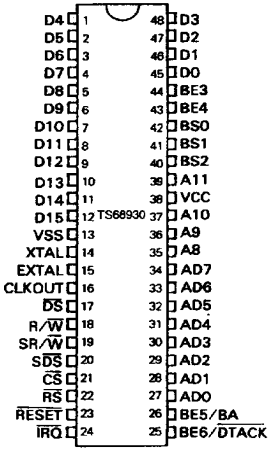
Symbol	Parameter	Min.	Max.	Unit
t_{INCH}	CLKOUT High to INCYCLE High	5	15	ns
t_{INCL}	CLKOUT Low to INCYCLE Low	5	15	ns
t_{IASW}	CLKOUT High to Address Valid		40	ns
t_{IAHW}	I-BUS Address Hold	20	40	ns
t_{IISR}	Instruction Valid	20		ns
t_{IIHR}	Instruction Hold	10		ns
t_{DSR}	CROM Data Set-up Time	tc/2 – 40		ns
t_{DHR}	CROM Data Hold Time	5		ns

Figure 28 : Bus Timing Diagram.



7. PIN CONNECTIONS

48 – Pin Dual – in – Line Package (top view)



M88TS68930-28

84 Pin Grid Array Ceramic(top view)

ID22	ID20	ID19	ID17	ID14	VDD	ID12	ID9	ID7	ID6	BE3
ID25	ID23	ID21	ID18	ID15	ID10	ID11	ID8	INCYCLE	HALT	B50
ID26	ID24			ID16	VSS	ID13			BE4	BS1
ID28	ID27								BS2	A11
ID31	ID30	ID29						A10	A9	A8
ID5	ID0	ID1						BE6 / DTACK	AD4	BES BA
ID3	ID4	ID2						AD7	AD5	AD6
D0	D1								AD2	AD3
D2	D4			D12	VSS	VDD			IRQ	AD1
D3	D6	D7	D10	D13	D15	EXTAL	R/W	CS	RESET	AD0
D5	D8	D9	D11	D14	CLKOUT	XTAL	DS	SR/W	SDS	RS

8. ORDERING INFORMATION

Part Number	Temperature Range*	Package
TS68930CP/PXXX**	0 to 70 °C	48 Pin Plastic DIL
TS68931CR	0 to 70 °C	84 Pin Grid Array

* For extended temp. range, please consult your sales office.
* * XXX is the specific number associated to a customer code.

SOFTWARE TOOLS

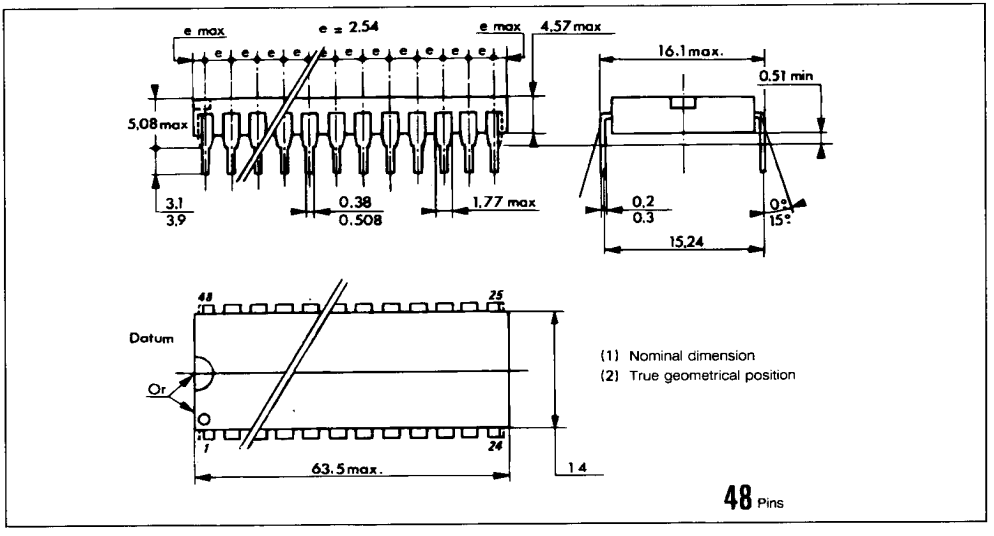
TS68930 SP-PC	Software Package Including Macroassembler Functionnal Stimulator Linker for PC
TS68930 SP-VMS	Same Software Package for VAX Machines
TS68930 SPC-PC	Same Software with C-compiler for PC
TS68930 SPC-VMS	Same Software Package with C-compiler for VAX

HARDWARE TOOLS

TS68930 EMU	Stand-alone Emulator
TS68930 HDS-1	Hardware Development System 110 V Power Supply
TS68930 HDS-0	Hardware Development System 220 V Power Supply
TS68930 EPR	EPROM Simulation Module for TS68930

9. PACKAGE MECHANICAL DATA

48 PINS – PLASTIC DIP



APPENDIX A

DEVELOPMENT TOOLS

DEVELOPMENT PROCESS

The development process of a digital signal processing application using the TS68930 or TS68931 is supported by a complete range of dedicated software and hardware tools which includes macroassembler, linker, simulator, C compiler and optimizer (respectively TS68930SP or TS68930SPC), standalone emulation card TS68930EMU, multiprocessor hardware development system TS68930HDS, EPROM emulation module, TS68930EPR.

SOFTWARE TOOLS

All the development softwares run on the most common computers, such as IBM-PC or AT® , under MS-DOS® or VAX® , VMS® , UNIX® or ULTRIX operating systems.

The macroassembler supports conditional assembly, high level language facilities for loop definition and generates all the files for simulation, emulation and PROM programming.

The functional simulator provides step by step execution, break on address and data values, access to all internal registers and interface to I/O files (ADX, DAC, test inputs).

The linker provides modular programming facilities.

The library consists of macros, basic DSP routines etc... and provides additional help to user's for their applications.

The C language compiler offers high-level language facilities which meets the advanced requirements (parallelism, pipe-line, three computation modes, 32-bit instruction set) of the TS68930/31.

HARDWARE TOOLS

All the hardware tools are designed to provide ease of use and minimum learning time by utilizing menu driven and DSP specific emulation features.

TS68930 EMU and TS68930 HDS have in common :

- Full speed emulation of TS68930 and TS68931
- Use of internal, external or application clock
- 20 breakpoints (stops at defined addresses)
- 8 complex breakpoints (stop after N address X and M address Y)
- Realtime trace of internal resources
- Emulation probes (for TS68930 or TS68931)
- Menu driven operation (about 100 commands)
- Resident Assembler/Disassembler with full screen editor
- Symbolic debbuging
- Direct link with PROM programmers

Emulator specific features.

The TS68930EMU is a low cost, stand-alone emulator providing advanced emulation features such as real-time trace. It can be driven via a RS232C link by a terminal or an IBM-PC^R and offers :

- 8K program memory (expandable to 64K)
- 2K x 16-bit data RAM
- A wire-wrapping area
- Full speed 100ns cycle emulation
- 2RS232C serial ports
- Complex conditions break-points

Hardware development station features :

The TS68930 HDS is a hardware development station, aimed at the development of multiprocessor applications. Up to four pairs of emulator boards, and logic analyser boards can be combined to match exactly the user needs :

- CMOS memory for backup of configuration
- 64K x 32 program memory
- 4K x 16 data RAM
- A logic analyser with :

* 2K x 19 bit for trace of TS68930/31 bus and 15 external inputs
* Synchronous analyzer on program and local buses
* Asynchronous analyzer on system bus or external inputs
* Triggering conditions (Address bus with count, data bus external branch inputs, mailbox exchanges, external inputs).

EPROM module.

The TS68930EPR is a small-sized module which uses the perfect compatibility between TS68930 and TS68931. The module uses a TS68931 and fast EPROM memories to emulate in real time a ROM masked TS68930 during prototyping or field tests to minimize hardware developments. The module is plug and function compatible with TS68930 pin out.

APPENDIX B

MASKING INFORMATION

The information required by SGS-THOMSON to realize a customer masked version of the TS68930 are provided below.

The files for masking must include program ROM content and coefficient ROM content. They can be transferred on EPROMS, 5" 1/4 floppy disks, magnetic tapes (VAX/VMS format) or by link to SGS-THOMSON Microelectronics. This must be done in conjunction with your local sales office or representative indications.

VERIFICATION MEDIA

All original pattern media are filed for contractual purpose and are not returned. A computer listing of the ROM content code will be generated and returned to the customer with a listing verification form. The listing should be carefully checked and the approval form completed, signed and returned to SGS-THOMSON Microelectronics. The returned verification form is the contractual agreement for generation of the customer masks and batch manufacturing.

VERIFICATION UNITS

Ten engineering samples containing the customer ROM patterns will be sent for program verification. These samples will be engineering samples and must be kept by user as reference parts.

DIGITAL SIGNAL PROCESSOR
CUSTOMER ORDERING SHEET

COMMERCIAL REFERENCE* : .TS68930CP/XXX...

CUSTOMER'S MARKING : .....

COMPANY : .....

ADDRESS : .....

PHONE : .....

PATTERN MEDIAS :

O EPROMS

O 5 1/4" FLOPPY

O MAGNETIC TYPE-

O OTHER*

OPTION :

O WATCHDOG

YEARLY QUANTITY FORECASTED :

START OF PRODUCTION DATE :

FOR A SHIPMENT PERIOD OF :

Customer Contact Name **Date** **Signature**

APPENDIX C

SUMMARY OF RESOURCES PER FUNCTION

OPERATING MODES

Symbol	Function	Resource	Paragraph Nb
MODE	2-bit register defining the operating mode (real/complex/double precision)	Access Mode Register	

OPERATING UNIT

Symbol	Function	Resource	Paragraph Nb
ALU	2 Port 16-bit Arithmetic Logic Unit 5 Possible Sources. 4 Possible Destinations. 30 ALU Codes Works on 32-bit. Data in 2 Machines Cycles.	Arithmetic Logic Unit	3. 2. 1
D	ALU Output Register		
BS	Variable 0 – 15-bit right shift, left shift, right rotation barrel shifter.	Barrel Shifter	3. 2. 2
MULT	16 x 16 → 32 parallel pipeline multiplier + 16-bit adder/substractor, used in complex Multiplications.	Pipeline Multiplier	3. 2. 3
M, N	2 x 16-bit registers containing multiplier operands.		
P	2 x 16-bit register containing multiplier result.		
STA	16-bit register containing status of ALU, mode, status of address calculation units,enable interrupt flag.	Status	3. 2. 4
A	2 x 16-bit accumulator.	Accumulators	3. 2. 4
B	2 x 16-bit accumulator.		
F	4 x 16-bit first in first out register.	Fifo	3. 2. 4
EF	Flag. Indicates that the Fifo is empty; can be set by software.	Empty Fifo	
RC	6-bit register allowing replacement of ALU operation code by a data coming from L-BUS.	Replace Code Register	3. 2. 4
T	2 x 16-bit register providing direct transfer between L-BUS and Z-BUS.	Transfer Register	3. 2. 4
SAT	Flag indicates saturation mode.	Saturation	3. 2. 4

DATA MEMORY BLOCK

Symbol	Function	Resource	Paragraph Nb
XRAM YRAM	128 x 16-bit Random Access Memories	Data RAMs	3. 3. 1
CROM	512 x 16-bit read only memory containing coefficients or constants.	Data ROM	
XACU YACU	Arithmetic units providing address incrementation, decrementation and automatic loop. XACU is dedicated to XRAM. (8 bits) YACU is dedicated to YRAM. (7 bits)	Address Calculation Units	3. 3. 2
ECACU	12-bit arithmetic unit providing incrementation, decrementation of address. Shared by CROM and ERAM (external RAM).		
XC YC	Flag indicates the circular addressing mode for XRAM. Flag indicates the circular addressing mode for YRAM.	XRAM Circular Flag YRAM Circular Flag	3. 3. 3
X0, X1 X	2 x 8-bit registers used for indirect addressing of XRAM Supplementary register used for circular addressing.	Pointers	3. 3. 4
Y0, Y1 Y	2 x 7-bit registers used for indirect addressing for YRAM. Supplementary register used for circular addressing.		
C0, C1	2 x 9-bit register used for indirect addressing of CROM.		
E0, E1	2 x 12-bit registers used for indirect addressing of ERAM.		

CONTROL BLOCK

Symbol	Function	Resource	Paragraph Nb
IROM IR	1280 x 32-bit word read-only-memory containing program code and immediate data for TS68930 (ref section 6. 6 for TS68931) 32-bit register containing instruction.	Instruction ROM Instruction Register	3. 4. 2
PC	Register containing address of program memory.	Program Counter	3. 4. 3
SEQ	The sequencer can test directly 16 conditions programmed on a high or low state and the sequencer controls next program address defined by BRANCH, subroutine call, next instructions.	Sequencer	3. 4. 1
RAS	2 x 16-bit register for saving programm counter in case of subroutine call or interrupt.	Return Address Stack	
LC	15-bit register containing a control word for automatic loop. It is divided into the following sub-registers.	Loop Counter	3. 4. 4
LCI LCR LCD	4-bit register containing the number of instructions to be executed in the loop. 8-bit register containing the number of loops. 3-bit register containing the number of instructions between declaration and start of the loop.		
	Prevents locked states for TS68930 only.	Watchdog Circuit	3. 6. 3

INPUT/OUTPUT BLOCK

Symbol	Function	Ressource	Paragraph Nb
AMR	8-bit register defining the access mode on the local bus.	Access Mode Register	3. 5. 7
RIN ROUT	3 x 8-bit shift register. Mailbox input. 3 x 8-bit shift register. Mailbox output.	Input Register Output Register	3. 5. 6
RDYOIN	Flag used in the protocol to indicate witch processor has access to the mailbox.	Read Out Internal	3. 5. 5