CMOS 8-BIT MICROCONTROLLER

TMP90CN72DF

1. OUTLINE AND CHARACTERISTICS

The TMP90CN72 is a high-performance 8-bit single-chip microcontroller ; TLCS-90 CPU core capacious ROM, RAM and peripheral circuits adequate to control VCR system are included.

(1) Efficiently systematized instructions
- 163 instructions
- Multiplication, division, 16-bit arithmetic operation, Bit manipulation

(2) Minimum instruction execution time: 250 ns at 16 MHz Oscillation, 122 μs at 32.8 kHz Oscillation.
(3) Internal ROM : 40K bytes
(4) Internal RAM : 768 bytes
(5) 20-bit time-base Counter (TBC)
(6) 8-bit timer / counter : 4 channels
- Timer mode / Event counter mode • 16-bit timer/counter mode

(7) Capture inputs : 8 terminals
- 18-bit timing data + 6-bit trigger data (with 8 level FIFO) : 1 channel
- 16-bit timing data + 1-bit trigger data : 2 channels

(8) Timing Pulse Generator (TPG) : 2 channels
- 16-bit timing data + 6-bit output data (with 4 level FIFO) : 1 channel
- 16-bit timing data + 4-bit output data: 1 channel

(9) PWM output
- 12-bit PWM : 2 channels • 8-bit or 14-bit PWM : 1 channel

(10) C-Sync signal separation
- H/V SYNC separation • Mute Detection

(11) VISS/VASS detection
- Index Search/Address code Search

(12) Head amp/Color rotary control circuit
(13) Pseudo synchronizing signal (PV/PH) output
(14) Serial interface
- 8-bit clock synchronous mode : 2 channels

(15) On-Screen Display (OSD) Control circuit
- 128 characters • 24 characters × 10 lines

(16) 8-bit A/D Converter : 12 inputs
(17) CTL amplifier, Capstan FG amplifier
(18) Input / Output port : 63 terminals
(19) Interrupt : 17 factors (19 interrupt sources)
- A multiplex interrupt control with independence latch
- External interrupt with edge select function

(20) Watch dog timer
(21) Operation mode under low Current Consumption (Dual Clock System)
- STOP mode : Oscillation stop (Battery / Capacitor back-up). Port output selection (Data hold / High impedance)
- SLOW mode : Slow speed operation with 32.8 kHz
- IDLE mode : CPU stop / peripheral circuit active at high speed / released by interrupt
- SLEEP mode : CPU stop / peripheral circuit active at slow speed / released by interrupt

(22) The TMP90CN72DF is molded in a 100-pin Quad Flat Package (QFP100-P-2222A)

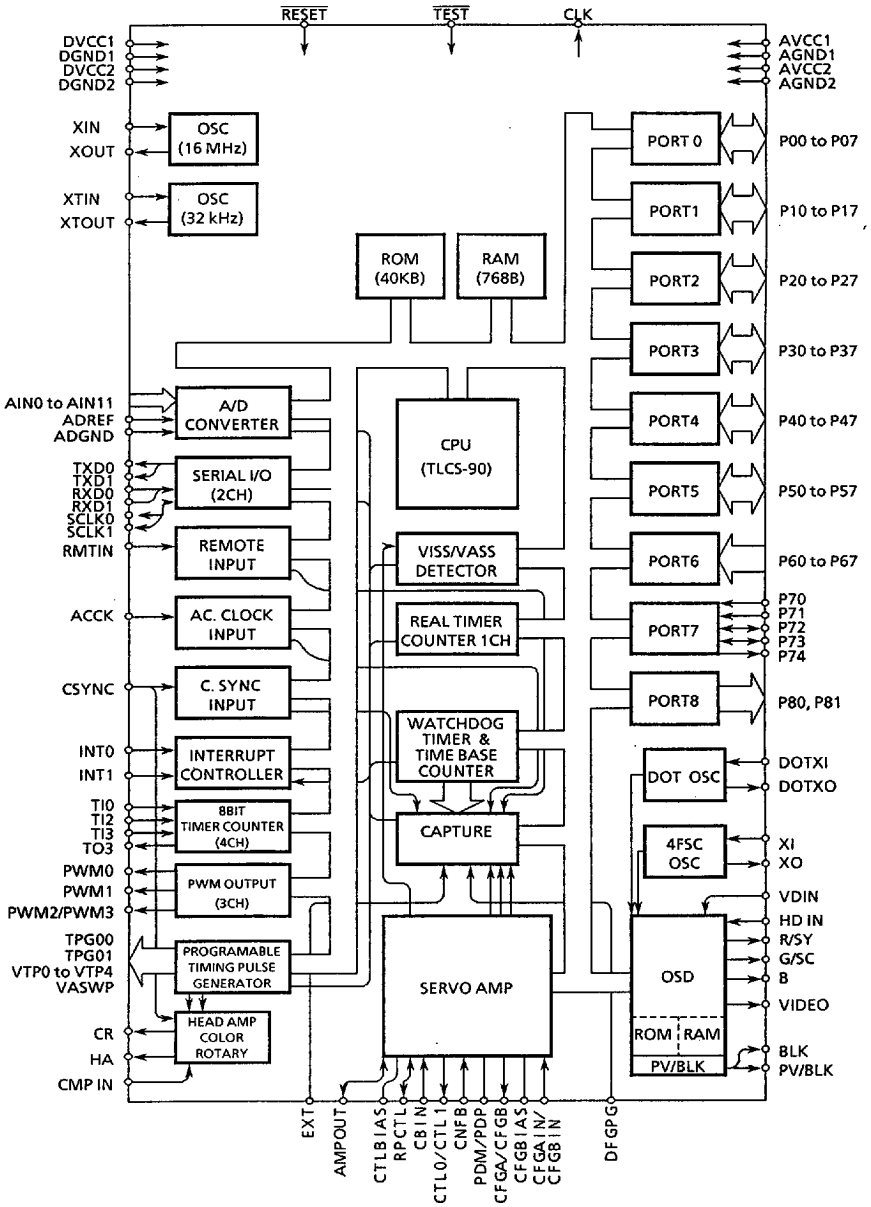


Fig 1.1 TMP90CN72DF Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The pin assignment of TMP90CN72DF is shown in Fig. 2.1 and its name and function are in Table 2.1.

2.1 Pin Assignment

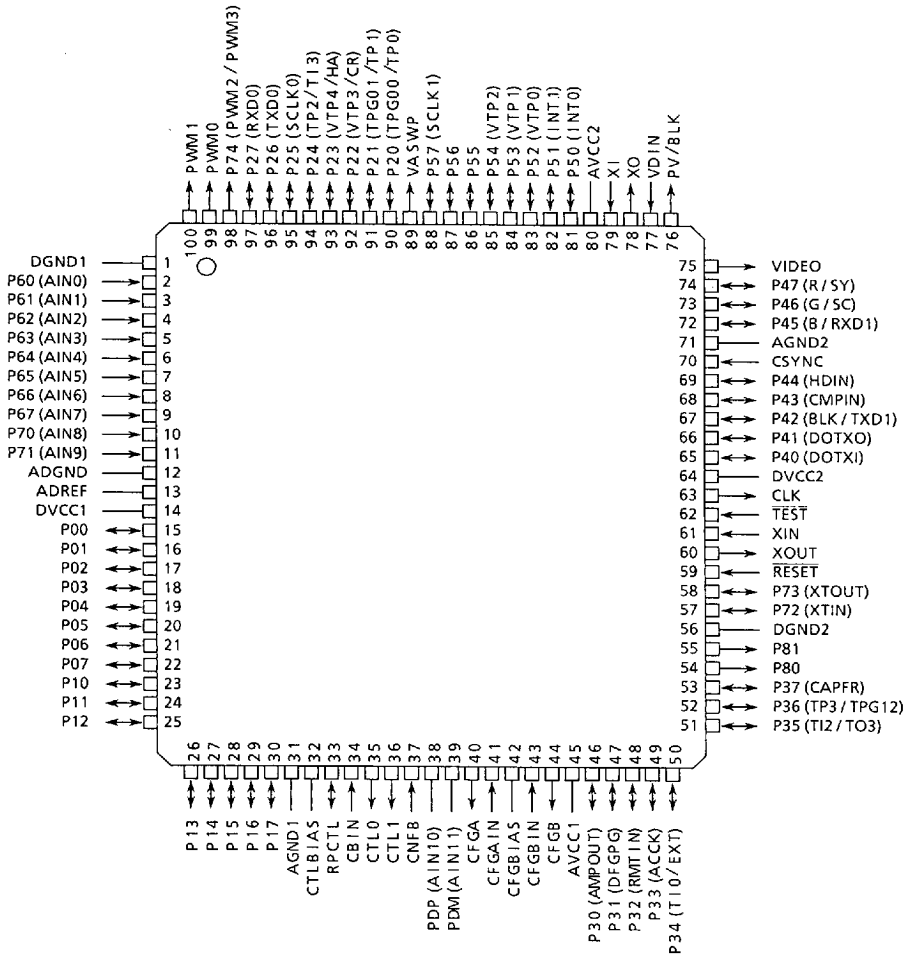


Fig. 2.1 Pin Assignment of TMP90CN72DF

2.2 Pin name and pin functions

The name and functions of each pin are shown in Table 2.1.

Table 2.1 Pin name and pin functions (1/4)

Pin Name	No. of PinS	I/O Port structure	Function
P00 to P07	8	I/O 3-state	P00 to P07 : 8-bit I/O port. Input and output can be set in bit unit.
P10 to P17	8	I/O 3-state	P10 to P17 : 8-bit I/O port. Input and output can be set in bit unit.
P20 (TPG00 / TP0) P21 (TPG01 / TP1)	2	I/O 3-state Programmable Open Drain	P20, P21 : 2-bit I/O port. Input and output can be set in bit unit. TPG00/TPG01 : Timing Pulse Generator 0 (TPG0) TP0/TP1 : Timing Pulse (TP) output.
P22 (VTP3 / CR) P23 (VTP4 / HA)	2	I/O 3-state Programmable Open Drain	P22, P23 : 2-bit I/O port. Input and output can be set in bit unit. VTP3/VTP4 : Video Timing pulse (VTP) output. CR : Color Rotary output. HA : Head Amp switching signal output.
P24 (TP2 / TI3)	1	I/O 3-state Programmable Open Drain Schmitt input	P24 : 1-bit I/O port. Input and output can be set in bit unit. TP2 : Timing pulse (TP) output. TI3 : Event count input for Timer3 (TC3).
P25 (SCLK0)	1	I/O 3-state Schmitt input	P25 : 1-bit I/O port. Input and output can be set in bit unit. SCLK0 : Serial clock input/output for SIO0.
P26 (TXD0)	1	I/O 3-state	P26 : 1-bit I/O port. Input and output can be set in bit unit. TXD0 : Serial transmit data output for SIO0.
P27 (RXD0)	1	I/O 3-state Schmitt input	P27 : 1-bit I/O port. Input and output can be set in bit unit. RXD0 : Serial receive data input for SIO0.
P30 (AMPOUT)	1	I/O 3-state	P30 : 1-bit I/O port. Input and output can be set in bit unit. AMPOUT : Monitor output of Analog amp (CTL amp / CFG amp) for servo control.
P31 (DFGPG) P32 (RMTIN) P33 (ACCK)	3	I/O 3-state Schmitt input	P31, P32, P33 : 3-bit I/O port. Input and output can be set in bit unit. DFGPG : Input for Drum PG/FG conposite signal. RMTIN : Input for remote control signal. ACCK : Input for AC power frequency.
P34 (TI0 / EXT)	1	I/O 3-state Schmitt input	P34 : I/O port. Input and output can be set in bit unit. TI0 : Event Count input for Timer0 (TC0). EXT : External trigger input for Capture 0 (CAP0).
P35 (TI2 / TO3)	1	I/O 3-state Schmitt input	P35 : 1-bit I/O port. Input and output can be set in bit unit. TI2 : Event Count input for Timer2 (TC2). TO3 : Timer3 (TC3) output.

Table 2.1 Pin name and pin functions (2/4)

Pin Name	No. of Pins	I/O Port structure	Function
P36 (TP3 / TPG12)	1	I/O 3-state Schmitt input	P36 : 1-bit I/O port. Input and output can be set in bit unit. TP3 : Timing pulse (TP) output. TPG12 : Timing pulse generator (TPG1) output.
P37 (CAPFR)	1	I/O 3-state Programmable Open Drain	P37 : 1-bit I/O port. Input and output can be set in bit unit. CAPFR : Capstan motor control output.
P40 (DOTXI) P41 (DOTXO)	2	I/O 3-state	P40, P41 : 2-bit I/O port. Input and output can be set in bit unit. DOTXI / DOTXO : Oscillator terminal for OSD dot-clock.
P42 (BLK / TXD1)	1	I/O Open Drain	P42 : 1-bit I/O port. Input and output can be set in bit unit. BLK : Blanking output for OSD. TXD1 : Serial transmit data output for SIO1.
P43 (CMPIN) P44 (HDIN)	2	I/O 3-state Schmitt input	P43, P44 : 2-bit I/O port. Input and output can be set in bit unit. CMP IN : Comparator signal input for Head Amp switch. HD IN : Horizontal sync. signal input.
P45 (B / RXD1)	1	I/O Open Drain Schmitt input	P45 : 1-bit I/O port. Input and output can be set in bit unit. B : Blue output from OSD. RXD1 : Serial receive data input for SIO1.
P46 (G / SC) P47 (R / SY)	2	I/O 3-state	P46, P47 : 2-bit I/O port. Input and output can be set in bit unit. G, R : Green and Red output from OSD. SC, SY : Chroma, luminance Signal output from OSD.
P50 (INT0) P51 (INT1)	2	I/O 3-state Schmitt input	P50, P51 : 2-bit I/O port. Input and output can be set in bit unit. INT0, INT1 : External interrupt request.
P52 (VTP0) P53 (VTP1)	2	I/O 3-state Programmable Open Drain Schmitt input	P52, P53 : 2-bit I/O port. Input and output can be set in bit unit. VTP0, VTP1 : Video timing pulse (VTP) output.
P54 (VTP2)	1	I/O 3-state Schmitt input	P54 : 1-bit I/O port. Input and output can be set. VTP2 : Video timing pulse (VTP) output.
P55 P56	2	I/O 3-state Open Drain Schmitt input	P55, P56 : 2-bit I/O port. Input and output can be set in bit unit.
P57 (SCLK1)	1	I/O Open Drain Schmitt input	P57 : 1-bit I/O port. Input and output can be set. SCLK1 : Serial clock input/output for SIO1.

Table 2.1 Pin name and pin functions (3/4)

Pin Name	No. of Pins	I/O Port structure	Function
P60 (AIN0) to P67 (AIN7) P70 (AIN8) to P71 (AIN9)	10	Input	P60 to P67 : 8-bit input port. P70, P71 : 2-bit input port. AIN0 to AIN9 : Analog input for A/D converter.
P72 (XTIN) P73 (XTOUT)	2	I/O 3-state	P72, P73 : 2-bit I/O port. Input and output can be set in bit unit. XTIN, XTOUT : Oscillator terminals for slow clock (32.768 kHz)
P74 (PWM2 / PWM3)	1	Output 3-state Programmable Open Drain	P74 : 1-bit output port. PWM2/PWM3 : 8-bit / 14-bit PWM (PWM2 / PWM3) output.
P80 P81	2	Output 3-state	P80, P81 : 2-bit output port.
PWM0 PWM1	2	Output 3-state Programmable Open Drain	PWM0 : 12-bit PWM (PWM0) output. PWM1 : 12-bit PWM (PWM1) output.
VASWP	1	Output 3-state	Video / Audio head switching control signal output.
CSYNC	1	Input Schmitt input	Composite sync. signal input.
CTLBIAS	1	–	Bias terminal for control (CTL) amplifier.
RPCTL	1	I/O	Input and output for Control (CTL) signal.
CBIN	1	Input	Bias input terminal for control (CTL) amplifier.
CTL0 CTL1	2	Output	CTL amplifier output for gain switching.
CNFB	1	Input	Negative feed-back terminal of CTL amplifier.
PDP (AIN10)	1		PDP : Terminal for Peak-Hold capacitor which keeps plus (positive) peak for control (CTL) Amplifier. AIN10 : Analog input for PDP level monitor.
PDM (AIN11)	1		PDM : Terminal for Peak-Hold capacitor which keeps plus (positive) peak for control (CTL) Amplifier. AIN11 : Analog input for PDM level monitor.

Table 2.1 Pin name and pin functions (4/4)

Pin Name	No. of Pins	I/O Port structure	Function
CFGA	1	Output	Capstan FG amplifier (CFGA amp.) output.
CFGA IN	1	Input	Capstan FG amplifier (CFGA amp.) input.
CFG BIAS	1	–	Capstan FG amplifier bias terminal.
CFGB IN	1	Input	Capstan FG amplifier (CFGB amp.) input.
CFGB	1	Output	Capstan FG amplifier (CFGB amp.) output.
VIDEO	1	Output	OSD video signal output.
PV / BLK	1	Output 4-state	Pseudo V-SYNC (PV) output / On Screen Display (OSD) Blanking (BLK) output.
VDIN	1	Input Schmitt input	Vertical sync signal input.
XI, XO	2	Input, Output	Oscillator terminals for 4fsc clock of OSD
CLK	1	Output	Clock output : 1/2 or 1/4 of system clock (16 MHz) is output. During RESET operation, output stays high. (Pulled up internally).
$\overline{TEST}$	1	Input	Test terminal : Should be connected to high.
XIN, XOUT	2	Input, Output	Oscillator terminals for main clock (16 MHz)
$\overline{RESET}$	1	Input Schmitt input	System reset input.
DVCC1 DVCC2	2	–	Digital Power supply.
DGND1 DGND2	2	–	Digital Ground.
AVCC1 AVCC2	1	–	Analog Power supply.
AGND1 AGND2	1	–	Analog Ground.
ADREF	1	–	A/D converter reference voltage.
ADGND	1	–	A/D converter Ground.

3. Operations

TMP90CN72 is different from TMP90CR74A in the functions and the operations. Please read Please see the technical documentation of TMP90CR74A besides.

Differences between TMP90CN72 and TMP90CR74A are shown in table 3.1.

Table 3.1 Difference of TMP90CN72 and TMP90CR74A

	TMP90CR74A	TMP90CN72
ROM	56K bytes (0000_H to $DFFF_H$)	40K byte (0000_H to $9FFF_H$)
RAM	1K byte ($FBB0_H$ to $FFAF_H$)	768 byte ($FCB0_H$ to $FFAF_H$)
I²CBUS	○	–
OSD		
· CHARACTER	256 (10000_H to $13FFF_H$)	128 (10000H to $11FFF_H$)
· BLINKING	○	–

3.1 Memory Map

3.1.1 Internal ROM

The TMP90CN72 contains an 40K-byte ROM. The address space from 0000H to 9FFFH is provided to the ROM. The CPU starts executing a program from 0000H by resetting.

The addresses 0008H to 004FH in this internal ROM area are used for the entry area for the interrupt processing.

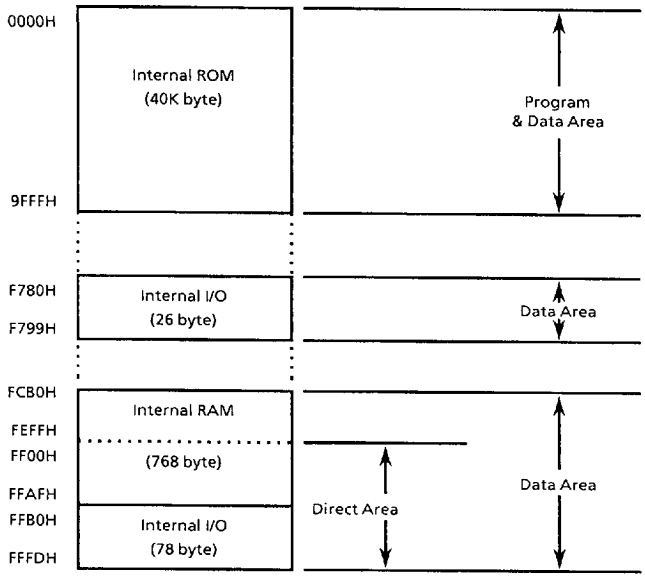
3.1.2 Internal RAM

The TMP90CN72 also contains a 768-byte RAM, which is allocated to the address space from FCB0H to FFAFH. The CPU allows the access to a certain RAM area (FF00H to FFAFH, 176 bytes) by a short operation code (opcode) in a "direct addressing mode".

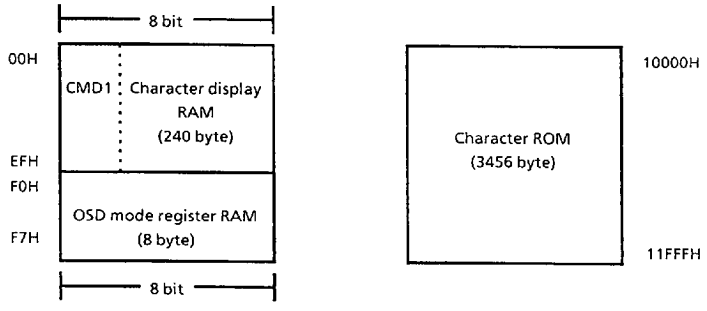
3.1.3 Internal I/O

The TMP90CN72 provides a 104-byte address space as an internal I/O area, whose addresses range from FFB0H to FFFDH (I/O area 1) and F780H to F799H (I/O area 2). This I/O area 1 can be accessed by the CPU using a short opcode in the "direct addressing mode".

Figure 3.1.1 is a memory map indicating the areas accessible by the CPU in the respective addressing mode.



(a) Memory map for CPU



(b) Memory map for OSD control RAM and character ROM

Figure 3.1.1 Memory map

3.2 Interrupt control circuit

The serial bus interface (SBI) is not included in TMP90CN72. Therefore, the interrupt control registers which are shown as follows are different from that of TMP90CR74A.

① Interrupt Enable Register1

INTE1 (F78DH)

7	6	5	4	3	2	1	0	
IET0DIR	IETBC	–	IETPG1	IETPG0	IECAP0	IECAP1	IE0	(Initial Value 0000 0000)

IET0DIR	INTT0DIR Interrupt Enable / Disable	0 : Disable 1 : Enable	R/W
IETBC	INTTBC Interrupt Enable / Disable		
IETPG1	INTTPG1 Interrupt Enable / Disable		
IETPG0	INTTPG0 Interrupt Enable / Disable		
IECAP0	INTCAP0 Interrupt Enable / Disable		
IECAP1	INTCAP1 Interrupt Enable / Disable		
IE0	INT0 Interrupt Enable / Disable		

② Interrupt Request Flag1

IRF1 (F790H)

7	6	5	4	3	2	1	0	
IRFT 0DIR	IRFTBC	–	IRFTPG1	IRFTPG0	IRF CAP0	IRF CAP1	IRF0	(Initial Value 0000 0000)

IRFT0DIR	INTT0DIR Interrupt Request	0 : No Interrupt Request 1 : Interrupt Request	R/W
IRFTBC	INTTBC Interrupt Request		
IRFTPG1	INTTPG1 Interrupt Request		
IRFTPG0	INTTPG0 Interrupt Request		
IRFCAP0	INTCAP0 Interrupt Request		
IRFCAP1	INTCAP1 Interrupt Request		
IRF0	INT0 Interrupt Request		

3.3 On screen display output circuit (OSD)

Out of the control registers to control OSD display, the following control registers are different from that of TMP90CR74A.

① OSD Control Register

OSDCR (FFCEH)

7	6	5	4	3	2	1	0
CMD1	"0"	TCEN	DISPON	EXT/$\overline{INT}$	4/$\overline{3}$	50/$\overline{60}$	P/$\overline{N}$

(Initial Value 0000 0000)

CMD1	Standard / Reverse characters	0 : Standard character 1 : Reverse character	R/W
TCEN	Dot clock (TC) enable	0 : Disable 1 : Enable	
DISPON	Display enable	0 : Disable 1 : Enable	
EXT/$\overline{INT}$	Display synchronization	0 : Internal mode (full page mode) 1 : External mode (Superimpose mode)	
4/$\overline{3}$	Selection of color sub-carrier (fsc) for full-page mode	0 : 3.58 MHz 1 : 4.43 MHz	
50/$\overline{60}$	Selection of V-sync frequency (fv) for full-page mode	0 : 60 Hz 1 : 50 Hz	
P/$\overline{N}$	Selection of color processing method in the internal synchronous mode	0 : NTSC 1 : PAL	

Note : Always write "0" to bit 6 in OSD Control Register (OSDCR).

② Display RAM Data Buffer Register / Display RAM (Character code register)

The character code is written to the character code register (CHARD0 to CHARD239) by writing data to the display RAM data buffer register (OSDDBR) in the indirect addressing. The character number of TMP90CN72 is 128 (including 4 words of the blank code). The lower 7 bits of OSDDBR are character codes, and the data of the most upper bit 7 is invalid. The value of the reverse character specification bit OSDCR<CMD1> is stored in the most upper bit (bit 7) of the character code register.

Display RAM Data Buffer Register

OSDDBR (FFD0H)

7	6	5	4	3	2	1	0
*	OSDD6 to OSDD0						

(Initial Value 0000 0000)

Note * : Don't care

Display RAM (character code Register)

CHARD0 (00H) to CHARD239 (0EFH)

7	6	5	4	3	2	1	0
OSDCR <CMD1>	CD6 to CD0 (OSDDBR<OSDD6 to 0>)						

7	6	5	4	3	2	1	0
OSDCR <CMD1>	CD6 to CD0 (OSDDBR<OSDD6 to 0>)						

CD6 to CD0	Character code (124 character code + 4 Blank code : 00H to 7FH)	Write only

③ OSD Mode Register 4

OSDMR4 (00F4H)

7	6	5	4	3	2	1	0
CB/$\overline{CF}$	FCPH2	FDPH2	FEPH2	–	–	"0"	"0"

(Reset Value 0000 0000)

CB/$\overline{CF}$	Area selection for color changing by Blank code	0 : Character font 1 : Character background	write only
FCPH2	Character or its background coloring after display position of Blank code (FCH)	PH2 of hue setting changed by Blank code (FCH)	
FDPH2	Character or its background coloring after display position of Blank code (FDH)	PH2 of hue setting changed by Blank code (FDH)	
FEPH2	Character or its background coloring after display position of Blank code (FEH)	PH2 of hue setting changed by Blank code (FEH)	

Note : Always write "0" to bit 1 and bit 0 in OSD Mode Register 4 (OSDMR4).

④ OSD Mode Register 6

OSD Mode Register 6

OSDMR6 (00F6H)

7	6	5	4	3	2	1	0
"0"	YL2	YL1	YL0	CFOFF	CFPH2	CFPH1	CFPH0

(Reset Value 0000 0000)

YL2 to YL0	Luminance (Y) level	Selecting from 5 to 100 IRE	write only
CFOFF	Coloring of character font	0 : ON 1 : OFF	
CFPH2 to CFPH0	Hue of character	8 kings of color (Hue) at every 45 deg. against color-burst (0 to 7H)	

Note : Always write "0" to bit 7 in OSD Mode Register 6 (OSDMR6).

3.4 Port

The serial bus interface (SBI) is not included in TMP90CN72. The port configurations which are shown as follows are different from that of TMP90CR74A.

① P52, P53

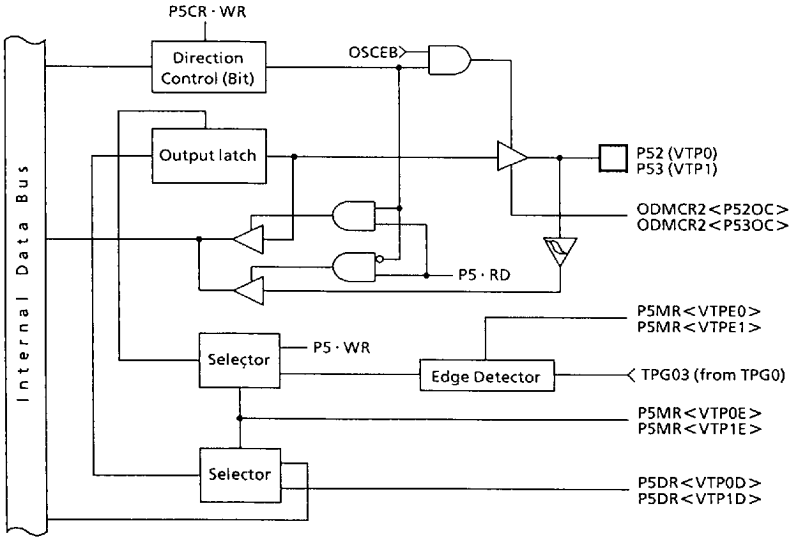


Fig 3.4.1 Port 5 (P52 and P53) Block Diagram

② P54

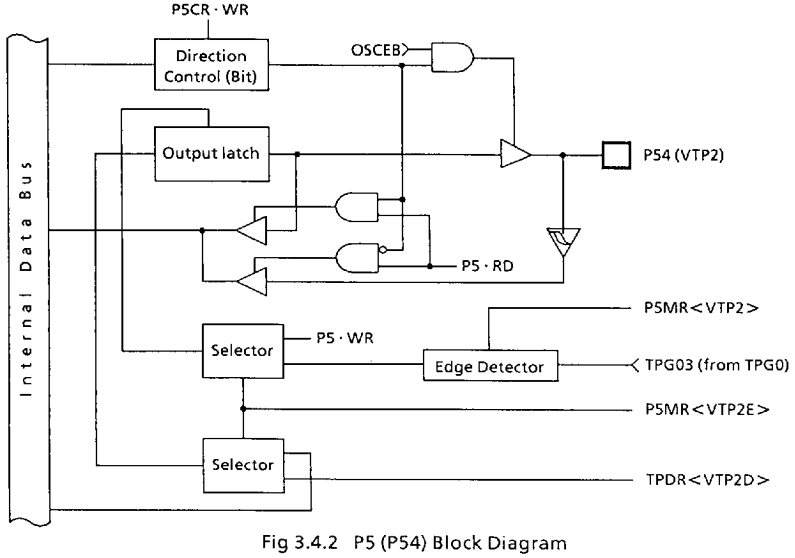


Fig 3.4.2 P5 (P54) Block Diagram

③ P55, P56

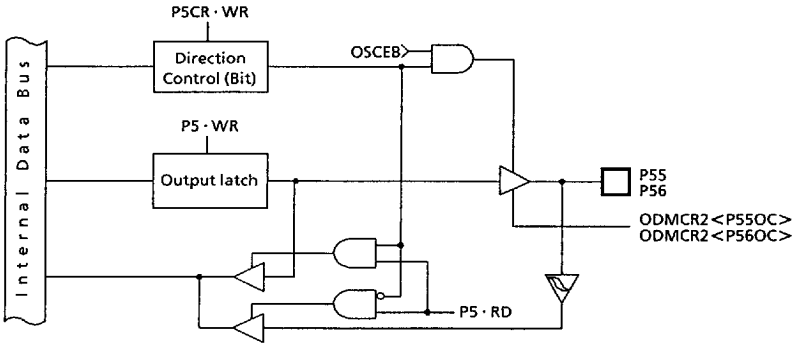
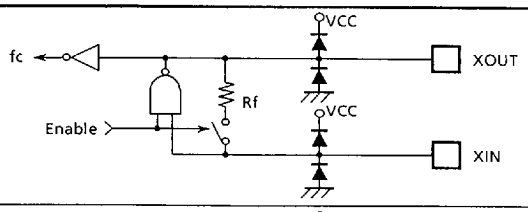
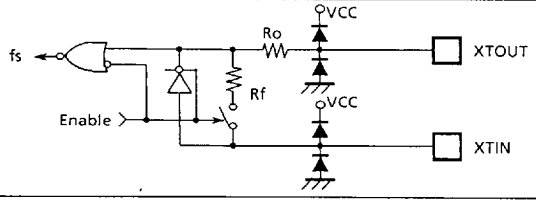
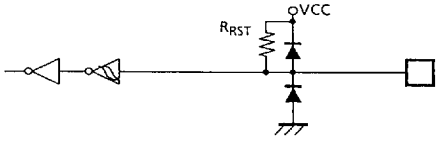
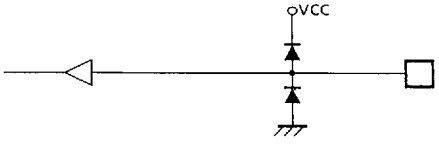
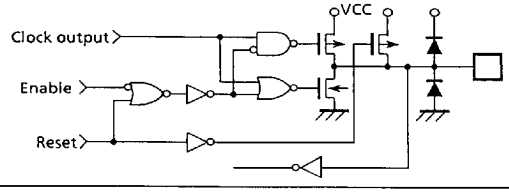
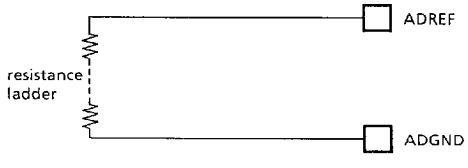
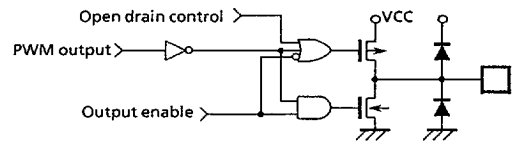
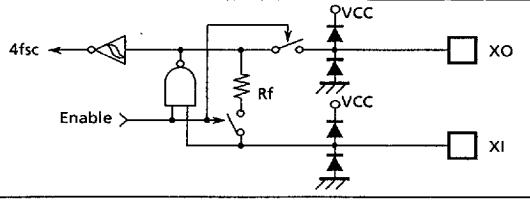
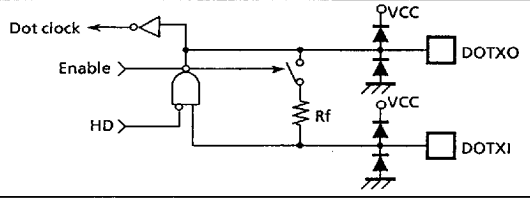
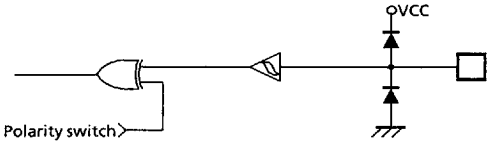
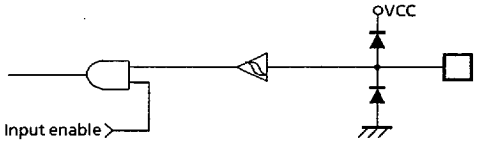
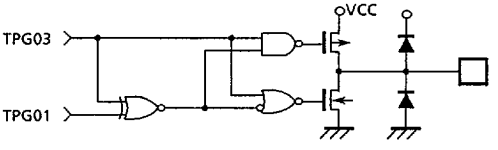


Fig 3.4.3 P5 (P55 and P56) Block Diagram

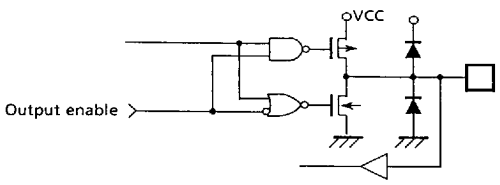
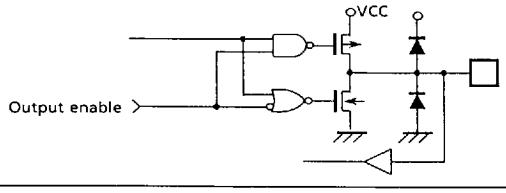
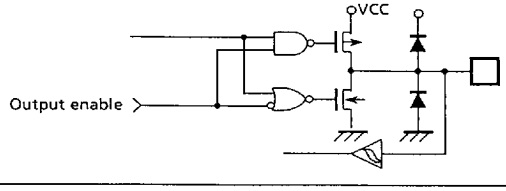
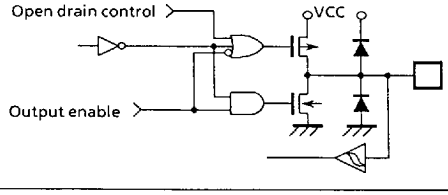
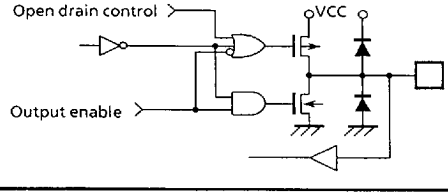
4. PINS OF INPUT / OUTPUT CIRCUIT

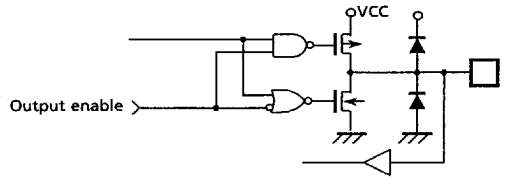
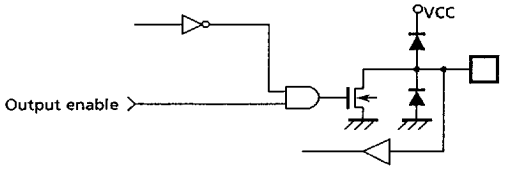
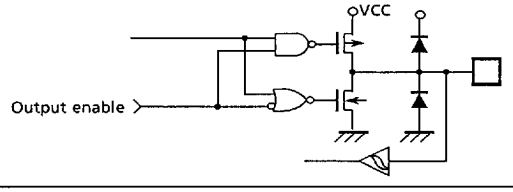
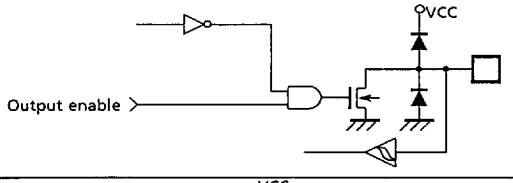
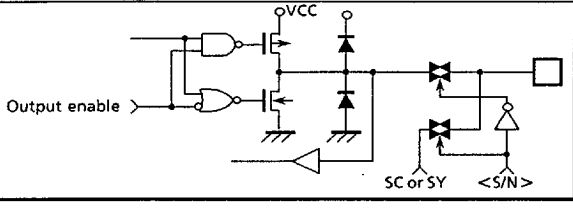
(1) Control pin

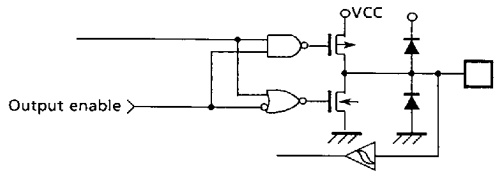
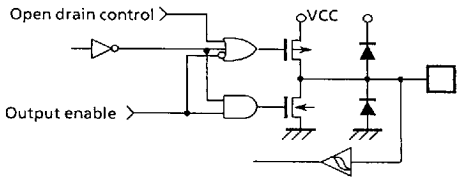
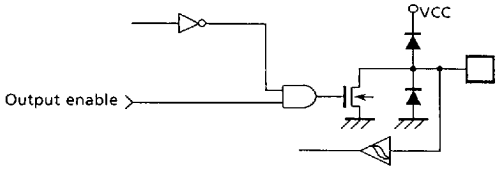
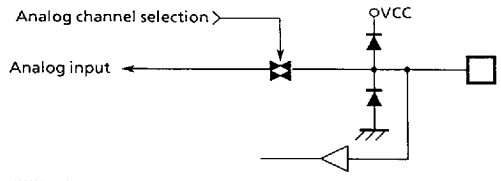
CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
XIN XOUT	Input / Output		Resonator connecting pins (high-frequency) Rf = 1.2 MΩ (Typ.)
XTIN XTOUT	Input / Output		Also used as resonator connecting pins (low-frequency), P72 and P73 Rf = 6 MΩ (Typ.) Ro = 220 kΩ (Typ.)
$\overline{\text{RESET}}$	Input		Schmit input Pull-up resistor R_{RST} = 100 kΩ (Typ.)
$\overline{\text{TEST}}$	Input		Final test pin Fix to "H" level
CLK	Output		
ADREF ADGND			Analog reference voltage pin I_{REF} = 0.6 mA (Typ.)

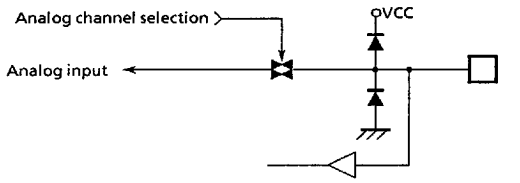
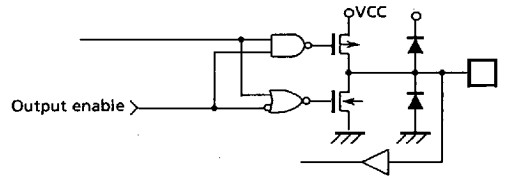
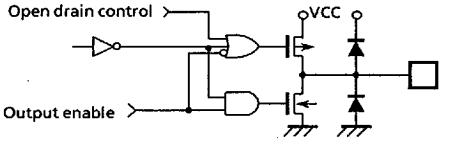
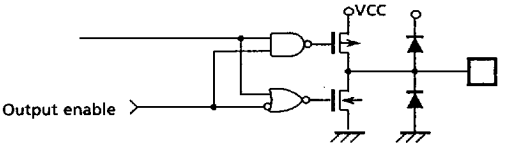
CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
PWM0 PWM1	Output		Tri-start output Open drain output (Programmable)
XI XO	Input / Output		OSD oscillator connecting pins Rf = 1.2 MΩ (Typ.)
DOTXI DOTXO	Input / Output		Also used as oscillator connecting pins, P40 and P41 Rf = 1.2 MΩ (Typ.)
CSYNC	Input		CSYNC input Schmit input
VDIN	Input		OSD VD input Schmit input
VASWP	Output		Head switch signal output Tri-state output

(2) I/O port

CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
P0 P1	Input/ Output		Tri-state I/O
P2 P3	Input/ Output		Tri-state I/O P26, P30
	Input/ Output		Tri-state I/O Schmit input P25, P27 P31 to P36
	Input/ Output		Tri-state I/O Open drain output (programmable) Schmit input P24
	Input/ Output		Tri-state I/O Open drain output (programmable) P20 to P23 P37

CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
P4	Input / Output		Tri-state I/O P40, P41
	Input / Output		Open drain output P42
	Input / Output		Tri-state I/O Schmit input P43, P44
	Input / Output		Open drain output Schmit input P45
	Input / Output		Tri-state I/O P46, P47

CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
P5	Input / Output		Tri-state I/O Schmit input P50, P51, P54
	Input / Output		Tri-state I/O Open drain output (Programmable) Schmit input P52, P53, P55, P56
	Input / Output		Open drain output Schmit input P57
P6	Input		

CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
	Input		P70, P71
P7	Input / Output		Also used as Tri-state output, XTIN and XTOUT P72, P73
	Output		Tri-state output Open drain output (programmable) P74
P8	Output		Tri-state output P80, P81

5. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS (or note)	RATING	UNIT
Supply voltage	V_{CC}	DVCC1, DVCC2, AVCC1, AVCC2	− 0.5 to + 6.5	V
Input voltage	V_{IN}		− 0.5 to V_{CC} + 0.5	V
Output Voltage	V_{OUT1}		− 0.5 to V_{CC} + 0.5	V
Output Current (Per 1 pin)	I_{OUT1}	Analog Output pin (Source Current)	− 10	mA
	I_{OUT2}	Digital Output pin (Source Current)	− 3.2	mA
	I_{OUT3}	Analog Output pin (Sink Current)	10	mA
	I_{OUT4}	Digital Output pin (Sink Current)	3.2	mA
Output Current (Total)	ΣI_M	$\Sigma I_M = \Sigma I_{OUT1} + \Sigma I_{OUT2}$	− 50	mA
	ΣI_P	$\Sigma I_P = \Sigma I_{OUT3} + \Sigma I_{OUT4}$	100	mA
Power Dissipation (Ta = 70°C)	P_D		700	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		− 65 to + 150	°C
Operating Temperature	Topr		− 20 to + 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, Topr = − 20 to + 70 °C)

PARAMETER		CONDITION	SYMBOL	Min.	Max.	UNIT
Supply voltage		NORMAL mode IDLE mode	V_{CC}	4.5	5.5	V
		SLOW mode SLEEP mode		2.7		
Input High Voltage	Normal input pin	Vcc ≧ 4.5 V	V_{IH1}	V_{CC} × 0.70	V_{CC}	V
	Hysteresis input pin	Vcc ≧ 4.5 V	V_{IH2}	V_{CC} × 0.75		
	All of degital input pin	Vcc < 4.5 V	V_{IH3}	V_{CC} × 0.90		
Input Low Voltage	Normal input pin	Vcc ≧ 4.5 V	V_{IL1}	0	V_{CC} × 0.30	V
	Hysteresis input pin	Vcc ≧ 4.5 V	V_{IL2}		V_{CC} × 0.25	
	All of degital input pin	Vcc < 4.5 V	V_{IL3}		V_{CC} × 0.10	
Clock Frequency	XIN / XOUT pin		fc	−	16.0	MHz
	XTIN / XTOUT pin		fs	30.0	34.0	kHz

D.C. Characteristics (Topr = – 20 to + 70 °C)

PARAMETER		CONDITION	SYMBOL	Min.	Typ.	Max.	UNIT
Digital Current consumption	NORMAL mode	V_{CC} = 5.5 V fc = 16 MHz, fs = 32.8 kHz	I_{CCO1}	–	30	60	mA
	IDLE mode		I_{CCL1}	–	12	25	mA
	SLOW mode	V_{CC} = 3 V fs = 32.8 kHz	I_{CCO2}	–	80	200	μA
	SLEEP mode		I_{CCL2}	–	40	100	μA
	STOP mode	V_{CC} = 5.5 V	I_{CCS}	–	0.5	50	μA
Analog Current consumption	NORMAL mode	$AV_{CC}1 = AV_{CC}2$ = 5.0 V	I_{CCA}	–	25	40	mA
High-level output voltage		V_{CC} = 4.5 V, I_{OH} = – 0.7 mA	V_{OH1}	V_{CC} – 0.4	–		V
High-level output voltage		V_{CC} = 4.5 V, I_{OH} = – 200 μA	V_{OH2}	2.4	–	–	V
Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 1.6 mA	V_{OL1}	–	–	0.4	V
Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 3.0 mA	V_{OL2}	–	–	0.4	V
Hysteresis voltage			V_{HS}	–	0.70	–	V
INPUT Leakage Current		$0V \leq Vin \leq V_{CC}$	I_{LI}	–	0.05	± 10	μA
OUTPUT Leakage Current		$0.2V \leq VOUT \leq V_{CC} - 0.2V$	I_{LO}	–	0.05	± 10	μA
$\overline{RESET}$ pin Pull-up Current		V_{CC} = 5.5 V, Vin = 0.2 V	I_{RST}	30	–	120	μA

A/D Conversion characteristic (Topr = – 20 to + 70 °C, V_{CC} = 4.5 to 5.5 V, fc = 16 MHz)

PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{REF}	V_{CC} – 1.5	V_{CC}	V_{CC}	V
	V_{AGND}	V_{SS}	V_{SS}	V_{SS}	V
Analog Input voltage	V_{AIN}	V_{ADGND}		V_{REF}	V
Supply Current for ADREF	I_{REF}	–	0.6	1.0	mA
Total error (Ta = 25 °C, $VCC = V_{REF}$ = 5.0 V)		–	–	± 3	LSB

Characteristics of CTL AMP (Topr = – 20 to + 70 °C, V_{CC} = 5.0 V)

BLOCK	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	CONDITION
CTL BIAS AMP	No load output voltage	V_{CB}	2.4	2.5	2.6	V	No load
	Output voltage (with high load)	V_{CBH}	–	–	+ 70	mV	I si = 5 mA, Difference from V_{CB}
	Output voltage (with low load)	V_{CBL}	– 70	–	–	mV	I so = – 5 mA, Difference from V_{CB}
REC CTL AMP	HIGH output voltage	V_{ROH}	3.2	–	–	V	I so = – 5 mA
	LOW output voltage	V_{ROL}	–	–	1.8	V	I si = 5 mA
	D/A CONVERTER Differential error	V_{RDA}	–	–	$\pm\frac{1}{3}$	LSB	
	SW REC internal resistance	R_{REC}	55	85	130	Ω	Set to on by SWREC
PB CTL AMP	Input offset voltage	V_{COF}	– 15	–	+ 15	mV	RPCTL terminal
	Input bias current	I_{CIB1}	– 750	–	+ 750	nA	RPCTL terminal
		I_{CIB2}	– 750	–	+ 750	nA	CNFB terminal
	HIGH output voltage	V_{COH}	3.6	–	–	V	I so = – 2 mA
	LOW output voltage	V_{COL}	–	–	1.2	V	I si = 2 mA
	Voltage gain	G_{C1}	–	60	–	dB	f : 1 kHz, Vin : 1mV, 60dB
		G_{C2}	–	51	–	dB	f : 10 kHz, Vin : 1mV, 60dB
	Feed back resistance	R_{SHORT}	5	10	20	kΩ	Fig3.20.1 (a) r3, SW internal resistance
		R_{AMP2}	20	40	60	kΩ	Fig3.20.1 (a) r4, SW internal resistance
	Resistance of Analog SW	R_{PB}	–	–	500	Ω	Set to on by SWPLY
		R_{BIAS}	–	–	500	Ω	Set to on by SWBAS
		R_{AMP0}	–	–	500	Ω	Set to on by <CAMP0>
		R_{AMP1}	–	–	500	Ω	Set to on by <CAMP1>
CTL PLUS SCHUMITTE	PDP Charge current	I_{CP}	4	–	–	mA	V_{COH} = 3.5V, V_{PDP} = 2.5V
	PDP Leakage current	I_{LP}	–	–	– 350	nA	V_{COL} = 1.5V, V_{PDP} = 2.5V R_{PDP} : OFF
	PDP Maximum output voltage	V_{OP}	4.3	4.7	–	V	Charge current : 0.1 mA
	PHSPDUP Resistance	R_{PDP}	5	10	20	kΩ	Fig3.20.1 (a) r5, r6, SW internal resistance
	1/2 level of Peak-hold Schmitt	V_{CSPA}	–	50	–	%	
	Manual Schmitt level	V_{CSP1}	–	100	–	mV	100 mV mode (to V_{CB})
		V_{CSP2}	–	200	–	mV	200 mV mode (to V_{CB})
		V_{CSP3}	–	300	–	mV	300 mV mode (to V_{CB})
		V_{CSP4}	–	500	–	mV	500 mV mode (to V_{CB})
	Noise Limit (plus)	V_{CSPL}	–	100	–	mV	to V_{CB}
CTL MINUS SCHUMITTE	PDM Charge current	I_{CM}	– 4	–	–	mA	V_{COL} = 1.5V, V_{PDP} = 2.5V
	PDM Leakage current	I_{LM}	–	–	350	nA	V_{COL} = 3.5V, V_{PDP} = 2.5V R_{PDM} : OFF
	PDM Minimum output voltage	V_{OM}	–	0.3	0.7	V	Charge current : – 0.1 mA
	PHSPDUP Resistance	R_{PDM}	5	10	20	kΩ	
	1/2 level of Peak-hold Schmitt	V_{CSMA}	–	50	–	%	
	Manual Schmitt level	V_{CSM1}	–	– 100	–	mV	– 100 mV mode (to V_{CB})
		V_{CSM2}	–	– 200	–	mV	– 200 mV mode (to V_{CB})
		V_{CSM3}	–	– 300	–	mV	– 300 mV mode (to V_{CB})
		V_{CSM4}	–	– 500	–	mV	– 500 mV mode (to V_{CB})
	Noise Limit (minus)	V_{CSML}	–	– 100	–	mV	(to V_{CB})

Characteristics of CFG AMP (Topr = − 20 to + 70 °C, V_{CC} = 5.0 V)

BLOCK	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	CONDITION
CFG BIAS AMP	No load output voltage	V_{FB}	2.4	2.5	2.6	V	No load
	Output voltage (with high load)	V_{FBH}	–	–	+ 150	mV	I si = 5 mA, Difference from V_{FB}
	Output voltage (with low load)	V_{FBL}	− 150	–	–	mV	I so = − 5 mA, Difference from V_{FB}
CFGA AMP	Input offset voltage	V_{FAOF}	− 15	–	+ 15	mV	
	Input bias voltage	V_{FAI}	− 750	–	+ 750	nA	
	HIGH output voltage	V_{FAOH}	4.3	4.7	–	V	I so = − 0.2 mA
	LOW output voltage	V_{FAOL}	–	0.3	0.7	V	I si = 0.2 mA
	Voltage gain	G_{FA1}	–	40	–	dB	f : 1 kHz, Vin : 10mV, 40dB
		G_{FA2}	–	37	–	dB	f : 10 kHz, Vin : 10mV, 40dB
CFGB AMP	Input offset voltage	V_{FBOF}	− 15	–	+ 15	mV	
	Input bias voltage	I_{FB1}	− 750	–	+ 750	nA	
	HIGH output voltage	V_{FBOH}	4.3	4.7	–	V	I so = − 0.2 mA
	LOW output voltage	V_{FBOL}	–	0.3	0.7	V	I si = 0.2 mA
	Voltage gain	G_{FB1}	–	40	–	dB	f : 1 kHz, Vin : 10mV, 40dB
		G_{FB2}	–	37	–	dB	f : 10 kHz, Vin : 1mV, 40dB
CFGA SCHMITT	P Schmitt Voltage 1	V_{FASP1}	–	80	–	mV	80 mV mode (to V_{FB})
	P Schmitt Voltage 2	V_{FASP2}	–	120	–	mV	120 mV mode (to V_{FB})
	M Schmitt Voltage 1	V_{FASM1}	–	− 80	–	mV	− 80 mV mode (to V_{FB})
	M Schmitt Voltage 2	V_{FASM2}	–	− 120	–	mV	− 120 mV mode (to V_{FB})
CFGB SCHMITT	P Schmitt Voltage 1	V_{FBSP1}	–	80	–	mV	80 mV mode (to V_{FB})
	P Schmitt Voltage 2	V_{FBSP2}	–	120	–	mV	120 mV mode (to V_{FB})
	M Schmitt Voltage 1	V_{FBSM1}	–	− 80	–	mV	− 80 mV mode (to V_{FB})
	M Schmitt Voltage 2	V_{FBSM2}	–	− 120	–	mV	− 120 mV mode (to V_{FB})

Characteristics of OSD AMP (Topr = – 20 to + 70 °C, V_{CC} = 5.0 V)

OUTPUT PIN	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
SC	Bias voltage	V_B	–	2.5	–	V	
	Burst amplitude	V_b	–	0.29	–	V (PP)	
	Chroma amplitude 1 / Burst amplitude	V_1 / V_b	–	2.0	–	–	
SY	Sync. tip level	V_S	–	1.60	–	V	
	Sync. to Pedestal	$\triangle V_{SP}$	–	0.60	–	V	$\triangle V_{SP} = V_P - V_S$
	Sync. to Luminance voltage 0	$\triangle V_{S0}$	–	0.66	–	V	$\triangle V_{S0} = V_0 - V_S$
	Sync. to Luminance voltage 1	$\triangle V_{S1}$	–	0.80	–	V	$\triangle V_{S1} = V_1 - V_S$
	Sync. to Luminance voltage 2	$\triangle V_{S2}$	–	1.08	–	V	$\triangle V_{S2} = V_2 - V_S$
	Sync. to Luminance voltage 3	$\triangle V_{S3}$	–	1.50	–	V	$\triangle V_{S3} = V_3 - V_S$
	Sync. to 100% White Level	$\triangle V_{SW}$	–	2.00	–	V	$\triangle V_{SW} = V_W - V_S$
OSD VIDEO	Color Burst amplitude	V_{Cb}	–	0.29	–	V_{P-P}	
	Chroma amplitude / Burst amplitude	V_C / V_{Cb}	–	2.0	–	–	
	Sync. tip level	VI_S	–	1.00	–	V	
	Sync. to Pedestal	$\triangle VI_{SP}$	–	0.30	–	V	$\triangle VI_{SP} = VI_P - VI_S$
	Sync. to Luminance voltage 0	$\triangle VI_{S0}$	–	0.33	–	V	$\triangle VI_{S0} = VI_0 - VI_S$
	Sync. to Luminance voltage 1	$\triangle VI_{S1}$	–	0.40	–	V	$\triangle VI_{S1} = VI_1 - VI_S$
	Sync. to Luminance voltage 2	$\triangle VI_{S2}$	–	0.54	–	V	$\triangle VI_{S2} = VI_2 - VI_S$
	Sync. to Luminance voltage 3	$\triangle VI_{S3}$	–	0.75	–	V	$\triangle VI_{S3} = VI_3 - VI_S$
	Sync. to 100% White Level	$\triangle VI_{SW}$	–	1.00	–	V	$\triangle VI_{SW} = VI_W - VI_S$

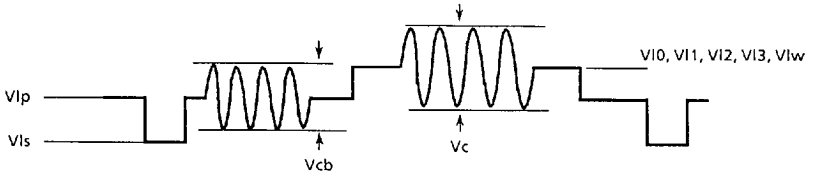


Fig. 4.1 OSD VIDEO Output Waveform

Characteristics of PV/BLK (Topr = − 20 to + 70 °C, V_{CC} = 5.00 V)

MODE	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	CONDITION
MIXOFF = 0	HIGH output voltage	V_H	4.70	–	5.00	V	I = + 100 μA
	MIDDLE-HIGH output voltage	VM2	3.00	3.30	3.60	V	I = ± 10 μA
	MIDDLE-LOW output voltage a	VM1a	1.30	1.60	2.0	V	I = ± 100 μA
	MIDDLE-LOW output voltage b	VM1b	1.30	1.60	2.0	V	I = ± 10 μA
	LOW output voltage	V_L	–	–	0.30	V	I = − 100 μA
MIXOFF = 1	HIGH output voltage	V_H	4.70	–	–	V	I = + 100 μA
	LOW output voltage	V_L	–	–	0.30	V	I = − 100 μA

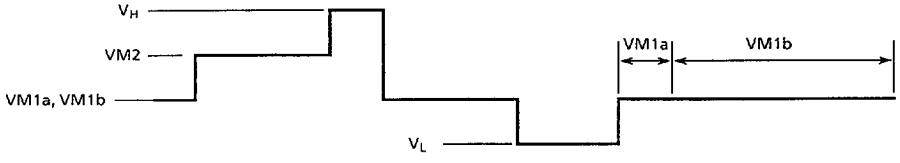


Fig. 4.2 PV / BLK Output Waveform