

Dual Voltage Controlled Oscillators

General Description

The DM54LS124/DM74LS124 features two fully independent voltage-controlled oscillators (VCO's) in a single monolithic chip. The output frequency of each is established by a single external component, either a capacitor or a crystal, in combination with two voltagesensitive inputs, one for frequency range and one for frequency control. An enable input is provided that can be used to start or stop the output pulses when it is low or high, respectively. The internal oscillator runs continuously, even while the output is disabled. A pulse synchronizer ensures that the first output pulse is neither clipped nor extended. Duty cycle of the output pulses is fixed at approximately 50 percent.

The highly stable oscillator can be set to operate at any frequency between 0.12 Hz and 50 MHz typically. The output frequency can be approximated as follows:

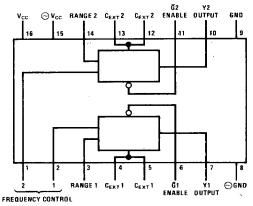
$$f_O = \frac{500}{C_{EX}}$$

where: $f_O = \text{output frequency in MHz}$ $C_{\text{EXT}} = \text{external capacitance in pF}$ The enable input and the buffered output operate at standard Schottky-clamped TTL levels. The enable input is one standard load in each series. Although these devices can operate from a single 5-volt supply, separate supply-voltage and ground pins are provided for the digital logic and for the oscillator/range control circuits so that effective isolation can be accomplished in the system.

Features

- Two fully independent VCO's in a 16-pin package
- Output frequency set by single external component:
 Crystal for high-stability fixed-frequency operation
 Capacitor for fixed- or variable-frequency operation
- Separate supply voltage pins for isolation of inputs and oscillators from logic circuitry
- Stable operation over specified temperature and/or supply voltage ranges

Connection Diagram



Note: While the enable input is low, the output is enabled. While the enable input is high, the output is high.

54LS124/74LS124(J), (N), (W)

Tentative Data

To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS		DM54 LS124			DM74 LS124			UNITS
VIH	High Level Input Voltage at Enable				2			2			V
VIL	Low Level Input Voltage at Enable						0.7			0.8	V
V,	Input Clamp Voltage at Enable		V _{CC} = Min, I ₁ =18 mA				-1.5			-1.5	l v
Іон	High Level Output Current				1		-1.2	-		-1.2	mA
VoH	High Level Output Voltage		V _{CC} = Min, V _{IH} = 2V, I _{OH} = -1.2 mA		2.5	3.4		2.7	3.4		V
loL	Low Level Output Current						12			24	mA
VOL	Low Level Output Voltage		V _{CC} = Min, V _{ENABLE} = V _{IL}			0.25	0.4		0.25	0.4	—
		· · · · · · · · · · · · · · · · · · ·	Pins 4 and 13 = V _{CC} (Min)-2V	I _{OL} = 24 mA					0.35	0.5	\ \ \
Ц	Input Current	Freq Control	V _{CC} = Max	V ₁ = 5V	<u> </u>	50	250		50	250	μΑ
		or range		V _i = 1V		10	50		10	50	
lı .	Input Current at Maximum Input Voltage	Enable	V _{CC} = Max, V ₁ = 7V				0.1			0.1	mA
I _{tH}	High Level Input Current	Enable	$V_{CC} = Max, V_1 = 2.7V$				20			20	μΑ
I _{IL}	Low Level Input Current	Enable	V _{CC} = Max, V _I = 0.5V		<u> </u>		−0.4			-0.4	mA.
los	Short Circuit Output Current		V _{CC} = Max, V _{ENABLE} = 4.5V(2)		-30		-150	-30		-150	mA
†cc	Supply Current, Total into Pins 15 and 16		V _{CC} = Max(3)			22	37		22	37	mA
V _I	Input Voltage at Frequency Control or Range Input				0		5	0		5	

Notes

- (1) All typical values are at $V_{CC} = 5V$, $T_A \approx 25^{\circ}C$.
- (2) Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- (3) I_{CC} is measured with the outputs disabled and open.

Switching Characteristics V_{CC} = 5V, R_L = 667 Ω , C_L = 45 pF, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
fo	Output Frequency	C _{E×T} ≈2pF	$V_{I(FREQ)} = 5V$, $V_{I(RNG)} = 0V$ $V_{I(FREQ)} = 0V$, $V_{I(RNG)} = 5V$	35	50		MHz
	Output Duty Cycle	C _{EXT} = 8.3 pF to 500µF		 ''	50%		
1 _{PHL}	Propagation Delay Time, High-to-Low Level Output From Enable	f _o ≥ 1 Hz			30+(4)		ns

Notes

(4) The delay will typically be 30 ns plus up to one half the period of one cycle (i.e. 30 ns to 30 ns $^{\frac{3}{4}}$ 5 x $10^8/f_{o(Hz)}$) depending upon the timing of the enable pulse with respect to the signal generated by the internal oscillator.