5902

DATA AND SPECIFICATIONS
DESCRIPTION AND INSTRUCTIONS

Optical Electronics Incorporated

PEAK SENSE AND HOLD ANALOG MEMORY

FEATURES

- FAST ACQUISITION: 10V step in 1.5 μs
- GATE ON TIME: 50ns
- RESET TIME: 50ns
- BANDWIDTH: DC - 300KHz

APPLICATIONS

- DATA ACQUISITION
- PULSE STRETCHER
- VIDEO PEAK SENSE
- NOISE MEASUREMENT

DESCRIPTION

The 5902 Peak Sense and Hold Analog Memory provides an output DC voltage equal to the positive peak value of an analog input signal. Because of the rapid reaction of the built-in switches, even pulse like signals can be sampled. The 5902 functions, in general, similar to two other OEI devices, the 5030A and the 5032A. Unlike them, however, it is packaged in a 16 pin DIP package and is slower. It, therefore, finds applications in data acquisition systems in the audio range, peak to peak measurements of absolute values, heat sensors and in sonar applications up to 50KHz.

The 5902 operates at +10 Volt input and output signal, and operates on a positive polarity only. The useful input bandwidth is 300KHz and the sensing error is ±50mV.

There is one other area where this device differs from its faster counter-parts. There is no internal charge capacitor provided, i.e. to make this device operable, a charge capacitor must be provided externally. The advantage, of course, is that the designer has complete freedom to choose the value of this very important part. It is recommended that an NPO type be used.

The 5902 can acquire a continuously sinusoidal wave shape of up to 10V at 300KHz. This should be interpreted to mean that a one half sinusoid can be acquired at 1.5μs. However, a pulse train with 100ns wide pulses can also provide a DC restoration output. when several pulses are sampled. Reset, gate turn on and gate turn off times are guaranteed at 50ns, 50ns, and 500ns respectively.

The error performance of the 5902 is, as mentioned, somewhat different, but input signals of down to 100mV can be processed. When signal levels become this small, good power supply bypassing is a must, because positive noise on the signal can raise havoc with the accuracy of the sampled output. In general, if low signal levels or accuracies of better than 3-5% are required, the use of the 5902 is not recommended.

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

MODEL	5902			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
Voltage	0.1		+10V	V
Resistance		1		MΩ
Reset Command Voltage		2	5	V
Gate Open		2	5	V
Peak Sense Command Voltage		0	0.8	V
Command Load		1.5	2	mA
RATED OUTPUT				
Voltage	+10V			V
Current	6			mA
Output Resistance			200	Ω
DYNAMIC RESPONSE				
Continuous Sinusoidal			300	KHz
Acquisition Time; 10v Step		1500		nsec
Reset Time		50		nsec
Gate Turn On Time		50		nsec
Gate Turn Off Time		500		nsec
MEMORY DECAY RATE				
Decay Rate		100		mV/mS
INPUT ERROR				
Offset Voltage		ADJ		
Gain Error		3		%
Sensing Error		50		mV
POWER SUPPLY				
Rated Voltage	±10	±15	±20	V
Current Quiescent		12		mA
TEMPERATURE RANGE				
Operating	-25		+85	°C
Storage	-65		+100	°C
Thermal Resistance			20	°C/W
Quiescent Rise*			20	°C

*Quiescent Rise is temperature above ambient

Because of the unique gating of the input signal, the device can be placed in a "Hold" mode, whereby the output voltage remains constant and is, thus, independent of the signal at the input. A reset function returns the signal voltage to zero.

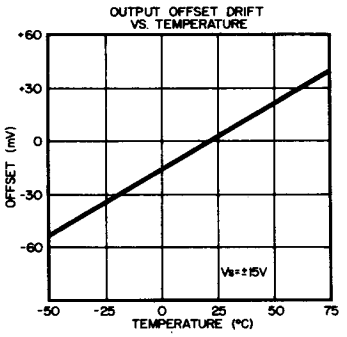
The device has positive input voltage requirements. If negative going voltages could be encountered in an application, it is advisable to include a clipping diode in the design of the input lines.

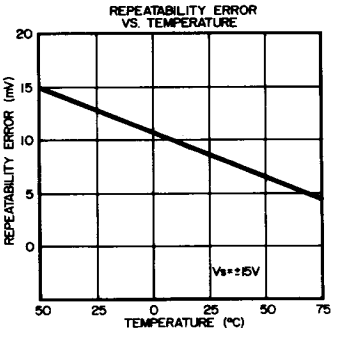
Offset adjustments can be accomplished by use of a trimpotentiometer of 1k ohm to the negative rail of the power supply.

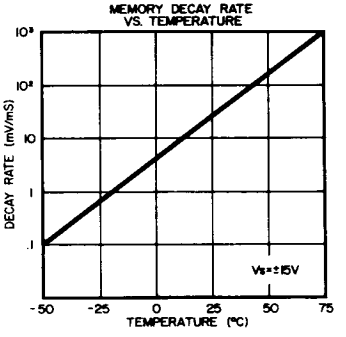
Layout for the 5902 is most critical. Refer to the end of the applications section for more details on this subject.

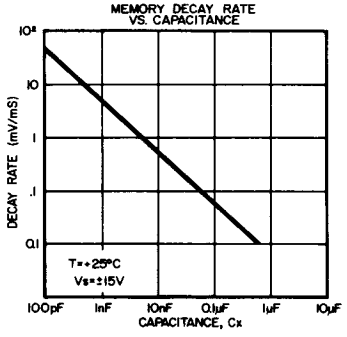
5902
TYPICAL PERFORMANCE CURVES

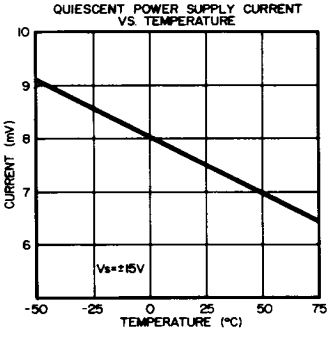
(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)



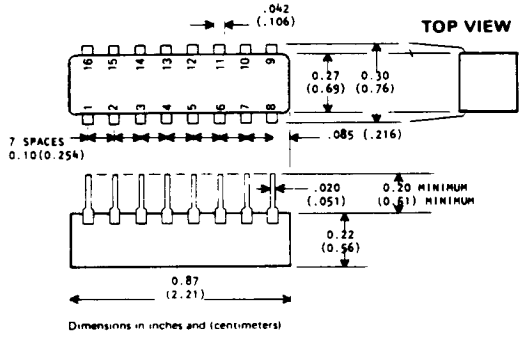








MECHANICAL DESCRIPTION: The 5090A uses a standard 16-pin DIP. The pins are compatible with standard 0.3-inch dual in-line sockets. The case is made of glass-fiber-filled diallyl-phthalate and is filled with an epoxy encapsulant.



PIN CONNECTIONS
1 INPUT
3 GATE
4 RESET
5 COMMON
7 Cx
8 -Vs
9 TRIM
10 OUTPUT
16 +Vs

FUNCTIONAL DESCRIPTION AND APPLICATIONS

The 5902 Positive Peak Sample and Hold Memory is a semiconductor device packaged in a 16 pin DIP package. The 5902 exhibits parameters that make it applicable at frequency rates that are complementary to the faster 5030A or the 5032A OEI devices.

It has a unity gain from input to output. As the block diagram in Figure 1 shows, it consists functionally of five distinct parts:

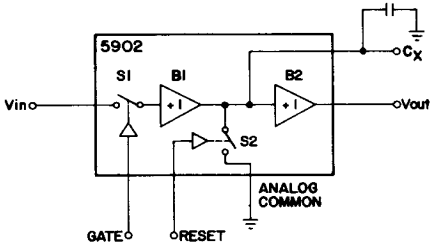


FIGURE 1: FUNCTIONAL BLOCK DIAGRAM

The input is gated on and off by a semiconductor switch SI that, as noted before, is driven by typical TTL logic levels. The gate, when closed, applies the input to the front end buffer BI. The input buffer provides a unity gain amplification to the signal and is capable of delivering the charge current to the external charge capacitor C_X, which is connected between the output of the buffer and ground. This outboard capacitor C_X, should be connected between this pin and analog common ground, and should, for a minimum dielectric leakage, be of the NPO type. **Across the capacitor, a reset semiconductor switch S2 is installed, which allows rapid discharge of the capacitor, thus setting the sampled (and held) voltage to zero. This, then, also sets the output voltage to zero.**

The voltage on the capacitor is sampled by an FET follower amplifier. This output amplifier, designed with low bias current to reduce errors in this stage, also provides a unity gain. Thus, overall gain from input to output is unity. The **device is unipolar, i.e. it responds to positive** voltages only. If the possibility of negative voltages is suspected, it is advisable to include a clipping diode on the input to the device. Any high grade switching diode, such as the 1N914/ 1N4148 will do fine.

In operation input voltages from +100mV to +10V (40dB dynamic range) can be applied to be sampled. The lower limit is dictated by an accumulation of gain and sensing errors and an additional offset. Sensing error is defined as repeatability from measurement to measurement for a like signal level. Although not guaranteed, this lower input limit will typically go to +30mV. The designer should be careful to make some measurements, if the devices are used at such a low input voltage, to assure accuracy requirements are still met. If necessary, an amplifying stage could precede the peak sense memory. Care must be taken that the preamplifier is chosen to match the input signal and the 5902 functionally.

The 5902 operates as follows: When S1, the gating switch, and S2, the reset switch, are closed, the input is referenced to ground and no signal can enter the device. When the reset switch S2 is open, information from the input is allowed through the input buffer, and the charge capacitor can then charge to the peak value of the input signal. When the capacitor has charged to the peak value, S2 can be opened to retain that voltage on the capacitor and the output of the device then presents this value. Closing the reset switch will dump the charge on the capacitor to ground, thus also zeroing the output and readying the device for the next peak sense cylce. The timing diagrams in Figure 2 exemplify these operations.

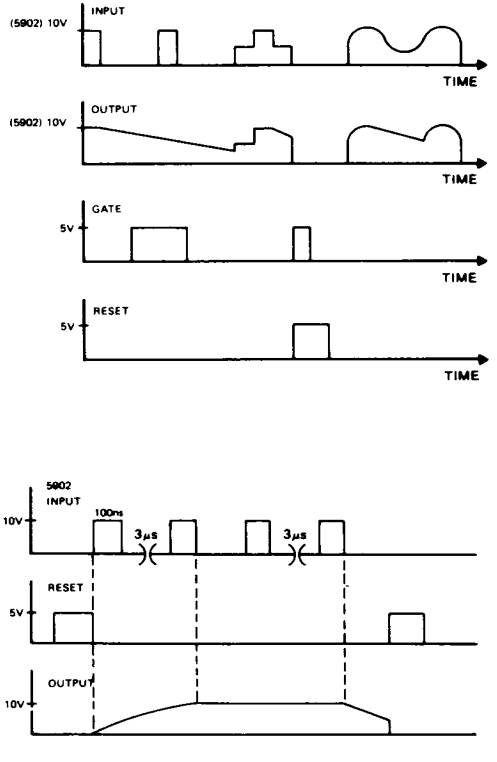


FIGURE 2: BASIC SIGNAL TIME RELATIONSHIPS

When designing with the 5902, the droop rate must, of course, be taken into account. To decrease droop and, at the same time, increase the acquisition time of the device, the value of Cx can be increased. As for all sample and hold applications, capacitors exhibiting low leakage and low dielectric absorption (NPO type) should be used. Typically, capacitors with polysterene, Teflon®, polycarbonate, polypropilene, or MOS dielectric are best suited. To aid in the selection of values, typical performance curves are given, which show the influence of Cx on decay rate and acquisition time.

The power supply leads in the 5902 are not decoupled internally. Therefore, external bypass capacitors are needed. Particularly, if other wideband devices are connected to the same power supply lines, use of a high capacitance, solid tantalum, bypass capacitor becomes a necessity. Values of 10μF to 15μF are recommended. Medium and high frequency noise can be filtered by additionally paralleling 0.1μF and 330pF capacitors on both rails to ground. Positive and negative supply lines should be bypassed and connections should be made as closely as possible to the memory devices. The speed of the device is influenced by the output load as well as by the input source impedance, and maximum speed can be expected with a source impedance of less than 50 ohms.

PEAK LIGHT LEVEL SENSING

In noisy industrial environments, it is often useful to use light and fiber optics devices for long signal lines. Other requirements, too, can dictate the use of light (or infrared) sensors for particular circumstances. In either case, the OEI device can fill the bill as a peak sense and hold memory. Since photo detectors usually operate on a variable current basis, a translation to a voltage is required. This is accomplished by a bias resistor at the input to the device as shown in Figure 3.

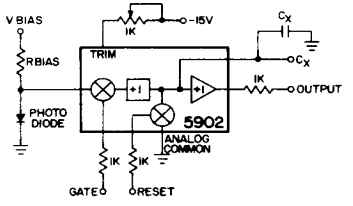


FIGURE 3: PEAK LIGHT LEVEL SENSING

The circuit depicts the device in an application, where the peak timing is known. If that is not the case, an "alert circuit" can be made as is shown later in this section.

The circuit shown is essentially a scaling device, the output of which can now be connected to an A/D converter or other device. As with all sample and hold devices, the charge capacitor Cx determines acquisition time and droop rate in a proportional fashion. Pins 8 and 9 are connected to the 1K ohm trim potentiometer. This potentiometer, in reality, adjusts the current in an internal current source. The resistors on pins 3 and 4 are current mixers on the control lines. They also help eliminate potentially possible feedthrough on these lines. A TTL low voltage activates sense, a high level activates the inhibit mode of operation.

MULTIPLEXED INPUT SIGNAL

For many occasions, several different signals need processing for their peak values. In such an instance, these signals can be multiplexed with analog switches. This reduces circuit complexity and cost.

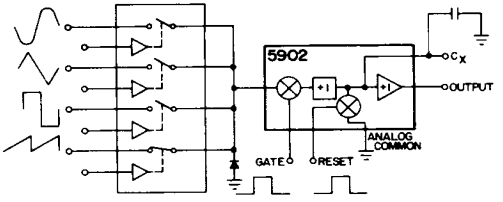


FIGURE 4: MULTIPLEX INPUT SIGNAL

Quad SPST CMOS analog switches that can easily qualify are the DG308, produced by Siliconix or the HI201 from Harris. Typical turn on and turn off times are 130ns and 90ns for the Siliconix device and 185ns and 220ns for the Harris device. Of course, these low switching times may not be needed in a particular application. One of these devices will allow for signals to be accessed and they can be ganged if more than four signals need to be processed. Switches, as well as the peak sense memories, can be controlled from a command center, consisting of discrete logic, a minicomputer, or microprocessor. Commands can be sent to the memory device to either peak sense or hold. The sampled voltage, fed to the hold capacitor, is then routed to the output via the FET follower and presented to an oscilloscope, DVM, analog to digital converter, or other device. Trim adjustments allow accurate offset nulling. The choice of Cx is critical in any application when the full bandwidth of the device is needed. Also, with increasing values of Cx, the acquisition time increases and the droop rate decreases, trade offs that must be considered when this capacitor value is selected.

PEAK SENSE AND HOLD WITH GAIN

In another typical combination of devices, shown in Figure 4, an AH0605, produced by OEI, is combined with the peak sense memory device because of the AH0605's excellent speed and

bandwidth capabilities. This combination can be used when the voltage to be sensed is too low to fit inside the specification limits of the 5902.

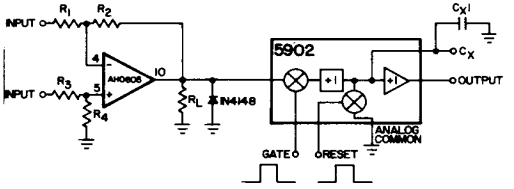


FIGURE 5: PEAK SENSE & HOLD WITH GAIN

The circuit shown in Figure 5 provides a gain of 1000 when the ratio of R_2/R_1 = 1000. The other resistors are R_3 = 1000 ohms and R_4 = 100k ohms. The load resistor R_L is selected to match the output of the AH0605 to the input of the 5902. The 1N4148 prevents any negative going voltages to reach the input and, thus, the charge capacitor. Here, as in other applications, analog common and digital common can be tied together. This should be done at one point only. Although not a necessity, it is recommended to bypass the power supply lines near the two devices. The value of Cx can be increased if the acquisition time needs to be extended or the droop rate be improved. Refer to the last application of this series for an example of droop rate improvement without the attendant penalties of decreased bandwidth and longer acquisition times.

PEAK SENSE AND HOLD WITH INTEGRATOR

Figure 6 shows the 5902 in an application with an integrator.

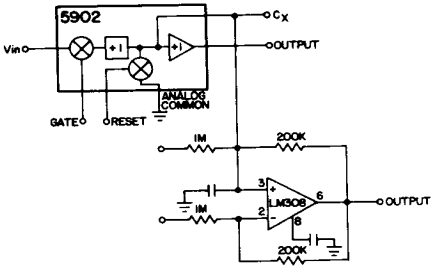


FIGURE 6: INTEGRATOR WITH PROGRAMMABLE RESET LEVEL

The integrator sets initial conditions. Cx is located at the summing node of the non-inverting input of the integrator and only charging and reset functions of the memory device is used. In essence, the 5902 functions as a charge and reset control for Cx. Thus a signal can be sampled and its amplitude superimposed on the initial conditions set by the integrator. The circuit can be used to set a given zero crossing to another, i.e. if there is a differential voltage between the sampled signal and the point where that sample should be further processed, the integrator can operate as a level adjuster.

PEAK SENSE AND HOLD, LOW DROOP RATE

A very interesting circuit is presented in Figure 7. This circuit allows the user to take full advantage of the rapid sampling capability of the 5902 and still enables interface to devices with slower processing speeds, such as analog to digital (A/D) converters. Therefore, slower and thus less expensive devices can be used, rather than faster and more expensive converters.

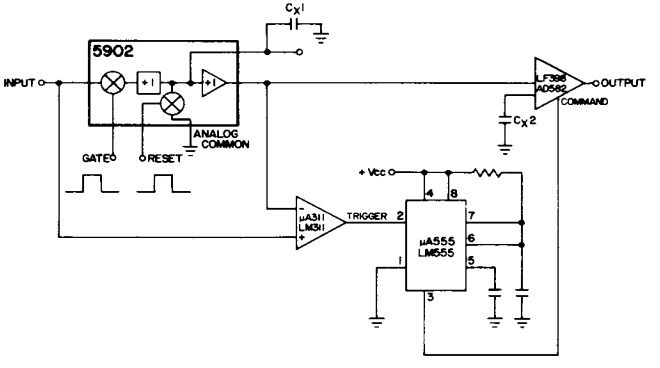


FIGURE 7: FAST ACQUISITION PEAK SENSE & HOLD WITH LOW DROOP RATE

Of course, there is a delay associated with this process and, even though the signal peaks can and will be recorded, there will be a delay of several hundred nanoseconds from the signal peak to the registration of the sensed value at the devices output. As shown, the circuit consists essentially of 6 parts. The 5902, the first charge capacitor Cx, a comparator, a timing device, the second charge capacitor Cx2, and a monolithic sample and hold device. In operation, the OEI devices are set to work at or near the limits of their characteristics. Very rapid sense operations require small values of Cx and, thus, will also result in relatively rapid decay of the voltage on this capacitor. To lengthen the overall droop rate, the 5902 is backed up with a slower sample and hold device which is outfitted with a larger Cx2. This, then, increases the acquisition time and improves droop rates. For example, the droop rate for the 5902 can be as high as 100mV/ms. The LF 398, on the other hand, can operate with a droop rate that is equal or better than 1μV/ms, and improvement of 100,000:1. Thus an A/D converter that could follow the two S&H devices can be much slower, the accuracy is maintained and the speed of the data acquisition can still be taken advantage of. The A/D converter should, however, not exceed 8 bits of conversion, because the error on the 5902 can be around $\pm$1mV and the S&H error of the slower device must still be added to this.

The problem now becomes one of controlling this arrangement. This is where the combination of comparator and timer enters the picture. They act as an alert system. As long as the input of the 5902 is higher than its output, the comparator output is low and nothing happens. When the output reaches the threshold value of the comparator, its output flips to a high state, thus triggering the 555, which is connected as a monostable flip-flop. When triggered, the output of the 555 goes low, thus giving the S&H device the go ahead for sampling to start. Its time constant is selected long enough to allow Cx2 to charge fully and to complete the sampling process.

Of course, if the 5902 were controlled from a microprocessor, the S&H commands could be served by an interrupt routing, triggered by the comparator, but this circuit frees the μP from yet an additional chore and more software with the associated overhead.

Gate and reset functions are based on the assumption that timing is known. The charge capacitor Cx will, by its value, determine acquisition time and droop rate. Trim adjustments are best done when a dynamic signal is applied. Although the reset switch is referenced to ground, trim adjustments made in the static mode seem not confirmable in the dynamic mode. Signals can easily be sampled to about 300kHz (continuous sinusoidal). If the acquisition time is considered to be 1.5μs, the designer cannot go wrong. This time takes into consideration all factors, and is valid, even though the gate and reset switches operate at nanosecond speeds.

PEAK MEASUREMENTS, ABSOLUTE VALUES

The 5902 can also be used for the measurement of absolute values. A circuit for this application is shown in Figure 8.

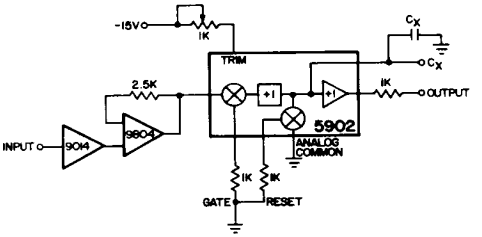
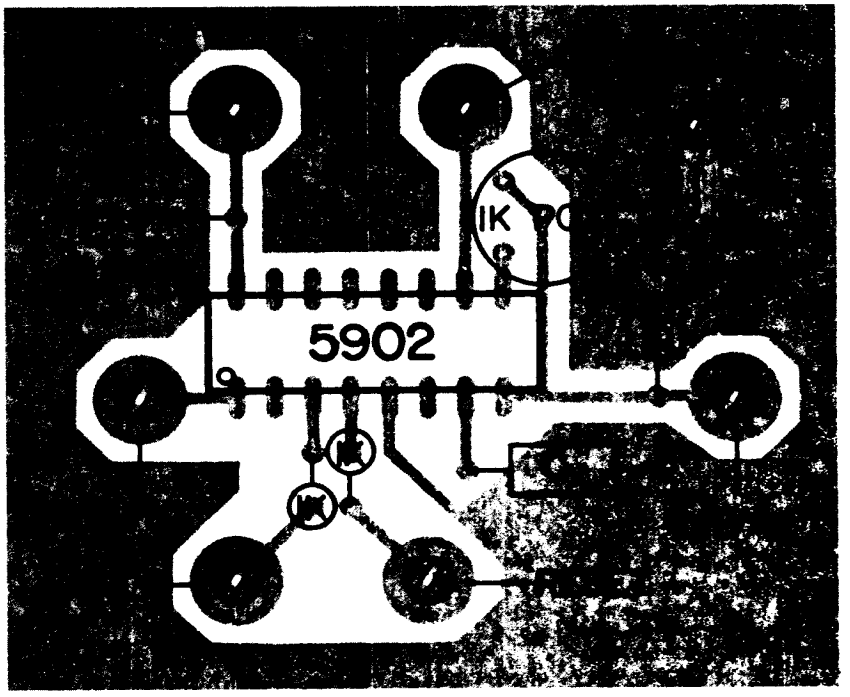


FIGURE 8: PEAK MEASUREMENT OF ABSOLUTE VALUES

The design philosophy is based on the assumption of a bipolar input signal. A full wave rectification not only gives the single sided positive peaks needed by the unipolar 5902, but also doubles the frequency that can be sampled. This will allow use of the slower part. Other OEI devices, namely the 5030A and 5032A, are available to cover higher frequency ranges. The 9014 and the 9804 are connected as a full wave rectifier. Gate and reset functions are connected to provide free running information. Bypass, time and charge capacitor functions are as mentioned above.

If the time of peak occurrence is not known, an alert system, mentioned above can be used. Also, the droop rate can be improved by the addition of another, slower sample and hold system with its own charge capacitor. It could be activated by the alert circuit or by other logic, either discrete or in the form of a mini or micro processor.

Refer to the application notes on the 5030A and the 5032A from OEI for more details on the alert and secondary sample and hold circuits.



TYPICAL COMPONENT BOARD LAYOUT

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