TECHNICAL BRIEF

O K I N E T W OS R K P R O D U C T

W722 USB Hub/Compound Device Controller 0.5 µm Technology Megamacro Function

August 1997

Oki Semiconductor

Contents

Oki Semiconductor

W722 USB Hub/Compound Device Controller

0.5 μm Technology Megamacro Function

DESCRIPTION

Oki's W722 Universal Serial Bus (USB) Hub/Compound Device Controller Megamacro Function is a featured element in Oki's 0.5 μm Sea of Gates (SOG) and Customer Structured Array (CSA) families.

The W722 provides Oki's Serial Interface Engine (SIE), a Hub Core Controller (HCC), a Hub Repeater (HR), and a status/descriptor/register file block in four highly integrated submodules. The submodule partitioning allows custom configurations to be easily developed. Oki also offers optional USB FIFO Controller and Application Interface Logic Modules to form a USB Compound Device function.

FEATURES

- USB v1.0 compliant.
- Supports up to four downstream ports (expandable).
- Can replace external downstream ports with internal ports to interface with embedded functions.
- Supports any combination of low-speed (1.5 Mbps) and full-speed (12 Mbps) downstream ports.
- Hub function supports one control endpoint and one interrupt endpoint.
- Embedded function supports 1 control end point and 6 additional endpoint addresses, expandable up to 32 endpoint addresses.
- Auto-sensing capability for power sources can behave as either a self-powered or bus-powered hub.
- Individual port power switching capability for bus-powered hubs.
- Individual port over-current protection mechanism and individual port over-current indicator for self-powered hubs.
- Supports remote-wakeup feature initiated by the hub itself, the embedded function, or the downstream devices.
- Built-in (dynamic phase-locked loop (DPLL); interface for optional external DPLL.

Supported ASIC Families

Family Name	Family Type
MSM13R0000	Sea of Gates
MSM98R000	Customer Structured Array

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Min.	Typical	Max.	Unit
Power supply voltage	V_{DD}	2.7	3.3	3.6	V
Operating temperature	T_j	-40	+25	+85	°C

Megamacro Function Characteristics

Megamacro Function	Description	Logic Gate Count	Logic Pin Count
W722	USB Hub/Compound Device Controller	15K [1]	154 [2]

1. The hub controller has 15K gates, with an additional 12K gates for the optional embedded function, FIFO control, and application interface logic.
2. Pin count is based on three downstream ports and one embedded function.

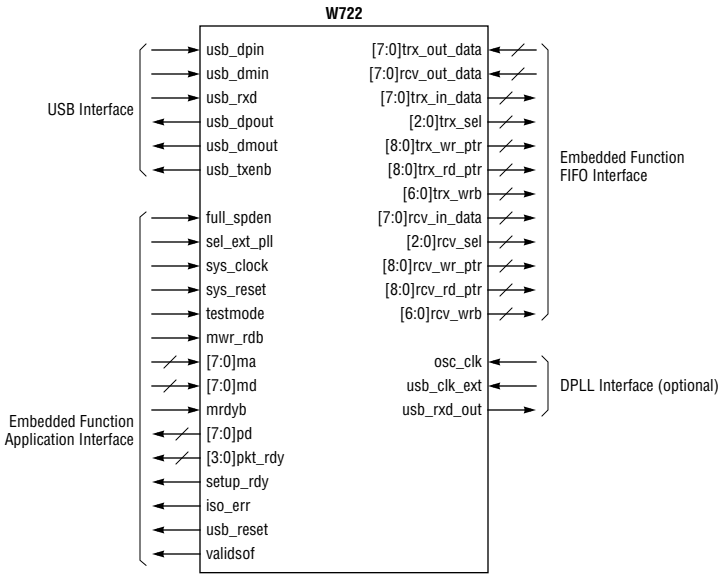

Figure 1. W722 Logic Symbol

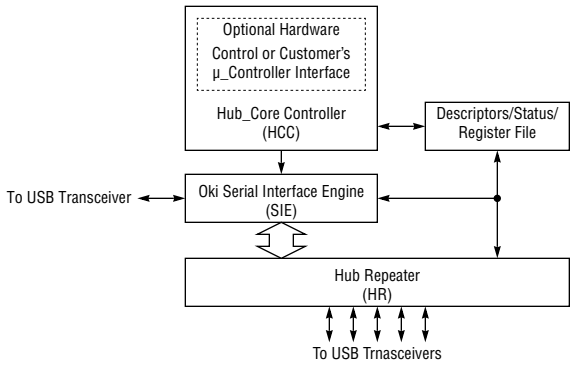

Figure 2. W722 Block Diagram

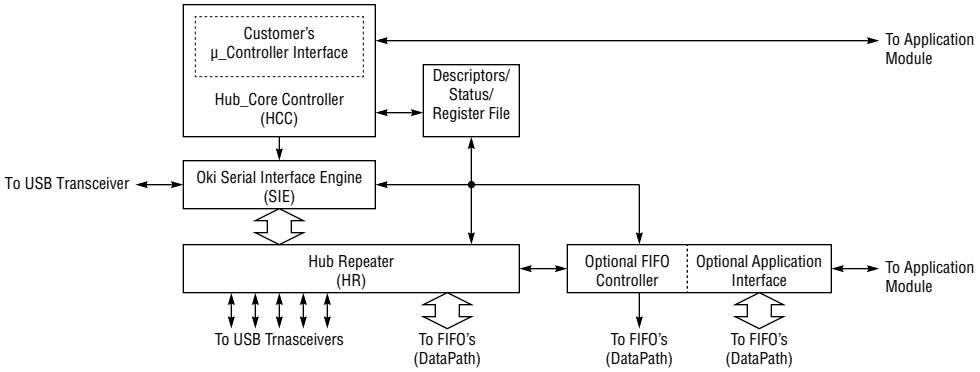

Figure 3. W722 Block Diagram with Optional Modules

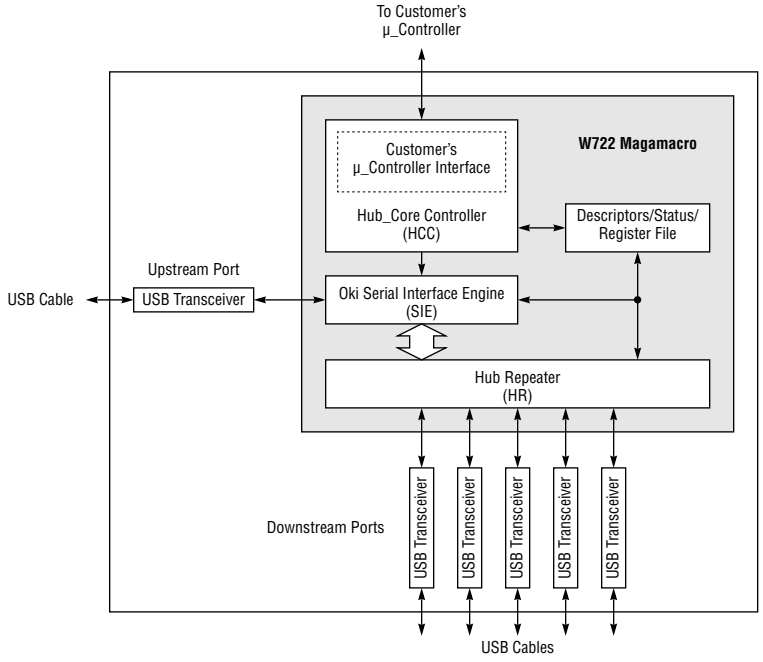

Figure 4. A USB Hub Megamacro Function Application (Standalone Hub) Example

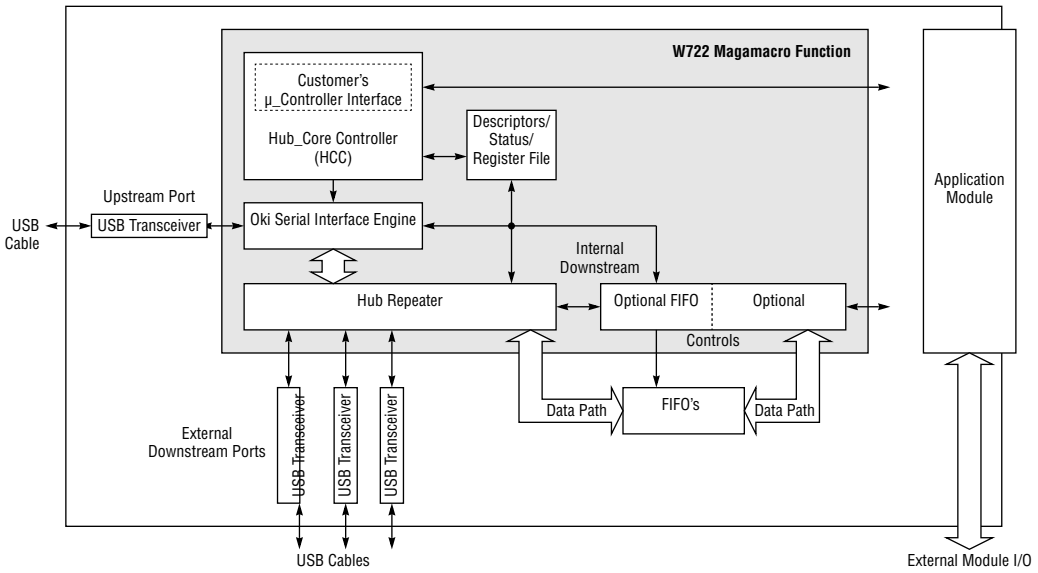

Figure 5. A USB Hub Megamacro Function Application (Compound Device) Example

SIGNAL DESCRIPTIONS

USB Interface

<table>
<tr><th>Signal</th><th>Type</th><th>Assertion</th><th>Description</th></tr>
<tr><td>[n:0] [1]usb_dpin</td><td>Input</td><td>—</td><td>USB Data Plus In. This input and the [n:0]usb_dmin input are the received single-ended data from the USB transceiver. The table below shows values and results for these signals.
<table>
<tr><th>usb_dpin</th><th>usb_dmin</th><th>Result</th></tr>
<tr><td>0</td><td>0</td><td>SE0</td></tr>
<tr><td>0</td><td>1</td><td>Logic “0”</td></tr>
<tr><td>1</td><td>0</td><td>Logic “1”</td></tr>
<tr><td>1</td><td>1</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>[n:0]usb_dmin</td><td>Input</td><td>—</td><td>USB Data Minus In. This input and the [n:0]usb_dpin input are the received single ended data from the USB transceiver. See the table above for the description, values, and results of the usb_dpin signals.</td></tr>
<tr><td>[n:0]usb_dpout</td><td>Output</td><td>—</td><td>USB Data Plus Out. This output and the [n:0]usb_dmout signal come from the USB transmit engine and drive the differential output buffers. The table below shows values and results for these signals.
<table>
<tr><th>usb_dpout</th><th>usb_dmout</th><th>Result</th></tr>
<tr><td>0</td><td>0</td><td>SE0</td></tr>
<tr><td>0</td><td>1</td><td>Logic “0”</td></tr>
<tr><td>1</td><td>0</td><td>Logic “1”</td></tr>
<tr><td>1</td><td>1</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>[n:0]usb_dmout</td><td>Output</td><td>—</td><td>USB Data Minus Out. This output and the [n:0]usb_dpout signal come from the USB transmit engine and drive the differential output buffers. See the table above for the description, values, and results of the usb_dpout signals.</td></tr>
<tr><td>[n:0]usb_rxd</td><td>Input</td><td>—</td><td>USB Differential Received Data. This input comes from the USB differential receiver, and connects to the W722 Megamacro Function.</td></tr>
<tr><td>[n:0]usb_txenb</td><td>Output</td><td>LOW</td><td>USB 3-State Output Enable. This signal connects to the transceiver EB input through an inverter gate. When the W722 Megamacro function asserts this signal LOW, the transceiver transmits data on the USB bus. See Appendix for the USB transceiver Data Sheets.</td></tr>
</table>

1. n = number of downstream ports.

{usb_dpin[0], usb_dmin[0], usb_dpout[0], usb_dmout[0], usb_rxd[0], usb_texnb[0]}: USB upstream port interface

{usb_dpin[i], usb_dmin[i], usb_dpout[i], usb_dmout[i], usb_rxd[i], usb_txenb[i]}, for i from 1 to n, is the USB downstream port interface for port i.

Application Interface

Signal	Type	Assertion	Description
sys_clock	Input	—	**Clock**. Attach a 12-MHz clock signal to this input for full-speed operation and 1.5-MHz clock signal for low-speed operation.
sys_reset	Input	HIGH	**W722 Reset.** Asserting this signal HIGH resets the W722 Megamacro Function. The application module is required to assert this signal at power-on.
mwr_rdb	Input	—	**Write/Read Select.** When external application logic asserts this signal HIGH, the application is in WRITE mode. When asserted LOW, the application is in READ mode. External application logic asserts this signal HIGH when writing data to the transmit FIFOs or to the register files. External application logic asserts this signal LOW when reading data from the receiving FIFOs or from the register files. The register files contain information describing the function and transaction status.
usb_reset	Output	HIGH	**USB Reset**. This is the reset signal from the USB device controller.
[7:0]ma	Input	—	**Address Bus.** These eight inputs receive the address of the register files in the USB device controller.
[7:0]md	Input	—	**Input Data Bus.** These eight inputs receive the data to be stored in the register files or transmit FIFOs.
mrdyb	Input	LOW	**Data Strobe.** When asserted LOW and in WRITE mode, the data on the [7:0]md signal lines are valid for writing. When asserted LOW and in READ mode, the data on the [7:0]pd signals are valid for reading.
[7:0]pd	Output	—	**Output Data Bus**. These eight outputs transmit data received from either the register files or the receive FIFOs.
[3:0]pkt_rdy	Output	HIGH	**Packet Ready**. When the W722 asserts this signal, it indicates that one of the four receive FIFOs contains valid data. The application reads the data through the [7:0]pd bus.
full_spden	Input	—	**USB Full Speed Enable.** The application module sets this pin to “1” to select full-speed operation and “0” to select low-speed operation.
setup_rdy	Output	HIGH	**Setup Ready.** Asserting this signal HIGH indicates an 8-byte SETUP data sequence has been received from the USB bus.
iso_err	Output	HIGH	**Isochronous Error.** Used for loopback testing or to indicate isochronous data has been received with DATA1 PID.
validsof	Output	HIGH	**Valid SOF**. This signal is asserted for two bit times, asynchronous to sys_clock, and indicates a valid SOF token is received when asserted HIGH.
sel_ext_pll	Input	HIGH	**Select External PLL**. Asserting this signal HIGH selects the external PLL option.
testmode	Input	HIGH	**Testmode**. Asserting this signal invokes a loopback test mode.

FIFO Interface

Signal	Type	Assertion	Description
[7:0]trx_out_data	Input	—	**Transmit FIFO(s) data output**. Output data from the transmission RAM selected for reading.
[7:0]rcv_out_data	Input	—	**Receive FIFO(s) data output**. Output data from the receiving RAM selected for reading.
[7:0]trx_in_data	Output	—	**Transmit FIFO(s) data input**. Input data to all transmission RAMs.
[2:0]trx_sel	Output	HIGH	**Transmit FIFO(s) select**. Selects one of the seven transmission RAMs for reading.
[8:0]trx_wr_ptr	Output	—	**Transmit FIFO(s) write pointer**. Write address to all transmission RAMs.
[8:0]trx_rd_ptr	Output	—	**Transmit FIFO(s) read pointer**. Read address to all transmission RAMs.
[6:0]trx_wrb	Output	LOW	**Transmit FIFO(s) write strobe**. Write enable. One bit per transmission RAM.
[7:0]rcv_in_data	Output	—	**Receive FIFO(s) data input**. Input data to all receiving RAMs.
[2:0]rcv_sel	Output	HIGH	**Receive FIFO(s) select**. Selects one of the seven receiving RAMs for reading.
[8:0]rcv_wr_ptr	Output	—	**Receive FIFO(s) write pointer**. Write address to all receiving RAMs.
[8:0]rcv_rd_ptr	Output	—	**Receive FIFO(s) read pointer**. Read address to all receiving RAMs.
[6:0]rcv_wrb	Output	LOW	**Receive FIFO(s) write strobe**. Write enable. One bit per receiving RAM.

DPLL Interface

Signal	Type	Assertion	Description
osc_clk	Input	–	**Oscillator Clock**. Attach a 48-MHz clock signal for full-speed operation or a 6-MHz clock signal for low-speed operation.
usb_clk_ext	Input	–	**USB Clock External**. This is the output clock signal from an external DPLL. This clock should run at 12 MHz for full-speed operation or 1.5 MHz for low-speed operation. If an external DPLL is not used, this pin should be connected to VDD or GND.
usb_rxd_out	Output	–	**Synchronized USB Differential Received Data**. This signal comes from the USB differential receiver and is synchronized with the oscillator input. This signal connects to the external DPLL if it is used.

FUNCTIONAL DESCRIPTION

The W722 provides Oki's SIE, a HCC, a HR, and a status/descriptor/register file block in four highly integrated submodules. The submodule partitioning allows custom configurations to be easily developed. Oki also offers optional USB FIFO Controller and Application Interface Logic Modules to form a USB Compound Device function.

Serial Interface Engine

Oki's SIE handles the USB communication protocol and performs:

- Clock generation
- Packet sequencing
- Signal generation/detection
- CRC generation/checking
- Bit-stuffing
- PacketID generation/decoding

When the W722 is in a compound device application, the Oki SIE can be shared by both the Hub function and the embedded function.

Core Controller

The HCC includes:

- A request parser to interpret the host requests/tokens to both the default Endpoint 0 and the Status Change Endpoint 1.
- A (DMA) controller/pointer block, which is capable of handling aborts and retries, to handle data movement from/to the status descriptor memory and the register file.
- A parallel read/write interface to a customer's microcontroller.
- Optional control state machines to execute requests, respond to tokens, and handle errors if customers choose not to use a microcontroller.

Repeater

The HR includes:

- Repeater logic to manage connectivity on a per packet basis. It can handle any combination of full-speed and low-speed devices at the downstream ports. It also supports exception handling, such as fault recovery, suspend/resume as directed by the Host, and remote-wakeup and Frame timer synchronization.
- Four-port state machines which can interpret and respond to bus events, such as connect/disconnect detection, port enable/disable, suspend/resume, reset, and power switching.
- The power manager and central clocking circuitry.

Port State Machine

The port state machine logic can be implemented as an external port, or an internal port for communication with an embedded function. To expand the Hub Megamacro function, additional port state machine functional blocks can be added.

Descriptors

The Descriptors/Status/Register File block includes standard and hub descriptors, hub and port status, and the register file to store all control and status information.

FIFO Control

The FIFO controller/application interface block:

- Manages all first-in/first-out (FIFO) operations for the embedded functions
- Provides a parallel read/write interface to the customer's application
- Supports up to eight asynchronous FIFOs (four transmit and four receive).

The FIFOS can be configured as described in the table below.

FIFO Configuration

FIFO Type	Endpoint Address	Programmable (bytes)	Function
Transmit	0	64	Control transfers
Transmit	5	64	Interrupt and bulk transfers
Transmit	6	64	Interrupt and bulk transfers
Transmit	7	2K	Isochronous, interrupt, and bulk transfers
Receive	0	64	Control transfers
Receive	1	64	Bulk transfers
Receive	2	64	Bulk transfers
Receive	3	2K	Isochronous and bulk transfers

Endpoint 3 and 7 are two-level FIFOs that support up to two separate data sets of variable sizes. All FIFOs have flags that detect full and empty conditions and have the capability of retransmitting or re-receiving the current data set. The FIFO controller logic can be customized to support various FIFO/endpoint requirements.

USB Interface

The W722 connects to the USB via Oki's USB transceiver. The USB-specific input/output (I/O) converts the W722's internal unidirectional signals into USB-compliant signals. The USB Transceiver allows the designer's application module to interface with the physical layer of the USB. By controlling the select signal, the USB is capable of transmitting and receiving serial data at both full-speed (12 Mbps) and low-speed (1.5 Mbps) data rates.

GLOSSARY

Term	Explanation
Bandwidth	The amount of data transmitted per unit of time, typically bits per second (bps) or bytes per second (Bps).
Bit	A unit of information used by digital computers. Represents the smallest piece of addressable memory within a computer. A bit expresses the choice between two possibilities and is typically represented by a logical one (1) or zero (0).
Bit Stuffing	Insertion of a “0” bit into a data stream to cause an electrical transition on the data wires which allows a PLL to remain locked.
Bulk Transfer	Nonperiodic, large burst communication typically used for a transfer that can use any available bandwidth and also be delayed until bandwidth is available.
Control Transfer	One of four Universal Serial Bus Transfer Types. Control transfers support configuration/command/status type communications between client and function.
CRC	See Cyclic Redundancy Check.
Cyclic Redundancy Check	A check performed on data to see if an error has occurred in transmitting, reading, or writing the data. The result of a CRC is typically stored or transmitted with the checked data. The stored or transmitted result is compared to a CRC calculated for the data to determine if an error has occurred.
Device Endpoint	A uniquely identifiable portion of a Universal Serial Bus device that is the source or sink of information in a communication flow between the host and device.
Endpoint	See Device Endpoint.
Interrupt Transfer	One of four Universal Serial Bus Transfer Types. Interrupt transfers characteristics are small data, nonperiodic, low frequency, bounded latency, device initiated communication typically used to notify the host of device service needs.
Isochronous Transfer	One of four Universal Serial Bus Transfer Types. Isochronous transfers are used when working with isochronous data. Isochronous transfers provide periodic, continuous communication between host and device.
Nonreturn-to-Zero-Invert	A method of encoding serial data in which ones and zeroes are represented by opposite and alternating high and low voltages where there is no return to zero (reference) voltage between encoded bits. Eliminates the need for clock pulses.
NRZI	See Nonreturn-to-Zero-Invert.
PLL	Phase-Locked-Loop. A circuit that acts as a phase detector to keep an oscillator in phase with an incoming frequency.
Protocol	A specific set of rules, procedures, or conventions relating to format and timing of data transmission between two devices.
Transaction	The delivery of service to an endpoint. Consists of a token packet, optional data packet, and optional handshake packet. Specific packets are allowed or required based on the transaction type.
Transfer	One or more bus transactions to move information between a software client and its function.
Transfer Type	Determines the characteristics of the data flow between a software client and its function. Four transfer types are defined: control, interrupt, bulk, and isochronous.
Universal Serial Bus	A collection of Universal Serial Bus devices and the software and hardware that allow them to connect the capabilities provided by functions to the host.
Universal Serial Bus Interface	The hardware interface between the Universal Serial Bus cable and a Universal Serial Bus device. This includes the protocol engine required for all Universal Serial Bus devices to be able to receive and send packets.
USB	See Universal Serial Bus.

APPENDIX

0.5 µm MSM13R0000 SOG
and MSM98R000 CSA
USB I/O
Library Data Sheets

The following section contains USB I/O library data sheets

References

See the *USB Specification Revision 1.0* for more information on USB functionality.

Oki Regional Sales Offices

Northwest Area
785 N. Mary Avenue
Sunnyvale, CA 94086
Tel: 408/720-8940
Fax: 408/720-8965

Southwest Area
2302 Martin Street
Suite 250
Irvine, CA 92715
Tel: 714/752-1843
Fax: 714/752-2423

North Central Area
17177 N. Laurel Park Drive
Suite 433
Livonia, MI 48152
Tel: 313/464-7200
Fax: 313/464-1724

South Central Area
2007 N. Collins Blvd.
Suite 303
Richardson, TX 75080
Tel: 214/690-6868
Fax: 214/690-8233

Northeast Area
138 River Road
Shattuck Office Center
Andover, MA 01810
Tel: 508/688-8687
Fax: 508/688-8896

Southeast Area
1590 Adamson Parkway
Suite 220
Morrow, GA 30260
Tel: 404/960-9660
Fax: 404/960-9682

OKI WEB SITE:
http://www.okisemi.com

OKIFAX SERVICE:
Call toll free 1-800-OKI-6994

Oki Stock No:

Oki Semiconductor

Corporate Headquarters
785 N. Mary Avenue
Sunnyvale, CA 94086-2909
Tel: 408/720-1900
Fax: 408/720-1918